Ph.D.Dissertation

Design of PAM-4 Receiver with Baud-Rate Phase Detector

보우-레이트 위상 검출기를 활용한

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by

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August, 2023

Department of Electrical and Computer Engineering
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Design of PAM-4 Receiver with Baud-Rate Phase Detector

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Abstract

In this thesis, design techniques of phase detection in clock and data recovery (CDR) are proposed. For the robust operation, a transition-weighted technique assigning a different gain to detected transitions is utilized. The analysis of performances such as phase detection characteristics and jitter tolerance (JTOL) is provided and demonstrated by the measurement results. Furthermore, an asymmetric-weighted phase detector (PD) with a digital implementation is proposed for robust CDR operation when adopting multilevel signaling.

At first, a programmable PD for the Baud-rate CDR in four-level pulse amplitude modulation (PAM-4) quarter-rate receiver is presented using a transition-weighted gain (TWG) technique. By assigning a different gain to the phase detection for each data-level transition, the TWG-based CDR (TWG-CDR) achieves stable CDR and jitter-tracking operation. An optimal phase detection transfer characteristic is obtained by assigning the highest weight on the 1-level data transition and the lowest on the 3-level transition. The proposed CDR fabricated in 40 nm CMOS technology performs at 64-Gb/s in PAM-4. The measured JTOL shows that the TWG-CDR improves the horizontal eye opening margin compared to the sign-sign Mueller-Müller CDR (SS-MMCDR). The TWG-CDR tested around a 6dB loss channel achieves a BER less than 10^{-11} and energy efficiency of 2.37 pJ/b.

For a more robust operation of a PAM-4 Baud-rate CDR, an asymmetric-weighted PD is proposed. The asymmetric-weighted PD minimizes pattern-dependent jitter and maximizes transition density by utilizing both full-swing transi-

tions and non-full-swing transitions. Based on the pseudo-linear analysis of the conventional scheme and the proposed scheme, an improvement in jitter tracking ability is shown and measured. Furthermore, an asymmetric-weighted technique can be adjusted to CDRs in other multilevel signalings, such as PAM-8. The CDR fabricated in 28 nm CMOS consumes 66 mW at 40 Gb/s and occupies an active area of 0.169 mm^2.

Keywords : Asymmetric weight, Baud-rate, clock and data recovery (CDR), data level (dLev), four-level pulse amplitude modulation (PAM-4), jitter tolerance (JTOL), Mueller-Müller CDR (MMCDR), phase detector (PD), receiver, transition density, transition weighted gain (TWG),

Student Number : 2019-24946

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Chapter 1

Introduction

1.1 Motivation

As the required data rate increases in wireline communication, many applications have adopted multilevel signaling, such as a four-level pulse amplitude modulation (PAM-4), instead of single-level signaling, such as non-return-to-zero (NRZ). However, the change from NRZ signaling to PAM-4 signaling causes some critical issues in clock and data recovery (CDR). Therefore the study of CDR in PAM-4 has increased.

Fig. 1.1 is the trend of the receiver paper published for the last 5 years [2], [4], [5], [21], [22], [28]-[62]. It is divided into NRZ and PAM-4 according to the signaling method, and PAM-4 can be divided into receivers that do not use an analog-to-digital converter (ADC) and receivers that use it. Research on multilevel signaling

such as PAM-4, which can carry more data on the same bandwidth, has been increased. With higher data rates required, the Baud-rate CDRs are preferred, which is less burdensome for multi-phase clock generation. In particular, the ADC-based receiver uses Baud-rate CDRs because it already uses enough multi-phase clocks due to time-interleaving.

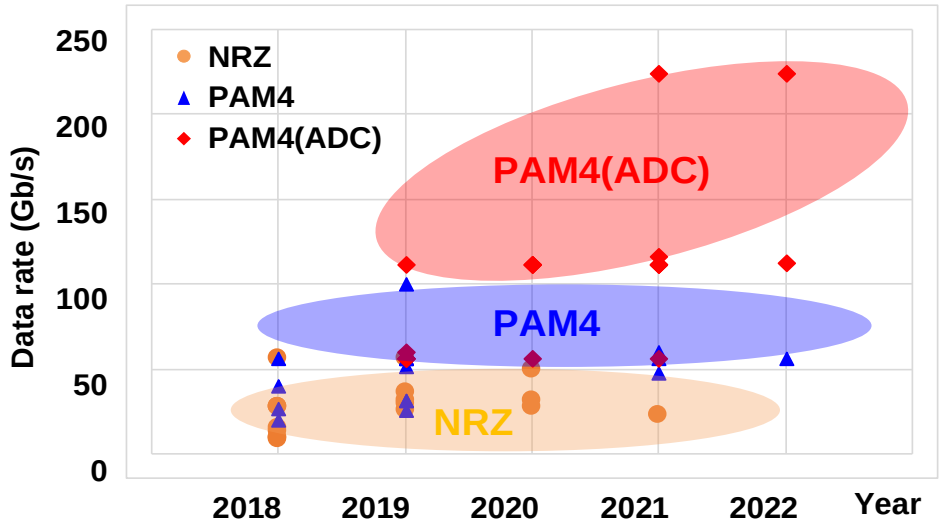


Fig. 1.1 Trend of the modulation methods for recent publications.

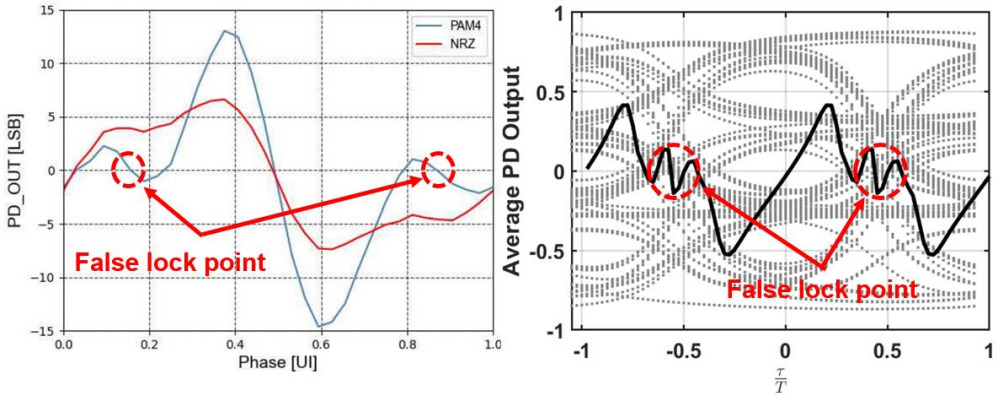


Fig. 1.2 False lock prolbem when adopting PAM-4 signaling.

Many papers on PAM-4 Baud-rate CDRs have been published, and there are problems that do not occur with PAM-4 2x-oversampling CDRs. Fig. 1.2 [22], [23] are false lock problems that occur with PAM-4 Baud-rate CDRs that were recently published in the paper. Compared to NRZ, the inter-symbol interference(ISI)-affected PAM-4 does not have a big problem with PD characteristics in the open eye area. However, when the phase error is large enough, the ambiguous boundary between the PD gain curve's “early” or “late” can occur. If the correct lock point is not obtained due to a false lock problem, it will affect performance such as receiver bit error rate (BER) degradation. The CDR with the transition-weighted PD (TWG-PD) is presented to resolve the false lock problem.

Also, there is a jitter problem with different lock points depending on the data pattern. Fig. 1.3 [12] shows the location of the threshold crossings in 2x-oversampling CDRs, leading to jitter. Assuming a uniform random pattern, a lock point is obtained at the middle of the lock points. Generally, the data pattern with the lock point is defined as a symmetric transition, and other data patterns with other

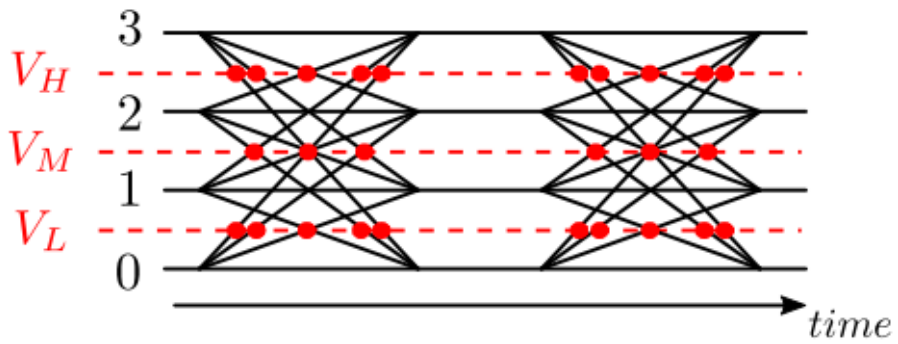


Fig. 1.3 Multi zero-crossing problem in PAM-4 2x-oversmapling CDR.

lock points are defined as an asymmetric transition. The decision to use or not use asymmetric transitions is a critical issue in PAM-4 CDR. Since a similar problem is investigated in PAM-4 Baud-rate CDR, we propose the asymmetric-weighted phase detection technique to resolve the problem.

1.2 Thesis Organization

This thesis is organized as follows. In Chapter 2, the backgrounds of PAM-4 Baud-rate CDR are explained. The basic operation and building blocks of multilevel amplitude modulation, equalizers, and CDRs are provided. And the necessity of improved PD is introduced. To resolve the problem described in the motivation, the comparison and limitations of the previously proposed phase acquisition schemes are presented.

In Chapter 3, a TWG-CDR assigning a different weight according to the type of transition is presented. The proposed phase detection scheme considers phase detection characteristics because of the not-detected region, leading to the false lock problem. All possible transitions in PAM-4 are investigated, and the PD gain curve is adjusted by assigning a different weight to each transition. The effect of TWG-PD is analyzed, and the PD gain curve is obtained. Then, the circuit implementation is explained, and the measurement results are shown.

In Chapter 4, an asymmetric-weighted phase detection technique is presented. Different from Chapter 2, degradation in jitter tracking ability is improved by assigning the different weights to a PD's “early” or “late” output. This technique is used only for transitions, recognized as a jitter at the major lock point. The analysis is based on the pseudo-linear analysis to model the non-linear bang-bang PD (BB-PD). Then, the circuit implementation is explained, and the measurement results are shown.

Chapter 5 summarizes the proposed works and concludes this thesis.

Chapter 2

Backgrounds

2.1 Basic Architecture in Serial Link

2.1.1 General Considerations

Transmission is generally divided into two types, parallel transmission and serial transmission according to the data transmission method. As shown in Fig. 2.1, parallel transmission simultaneously sends many bits through several channels and is faster than serial transmission. However, the cost is high since many pins and channels are required to transmit simultaneously. In addition, because multiple channels are used, problems such as skew and crosstalk occur. As a result, parallel transmission is used only for short channels and unsuitable for long channels.

On the other hand, in the serial link in Fig. 2.2, parallel data is serialized in the

transmitter and transmitted to the receiver through the channel. The receiver deserializes the received serial data for parallel processing. Since data is transferred through one pin and channel, there is no problem with skew and crosstalk. Although bandwidth overhead becomes very large compared to parallel transmission, a serial link recently becomes the preferred interface in high-speed transmission because the overall cost is very low. These are known as SerDes, with examples of Ethernet, optical fiber, PCIe, SONET, etc. As many applications require much more information than before, the data rate of serial communication has increased to satisfy this demand. For example, PCIe Gen 4.0, running at 16 Gb/s, is moving to Gen 5 of the specification running at 32 Gb/s. The channel and interconnects could consist of cables, a printed circuit board (PCB), connectors, vias, and backplanes.

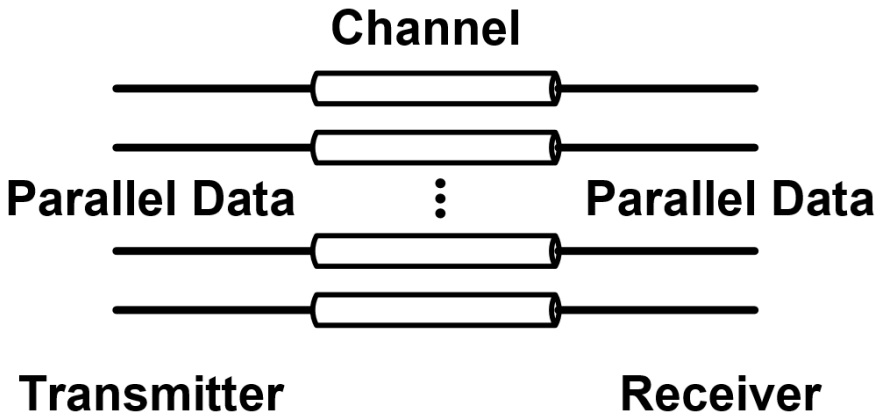


Fig. 2.1 Architecture of parallel link.

Some design issues increase as high data bandwidth is required for the chip-to-chip interface between chiplets. For example, an equalizer is an architecture to compensate for the bandwidth-limiting channel response. However, it becomes difficult to design the equalizer as the required bandwidth increases. As a result, a new approach such as multilevel signaling is needed. For example, four-level pulse amplitude modulation (PAM-4) offers a doubled data rate with the same bandwidth. However, the change from non-return-to-zero (NRZ) to PAM-4 causes some critical issues in clock and data recovery (CDR) because diverse patterns disturb the robust performance of CDR, which does not exist in NRZ.

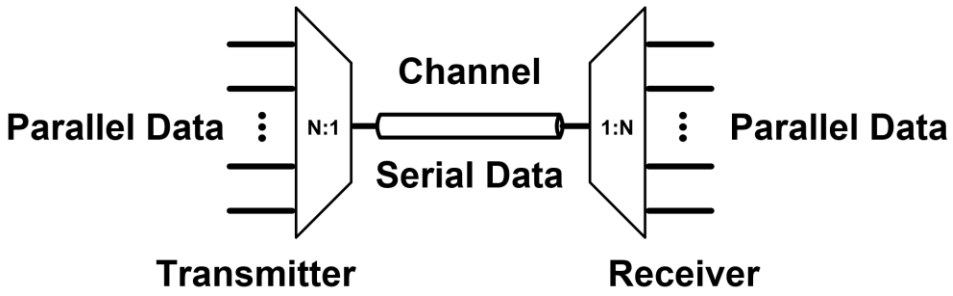


Fig. 2.2 Architecture of serial link.

2.1.2 Equalizer

In a serial link, an equalizer is a signal processing technique used to mitigate the effects of channel distortion and noise. A serial link is a communication channel that transmits data sequentially over a single signal path, such as a wire or fiber optic cable. The signal transmitted over a serial link can be degraded by several factors, including attenuation, noise, and ISI, resulting in errors in the received data. An equalizer is a circuit used to compensate for the distortions introduced by the channel. It works by adjusting the amplitude and phase of the received signal to improve the signal-to-noise ratio (SNR) and reduce ISI. Equalizers can be implemented using various techniques. For example, the representative equalizers used in a receiver are a continuous time linear equalizer (CTLE) and a decision feedback equalizer (DFE).

CTLE is an equalizer used in high-speed digital communication systems to compensate for the attenuation dependent on frequency. It is a linear equalizer that removes unnecessary frequency components and acts as a high pass filter to compensate for the distortion in low frequency by channel. While two types of CTLE, passive RC CTLE and active CTLE, can be used, active CTLE is generally preferred to adjust the zero and pole frequency, which sets peaking and DC gain. Fig. 2.3(a) shows the schematic of the conventional active CTLE. The transfer function of CTLE is described as

$$\mathrm{H(s)} = G_{DC}\frac{(s+\omega_z)}{(s+\omega_{p1})(s+\omega_{p2})} \tag{2.1}$$

where G_{DC} is the DC gain of CTLE. ω_z is the zero frequency decided by the degeneration resistor and capacitor. ω_{p1} is the first pole frequency decided by the degeneration resistor, capacitor and transconductance g_m of a driving transistor. And ω_{p2} is the second pole frequency decided by the load resistor and parasitic capacitor of output, which is the main reason for degrading the bandwidth of CTLE. Overall parameters are obtained as

$$\mathrm{G}_{DC} = \frac{\mathrm{g}_m \mathrm{R}_{LOAD}}{1 + \mathrm{g}_m \mathrm{R}_C/2}, \omega_z = \frac{1}{\mathrm{R}_C \mathrm{C}_C}, \omega_{p1} = \frac{1 + \mathrm{g}_m \mathrm{R}_c/2}{\mathrm{R}_C \mathrm{C}_C}, \omega_{p2} = \frac{1}{\mathrm{R}_{LOAD} \mathrm{C}_{LOAD}} \quad (2.2)$$

While CTLE provides gain and equalization with good power and area overhead and can cancel pre-cursor and long tail post-cursor ISIs, there are some problems. CTLE amplifies noise and crosstalk as well as the main signal, resulting in a limit of

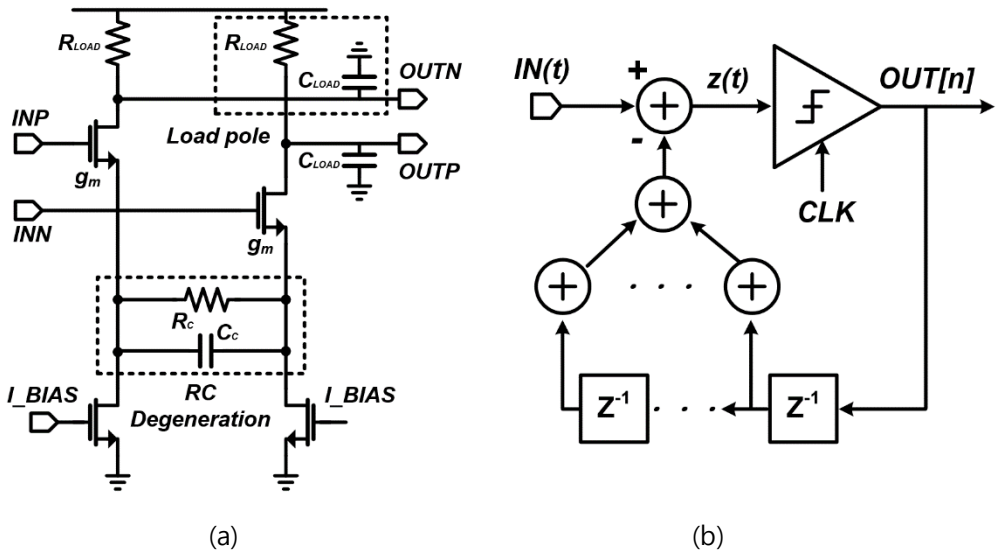


Fig. 2.3 (a) Schematic of the CTLE, and (b) block diagram of the DFE.

amplifying. To reduce the overload of CTLE, DFE is generally used after CTLE. DFE is a non-linear equalizer, which is different from a linear equalizer, CTLE. Fig. 2.3(b) shows a block diagram of the DFE. The DFE is composed of decision blocks (samplers) and feedback filters. The sampler outputs the determined value, 1 or -1, multiplied by a tap coefficient. Using a feedback FIR filter, all post-cursor ISIs can be directly subtracted from the incoming signal, IN(t). Since the DFE is a non-linear equalizer, it can boost high frequency components without amplifying the noise and crosstalk. Although it cannot cancel any pre-cursor ISI, all post-cursor ISIs can be removed using feedback FIR filters. However, if the feedback timing constraint is not satisfied, post-cursor ISI cannot be canceled properly. The feedback loop should settle before the following sampling timing. Therefore, reducing the feedback time is an important issue in adopting the DFE in the receiver. Generally, feedback time consists of a C-to-Q delay, setup time of the sampler, and settling time at the summing node. Since the feedback time to cancel the first post-cursor ISI is the shortest, the critical path delay should be less than one unit interval (UI) as shown in Fig. 2.4.

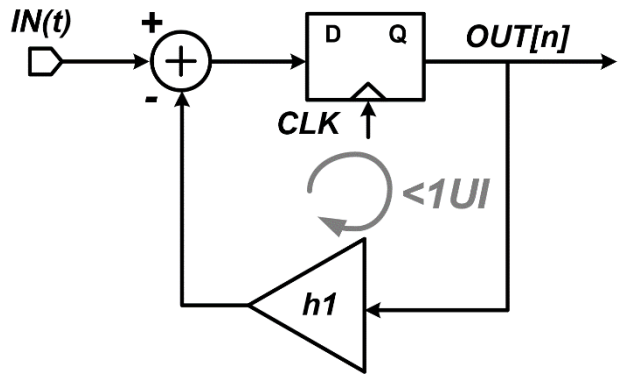


Fig. 2.4 Feedback timing constraint of DFE.

2.1.3 Pulse-Amplitude Modulation

As mentioned in 2.1.1, the design of the equalizer also came to a limit, and multi-level pulse amplitude modulation (PAM) was suggested as a new method. PAM is a type of signal modulation that encodes message information using the amplitude of a series of signal pulses. This modulation technique is analog and involves varying the amplitudes of a series of carrier pulses based on the sample value of the message signal. To demodulate the signal, the amplitude level of the carrier is detected during each period.

NRZ, which is generally used, is two-level pulse amplitude modulation (PAM-2) signaling. NRZ represents digital bits as two levels, +1 and -1. In contrast, PAM-4 uses four levels to represent two bits, +3, +1, -1, and -3. Since the PAM-4 signaling transmits two bits per symbol, while NRZ signaling transmits one bit per symbol, PAM-4 signaling offers a doubled data rate with the same bandwidth. As shown in Fig. 2.5, the eye height of PAM-4 in the eye diagram per UI is 1/3 of the eye height of NRZ, thus SNR is degraded. However, the horizontal eye of PAM-4 is twice the horizontal eye of NRZ assuming the same data rate. For example, assume there is a data pattern, 0111000110110100, with 64 Gb/s data transmission in Fig. 2.6. In PAM-4, the pattern is divided into a most significant bit (MSB) and a least significant bit (LSB) every two bits. The four electrical levels are 01, 11, 00, 01, 10, 11, 01, and 00. The Nyquist frequency of the channel is 32 GHz for NRZ signaling and 16 GHz for PAM-4 signaling. 1 UI in PAM-4 is 31.25ps, and 15.625ps is obtained in NRZ.

However, PAM-4 signaling requires more complex modulation/demodulation

techniques. Also, since it has much more diverse data patterns than NRZ signaling, the design of CDR is essential.

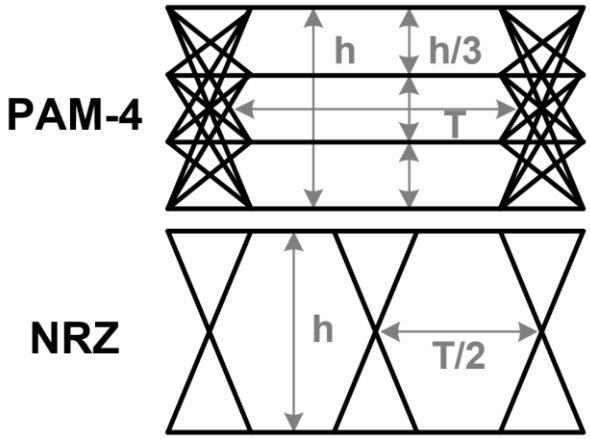


Fig. 2.5 Eye diagram of NRZ and PAM-4.

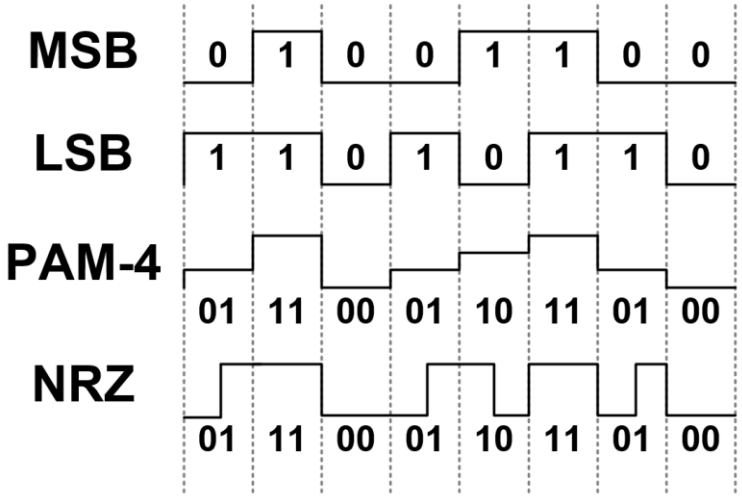


Fig. 2.6 Data pattern example of NRZ and PAM-4.

2.1.4 Clock and Data Recovery

A CDR is an essential circuit for timing recovery between the received symbols and sampling clock to get a low BER. In digital communication systems, the transmitter sends data using a clock signal. The receiver needs to recover and use this clock signal to sample and interpret the data signal correctly. However, the clock signal can become distorted or lost during transmission due to various factors such as transmission noise, distortion, and frequency drift. A CDR circuit helps recover the clock signal by using the incoming data signal to generate a new clock signal synchronized with the data signal. Then, the circuit samples the incoming data signal at the correct time using this recovered clock signal, which enables accurate data recovery.

There are various types of CDR circuits available, which are generally divided into two, 2x-oversampling PD (Alexander PD) and Baud-rate PD. These circuits operate by adjusting the phase or delay of the clock signal until it aligns with the incoming data signal. CDR circuits are commonly used in high-speed communication systems such as fiber-optic communication, Ethernet, and USB. They play a critical role in ensuring accurate and reliable data transmission over long distances and in noisy environments.

2.2 Phase Acquisition

2.2.1 2x-oversampling PD (Alexander PD)

The 2x-oversampling PD needs two samplers per one data time interval for phase relation between data and clock. The alexander PD is the most widely used for robust operation using a data sampler and an edge sampler. Fig. 2.7 shows the operation of the alexander PD. The alexander PD is based on two successive data samples (D[n−1] and D[n]) and an edge sample (E[n]). Since data samples and an edge sample is simultaneously needed, multi-clock generation (twice in this case) is essential. The relation between the data sample and the edge sample generates “Early” and “Late” signals. “Early” means the sampling clock is leading, and “Late” means the sampling clock is lagging.

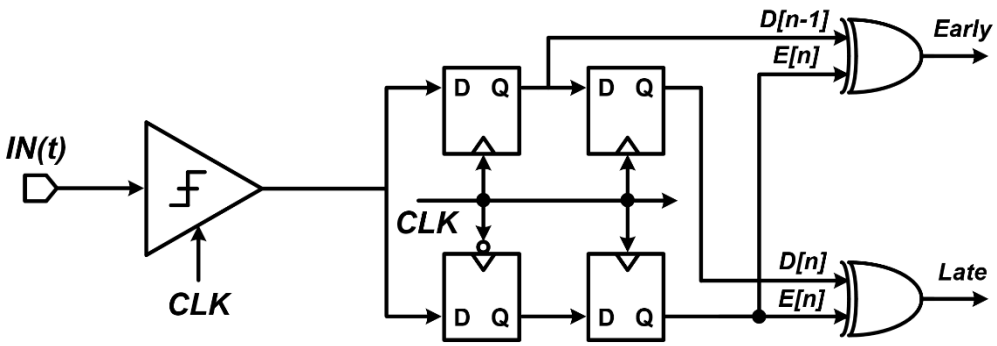
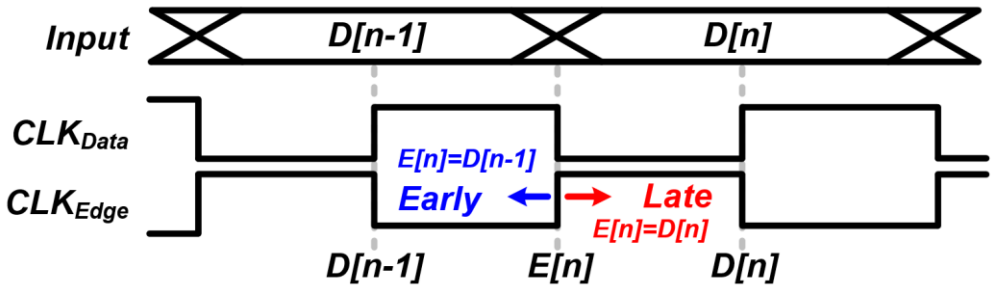


Fig. 2.7 Implementation of an alexander PD.

Fig. 2.8 shows the operating principle of the alexander PD. Firstly, if any data transition is not detected, both “Early” and “Late” are not obtained. However, if data transition is detected, either “Early” or “Late” is output because D[n−1] and D[n] are not the same, and E[n] is the same as one of them. As shown in Fig. 2.8, when the sampled output at the edge E[n] is the same as the previous data D[n−1], PD output is "Early". In the same way, "Late” is output when the edge sample and the following data are the same. As a result, the alexander PD locks at the zero crossing point, where $h_{-1/2} = h_{1/2}$.



Pattern			PD output
D[n-1]	E[n]	D[n]	
-1	-1	+1	Early
-1	+1	+1	Late
+1	-1	-1	Late
+1	+1	-1	Early
Other cases			Hold

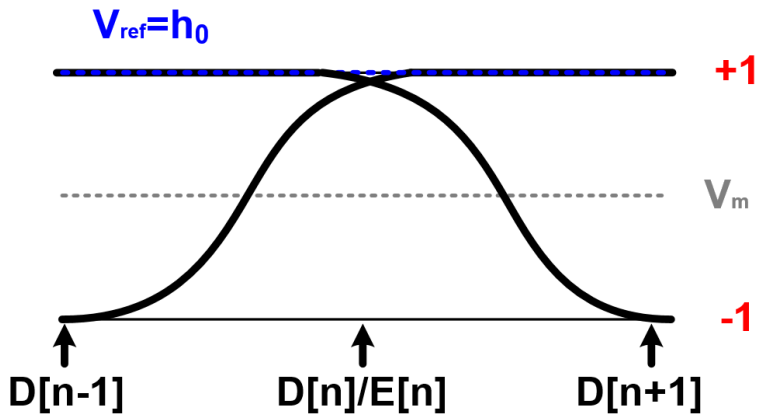
Fig. 2.8 Principle of alexander PD including “Early”, “Late”, and “Hold”.

Since the alexander PD has a robust phase detection characteristic, it has been commonly adopted. However, as the required data rate increases, the overload of a multi-phase clock generation also increases, leading to the adoption of Baud-rate PD.

2.2.2 Baud-rate PD

Since the Baud-rate PD needs only one data sampler per one data time interval, the overhead of multi-phase clock generation is reduced. Instead of edge samplers, additional error samplers sampled by the data clock are adopted. It can result in a simpler PD circuit, lower power consumption, and lower cost than 2x-oversampling PD. Mueller-Müller PD (MMPD) is a representative Baud-rate PD.

Fig. 2.9 shows the operation of the MMPD with one error sampler [24]. For the rising transition, the three successive data $D[n-1]/D[n]/D[n+1]$ is -1/+1/+1. The signal level, including ISIs, is decided as $h_0 + h_{-1} - h_1$. Since the reference level of



Pattern				PD output
D[n-1]	D[n]	D[n+1]	E[n]	
-1	+1	+1	-1	Early
-1	+1	+1	+1	Late
+1	+1	-1	-1	Late
+1	+1	-1	+1	Early

Fig. 2.9 Principle of the MMPD with one error sampler.

the error sampler is h_0, the lock point of the rising transition is obtained at $h_{-1} = h_1$. When the $E[n]$ is -1, “Early” is output because it means $h_{-1} < h_1$. In the same way, “Late” is output when the $E[n]$ is +1. However, PD output is inversed in the falling transition. The signal level of falling transition +1/+1/-1, including ISIs, is obtained as $h_0 - h_{-1} + h_1$. The difference between the error sampler's signal level and the reference level in the falling transition shows the opposite sign compared to that in the rising transition. Therefore, “Late” is output when the $E[n]$ is -1, and “Early” is output when the $E[n]$ is +1. To satisfy both the rising transition and the falling transition, the final lock point is obtained at the $h_{-1} = h_1$.

Since the MMPD has a lock point in the relation between the pre-cursor and post-cursor ISI different from the alexander PD, which has a lock point at the zero crossing point, the reference level of the error sampler should be adaptively adjusted before the CDR. Also, as multilevel signaling has been adopted recently, decisions to use various patterns for phase detection are essential issues. The next Chapter follows the specific consideration.

Chapter 3

PAM-4 Receiver with Transition-Weighted Phase Detector

3.1 Overview

In the traditional NRZ receiver, 2x-oversampling CDR is typically employed with the sampling clock phase locked at $h_{-1/2} = h_{1/2}$. However, in PAM-4, zero-crossing times vary with data patterns, causing significant jitter, especially with asymmetric data transitions such as -1 to +3, when using only one edge sampler with the middle threshold. However, eliminating the asymmetric data transitions for phase detection gives worse performance when samplers with three thresholds are used [12] . In other words, three edge samplers are needed to use asymmetric transitions for less injected jitter. A phase-error-dependent BB-PD is proposed for better

tracking capability [5] . However, such 2x-oversampling CDRs are unsuitable in PAM-4 since using an extra clock for edge sampling is difficult. The added hardware and associated power consumption are not justifiable in PAM-4 signalings. A viable solution is to use only data samples to extract phase information obviating the use of edge samplers. Baud-rate CDRs [6] -[7] , [13] are proposed to reduce the overhead of generating an extra clock. However, additional circuits such as integrators [6] , additional error samplers for changing the lock point [7] , or added capacitors for slope detection [13] are used, which limits the bandwidth of the analog front-end, and results in additional power consumption. In the proposed structure, only one error sampler per one data time interval is used to minimize the load capacitance and reduce additional power consumption. Generally, with such BB-type PDs used in PAM-4 Baud-rate CDRs, characteristics of multilevel transitions are not properly considered even though the PD gain varies depending on the amount of jitter, resulting in a varied loop response. In this paper, the transition-weighted gain (TWG) technique is proposed to make the most of the advantages of multilevel transitions. Loop gain adaptation for optimum JTOL is presented in [14] , avoiding underdamped cases. However, it does not offer the optimum JTOL in a specific condition where the magnitude of the jitter varies. TWG technique improves the jitter tracking capability for the large jitter by taking advantage of the nonlinear PD characteristic. The benefits of weighting the PD outputs are confirmed by measuring the loop dynamics and the steady-state jitter performance [8] .

In this Chapter, we present the proposed phase acquisition scheme analyses using all possible transitions in PAM-4 Baud-rate CDR. First, with quantitative analyses, we propose TWG technique to improve the phase acquisition performance. Then,

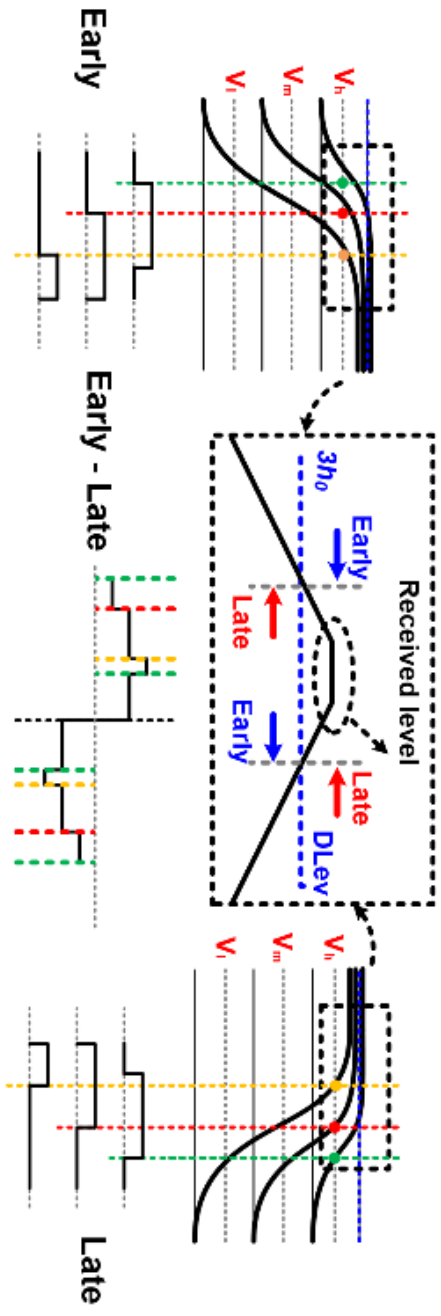
the detailed operation of the phase detector will be described. Finally, the measurement results of the prototype chip show the performance and demonstrate the theoretical analyses.

3.2 Proposed Phase Acquisition

3.2.1 Operation of SS-MM CDR

The Sign-Sign Mueller-Müller (SS-MM) CDR [15] used in binary signaling generally uses two types of information: binary decision data and error polarity from the received signal. However, in PAM-4, since the number of data levels is four, its equivalent phase detection requires three data samplers and four error samplers, whereas only one data sampler and two error samplers are required for the binary signaling. Thus, for practical reasons, we propose a simple, high-speed CDR scheme using only one error sampler that is shared with an adaptive equalizer in addition to three data samplers. The number of detected transitions per edge/error sampler is four in [5] , [6] , three in [7] , and six in the proposed scheme. Denote data levels as +3, +1, -1, and -3 from top to bottom. The threshold of the error sampler, which is commonly called data level (dLev), is set adaptively at the highest data level +3 or $3h_0$, where h_0 denotes the main cursor of the channel response. A typical received signal includes ISI with a pre-cursor h_{-1} and a post-cursor h_1. Since the SS-MM PD relies on ISI, an eventual lock is obtained where $h_{-1} = h_1$. Fig. 3.1 shows typical data transitions in the presence of such ISI. The phase detection table, using two sets of the samples of PAM-4 data and error, asserts either "early", "late", or "neutral" in the proposed PD. Since only one error sample at the +3 level is available, rising edges to the +3 level are examined and produce the output "early" when the error output is -1, and "late" when the error output is +1. In the same way, falling

edges from the +3 level are examined to generate "late" when the error output is -1, and "early" otherwise. When the data has no transition such as, from +3 to +3 level, no timing information is available so neither "early" or "late" is asserted, representing "neutral".



Transition	Rising edges				Falling edges				Weight
	D[n-1]	D[n]	E[n]	PD	D[n]	D[n+1]	E[n]	PD	
1-level	+1	+3	-1/+1	E/L	+3	+1	-1/+1	L/E	W_{1L}
2-level	-1	+3	-1/+1	E/L	+3	-1	-1/+1	L/E	W_{2L}
3-level	-3	+3	-1/+1	E/L	+3	-3	-1/+1	L/E	W_{3L}

Fig. 3.1 Phase detection principle, and PD gain curve considering not detected region.

3.2.2 Proposed Transition-Weighted Gain Technique

The symbolic table entries of "early", "late", or "neutral" logically represent +1, -1, and 0, respectively, and the final output is produced by weighting by W_{1L} when the data transition is from the +1 level to +3, W_{2L} when from the -1 level to +3, and W_{3L} when from the -3 level to +3, respectively.

Table 3.1 shows how the PD outputs are generated with three consecutive samples, the middle one being at the +3 level, according to the PD table shown in Fig. 3.1. Since the middle sample is $D[n] = +3$, only 32 combinations of $D[n-1]$, $D[n+1]$, and $E[n]$ are possible. Symmetric transitions such as +3/+3/+3, +1/+3/+1, -1/+3/-1, and -3/+3/-3 are removed since they bear no phase information since it produces "neutral", which is canceled by "early" and "late" with the same weight. Assuming that the first pre-cursor h_{-1} and the first post-cursor h_1 are positive and the noise is absent, the received levels including ISIs for transitions such as +1/+3/+3 or +3/+3/+1, are always positive, resulting in the error output +1 all the time while an error output of -1 never occurs. In the same way, the error outputs from cases such as -1/+3/-3 or -3/+3/-1 are always -1. Therefore, a total of twenty cases comprise the table. The blue boxes in Table 3.1 are such cases, and PD outputs are not used.

Pattern			Recevied level-V_{ref}	Error	PD output		
D[n-1]	D[n]	D[n+1]	h_{-1}, $h_1 > 0$	E[n]	Early	Late	Early-Late
+1	+3	+3	$3h_{-1}+h_1 > 0$	+1	-	W_{1L}	$-W_{1L}$
-1	+3	+3	$3h_{-1}-h_1 < 0$	-1	W_{2L}	-	W_{2L}
-1	+3	+3	$3h_{-1}-h_1 > 0$	+1	-	W_{2L}	$-W_{2L}$
-3	+3	+3	$3h_{-1}-3h_1 < 0$	-1	W_{3L}	-	W_{3L}
-3	+3	+3	$3h_{-1}-3h_1 > 0$	+1	-	W_{3L}	$-W_{3L}$
+3	+3	+1	$h_{-1}+3h_1 > 0$	+1	W_{1L}	-	W_{1L}
-1	+3	+1	$h_{-1}-h_1 < 0$	-1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
-1	+3	+1	$h_{-1}-h_1 > 0$	+1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
-3	+3	+1	$h_{-1}-3h_1 < 0$	-1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
-3	+3	+1	$h_{-1}-3h_1 > 0$	+1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
+3	+3	-1	$-h_{-1}+3h_1 < 0$	-1	-	W_{2L}	$-W_{2L}$
+3	+3	-1	$-h_{-1}+3h_1 > 0$	+1	W_{2L}	-	W_{2L}
+1	+3	-1	$-h_{-1}+h_1 < 0$	-1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
+1	+3	-1	$-h_{-1}+h_1 > 0$	+1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
-3	+3	-1	$-h_{-1}-3h_1 < 0$	-1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
+3	+3	-3	$-3h_{-1}+3h_1 < 0$	-1	-	W_{3L}	$-W_{3L}$
+3	+3	-3	$-3h_{-1}+3h_1 > 0$	+1	W_{3L}	-	W_{3L}
+1	+3	-3	$-3h_{-1}+h_1 < 0$	-1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
+1	+3	-3	$-3h_{-1}+h_1 > 0$	+1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
-1	+3	-3	$-3h_{-1}-h_1 < 0$	-1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
Other cases			-	-	-	-	-

Table 3.1 PD outputs for all possible transitions in PAM-4

3.2.3 Analysis of PD Characteristics

The overall PD output is calculated as follows, assuming that all the cases in Table 3.1 occur with equal probability.

$$\mathrm{PD_{output}} = \begin{cases} 4(W_{3L}+W_{2L}-W_{1L}), & h_{-1} < h_1/3 \\ 2(W_{3L}+W_{2L}-W_{1L}), & h_1/3 \le h_{-1} < h_1 \\ -2(W_{3L}+W_{2L}-W_{1L}), & h_1 \le h_{-1} < 3h_1 \\ -4(W_{3L}+W_{2L}-W_{1L}), & 3h_1 \le h_{-1} \end{cases} \quad (3.1)$$

Fig. 3.2 shows the PD characteristic curve according to the values of the pre-cursor h_{-1} and the post-cursor h_1, using (3.1). Fig. 3.2(a) shows the case when the sum of the 3-level transition weight W_{3L} and the 2-level transition weight W_{2L} is larger than the 1-level transition weight W_{1L}, that is $W_{3L} + W_{2L} - W_{1L} > 0$. Fig. 3.2(b) shows the cases when the sum is smaller, $W_{3L} + W_{2L} - W_{1L} < 0$. In either case, a lock is reached with the proper polarity inversion in the CDR loop. Green, red, and orange lines in Fig. 3.1 show the boundaries of 1-level, 2-level, and 3-level data transitions that separate an "early" or "late" condition. For the 1-level data transition starting from +1 to +3, "early" is detected when the clock edge is located right after passing the V_h threshold but before passing dLev, $3h_0$, as shown in Fig. 3.1. For the rising transition from -1 or -3, "early" is again detected when the clock edge is located right after the signal passing the V_m or V_l threshold, respectively, and continuously detected as "early" up to the center of the data eye. Therefore, as the phase error increases, an "early" signal disappears in the order of the 3-level, 2-level, and 1-level transitions. To understand the effect of varying weights, the weight ratio

$W_{3L}:W_{2L}:W_{1L}$ of 1:1:1 is analyzed. The phase detection curves show a proper operation in this case. With a small phase error, all three transition cases play a role and contribute to phase detection. However, when the phase error is large, the PD output from 3-level transitions becomes scarce, thereby resulting in a reduced gain. Thus, for the 1:1:1 case, the PD output, $W_{3L}+W_{2L}-W_{1L}=1$, is reduced to $W_{2L}-W_{1L}=0$ with a zero gain. This condition is avoided when the weight ratio $W_{3L}:W_{2L}:W_{1L}$ of 1:2:4 is used instead. For a large phase error, $W_{3L}+W_{2L}-W_{1L}$ is -1, and $W_{2L}-W_{1L}$ is -2, thereby avoiding the zero-gain problem. Note that $W_{3L}:W_{2L}:W_{1L}$ of 1:2:3 does not yield any gain, failing as the PD. When $W_{3L}+W_{2L}<W_{1L}$, the PD is operational with jitter tracking capability, but the PD characteristic in Fig. 3.2(b) exhibits the opposite sign, resulting in the edge lock instead of locking at the center of the data eye. Thus, the inversion of "early" and "late" is necessary. The weight ratio $W_{3L}:W_{2L}:W_{1L}$ is not critical because all other cases satisfying the condition, $W_{3L}+W_{2L}-W_{1L}<0$, would exhibit a similar characteristic. As a result, the 1:2:4 case is chosen to minimize the multiplication overhead by using only shift operations.

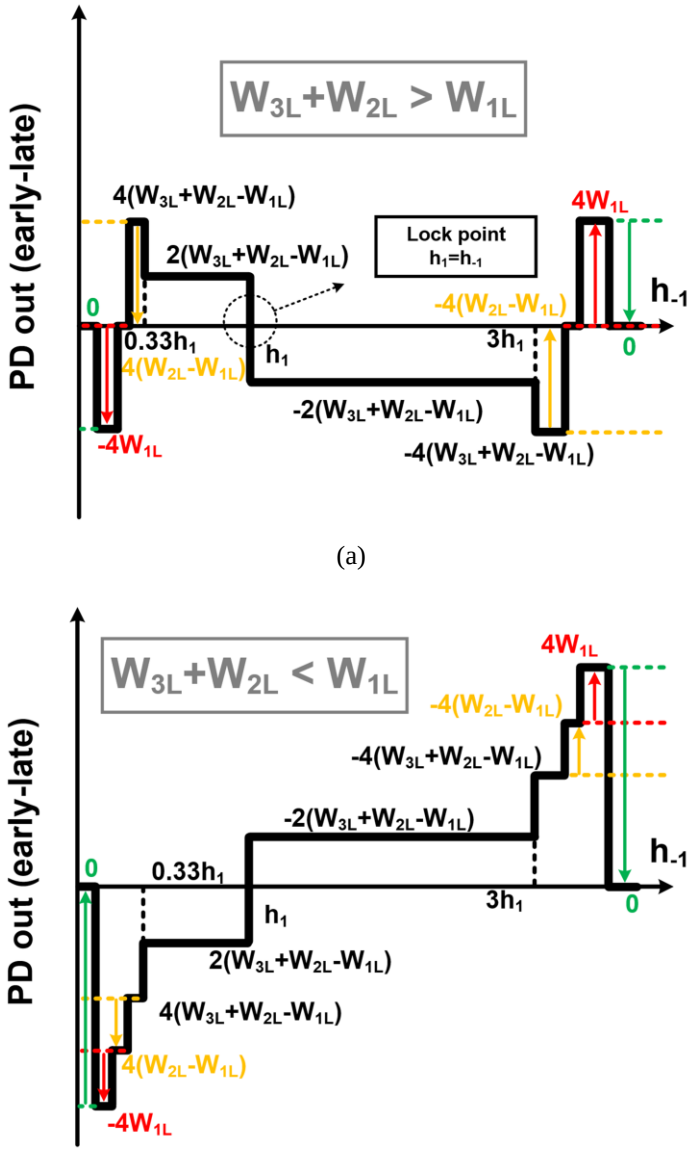
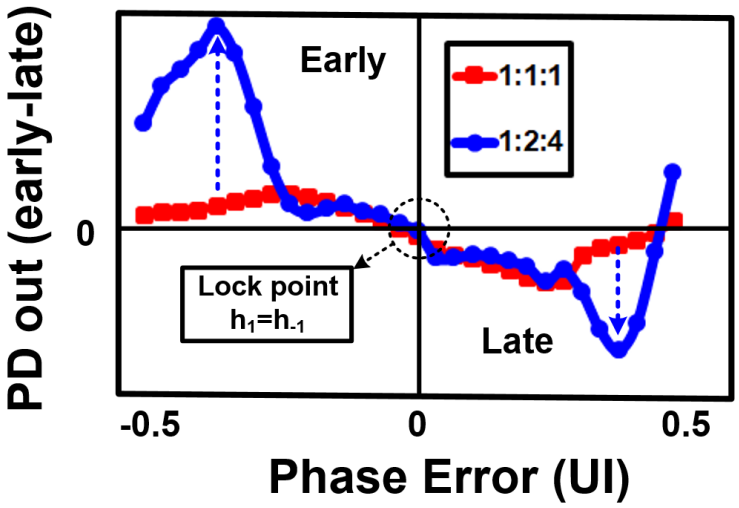
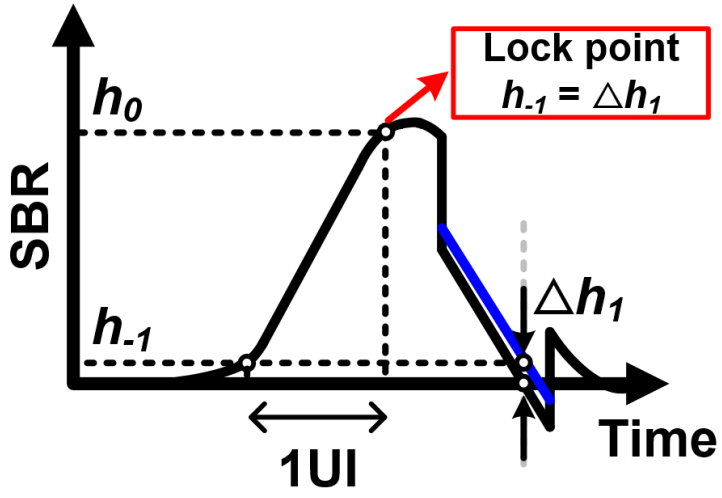


Fig. 3.2 PD characteristics (a) when sum of 2-level and 3-level transition weights is larger than 1-level transition weight and (b) opposite case.

Fig. 3.3(a) shows the simulated PD characteristic for the above-mentioned cases, 1:1:1 and 1:2:4. The PRBS-7 pattern is used with a 7dB loss channel, and a 2-tap DFE is used to match the channel characteristic. Since the DFE drives the post-cursor h_1 to zero as shown in Fig. 3.3(b), the proposed PD continuously generates "early", moving the clock phase toward $h_{-1} = 0$, failing to obtain the lock. To prevent the lock problem when combined with the DFE, a very small post-cursor offset, $\Delta h_1 = 1/20 h_0$, is intentionally added to the first cursor h_1 of the DFE as shown in Fig. 3.3(b). When the phase error is small, the 1:1:1 and 1:2:4 cases have the same PD output. However, they have a strikingly different tendency as the phase error increases. The PD output in the 1:1:1 case starts decreasing when the phase error is increased beyond ±0.25 UI. On the other hand, the 1:2:4 case starts to decrease at ±0.4 UI. Considering the PD characteristic in Fig. 3.2, ±0.25 UI is the expected maximum phase error beyond which the 3-level transition failed to detect. The result shows that the 1-level transition gain $W_{1\mathrm{L}}$ is a dominant parameter for obtaining the jitter tracking ability under the large jitter and maintaining the same gain at the small phase error. Thus, the TWG-CDR offers the stability of the CDR in both cases of small and large jitter.



(a)



(b)

Fig. 3.3 (a) TWG PD gain curve with two cases, when the transition weight ratio W_{3L}:W_{2L}:W_{1L} is 1:1:1 and 1:2:4. (b) small offset introduced in h_1 in DFE to stably lock at $\Delta h_1 = h_{-1}$.

3.2.4 PD Characteristics with Equalizer

The PD characteristics mentioned in 3.2.3 are the most common cases, where both post-cursor and pre-cursor are positive, $h_1 > 0$ and $h_{-1} > 0$. However, using an equalizer does not always satisfy the conditions of $h_1 > 0$ and $h_{-1} > 0$, and thus additional analysis is required. For example, the following is the case of $h_{-1} > 0$ and $h_1 < 0$, and it is considered that the value subtracted by DFE is overboosted.

$$\mathrm{PD_{output}} = \begin{cases} -4(W_{3L}+W_{2L}-W_{1L}), & h_{-1} < -h_1/3 \\ -2(3W_{3L}+W_{2L}-W_{1L}), & -h_1/3 \le h_{-1} < -3h_1 \\ -4(W_{3L}+W_{2L}-W_{1L}), & -3h_1 \le h_{-1} \end{cases} \quad (3.2)$$

(3.2) is an analysis of all possible patterns, as seen in Table 3.2. The PD characteristic is shown in Fig. 3.4.

$$\mathrm{PD_{output}} = \begin{cases} 4(W_{3L}+W_{2L}-W_{1L}), & h_{-1} < -3h_1 \\ 2(3W_{3L}+W_{2L}-W_{1L}), & -3h_1 \le h_{-1} < -h_1/3 \\ 4(W_{3L}+W_{2L}-W_{1L}), & -h_1/3 \le h_{-1} \end{cases} \quad (3.3)$$

(3.3) is the case of $h_{-1} < 0$ and $h_1 > 0$, which can be caused by the de-emphasis of FFE or overboosting of a CTLE. As mentioned earlier, Table 3.3 analyzed all possible patterns as follows: This is the same as Fig. 3.5.

$$\mathrm{PD_{output}} = \begin{cases} 4(W_{3L}+W_{2L}-W_{1L}), & h_{-1} < 3h_1 \\ 2(W_{3L}+W_{2L}-W_{1L}), & 3h_1 \le h_{-1} < h_1 \\ -2(W_{3L}+W_{2L}-W_{1L}), & h_1 \le h_{-1} < h_1/3 \\ -4(W_{3L}+W_{2L}-W_{1L}), & h_1/3 \le h_{-1} \end{cases} \quad (3.4)$$

Finally, the case of $h_{-1} < 0$ and $h_1 < 0$ appears similar to the case of $h_{-1} > 0$ and $h_1 > 0$, where equalizers are overboosted. Similarly, all pattern analyses in Table 3.4 are obtained as (3.4), graphically represented in Fig. 3.6.

Pattern			Recevied level-V_{ref}	Error	PD output		
D[n-1]	D[n]	D[n+1]	$h_{-1} > 0, h_1 < 0$	E[n]	Early	Late	Early-Late
+1	+3	+3	$3h_{-1}+h_1 > 0$	+1	-	W_{1L}	$-W_{1L}$
+1	+3	+3	$3h_{-1}+h_1 < 0$	-1	W_{1L}	-	W_{1L}
-1	+3	+3	$3h_{-1}-h_1 > 0$	+1	-	W_{2L}	$-W_{2L}$
-3	+3	+3	$3h_{-1}-3h_1 > 0$	+1	-	W_{3L}	$-W_{3L}$
+3	+3	+1	$h_{-1}+3h_1 > 0$	+1	W_{1L}	-	W_{1L}
+3	+3	+1	$h_{-1}+3h_1 < 0$	-1	-	W_{1L}	$-W_{1L}$
-1	+3	+1	$h_{-1}-h_1 > 0$	+1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
-3	+3	+1	$h_{-1}-3h_1 > 0$	+1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
+3	+3	-1	$-h_{-1}+3h_1 < 0$	-1	-	W_{2L}	$-W_{2L}$
+1	+3	-1	$-h_{-1}+h_1 < 0$	-1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
-3	+3	-1	$-h_{-1}-3h_1 > 0$	+1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
-3	+3	-1	$-h_{-1}-3h_1 < 0$	-1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
+3	+3	-3	$-3h_{-1}+3h_1 < 0$	-1	-	W_{3L}	$-W_{3L}$
+1	+3	-3	$-3h_{-1}+h_1 < 0$	-1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
-1	+3	-3	$-3h_{-1}-h_1 > 0$	+1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
-1	+3	-3	$-3h_{-1}-h_1 < 0$	-1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
Other cases			-	-	-	-	-

Table 3.2 PD outputs for all possible transitions when $h_{-1}>0$, and $h_1<0$ in PAM-4.

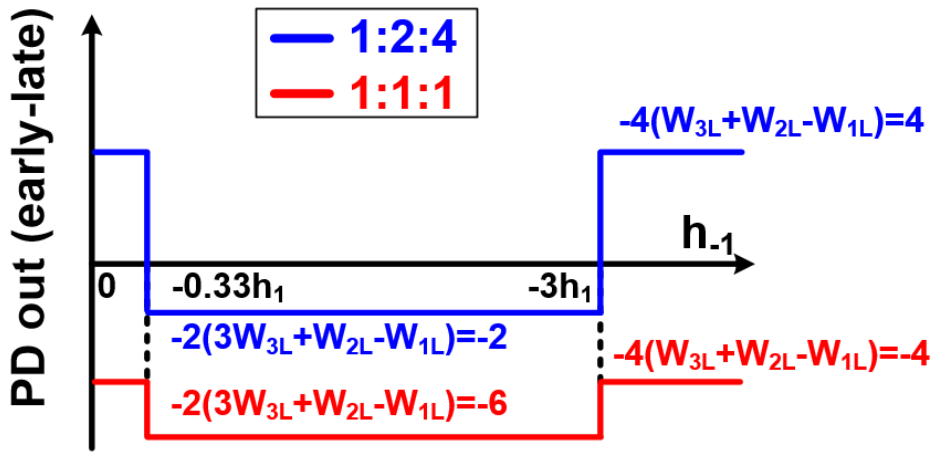


Fig. 3.4 PD characteristics when $h_{-1}>0$, and $h_1<0$ in PAM-4.

Pattern			Recevied level-V_{ref}	Error	PD output		
D[n-1]	D[n]	D[n+1]	$h_{-1} < 0$, $h_1 > 0$	E[n]	Early	Late	Early-Late
+1	+3	+3	$3h_{-1}+h_1 > 0$	+1	-	W_{1L}	$-W_{1L}$
+1	+3	+3	$3h_{-1}+h_1 < 0$	-1	W_{1L}	-	W_{1L}
-1	+3	+3	$3h_{-1}-h_1 < 0$	-1	W_{2L}	-	W_{2L}
-3	+3	+3	$3h_{-1}-3h_1 < 0$	-1	W_{3L}	-	W_{3L}
+3	+3	+1	$h_{-1}+3h_1 > 0$	+1	W_{1L}	-	W_{1L}
+3	+3	+1	$h_{-1}+3h_1 < 0$	-1	-	W_{1L}	$-W_{1L}$
-1	+3	+1	$h_{-1}-h_1 < 0$	-1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
-3	+3	+1	$h_{-1}-3h_1 < 0$	-1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
+3	+3	-1	$-h_{-1}+3h_1 > 0$	+1	W_{2L}	-	W_{2L}
+1	+3	-1	$-h_{-1}+h_1 > 0$	+1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
-3	+3	-1	$-h_{-1}-3h_1 > 0$	+1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
-3	+3	-1	$-h_{-1}-3h_1 < 0$	-1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
+3	+3	-3	$-3h_{-1}+3h_1 > 0$	+1	W_{3L}	-	W_{3L}
+1	+3	-3	$-3h_{-1}+h_1 > 0$	+1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
-1	+3	-3	$-3h_{-1}-h_1 > 0$	+1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
-1	+3	-3	$-3h_{-1}-h_1 < 0$	-1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
Other cases			-	-	-	-	-

Table 3.3 PD outputs for all possible transitions when $h_{-1}<0$, and $h_1>0$ in PAM-4.

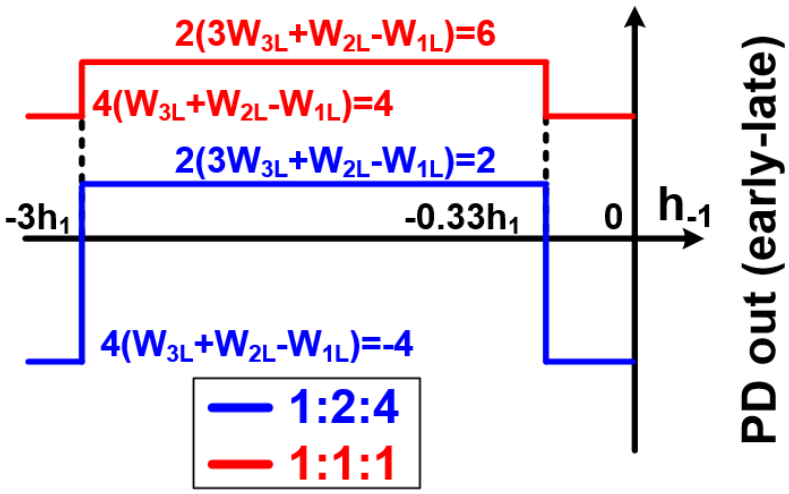


Fig. 3.5 PD characteristics when $h_{-1}<0$, and $h_1>0$ in PAM-4.

Pattern			Recevied level-V_{ref}	Error	PD output		
D[n-1]	D[n]	D[n+1]	h_{-1}, h_1 < 0	E[n]	Early	Late	Early-Late
+1	+3	+3	$3h_{-1}+h_1$ < 0	-1	W_{1L}	-	W_{1L}
-1	+3	+3	$3h_{-1}-h_1$ > 0	+1	-	W_{2L}	$-W_{2L}$
-1	+3	+3	$3h_{-1}-h_1$ < 0	-1	W_{2L}	-	W_{2L}
-3	+3	+3	$3h_{-1}-3h_1$ > 0	+1	-	W_{3L}	$-W_{3L}$
-3	+3	+3	$3h_{-1}-3h_1$ < 0	-1	W_{3L}	-	W_{3L}
+3	+3	+1	$h_{-1}+3h_1$ < 0	-1	-	W_{1L}	$-W_{1L}$
-1	+3	+1	$h_{-1}-h_1$ > 0	+1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
-1	+3	+1	$h_{-1}-h_1$ < 0	-1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
-3	+3	+1	$h_{-1}-3h_1$ > 0	+1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
-3	+3	+1	$h_{-1}-3h_1$ < 0	-1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
+3	+3	-1	$-h_{-1}+3h_1$ > 0	+1	W_{2L}	-	W_{2L}
+3	+3	-1	$-h_{-1}+3h_1$ < 0	-1	-	W_{2L}	$-W_{2L}$
+1	+3	-1	$-h_{-1}+h_1$ > 0	+1	W_{2L}	W_{1L}	$W_{2L}-W_{1L}$
+1	+3	-1	$-h_{-1}+h_1$ < 0	-1	W_{1L}	W_{2L}	$W_{1L}-W_{2L}$
-3	+3	-1	$-h_{-1}-3h_1$ > 0	+1	W_{2L}	W_{3L}	$W_{2L}-W_{3L}$
+3	+3	-3	$-3h_{-1}+3h_1$ > 0	+1	W_{3L}	-	W_{3L}
+3	+3	-3	$-3h_{-1}+3h_1$ < 0	-1	-	W_{3L}	$-W_{3L}$
+1	+3	-3	$-3h_{-1}+h_1$ > 0	+1	W_{3L}	W_{1L}	$W_{3L}-W_{1L}$
+1	+3	-3	$-3h_{-1}+h_1$ < 0	-1	W_{1L}	W_{3L}	$W_{1L}-W_{3L}$
-1	+3	-3	$-3h_{-1}-h_1$ > 0	+1	W_{3L}	W_{2L}	$W_{3L}-W_{2L}$
Other cases			-	-	-	-	-

Table 3.4 PD outputs for all possible transitions when h_{-1}<0, and h_1<0 in PAM-4.

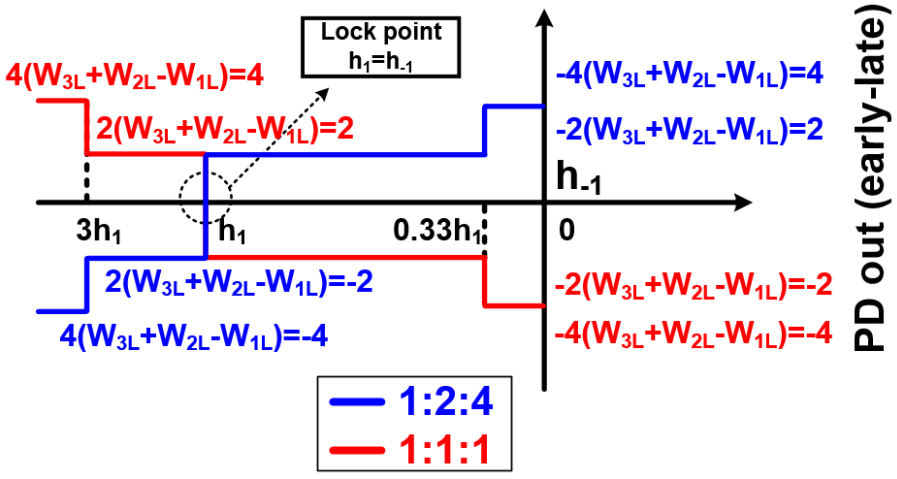


Fig. 3.6 PD characteristics when h_{-1}<0, and h_1<0 in PAM-4.

3.3 Circuit Implementation

3.3.1 Overall Architecture

Fig. 3.7 shows the circuit implementation of the PAM-4 receiver, which is composed of the TWG-PD, a CTLE, a 2-tap DFE, samplers, 4 to 64 deserializers, a phase interpolator (PI), and digital logic. To reduce the timing constraints, quarter-rate clocking is employed.

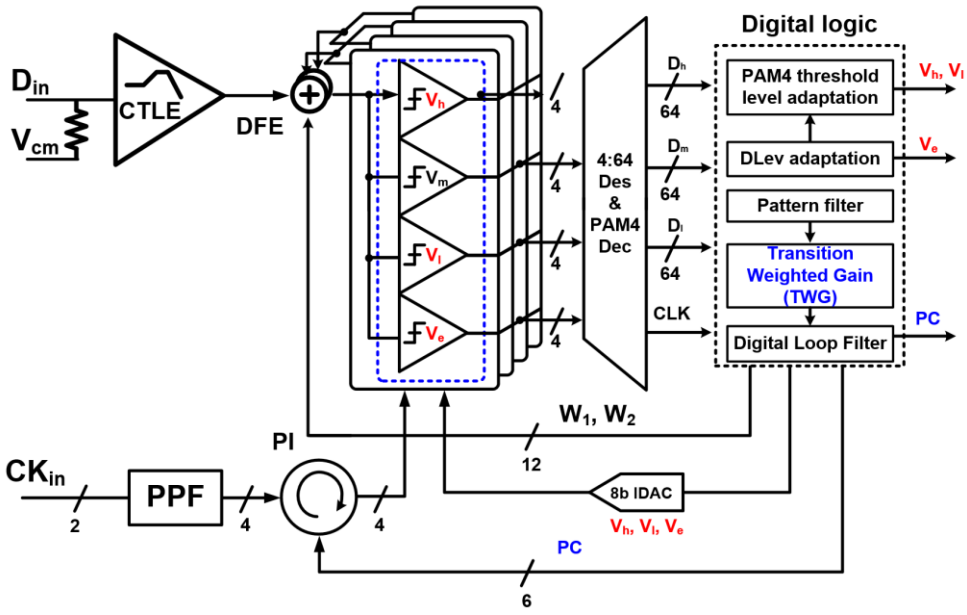
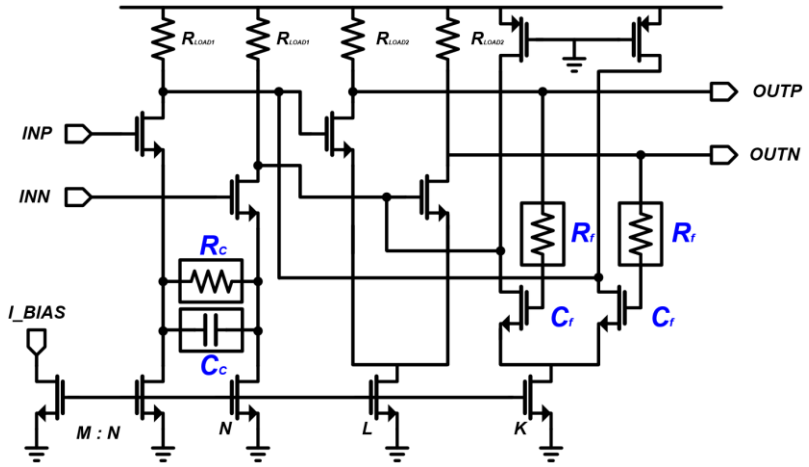


Fig. 3.7 Overall architecture of PAM-4 receiver.

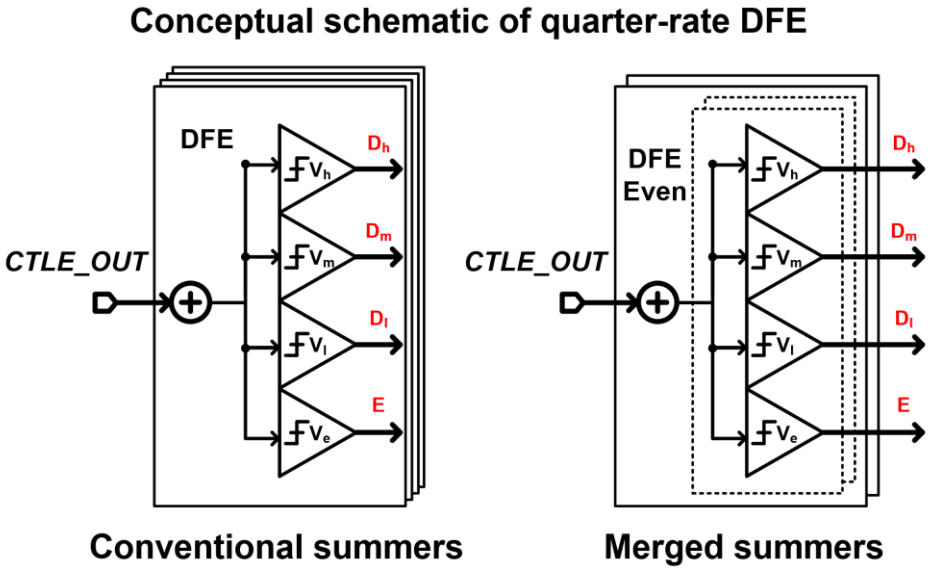
3.3.2 Analog Block

Since the PAM-4 receiver requires many samplers, the summing node of the feedback filter in the DFE is very capacitive, subject to the bandwidth limit. Thus, as shown in Fig. 3.8(a), the CTLE incorporates the Cherry-Hooper topology to offer low output resistance with a small area and low power consumption [9] . Only moderate boosting of 3-dB is provided.

The remaining post-cursor ISIs after the CTLE are removed by the 2-tap DFE. Although four summers are required from the feedback filters of the 4 DFEs, summers working at differential phases such as (CK0, CK180) and (CK90, CK270) are merged at the input to the DFE samplers, thereby reducing the load capacitance of the CTLE [7] . Since the number of summers is reduced from four to two, power consumption, active area, and the effort of tuning the offset are significantly reduced. Fig. 3.8(b) shows the architecture of a merged summer. The strong-arm latch is used for the samplers, and a 6-bit offset control code calibrates and removes the offset of each sampler. The quarter-rate 8 GHz clock is generated by a polyphase filter (PPF) from the 8 GHz differential clock. Since the sampler outputs are in the form of a thermometer code, all the high speed operations are done with the thermometer code. Thus, three bits of data samples and one error sample are deserialized at low speed.



(a)



(b)

Fig. 3.8 (a) CTLE (b) merged summer.

3.3.3 Digital Block

The digital logic composed of the PAM-4 dLev adaptation logic, the pattern filter, the TWG logic, and the digital loop filter operates at 500 MHz. The TWG logic and the DLF adjust the phases of the four-phase 8 GHz clock for the quarter-rate CDR with a PI. The current-output digital-to-analog converter (IDAC) converts the code to the dLev of the data samplers.

Before activating the operation of the CDR, dLev adaptation should be preceded to decide the threshold levels of PAM-4 signal, V_h and V_l for obtaining the maximum eye margin. Fig. 3.9 shows the dLev adaptation procedure with the error comparator periodically estimating the vertical height of the +3 level and placing the other thresholds. The dLev is adaptively adjusted by the equation $V_{DLev}[n+1] = V_{DLev}[n] + \mu_{DLev} \cdot (UP - DN)$. Regardless of ISI, if all the data transition probabilities are uniform, V_{DLev} is located at the center of the dispersion of $3h_0$, and threshold levels, V_h and V_l, are set at $2h_0$, and $-2h_0$. The initial foreground calibration step is performed for all sixteen comparators to compensate for each comparator offset. Two digital loops, the reference voltage for threshold adaptation and the CDR, are performed in the background. The bandwidth of the dLev and threshold adaptation loop is designed to be higher than the CDR loop to prevent instability arising from interacting loops. Since only the transitions involving the +3 data level are examined and selected by the pattern filter, the bandwidth tends to be low. The PI control code (PC) is 6-bit wide and given as a thermometer code.

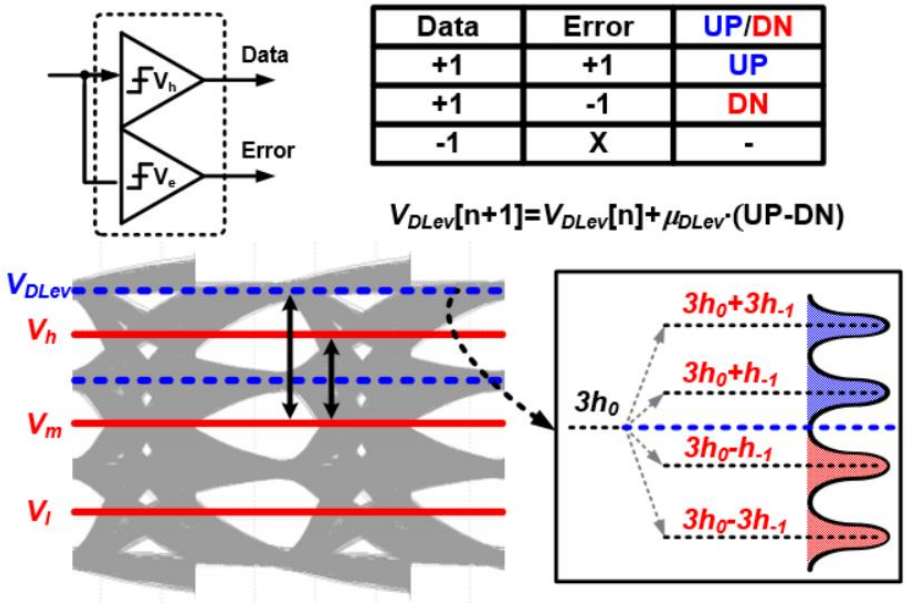


Fig. 3.9 Eye-diagram with data levels considering only pre-cursor ISI.

3.4 Measurement Results

The proposed PAM-4 receiver prototype is fabricated in a 40 nm CMOS process. Fig. 3.10 shows the chip photomicrograph. The chip is measured with a PRBS-7 pattern, operating at 64-Gb/s in PAM-4.

The measurement setup is shown in Fig. 3.11(a). The bit error rate tester (BERT) produces two binary PRBS data streams for MSB and LSB. To make a PAM-4 signal stream, a passive power combiner is employed with one port coming from MSB and the other from LSB through a 6 dB attenuator. The PAM-4 input signal is shown

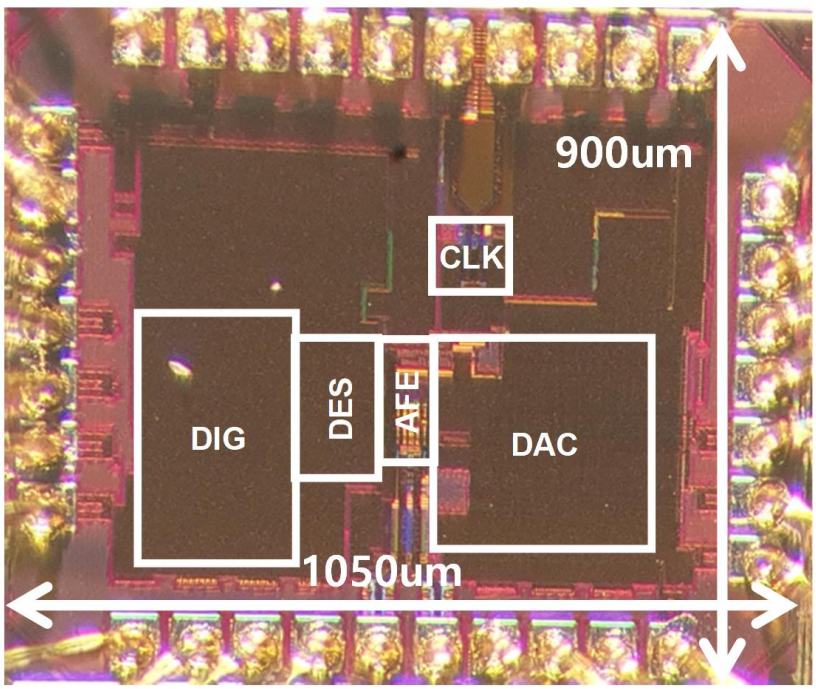


Fig. 3.10 Chip photomicrograph of the implemented receiver.

in Fig. 3.11(b). As shown in Fig. 3.12, the overall path with SMA cables and PCB exhibits an insertion loss of around 6.6 dB at the Nyquist frequency of 16 GHz. Fig. 3.13 shows that the actual area is 0.175 mm^2, and power consumption is 152 mW.

Fig. 3.14(a) shows the bathtub curve when the transition weight ratio of $W_{3L}:W_{2L}:W_{1L}$ is 1:2:4 measured from the error detector using an I^2C interface with an automated Python script. A slightly larger sampling window is measured for MSB as expected. A significantly larger window is observed when the BER of 10^{-6} is specified, which is normally the case of PAM-4 signalings where a forward error correction capability is employed. Fig. 3.14(b) shows that JTOL is measured in four cases: the conventional MM-CDR with a 1:1:1 ratio for MSB and LSB, and the proposed TWG-CDR with a 1:2:4 ratio also for MSB and LSB. MSB and LSB are respectively measured with PRBS-7 pattern checker in BERT. Fig. 3.15 shows jitter

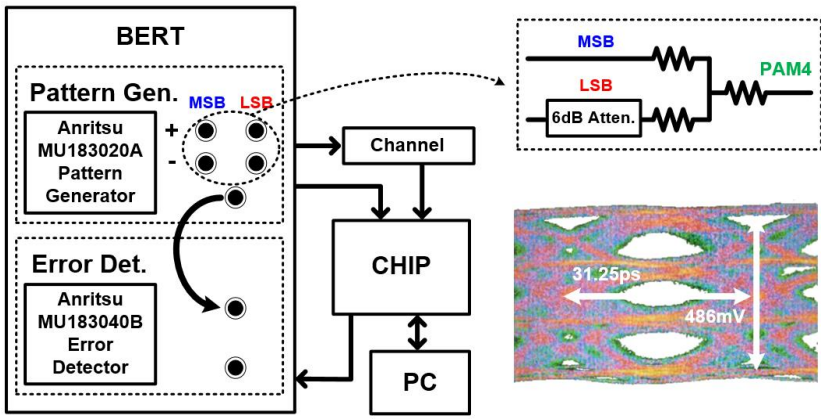


Fig. 3.11 (a) Measurement set-up, and (b) PAM-4 input signal.

histograms of the recovered clock. The horizontal eye opening margin and jitter performance of the TWG-CDR are improved compared with the sign-sign MMCDR (SS-MMCDR), as shown in Fig. 3.15, which are also indirectly verified with the JTOL measurement result shown in Fig. 3.14(b).

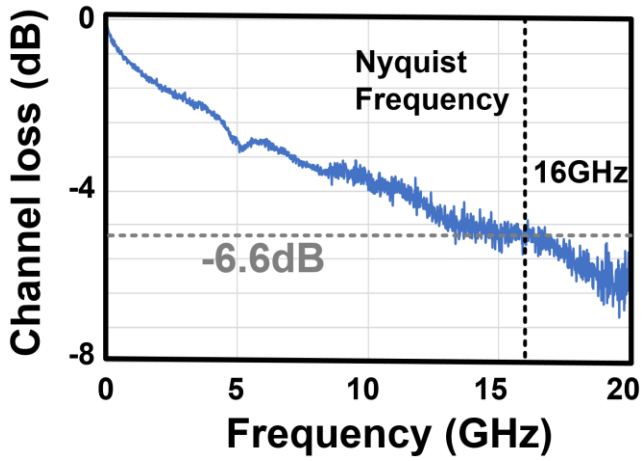


Fig. 3.12 Insertion loss of a channel used for measurement.

Block Description	Area (um^2)	Power (mW)
Analog Front-end (AFE)	6430	102.3
Digital-to-Analog Converter (DAC)	63250	
Phase Interpolator (CLK)	5320	12
Deserializer (DES)	14400	37.72
Digital Logic (DIG)	87400	

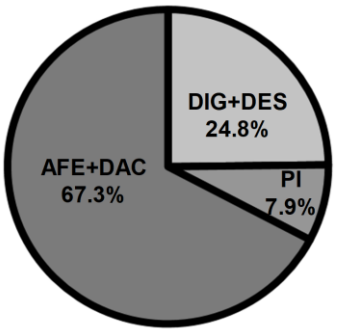
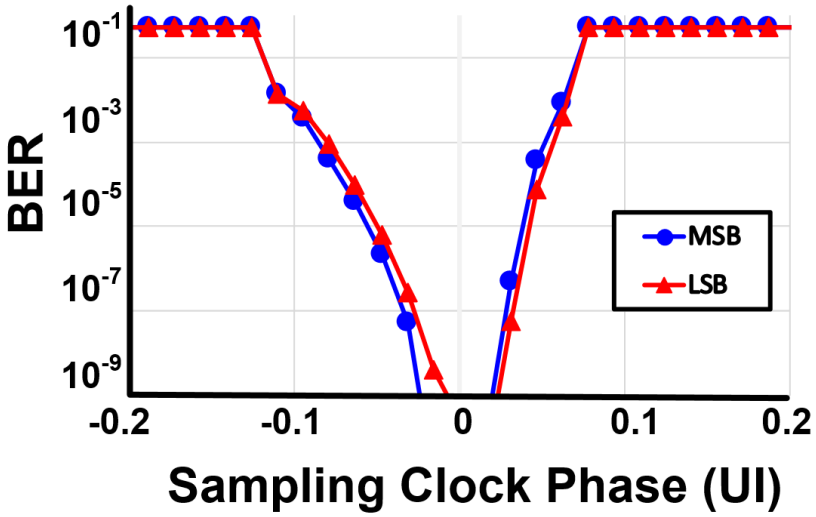
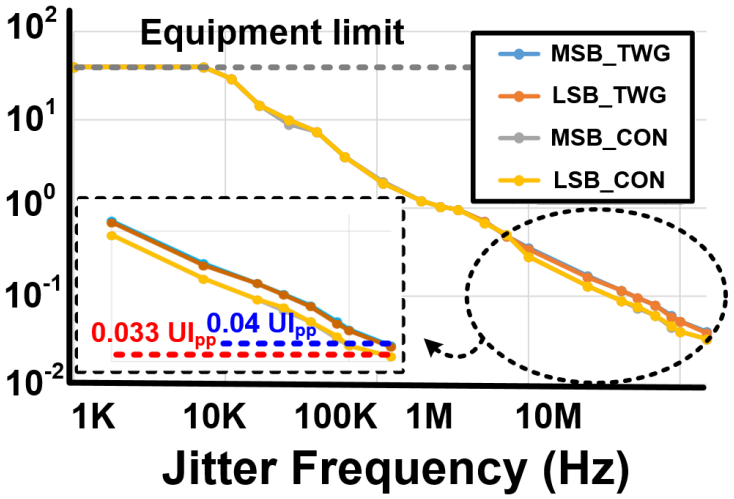


Fig. 3.13 Power breakdown and area.

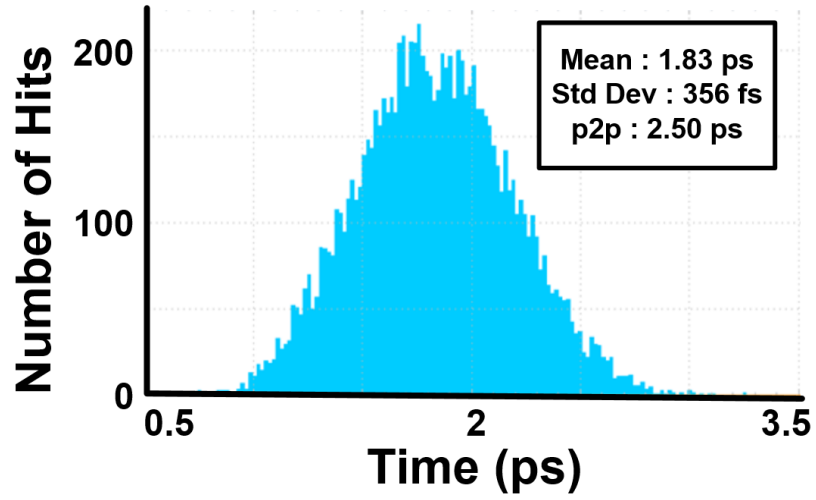


(a)

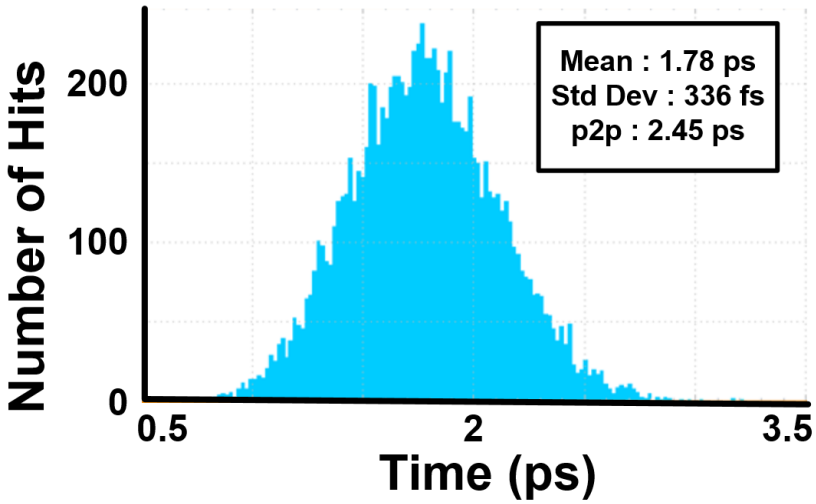


(b)

Fig. 3.14 (a) Measured bathtub curve, and (b) JTOL comparison between MM-CDR and TWG-CDR



(a)



(b)

Fig. 3.15 The histogram of random jitter for the recovered clock with (a) MM-CDR and (b) TWG-CDR

Table 3.5 summarizes and compares the performance of the published state-of-the-art PAM-4 receivers, including the type of PDs. The proposed TWG-PD achieves the highest speed with better energy efficiency and less silicon area among the 64-Gbps classes. In addition, since the proposed phase detection technique is implemented with digital circuitry, insensitivity to the mismatch of the devices is another benefit.

	JSSC'19	ISSCC'19	ASSCC'21	ISSCC'18	ISSCC'18	This work
Technology Node	65nm CMOS	28nm CMOS	40nm CMOS	65nm CMOS	28nm FDSOI	**40nm CMOS**
Modulation	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	**PAM-4**
PD type	Oversampling (BB-PD)	Oversampling (BB-PD)	Baud-rate (compatible multi-level)	Baud-rate (Pulse-Catcher)	Oversampling (BB-PD)	**Baud-rate (TWG)**
Data Rate (Gb/s)	56	25.6	48	32	64	**64**
Area(mm^2)	0.51	~0.41	0.24	0.16	0.32	**0.177**
Equalizer	CTLE, 1-tap FIR, 1-tap IIR DFE	CTLE	CTLE, 1-tap DFE	TX FIR, CTLE, 1-tap DFE	TX FIR, CTLE	**CTLE, 2-tap DFE**
Efficiency (pJ/b)	4.63	2.22	2.42	2.5	2.8	**2.37**
Power (mW)	259	56.8	116.3	80	180	**152**
BER	<1E-12	<1E-12	<1E-11	<1E-12	~1E-12	**~1E-11**

Table 3.5 Performance summary and comparison

Chapter 4

A Low-Jitter PAM-4 Baud-rate Digital CDR

4.1 Overview

As the demand for higher data rates in wireline communication increases, multi-level signaling such as PAM-4 has been adopted in many applications instead of NRZ [1]-[7], [10]-[12], [16]-[23]. While PAM-4 signaling provides a doubled data rate with the same bandwidth, the patterns of transitions are more diverse than NRZ signaling, leading to a degradation of the vertical and horizontal eye margins. Therefore, an improved CDR circuit is required to fully utilize the patterns that are not

present in NRZ signaling.

Typically, two types of CDRs, namely, a 2x-oversampling CDR and a Baud-rate CDR, are commonly used [1]-[7], [10], [12], [18]-[23]. The 2x-oversampling CDR uses edge and data information for phase detection, locking at the zero-crossing point. In NRZ signaling, the zero-crossing point is unique, guaranteeing robust CDR operation. However, PAM-4 signaling has multiple zero-crossing points due to various types of transitions, including asymmetric transitions, as shown in Fig. 4.1. This problem has been addressed in several papers [3]-[6]. In [3], [6], a technique to filter only symmetric transitions and ignore patterns that appear as jitter is proposed. However, this technique reduces the available transition density, degrading the phase tracking performance. Other papers utilize asymmetric transitions as "very

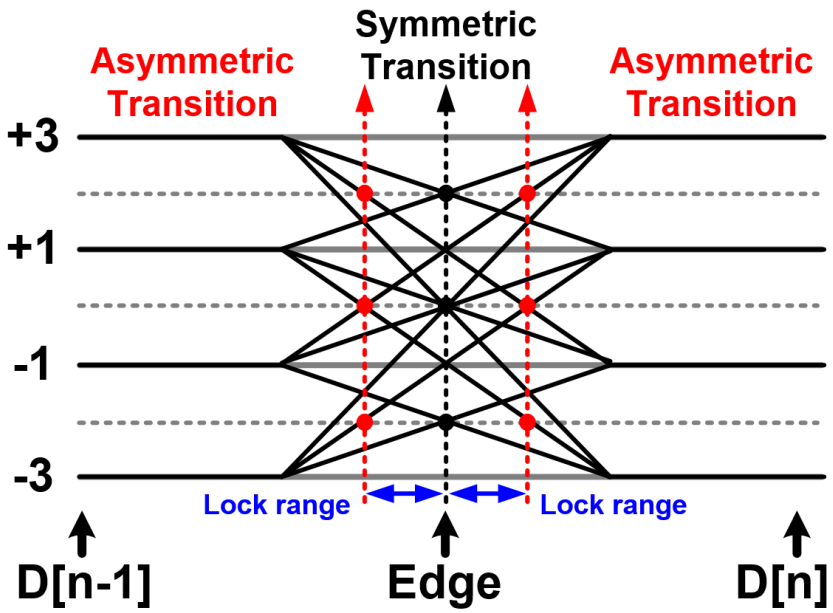


Fig. 4.1 Symmetric and asymmetric transitions in a PAM-4 waveform.

early" and "very late" states to increase the transition density [4], [5], which are defined as a partial elimination technique in [12]. While this technique increases the effective transition density when the phase is located away from the minor lock point, the asymmetric patterns do not produce phase information after the clock phase enters the lock range. The lock range is the range between the lock point of the asymmetric transitions and the lock point of the symmetric transitions, as shown in Fig. 4.1. When the channel bandwidth is large enough, the partial elimination technique appears worse than no elimination, which corresponds to the conventional 2x-oversampling CDR, as analyzed in [12].

Recently, Baud-rate CDRs have been preferred over the 2x-oversampling CDR to reduce the overhead of multi-phase clock generation. However, the problem caused by various transitions in multilevel signaling also occurs in the Baud-rate CDRs. Since the Baud-rate CDR uses error samples instead of edge samples, the transitions can be divided into two types: full-swing transitions and non-full-swing transitions, as shown in Fig. 4.2. The full-swing transitions have the maximum voltage swing like the NRZ signaling, while the non-full-swing transitions have a smaller swing. In [21], to obtain a simple implementation, only the full-swing transitions in PAM-4 signaling are used for phase detection. However, this approach makes it difficult to achieve robust CDR due to the limited transition density. To overcome this limitation, techniques of the PAM-4 Baud-rate CDRs considering the non-full-swing transitions have been proposed [22], [23]. However, these techniques only focus on a convergence problem rather than different lock points of various patterns and jitter tracking ability.

In this Chapter, we propose a low-jitter Baud-rate PD using an asymmetric-

weighted technique based on quantitative analysis. JTOL is measured to provide a comparison of jitter tracking ability. The proposed PD achieves improved jitter performance compared to the conventional PD.

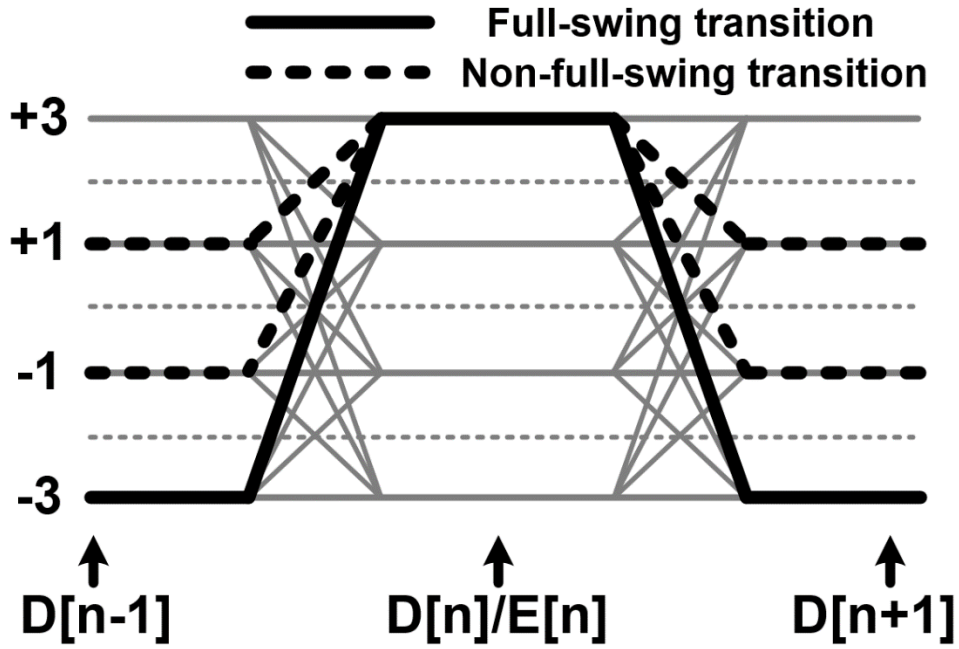


Fig. 4.2 Full-swing and non-full-swing transition in a PAM-4 waveform.

4.2 Overall Architecture

Fig. 4.3 shows the circuit implementation of the proposed PAM-4 receiver, which comprises analog blocks and digital logics. The analog blocks consist of several components: a CTLE, a 2-tap DFE, a voltage-output digital-to-analog converter (VDAC), samplers, 4:32 deserializers, and PIs. To handle the high bandwidth requirements of PAM-4 reception, the Cherry-Hooper topology [9] is adopted to the CTLE design. The 2-tap DFE removes post-cursor distortions that remain after the CTLE processing. In addition, summers that operate with differential phases are merged to reduce power consumption and tuning complexity. The samplers utilize a strong-arm latch, and no additional analog circuit is needed for offset calibration since the threshold of the data samplers already includes offset information. The DFE utilizes two 6-bit IDACs, and a total of twenty 7-bit VDACs are used for reference level generation, with twelve for data samplers and eight for error samplers. Because of the limit in digital logic synthesis, 4 to 32 deserializers are used.

The quarter-rate clocking is adopted to relax timing constraints, with the quarter-rate 5 GHz clock being generated by dividing a 10GHz differential clock. In addition, two parallel PIs are employed to cancel skew between adjacent clocks.

The proposed receiver includes various adaptation logics as well as the clock recovery logic. The three adaptation logics for the PAM-4 threshold levels of data samplers, dLev and biased-reference of error samplers, and DFE coefficients should be performed adequately to achieve the proposed Baud-rate CDR.

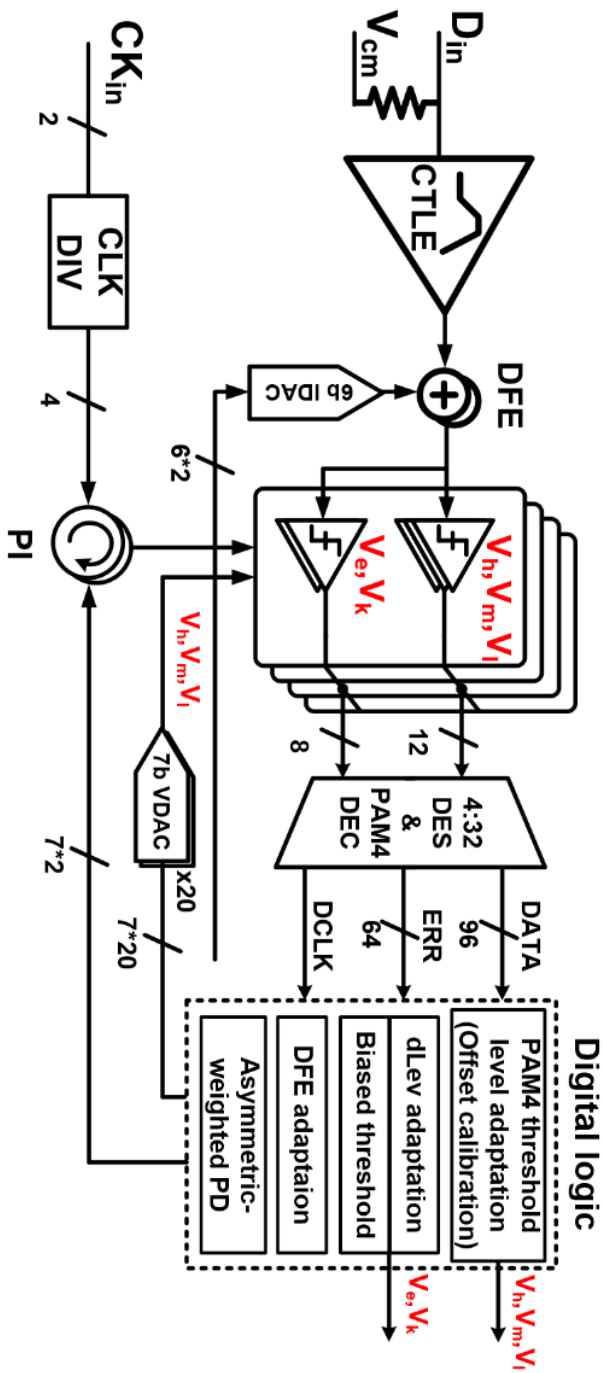
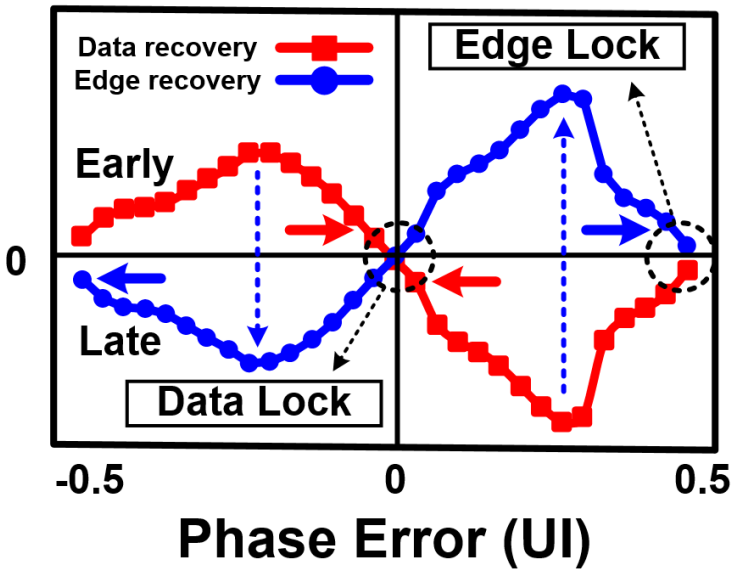


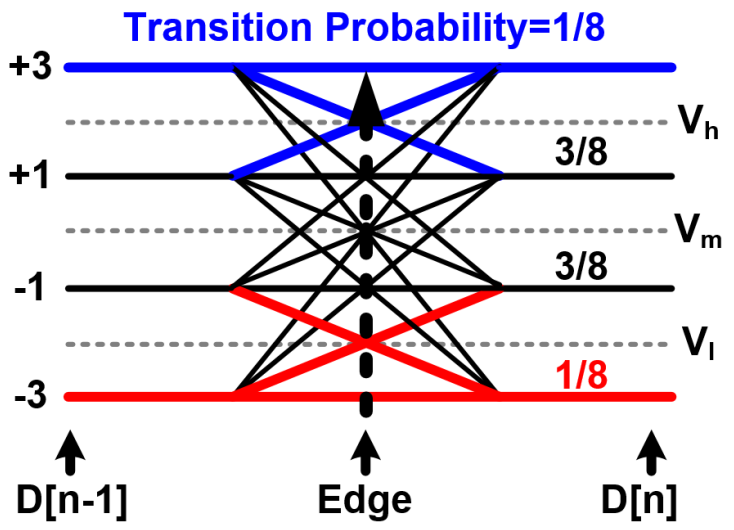
Fig. 4.3 Overall PAM-4 receiver circuits including analog blocks and digital logics.

4.2.1 Threshold Level Adaptation

First, the adaptation for the PAM-4 threshold levels should be preceded by other adaptations because it decides the threshold levels of the data samplers used for further adaptations. To obtain the threshold level adaptively, the sampling clock should be located at the edge of the signal. Fig. 4.4(a) shows an operation to obtain the edge clock. Considering that the general Baud-rate CDR has a data lock point at $h_{-1} = h_1$, an edge lock point can be obtained by inverting the UP/DN of the PD. Since the inversion of the UP/DN changes “early” to “late”, and “late” to “early’, the data lock point is changed to the edge lock point. Only full-swing transition is used for clean edge information of transitions. After the edge lock, the transition probability is determined as shown in Fig. 4.4(b). Assuming random patterns, the probability of being sampled as +3 is 1/8 at the edge. In the same way, each probability of +1, -1, and -3 is obtained as 3/8, 3/8, and 1/8, respectively. As a result, the high threshold level (V_h) is adaptively locked at the point where the ratio of the high-level sampler output becomes 1:7. Since the threshold level includes the offset of the sampler, additional offset calibration is not needed. In the same way, the threshold levels of all other data samplers are adaptively obtained.



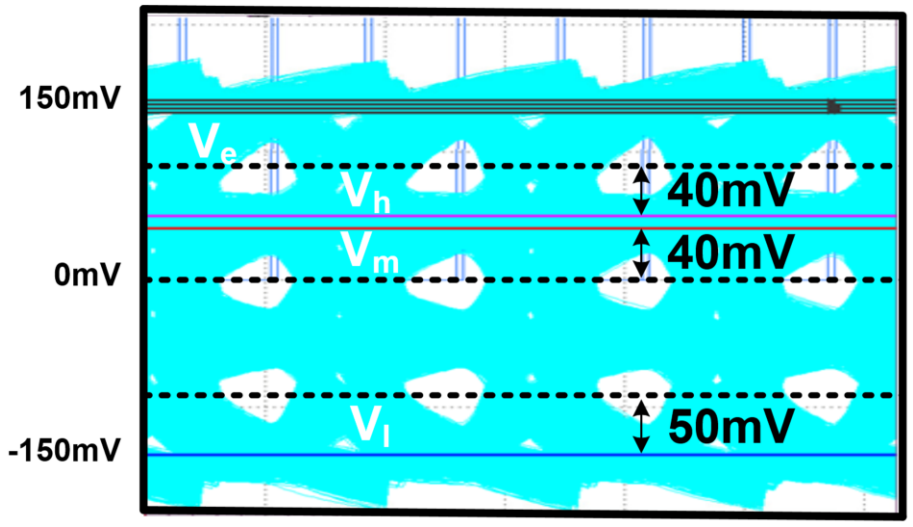
(a)



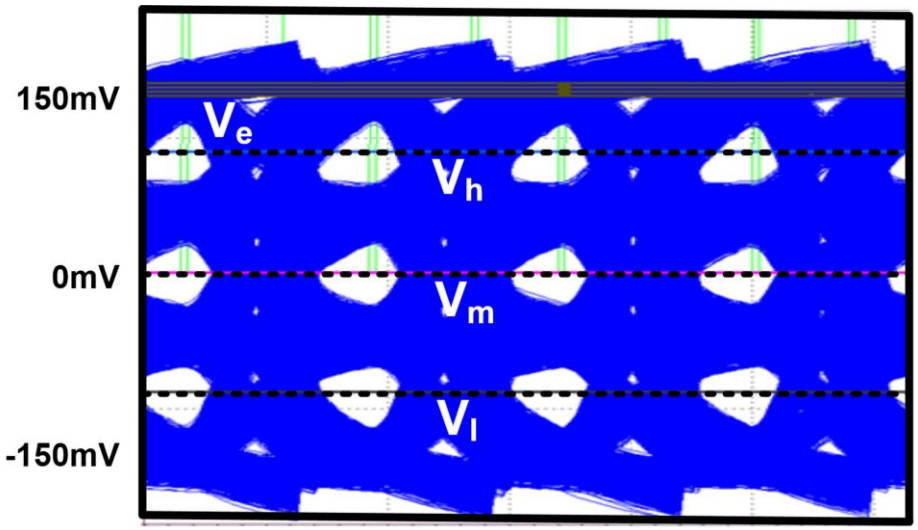
(b)

Fig. 4.4 Threshold level adaptation including the method of obtaining (a) the edge clock, and (b) threshold levels.

Fig. 4.5(a) shows an eye diagram of 40 mV for D_h, –40 mV for D_m, and 50 mV for D_l for offset when threshold level adaptation is used and when the adaptation is not used. When threshold level adaptation is not used, it is a method that decides the threshold as 2/3 of the reference level of the error sampler, which is commonly used in PAM-4. The horizontal line is the data level that is actually sampled, including offset, and thus the receiver does not function properly. Fig. 4.5(b) shows that the horizontal line is located in the center of each eye and works properly as a result of using adaptation for the same offset.



(a)



(b)

Fig. 4.5 Simulated eye-diagrams of (a) before threhold level adaptation, and (b) after threshold level adaptation.

4.2.2 DLev/Biased-Reference and DFE Adaptation

The adaptations logics for dLev, biased-reference, and DFE coefficients are implemented by using the SS-LMS algorithm [27]. Since correctly sampled error information is needed in the DFE adaptation, the loop gain of the DFE adaptation is smaller than that of the dLev adaptation. The DFE adaptation is divided into two loops for the 1st post-cursor and the 2nd post-cursor. Since the 1st post-cursor is normally larger than the 2nd post-cursor, the loop gain for the 1st post-cursor should be larger.

Fig. 4.6 shows the dLev and biased-reference adaptation procedure with the error sampler including all possible ISIs. The dLev is adaptively adjusted by the equation:

$$V_e[\mathrm{n}+1] = V_e[\mathrm{n}] + \mu_e(UP - DN) \tag{4.1}$$

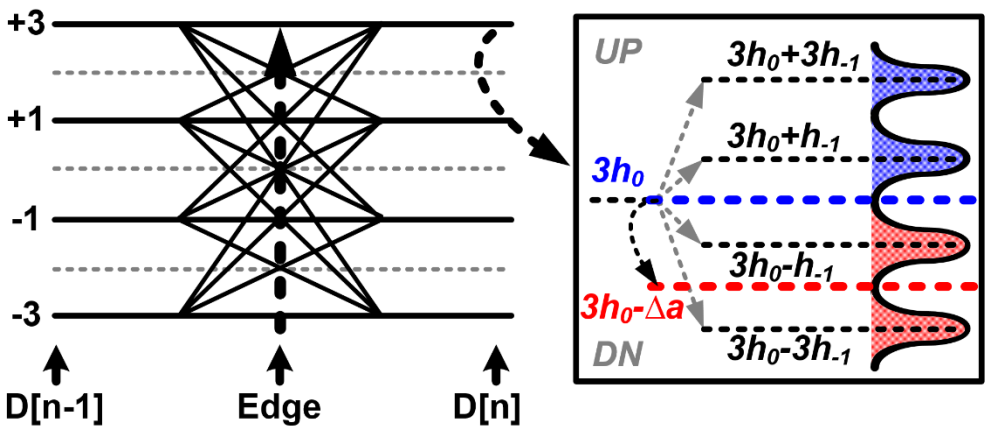


Fig. 4.6 Operation of dLev and biased-reference adaptation.

where μ_e is the weight of updating the threshold code, which is digitally controlled. As shown in Fig. 4.6, if the output of the error sampler is +1, UP is obtained, leading to increasing the reference level of the error sampler. In the same way, DN is output for the case of -1, resulting in a smaller reference level of the error sampler. Regardless of ISI, the threshold of the error sampler is always located at the center of the signal, $3h_0$, if all data transition probabilities are uniform. The DFE coefficients are also adaptively adjusted while the dLev adaption is performed. At the same time, the biased reference of the error sampler, $V_{k,}$ is obtained as:

$$V_k[\mathrm{n}] = V_e[n] - K * LSB_{VDAC} \tag{4.2}$$

where K is a 4-bit digital code to make a biased reference level. The constant value, Δa, in Fig. 4.6 is decided by equation (4.2), $\Delta \mathrm{a} = K * LSB_{VDAC}$.

4.3 PAM-4 Baud-Rate Phase Detector

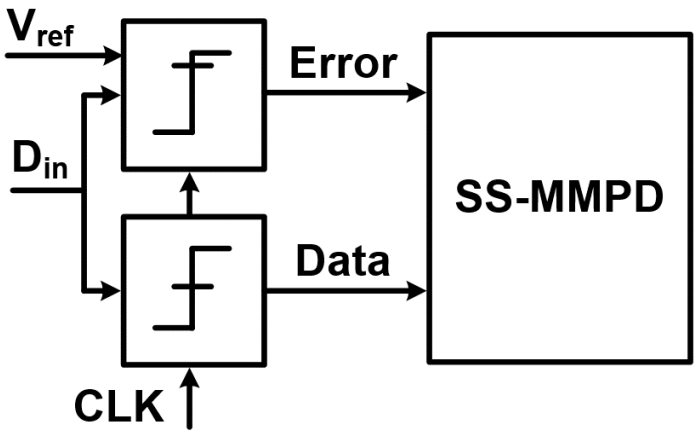
There are two commonly used PDs in Baud-rate CDRs, namely MMPD and SS-MMPD. The MMPD compares the phase difference between two input signals and generates an output proportional to the magnitude of the phase difference. On the other hand, the SS-MMPD compares the signs of the inputs and generates an output based on the sign of the phase difference. As a result, the SS-MMPD, which operates digitally and detects only the input signal signs, achieves better noise immunity and reduces offset effects. Moreover, the SS-MMPD operation is suitable for ADC-based receivers, widely used in high-speed links for high-loss compensation. Therefore, we adopt the SS-MMPD as the conventional PD in the PAM-4 Baud-rate CDR. To obtain PD characteristics, we analyze the lock points in the conventional PD with two possible transitions: the full-swing transition and the non-full-swing transition.

4.3.1 SS-MMPD with One Error Sampler (Full-Swing Transition)

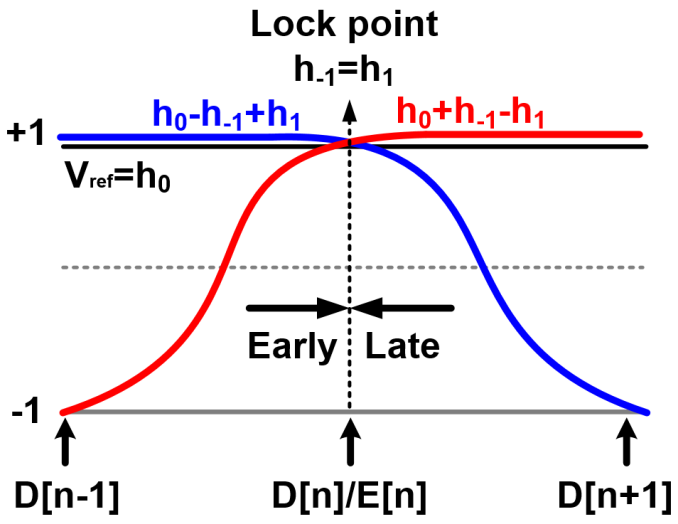
Fig. 4.7(a) depicts the SS-MMPD with one error sampler utilized in NRZ signaling [24]. The PD takes into account three consecutive data samples and an error sample, updating outputs only when the three data samples are -1/+1/+1 (rising transition) or +1/+1/-1 (falling transition), as demonstrated in Fig. 4.7(b). The reference voltage level of the error sampler is established by the signal level including ISIs when the data pattern of $D[n-1]/D[n]/D[n+1]$ has a transition. Specifically,

when the data pattern is the rising transition, the signal level is determined as $h_0 + h_{-1} - h_1$, considering the first pre-cursor and the first post-cursor. Similarly, when the data pattern is the falling transition, the signal level is derived as $h_0 - h_{-1} + h_1$. Using the SS-MMPD, the reference level of the error sampler is established where both signal levels, $h_0 - h_{-1} + h_1$ and $h_0 + h_{-1} - h_1$, are identical, resulting in a lock point at $h_{-1} = h_1$ for the CDR.

The SS-MMPD operation in NRZ signaling can be extended to PAM-4 signaling. The PAM-4 SS-MMPD also considers three consecutive data samples of $\mathrm{D[n-1]}$, $\mathrm{D[n]}$, and $\mathrm{D[n+1]}$ and the middle error sample of $\mathrm{E[n]}$. With PAM-4 signaling, the data samples are classified as +3/+1/-1/-3, while the error samples are assigned as +1/-1 based on the highest reference level. The transitions are categorized into rising and falling transitions and also into 1-level transition, 2-level transition, and 3-level transition based on the swing size. The 3-level transition is identified as a full-swing transition, the same as the transition in NRZ signaling. In the 3-level rising transition, the data pattern is -3/+3/+3, and the signal level is established as $3h_0 + 3h_{-1} - 3h_1$. On the other hand, the 3-level falling transition, corresponding to the data pattern of +3/+3/-3, has a signal level of $3h_0 - 3h_{-1} + 3h_1$. Therefore, the reference voltage level of the error sampler is established as $3h_0$, and the same lock point, $h_{-1} = h_1$, is obtained regardless of the rising transition or the falling transition. Therfore, the 3-level transition is created as a symmetric transition by combining the 3-level rising transition and the 3-level falling transition, and its lock point, $h_{-1} = h_1$, is defined as a major lock point.



(a)



(b)

Fig. 4.7 (a) Implementation of a PD with one error sampler, and (b) operation of SS-MMPD in NRZ signaling.

4.3.2 Non-Full-Swing Transition

Unlike the full-swing 3-level transition, the 1-level transition and the 2-level transition are referred to as non-full-swing transitions, and their lock points vary depending on the type of transitions. The 1-level transition has data patterns of +1/+3/+3 and +3/+3/+1, which have a swing that is 1/3 of the swing in the 3-level transition. The 1-level rising or falling transition signal level is $3h_0 + 3h_{-1} + h_1$ or $3h_0 + h_{-1} + 3h_1$, respectively. Assuming that the pre-cursor and the post-cursor are positive, the signal levels of the 1-level transitions are always higher than the reference voltage determined by the 3-level transitions, which is $3h_0$. Therefore, the 1-level transitions cannot be used to detect the phase.

In contrast, the 2-level rising transition and the 2-level falling transition provide information for phase detection and have 2/3 of the swing in the 3-level transition. The rising transition includes the -1/+3/+3 data pattern, and the falling transition consists of the +3/+3/-1 data pattern. As shown in Fig. 4.8, the signal level for the 2-level rising transition is $3h_0 + 3h_{-1} - h_1$, resulting in a lock point of $3h_{-1} = h_1$. Similarly, the signal level for the 2-level falling transition is $3h_0 - h_{-1} + 3h_1$, resulting in a different lock point of $h_{-1} = 3h_1$. Since the lock points of the 2-level rising and falling transitions differ from the major lock point of $h_{-1} = h_1$, these transitions are considered as a jitter. Therefore, we refer to the two lock points as minor lock points.

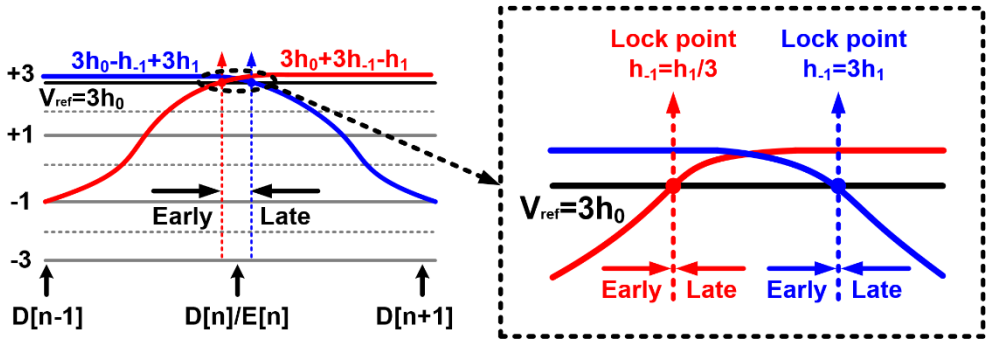


Fig. 4.8 Different lock points of 2-level rising transitions and 2-level falling transitions.

4.3.3 PD Characteristics

Fig. 4.9 shows the phase detection characteristics of all transitions employed in PD, the 3-level transition, 2-level rising transition, and 2-level falling transition. If the phase is located at the major lock point, the PD output is DN for the 2-level rising transition, resulting in a visible jitter. Similarly, for the 2-level falling transition, the PD output is UP, which is also noticeable as a jitter at the major lock point. If all transitions, including full-swing and non-full-swing transitions, are utilized, the jitter is broadly distributed in the range of $h_1/3 < h_{-1} < 3h_1$. Assuming that the distances between the major lock point and each minor lock point are equivalent for simplicity, this distance is referred to as the lock distance (LD), or *d*.

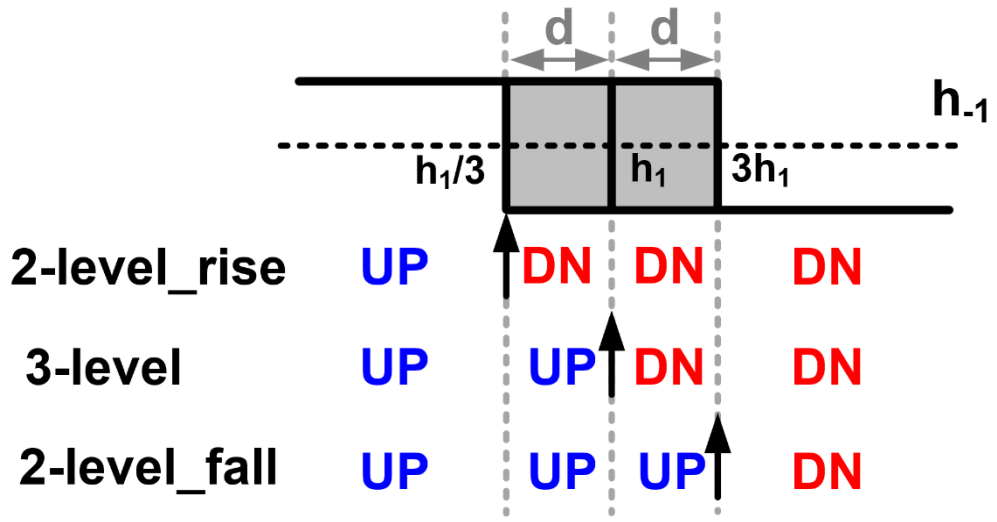


Fig. 4.9 PD characteristics of detected transitions.

4.4 Proposed Baud-Rate Phase Detection

4.4.1 Asymmetric-Weighted Phase Detection

To resolve the problem of jitter, we propose an asymmetric-weighted PD. This involves assigning different weights to the UP ("early") and DN ("late") based on the transition types. For the 3-level transitions, the weight of UP/DN should be symmetric since the rising and falling transitions have the same lock point, $h_{-1} = h_1$. Thus, we apply the same weight to the UP/DN generated by the 3-level transitions, and the PD output is expressed as

$$PD_{out}(3\text{–level}_{\text{rise}}) = PD_{out}(3\text{–level}_{\text{fall}}) = \text{UP} - \text{DN} \tag{4.3}$$

However, for the 2-level transitions, asymmetric weights are necessary since the rising and falling transitions have different lock points where $h_{-1} = h_1/3$ and $h_{-1} = 3h_1$, respectively. Therefore, the proposed PD adopts asymmetric weights for the 2-level transitions. In the case of the 2-level rising transition, UP is multiplied by α, and DN is multiplied by β. The same weights are adopted for the 2-level falling transition, but the weights for UP and DN are interchanged. Therefore, the PD outputs for the 2-level transitions are obtained as

$$\begin{aligned} PD_{out}(2\text{–level}_{\text{rise}}) &= \alpha * UP - \beta * DN \\ PD_{out}(2\text{–level}_{\text{fall}}) &= \beta * UP - \alpha * DN \end{aligned} \tag{4.4}$$

Since the major and minor lock points are determined by the relation between the pre-cursor, h_{-1}, and the post-cursor, h_1, the PD gain curve depends on the magnitudes of h_{-1} and h_1 as shown in Fig. 4.10. In the condition of $h_{-1} < h_1/3$, both 3-level transitions and 2-level transitions generate UP, thereby the PD gain is $2 + \alpha + \beta$. On the other hand, the PD gain is 2 under $h_1/3 < h_{-1} < 3h_1$ because the 2-level rising transition and the 2-level falling transition generate opposite decisions. In the same way, DN is generated by the same gain of $2 + \alpha + \beta$, and 2 under $h_{-1} > 3h_1$, and $h_1 < h_{-1} < 3h_1$, respectively. In the conventional case where the SS-MMPD is used, both α and β are 1, and the PD gain becomes 4 under $h_{-1} < h_1/3$. To fairly compare the jitter injected by PD, we set $\alpha + \beta = 2$, which is matched with the SS-MMPD. Therefore, the PD gain curve appears the same regardless of α value when the data transition probability is the same.

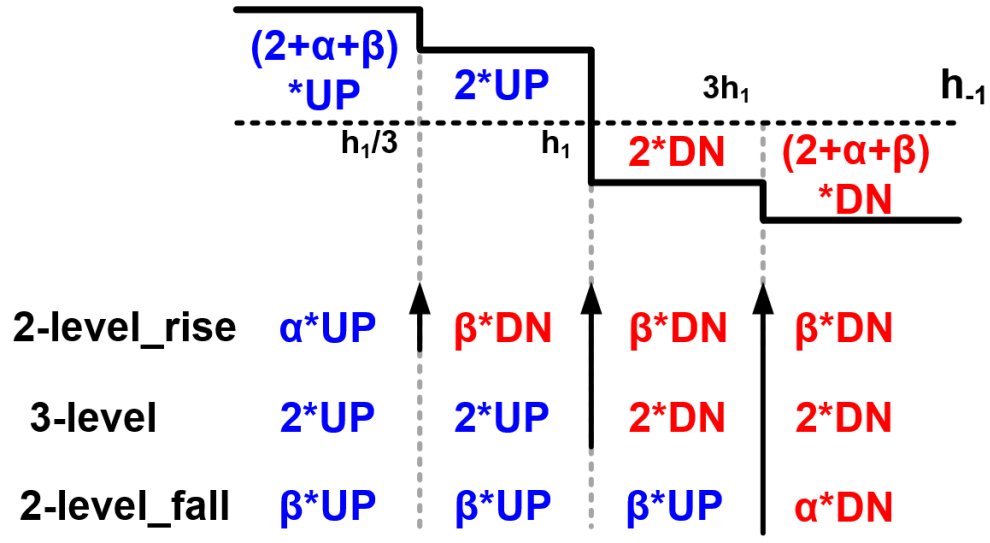


Fig. 4.10 PD gain curve with an asymmetric-weighted technique.

We assume the input phase error is distributed according to a Gaussian distribution, as illustrated in Fig. 4.11, with a major lock point of $h_{-1} = h_1$. In the case of a 2-level rising transition, the DN distribution is more stochastic than the UP distribution because it has a lock point, $h_{-1} = h_1/3$, located at a distance to the left of the LD. Consequently, the weight of UP must be raised to shift the minor lock point to the right. As a result, we determine that $\alpha > 1$. Similarly, in the case of a 2-level falling transition, the UP distribution is dominant, leading to the same conclusion. The optimal value of α is determined based on the variances of random jitter and LDs. When a 2-level rising transition is detected based on the major lock point, the probability of UP becoming dominant is $\Phi\left(-\frac{d}{\sigma}\right)$, and the probability of DN becoming dominant is $1-\Phi\left(-\frac{d}{\sigma}\right)$. Consequently, the minor lock point can be transferred to the major lock point by multiplying the UP distribution by $1-\Phi\left(-\frac{d}{\sigma}\right)$ and the DN distribution by $\Phi\left(-\frac{d}{\sigma}\right)$. Similarly, the weight of UP is $1-\Phi\left(\frac{d}{\sigma}\right)$, and the

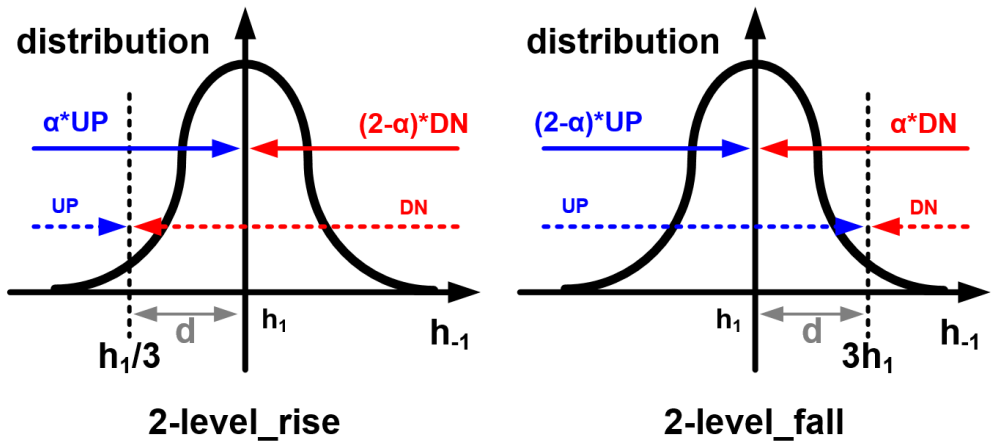


Fig. 4.11 Operation of an asymmetric PD considering a random Gaussian distribution at the major lock point.

weight of DN is $\Phi\left(\frac{d}{\sigma}\right)$. Here, $\Phi()$ refers to the Cumulative Density Function of the Standard normal distribution, which is defined as

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} \exp\left(-\frac{t^2}{2}\right) dt \tag{4.5}$$

As a result, optimum α is calculated as $2\Phi\left(\frac{d}{\sigma}\right)$, which satisfies the equation (4.6):

$$\alpha : 2 - \alpha = \Phi\left(\frac{d}{\sigma}\right) : 1 - \Phi\left(\frac{d}{\sigma}\right) \tag{4.6}$$

Using the optimal value of α, the minor lock points of 2-level rising and falling transitions are stochastically shifted to the major lock point. However, this does not guarantee the performance of the jitter injected by the PD in the CDR system. A quantitative analysis of the jitter aspect is described in Section 4.5.

4.4.2 Biased-Reference of Error Sampler

The previous discussion has established that the lock points arise in the relationship between the pre-cursor and the post-cursor. However, when the post-cursor is eliminated by a DFE, the value of h_1 becomes zero, resulting in a lock point at $h_{-1} = h_1 = 0$. At the same time, if the equalization for removing the pre-cursor is insufficient and h_{-1} cannot be set to zero, the PD will continue to output DN ("late"), leading to a slip without a lock point. One proposed solution for this issue is manually managing digital offsets in the PD output, as described in [25]. However, determining the optimal value of the digital offset for various channels is challenging. Therefore, an alternative method, called maximum-eye tracking (MET), has been presented in [24]. Nevertheless, both techniques depend on the transition pattern, meaning that the correlation between the pre-cursor, main-cursor, or post-cursor does not determine the lock point.

To address these issues, we propose a method of giving an offset to the reference level of the error sampler to determine the lock point based solely on the pre-cursor value. Fig. 4.12 shows how the PD operates when a bias, Δa, is added to the reference of the error sampler. Since there is no post-cursor, only the falling transition is considered for phase detection. Thus, for the 2-level transition, a lock point at $h_{-1} = \Delta a$ is obtained, where the reference level, $3h_0 - \Delta a$, and the signal level, $3h_0 - h_{-1}$, become the same. Similarly, for the 3-level transition, a lock point at $3h_{-1} = \Delta a$ is obtained. Although this resolves the slip problem of the Baud-rate CDR with DFE, the jitter problem mentioned earlier still arises when using the DFE.

The lock point is located between $h_{-1} = \Delta a$ and $3h_{-1} = \Delta a$, thus it cannot be

classified into major or minor lock points. Therefore, the lock point is positioned in the middle of the two lock points, and the PD output is obtained according to equation (4.7):

$$PD_{out}(3-\text{level}) = \alpha * \text{UP} - \beta * \text{DN}$$
$$PD_{out}(2-\text{level}) = \beta * \text{UP} - \alpha * \text{DN} \quad (4.7)$$

In the same reason for a fair comparison of the jitter injected, the values of α and β are constrained such that $\alpha + \beta = 2$, leading to the same PD gain curve regardless of α value. The optimal value of α is obtained as $2\Phi\left(\frac{d}{\sigma}\right)$, where *d* represents the distance between the center of the two lock points, and each lock point is assumed to correspond to the LD.

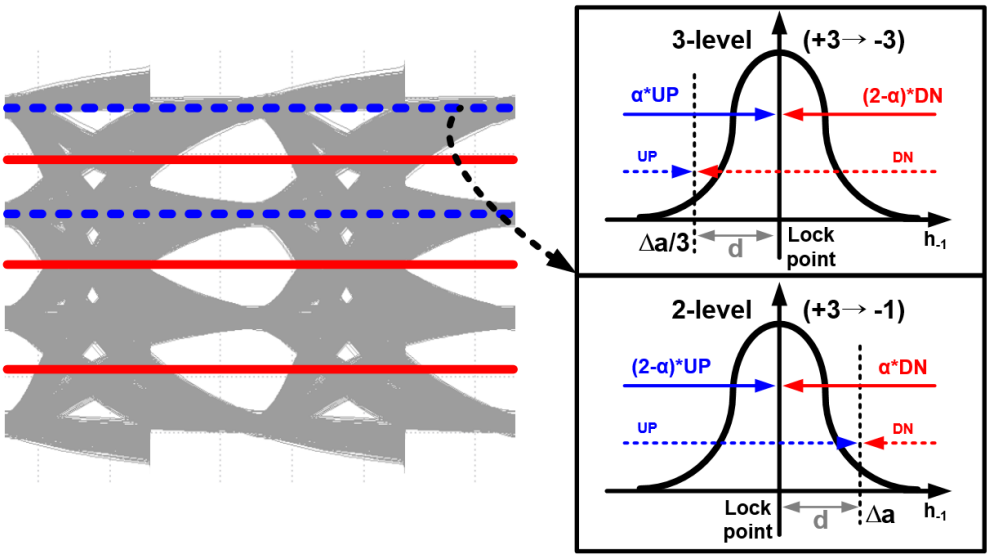


Fig. 4.12 Operation of the biased-reference of the error sampler.

4.5 Pseudo-Linear Analysis of SS-MMPD

For the specific jitter analysis, a pseudo-linear analysis technique is utilized to quantitatively model the non-linear behavior of the SS-MMPD and the proposed PD, as discussed in the literature [26]. Typically, a BB-PD is represented by a sampler where a positive phase error, ϕ_e, results in an output of +1 indicating an early signal, while a negative phase error results in an output of -1, indicating a late signal. The non-linear characteristics of the sampler are modeled by using a pseudo-linear analysis technique, as depicted in Fig. 4.13(a). The phase error consists of a deterministic term, $\phi_{e,d}$, and a random term, $\phi_{e,r}$. The two error terms are each multiplied by different gain factors, K_D and K_R, respectively, to minimize the power of quantization noise, ϕ_q, as described in [26]. For a more accurate model, the quantization noise ϕ_q is defined as the difference between the output of the sampler, ϕ_u, and the linear term, $\phi_{e,d}K_D + \phi_{e,r}K_R$.

$$\phi_q = \phi_u - \phi_{e,d}K_D - \phi_{e,r}K_R \tag{4.8}$$

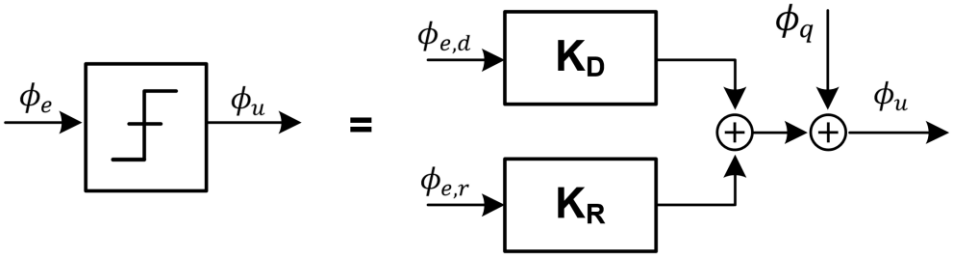
To determine the weight α discussed in Section 4.4.1, a comparison is made between the proposed PD and SS-MMPD by modifying the sampler output multiplied by α or $2-\alpha$. As shown in Fig. 4.13(b), α is the weight multiplied when the output of the sampler is +1, and $2-\alpha$ is the weight when the output is -1 for the 3-level transition. Similarly, for the 2-level transition, $2-\alpha$ and α are the weights when the output of the sampler is +1 and -1, respectively.

Assuming sufficient noise in the system, the random noise component $\phi_{e,r}$ becomes the dominant element. The deterministic noise component $\phi_{e,d}$ occurs independently of all transitions, resulting in an expectation value of zero. As a result, decoding only the random gain K_R using Bayes' rule yields the following:

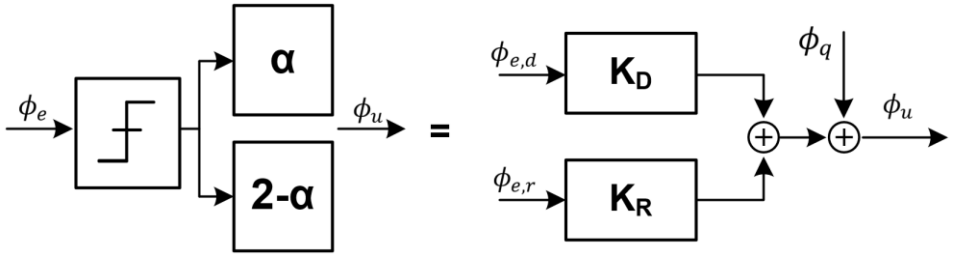
$$K_D = \frac{E[\phi_{e,d}\phi_u]}{E[{\phi_{e,d}}^2]} = \sum_X \text{Prob}[X]K_{D,X} \tag{4.9}$$

$$K_R = \frac{E[\phi_{e,r}\phi_u]}{E[{\phi_{e,r}}^2]} = \sum_X \text{Prob}[X]K_{R,X} \tag{4.10}$$

Here, X represents the transition used for each PD, which consists of the 3-level and 2-level transitions. Prob[X] denotes the probability of occurrence for each detected transition. When the DFE is used, the gain factors of the 3–level and 2–level transitions are the same because the LDs of both transitions are assumed to be identical. Consequently, the expectation value of the deterministic terms is zero. Any variation due to the LD will be included in the quantization noise, ϕ_q, as a random variation under uncorrelated conditions. Therefore, only the random gain factor, K_R, is considered to compare the jitter injected into the CDR by the PD.



(a)



(b)

Fig. 4.13 Decomposed pseudo-linear gains K_D and K_R of (a) the conventional BB-PD, and (b) asymmetric-weighted BB-PD

4.5.1 Conventional SS-MMPD with DFE

First, we investigate the conventional SS-MMPD prior to the proposed asymmetric-weighted PD. Since the DFE is used, biased-reference technique in 4.4.2 is adopted. We denote this case as Case A. For the SS-MMPD, the value of α is 1, and the lock point is located exactly middle between the two lock points. As a result, the gain factors for the 3-level and 2-level transitions, denoted by $K_{R,3\text{-level}}$ and $K_{R,2\text{-level}}$, are equal and expressed as

$$K_{R,3-level} = K_{R,2-level}$$
$$= \frac{\left(\int_{-\infty}^{-d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_e + \int_{-d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_e}^2\right]} = 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \quad (4.11)$$

Then, the overall noise gain $K_{R,A}$ is calculated using (4.10) and (4.11):

$$K_{R,A} = 2\alpha_T \left(2\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} \quad (4.12)$$

where α_T is a unit probability of the detected transitions. Two sequential data are needed because only falling transition is considered. Thus, α_T is 1/16 in this case. σ is the standard deviation of $\phi_{e,r}$, which is the random term of the phase difference. Since the phase error input is assumed as a Gaussian distribution, $\mathcal{N}()$ is the Probability Density Function of the Standard normal distribution defined by:

$$\mathcal{N}(x) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) \tag{4.13}$$

Using the overall noise gain and the PD's outputs, a power of quantization error can be calculated. The absolute value of ϕ_u can be considered as 1 or 0 in binary output and calculated as

$$E[\phi_u^2] = E\left[\left(K_R\phi_{e,r} + \phi_q\right)^2\right] = K_{R,A}^2 E\left[\phi_{e,r}^2\right] + E\left[\phi_q^2\right] \tag{4.14}$$

With (4.12) and (4.14), the variance of quantization error, ${\sigma_{q,A}}^2$, can be obtained as:

$$\sigma_{q,A}^2 = E[\phi_u^2] - K_{R,A}^2 E\left[\phi_{e,r}^2\right] = 2\alpha_T - \left(4\alpha_T \mathcal{N}\left(\frac{d}{\sigma}\right)\right)^2 \tag{4.15}$$

The variance of quantization noise is perceived as the amount of jitter injected by PD. Therefore, (4.15) means the ratio of the LD and the standard deviation of random phase noise, d/σ, should be small to lower the jitter in the system. However, d/σ is generally decided by the system, and it is difficult to change its value.

4.5.2 Asymmetric-Weighted PD with DFE

Now, we examine the proposed asymmetric-weighted PD with the DFE, denoted as Case B. For the same reason as 4.5.1, biased-reference technique is adopted. With the asymmetric weights, the UP/DN weights are $\alpha/2-\alpha$ and $2-\alpha/\alpha$ for the 3-level transition and the 2-level transition, respectively. The gain factors of them, $K_{R,3-level}$ and $K_{R,2-level}$, are given by calculation of:

$$K_{R,3-level} = \frac{\left(\alpha \int_{-\infty}^{-d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r} + (2-\alpha) \int_{-d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_{e,r}}^2\right]}$$

$$= \left(\alpha \mathcal{N}\left(\frac{d}{\sigma}\right) + (2-\alpha)\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} = 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \qquad (4.16)$$

$$K_{R,2-level} = \frac{\left((2-\alpha) \int_{-\infty}^{+d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r} + \alpha \int_{+d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_{e,r}}^2\right]}$$

$$= \left((2-\alpha)\mathcal{N}\left(\frac{d}{\sigma}\right) + \alpha\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} = 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \qquad (4.17)$$

where $f_{e,r}(\phi_{e,r})$ is the probability density function of the phase error $\phi_{e,r}$.

From (4.10), (4.16), and (4.17), the proposed PD has the same gain factors as the SS-MMPD. Therefore, the overall noise gain, $K_{R,\mathrm{B}}$, is calculated in the same way as Case A.

$$K_{R,B} = 2\alpha_T \left(2\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} \tag{4.18}$$

However, the phase output ϕ_u is not a binary output but is determined by α, 0, or $2-\alpha$ according to the output of PD in each transition. Consequently, the power of PD output is expressed as

$$\begin{aligned}
&\mathrm{E}[\phi_u^2] = \sum_X \mathrm{Prob}[\phi_u]\,\phi_u^2 \\
&= \mathrm{Prob}[3\text{–level}]\begin{pmatrix} \mathrm{Prob}\left[\phi_{e,r} < -d \;\middle|\; 3\text{–level}\right] * \alpha^2 \\ +\mathrm{Prob}\left[\phi_{e,r} > -d \;\middle|\; 3\text{–level}\right] * (2-\alpha)^2 \end{pmatrix} \\
&+ \mathrm{Prob}[2\text{–level}]\begin{pmatrix} \mathrm{Prob}\left[\phi_{e,r} > d \;\middle|\; 2\text{–level}\right] * \alpha^2 \\ +\mathrm{Prob}\left[\phi_{e,r} < d \;\middle|\; 2\text{–level}\right] * (2-\alpha)^2 \end{pmatrix} \\
&= 2\alpha_T \left(\left(1 - \Phi\left(\frac{d}{\sigma}\right)\right)\alpha^2 + \Phi\left(\frac{d}{\sigma}\right)(2-\alpha)^2 \right)
\end{aligned} \tag{4.19}$$

where α_T is the same as the value in Case A. The UP/DN probabilities are different according to d/σ, thus optimum α is dependent on d/σ. To minimize ${\sigma_q}^2 = \mathrm{E}\left[{\phi_u}^2\right] - {K_R}^2\mathrm{E}[{\phi_{e,r}}^2]$ compared with Case A, $\mathrm{E}\left[{\phi_u}^2\right]$ should be minimized because ${K_R}^2\mathrm{E}[{\phi_{e,r}}^2]$ is the same. To minimize $\mathrm{E}\left[{\phi_u}^2\right]$, a function is defined, and the differential value is found to be 0, as shown in the following formula:

$$y(\alpha) = \left(1 - \Phi\left(\frac{d}{\sigma}\right)\right)\alpha^2 + \Phi\left(\frac{d}{\sigma}\right)(2-\alpha)^2$$

$$\frac{\partial y(\alpha)}{\partial \alpha} = 0, \qquad \alpha = 2\Phi\left(\frac{d}{\sigma}\right) \tag{4.20}$$

As a result, the optimum α calculated in this case is the same as the optimum α, obtained to match the lock points in Section 4.4.1. The quantization noise power is obtained by adding the obtained optimum α value:

$$\sigma_{q,B}^2 = E[\phi_u^2] - K_{R,B}^2 E\left[\phi_{e,r}^2\right]$$

$$= 2\alpha_T\left(4\Phi\left(\frac{d}{\sigma}\right)\left(1 - \Phi\left(\frac{d}{\sigma}\right)\right)\right) - \left(4\alpha_T \mathcal{N}\left(\frac{d}{\sigma}\right)\right)^2 \tag{4.21}$$

Since the variance of quantization noise in Case B, ${\sigma_{q,B}}^2$, is also dependent on d/σ, there is a limit to reducing the jitter injected in the CDR by the PD. However, it is always smaller than ${\sigma_{q,A}}^2$ when using optimum α, which shows better performance in jitter characteristics.

4.5.3 Conventional SS-MMPD without DFE

In this case, denoted as Case C, a typical SS-MMPD without DFE is analyzed, where the α of 3-level, 2-level rising, and 2-level falling transitions are 1. For the 3-level, the phase detected as the phase error is at the lock point, so LD is zero. However, for both cases of 2-level rising and 2-level falling, each LD is not zero, therefore the gain factors of 2-level rising and 2-level falling, $K_{R,2-level\_\mathrm{rise}}$ and $K_{R,2-level\_\mathrm{fall}}$ are different from the 3-level gain factor, $K_{R,3-level}$:

$$K_{R,3-level} = \sqrt{\frac{2}{\pi}}\frac{1}{\sigma} \tag{4.22}$$

$$\begin{aligned} K_{R,2-level\_rise} &= K_{R,2-level\_\mathrm{fall}} \\ &= \frac{\left(\int_{-\infty}^{-d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_e + \int_{-d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_e}^2\right]} \\ &= 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \end{aligned} \tag{4.23}$$

Overall noise gain $K_{R,C}$ is calculated using (4.23):

$$K_{R,C} = 2\alpha_{T'}\left(\sqrt{\frac{2}{\pi}} + 2\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} \tag{4.24}$$

In (4.24), $\alpha_{T'}$ is 1/64 because three sequential data are needed. The quantization

noise power is obtained in the same way:

$$\begin{aligned}\sigma_{q,C}^2 &= E[\phi_u^2] - K_{R,C}^2 E\left[\phi_{e,r}^2\right] \\ &= 4\alpha_{T'} - \left(2\alpha_{T'}\sqrt{\frac{2}{\pi}} + 4\alpha_{T'}\mathcal{N}\left(\frac{d}{\sigma}\right)\right)^2 \end{aligned} \tag{4.25}$$

4.5.4 Asymmetric-Weighted PD without DFE

The gain factor of 3-level transition, $K_{R,3-level}$ is the same as that in Case C. This case is denoted as Case D. In the same way above, gain factors of them, $K_{R,2-level\_rise}$ and $K_{R,2-level\_fall}$, are given by calculation of:

$$K_{R,2-level\_rise}$$
$$= \frac{\left(\alpha \int_{-\infty}^{-d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r} + (2-\alpha) \int_{-d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_{e,r}}^2\right]}$$
$$= \left(\alpha \mathcal{N}\left(\frac{d}{\sigma}\right) + (2-\alpha)\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} = 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \quad (4.26)$$

$$K_{R,2-level\_fall}$$
$$= \frac{\left((2-\alpha) \int_{-\infty}^{+d} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r} + \alpha \int_{+d}^{+\infty} \phi_{e,r} f_{e,r}(\phi_{e,r}) d\phi_{e,r}\right)}{E\left[{\phi_{e,r}}^2\right]}$$
$$= \left((2-\alpha) \mathcal{N}\left(\frac{d}{\sigma}\right) + \alpha\mathcal{N}\left(\frac{d}{\sigma}\right)\right)\frac{1}{\sigma} = 2\mathcal{N}\left(\frac{d}{\sigma}\right)\frac{1}{\sigma} \quad (4.27)$$

Since each gain factor of the 2-level rising and the 2-level falling transition is the same as the gain factor in Case C, the overall noise gain $K_{R,D}$ is also the same as the noise gain in Case D. The power of the PD output is calculated as follows:

$$\mathrm{E}[\phi_u^2] = \sum_X \mathrm{Prob}[\phi_u]\,\phi_u^2$$

$$= \mathrm{Prob}[3-\mathrm{level}]$$

$$+ \mathrm{Prob}[2-\mathrm{level\_rise}]\begin{pmatrix}\mathrm{Prob}\left[\phi_{e,r} < -d \;\middle|\; 2-\mathrm{level\_rise}\right] * \alpha^2 \\ +\mathrm{Prob}\left[\phi_{e,r} > -d \;\middle|\; 2-\mathrm{level\_rise}\right] * (2-\alpha)^2\end{pmatrix}$$

$$+ \mathrm{Prob}[2-\mathrm{level\_fall}]\begin{pmatrix}\mathrm{Prob}\left[\phi_{e,r} > d \;\middle|\; 2-\mathrm{level\_fall}\right] * \alpha^2 \\ +\mathrm{Prob}\left[\phi_{e,r} < d \;\middle|\; 2-\mathrm{level\_fall}\right] * (2-\alpha)^2\end{pmatrix}$$

$$= 2\alpha_{T'} + 2\alpha_{T'}\left(\left(1-\Phi\left(\frac{d}{\sigma}\right)\right)\alpha^2 + \Phi\left(\frac{d}{\sigma}\right)(2-\alpha)^2\right) \quad (4.28)$$

$\alpha_{T'}$ is the same as the value in Case C. Optimum α calculated in this case is the same as the optimum α obtained in Section 4.4.1. The quantization noise power is obtained by adding the obtained optimum α value:

$$\sigma_{q,D}^2 = E[\phi_u^2] - K_{R,D}^2 E\left[\phi_{e,r}^2\right]$$

$$= 2\alpha_{T'}\left(1 + 4\Phi\left(\frac{d}{\sigma}\right)\left(1-\Phi\left(\frac{d}{\sigma}\right)\right)\right) - \left(2\alpha_{T'}\sqrt{\frac{2}{\pi}} + 4\alpha_{T'}\mathcal{N}\left(\frac{d}{\sigma}\right)\right)^2 \quad (4.29)$$

4.5.5 Comparison

In general, since the noise gains of the phase detector are different, it is appropriate to adjust the loop gain to compare CDRs with the same bandwidth [12]. As a result, compensation gain K_C is needed for reasonable comparison when using DFE and not using DFE. For the same bandwidth, we assume the same overall equivalent gain $K_o = K_R * K_C = \sqrt{\frac{2}{\pi}}\frac{1}{\sigma}$. Since noise gain factors of Case A and B are the same ($K_{R,A} = K_{R,B}$), they have the same compensation gain, $K_{C,AB}$:

$$K_{C,AB} = \frac{4\sqrt{\frac{2}{\pi}}}{\mathcal{N}\left(\frac{d}{\sigma}\right)} \tag{4.30}$$

In the same way, the compensation gains of Case C and D are the same:

$$K_{C,CD} = \frac{32\sqrt{\frac{2}{\pi}}}{\sqrt{\frac{2}{\pi}} + 2\mathcal{N}\left(\frac{d}{\sigma}\right)} \tag{4.31}$$

The variance of the compensated quantization noise is calculated:

$$\sigma_{q,c}^2 = \sigma_q^2 K_C^2 \tag{4.32}$$

Fig. 4.14 shows the variance of the compensated quantization noise for the CDR systems based on Case A, B, C, and D by changing the LD. Again, there is no point where the expected jitter of the conventional SS-MMPD is smaller than that of the proposed PD. Further, the case of using DFE and the proposed asymmetric-weigthed PD with biased-reference technique has a better jitter performance than others.

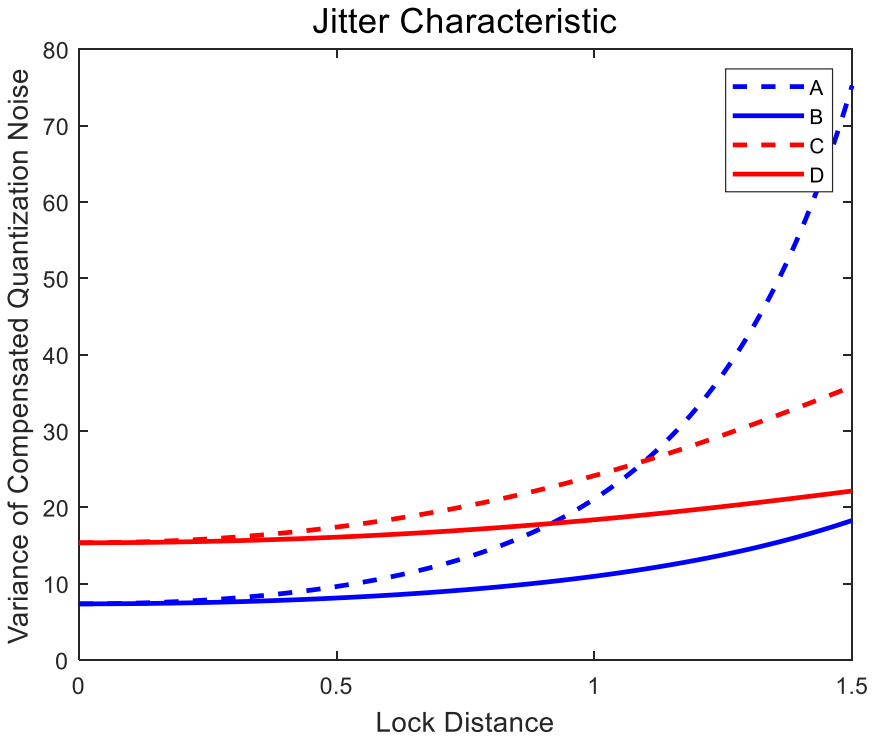
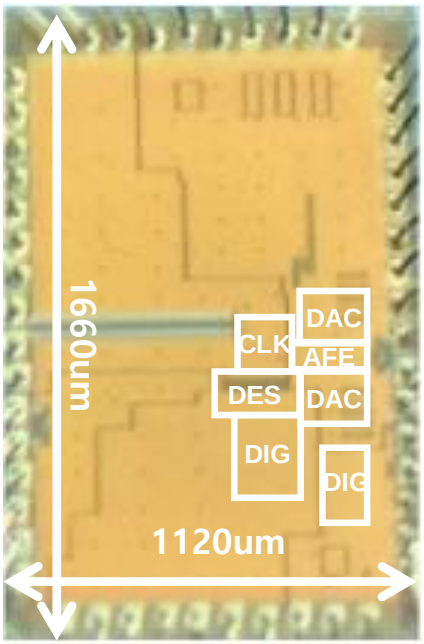


Fig. 4.14. Variance of the compensated quantization noise.

4.6 Measurement Results

The proposed PAM-4 receiver is fabricated in a 28-nm CMOS process and demonstrated at 40Gb/s with PAM-4 signaling. The chip photomicrograph and power consumption breakdown are shown in Fig. 4.15. The active area is 0.169 mm^2, and power consumption is 66 mW at 40-Gb/s. Fig. 4.16 shows the measurement set-up including the method of generating the PAM-4 signal. To generate the PAM-4 signal using two differential NRZ signals, one of the NRZ signals (Data2) is passed through a 6 dB attenuator, having a half swing of the other NRZ signal (Data1). Af-



Block Description	Area (um^2)	Power (mW)
Analog Front-end (AFE)	3300	30.8
Deserializer (DES)	4800	
Digital-to-Analog Converter (DAC)	26100	
Clock (CLK)	37500	22
Digital Logic (DIG)	97500	13.2

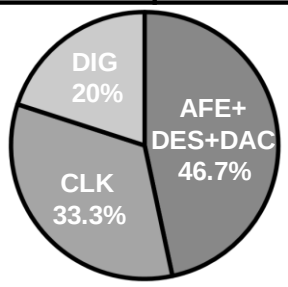


Fig. 4.15. Chip photomicrograph and power consumption breakdown.

ter that, a passive power combiner is employed to merge the two signals. The recovered data generated from the chip is forwarded to an error detector to measure a BER and JTOL.

Fig. 4.17 shows the measured bathtub curve. The receiver achieves a BER of 10^{-9} with a timing margin of 0.28 UI. To demonstrate the jitter performance of the asymmetric-weighted PD, the JTOL is measured with various α values at the BER of 10^{-6} as shown in Fig. 4.18. As mentioned in Section 4.4.1, there is no difference in the bandwidth of CDR according to the change of α value. Note that the conventional PD which has symmetric weights corresponds to the case of $\alpha = 1$. While the high-frequency JTOL is 0.23 UI_{pp} for the case of $\alpha = 1$, the JTOL is enhanced to be 0.36 UI_{pp} when α is set between 1.125 and 1.25, which has the best jitter perfor-

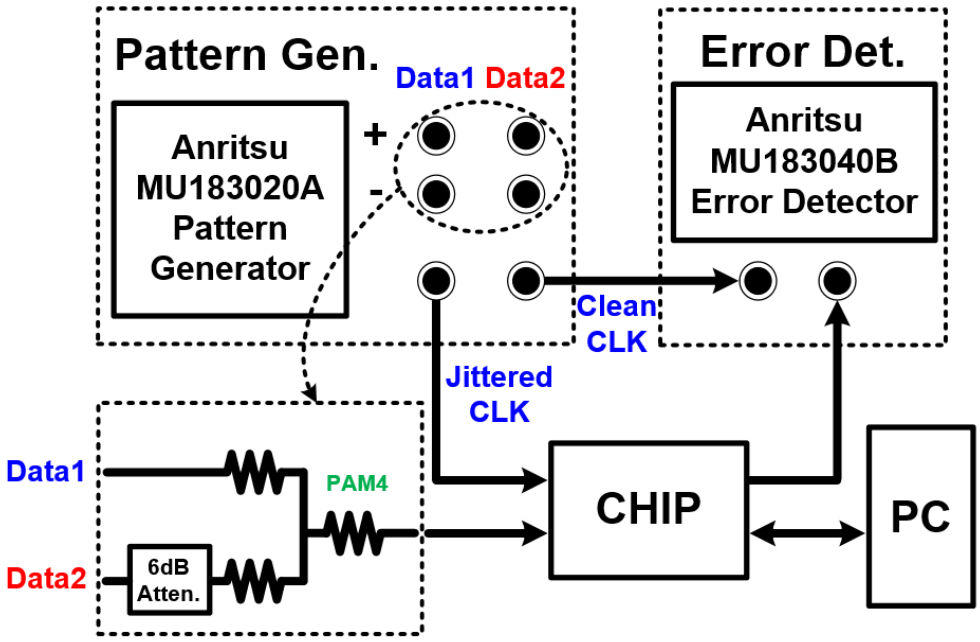


Fig. 4.16. Measurement setup.

mance under our measurement condition. However, the jitter performance is steeply degraded when α is larger than 1.25, which means the proposed PD has an optimum α. Using equations (4.15), (4.20), and (4.21), LD and the variance of the quantization noise can be expected as shown in Table 4.1. It is considered that LD exists between 0.1573 and 0.3186; thus 2~7% variance of quantization noise improvement is expected. As a result, performance improvement of up to 7% or more can be obtained under the given measurement conditions.

Optimum alpha	LD(d)	$\sigma_{q,conv}$	$\sigma_{q,pro}$	$\sigma_{q,pro}/\sigma_{q,conv}$
1.125	0.1573	0.1153	0.1133	0.98
1.25	0.3186	0.1160	0.1082	0.93

Table 4.1. Expected LD and vairance of quantization noise.

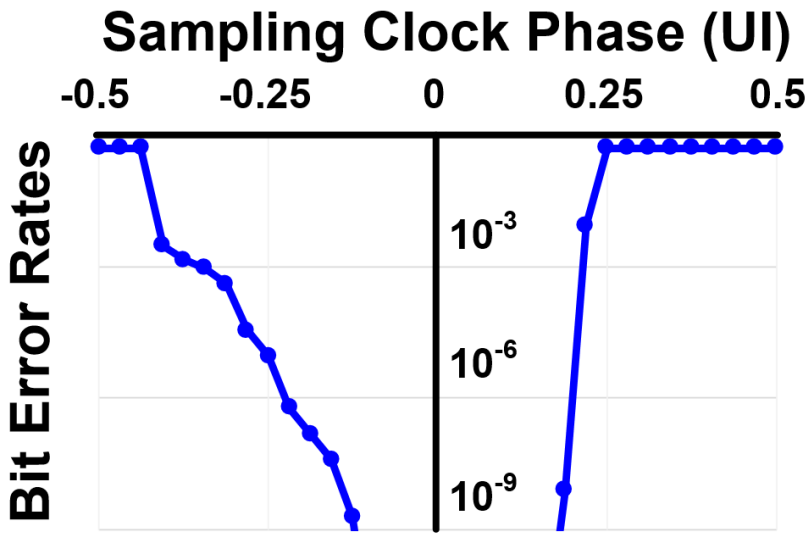


Fig. 4.17. Bathtub curve.

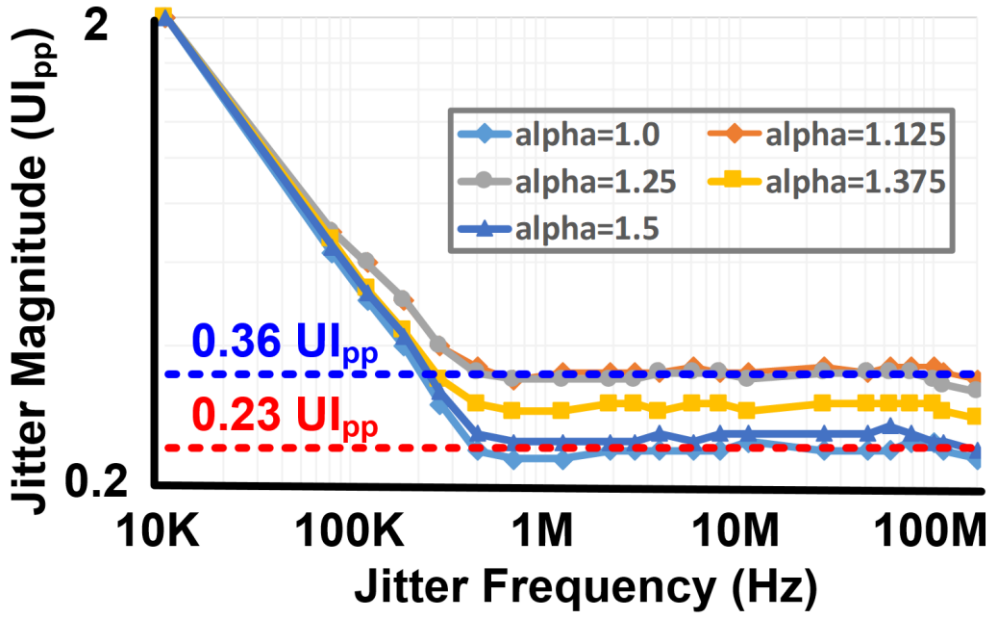


Fig. 4.18. JTOL measurement by changing the weight of asymmetric-weighted PD.

Chapter 5

Conclusion

In the first work, the TWG-CDR is proposed to provide a robust phase detector gain over a wide phase error range, using the uneven transition weight ratio of 1:2:4, where the shortest transition holds the highest weight. As a result, the proposed TWG technique resolve the false lock problem, exhibiting a lower BER than the conventional sign-sign Mueller-Müller CDR. Furthermore, the proposed TWG-CDR implements the robust phase detection algorithm mostly with digital circuits utilizing the characteristics of the PAM-4 ISI. Therefore, it is more amenable to CMOS scaling and extendable to other multilevel pulse amplitude modulations such as PAM-8 or PAM-16. Measurement results show the proposed TWG-CDR offers the highest speed of 64-Gb/s and the highest energy efficiency of 2.37pJ/b among state-of-the-art designs with similar implementation technology.

The second work investigates a low-jitter phase detection technique for the PAM-4 Baud-rate CDR. The proposed phase detection technique adopts asymmetric weighting according to the transition types to reduce the jitter caused by various

lock points in the multilevel signaling. Through pseudo-linear analysis, we demonstrated that the proposed PD exhibits a better jitter tolerance than the conventional SS-MMCDR. This technique can be adapted to other multilevel signaling, such as PAM-8, as well as PAM-4. It achieves enhanced jitter tracking performance regardless of the channel bandwidth, but a much greater effect can be seen when the bandwidth is small. These are backed by quantitative analysis and measurements. The measurement results show that the proposed receiver offers a data rate of 40-Gb/s and an energy efficiency of 1.65 pJ/b.

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초 록

본 논문에서는 보우-레이트 위상 검출 방식 (Baud-rate phase detection)을 이용하여 4 레벨 펄스 진폭 신호 변조 기술 (four-level pulse amplitude modulation)을 사용한 시스템에서 사용될 클럭 및 데이터 복원회로 (clock and data recovery)를 설계하는 방법을 제안한다. 기존 방식들에서 발생하는 위상 고정 오류 (false lock)문제를 해결하는 새로운 방식을 제안한다. 안정적인 동작을 위해 데이터 전환 종류에 따라 다른 가중치를 인가하는 전환 가중 (transition-weighted gain) 기법을 제안한다. 위상 검출 특성 및 성능 분석은 이론적인 분석 및 측정을 통해 검증하였다. 40nm CMOS 공정을 이용하여 만들어진 칩은 64 Gb/s 에서 2.37 pJ/b 의 파워 성능을 갖으며 비트 에러율 10^{-11} 이하 기준에서 문제없는 동작을 보여주었다.

위상 고정 문제를 해결하는 앞선 버전에 이어, 지터에 안정적인 동작을 할 수 있는 위상 검출기를 제안한다. 4 레벨 펄스 진폭 신호 변조 기술을 사용함에 따라 다중 위상 고정 지점 (multi lock points)으로 인해 지터 측면에서 성능이 떨어지게 된다. 이를 해결하기 위해, 위상 검출기의 두 가지 출력 (“early” and “late”)에 다른 가중치를 두어 안정적으로 동작하도록 제안하였다. 이를 통해, 제안한 비대칭 가중 방식 (asymmetric-weighted technique)을 사용하지 않을 때보다 항상 더 나은 지터 특성을 보여줌을 보여주었다. 위상 검출 특성 및 성능 분석은 이론적인 분석 및 시뮬레이션 결과 그리고 측정 결과를 통해 검증하였다. 28 nm CMOS 공정을 이용하여 만들어진 칩은 40 Gb/s 에서 66 mW 의 파워를 소모하고 0.169 mm^2 의 면적을 차지한다. PRBS7 패턴을 이용하여 측정되었으며 제안하는 클럭 및

데이터 복원회로는 비트에러율 10^{-9} 이하 기준에서 문제없는 동작을 보여주었다.

주요어 : 보우-레이트 위상 검출 방식, 4 레벨 펄스 진폭 신호 변조, 클럭 및 데이터 복원회로, 위상 고정 오류, 전환 가중, 다중 위상 고정, 비대칭 가중,

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