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High-performance organometal halide perovskite resistive memory and its current noise analysis

유무기 페로브스카이트 물질 기반의 고성능 저항 변화메모리 소자 제작 및 노이즈 분석 연구

2023 년 8 월

서울대학교 대학원

물리천문학부

안 희 범

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Abstract

High-performance organometal halide perovskite resistive memory and its current noise analysis

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Resistive random access memories have shown the potential to open a niche area in memory technology by combining the long endurance of dynamic random-access memory and the long retention time of flash memories. Recently, resistive memory devices based on organometal halide perovskite materials with ABX_3 structure (A: organic cation, B: metal ion, X: halide anion) have demonstrated outstanding memory properties, such as a low-voltage operation and a high ON/OFF ratio, which is essential for low power consumption memory devices. However, despite such advantages these perovskite-based devices present, the lack of high-density array based on pinhole-free uniform film and the random distribution in operation voltage due to stochastic formation of conducting filaments remain challenges for practical application.

This dissertation addresses both the fabrication of unipolar resistive memory devices in a cross-bar array using a non-halide lead source and the investigation of the structural properties of conducting filaments through a current noise analysis. By employing a simple single-step spin-coating method with non-halide lead source $PbAc_2$, highly uniform and dense perovskite film was achieved. As a result, high-

yield (up to 94%) unipolar memory device in an 8 × 8 crossbar array were fabricated. These devices displayed a high ON/OFF ratio up to 10^8 with a relatively low operation voltage, a large endurance, and long retention times. Furthermore, one diode-one resistor (1D-1R) scheme for preventing parasitic current path in an array was compatible with the perovskite memory device. This research demonstrates the potential for low-cost and high-density practical perovskite memory devices.

Next, by analyzing current noise from various intermediate resistance states and temperature-dependent electrical properties, I investigated the geometric features and dynamics of conducting filaments which are a nanoscale structure formed in the resistive switching medium. Resistive switching phenomena was understood in terms of percolation model, and conducting filament as a percolation path in the perovskite medium was characterized as a fractal structure whose fractal dimension was found to be 2.25. Additionally, by controlling the ion migration in the material with temperature-dependent experiment, it was suggested that robust and stable conducting filaments are formed under elevated temperature condition where ion migration is more active. These investigations enhance our understanding of the resistive switching phenomena in the organometal halide perovskites and also pave the way to control the conducting filament structure and dynamics of the switching processes for achieving stable memory operations, which is a critical step toward the implementation of perovskite-based memory technology.

Keywords: Organometal halide perovskites, Ion migration, Resistive memory (RRAM), Noise analysis, Percolation, Conductive filament.

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Chapter 1. Introduction

1.1. Resistive random access memory based on organometal halide perovskites materials

Resistive random access-memory (RRAM) has emerged as a promising candidate as the next-generation memory technology because of their advantages such as nonvolatility, low operational energy, and simple operation principles based on resistive switching effect.[1,2] Moreover, a metal−insulator−metal structure commonly used for an RRAM cell has a scaling potential in the form of a cross-bar architecture, in which memory cells are sandwiched between a set of parallel bottom electrode lines (word lines) running perpendicular to top electrode counterparts (bit lines).[3,4] The cross-bar geometry enables a highly integrated RRAM architecture with the minimum cell size defined by $4F^2$ (F = minimum feature size[3]) and has been even projected to overcome the scaling limit of current silicon-based Flash memory technologies.[4]

During the last decade, RRAM devices based on solution-processed materials have been extensively explored owing to their easy and low-cost fabrication processes. In particular, the performance of memory devices made with solution-processed organic and organic−inorganic hybrid materials[5−9] has improved significantly due to a concerted effort of creative material designs and an active pursuit of the resistive switching mechanism governing the memory operation. Among these materials, organometal halide perovskite materials with ABX_3 structure, where A is an organic cation, B is a metal ion, and X is a halide anion, have demonstrated its promising

device performances; such as a low-voltage operation, long retention time, and high ON/OFF ratio.[10−14]

1.2. Resistive switching mechanism in organometal halide perovskite materials related to conducting filaments

Almost all the organometal halide perovskite memory devices studied so far have shown bipolar resistive switching. Electrochemical metallization (ECM) is one of the widely proposed mechanisms to explain the bipolar resistive switching phenomenon. In this case, one of the electrodes is made from an electrochemically reactive metal, such as Ag. The studies by Choi et al. and Han et al. both claimed that the formation of metallic Ag filaments, which is originated from the Ag^+ migration from the electrode, contributes to the formation of conducting paths, which results in the set process in the memory device.[15,16] Oxidation of the Ag electrode due to an applied electric field generates Ag^+ which moves to the counter electrode through the perovskite layer, which lead to a spontaneous growth of a Ag metal. The migration of the Ag^+ can be understood as the thermally activated ion hopping in the perovskite layer. Under a negative voltage bias, the filament is dissolved, assisted by Joule-heating. The Ag^+ moves to the opposite direction when an opposite electric field is applied during the reset process.[16] The second proposed mechanism for bipolar resistive switching is based on the migration of halide vacancies (i.e. iodine vacancies for $MAPbI_3$) which lead to the formation of metal-halide complexes near the electrode where the halide ions are accumulated.[17] Zhu et al. verified the formation of AgI_x when Ag was used as one of the electrodes by energy-dispersive

X-ray spectroscopy measurements. They also found that the formation of the metal-halide complexes was negligible if the Au electrodes were used instead of the Ag electrode.

Both mechanisms outlined above require re-dox reaction between either metal ions and a counter electrode or halide ions and a metal electrode. Therefore, these mechanisms are inappropriate to explain the resistive switching mechanism for our device which will be described in latter part of the thesis (Au/$MAPbI_3$/Au); ECM is unlikely to occur with Au electrodes and the formation of the metal-halide complexes would be negligible for Au. Instead, our unipolar perovskite resistive memory device can be compared to the oxide-based unipolar memory which shows similar electrical characteristics. The I-V curves of many oxide-based unipolar memory devices resemble the I-V curves of our perovskite memory.[18,19]

Most of the reported oxide-based that showed unipolar resistive switching behavior had device structures with symmetric electrodes, which is the same as our perovskite memory device. For example, many oxide materials that show unipolar switching, including NiO, [18,20] TiO_2,[21] Ga_2O_3,[22] CuO,[23] Fe_2O_3,[24] ZnO,[25] had the same top and bottom electrodes (in most of the devices both electrodes are Pt which is a non-reactive metal).

One of the widely accepted mechanisms for the unipolar resistive switching behavior in oxide-based memory devices is the formation and the rupture of conducting paths composed of oxygen ion vacancies via a dominant role of a thermal driving force generated by Joule heating rather than the role of the electric field.[26] In light of the resistive switching mechanism for oxide-based unipolar memory devices, a similar

mechanism can be proposed for our unipolar perovskite memory by considering halide vacancies instead of oxygen vacancies as outlined below.

Initially, when an electric field is applied, the migration of iodine-ion vacancies (V_I's) occurs along the direction of the field (i.e. the positively charged vacancies move along the direction of the electric field and the negatively charged halide ions move in the opposite direction). This is reasonable since a highly mobile nature of V_I's is widely accepted in the community; the migration of V_I's in $MAPbI_3$ occurs easily due to a low activation energy for halide ion migration as confirmed from numerous theoretical results,[27-30] and experimental studies. [31-34] The migration of V_I's initiates aggregation of V_I's from near the negative electrode, as recently confirmed by EDX scanning measurements of a lateral Au/$MAPbI_3$/Au device upon an applied lateral electric field.[17] However, the migration of the vacancies by the applied electric field is not sufficient for a unipolar resistive switching to occur. A significant amount of Joule heating is required to induce further movement of vacancies in and out of the conducting filaments. The current through initially formed unstable conducting filaments ("soft breakdown") generates a temperature gradient radially towards the conducting filaments. In the oxide-based memory devices, the temperature gradient induces the movement of the oxygen vacancies (and simultaneously, oxygen ions) in and out of the conducting paths through two competing effects; Soret force and Fick force.[35] The Soret force attracts the vacancies towards the filaments via the movement of oxygen vacancies along the temperature gradient, whereas the Fick force pushes out the vacancies from the filaments via the movement of oxygen ions along the concentration gradient. The two microscopic forces can act in similar ways in our perovskite memory devices

such that the set process is dominated by the Soret force; V_I's are attracted and effectively condensed to form conducting paths in the perovskite film. On the other hand, the reset process would be dominated by the Fick force which leads to the outward movement of the V_I's that ruptures the conducting paths.[36] During the reset process, a smaller amount of Joule heating is required to create a small thermal gradient that makes the Fick force (proportional to concentration gradient) dominate over the Soret force (proportional to temperature gradient).[36]

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Chapter 2. Fabrication and characterization of high-performance $MAPbI_3$ resistive memory in a cross-bar array

In this chapter, I will discuss the perovskite RRAM devices in a cross-bar array structure with solution-processed $MAPbI_3$ memory elements prepared from $PbAc_2$ by a single-step spin-coating method. The characteristics of memory devices made from this deposition method showed a desirable performance, with a high ON/OFF ratio, good retention time and endurance cycles, and the low operation voltage. In addition, the uniform perovskite film produced from the $PbAc_2$ precursor achieved high-yield (up to 94%) memory devices in an 8 × 8 cross-bar array structure with uniform memory cell characteristics. Furthermore, to avoid a cross-talk interference problem among the memory cells in the 8 × 8 cross-bar array structure, we utilized one diode−one resistor (1D−1R) scheme using our perovskite RRAM devices exhibiting unipolar resistive switching behaviors.

2.1. Introduction

Resistive memory devices based on perovskite materials have shown promising device performances, such as a low-voltage operation, long retention time, and high ON/OFF ratio.[1−5] One of the well-established perovskite materials is methylammonium lead iodide ($MAPbI_3$) for which various solution-processing methods for thin-film deposition have been developed for high-efficiency optoelectronic devices, including single-step spin-coating, sequential deposition, [6−8] and solvent-engineering techniques.[9-11]

A widely used technique in perovskite film deposition for RRAM fabrication is the solvent-engineering method (or known as “solvent-dropping”), in which a fast deposition–crystallization[10] is induced by dropping a solvent during the spin-coating of a solution mixture of methylammonium iodide (MAI) and lead iodide (PbI_2).[2,3,5,12,13] Although this method has been used to produce a denser and more uniform perovskite film than the conventional single-step spin-coating method or the sequential deposition method, the film quality is extremely sensitive to the solvent-dropping conditions such as the type, amount, the time, and the position of displacement of the solvent;[10,11] this sensitivity potentially limits its applicability for large-scale film deposition. Moreover, Zhang et al.[14] discovered that the lead-containing precursor played an important role in the perovskite crystal growth and that the use of $PbAc_2$ in a simple single-step spin-coating method achieved a highly uniform and dense perovskite film without any additional solvent-engineering. Based on the high quality perovskite film achieved by non-halide lead source, we demonstrated the integration of the perovskite RRAM devices in a crossbar architecture.

2.2. Experiments

2.2.1 Device fabrication

The device fabrication process is illustrated in Figure 2.1. Au bottom electrodes with linewidths of 50 μm and a thickness of 50 nm were deposited by e-beam evaporation through a shadow mask on cleaned SiO_2/Si substrates. Two different shadow masks were used when depositing the bottom Au electrodes for 1 × 8 and 8 × 8 cross-bar array devices. The bottom electrodes and the substrate were treated with UV−ozone illumination for cleaning. The $MAPbI_3$ solution was made from solution mixtures of MAI and $PbAc_2$ dissolved in N,N-dimethylformamide at a 3:1 molar ratio to make the concentration of 0.75 M. The solution was stirred for 30 min while being heated on a hotplate at 60 °C . The heated solution was spin-coated onto the bottom electrodes in a controlled environment inside a glovebox at a rate of 3000 or 5000 rpm for 45 s. After leaving the sample for 10 min at room temperature to allow evaporation of remaining solvent in the sample, the sample was heated at 100 °C for 5 min to initiate the formation of $MAPbI_3$ crystals.

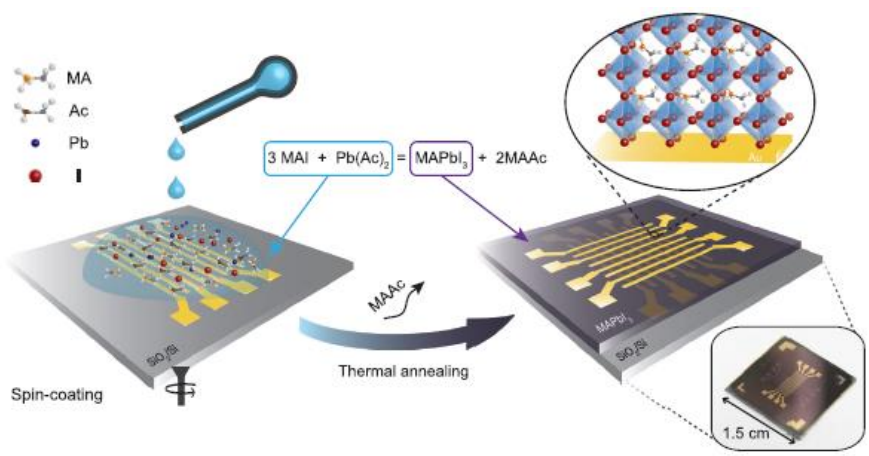

Figure 2.1 A schematic image of the fabrication process for $MAPbI_3$ memory devices.

The top Au electrodes with linewidths of 50 μm and a thickness of 100 nm were deposited through a shadow mask by electron beam evaporation. The memory cell size was defined as 50 μm × 50 μm.

Figure 2.2 shows the cross-sectional and top surface images of fabricated perovskite film measured by a field emission scanning electron microscope (SEM) (Figure 2.2(a),(b), respectively). A typical size of the grains formed in the film was found to be =150 nm, which is a similar value compared to that reported in the literature.[15] The crystal structure of the $MAPbI_3$ film was confirmed to be identical to that of a film deposited via a conventional PbI_2 precursor[14] according to X-ray diffraction (XRD) data (Figure 2.2(c)), except that the peak corresponding to PbI_2 at $2\theta = 12.5°$ is significantly smaller in the $PbAc_2$-based film. This result reflects a more complete conversion of the precursors to perovskite crystals in our film compared to the conventional spin-coating method.[15]

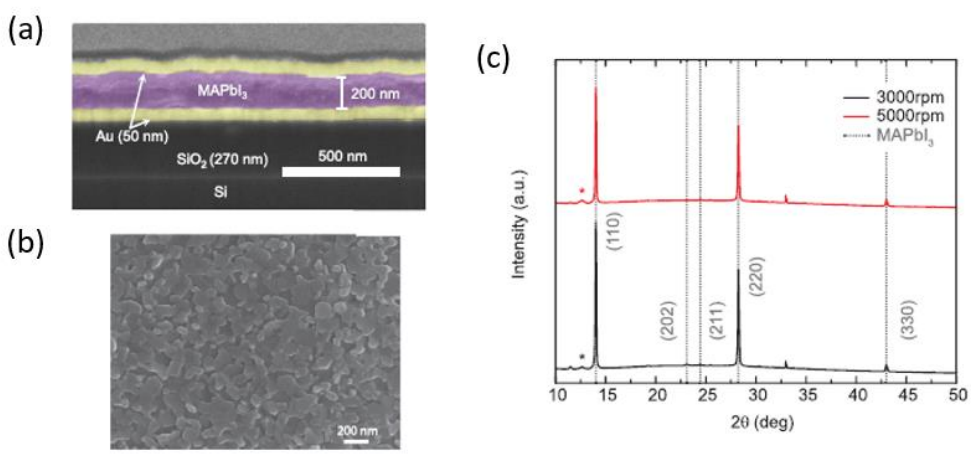

Figure 2.2 (a) A cross-sectional SEM image of the Au/$MAPbI_3$/Au on a SiO_2/Si substrate. (b) The top surface SEM image of a $MAPbI_3$ film. (c) XRD spectra of $MAPbI_3$ films spin-coated at 3000 rpm (red line) and 5000 rpm (black line).

Compactness and smoothness of the $PbAc_2$-based perovskite film was confirmed also with an atomic force microscope (AFM). The high-quality perovskite film is an essential requirement in achieving high-yield memory devices.

2.2.2 Electrical characterization.

The electrical measurements were performed using a semiconductor parameter analyzer (Keithley 4200 SCS) in a vacuum environment ($\approx 10^{-3}$ Torr). The scan rate of the voltage sweep in I–V measurements was typically 0.54 V s^{-1}. The voltage bias was applied to the top Au electrode while the bottom Au bottom was grounded.

2.3. Results and discussion

2.3.1 Electrical characteristics of single perovskite memory device

To investigate the properties of our memory cells, we first fabricated 1 × 8 cross-bar array memory cells with the perovskite film deposited as described above. The memory cells showed typical current−voltage (I–V) characteristics that represent unipolar resistive switching behaviors, as shown in Figure 2.3(a). The first I−V sweep of the memory cell (indicated as process 1 in Figure 2.3(a)), originally in the high-resistance state (HRS or OFF state), underwent forming at a typically high voltage (of ≈ 2.7 V), while the compliance current was set to 200 μA. The device switched to low-resistance state (LRS or ON state) during the forming process. The reset process (process 2 in Figure 2.3(a)) involved a subsequent I−V sweep from 0 V under no compliance. The current increased beyond the compliance current set in the forming process and underwent a rapid reduction in the current at 0.55 V which is the reset voltage. The memory cell was then switched back to HRS. The HRS could be switched to LRS again via the set process which was a new I−V sweep starting from 0 V (process 3 in Figure 2.3(a)). The current increased rapidly at ≈0.96 V, which is the set voltage. Note that these characteristics unambiguously represent unipolar resistive switching and resemble that of well-established unipolar metal-oxide-based resistive memory devices made with TiO_2, SiO_x, and NiO_x.[16−20] The relatively low-voltage operation demonstrated above is a common feature of perovskite resistive memory devices.[1−5] The average set and reset voltages in our study were 1.16 and 0.46 V, respectively, with a certain distribution. Based on the thickness (200 nm) of the perovskite film determined by the cross-sectional scanning

electron microscope (SEM) image (Figure 2.2(a)), the average electric field required for set and reset were 5.8 and 2.3 MV m^{-1}, respectively, the same order of magnitude as those of the reported bipolar memory devices based on organometal iodide perovskite.[2−4] From the I–V curves in Figure 2.3(a), we determined the ON/OFF ratio in our perovskite memory devices to be ≈10^8 (Figure 2.3(b)), which can be considered a high ON/OFF ratio reported for the resistive memories fabricated with various types of materials.

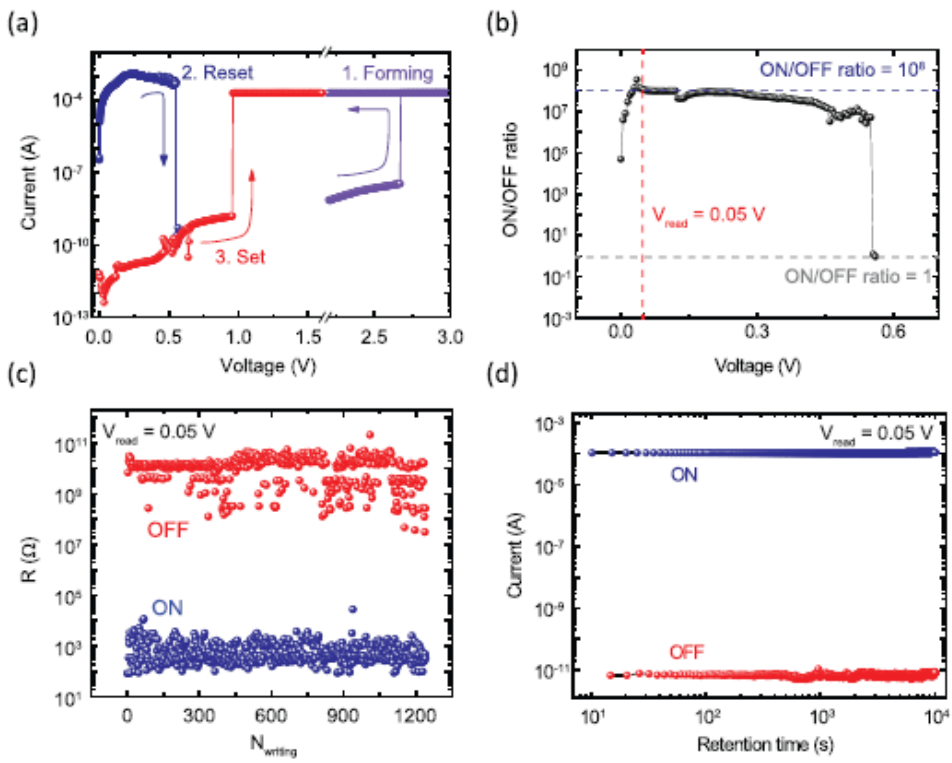

Figure 2.3 (a) Representative I-V curve of a unipolar Au/$MAPbI_3$/Au device. (b) The ON/OFF ratio as a function of voltage. (c) The electrical endurance test and (d) the retention test results.

In addition to the excellent ON/OFF ratio and the low-voltage operation of the perovskite resistive memory devices, the memory showed stable electrical characteristics from both a relatively large endurance of >1000 writings with the average ON/OFF ratio $\approx 2 \times 10^7$ and a long retention time of over 10^4 s (Figure 2.3(c),(d)). The reading voltage was chosen as 0.05 V in order to avoid unintentional switching of the memory devices during the measurements. The memory devices also exhibited stable multilevel resistance states that could be accessed by using different compliance currents during the set process, which will be discussed in the latter part of the thesis.

The perovskite memory devices fabricated in this study are unique in that they exhibit unipolar (or nonpolar) resistive switching unlike most of the reported $MAPbI_3$ and other solution-processed perovskite-based memory devices, which showed bipolar resistive switching. The main difference of this memory device is that we employed symmetric Au electrodes ($Au/MAPbI_3/Au$) unlike the other studies. Since Au is unlikely to react electrochemically, any resistive switching mechanisms that involve redox reaction between active metal ions (e.g., Ag) and a counter electrode of halide ions are inappropriate.

One of the widely accepted mechanisms for explaining the non-polarity of unipolar resistive memory devices is the formation and rupture of conducting paths composed of anion vacancies via a dominant role of a thermal driving force generated by Joule heating rather than the role of the electric field. In light of the resistive switching mechanism for oxide-based unipolar memory devices, many of which show I-V characteristics that resemble our unipolar perovskite memory devices, a similar mechanism can be proposed by considering iodine ion vacancies

instead of oxygen vacancies. The formation and dissolution of the conducting paths can be explained in terms of two competing forces that drive the diffusion of halide ion vacancies; one via a thermal gradient (Soret force) and one via a vacancy concentration gradient (Fick force) both of which are induced by Joule heating. Detailed explanation of the resistive switching mechanism in our unipolar memory devices will be discussed in the latter part of the thesis.

2.3.2 Electrical characteristics of the 8 × 8 cross-bar array

Most of the device architectures for perovskite RRAM have been limited to dot-array structures and there have only been a few reports that directly demonstrated the integration of the perovskite RRAM in a cross-bar architecture. In our study, we fabricated high-yield perovskite memory devices in an 8 × 8 cross-bar array structure with the solution-processed perovskite film deposited with $PbAc_2$. The resistances values of the LRS and HRS of each memory cell (64 cells in total) are shown as color maps in Figure 2.4(a) and Figure 2.4(b), respectively. The yield of the memory devices was found to be ≈86% (55 devices out of 64 devices were functional) (Figure 2.4(a),(b)) (A good in-wafer uniformity of the crossbar-array device is also supported from the data for a crossbar-array device with the device yield of 94%, shown in Figure 2.5). The nine devices that could not be turned off were short-circuited after the forming process. In addition, the device-to-device variation was found to be small. The resistance values of the LRS and HRS are plotted cell by cell in Figure 2.4(c). The plot reflects well-defined bistable states in our perovskite memory devices in the cross-bar array structure. In particular, the high average ON/OFF ratio of 10^6 is unprecedented in cross-bar array perovskite RRAM devices. Moreover, the

distributions of the resistance values of LRS and HRS were found to be narrow; ≈1 order of magnitude range for LRS and ≈2 orders of magnitude range for HRS (see the insets of Figure 2.4(a),(b),(d)). The maximum LRS resistance was found to be ≈2 × 10^4 times smaller than the minimum HRS resistance. The in-wafer uniformity of set and reset operation voltages is also a critical requirement for an accurate operation of large crossbar-array memory devices. Although the overlap between the set and reset voltage distributions was found, its effect is not significantly large to induce erase failure.

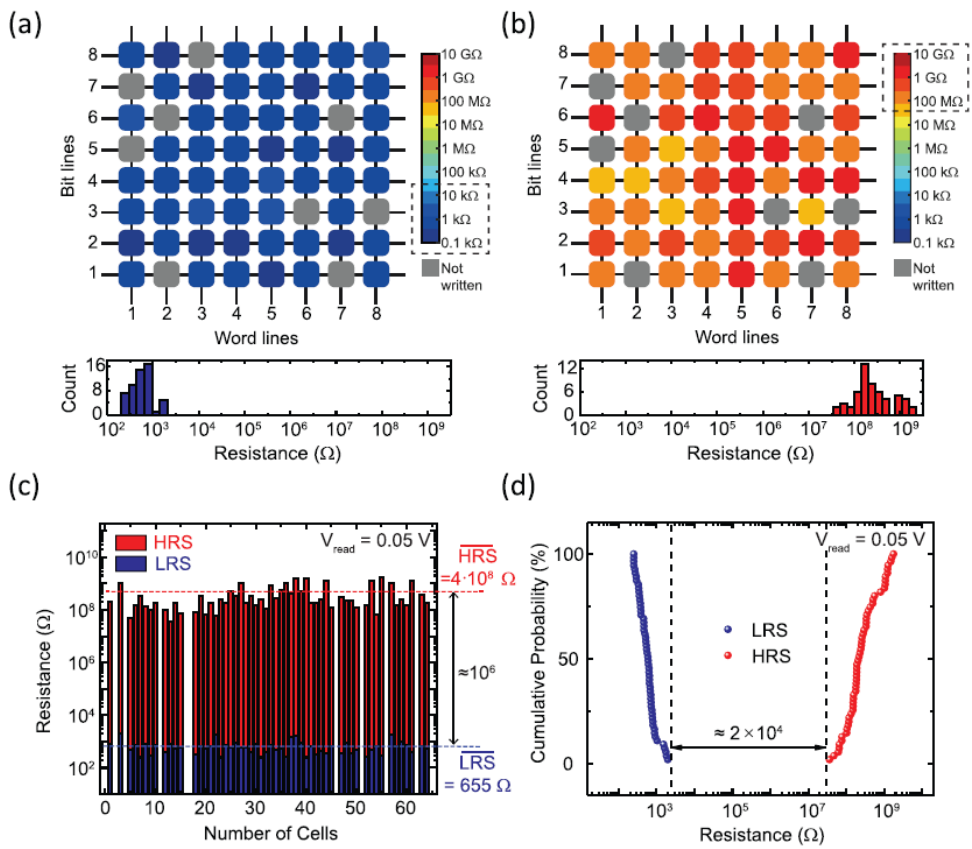

Figure 2.4 The color map plots of the resistance distribution of the 64 memory cells in the (a) LRS (b) and HRS. The gray cells indicate short-circuited devices. (c) The resistance values of the memory cells. (d) The cumulative probability plot for the resistance values of the LRS and HRS.

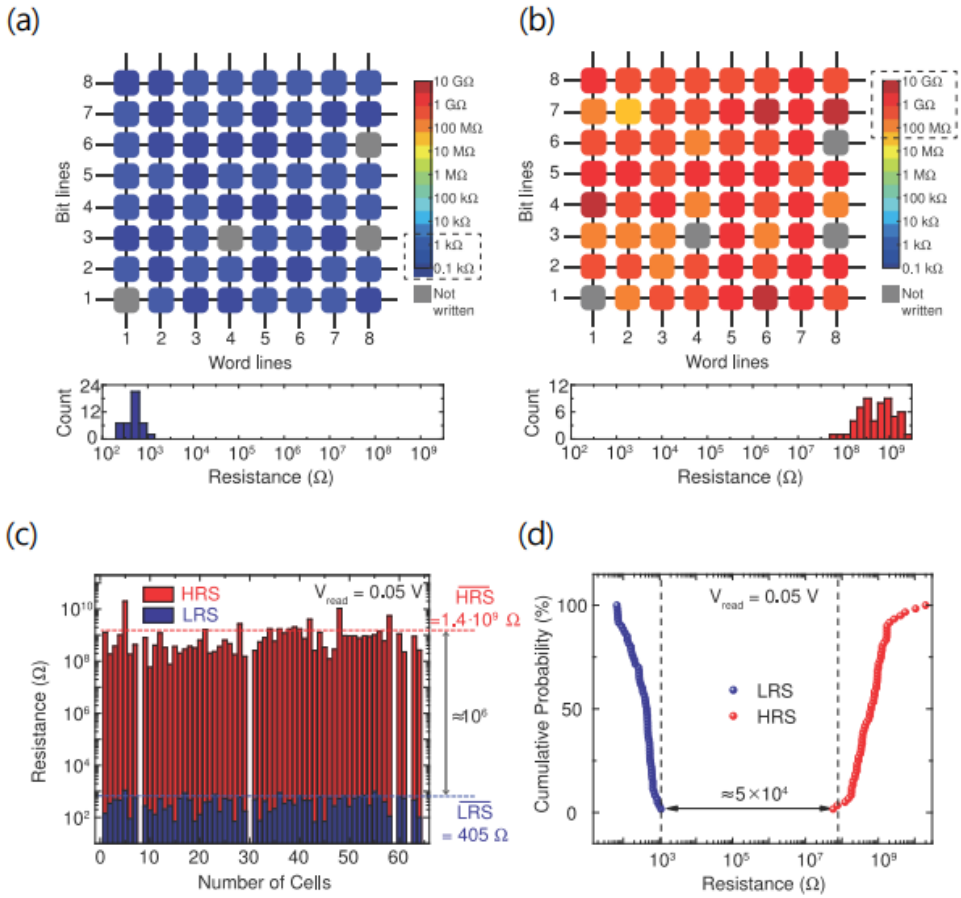

Figure 2.5 The color map plots of the resistance distribution of the 64 memory cells in the best-yield device (a) LRS (b) and HRS. The gray cells indicate short-circuited devices. (c) The resistance values of the memory cells. (d) The cumulative probability plot for the resistance values of the LRS and HRS.

2.3.3 Compatibility with the 1diode-1resistor (1D-1R) scheme

Although the crossbar-array structure guarantees an excellent scaling potential, the pure passive cross-bar array structure suffers from cross-talk interference between interconnected memory cells, thereby preventing a reliable reading operation of a selected memory cell due to parasitic conducting paths composed of interconnects and the neighboring cells.[21,22] Here, we demonstrate that the cross-talk interference can be significantly reduced by employing the 1D−1R scheme[23−25] in perovskite RRAM devices connected to external diodes. The 1D−1R scheme is feasible with memory cells that exhibit unipolar resistive switching.[26]

Before integrating external diode elements for achieving the 1D−1R scheme, we note that the requirements for the diodes are quite strict because of the low operation voltages of the perovskite memory cells. Therefore, we employed commercial diodes (1N4007 Fairchild Semiconductor) with a low operation voltage to examine their compatibilities with the perovskite memory devices exhibiting typical I–V characteristics shown in Figure 2.6(a). The diode shows a good rectification ratio of $\approx 1.5 \times 10^5$ at the voltage of 0.5 V (chosen as the reading voltage). When electrically connected in a series with the unipolar perovskite memory cells (typical I–V characteristics shown in Figure 2.6(b)), the resulting 1D−1R cell showed a current-rectified property (Figure 2.6(c)). The set voltage remained the same when the memory cell was connected to the diode, whereas the reset voltage shifted to a higher voltage due to an extra series resistance from the diode. The diode has a finite on-current limit at the voltage below 0.5 V and limits the current through the whole circuit. This may result in an insufficient amount of Joule heating required for the reset process, which plays critical role in reset process. In addition, the ON/OFF ratio

is still high (≈10^5) but lower than the average ON/OFF ratio of the memory cells alone due to the finite resistance of the diode. The 1D−1R cell also preserved a reliable retention (longer than 10^4 s) and stable electrical endurance properties (more than 500 writings with the average ON/OFF ratio ≈ 2×10^4) of the original $MAPbI_3$ perovskite memory cell.

In a pure passive cross-bar array structure of memory cells (1R array), neighboring 2 × 2 cells can be described with an equivalent circuit of one memory cell and three memory cells in parallel connection. The total current measured in this circuit, I_{total}, will be a combination of the current through a selected cell, I_{OFF}, and the parasitic current through the three cells, I_{sneak}. This is known as the cross-talk phenomenon, which induces misreading of a selected memory cell. When we read the resistance of an OFF cell ((1,1) in Figure 2.6(d)) surrounded by three neighboring cells ((1,2), (2,2), and (2,1) in Figure 2.5(d)) that were turned ON, the measured resistance of 508 Ω (see Figure 2.6(e)) nearly corresponded to that of an ON state. Therefore, this leakage current through the sneak path, I_{sneak} (shown in Figure 2.6(d)), prevents a selective reading/operation of memory cells because it is much larger than I_{OFF}. This also ultimately limits the overall scaling advantage of RRAM because of the requirements for relatively large sensing circuits to prevent reading errors.[21] In this study, we demonstrate an effective 1D−1R scheme by connecting four different memory cells through an external circuit that contains four diodes via wire bonding (see Figure 2.6(f)). Different from the four neighboring cells in 1R array (above), the resistance value read for the (1,1) cell clearly showed the reduction in the cross-talk. The read resistance was found to be 270 MΩ at the read voltage of 0.5 V, even if the (1,2), (2,1), and (2,2) cells were all turned ON (i.e., their resistance values were more

than four orders of magnitude lower than that of the (1,1) cell) (see Figure 2.6(g)). This is a clear indication that the I_{sneak} is suppressed by the diodes that are connected in opposite configurations to one another in the parasitic current path that connects the cells (1,2), (2,1), and (2,2). Our results demonstrated the selective operation of unipolar perovskite memory cells in 1D−1R scheme. Note that the resistance measurement was performed after carefully checking the resistance and electrical connection of each component in the connected circuit in order to eliminate any artifacts in the measurement (see Figure 2.7). In overall, our demonstration of suppressed cross-talk interference can be taken further and used as guidelines for developing a large array size on-chip 1D−1R perovskite memory architecture.

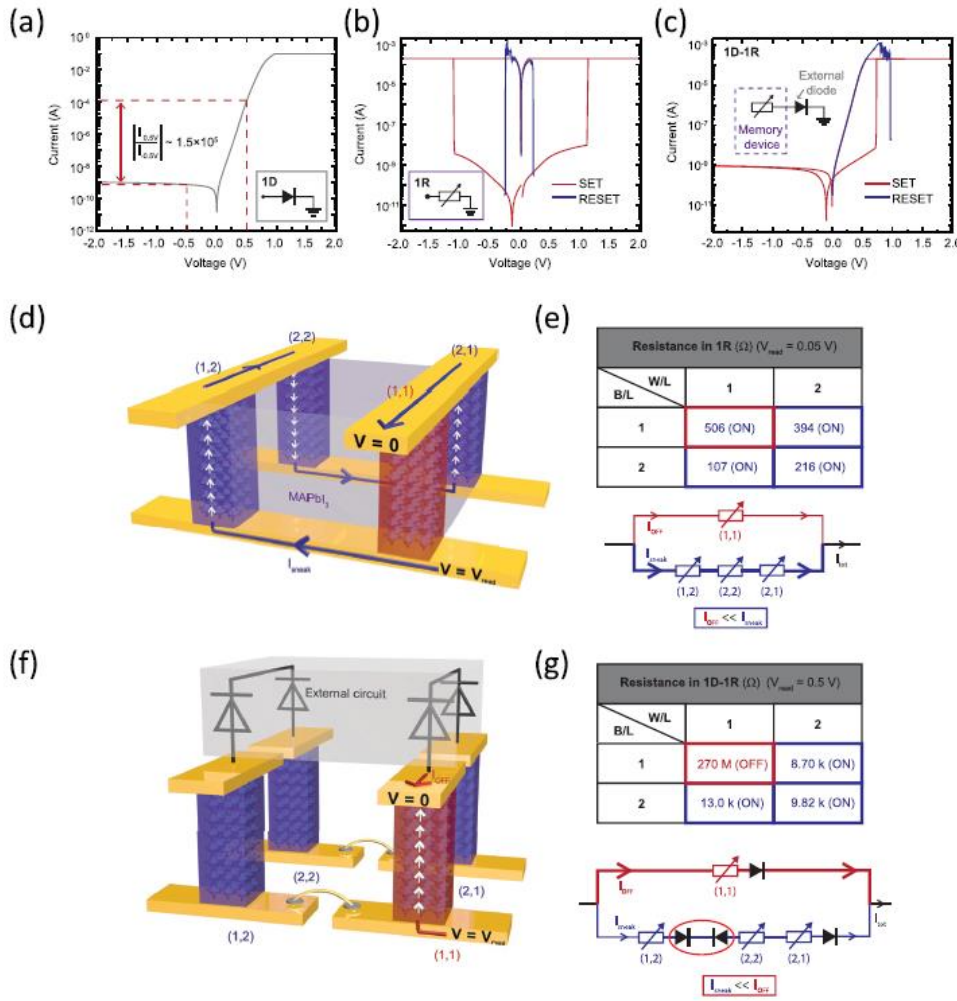

Figure 2.6 (a) The I-V curve of the external diode used for the 1D-1R scheme. (b) A typical I-V curve of the unipolar perovskite memory used for the 1D-1R scheme. (c) The I-V curve of the diode and the memory device connected in series, showing a rectification behavior. (d) A schematic diagram illustrating the reading operation of the (1,1) cell in a 2 × 2 array memory cells with cross-talk interference (e) The resistance values of each cell and the equivalent circuit of the 2 × 2 array memory cells. (f) A schematic illustration of the same reading operation in a 2 × 2 array in 1D-1R scheme. (g) The resistance values of each cell and the equivalent circuit of the 2 × 2 array memory cells in 1D-1R scheme.

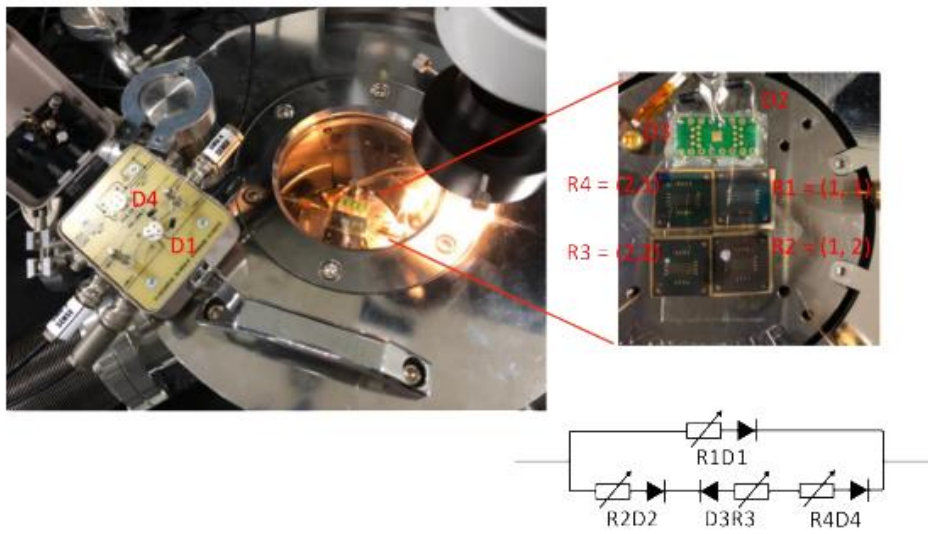

Figure 2.7 The cross-talk measurement configuration with labels shown in red. R1, R2, R3, and R4 represent (1,1), (1,2), (2,2) and (2,1) cells, respectively, from Figures 2.6(f) and 2.6(g). The circuit diagram shown at the bottom right corner shows the equivalent circuit for the measurement.

2.4. Conclusion

In this chapter, we demonstrated high-performance resistive memory devices based on organometal halide ($MAPbI_3$) perovskite films prepared with a $PbAc_2$ precursor via a simple single-step spin-coating method. The perovskite memory devices exhibited a unipolar resistive switching behavior in Au/$MAPbI_3$/Au structure with a high ON/OFF ratio of up to 10^8 and with an excellent stability, as confirmed from the endurance (more than 1000 writing cycles) and retention (>10^4 s) test results. In addition, the reliability of the perovskite memory devices integrated in an 8 × 8 cross-bar array architecture was demonstrated, achieving a high yield of up to 94% and uniform memory cell characteristics. Furthermore, the demonstration of 1D−1R scheme using our perovskite memory devices demonstrated a selective operation of memory cells by suppressing the cross-talk interference between neighboring cells connected via external diodes. These results are highly relevant for realizing low-cost and high-density practical perovskite memory devices via a simple solution process.

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Chapter 3. Characterization of percolative conducting filaments in organometal perovskite RRAM using current noise analysis

In this chapter, we observe and systematically analyze the noise scaling in various resistance states in perovskite unipolar resistive memory devices consisting of $MAPbI_3$ thin film as the active layer and a pair of symmetrical Au electrodes. By employing the model of percolation clusters with fractal geometry, the scaling behavior could be correlated to conducting filament with particular structures with a fractal dimension in an organometal perovskite. We investigate how the current fluctuation of conducting filaments occurs at different temperatures through the current noise measurement in the time domain. The study on conducting filament geometry in perovskites will contribute to an understanding of each resistance state in the material, leading to stable resistive memory operations based on perovskite materials.

3.1. Introduction

Organometal halide perovskite has attracted significant attention as a resistive switching material. However, there are only a few studies on mechanistic investigation of their switching properties, instead of enhancing their performance. Various mechanisms have been proposed for the resistive switching phenomenon of organic materials and metal oxides,[3,4] but many studies have suggested the formation and rupture of conducting filaments as the origin of resistive switching phenomena in organometal halide perovskite.[1,2,5−7] There is a consensus in the community that iodine vacancy with the lowest activation energy of migration plays a significant role in resistive switching.[2,5,8,9] Since these mobile point-defects are abundant in the material due to their low formation energy, metal ions from

electrochemically active electrodes, such as Ag, can easily migrate to form a metallic filament through a redox reaction,[1,10] or vacancies can aggregate to form conductive clusters; thus, creating conducting filaments.[2,5−7]

By setting compliance current or controlling operation voltage, the growth of conducting filament can be controlled, which may lead to multistate operation in a resistive memory. Many studies have reported various intermediate resistance states (IRSs) in the organometal perovskite memory devices. However, the nature of different IRSs, which is related to the structure of conducting filaments in the material, has rarely been investigated. Moreover, a random structure of conducting filaments results in cycle-to-cycle and device-to-device variations in the perovskite memory devices. Therefore, understanding and controlling the structures of conducting filament is a key factor for determining the device's performance.[11,12] Several attempts have been made to observe and understand the properties of this filamentary structure using transmission electron microscopy.[13−16] However, it is not easy to observe the nanoscale structure and their 3D interconnection in conducting filaments directly.[17,18]

On the other hand, current noise analysis can be a powerful tool for probing the current distribution in a resistive medium. This method is indirect but simple, noninvasive, and can also provide statistical and microscopic insight into the charge transport phenomena. Current noise gives information about the origin of the current fluctuation in charge transport.[19,20] For example, noise analysis was used to figure out a trap distribution inside the channel material of field-effect transistors and at interfaces of light-emitting diodes.[21,22] Additionally, the magnitude of current noise is sensitive to the geometry of the current path; it has been applied to study

conducting filaments in resistive memory devices through scaling analysis.[19,23,24] Using such methods, we analyzed the noise scaling in perovskite RRAM based on $MAPbI_3$ thin film and characterized the structural features of the conducting filament formed in the material.

3.2. Experiments

3.2.1 Device fabrication

Organometal perovskite resistive memory devices were fabricated as previously described. Ti/Au bottom electrodes with line widths of 50 μm were deposited on the Si/SiO_2 substrate by electron beam evaporation through a shadow mask. First, 5 nm-thick Ti, which serves as an adhesive layer, was deposited, followed by 50 nm-thick Au. The substrate with the bottom electrodes was treated with UV-ozone (15 min) to enhance the film quality of the spin-coated $MAPbI_3$. MAI and $PbAc_2$ were dissolved by 3:1 in a molar ratio in N,N-dimethylformamide to form a 0.63 M solution. The solution was stirred at 60 °C for 30 min, then spin-coated onto the substrate in an N_2-filled glove box at a rate of 5000 rpm for 45 s. After the spin-coating, the samples were air-dried for 10 min and soft-baked at 100 °C for 5 min. Top electrodes (50 nm-thick Au) were deposited through a shadow mask of line-width 50 μm by electron beam evaporation.

3.2.2 Device characterization

The electrical measurements were performed using a semiconductor parameter analyzer (Keithley 4200 SCS) and a probe station system (JANIS ST-500) in a vacuum environment (≈10^{-5} Torr). The voltage sweep rate in I–V measurements was 0.54 V s^{-1}. The bottom electrode was grounded, and a voltage was applied to the top electrode.

For the noise measurement, a low-noise current amplifier (Ithaco 1211) was used for converting the current noise signal into an amplified voltage signal. The signal was measured in the frequency domain using a spectrum analyzer (Stanford Research SR760) and in the time domain using a ground-isolated 16-bit analog-digital converter (ADC). A 16-bit digital-analog converter (DAC) controlled by a LABVIEW was used to apply a voltage. A digital multimeter (Agilent 34401A) was used to measure the average current.

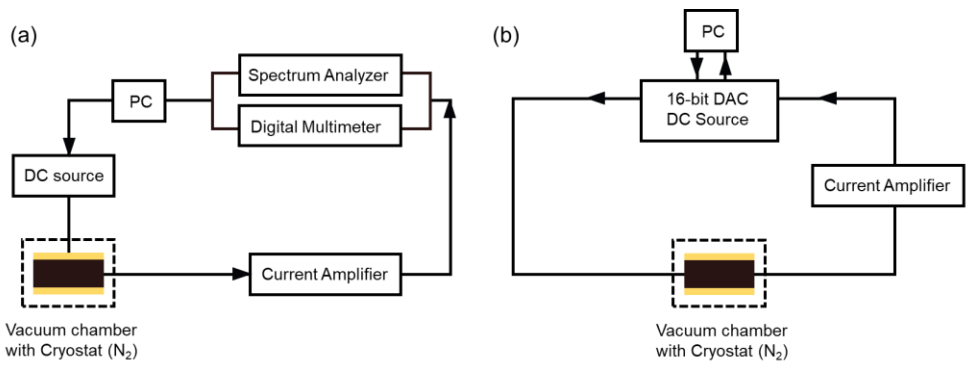

Figure 3.1 Experimental setup for (a) noise spectra measurement and (b) current time trace measurement.

3.2.3 Thermal simulation

A numerical simulation for heat dissipation was performed through the organometal perovskite device. Figure 3.2(a), shows the simulation setup for the $MAPbI_3$ device, which was a 3D cylindrical structure with a radius of 1 μm. The $MAPbI_3$ layer with a thickness of 200 nm was sandwiched by 50 nm-thick Au bottom and top electrodes on a 270 nm-thick SiO2 substrate. The top electrode was covered by a 400 nm-thick air layer. A cylindrical conducting filament with a radius of s nm was located at the center inside the $MAPbI_3$ layer. For simplicity, the fractal structure of the conducting filament was not considered in this simulation. With this setup, the heat equation

$$\rho C_p \frac{dT(\vec{r})}{dt} = k\nabla^2 T(\vec{r}) + q(\vec{r}) \qquad (3.1)$$

was numerically solved for calculating the temperature profile of the device using the finite element method with a mesh size of 2 nm. In the Equation (3.1), ρ, C_p, k, and $q(\vec{r})$ are the density, specific heat, thermal conductivity, and heat power, respectively. The parameters used for this simulation are listed in Table 3.1.

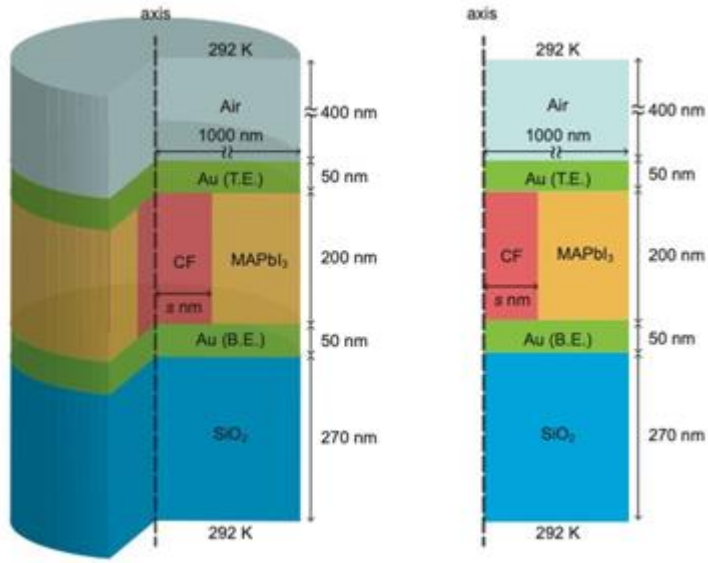

Figure 3.2 Simulation setup for the $MAPbI_3$ memory.

Table 3.1 Parameters k, C_p, and ρ for various materials used for the simulation.

	$MAPbI_3$	SiO_2	Au	Air	Ni	Nb:STO
k (W $m^{-1}K^{-1}$)	0.4	1.5	301	0.0243	91	12
C_p (J $kg^{-1}K^{-1}$)	311	730	129	1005	440	538
ρ (g cm^{-3})	4.16	2.65	19.3	0.001293	8.9	5.13

3.3. Results and discussion

3.3.1 Noise scaling in various resistance states

The perovskite memory devices showed different intermediate resistance states (IRSs) by controlling the compliance current (Figure 3.3(a)). In each resistance state, current noise was measured when applying a small voltage (0.1 V) where resistive switching would not occur. Figure 3.3(b) shows the current noise amplitude (S_I, spectral noise power density) as a function of frequency for four resistance states, indicating that low-frequency 1/f type noise characteristics were observed in the frequency range between 10 and 1500 Hz for each resistance state. As shown in Figure 3.3(b), the magnitude of S_I increases as the resistance value of the state increases.

Figure 3.3(c) shows the normalized current noise power spectral density (S_I/I^2; hereafter denoted as normalized current noise) measured at 998.4 Hz in each IRS. The scaling behavior was observed according to the power-law between the S_I/I^2 and resistance values. Such a scaling behavior can be attributed to the formation of percolation paths within the material.[24-26] According to the percolation theory, a resistive switching medium is a network consisting of conducting and insulating fractions. A percolation path between the two electrodes is formed when the conductive volume fraction (φ) increases and reaches a certain threshold (critical conductive volume fraction, φ_c). Here, the noise of the entire system is mainly determined by the smallest bottleneck region of the percolative path, where the electric field and current density are the most concentrated. The noise decreases as a power law as the number of current paths increases, decreasing the resistance of the

total network.[27,28] It means that the following relationship is satisfied between the total resistance (R) and normalized current noise.

$$\frac{S_I}{I^2} \propto R^{\gamma} \tag{3.2}$$

when $\varphi > \varphi_c$. Here, φ is conductive volume fraction and φ_c is critical conductive volume fraction. Note that the observed power law of the scaling behavior suggests that the resistive switching of our $MAPbI_3$ memory device is governed by the percolative conducting filament in the bulk rather than a homogeneous switching by interfacial effect.

The two scaling regimes depending on the resistance appeared: $\frac{S_I}{I^2} \propto R^{9.0}$ for $R<R_{co}$ and $\frac{S_I}{I^2} \propto R^{0.85}$ for $R>R_{co}$. Here, R_{co} is the resistance at which scaling exponent crossover occurred (marked as an arrow in Figure 3.3(c)) and was found to be about 400 Ω. Similar crossover behaviors with two scaling regimes were observed in the oxide-based unipolar resistive memory.[29,30] To investigate this scaling crossover, a model of a percolating cluster with fractal geometry was proposed.[31] The total resistance and normalized noise are closely related to the current distribution in the system; both quantities depend on the interconnection within the conducting network.[27,32] They can be expressed in terms of n_t, which stands for the number of current paths at distance t from the origin (top electrode in this study, schematically shown in Figure 3.3(d)). It is known that n_t satisfies the relationship: $n_t \propto t^{D_f-1}$ for a fractal structure.[33,34] Here, D_f is the fractal dimension of the filament structure. Fractal is a mathematical object that exhibits self-similarity, and a fractal dimension derived from the scaling relation of a structure is an indicator of the complexity. An object with a large fractal dimension has a

complex structure, and it densely fills the embedded space. The fractal dimension of the conducting filaments can be obtained using the scaling behavior between the normalized noise magnitudes and total resistance for each state. Another important parameter for explaining the scaling crossover is the lateral size of the bottleneck (s_0) where the current is most concentrated. From the fractal geometry, the following relationship can be used:

$$n_t \approx (s_0 + t)^{D_f - 1} \quad (3.3)$$

Scaling relationships for total resistance and normalized noise magnitude are divided into two regions according to the size of s_0, thus scaling exponent (γ) in equation (3.2) changes at a certain threshold of s_0 (see Figure 3.3(d)).[31,35]

$$\gamma = \frac{D_f}{D_f - 2} \text{ for } R < R_{co} \text{ and } \gamma = 1 \text{ for } R > R_{co} \quad (3.4)$$

The fractal dimension of conducting filaments in perovskite was best fitted to be about 2.25. This value is similar to (and slightly smaller than) that reported in a previous study for metal oxide thin film-based resistive memory ($D_f \approx 2.54$),[31] suggesting that a relatively simple conducting filament structure has been formed. A smaller fractal dimension of 2.25 might be related to the formation of conducting filaments around the grain boundaries, where the ion migration is frequent in organometal perovskite.[36]

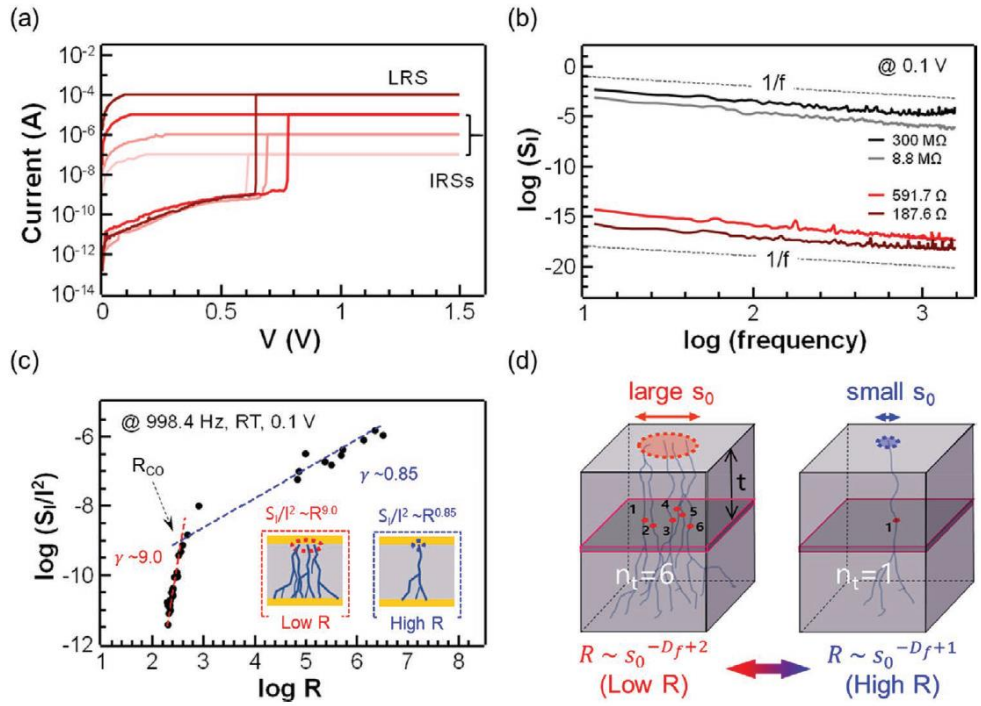

Figure 3.3 (a) I-V curves of a perovskite RRAM showing LRS and various IRSs. (b) Spectral noise power density versus frequency for four resistance states showing low-frequency 1/f noise characteristics. (c) Normalized current noise power spectral density for various resistance states showing a crossover behavior at about 400 Ω. (d) schematic of conducting filaments with fractal geometry. The number of current paths (n_t) is shown on the cross-section at a distance t from the top electrode. The lateral size of the bottleneck structure (s_0) is closely related to the scaling crossover behavior.

3.3.2 Temperature-dependent characteristics of conducting filaments

The ion migration responsible for the formation of conductive clusters in organometal perovskite is expected to occur more readily at higher temperatures.[37] Therefore, the structure of conducting filaments discussed above is expected to vary with temperature. Figure 3.4(a) shows the magnitude of normalized current noise at 998.4 Hz in each IRS measured at two temperatures (275 and 323 K). As shown in Figure 3.3(c) (measured at room temperature), the scaling behavior also showed the crossover at R_{co} of about 400 Ω at 275 and 323 K (Figure 3.4(a)). Compared with the results at room temperature (Figure 3.3(c)), the scaling exponents have similar values in $R > R_{co}$ and $R < R_{co}$ regions among the three temperatures, which also indicates a similar fractal dimension ($D_f \approx 2.25$). However, the scaling exponent tended to slightly increase as the temperature decreases. This is presumably because the magnitude of elementary fluctuations from the material constituting the conducting filaments increases as temperature decreases. Accordingly, the effect of normalized noise magnitude over total resistance increases to modify the scaling exponents. The most distinct difference in the noise scaling at high and low temperatures was the noise magnitude. The magnitude of the normalized noise at high temperature is similar to that of room temperature; however, four to five orders of magnitude are larger in the low-temperature case, suggesting that the current fluctuation of conducting filaments at low temperature is relatively large.

To further support the percolation-scaling behavior and related fractal structure of the conducting filaments, reset current, which is the maximum current value before the reset occurs, was plotted as a function of resistance (called “I-R scaling”) in Figure 3.4(b). Similarly, two scaling regimes were observed in the I-R scaling. The I-R scaling behavior can also be explained by the same percolation model with fractal geometry. According to the model proposed by Lee et al., the change in the scaling exponent across the crossover occurs based on the area of the bottleneck

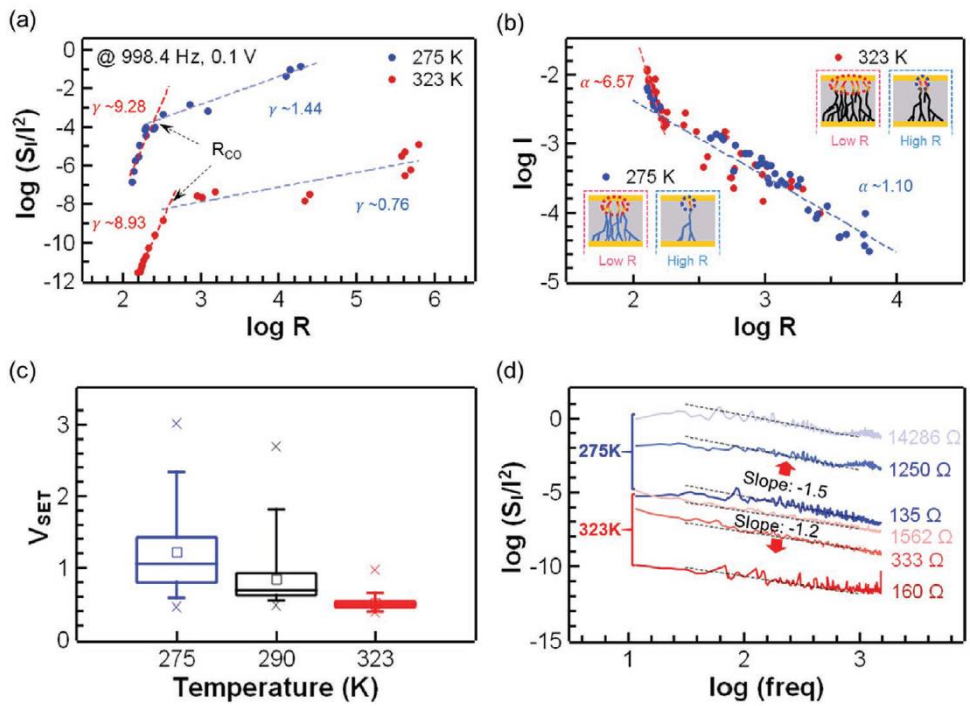

Figure 3.4 (a) Normalized current noise power spectral density versus the resistance of a perovskite resistive memory device at 275 and 323 K. (b) Reset current versus resistance at 275 and 323 K showing scaling crossover behavior. Insets show schematics of conducting filaments and the hottest bottleneck region (dotted circles in red) at each temperature. (c) Distribution of the set voltage during the 50 cycles of set/reset operation at 275, 290, and 323 K. (d) Normalized noise spectra in a frequency domain measured at 275 and 323 K.

region, where the current is the most concentrated among the conducting filaments (see inset of Figure 3.4(b)). During the reset process, the bottleneck area through which the largest current flows becomes the hottest region in the entire conducting network due to Joule heating. When the temperature of the bottleneck area exceeds the critical temperature, even if the remaining filament structure is maintained, the bottleneck region of the filament is ruptured, and the resistance state of the memory device is switched to HRS. The heat conduction and dissipation that occur during such a reset event can be simulated based on the heat equation using the finite element method. As a result, the minimum heat required to raise the temperature of the bottleneck region to the critical temperature exhibits a power-law relationship with the cross-sectional area of the bottleneck region. The scaling theory predicts that the exponent for reset current scaling (α) and resistance satisfies the following relationship.[31]

$$I_{Reset} = R^{-\alpha} \tag{3.5}$$

$$\alpha = \frac{D_f - \beta + 1}{2(D_f - 2)} \text{ for } (R < R_{co}) \text{ and } \alpha = \frac{D_f - \beta + 1}{2(D_f - 1)} \text{ for } (R > R_{co}) \tag{3.6}$$

From the simulation, the β value was calculated to be 0.33 for the $MAPbI_3$. The extracted scaling exponents were 6.57 and 1.10 in $R < R_{co}$ and $R > R_{co}$ regions, respectively. Accordingly, D_f value of the conducting filament was calculated to be about 2.2, which matches well with the fractal dimension estimated by the noise scaling, supporting the validity of the proposed fractal geometry model of the filamentary paths.

The temperature-dependent ion migration process is expected to be apparent from the memory operation characteristics, especially the set and reset characteristics of the perovskite memory devices. Figure 3.4(c) shows the distribution of the set

voltage during the 50 cycles of the set/reset operation at each temperature for the same device. The set process is the result of electric field-driven vacancy migration toward the conducting filament. Therefore, the set voltage decreases at a high temperature where ion migration is active, which is consistent with our experimental results in Figure 3.4(c). Additionally, the set voltage distribution becomes narrower as the temperature increases. Although the temperature dependence of the set voltage magnitude can be explained by the ion migration picture, predicting the temperature dependence of the set voltage distribution is nontrivial. As previously mentioned, conducting filaments formed are not completely dissociated during the reset process but are ruptured only in the bottleneck region where the current is the most concentrated. Then, the remaining filament structure affects the subsequent set processes since it concentrates electric field. Thus, it gives spatial confinement to filament growth. As more parts of the structure remain (i.e., the ruptured gap of the conducting filament becomes smaller), the subsequent set voltage distribution becomes narrower.[38,39] Previous studies using numerical simulations have reported a robust filamentary structure with relatively large lateral size leaves rather than a small gap during the rupture process.[6,9] Therefore, it can be inferred that in our experiments, a more robust filamentary structure with numerous current paths was formed at LRS of 323 K than that of 290 and 275 K.

Figure 3.4(d) shows a comparison of normalized noise spectra in a frequency domain of the same device measured at 275 and 323 K. There are differences in the results measured at different temperatures. The noise magnitude level was four to five orders of magnitude larger at 275 K than that of 323 K, even though they have similar resistance. It means that the current fluctuation was relatively larger in the

275 K case. The slope of 1/f type noise at high temperature fits well to about 1.2, but the slope at low temperature best fits at about 1.5. As reported previously, the slope of ≈1.5 is often related to current fluctuations induced by diffusion/migration processes.[40−43] Such current fluctuations can be directly probed in the time domain, which will be the focus of the latter part of this study. This $1/f^{1.5}$ noise with a larger magnitude suggests that the underlying process of noise at IRSs of 275 K is different compared to 323 K or room temperature cases. The measured temperature range was limited below 323K due to potential artifacts from the phase transition from tetragonal to cubic phase at ≈330 K.[44,45]

3.3.3 Current time trace measured at 275 K

In order to examine the correlation between the larger slope of the noise spectra for lower temperature (Figure 3.4(d)) and current fluctuations, we collected the current time trace data for various resistance states accessible in our perovskite memory devices. The time trace data were collected by applying a small bias (0.05 V). As shown in Figure 3.5(a), the current trace in the IRS states at low-temperature conditions (275 K) showed step-like fluctuations, which is a typical feature of random telegraph noise (RTN). The RTN features were observed for the IRSs with higher resistance values (bottom three panels of Figure 3.5(a)) whereas the lowest resistance states (top panel of Figure 3.5(a)) did not show any current fluctuations within the measured time range. Similar current fluctuations have previously been associated with processes such as charge trapping/ de-trapping at the defects close to the conducting filaments or current fluctuations induced by diffusion/migration of ions, which provided a mechanistic picture towards understanding resistive

switching mechanisms in various material-based memory systems.[26,42,43,46-48] Therefore, we proceeded with a detailed analysis of the observed current fluctuations in our perovskite memory devices for the different resistance states by visually representing the distribution of the current levels in the time trace as current histograms (Figure 3.5(b)). From the histograms collected from the time trace data over a period of 0.1 s, we can extract the discrete current levels among which the fluctuations occur by determining the major peaks. We can verify that the discrete current levels are distributed over about an order of magnitude in current for the IRSs (three bottom panels in Figure 3.5(b)), whereas the LRS shows a single major current peak (top panel in Figure 3.5(b)). This is also reflected in the time trace data in Figure 3.5(a) where the LRS (140 Ω state) shows almost no current fluctuations, which can be related to stable and numerous current paths (see top panel in Figure 3.5(c)).

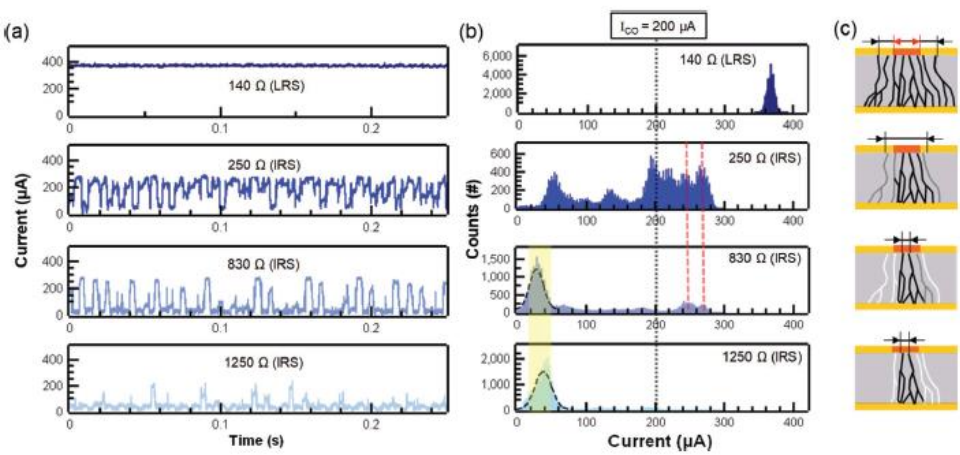

Figure 3.5 (a) Current time trace for various resistance states measured at 275 K and (b) corresponding current histogram for 0.1s. RTN is exhibited in IRSs. Common current level peaks near ≈245 and ≈270 μA are indicated with red dashed lines. Common current level peaks located in the range of ≈20 to ≈50 μA (yellow box) are Gaussian-fitted. (c) Schematic representation of fluctuations in conducting filaments at corresponding resistance states.

On the other hand, the large current fluctuations in the IRSs spanned over the cross-over current I_{co} of ≈200 μA (i.e., the current at R_{co}, see Figure 3.4(a)) where the bottleneck size of the conducting filaments is equal to the threshold bottleneck size s_{co} (= s_0 at R_{co}, see Figure 3.3(c),(d)).

Since each major peak in the current histogram corresponds to a possible configuration of conducting filaments, the existence of multiple major peaks in our current histogram (Figure 3.5(b)) suggests that the resistive switching in our perovskite memory devices involves multi-level transitions like in organic nanocomposite memory devices.[26,43] (Figure 3.6; A time lag plot is used to visualize the dynamic transition between the current state in Figure 3.6. The x-axis represents the current at a specific time t, and the y-axis represents the current at t + Δt. Therefore, the transition between each state is shown along the clockwise direction on the time lag plot as indicated by the red arrows. Δt was set to be 500 μs which is on a similar scale to the transition time. A time lag plot was drawn with the data of 0.1 s, and the corresponding current value histogram is shown at the bottom. The transition between each state can be tracked through off-diagonal points.) Furthermore, we can identify the underlying configurational relationships between the different IRSs by comparing the peak positions of these multi-current levels from the current histograms. We suggest that the formed percolative conducting paths in different resistance states are not completely random but have a common configuration to some degree. Specifically, we can observe common current level peaks near ≈ 245 and ≈ 270 μA (indicated with red dashed lines) for both the 250 and 830 Ω states (middle two panels in Figure 3.5(b)). Also, we can find common current levels in the range of ≈ 20 to ≈ 50 μA (indicated as a yellow box) for both

the 830 and 1250 Ω states (bottom two panels in Figure 3.5(b)). However, the relative stability differs depending on the resistance state, which can be related to the relative frequency of each current peak in the histogram, accordingly. The higher current level peaks are more frequent in the LRSs, whereas the lower current level peaks are more frequent in the HRSs (Figure 3.5(b)).

Now, we propose an overall picture for summarizing the different configurations of local conducting filaments and their relative stability based on our previous discussions. The number of conducting filament branches is represented as an indicator for the average resistance of the resistance state (Figure 3.5(c)); the larger the number of the conducting filament branches, the lower the average resistance. The conducting filament branches are expressed in different colors; black, gray, and white filaments indicate stable, less stable, and the least stable paths, respectively. The origin of the multiple current peaks in the current histogram observed for the IRSs (Figure 3.5(b)) is depicted as the current fluctuation induced by the formation and dissolution of unstable conducting filament branches. The sizes of the bottleneck (s_0) are expressed as black arrows with respect to the threshold bottleneck size (s_{co}) expressed as red arrows. The number of stable conducting filaments and the size of bottleneck regions decrease as the average resistance of the state increases (Figure 3.5(c) and also see Figure 3.4(d)). Furthermore, the physical origin of the current fluctuation in our perovskite memory devices is presumed to be due to the local change in the structure of conducting filaments induced by ion migration processes. This is consistent with the disappearance of the RTN at a high temperature (323 K) (see Figure 3.7), indicating a relatively small contribution of local unstable current paths toward the total current due to a more active ion migration at higher

temperatures. Accordingly, although this is beyond the scope of our study, the conducting filaments are expected to be more stable in the cubic phase (above 330K) than in the tetragonal phase (this work) due to a lower activation energy for ion migration.[49-51]

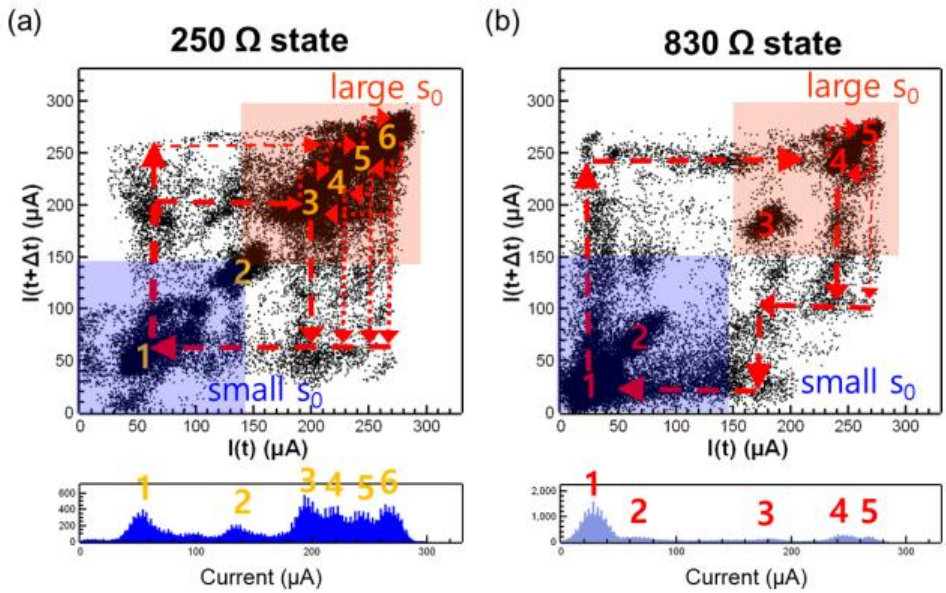

Figure 3.6 Time lag plot for (a) 250 Ω state (average) and (b) 830 Ω state (average) at 275 K. Corresponding current peak in the histogram is also denoted in the current histogram at the bottom.

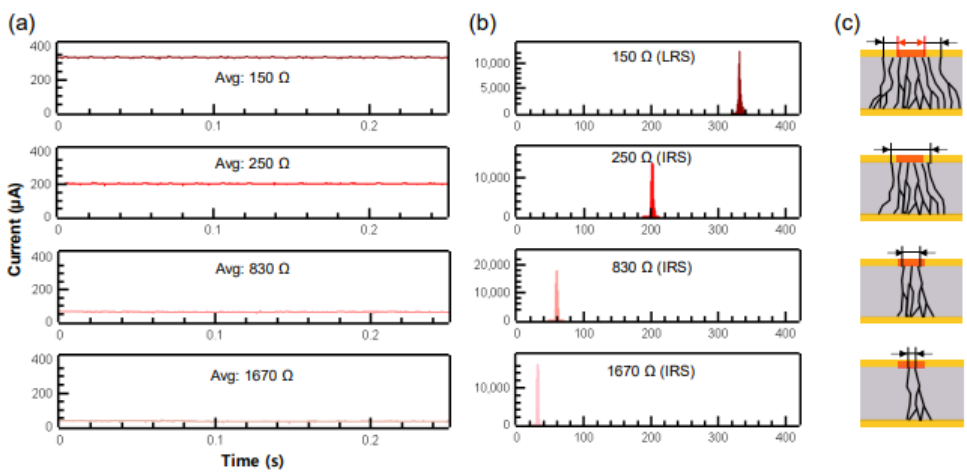

Figure 3.7 (a) Current time trace for various resistance states measured at 323 K and (b) corresponding current histogram for 0.1s. (c) Schematic representation of fluctuations in conducting filaments at corresponding resistance states. The figure in red indicates the threshold of the bottleneck area, s_{co}.

3.4. Conclusion

In this chapter, we investigated the electrical properties of resistive memory devices made with $MAPbI_3$ organometal perovskite. We adopted the current noise analysis as a simple and non-invasive tool to investigate the characteristics of conducting filaments in perovskite memory. By applying the percolation model with fractal geometry, we explained the scaling crossover behaviors in the normalized current noise and reset current. Additionally, by measuring the current noise at different temperatures, we observed the alteration of current levels in IRSs under low-temperature (275 K) conditions and a single peak distribution of current values at high temperature (323 K). We suggest that stable and robust filaments are formed under elevated-temperature conditions where ion migration is more active, resulting in stable multilevel operations with less noise. Our work demonstrates that the employed noise analysis can be a powerful tool for revealing the resistive switching mechanism in organometal halide perovskites, which can be expanded to other perovskite materials including all-inorganic perovskites for enhancing the operation stability in multi-state perovskite memory devices.

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Chapter 4. Summary

Devices based on organometal halide perovskite materials have recently shown exceptional memory properties like low-voltage operation and a high ON/OFF ratio, making them suitable for low power consumption memory devices. Despite these benefits, practical application of these perovskite-based devices still face challenges such as fabricating high-density arrays and detailed understanding of switching mechanism. In this thesis, I described the research results mainly focusing these two challenges in the field of perovskite resistive memory.

In the first part, high-performance resistive memory devices based on organometal halide ($MAPbI_3$) were demonstrated. Highly uniform and pinhole-free perovskite films were fabricated using a $PbAc_2$ precursor through a straightforward, single-step spin-coating technique. These perovskite-based memory devices displayed unipolar resistive switching characteristics within an Au/$MAPbI_3$/Au configuration, and achieved an impressive ON/OFF ratio, reaching as high as 10^8. This was coupled with excellent stability, verified through endurance tests (surpassing 1000 write cycles) and retention tests (exceeding 10,000 seconds). Furthermore, we showcased the dependability of the perovskite memory devices when fitted into an 8 x 8 cross-bar array structure, achieving an impressive yield of up to 94% and consistent memory cell characteristics. Additionally, we demonstrated a 1D-1R scheme with our perovskite memory devices that effectively curtailed cross-talk interference among neighboring cells linked via external diodes. These findings play a crucial role in the potential realization of cost-effective and high-capacity practical perovskite memory devices using a simple solution process.

In the second part, electrical characteristics of resistive memory devices fabricated with $MAPbI_3$ organometal perovskite was investigated. Current noise analysis, a non-invasive method, was utilized to examine the properties of conducting filaments within the perovskite memory. We used the percolation model paired with fractal geometry to elucidate the scaling crossover behavior in normalized current noise and reset current. Furthermore, we measured the current noise at varying temperatures, which revealed changes in current levels in IRSs under lower temperature conditions (275 K), as well as a single peak current value distribution under higher temperature conditions (323 K). Our findings suggest that when ion migration is more active under higher temperatures, and more consistent and robust filament structures are formed, leading to stable multilevel operations with reduced noise. This study underscores that noise analysis can serve as a useful tool for investigating the resistive switching mechanisms in organometal halide perovskites. The technique may also be extended to other materials, including all-inorganic perovskites, to boost the operational stability in multi-state perovskite memory devices.

국문초록

고성능 유무기 페로브스카이트 물질 기반 저항변화메모리 제작 및 전류 노이즈 분석 연구

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저항변화메모리 소자(Resistive Random Access Memory, RRAM)는 간단한 구조를 가져 저비용으로 제작이 가능한 동시에 비휘발성 및 빠른 스위칭 속도 등의 우수한 특성으로 많은 주목을 받고 있는 전자 소자이다. 다양한 재료 기반의 저항변화메모리가 연구되어 왔고, 그 중에서 최근 유무기 페로브스카이트 물질을 기반으로 한 메모리 소자는 낮은 동작 전압과 높은 ON/OFF 비율 등의 탁월한 특성을 나타내어 저전력 메모리 소자로서 큰 가능성을 보였다. 그러나 이러한 페로브스카이트 기반 메모리 소자의 장점에도 불구하고, 고품질 박막 제작의 어려움에 기인한 고밀도 어레이 제작 상의 난점과 소자 내 저항변화현상을 일으키는 전도성 필라멘트의 불규칙적인 구조로 인한 랜덤한 구동 특성이 실용화에 앞서 해결해야할 과제로 남아있다.

본 연구에서는 이러한 문제를 해결하기 위해 먼저 비할라이드계 납 전구체를 사용한 단일과정 용액공정을 통해 균일하고 pinhole이 없는 고품질 페로브스카이트 박막을 제작하였으며, 이를 바탕으로 고수율의 (최대 94%) 8 × 8 페로브스카이트 저항변화 메모리 어레이를 제작하였다. 제작한 단극성 소자는 낮은 동작 전압과 최대 10^8에 이르는 높은 ON/OFF 비율, 높은 구동횟수와 저장 시간 등의 우수한 동작 특성을 보였다. 또한 어레이를 구현하였을 때 누설 전류 문제를 해결할 수 있는

1 다이오드-1 저항 scheme을 (one diode-one resistor scheme) 본 연구에서 제작한 단극성 페로브스카이트 메모리 소자에 적용할 수 있음을 보였다. 해당 연구를 통해 저비용, 고밀도의 실용적인 페로브스카이트 메모리 소자의 가능성을 확인할 수 있었다.

다음으로는 소자의 다양한 중간 저항상태에서의 전류 노이즈 분석과 온도에 따른 전기적 특성 및 전류 노이즈의 변화를 분석하여 유무기 페로브스카이트 저항변화메모리 내에서 형성되는 불규칙한 모양의 나노구조물인 전도성 필라멘트의 기하학적 특성과 동적 특성을 연구하였다. 소자 내의 저항변화현상은 침투이론(percolation theory) 모델을 사용하여 이해되었고, 물질 내 전도성 필라멘트는 약 2.25의 소수점 차원을 지니는 프랙탈 구조를 가진 것으로 분석되었다. 또한 전도성 필라멘트 형성 및 해리의 원인인 이온 이동을 온도를 통해 조절함으로, 이온 이동이 원활한 고온 조건에서 더 강한 전도성 필라멘트 구조물이 형성되어 안정적인 multi-level 구동이 가능한 이점이 있음을 확인하였다. 전도성 필라멘트의 구조 및 동적 특성에 대한 심화된 이해를 바탕으로 추후 해당 구조의 제어 및 안정적인 구동 조건 파악이 가능할 것으로 예상하며, 결과적으로 유무기 페로브스카이트 물질 기반 저항변화메모리 소자 기술 발전에 기여할 것으로 기대한다.

주요어 : 유무기 페로브스카이트 물질, 이온 이동, 저항변화메모리, 전류 노이즈 분석, 침투이론(percolation theory), 전도성 필라멘트

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