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A Single-Chip 2.4GHz Direct-Conversion CMOS Transceiver with GFSK Modem for Bluetooth Application

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Abstract

This paper describes the radio transceiver for Bluetooth application operating at 2.4GHz ISM band. The transceiver uses low cost CMOS technology and integrates all components including PLL. Only RF matching elements and bypassing capacitors for power supply stability are required for complete transceiver. The proposed transceiver is implemented with 0.25um CMOS process and draws 60mA from 2.7V supply in receiver active mode.

Introduction

For recent years, wireless local area network are gaining more attention as a candidate for flexible connection among multi-media devices. Bluetooth is an up-coming wireless standard operating at 2.4GHz ISM band. The success of Bluetooth depends especially on its cost and thus Bluetooth has loose specification compared with other wireless standard such as IS-95 and GSM[1]. This requirement mandates the use of pure CMOS technology to implement Bluetooth IC, which is most popular IC technology. This paper describes full CMOS radio transceiver with integrated GFSK modem for Bluetooth application. The proposed radio transceiver uses direct conversion architecture for various purposes, which will be explained later.

System Architecture

Figure 1 shows the block diagram of transceiver. All functional blocks from LNA to ADC in receiver block and DAC to Pre-Amp in transmitter block are included in the transceiver. The transceiver includes not only a PLL block which is shared between receiver and transmitter but also GFSK modem. Only matching elements for LNA and bypass capacitors to suppress supply noise is needed as external components for complete transceiver. Direct conversion architecture has important merits that it is easy to integrate because of its simple architecture and has no image problem[2-3]. But there are significant disadvantages of dc-offset problem, strict requirement for PLL in the high frequency and VCO pulling problem. Thus, quadrature down-converter and up-converter using I/Q 6-phase mixer is adopted in the transceiver to eliminate dc-offset problems and strict requirement for PLL in direct conversion[4]. The PLL, which is shared between receiver and transmitter, is composed of 12-phase VCO, prescaler, phase frequency detector, loop filter, and generates 12-phase 800MHz LO signals.

Circuit Description

In the proposed receiver, the dc-offset can be drastically reduced due to quardrature down-converter using I/Q 6-phase mixers and the remaining DC offset in the receiver can be eliminated by the DC offset cancellation scheme shown in Figure 2. By the *dc_set* signal from the modem, the amount of DC offset generated by the circuit is sampled in the capacitor, and DC offset is compensated in the VGA. During the normal operation mode, *dc_set* signal is disabled, and the receiver can operate without DC offset problem. In the transmitter, if there are DC-offset in the inputs of up-converter and phase error in the LO signal, carrier leakage is generated.

In the proposed transmitter, the carrier leakage due to DC offset at the inputs of up-converter is eliminated by DC offset cancellation block and that due to phase error in the LO signal can be suppressed by the pre-amp scheme shown in Figure 3. Because the carrier leakage generated by phase error appears in the RF_OUT as common-mode signal, differential-to-single pre-amp suppresses the carrier leakage. And the following pre-amp stage which drives the 50Ω load can be single-ended scheme, and this eliminates the need of balun at pre-amp output.

Experimental Results

The transceiver is fabricated by 0.25um CMOS process. Figure 4 shows the chip microphotograph. The total area of transceiver is 4.0mm x 4.5mm. Figure 5 shows the measured result of VCO phase noise. The phase noise of the closed loop VCO at 816.9MHz center frequency is −100dBc/Hz at 500kHz offset when all the receiver blocks are operating. Figure 6(a) shows the Lissajous's waveform and Figure 6(b) shows phase trajectory waveform at ADC output in the receiver, when '1010' pattern is applied to DAC input in the transmitter. Phase alternation according to '1010' data pattern is shown in magnified view. And phase trajectory in the Figure 6(b) continuously increases because there is frequency offset between transmitter and receiver.

Table I shows the summary of the chip characteristics.

Conclusion

In this paper we presented a single chip 2.4GHz direct-conversion full CMOS transceiver for Bluetooth. A quardrature down/up converter using I/Q 6-phase mixer and DC offset cancellation scheme in the transceiver are adopted to eliminate problems in conventional direct conversion architecture. Overall noise figure and dynamic range of the receiver are 10dB and 60dB respectively, and maximum power and ACPR of transmitter are 0dBm and 50dB at 2MHz offset.

References

[1] James P. K. Gilb, "Bluetooth Radio Architectures", RFIC Symp., pp.3-6, June 2000

[2] Aarno Parssinen *et al.*, "A Wide-Band Direct Conversion Receiver for WCDMA Applications," ISSCC, pp.220-221, Feb. 1999.

[3] A. Rofougaran, *et al.*, "A Single-chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS-Part I & II," IEEE JSSC, vol.33, no. 4, pp.515-547, April 1998.

[4] Kyeongho Lee et al., "A Single-Chip 2.4GHz Direct-Conversion CMOS Receiver for Wireless Local Loop using One-third Frequency Local Oscillator," SOVC, pp.42-45, June 2000

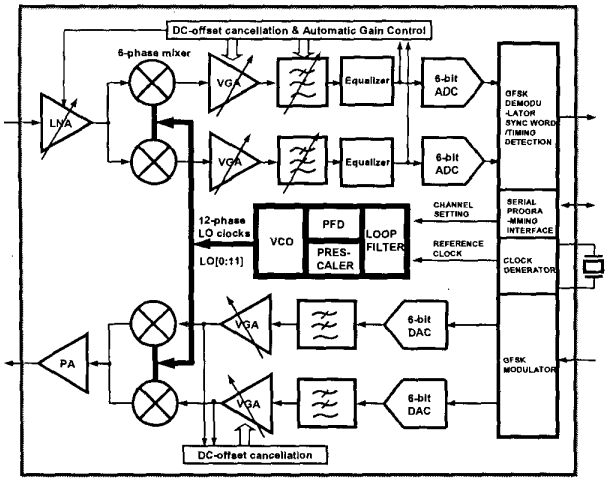

Figure 1. Transceiver architecture

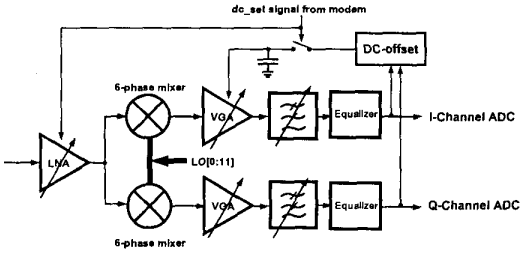

Figure 2. DC-offset cancellation scheme in receiver

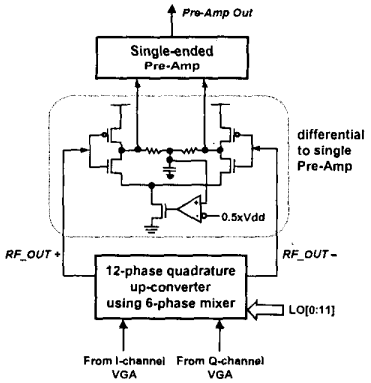

Figure 3. Pre-amp

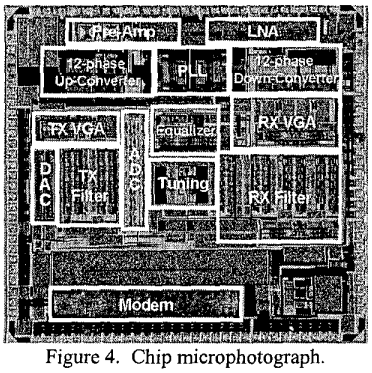

Figure 4. Chip microphotograph.

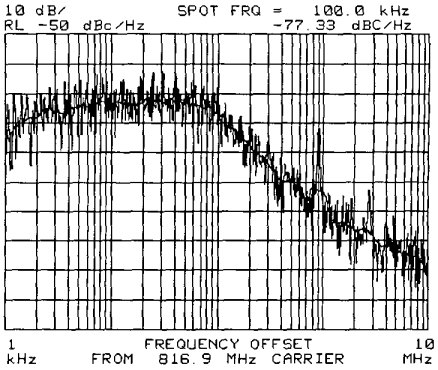

Figure 5. Phase noise of VCO

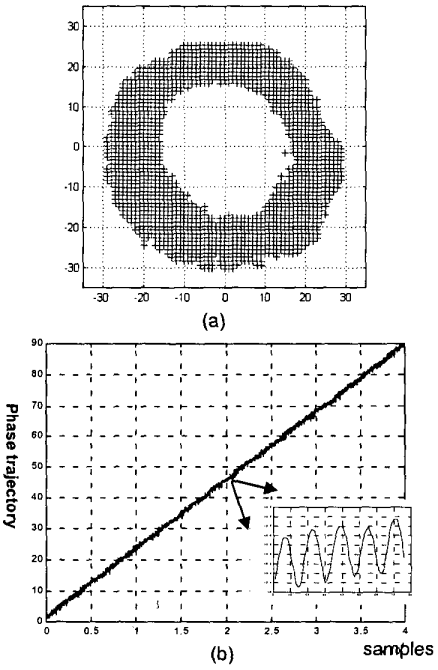

Figure 6. (a) Lissajous's waveform at ADC output
(b) phase trajectory at ADC output

Table I. Summary of chip characteristics

Over all	
Frequency Range	2402 ~ 2480 MHz
Die Area	4.0mm x 4.5mm
Technology	0.25um CMOS
Transmitter	
Maximum Output Power	0 dBm
ACPR	50 dB @ 2MHz offset
Power Dissipation	150 mW @ 2.7V
Receiver	
Receiver Sensitivity	-83 dBm
Dynamic Range	60 dB
Overall NF	10 dB
Power Dissipation	162mW @ 2.7V
Phase Locked Loop	
LO Phase Noise	-100dBc/Hz@500kHz offset