

Figure 2. Proposed BBPFD and retimer.

MDCO, and dithers the output clock signal to improve the resolution of the output frequency. The MDCO is a differential 3-stage ring oscillator with a digitally controlled resistor [1]. The division ratio of the fractional divider ranges from 3 to 4 in steps of $1/3$. The input phase error due to the alternating integer modulus of the feedback divider drops as the step size is reduced.

B. Bang-Bang Phase-Frequency Detector

A linear TDC is used for phase detection in many ADPLL circuits. A conventional TDC consists of many cascaded inverters and flip-flops. Its time resolution and detection range are respectively determined by an inverter delay and inverter chain length. A high-resolution TDC yields better performance, but only at the expense of an excessive number of inverters, which use up a lot of power and area [2]. Furthermore, an additional aid to frequency-locking will be required due to the limited frequency detection capability of a TDC, which makes the circuit more complicated. Conversely, a BBPFD, which is an effectively nonlinear PD, has an intuitive structure. This makes it easy to design, but it has a limit cycle problem, and the quantization effect of the DCO increases the output jitter. It is difficult to resolve these nonlinearities in an analog design, since that will require dealing with analog quantities. However, in an ADPLL, all communication between building blocks are digital and its core behavior is described in a hardware description language (HDL). As a result, nonlinear effects can easily be controlled, and furthermore the RTL code can be reused without major modifications.

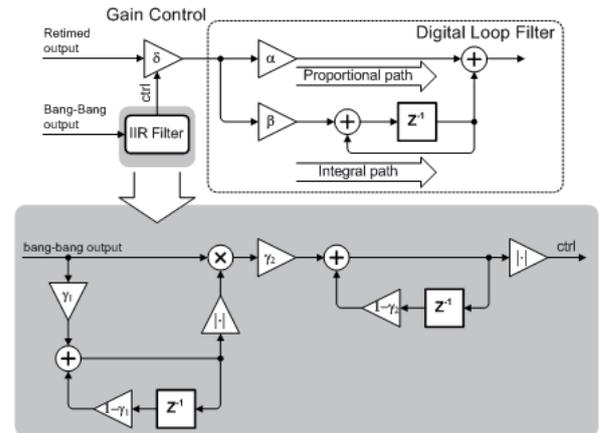


Figure 3. Digital loop filter and adaptive loop gain controller.

We use the BBPFD shown in Fig. 2 to simplify the design and implementation of our ADPLL. Unlike previous BBPFD [3], ours generates two sets of results; one is a typical bang-bang output to control the adaptive gain, and the other is a retimed output which is fed into the DLF. Because bang-bang signals are maintained for a relatively long period until the polarity of input phase error changes, the quantization error is integrated over a considerable time. To shorten the integration period and reduce the output jitter, our BBPFD produces retimed output.

The proposed retimer and the resulting timing waveform are shown in Fig. 2. The retimed signal is generated by sampling outputs from a conventional PFD using the FCLK signal. Although a conventional DFF is used as a simple retimer, the phase error information can be lost when the duration of the up or down pulse is shorter than the period of the FCLK signal, which causes a dead zone in the transfer characteristic. As a result, the output phase of the ADPLL wanders over the dead zone and the output jitter increases. The proposed retimer, consisting of an edge detector and a sampling flip-flop, eliminates the dead zone. The edge detector extends the width of the up or down pulse until the next FCLK edge arrives, and the sampling flip-flop converts this extended output to a one-cycle-long pulse, so that no signal transitions are missed. The bang-bang output signals inhibit the retimer from generating opposite direction retimed pulses as shown at the bottom of Fig. 2.

C. Adaptive Loop Gain Controller

Although the BBPFD is easy to implement, its nonlinear operation and relatively large gain can cause significant output jitter. Lowering the loop bandwidth is a typical solution to getting better jitter performance, but that increases the lock time considerably. Instead, in our design, the ALGC dynamically adjusts the loop bandwidth to reduce the output jitter without seriously affecting the lock time. Fig. 3 shows the structure of the DLF and ALGC. The DLF is separated into proportional and integral paths, and its overall gain is controlled by the ALGC using a 2-stage IIR filter. This filter has a cascaded structure and each stage uses a leaky integrator. The filter effectively averages the bang-bang output from the

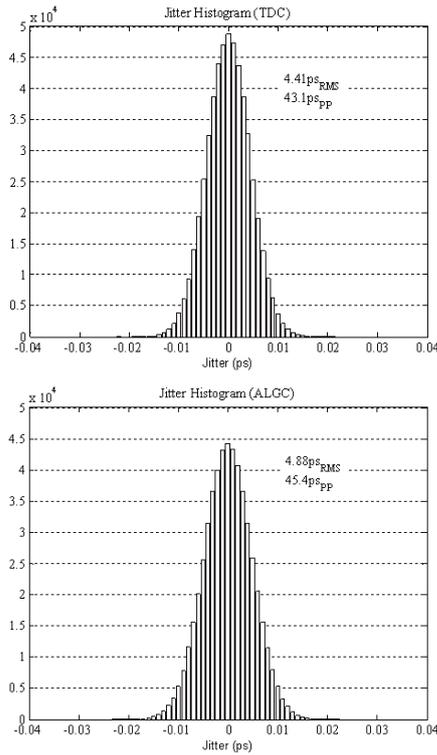


Figure 4. Jitter comparison (TDC vs. ALGC).

BBPFD. When the input phase error is large, the absolute value of the output of the IIR filter is one. As the input phase error drops, the bang-bang output alternates more quickly and the absolute value of the output of the IIR filter approaches $\gamma_1\gamma_2/4$ ($0 < \gamma_1, \gamma_2 \ll 1$), and the loop gain is adjusted accordingly. In effect, the ALGC makes the loop gain proportional to the average phase error, and as a result the loop bandwidth changes dynamically. If the ADPLL is in its locked state, the average phase error will be smaller, the loop bandwidth is reduced, and the output jitter drops. However, when the ADPLL is in its frequency tracking state, the loop bandwidth will be larger and the lock time will not be affected.

We verified the effect of the ALGC by means of an HDL simulation. The core RTL code used in this simulation is synthesizable except the DCO and TDC models. The DCO behavioral model includes $3.2\text{ps}_{\text{RMS}}$ random timing jitter and 80fs_{RMS} random timing wander [4]. Fig. 4 compares the output jitter for two cases, and the ADPLL with a linear TDC has slightly better performance. However, the ALGC is fully synthesizable, which makes it more appropriate for an all-digital design than a fully custom linear TDC.

D. Fractional Divider

A typical fractional-N frequency synthesizer adopts a dual-modulus divider. This generates a fraction of the input frequency by alternating the modulus between two consecutive integers. However, fractional-N PLL suffers from fractional spurs caused by the modulation of the feedback divider. In our architecture, a fractional divider is used to reduce the large phase error resulting from the changes of

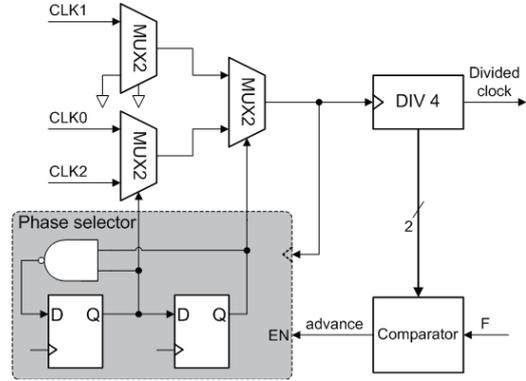


Figure 5. Proposed fractional divider.

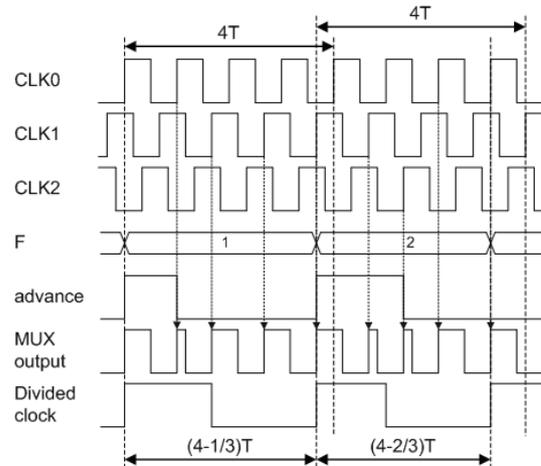


Figure 6. Timing diagram of the fractional divider.

division ratio. The fractional divider consists of a phase multiplexer (MUX), a divider, a phase selector, and a comparator, as shown in Fig. 5. This structure can be described by a fully synthesizable HDL code. The differential output of the MDCO is multiplexed and fed into the divider. The comparator produces an advance signal by comparing the fractional part (F) with the internal count of the divider. The phase selector is activated while the advance signal is high, and the MUX control inputs are changed accordingly. Then the leading phase is selected by the MUX. Repeating this process achieves fractional division. The number of phases determines the control step of the fractional divider. If the fractional divider uses M -phase clock and F times of phase advance take place every N input cycles ($N \geq F$), its division ratio is $(N-F/M)$. Fig. 6 shows an operation example of the fractional divider using 3-phase clock. During the first operation, N and F are 4 and 1 respectively, and the resulting division ratio is $(4-1/3)$. Next, F is changed to 2, so the result is $(4-2/3)$. In this design, the division ratio ranges from 3 to 4 in steps of $1/3$.

E. Digitally Controlled Oscillator

The MDCO consists of a differential 3-stage ring oscillator and a digitally controlled resistor (DCR) [1]. It generates the

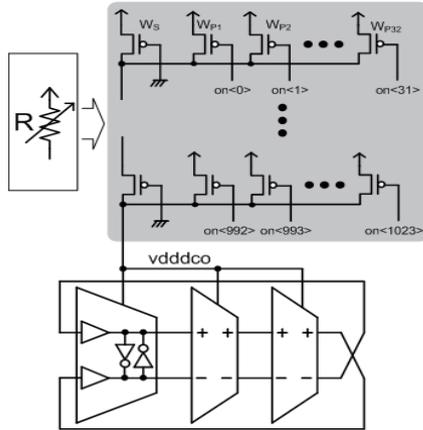


Figure 7. Digitally controlled oscillator.

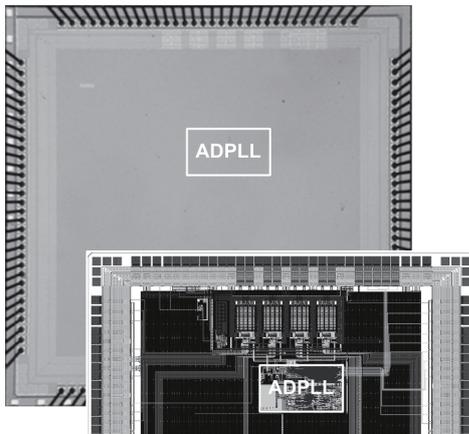


Figure 8. Chip layout and microphotograph.

6-phase clock required to operate the fractional divider. Fig. 7 shows a block diagram of the MDCO. The digitally controllable PMOS transistors are arranged in a 32×32 matrix, and segmented thermometer control is used to obtain linearity with a small hardware.

III. EXPERIMENTAL RESULTS

The layout and microphotograph of the prototype chip, implemented in a $0.13\mu\text{m}$ CMOS process, are shown in Fig. 8. The area of circuits, excluding the ESD protection structure, is 1.1mm^2 and the ADPLL core occupies only 0.19mm^2 . The ADPLL consumes 13.7mW from a 1.2V supply. Fig. 9 shows a measured clock jitter at 1.35GHz . The RMS and peak-to-peak jitter resulting from operation of the ALGC and fractional divider are 4.17ps and 32ps respectively. A comparison of the performance of this circuit with other ADPLLs is shown in Table I.

IV. CONCLUSION

The all-digital phase-locked loop is appreciated for its scalability, flexibility and robustness. We present an ADPLL which incorporates an adaptive gain controller and a fractional

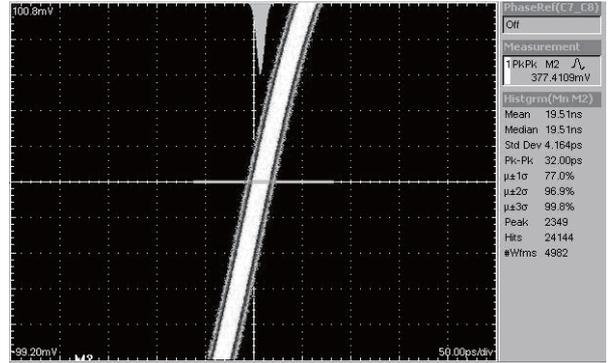


Figure 9. Measured clock jitter.

TABLE I. PERFORMANCE COMPARISON

		<i>This work</i>	[3]	[5]	[6]
Process		$0.13\mu\text{m}$	65nm	$0.18\mu\text{m}$	65nm
Output frequency (GHz)		0.3–1.4	0.09–1.2	0.03–1.04	3
Power supply (V)		1.2	0.5	1.8	1.2
Jitter (ps)	RMS	4.17 (@1.35GHz)	3 (@1GHz)	13.8 (@950MHz)	0.4 ^a (@3GHz)
	P-to-P	32 (@1.35GHz)	N/A	86.7 (@950MHz)	N/A
Area (mm^2)		0.19	0.03	0.32	0.4
Power dissipation (mW)		13.7 (@1.35GHz)	1.65 (@1GHz)	15.7 (@1.04GHz)	10 (@3GHz)

a. Estimated from the phase noise characteristic.

divider. Simulation and measurement show how the ALGC is able to suppress the nonlinear effects of the bang-bang design. The fractional divider, which has $1/3$ division step, reduces the occurrence of fractional spurs. The acceptable performance of this prototype chip demonstrates the practical applicability of the ADPLL.

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