An InGaAs/InP p-i-n-JFET OEIC with a Wing-Shaped p^+-InP Layer

Ki-Sung Park, Kwang-Ryong Oh, Jeong-Soo Kim, Yong-Tag Lee, Sung-June Kim, and Young-Se Kwon

Abstract—**A new receiver OEIC structure with an InGaAs p-i-n photodiode, InGaAs self-aligned junction FET's and a bias resistor has been fabricated on a semi-insulating InP substrate. The fabrication processes are highly compatible between the photodiode and the JFET, and reduction in FET gate length is achieved using anisotropic selective etching and a two-step OMVPE growth schedule.**

The 80 μm diameter p-i-n detector exhibits a leakage current of 2 nA and a capacitance of about 0.35 pF at -5 V bias voltage. Extrinsic transconductance and a gate-source capacitance of the JFET are typically 45 mS/mm and 4.0 pF/mm at 0V, respectively. The maximum voltage gain of the pre-amplifier is 12.5 and the bandwidth of the p-i-n amplifier OEIC is expected to be about 1.2 GHz.

Introduction

THERE have been many research efforts on monolithic optoelectronic integrated circuits (OEIC's) which are projected to have the advantages of high performance, high reliability, and low cost compared with hybrid integrated circuits. Among these, the monolithically integrated photoreceiver that includes a photodiode and a preamplifier has drawn the most attention since high-speed and low-noise operation can be achieved by reducing front-end capacitance. Such receiver OEIC's have been fabricated in GaAs and InGaAs/InP material systems. Short wavelength (0.8 ~ 0.9 μm) GaAs OEIC's have shown a bandwidth of more than 5 GHz [1] and an integration scale of more than 2000 devices [2] based on the well-developed MESFET technology. However, the performance of the long wavelength (1.3 ~ 1.6 μm) receiver OEIC's using the InGaAs/InP system still falls short of hybrids, and the integration scale is small, due to the incompatibility of structure and processes between transistor and photodetector and the inferior characteristics of the preamplifier resulting from the immature InP-based electronic device technology. Hence, various integration structures for the InGaAs/InP system have been attempted, and various kinds of transistors have been integrated with photodetectors, including MISFET's [3] and JFET's [4]. Recently MESFET's [5] or HEMT's [6] using large-energy-gap materials such as GaAs or InAlAs have been applied to receiver OEIC's for high performance.

In this letter, we demonstrate a new InGaAs p-i-n-JFET OEIC structure. Conventional receiver OEIC's have seperate epilayers for photodetector and transistor, and fabrication processes are also done seperately. In these structures, a thick photoabsorption layer on the transistor region is not necessary and has to be removed. However, in our structure all the epilayers and all the fabrication steps are necessary for both p-i-n and JFET, as well as an undoped-InGaAs photoabsorption layer which is located in the FET region and utilized to achieve reduction in gate length and formation of a self-aligned structure.

Structure and Fabrication

The cross-sectional schematic diagram and processing steps of the proposed receiver OEIC are illustrated in Fig. 1. The p-i-n photodiode is constructed with a p^+-InP layer, an n^--InGaAs absorption layer, an n^--InP etch-stop layer, and an n-InGaAs layer. The diameter of photo-detective region is 80 μm for coupling with multimode fiber. The self-aligned InGaAs JFET consists of a wing-shaped p^+-InP layer and an n-InGaAs channel layer. The gate length and the width of JFET are 2 and 150 μm, respectively. This receiver OEIC is fabricated using two-step OMVPE growth.

The fabrication process starts with the first OMVPE growth of an undoped-InGaAs layer with 1.5 μm thickness and about 1×10^{15} cm^{-3} carrier concentration, an undoped-InP layer with 0.1 μm thickness, and an n-InGaAs layer with 0.3 μm thickness and 1×10^{17} cm^{-3} carrier concentration on semi-insulating InP substrate. The undoped-InGaAs layer and InP etch-stop layer are anisotropically and selectively etched to reveal a (111) In plane. The etched areas form the gate regions in which the pn junctions of FET's are to be formed and the isolation regions in which the devices are not located. The gate length L_G is obtained in this process as predicted by the following equation through controling the undoped-InGaAs layer thickness t and the channel opening L_M.

L_G is given as

$$L_G = L_M - 2t/\tan\theta$$

where θ is the crystallographic etched angle and is about 55°. Hence, a shorter gate than defined by photolithography can be achieved. The pn junction for both p-i-n and JFET is formed by the second OMVPE growth of 0.5 μm thick p^+-InP layer with 1×10^{18} cm^{-3} carrier concentration, where the growth pressure and the growth temperature are 76

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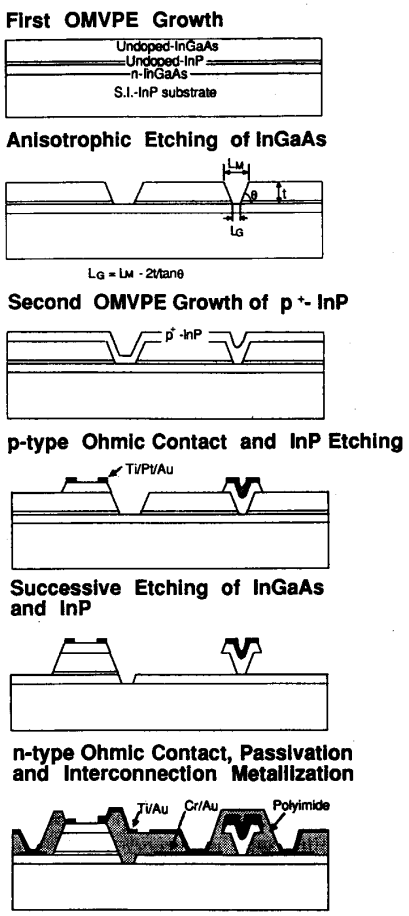

Fig. 1. Schematic cross-sectional views of receiver OEIC in fabrication steps. InGaAs p-i-n photodiode and self-aligned JFET are integrated on a S.I.-InP substrate.

torr and 600°C, respectively. The smooth regrowth profile can be obtained in this condition [7]. Ti(200 A)/Pt(400 A)/Au(2000 A) are deposited by liftoff and annealed at 412°C for 30 s for p-type ohmic contacts. The InP, InGaAs and InP layers are successively etched with masks of p-type metal for the JFET and photoresist for the p-i-n photodiode, to form a wing-shaped self-aligned JFET structure. The etching solutions are $1HCl + 8H_3PO_4$ for InP and $5H_3PO_4 + 1H_2O_2$ for InGaAs, respectively. Remaining processes are a self-aligned Cr(200 A)/Au(2000 A) deposition and annealing for n-type ohmic contacts, a 1.0 μm thick polyimide process for planarization and passivation, and finally Ti(200 A)/Au(2500 A) deposition for interconnection and bonding pads.

A photomicrograph and circuit diagram of a fabricated receiver OEIC chip are shown in Fig. 2. The receiver chip has a size of a 600 × 500 μm^2 and contains four elements: one p-i-n photodiode, one bias resistor made of n-InGaAs channel layer, and two JFET's.

Device Characteristics and Discussions

A typical integrated p-i-n photodiode with 80 μm diameter exhibited a dark current of 2 nA and a junction capacitance of

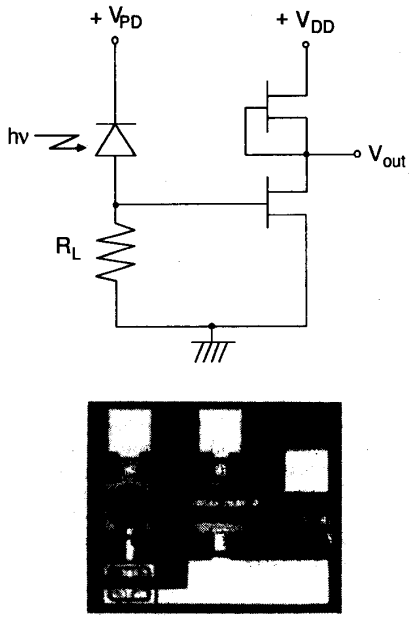

Fig. 2. Circuit diagram and photomicrograph of fabricated receiver OEIC chip. The chip has a size of 500 × 600 μm^2 and contains 1 p-i-n PD, 1 bias resistor, and 2 JFET's.

0.35 pF at −5 V bias voltage. The responsivity was about 0.47 A/W for 1.3 μm wavelength without AR coating, corresponding to quantum efficiency of 45%. The capacitance of a small-area photodiode with 20 μm diameter was measured to be less than 75 fF at the same bias voltage, which means that the parasitic capacitance of the photodiode is very small.

The I–V characteristic and g_m curves of the integrated JFET with 2 μm gate length are shown in Fig. 3 (a) and (b). This shows a good pinchoff. The threshold voltage is about −2.6 V, with a typical extrinsic transconductance of 45 mS/mm at a drain-source voltage of 3 V and gate voltage of 0 V. The drain conductance exhibited 10 mS/mm at these bias voltages. The gate-to-source capacitance (C_{gs}) at 0 V gate bias was about 4.0 pF/mm. Therefore the cut-off frequency of this integrated JFET is calculated to be about 1.8 GHz. It is believed that the kinks observed in $I_D - V_{DS}$ and $I_D - V_{GS}$ curves in Fig. 3 originate from the gate length modulation effect due to the expansion of the depletion region to the residual n^--InGaAs layer under the p^+-InP wings.

The integrated bias resistor was 100 Ω for high-speed operation. A larger external resistor is needed to improve the sensitivity of the OEIC.

The preamplifier voltage gain was measured when the drain bias voltage (V_{DD}) was varied from 4 to 15 V. The maximum gain was approximately 12.5 at V_{DD} = 15 V. Fig. 4 shows the dc voltage transfer curve and corresponding voltage gain of the preamplifier. The RF characteristic of the p-i-n amplifier circuit was simulated using SPICE and the measured device parameters. The −3 dB bandwidth was about 1.2 GHz. This value agrees with a bandwidth of 1.3 GHz calculated from the input RC time constant. In an

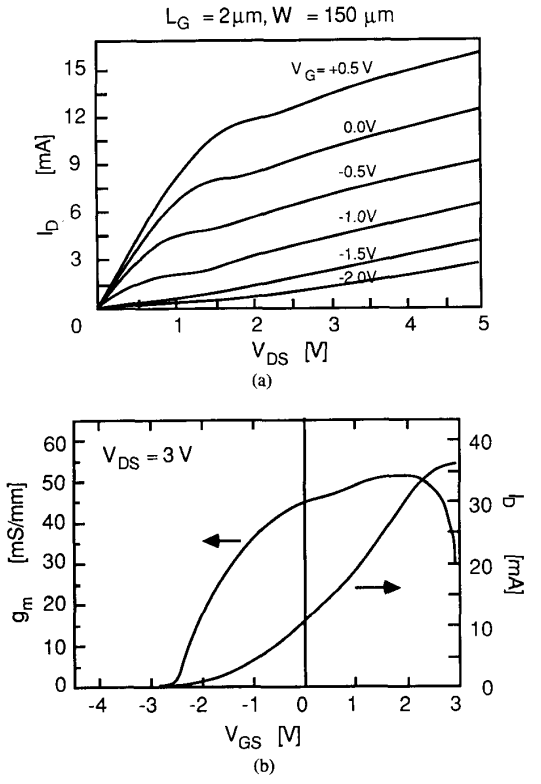

Fig. 3. (a) I–V characteristic and (b) g_m curves of the integrated InGaAs JFET.

optical receiver circuit, the bandwidth and the bit rate are related in the following equation:

$$f_{3dB} = I_2 B$$

where I_2 is a Personick integral constant, that is 0.56 for the NRZ code [8]. This indicates that this receiver OEIC is capable of detecting a 2 Gb/s NRZ signal.

Conclusion

A monolithic receiver OEIC comprised of an InGaAs/InP p-i-n photodiode, self-aligned JFET's, and a bias resistor was fabricated using an anisotropic etching and two-step OMVPE growth process. The fabrication process is highly compatible between the photodiode and the self-aligned JFET, and further reduction in gate length can be achieved. A voltage gain of the preamplifier was measured as 12.5 at a bias voltage of 15 V, and the simulated bandwidth of the p-i-n amplifier was about 1.2 GHz.

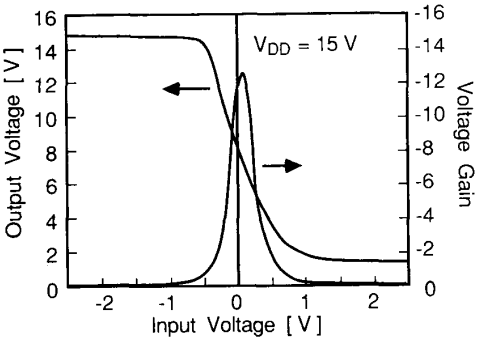

Fig. 4. DC voltage transfer curve and voltage gain of the preamplifier.

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