Monolithic Integration of InGaAs p-i-n Photodetector with Fully Ion-Implanted InP JFET Amplifier

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Abstract—**A monolithically integrated p-i-n FET amplifier has been fabricated using ion-implanted indium phosphide (InP) JFET's. The vertically integrated material structure consists of a vapor phase epitaxy (VPE) grown InGaAs photoabsorption layer and a metal organic chemical vapor deposition (MOCVD) grown Fe-doped semi-insulating layer. A Zn diffusion was performed to complete the p-i-n photodiode. High-performance fully implanted InP JFET's were used to form the integrated amplifier with a symmetrical design to remove the dc offset. With a receiver sensitivity of −36.4 dBm measured at 200-Mbit/s NRZ for 10^{-9} BER, it is easily the most sensitive monolithic p-i-n FET preamp yet reported in this frequency range. The p-i-n amplifier has a dynamic range of 15 dB.**

I. Introduction

THE OPTICAL communication systems developed in this decade use both short- (0.8–0.9 μm) and long- (1.3–1.6 μm) wavelength regions, but due to the lower attenuation transmission windows in silica fibers in the long-wavelength region, the GaInAsP alloy materials grown lattice matched to indium phosphide (InP) have drawn much attention. The InP-based optoelectronics integrated circuits (OEIC's), therefore, have become an important component for communication systems to be built in the future. In order to build such integrated circuits, one requires a good electronics technology. Unlike Si and GaAs, however, InP does not have a well-established FET technology. Due to gate–semiconductor interfacial problems, the metal–insulator–semiconductor (MIS) and metal–semiconductor (MES) FET's do not appear to be practical in InP. InP JFET's have demonstrated good performance and may be the device of choice until the problems with other options can be solved.

Several groups have reported long-wavelength integrated p-i-n FET photodetector devices using InP/InGaAs FET's operating at various bit rates [1]–[5], but the sensitivities were relatively low. In [6], an alternative approach has been taken to fabricate MESFET's on a GaAs layer grown lattice mismatched to an InP substrate. Among the reported p-i-n FET devices, only [5] and [6] employ integration of a complete amplifier, including a level-shifting buffer stage. We report in this paper the fabrication and performance of an integrated p-i-n FET amplifier with high sensitivity. The amplifier is made using high-performance fully ion-implanted InP JFET's and, therefore, only materials grown lattice matched to an InP substrate are used.

Manuscript received May 5, 1988; revised June 24, 1988.

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IEEE Log Number 8823106.

II. Device Structure and Fabrication

Fig. 1 shows schematically the structure of the integrated p-i-n JFET device. The material was grown on an n^+-InP substrate in two steps. The first growth was done by chloride vapor phase epitaxy (VPE) [7]. Following the growth of an undoped InP buffer, a 3.5-μm-thick $In_{0.53}Ga_{0.47}As$ layer with an electron concentration less than 1×10^{15} cm^{-3} was grown and capped by another layer of undoped InP. The second growth was done by atmospheric pressure metal organic chemical vapor deposition (MOCVD) [8], [9] and resulted in a 3-μm-thick Fe doped semi-insulating InP layer with a typical resistivity higher than 10^7 Ω·cm.

The wafer with grown epilayers was then subjected to a series of ion implantations to form the JFET. The details of the ion implantation and activation are similar to those reported earlier [10]. The channel was formed by implanting ^{29}Si, and it was followed by the source–drain implant to form highly doped regions. Subsequently, As/Be coimplant was used to form the p^+ gate region. All implants were selective, non-self-aligned using SiN_x and photoresist as an implantation mask. The implanted wafer was then activated in a rapid thermal annealer (RTA) using a dielectric capping layer.

Following deposition of a SiN_x passivation layer, the Zn diffusion to form the p-i-n diode was performed using an evaporated film of zinc phosphide patterned by a lift-off. Diffusion was performed in an RTA, and the resulting p-n junction was located near the InP–InGaAs interface. Further details of the p-i-n fabrication will be reported elsewhere. The rest of the device processing consists of three metallization steps: for the gates, sources and drains, and interconnects.

III. Device Performance

Previously, we reported [10], [11] on the fabrication of fully ion-implanted InP JFET's on semi-insulating (SI) substrates. We have fabricated JFET's with similar performance

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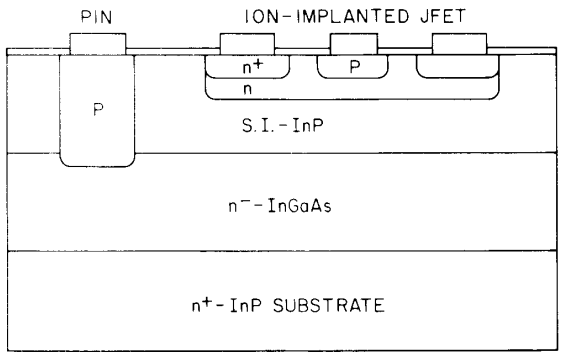

Fig. 1. Cross-sectional view of the integrated p-i-n JFET device.

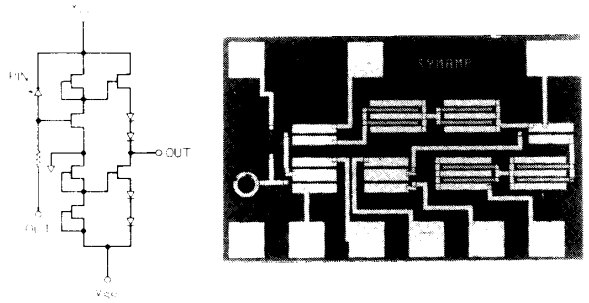

Fig. 2. p-i-n JFET symmetrical amplifier circuit diagram and microphotograph of a fabricated chip.

on the MOCVD-grown SI layer. From the JFET's used in this work, a transconductance g_m of 100 mS/mm was measured at $V_{gs} = 0$. With C_{gs} of 1.8 pF/mm, a 3-dB cutoff frequency $g_m/(2\pi C_{gs})$ of 9 GHz is calculated.

Fig. 2 shows the circuit diagram of the integrated p-i-n JFET amplifier and the microphotograph of a fabricated chip. The p-i-n's are fabricated into a 75-μm-diameter circle. Within the circle, the p-contact metal is defined as a 10-μm-wide ring. The p-i-n has a dark current of 10 nA and a capacitance of 0.25 pF at -5 V. A 30-kΩ resistor was also fabricated using the channel implant to serve as a feedback resistor for the amplifier.

The amplifier consists of a symmetrical design which, as described in [11], results in negligible dc output offset. All FET's are 100 μm width, and the level-shifting diodes are implemented with p-n junctions 10×200 μm^2 in area. At $V_{in} = 0$, an open-loop voltage gain of 5.5 was measured from the amplifier.

The fabricated p-i-n amplifier circuit has been mounted on a ceramic carrier for optical sensitivity measurements. Bond-wire connections were made from the chip to the ceramic carrier for power supply and ground connections and also to form the transimpedance configuration. Only two power-supply voltages ($V_{dd} = -V_{ss} = 5$ V) were used.

A bandwidth of 40 MHz was measured from the p-i-n amplifier in transimpedance configuration. The bandwidth was limited by the RC delay at the amplifier input where R is the effective resistance (feedback resistance/(open-loop gain + 1)) and C is the total capacitance (p-i-n, FET, and stray capacitance). The output was equalized to obtain a 100-MHz bandwidth.

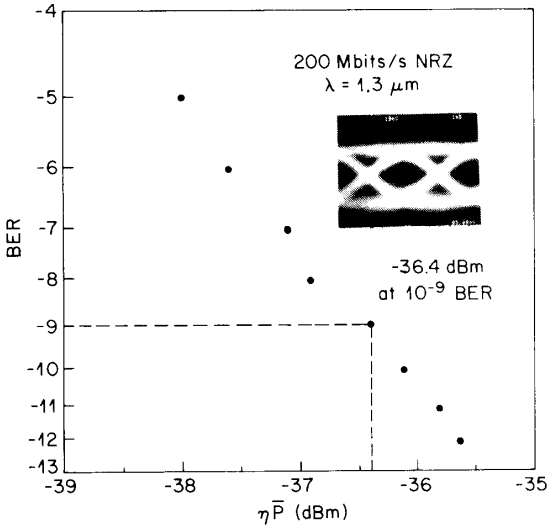

Fig. 3. Detector sensitivities measured for several BER's. The insert shows an eye diagram taken at 200-Mbit/s NRZ for 10^{-9} BER.

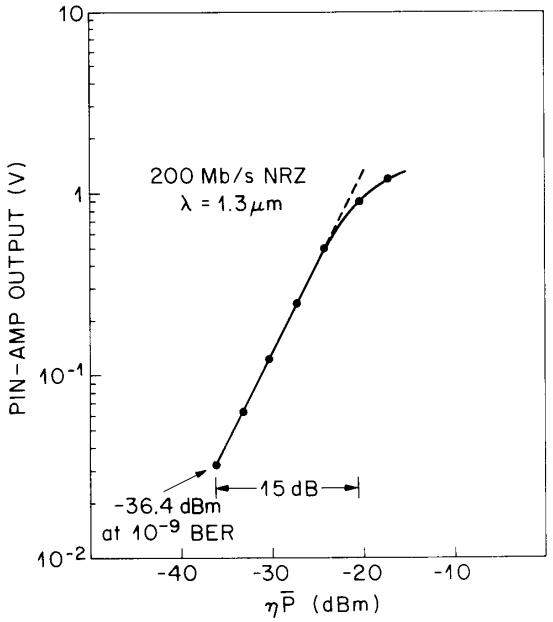

Fig. 4. Peak-to-peak amplifier output voltage versus detected optical power. A dynamic range of 15 dB is measured.

The sensitivity measurement was performed at 200-Mbit/s NRZ format. Detected power was measured for several bit-error rates (BER's) (Fig. 3). For 10^{-9} BER, the sensitivity was -36.4 dBm. We believe that this is the best sensitivity reported to date from a p-i-n FET device designed for 1.3–1.55-μm wavelength at this bit rate. The insert in Fig. 3 shows an eye diagram taken at 200 Mbit/s for 10^{-9} BER.

Fig. 4 shows the peak-to-peak amplifier output voltage as a

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function of detected optical power. For every 3-dB increment of the optical power, the amplifier output doubles until it saturates. From the minimum detected power of -36.4 dBm (at 10^{-9} BER) to the saturated knee point, a dynamic range of 15 dB is measured.

IV. Conclusion

An InGaAs p-i-n has been monolithically integrated with a full amplifier circuit using InP JFET's to achieve high sensitivity. The fully implanted FET's were fabricated on an MOCVD-grown semi-insulating InP layer together with a diffused p-i-n. A receiver sensitivity of -36.4 dBm was measured at 200-Mbit/s NRZ for 10^{-9} BER. This sensitivity can be improved by reducing the gate length of the FET's and capacitance of the p-i-n. The absence of a dc offset at the output of the symmetrical amplifier facilitates the cascading of multiple stages, which will further enhance the sensitivity.

Acknowledgment

The authors would like to acknowledge the help from Y. Ota, J. M. Geary, R. E. Frahm, and K. J. O'Brien in device packaging and in dielectric deposition.

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