Integrated Amplifiers Using Fully Ion-Implanted InP JFET's with High Transconductance

SUNG J. KIM, MEMBER, IEEE, G. GUTH, AND G. P. VELLA-COLEIRO, MEMBER, IEEE

Abstract—**Monolithically integrated amplifiers have been fabricated on indium phosphide (InP) using fully ion-implanted JFET's. The FET's have a gate length of 1.5 μm and a maximum transconductance of 110 mS/mm, the highest ever reported for ion-implanted InP JFET's. The amplifiers utilized both a conventional direct-coupled design as well as a new symmetrical design. The conventional direct-coupled amplifier shows a maximum gain of 8 (18 dB) while the symmetrical amplifier design exhibits the same gain without dc offset regardless of the FET threshold voltage and the power supply voltage used.**

I. INTRODUCTION

DUE TO their optical properties in the long-wavelength region (1.3–1.55 μm), the materials grown lattice matched to indium phosphide (InP) substrate are of considerable interest for lightwave applications. InP also shows good electronic properties such as high peak electron velocity and large intervalley energy gap [1] suitable for high-speed devices [2], and high breakdown fields [3] and high thermal conductivity [4] for high-power applications. MESFET's are not feasible on InP due to low Schottky barriers, and MISFET's suffer from drain current drift caused by large surface state density at the insulator–semiconductor interface, making JFET's the best compromise at this time.

Among the integrated circuits built on InP substrate, there have been only two reports on the fabrication of amplifiers. J. Cheng *et al.* [5] showed an amplifier using InGaAs JFET's grown on InP substrate with a dc gain of 4. An InP amplifier was also demonstrated by C. Cheng *et al.* [6] using MISFET's with a dc gain of 5. In this paper we report for the first time on the fabrication and performance of amplifier circuits using high-performance fully implanted InP JFET's.

II. ION-IMPLANTED JFET'S

Fig. 1 shows schematically the structure of the JFET used. The FET's were fabricated on commercially available semi-insulating substrates. The details of the processing steps are the same as those previously described [7] except for the channel implant. The energy and dose of the Si channel implant has been changed from 240 keV, 4×10^{12} cm^{-2} to 220 keV, 10^{13} cm^{-2}. This change caused the peak channel doping concentration to increase from 6×10^{16} to 1.5×10^{17} cm^{-3}.

The transconductance of a JFET is proportional to the saturated electron velocity (for short gate length) and inversely proportional to the depletion region width at a given gate–source voltage (see, for example, [8]). A higher channel doping decreases the depletion region width, resulting in increased transconductance. However, it also causes the electron mobility to decrease due to increased impurity scattering of carriers (we have measured an electron Hall mobility of 1300 cm^2/V·s compared to 2000 cm^2/V·s measured in previous work), and the saturated electron velocity is expected to decrease as well. Therefore the transconductance should increase with higher channel doping, but the increase will be limited by the reduced saturated electron velocity.

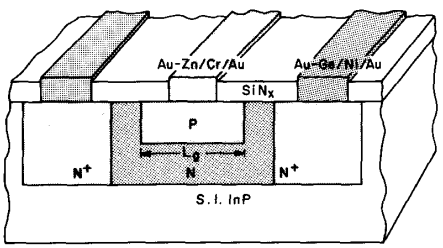

Fig. 1. Cross-sectional view of the ion-implanted JFET structure.

The other change in the new JFET is in the decrease in gate length (from 2 to 1.5 μm). This not only increases the transconductance further, but also reduces the gate capacitance per unit gate length for a given channel doping. Due to the factor of 2.5 increase in channel doping, however, the gate capacitance increased from 1.2 to 1.5 pF/mm. The reverse bias junction leakage is 15 nA at 5 V for a junction of 1.5×100 μm^2.

Fig. 2(a) shows the FET I–V characteristics for a 1.5-μm gate FET where the gate voltage used ranges from 1 to -3 V with 0.5-V step. Fig. 2(b) shows the transconductance as a function of gate–source voltage. Transconductance as high as 110 mS/mm is measured when $V_{gs} = 0.7$ V (with a gate leakage of 1 μA), and when $V_{gs} = 0$ the transconductance is 90 mS/mm. These transconductance values are believed to be the highest ever reported for fully implanted InP JFET's.

As was discussed before, the improvement in transconductance from the previous work is due to the increase in channel doping (peak concentration of 6×10^{16} to 1.5×10^{17} cm^{-3}) and a shorter gate length (2 to 1.5 μm). As previously explained, the gate capacitance C_{gs} has been slightly increased to 1.5 pF/mm at zero gate bias due to higher channel doping which makes the calculated cutoff frequency of the JFET (g_m/

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The authors are with AT&T Bell Laboratories, Murray Hill, NJ 07974.
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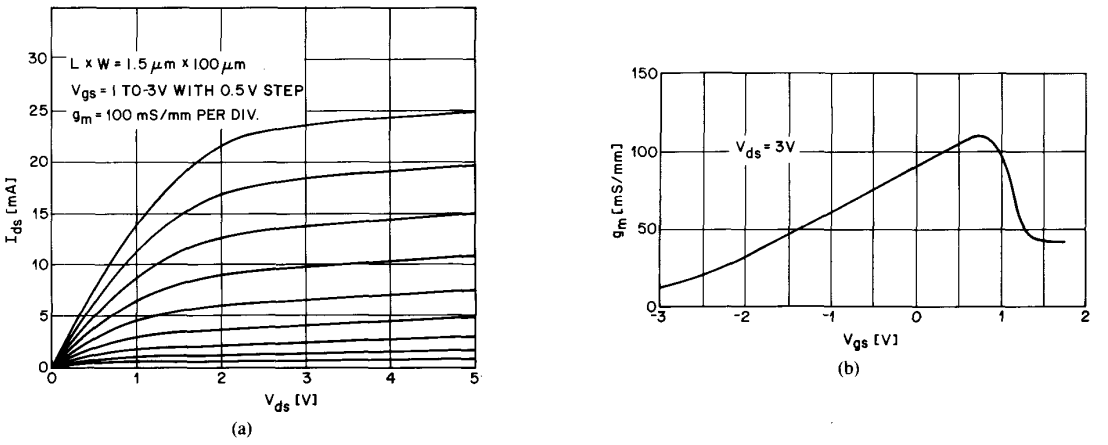

Fig. 2. (a) Typical FET I–V characteristics taken from a JFET with a gate 1.5 μm long and 100 μm wide. (b) Transconductance plotted as a function of gate–source voltage.

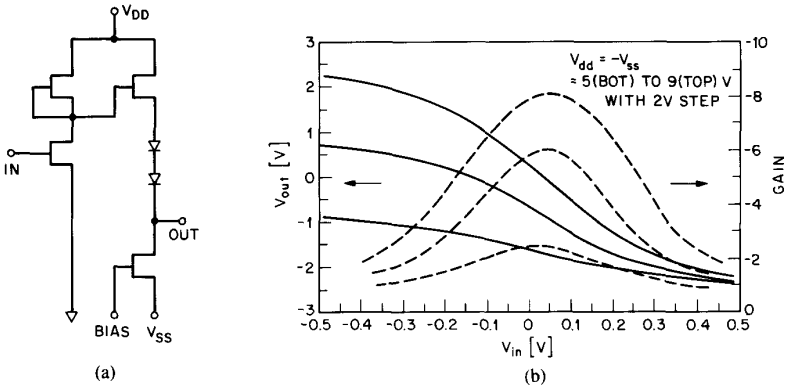

Fig. 3. Conventional direct-coupled amplifier (a) circuit diagram and (b) amplifier dc characteristics (V_{out} (solid lines) and gain (dotted lines) versus V_{in}).

$2\pi C_{gs}$) to be 9.5 GHz. The output conductance g_d is 4.5 mS/mm.

The saturation current is 150 mA/mm and the JFET pinches off at -3.2 V. Work is in progress to further reduce the saturation current and the threshold voltage while maintaining a high transconductance.

III. Integrated Amplifiers

Fig. 3(a) shows the circuit diagram of the direct-coupled amplifier that was fabricated. The amplifier design is the same as in [9] consisting of a gain stage and a level-shifting buffer stage. All JFET's are 100 μm wide except for the current source in the level-shifting stage where the JFET is larger (150 μm wide) and its gate terminal is brought out to provide the ability to null the output dc offset. Two JFET's with gates of 10×200 μm^2 are used as diodes (source and drain connected together) for level shifting, each providing a turn-on voltage of about 1.1 V with a series resistance of 20 Ω. The gain of the inverter, G_{inv}, is

$$G_{inv} = g_m/(g_d + g_d)$$
$$= 1/2\ (90\ \text{m})/(4.5\ \text{m}) = 10.$$

The total gain of the amplifier is reduced by the source-follower buffer stage of which the gain can be calculated to be approximately 0.9. The expected total gain, therefore, is about 9.

The measured dc transfer characteristic and the calculated gain of the amplifier is shown in Fig. 3(b) for several power supply voltages ($V_{dd} = -V_{ss}$). The gain increases for higher supply voltage to a maximum value of 8. This agrees well with the expected gain shown above. The bias terminal (gate of the current source) was left at the same potential as V_{ss} for all cases.

One can note in the transfer curves in Fig. 3(b), however, that a dc offset results as the power supply voltage changes. The same is true when the transistor characteristics, especially the threshold voltage, change for a fixed power supply voltage. This dc offset voltage can be removed by either adjusting the power supply voltages (V_{ss} and V_{dd}), or by adjusting the bias to the gate of the current source FET which, in turn, changes the bias current for the level-shifter stage.

For most applications requiring dc coupling, neither of these alternatives is acceptable. In the new symmetrical amplifier design shown in Fig. 4(a), the output dc offset is

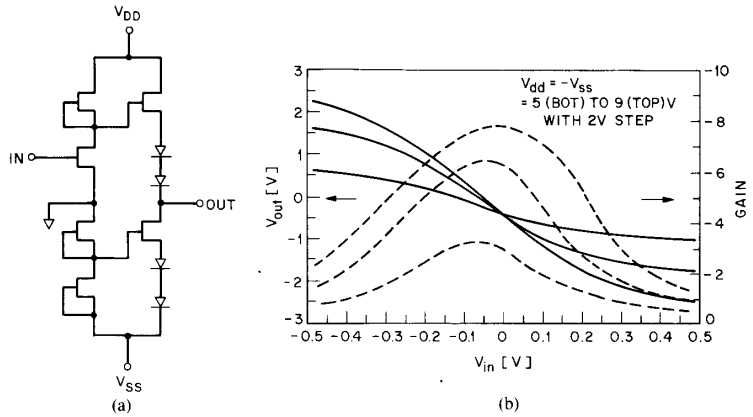

Fig. 4. New symmetrical amplifier (a) circuit diagram and (b) amplifier dc characteristics (V_{out} (solid lines) and gain (dotted lines) versus V_{in}).

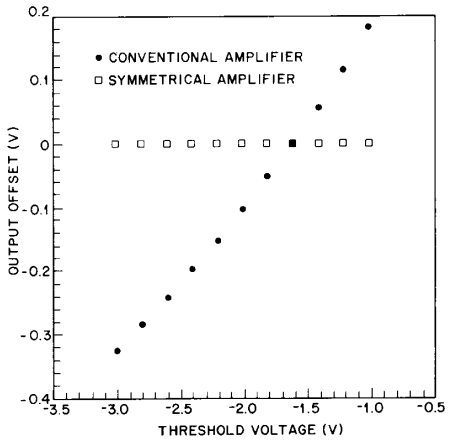

Fig. 5. Computer simulated output offset versus JFET threshold voltage for conventional and symmetrical amplifiers.

zero by design. The circuit is symmetrical with respect to V_{dd} and V_{ss}, hence for a zero dc input the output voltage is zero for any supply voltage as long as $V_{dd} = -V_{ss}$. The circuit's ability to produce zero dc offset regardless of other circuit parameters is demonstrated in the amplifier transfer curves in Fig. 4(b). Notice that the curves cross near $V_{in} = V_{out} = 0$ instead of merging at the lowest end of the output voltage as in the conventional amplifier (Fig. 3(b)). The gain versus V_{in} plots of the symmetrical amplifier, which are similar to the ones for the conventional amplifier, are also shown in Fig. 4(b).

The symmetrical amplifier is also insensitive to variations in the FET threshold voltage. In the ADVICE[1] simulations shown in Fig. 5, the threshold voltage was varied from -3 to -1 V and the output offset remained zero, whereas the output of the conventional amplifier varied from -0.33 to 0.18 V for the same variation.

The results reported above were obtained using a wafer probing station which has limited high-frequency capability. The amplifiers are presently being packaged for high-speed testing and the results will be reported elsewhere.

[1] ADVICE is a circuit simulator developed by AT&T Bell Laboratories based on the University of California, Berkeley's simulator SPICE.

IV. Conclusion

We have developed fully implanted InP JFET's with improved characteristics, and using them, fabricated high-performance amplifiers. The 1.5-μm gate FET's showed a maximum transconductance of 110 mS/mm and the amplifiers showed a dc gain of 8. The new symmetrical amplifier design is shown to be effective in removing dc offset without trimming of bias voltages.

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