# A Low-Power High-Speed Ion-Implanted JFET for InP-Based Monolithic Optoelectronic IC's

SUNG J. KIM, MEMBER, IEEE, K. W. WANG, G. P. VELLA-COLEIRO, MEMBER, IEEE, J. W. LUTZE, Y. OTA, AND G. GUTH

*Abstract*—**We describe a high-performance fully ion-implanted planar InP junction FET fabricated by a shallow (4000-Å) n-channel implant, an $n^+$ source-drain implant to reduce FET series resistance, and a p-gate implant to form a shallow (2000-Å) abrupt p-n junction, followed by a rapid thermal activation. From FET's with gates 2 μm long, a transconductance of 50 mS/mm and an output impedance of 400 Ω·mm are measured at zero gate bias with a gate capacitance of 1.2 pF/mm. The FET has a threshold voltage of −2.4 V, and a saturated drain current of 60 mA/mm at $V_{gs}$ = 0 V with negligible drift.**

## I. INTRODUCTION

THE MONOLITHIC integration of optoelectronic devices is a field of growing importance and interest as it allows enhanced performance at a reduced cost for the components that are now used in hybrid form. In spite of the immaturity of the material compared to GaAs and Si, the InP-based optoelectronic integrated circuits (OEIC's) are of interest due to the material's ability to generate and sense light in the long-wavelength region (1.3–1.55 μm) where the loss and dispersion of silica fibers are minimum at the present time [1].

Heavily developed technologies for the fabrication of field effect transistors (FET's) exist both in Si (metal oxide semiconductor FET (MOSFET)) and in GaAs (metal semiconductor FET (MESFET)). In contrast, a well-established FET technology in InP does not exist at present. The MESFET is not practical in InP due to low barrier height and, therefore, high gate-leakage current. The metal insulator semiconductor FET (MISFET) on the InP substrate suffers from a high density of surface states, which causes drift in drain current and degradation of transconductance, requiring further study.

The junction FET (JFET), which has none of the above problems, has been demonstrated in both the InGaAs and the InP. Using grown InGaAs layers as the channel, JFET's with high transconductances (110 mS/mm in [2], 210 mS/mm in [3], and very recently 553 mS/mm in [4]) have been fabricated. In [2] and [3], the p-n junctions were grown by MBE and MOCVD, respectively, but in [4], the junction was made by Zn diffusion in the LPE grown channel layer.

The InP JFET's, on the other hand, have been made using channel layers formed by ion implantation of Si directly into the semi-insulating InP. The junctions have been formed by selective Zn diffusion [5] or by Be ion implantation [6]–[8]. The fully ion-implanted JFET is attractive for making planar devices with high throughput. Planar devices have the advantages of simpler processing, easier passivation, and the ability to lay out transistors independent of crystal orientation. However, the fully ion-implanted JFET devices reported [6]–[8] had very high pinchoff voltages (10–12 V) and therefore high drain saturation currents ($I_{dss}$ = 360 to 600 mA/mm), which makes them unsuitable for low-power high-speed applications such as monolithic optoelectronic IC's, where avoidance of thermal interaction of electronic and optical components is crucial. The design and fabrication of a fully planar fully ion-implanted JFET with low saturation current and high transconductance is the subject of this paper.

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The authors are with AT&T Bell Laboratories, Murray Hill, NJ 07974.
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## II. DEVICE DESIGN CONSIDERATIONS

A cross section of the device is shown in Fig. 1. Three important features of the device should be noted. First, the p-n junction is shallow (2000 Å) and abrupt formed by a co-implantation of As and Be, which prevents the indiffusion of Be during activation [9]. Boos *et al.* reported in [6] and [7] a graded junction that resulted by Be indiffusion. Compared to the graded junction, an abrupt junction can deplete more channel for a given gate-bias change, yielding higher transconductance. Formation of the abrupt junction also enhances the control of the junction depth within a shallow channel, essential in making a low-threshold low-power device. Another feature of the device is the shallow channel (4000 Å). This not only gives a low current capability of the device, but also higher transconductance ($g_m$) given by the following relationship [10]:

$$g_m \alpha \left(\frac{N}{aL}\right)^{1/3}$$

where $N$ is the channel doping, $a$ is the channel thickness, and $L$ is the channel length.

Thirdly, $n^-$ source and drain implant is done to reduce the FET series resistance and thus to minimize the degradation of $g_m$ from its intrinsic value. A gate–source spacing of 0.5 μm was used to allow for the lateral diffusion of the dopants.

## III. DEVICE PROCESSING

The FET's were fabricated by the sequential selective implantation of Si and As/Be into (100) Fe-doped LEC semi-insulating substrates. The substrates were first etched with a 10:1:1 $H_2SO_4$:$H_2O_2$:$H_2O$ solution for 5 min to remove the polishing damage. Three selective implants were done in the order of channel, $n^+$, and gate implants. The implant mask

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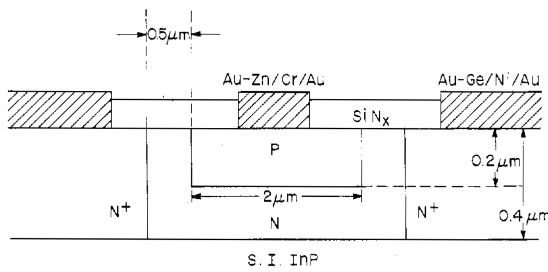


Fig. 1. Cross-sectional view of the ion-implanted JFET structure.

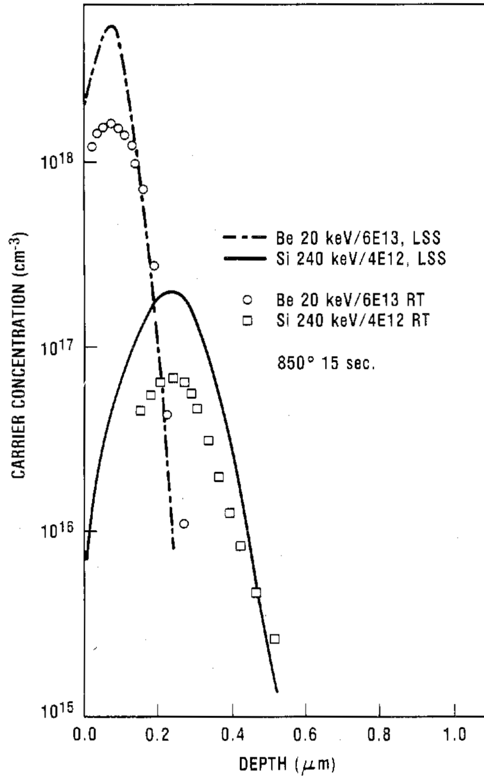


Fig. 2. Carrier concentration profile of the channel and the gate implants compared with LSS distributions.

used for all three implants was a 2000-Å-thick $SiN_x$ layer delineated by photoresist after $CF_4/O_2$ plasma etching. 240-keV Si implants were used for the channel (dose: 4E12/$cm^2$) and $n^+$ (5E13/$cm^2$) implants and a 180 keV As (6E13/$cm^2$)/20 KeV Be (6E13/$cm^2$) co-implant was used to form the gate. The implants were activated simultaneously in a rapid thermal annealer (RTA) with $Al_2O_3$ as the capping layer [11].

The resulting p-n junction profile is depicted in Fig. 2 and compared with the theoretical prediction of the LSS model. The concentration profile was obtained using an electrochemical Polaron profiler with dilute HCl solution as the electrolyte. Hall measurement showed a mobility of 2000 $cm^2/V \cdot s$ in the channel layer. A sheet resistance of 100 Ω/sq was measured from a $n^+$-implanted van der Pauw pattern.

The rest of the processing consists of depositing a $SiN_x$ passivation layer and p and n metallizations. Au-Zn/Cr/Au (20/1000/1000 Å) and Au-Ge/Ni/Au (800/200/1000 Å) were used as the gate and source–drain metals, respectively, which

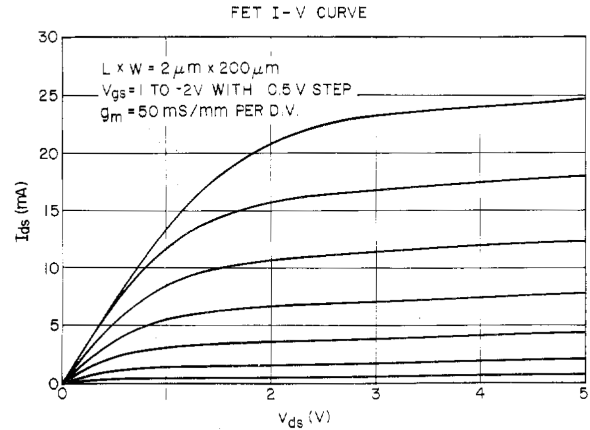


Fig. 3. A typical *I–V* curve of a JFET with a gate 2 μm long and 200 μm wide. The gate bias changes from +1 V (top trace) to −2 V (bottom trace) with a 0.5-V step.

were then alloyed in a RTA at 420 and 380°C for 30 s, respectively.

The device reported here has a gate length of 2 μm. The reduction of the gate length to the submicrometer region is presently limited by the resolution of the phololithographic system used. However, submicrometer devices can be fabricated if an etching technique similar to ones used in [2] or [7] is used in defining the $p^+$ region under the gate metal. This is being investigated.

## IV. Device Performance

Fig. 3 shows typical *I–V* characteristics of the FET with a 2-μm-long 200-μm-wide gate. The gate voltage used ranged from 1 to −2 V with 0.5-V steps. This device has a maximum $g_m$ of 75 mS/mm at +1-V gate bias, but with a high (1-mA) gate leakage current. At 0-V gate bias where this device is intended to operate, the $g_m$ is 50 mS/mm, the output impedance $r_d$ at $V_{ds} = 3$ V is 400 Ω·mm, with a gate-source capacitance $C_{gs}$ of 1.2 pF/mm. These transconductance values can be compared with the 30–40 mS/mm reported in [6] for the etched-gate JFET, the 53 mS/mm reported in [7] for the planar JFET, and the 75 mS/mm reported in [8] for the p-column JFET.

From these parameters, a 3-dB cutoff frequency ($f_T = g_m/2\pi C_{gs}$) of 6.6 GHz and an inverter gain ($g_m r_d$) of 20 are obtained. These data compare favorably with GaAs MESFET's where $f_T = 9 \sim 12/L$ GHz [10], [12], where $L$ is the gate length in micrometers, and $g_m r_d$ of 14 are typically obtained [12]. The FET pinches off well at −2.4-V gate bias. The drain current saturates at about $V_{ds} = 1.5$ V at 60 mA/mm (for $V_{gs} = 0$ V) and showed less than 0.4 percent of drift in 36 h of continuous biasing ($V_{ds} = 5$ V).

The linearity in the $1/C^2$ versus $V$ plot in Fig. 4 together with the Polaron carrier concentration profile in Fig. 2 proves the abrupt junction. The junction has a low dark current of 15 nA at −2 V for a 200-μm-wide gate as can be seen from the diode log *I–V* curve shown in Fig. 5. From the forward bias *I–V*, a diode ideality factor of 1.25 is obtained. With $V_{gs} = 0$ and $V_{ds} = 5$ V, the sum of the gate–source and the gate–drain leakage current is as low as 100 nA, an attractive feature for a low noise application such as an integrated p-i-n amplifier [13].

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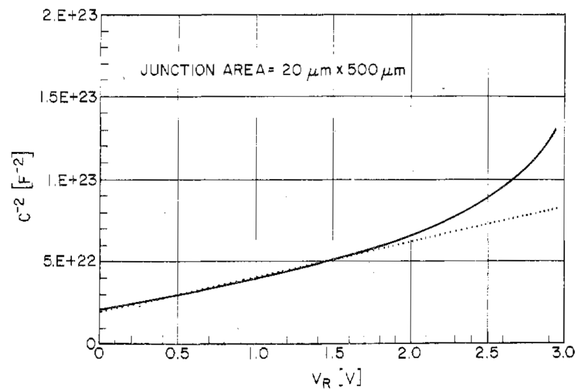


Fig. 4. Junction capacitance versus reverse bias shown as $1/C^2$ versus $V_R$ for the implanted junction diode. ($1/C^2 = 10^{22}$ (1.91 + 2.14 $V_R$) with goodness of fit of 0.9935 for $0 \leq V_R \leq 1.5$ V.)

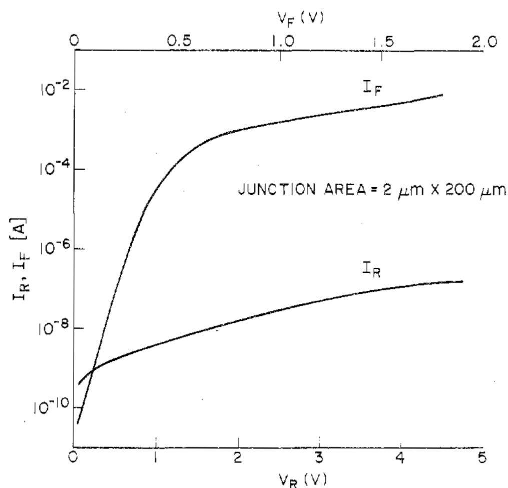


Fig. 5. The p-n junction forward and reverse bias $I$–$V$ characteristics shown in log scale.

## V. Conclusion

This ion-implanted JFET is simple in structure, requiring no critical processing, and yet it exhibits a high transconductance permitting a high-speed operation. The FET also has low dark current and low saturation current, which makes it well suited for low-noise low-power applications. Future work on this device includes reliability and high-frequency tests.

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