Abstract

In this thesis, I developed real-time image processing programs, which include shading correction, X-zoom, 2-D filtering and error diffusion half-toning, for a digital copier using a VLIW programmable digital signal processor, TMS320C6414. The CPU not only issues up to 8 instructions at each clock cycle but also supports SIMD (Single Instruction Multiple Data) type instructions. Thus, it is possible to implement the time-critical image processing functions in real-time while allowing the software-based implementation of less-frequently needed off-line functions, such as JPEG compression. However, it needs careful programming to exploit deep pipelining, multiple functional units and packed-data instructions. All the image processing algorithms for a digital copier are implemented through linear assembly programming followed by the assembly optimizing, and the results are compared with those of the manually optimized assembly codes. The results show that explicit disambiguation of memory dependency is most critical for the efficient use of the assembly optimizer. The results also show that it is more important to keep a regular structure for parallel processing instead of reducing the number of arithmetic operations.

Keywords: image processing, digital copier, VLIW, DSP, software pipeline, packed-data processing, parallel processing