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Reduction of threading dislocations in a Ge epitaxial layer grown on a Si(001) substrate

실리콘(001) 기판 위 성장한 게르마늄
에피층의 관통전위 감소에 대한 연구

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Abstract

Reduction of threading dislocations in a Ge epitaxial layer grown on a Si(001) substrate

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The primary goal of this research is to obtain high quality Ge layers on Si(001) substrates for various applications such as multi-junction solar cells and near-infrared photodetector. In order to achieve the final goals, this research is composed of three parts: two-step Ge growth, post RTA and Ge regrowth on silica nano-spheres (NS) integrated Ge/Si template.

First, Ge layers were grown on Si(001) substrates using UHV-CVD. By using two-step method, pure Ge layers with flat surfaces were successfully grown on Si suppressing 3-dimensinal growth. As the thickness increases from 250 to 900 nm, the threading dislocation density (TDD) in Ge layer was reduced from 2.4×10^9 to 4.3×10^8 cm^{-2} since threading dislocations in Ge layer annihilated during growth. The reduction of TDD leads to the quality improvement of Ge layer.

In order to reduce the TDD in Ge layer, post thermal treatment was done by rapid thermal annealing (RTA). When Ge layers were annealed by RTA, surfaces were roughened with pit formations. The surface roughening could be suppressed by depositing SiO_2 on Ge surface. However, RTA at 850 ^oC leads to the formation of large holes with the diameter of 20 μm, indicating the temperature limitation of RTA. As the RTA temperature increased from 650 to 800 ^oC, crystal quality was improved with reduced TDD. The reduction of TDD is caused by the thermal stress. The higher RTA temperature can induce more stress into Ge due to the difference of thermal expansion coefficient between Ge and Si, allowing dislocations to glide and to be annihilated more easily. However, after RTA at 800 ^oC, TDD was 2.24 x 10^8 cm^{-2}. For further reduction of TDD, cyclic RTA was performed. Repetitive tensile and compressive stresses are induced in Ge layer during cyclic RTA. Increasing the number of cycle lead to more effective TDD reduction rather than RTA time increasing and TDD of 3.5 x 10^7 cm^{-2} was obtained by 20 times RTA. The amount of TDD reduction per each cycle decreased as the number of cycle increased due to the increasing average distance between two adjacent dislocations.

Then, Ge layer grown on vicinal Si(001) substrate was annealed by cyclic RTA for the MJSC application. Unlike Ge layer grown on nominal Si(001), TDD was 1.96 x10^8 cm^{-2} even after 10 times RTA which is higher value than that of Ge layer grown on nominal Si(001). TEM analyses show that Ge layer grown on vicinal Si(001) has more edge dislocations compared to Ge layer grown on nominal Si(001). In

Ge, pure edge dislocation has burgers vector of a/2[1-10] which lies on (001) plane. Because (001) is not the slip plane, edge dislocations are immobile. Ge layers grown on vicinal Si(001) with more edge dislocations are less affected by RTA. Reduced TDD in Ge enhanced the optical properties of GaAs grown on Ge/Si by cathodolumineascence.

Finally, Ge regrowth was proceeded on dislocation masked Ge/Si templates with silica NSs. The templates were fabricated in a three-step: two-step growth of initial Ge layer, defect etching by Secco etchant and integration of silica NSs into etch pits. Dislocations were selectively etched with inverted pyramidal shape by using Secco etchant and each plane of etch pit has {113} facets. The etch pit density of initial Ge layer was 6.44 x 10^8 cm^{-2}. The size of etch pits increased with etch time increasing. Beyond 120 sec, the pit size was decreased and saturated due to the intersection of near etch pits, roughening surfaces. Then, silica nano-spheres were coated on the 60 sec etched Ge/Si substrates by spin coater. By controlling the concentration of silica in ethanol, silica NSs can be preferentially integrated into only etch pits not on the planar surface. When Ge was grown on the silica NSs integrated Ge/Si templates, 3-dimensional growth was observed like selective epitaxial growth on patterned substrates. The lower temperature growth suppressed the formation of {111} facet and enhanced lateral overgrowth. By regrowing Ge in a two-step, fully coalesced Ge layer was obtained but surface was roughened due to the facet growth. TEM analysis confirmed that dislocations were blocked by silica NSs and

were not propagated toward surface. At some regions, there were dislocations generated from the silica NSs due to the growth error during epitaxial lateral overgrowth. The resulting TDD in regrown Ge was 6.94 x 10^7 cm^{-2}, and further reduction to 1.4 x 10^7 cm^{-2} was possible combined with 10 times RTA. However, rough surface requires additional planarization process.

Keywords: ultrahigh vacuum chemical vapor deposition (UHV-CVD), Germanium, rapid thermal annealing (RTA), regrowth, silica nano-sphere
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Contents

List of Tables

List of Figures

Chapter 1. Introduction

In 21th century, technologies have been changed in information, communication and energy conversion. Most of efforts are focused on the Si due to the fact that Si based process has been widely investigated ,based on reliable mass production such as oxidation, etching, cleaning lithography and so on. However, there exist problems of advanced Si based technologies in semiconductor industry such as short channel effect.[1] Furthermore, indirect bandgap of Si limits the application of Si on optical devices. In order to overcome such limitations, new materials and novel device design are required.

Table 1-1 shows the properties of semiconductor materials.[2] Ge has a diamond structure, high carrier mobilities and similar lattice constant with GaAs. Each property makes a Ge as a strong candidate for various device applications with high performance such as electronic and optical devices. The high carrier mobility shows the possibility to be used for ultra-large scale integration (ULSI) applications beyond 32 nm node. The similar lattice constant with GaAs open the opportunity to replace Si channel in complementary metal-oxide-semiconductor (CMOS) devices with Ge and GaAs. Due to the higher hole mobility of Ge and higher electron mobility of GaAs than those of Si, high performance CMOS can be fabricated consisted of Ge pMOS and GaAs nMOS.[16]

Recently, Ge has been adapted to optical devices due to the narrow bandgap of 0.67 eV and high absorption coefficient at

near-infrared (NIR) region. Furthermore, optical properties of strained Ge has been revealed.[3] Figure 1-1 shows the E-k diagrams of Ge. Bulk Ge is known to have indirect bandgap in which minima of conduction band (CB) has different k value from valence band (VB) maxima. The electron in CB minima falls to VB, undergoing momentum and energy change. In indirect bandgap semiconductor, radiative transitions are involved with heat rather than photon. In the case of Ge, energy difference between direct gap at Γ valley and indirect bap at L valley is 136 meV. When biaxial tensile stress is applied to Ge, both direct and indirect gap begins to shrink. In this case, direct gap shows faster shrinkage. Thus, Ge changes from indirect to direct gap material with increasing tensile stress, meaning that improved optical properties.

The growth of Ge on a Si substrate is a promising technology in that high performance Ge device can be fabricated on cheap Si wafers with large area. Furthermore, when Ge epitaxial layer is grown on Si at high temperature and then temperature is cooled down to room temperature, tensile strain is accumulated in Ge layer due to the difference of thermal expansion coefficient between Si and Ge, indicating that tensile strained Ge layer can be obtained by epitaxial growth of Ge on Si. The improved absorption coefficient of epitaxially grown Ge on Si is shown in Fig. 1-2.[4]

However, when Ge layer is grown on a Si substrate, there are two main problems due to 4.2% lattice mismatch between Ge and Si: rough surface and generation of threading dislocations. In order to adapt Ge layer on device applications, flat Ge layer with

low defect density is required.

In this study, Ge layers were grown on Si(001) substrates using two-step method in ultrahigh vacuum chemical vapor deposition (UHV-CVD). In addition, two methods were proposed to obtain Ge layer with reduced threading dislocation density: post RTA and Ge regrowth on silica nano-spheres integrated Ge/Si templates.

Table 4-1 Material properties of semiconductors.[2]

	Structure	E_g (eV)	a (nm)	m_n (cm^2/Vs)	m_p (cm^2/Vs)
Si	Diamond	1.12	0.543	1350	480
Ge	Diamond	0.67	0.565	3900	1900
GaAs	Zincblende	1.43	0.565	8500	400
InAs	Zincblende	0.36	0.303	40000	500

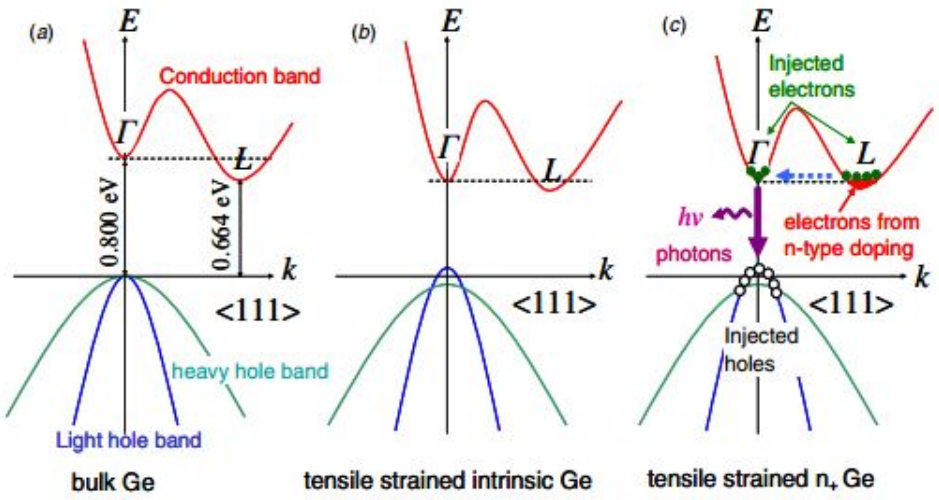

Fig.1-1.E-k diagram of (a) bulk, (b) tensile strained intrinsic and (c) tensile strained n^+ Ge.[3]

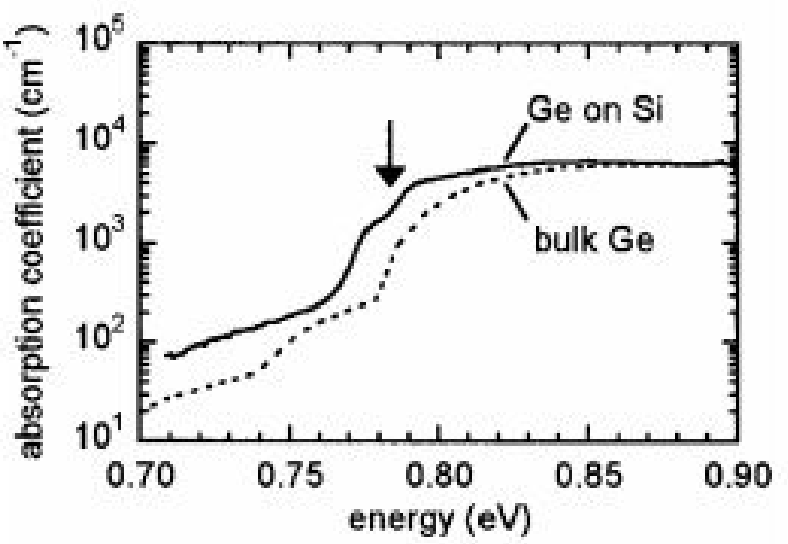

Fig.1-2. Absorption coefficient of Ge on Si and bulk Ge.[4]

1.1 Device applications of Ge layers grown on Si

1.1.1 NIR photodetector using Ge layer

The interest in opto-electronics has been grown to solve the problem of interconnects for high-density systems. To realize the integration of electronic-photonic integration, one of important part is photodetector. Although Si has indirect bandgap, the studies of photodetctor using Si were progressed due to the progress of Si-based semiconductor technology. However, the fabrication of Si photodetector with high performance is still challenge.[5] Photodetectors using III-V materials showed high performance in near infrared region (NIR) but they are not compatible with Si-based technology.[6] Alternative choice for NIR photodetector is Ge epitaxial layer grown on Si. The bandgap of Ge is suitable for the absorption of 1.3-1.55 μm wavelength and Ge is compatible with Si-based technology.[7,8,9,10]

Metal-semiconductor-metal NIR photodetector was fabricated by Colace et al. as shown in Fig. 1-3.[7] Low dark current, high response and high efficiency was obtained under 1.55 μm by using metal contact which is light transparent. Oehme *et al.* reported that high performance NIR photodetector was fabricated with quantum efficiency of 10-20% in by using Ge p-i-n structure (Fig. 1-4).[8] However, in this structure, misfit dislocation arrays at the interface induce high dark current.

1.1.2 Multi-junction solar cells

The solar cell is a promising energy source which converts solar energy to electricity. Furthermore, semi-permanent power can be obtained by a highly efficient solar cell at low cost without pollution.[11]

There have been many researches about solar cell fabrication using various materials. So far, many materials have been suggested such as silicon, copper indium diselenide (CIS), copper indium gallium diselenide (CIGS), cadmium telluride (CdTe), dye-sensitized solar cells and III-V compound semiconductor.[12,13,14,15,16,17,18]

Among them, III-V compound semiconductor materials such as GaAs are direct bandgap materials and have high absorption coefficient, meaning that thinner layer is required to absorb sunlight. Figure 1-5 show the reported timeline of conversion efficiency of various solar cells from National Renewable Energy Laboratory (NREL). In Fig. 1-5, solar cells with III-V materials show the highest efficiency. Because GaAs solar cells are less influenced by heat and radiation damage, they have been used for concentrator photovoltaic and space application. III-V materials are very attractive to obtain solar cells with high conversion efficiency because of their direct bandgap. For further increasing conversion efficiency, the multi-junction solar cell was proposed in which subcells composed of materials with different bandgap are stacked monolithically. The each subcell in connected by tunnel junction. In multi-junction solar cells (MJSCs), material with larger bandgap is located on the material

with narrower bandgap. By using this structure, sunlight with long and short wavelength are absorbed within large and narrow bandgap materials in sequence, respectively. Therefore, loss of sunlight can be minimized using MJSCs, leading to the higher conversion efficiency. In order to fabricate MJSCs based on III-V materials, lattice constant also should be considered besides bandgap. When materials are grown on another materials which has different lattice constant, defects are generated from the interface which degrade solar cell performance. GaInP/GaAs/Ge is the typical structure of III-V MJSCs which have similar lattice constant of 0.565 nm but different bandgap as shown in Fig. 1-6.[17,18] In this structure, ultraviolet and visible region are absorbed by GaInP with E_g of 1.85 eV. Near-infrared light is absorbed by GaAs which has bandgap of 1.42 eV. The rest of lower photon energies in the longer wavelength region are absorbed by Ge with E_g of 0.67 eV. As shown in Fig. 1-5, MJSCs with III-V materials show the highest conversion efficiency above 30%.

In MJSCs, Ge acts as a bottom cell due to its narrow bandgap and a substrate. Si has better material properties such as mechanical strength and thermal conductivity than those of Ge. Furthermore, large Si wafer with cheap price is available. Therefore, if Ge substrates can be replaced with Si substrates, it is possible to monolithically integrate a highly efficient multi-junction structure on a Si substrate with large area.

However, the lattice constant of Si is 0.543 nm which is smaller one than that of GaInP, GaAs and Ge. Therefore, threading dislocations are generated during the Ge growth on Si. Several

studies were performed to fabricate MJSCs on Si. The state-of-art MJSCs on Si were made by Andre *et al.* of Ohio State University.[19] The structure of MJSC and I-V curve are shown in Fig. 1-7. They used $Si_{1-x}Ge_x$ buffer layer to reduce threading dislocation density (TDD) and obtained conversion efficiency of 18.1% with low TDD of 1 x 10^6 cm^{-2}. In previous research of my laboratory, directly grown Ge layer on Si was adjusted to MJSCs.[20] GaAs/Ge double junction solar cell was fabricated on Si and the structure is presented in Fig. 1-8(a). While the double junction solar cell fabricated on Ge substrate shows the conversion efficiency of 23.6% with the V_{oc} of 1.18 V and J_{sc} of 25.4 A/cm^{-2}, conversion efficiency dropped to 10.6% with V_{oc} drop of 0.83 V by replacing Ge substrate with Si substrate.(Fig. 1-8(b))

Oh *et al.* simulated the effect of threading dislocation on the solar cell operation.[21] They reported that when threading dislocations exist in solar cell structure, carrier lifetime and thus efficiency is reduced with TDD increasing as shown in Fig. 9. Therefore, in order to achieve MJSCs on Si with high conversion efficiency, TDD reduced III-V and Ge layer should be grown on Si.

1.1.3 Channel application using Ge layer

Ge channel in MOSFET has superior advantages due to higher electron and hole mobility than thouse of Si.[22] High carrier mobility allows boosting the drive current of the transistors. The lower bandgap of Ge makes further V_{DD} scaling possible. Moreover, the thermal budget can be reduced because dopant in

Ge is activated at lower temperature around 500 – 600 ^{o}C compared to Si (1000 – 1100 ^{o}C), making Ge interesting with respect to high-k/metal gate.[23] Finally, similar lattice constant of Ge and GaAs shows the possibility of fabracation of high speed CMOS consisted of Ge p-MOS and GaAs n-MOS as shown in Fig. 1-10.[24]

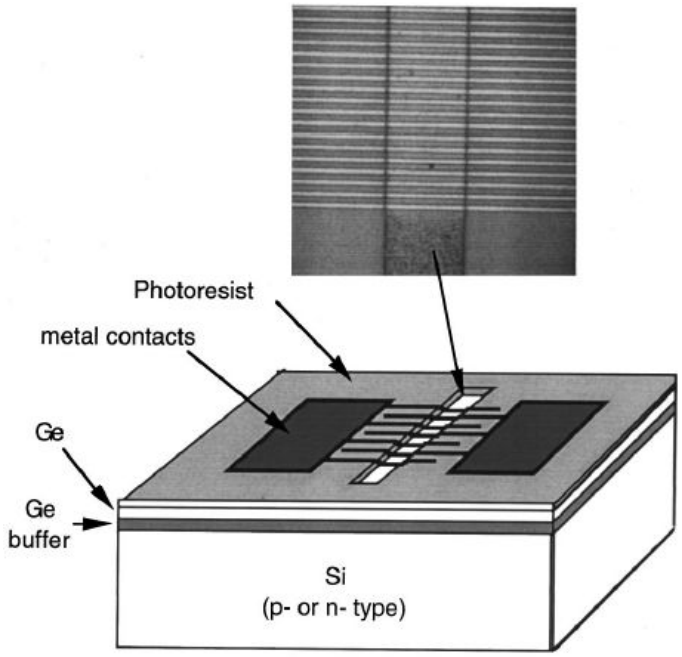

Fig.1-3. Schematic image of metal-semiconductor-metal photodetector.[7]

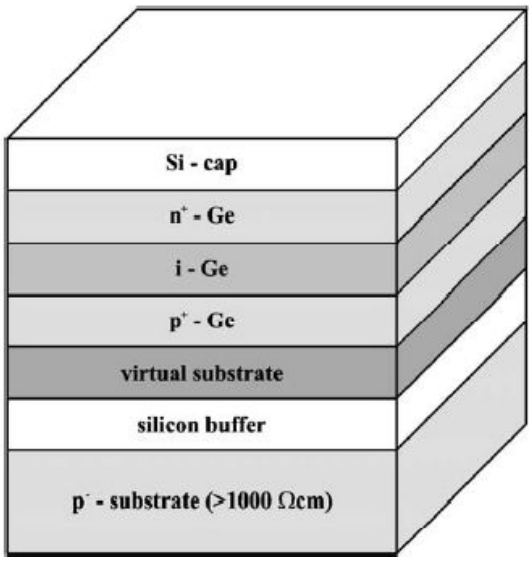

Fig.1-4. Schematic diagram of vertical-type p-i-n photodetector.[8]

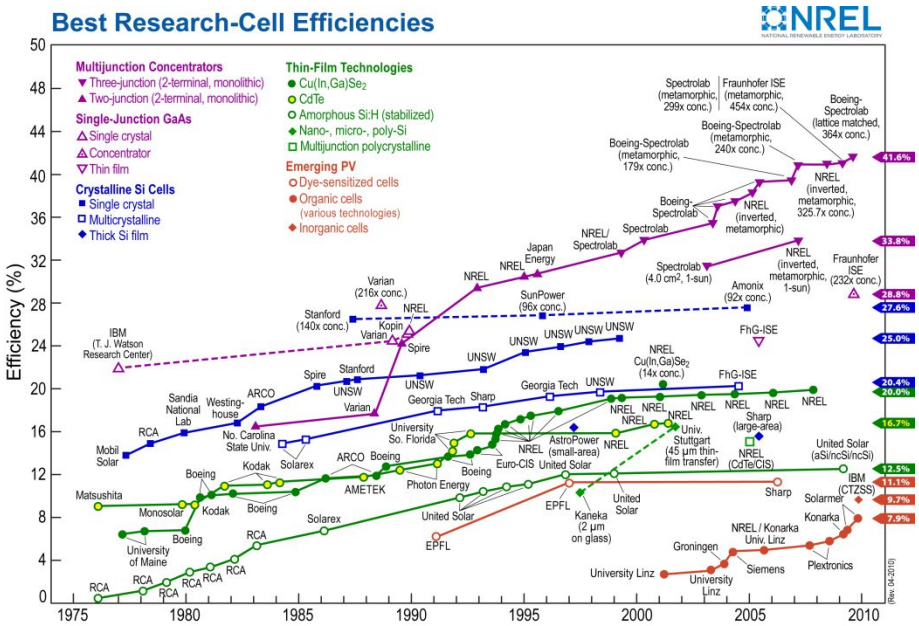

Fig. 1-5. The chart of solar cell conversion efficiency from National Renewable Energy Laboratory.(NREL)

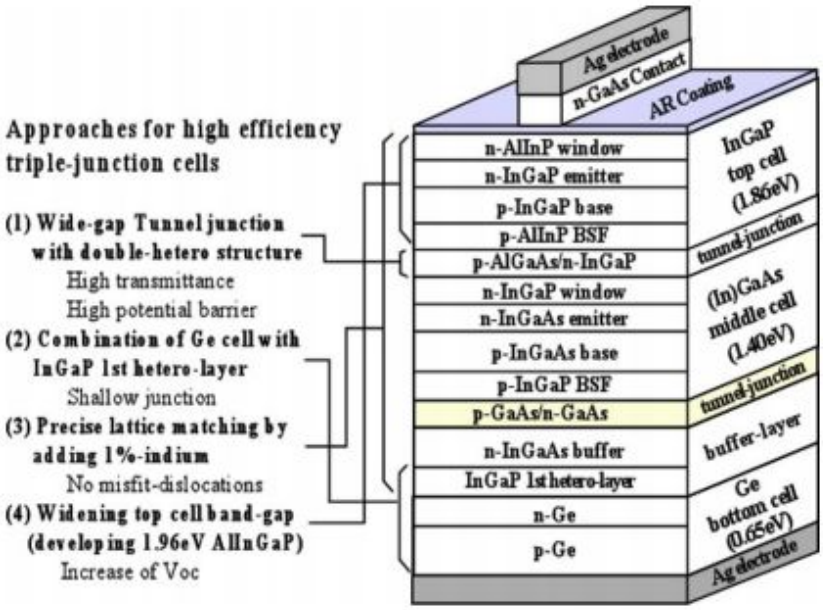

Fig. 1-6. Schematic depict of triple-junction solar cells.[18].

(a)

p^{++} GaAs contact layer (1000Å)	~1x10^{19} cm^{-3}
p^{+} $In_{0.49}Ga_{0.51}P$ window (500 Å)	~1x10^{18} cm^{-3}
p^{+} GaAs emitter (5000 Å)	~2x10^{18} cm^{-3}
n GaAs base (2.0 μm)	~1x10^{17} cm^{-3}
n^{+} $In_{0.49}Ga_{0.51}P$ back surface field (1000 Å)	~1x10^{18} cm^{-3}
n^{+} GaAs buffer (1000 Å)	~1x10^{18} cm^{-3}
low-temperature n^{+} GaAs buffer (1000 Å)	~2x10^{18} cm^{-3}
SSMBE Ge buffer layer (300 Å)	uid
Ge termination layer (~1.0 μm)	~1x10^{18} cm^{-3}
n SiGe step graded buffer layers (~ 10 μm)	~1x10^{18} cm^{-3}
n Si substrate	~0.5-2 1x10^{18} cm^{-3}

(b)

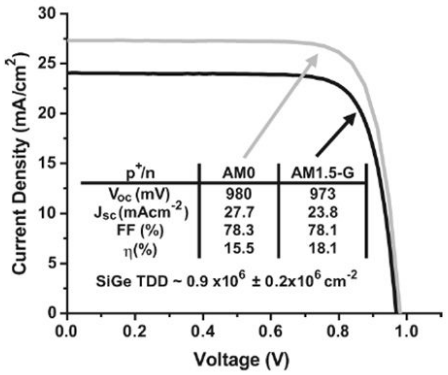

Fig. 1-7. (a) p^+/n GaAs solar cell device structure grown by MOCVD on Ge–$Si_{1-x}Ge_x$ –Si substrates depict of triple-junction solar cells and (b) J-V curve.[19]

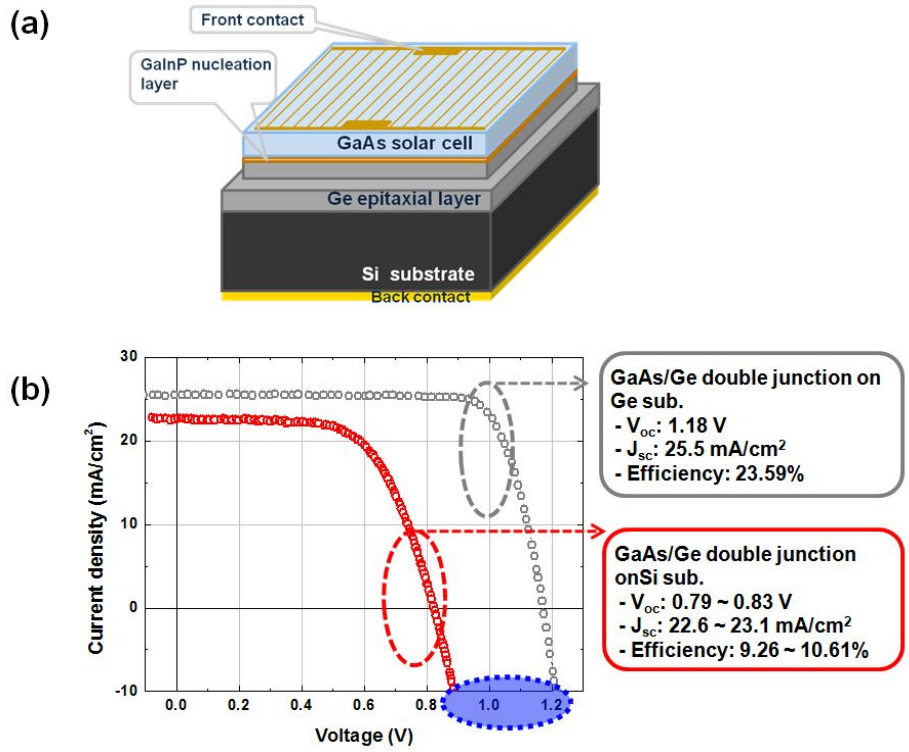

Fig. 1-8. (a) Schematic image of GaAs/Ge double-junction solar cell fabricated on Si substrate. (b) J-V curves of GaAs/Ge double-junction solar cells fabricated on Ge and Si substrates.[20]

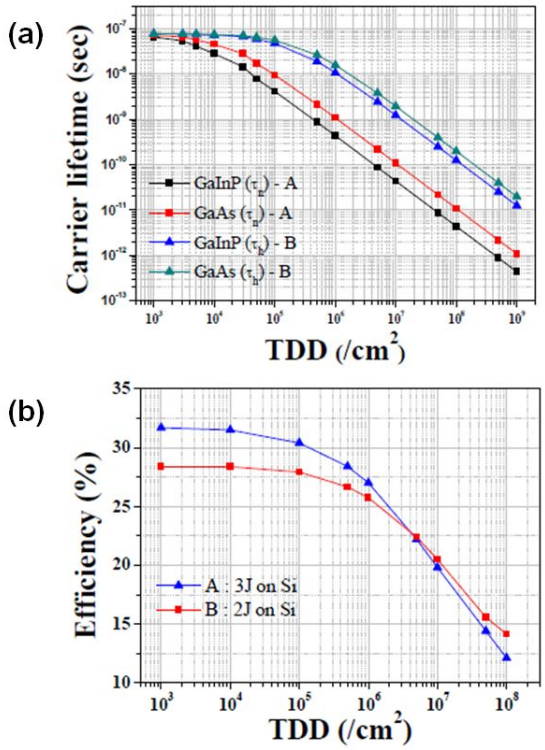

Fig. 1-9. (a) Minority carrier lifetime and (b) efficiency of MJSC on Si as a function of TDD.[21]

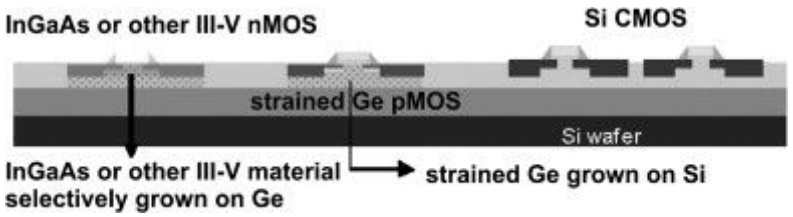

Fig. 1-10. Schematic image of the integration of Ge and GaAs in a planar CMOS technology on Si substrates.[24]

1.2 Methods of Ge growth on Si

When the Ge is grown on Si substrate, stress is built in Ge layer at the initial growth stage. The main reasons of stress are from two sources: the difference in lattice constant (4.2%) and different thermal expansion coefficient between Ge and Si. Due to the stress, the in-plane lattice constant of Ge layer is elastically distorted to that of the substrate in Fig. 1-11(a). The tetragonally distorted Ge layer accommodates large elastic strain energy. Beyond critical thickness, few monolayers in the case of Ge on Si, stress is relaxed by two main mechanisms: surface roughening and formation of misfit dislocation. Figure 1-11(b) shows that atomic bonds are relaxed towards their equilibrium length and orientation by surface roughening. The rough surface inhibits the planarization processing for the device fabrication. Another mechanism for strain relaxation is formation of misfit dislocation which allows Ge layer to relax toward bulk lattice constant as shown in Fig. 1-11(c). When misfit dislocations are generated at the interface, the geometrical requirement is that a dislocation should terminate at another dislocation or at a free surface. This needs threading dislocations which thread through Ge layer to the surface. Generally, misfit dislocation is connected with two threading dislocations at each end.[25] It is well known that threading dislocation acts as a non-recombination center, degrading device performance. Figure 1-12 shows that leakage current of SiGe p-i-n diode increases as the threading dislocation density (TDD) increases.[26] Thus, In order to adapt Ge layer grown on Si to devices, flat Ge layer with low TDD is required and many methods to grow Ge on Si have been suggested.

1.2.1 Compositionally-graded buffer layer

The compositionally-graded buffer layer has been widely used in order to obtain strain relaxed $Si_{1-x}Ge_x$ layers on Si(001) substrates. The composition of Ge in graded buffer layer is gradually increases and misfit strain is relieved as the thickness increases.[27,28,29,30]. Figure 1-13(a) shows the schematic image of the relaxation process in graded buffer layer. It has been reported that rougher surfaces was obtained when the compositional grading rates and/or final Ge content were higher.[28] Thus, in order to grow strain relaxed $Si_{1-x}Ge_x$ with root-mean-square (RMS) roughness less than 10 nm, thick buffer layer is needed with the typical thickness of 5 to 10 μm.

Since the Ge content is increases gradually, there exists mismatch in whole graded buffer layer, forming misfit dislocations as each grading step as shown in Fig. 1-13(b).[31]. Strain fields of misfit dislocations can block the glide of threading dislocations, resulting in dislocations reduction. Thus, low grading rate and thick layer is required to decrease the TDDs on the top of graded buffer layers. Currie *et al.* reported that *ex-situ* chemical-mechanical polishing (CMP) process at x =0.5 reduced TDD to 2.1 x 10^6 cm^{-2}(Fig. 1-14).[32] However material consumption to grow μm-range thick layers and the requirement of post CMP for further reduction of the final surface roughness remain have been known as disadvantages.

1.2. 2 Surfactant mediated Ge growth

Layer-by-layer growth is possible by introducing surfactant beyond critical thickness. Mostly group V elements has been used such as As and Sb. The island formation can be kinetically suppressed because surfactants reduce surface energy of Ge. Figure 1-15 show that Sb is more effective to grow 2-dimensional Ge layer.[33] Furthermore, it is reported that the TDD was reduced to 2 x 10^7 cm^{-2} by using Sb as a surfactant.[34] However, those group V elements can cuse the unwanted doping which deteriorates electrical properties of Ge. To avoid such problem, hydrogen was introduced as a surfactant which can saturate Si surfaces and is used as a carrier gas or dissociation by-product of source gas. It has been reported that layer-by-layer Ge growth was possible by using hydrogen because that increased the adsorption sites and decreased the diffusivity of Ge adatom.[35,36]

1.2. 3 Two-step growth

High quality Ge layers can be directly grown on Si substrates without graded buffer layers. Two-step growth has been proposed by many groups to grow two-dimensional Ge layers on Si substrates, suppressing island formations.[37,38,39,40] In two-step growth, Ge buffer layers are grown on Si substrates with the thickness of 40-100 nm at 300-350 ^oC. At such low temperature (LT), diffusion length of adatom on the surface is reduced and hydrogen acts as a surfactant, leading to the suppression of island formations.[39,40] The following Ge growth at higher temperature (HT) above 500 ^oC enhances growth rate and crystal quality. In my previous experiments, when LT buffer layer is thick

enough, Ge growth is no longer affected by lattice mismatch between Si and Ge. Thus, flat surface is still maintained during HT growth as shown in Fig. 1-16.[40] However, the TDD in Ge layer is typically 10^8-10^9 cm^{-2}.[38] For further reduction of TDD, modified two-step growth was suggested using thin SiGe layers.[41,42,43] Loh *et al.* reported that low TDD of 6 x 10^6 cm^{-2} was achieved by using this method.[42]

1.2.5 Aspect ratio trapping (ART) and epitaxial lateral overgrowth (ELO)

It has been reported that TDD was greatly reduced by a combination of substrate patterning and selective epitaxial growth and this technique is called as ART.[44,45,46]. As shown in Fig. 1-17(a), ART technique is effective in TDD reduction because threading dislocations are trapped in trenches. The threading segments in diamond structures on (111) plane make 45^o to Si(001) surface. Thus, if aspect ratio is higher than 1, they are blocked by side wall, resulting in the defect free top surface and Fig. 1-17(b) represents the results of ART. Figure 1-17(c) shows that planar defects such as twin and stacking faults are generated from the ELO fronts on SiO_2 after coalescence.[44] Furthermore, anisotropic growth within trenches with facet formation requires planarization process.[46]

1.2.6 Ge regrowth on patterned Ge/Si templates

Leonhardt *et al.* suggested the Ge regrowth for the defect reduction in Ge layer.[47] They used passivation step to fill the etch pits which were originated from the threading dislocation

using SiO_2 and Ge layers were subsequently regrown over SiO_2 lined etch pits. The total process flow is depicted in Fig. 1-18(a).The threading dislocations are blocked by SiO_2 as shown in Fig. 1-18(b). While the TDD in initial Ge layer was 2.6 x 10^8 cm^{-2}, total defect density was reduced to the 8.7 x 10^6 cm^{-2} after regrowth step. However, planar defects such as twin and/or stacking fault are resulted from the coalescence of Ge ELO layer over SiO_2 lined etch pits. They proposed that the planar defects might be originated from the atomic-scale roughness of SiO_2 and/or translation misalignment and/or thermal stress. Reduced total defect density was obtained of 1.7 x 10^6 cm^{-2} by annealing initial Ge layer.(Fig. 1-18(d))

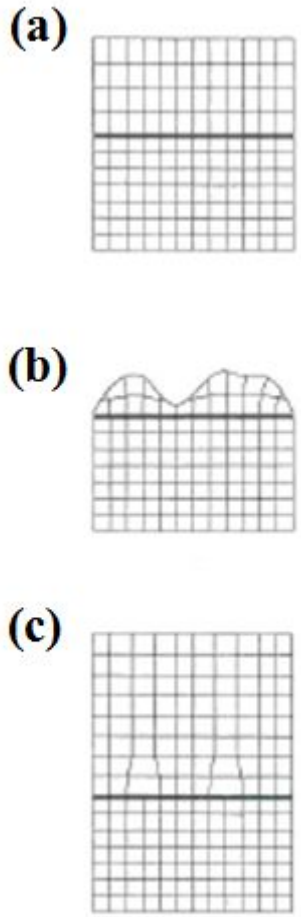

Fig. 1-11. Schematic images of (a) tetragonal distortion, (b) roughening and (c) plastic relaxation via misfit dislocations of epitaxial layer.[25]

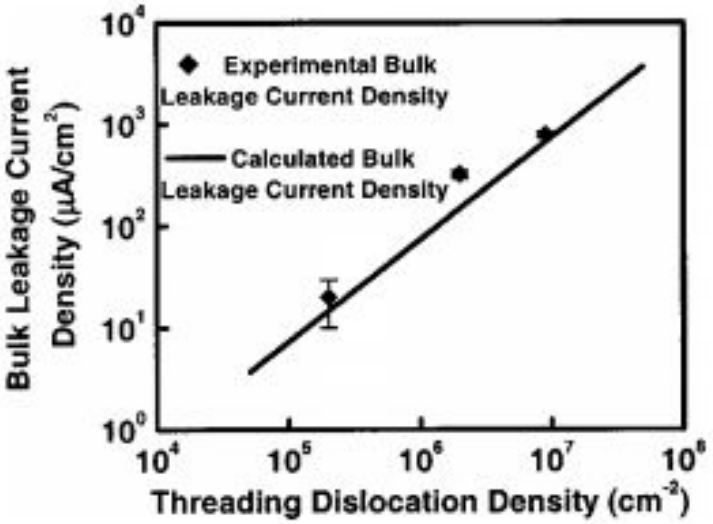

Fig. 1-12. Bulk leakage current density as a function of threading dislocation density.[26]

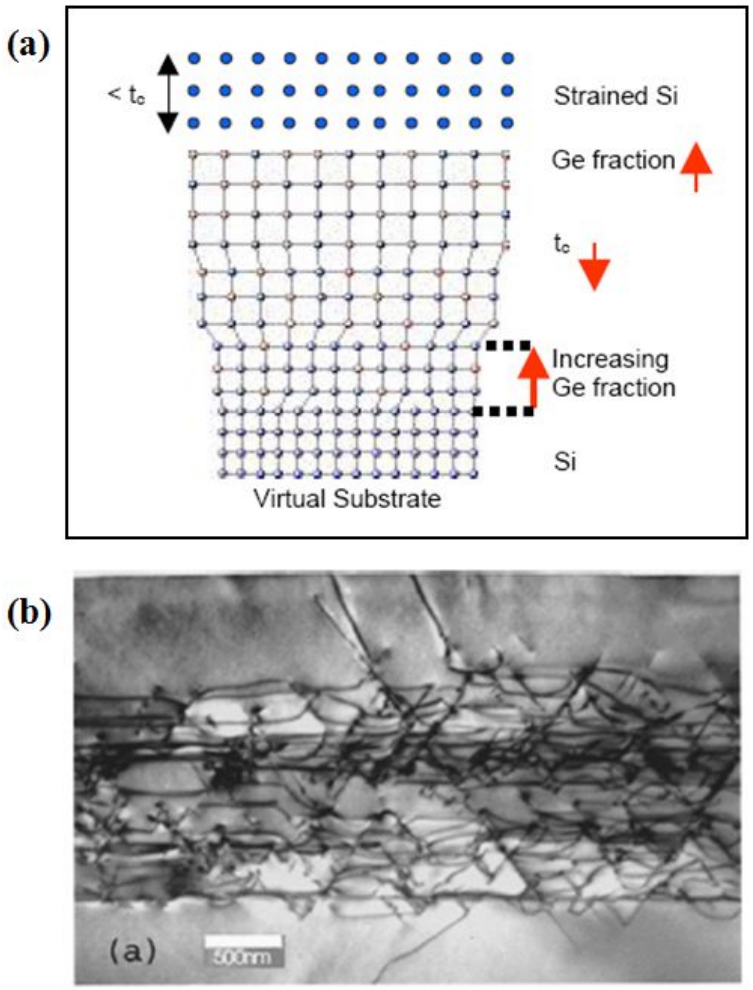

Fig. 1-13. (a) Schematic image of the strain relaxation in compositionally-graded $Si_{1-x}Ge_x$ buffer layers and (b) network of dislocations formed at each steps of composition grade. Threading dislocations are confined in the graded buffer region.[31]

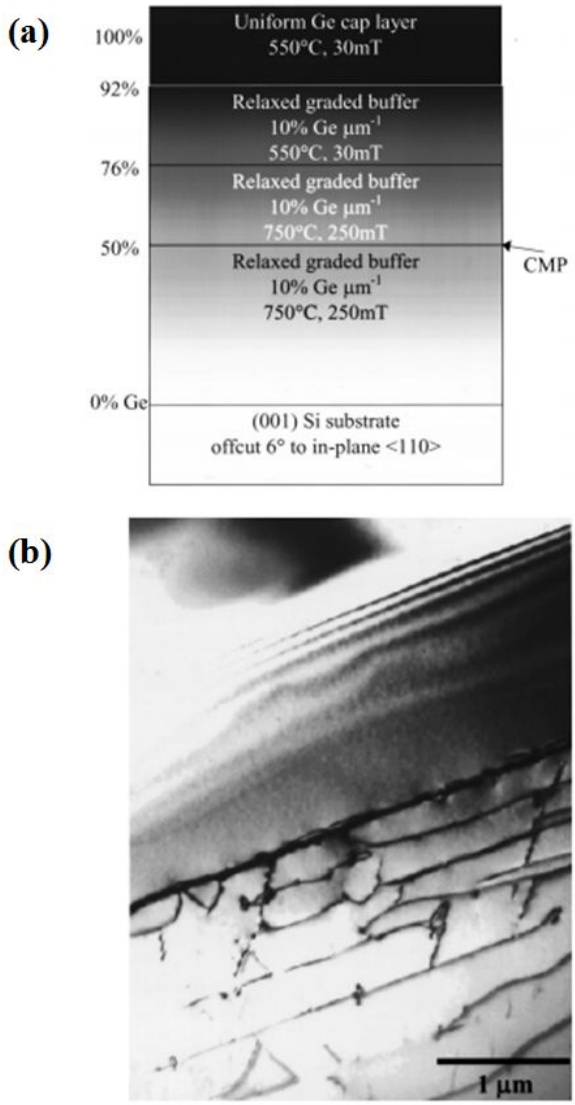

Fig. 1-14. (a) Schematic of the structure and growth conditions using graded buffer layer combining with CMP and (b) cross-sectional TEM image of corresponding sample.[32]

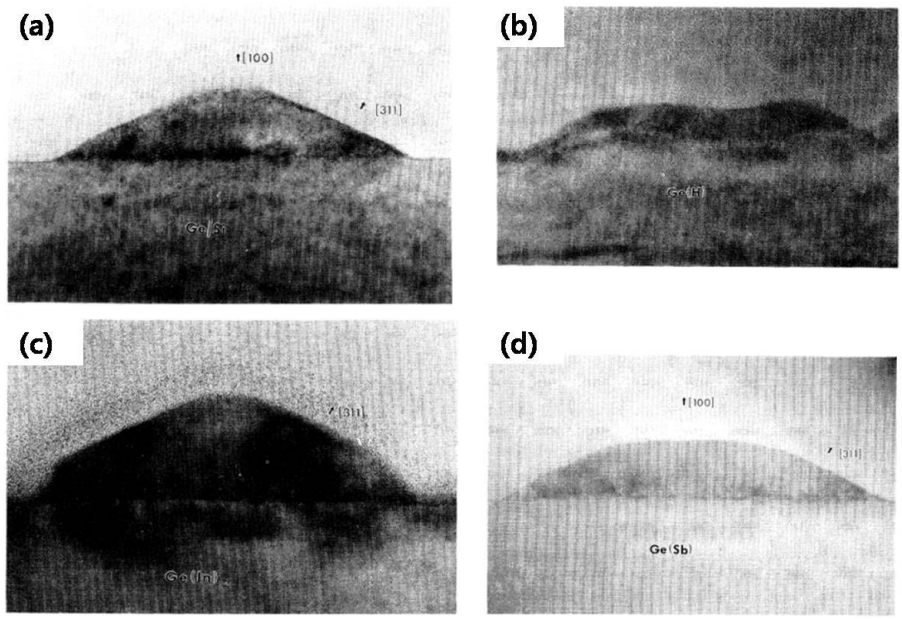

Fig. 1-15. Cross-sectional TEM images of Ge on Si (a) without surfactant and with (b) H, (c) In, (d) Sb as surfactant.[33]

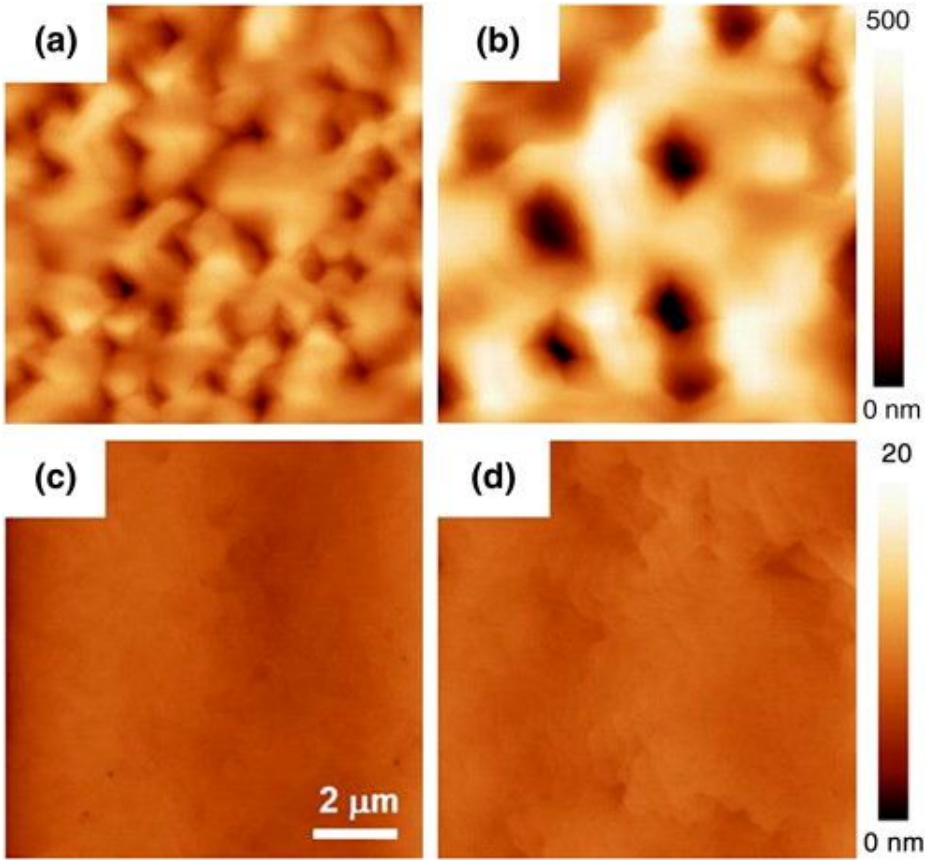

Fig. 1-16. 10 × 10 μm^2 AFM images of two-step grown Ge layers on Si using LT Ge buffer layers of (a) 20, (b) 40, (c) 60 and (d) 80 nm. The RMS roughnesses of samples are 59.7, 100, 0.5, and 0.8 nm, respectively.[40]

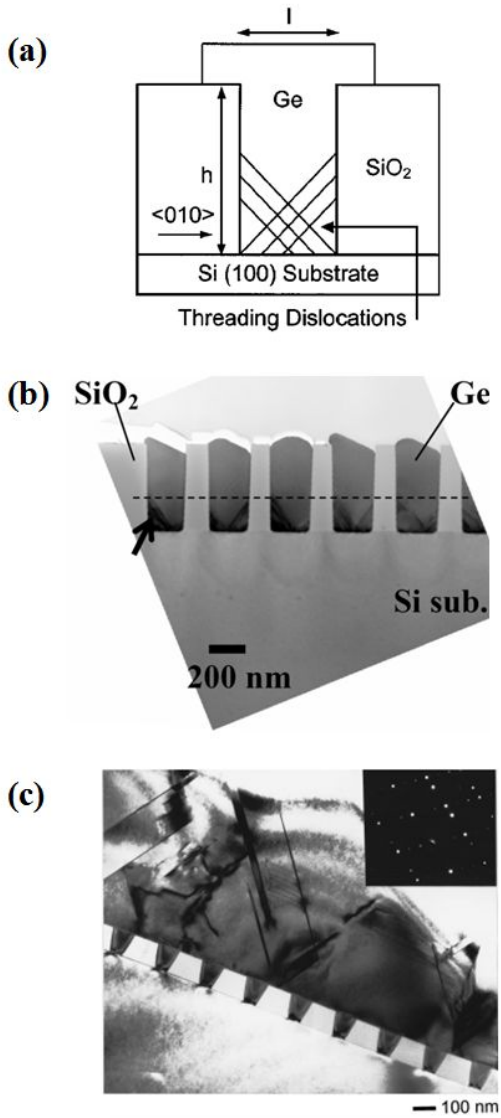

Fig. 1-17 (a) Cross-sectional schematic of Ge growth on Si by ART, (b) the threading dislocations are trapped by the oxide sidewall and (c) the defects are originated from ELO coalescence.[44,45]

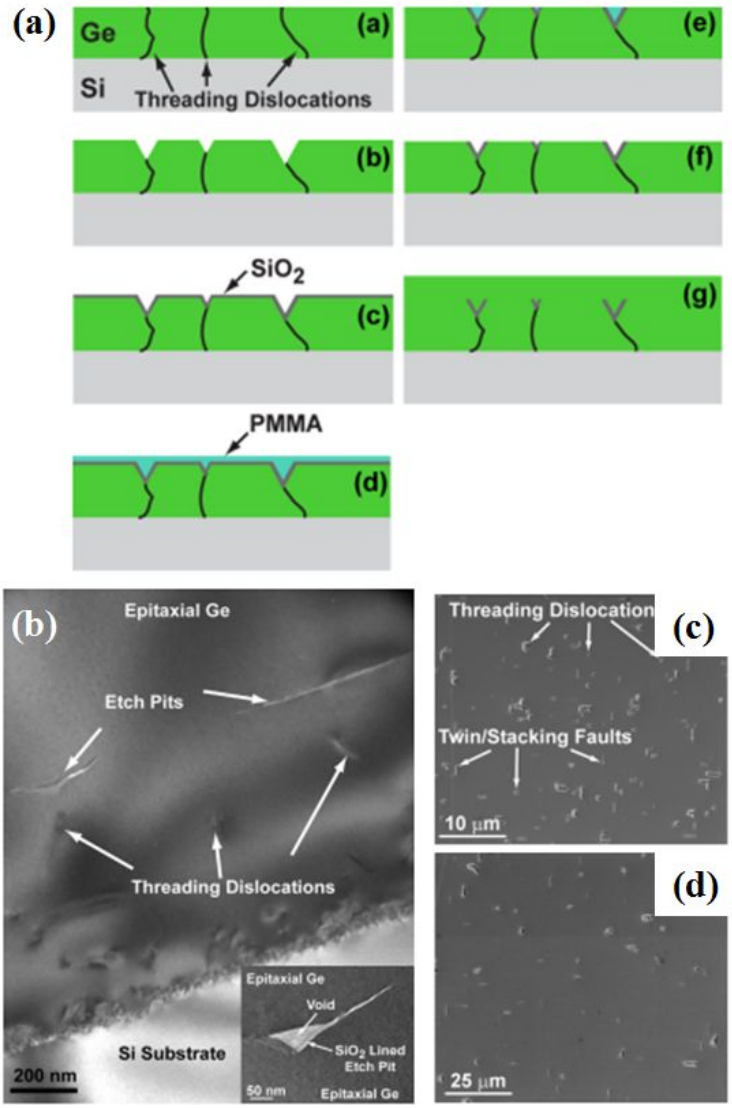

Fig. 1-18 (a) Schematic images of the sample fabrication process, (b) cross-sectional TEM image of regrown Ge ELO films over SiO_2 lined etch pits, (c) and (d) show the etch pit density in regrown Ge layers (c) without and (d) with annealing of initial Ge layer.[47]

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Chapter 2. Experiments and analysis

2.1 Growth equipment

2.1.1 Ultrahigh vacuum chemical vapor deposition (UHV-CVD)

In this work, All Ge layers were grown on Si(001) substrates by a cold-wall type ultra high-vacuum chemical vapor deposition (UHV-CVD). The schematic of the UHV-CVD system is presented in Fig. 2-1. The equipment is composed of load lock and main chamber to maintain vacuum of main chamber and inhibit the contamination during the loading Si wafer. Load lock chamber is connected with turbomolecular pump with pumping speed of 400 l/sec backed by rotary pump and 1 x 10^{6} torr can be achieved within 2 min. Re-contamination of ex-situ cleaned Si wafers is minimized by purging with high-purity nitrogen. Si wafers are transferred from load lock chamber to main chamber by magnetic loading arm.

Main chamber has turbomolecular pump with pumping speed of 1300 l/sec backed by rotary pump and ion pump with pumping speed of 220 l/sec in order to maintain the pressure of 3 x 10^{-9} torr. Main chamber is cooled by water and is equipped with heating line to eliminate contaminations stick to the inner wall of chamber. Susceptor is made with high purity graphite and Si is deposited on surface to suppress out-gassing. Si wafer loaded from load lock chamber is attached to susceptor by Mo pin and the susceptor is designed to use 6 inch wafer. The susceptor can move along Z direction maintaining ultra high vacuum. Heating element is

sintered SiC and consists of 2-zone; 4 inch circular inner heater and 3 inch ring-shaped outer heater. The temperature uniformity on whole susceptor is controlled within 1% by controlling inner heater and outer heater independently. Heating elements are fixed with quartz supporters by Mo electrodes and are cooled by water for stable operation in high temperature.

During experiments, H_2 gas having 99.9999% purity was used through gas purifier. Gas purifiers are also installed in 99.99% Si_2H_6 (diluted to 10% by He), 99.999% GeH_4 (diluted to 5% by H_2) lines to limit content of oxygen and water vapor less than 1 ppb. Gases used in experiments are flown into main chamber through nozzle installed in upper area of the chamber in order not to be directly flushed on Si wafers. Flow rate of source gases is controlled by mass flow controller (MFC) and pneumatic valve without delay and by-pass line is installed to infiltrate stabilized source gas into main chamber.

2.3.1 Metalorganic chemical vapor deposition (MOCVD)

The III-V layers were grown by a Axitron 2600 G3 low pressure metal-organic chemical vapor deposition (MOCVD) system which is consisted of electrical cabinet, gas mixing cabinet, operation terminal, reactor cabinet and RF generator cabinet. Wafers are loaded and unloaded by the glove box located in the reactor cabinet. Contamination is avoided by nitrogen filling in glove box. Wafers are transported into the glove box via the load lock chamber for loading/unloading.

The reactor pressure is maintained at 50 mbar, controlled by pump and throttle valve. Substrates are loaded on a rotated

susceptor in order to keep uniform temperature during the growth. 12 substrates of 2 or 4 in. can be loaded at once. The reactor is heated by an RF inductor.

The working pressures and gas flow rates are controlled by pressure controllers (PCs) and mass flow controller (MFCs), respectively. Trimethylgallium (TMGa, $(CH_3)_3Ga$), Trimethylindium (TMIn, $(CH_3)_3In$), and Trimethylaluminium (TMAl, $(CH_3)_3Al$) are used as group III precursors. Arsine (AsH_3) and Phosphine (PH_3) are used for sources for group V materials. *In-situ* is possible by using Diethylzinc (DEZn, $(C_2H_5)_2Zn$), Tetrabromomethane (CBr_4), Silane (SiH_4) and Diethyltelluride (DETe, $(C_2H_5)_2Te$).

2.3.1 Plasma-enhanced chemical vapor deposition (PECVD)

SiO_2 layers were deposited on Ge surfaces by 310PC of STS. The temperature of PECVD is maintained to 300 ^oC. Source gases used in experiments were SiH_4, N_2O and N_2. RF power was set to 60 watts with 187 kHz. The deposition rate of SiO_2 was 33.3 nm/min.

2.2 Preparation of substrates

The 6-inch Si(001) substrates were used for Ge growth. The orientations were (001) with 0 and 6 degree offcut toward <111>. The Ge substrates were p-type and resistivity was 1 – 10 ohm-cm.

The organic contaminants of Si substrates were cleaned by SPM cleaning with H_2SO_4:H_2O_2=4:1 solution at 120 ^oC for 10 min, followed by rinsing with deionized (DI) water. To remove

native oxide on the substrate and to passivate the surface dangling bonds with hydrogen, wafers were subsequently dipped into 10:1 HF solution diluted by DI water. Before being loaded into the load lock chamber, each wafer was dried by spin drier in hot nitrogen ambient without DI water rinse.

2.3 Post thermal treatment

Grown Ge layers were thermally annealed by rapid thermal annealing (RTA) with KVR-3006T. The main chamber is connected with dry pump backed by rotary pump and the base pressure is less than 10^{-2} torr. Main chamber consisted of heater and graphite susceptor. Four gases of N_2, O_2, H_2 and Ar are available as ambient gases. Flow rate of source gases and working pressure are controlled by mass flow controller (MFC) and throttle valve, respectively.

2.4 Analysis tools

2.4.1 High resolution X-ray diffractometry (HR-XRD)

Panalytical X'pert instrument was used for high resolution XRD measurement and ω-scan. The angle divergence of 12 arcsec or less can be obtained by 4 bounce Ge 022 channel cut monochromator.

2.4.2 Atomic force microscopy (AFM)

Non-contact AFM measurements were performed in using Park systems XE-100 in order to investigate surface morphology. The

Au-coated Si tips were used. For statistical analyses, XEI ver. 1.8.0 was used.

2.4.3 Transmission electron microscopy (TEM)

The TEM specimens were made by using focused ion beam (FIB). The cross-sectional and plan-view images of transmission electron microscopy (XTEM) were obtained by a JEOL JEM-2100F in Korea Advanced Nano Fab Center and JEOL JEM-3000F in Seoul National University. Bright field techniques were used to observe the threading dislocations..

2.4.4 Field emission scanning electron microscopy (FE-SEM)

FE-SEM analyses were performed by using a SU-70 of Hitachi, which incorporates a cold field emission electron source and provides 1 nm microscope resolution at 10 kV, magnification range of 30 - 800,000x.

2.4.5 Cathodoluminescence (CL)

The CL was measured by PMT detector with spectral range from 200 to 1800 nm. Panchromatic mode was used to obtain CL images and spectra.

2.4.6 Secondary ion mass spectrometry (SIMS)

The Ge content and the total B content were measured by a CAMECA IMS-6f Magnetic Sector SIMS with the first ion of O_2^+ and Cs^+.

2.4.7 Secco etching

Defects in Ge layers were etched for counting the etch pit density (EPD) using Secco etchant. Secco etchant contains 2 HF : 1 $K_2Cr_2O_7$ (0.15 M).[1, 2]

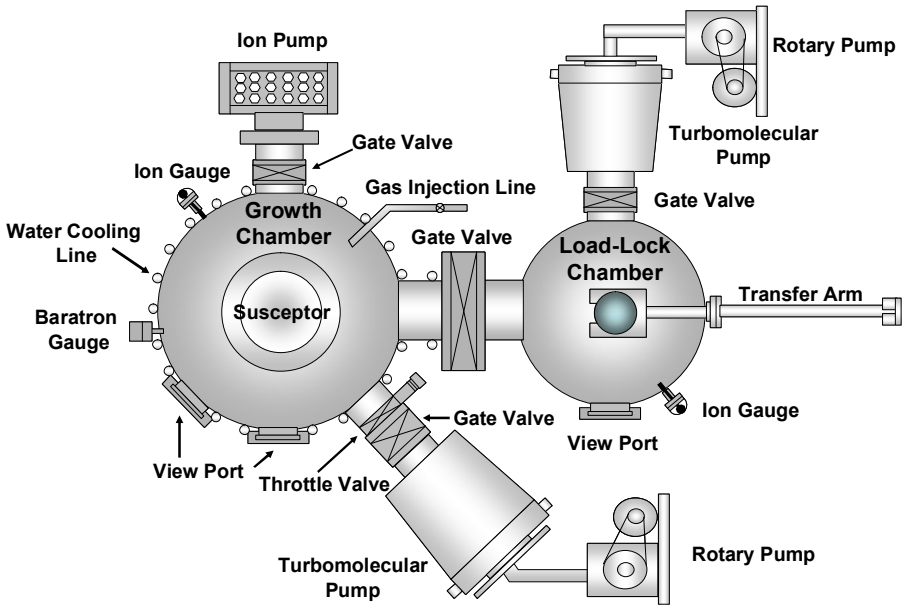

Fig. 2-1. Schematic image of the cold-wall type UHV-CVD system used in this experiment.

2.5 References

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Chapter 3. Two-step Ge growth on Si(001) substrates

3.1 Introduction

In this chapter, fully relaxed Ge layers were grown in UHV-CVD using two-step method for the MJSCs application.[1] I investigated the surface morphologies of Ge layers using AFM. The quality of Ge layer was studied by HR-XRD, EPD and TEM measurement.

3.2 Experimental procedures

All Ge layers were grown on B-doped Si(001) wafers (15 cm in diameter, resistivity = 1~10 Ω-cm) by cold wall type ultrahigh vacuum deposition (UHV-CVD) with a base pressure of 1 x 10^{-9} Torr. The growth proceeded in a two-step. 40 nm-thick Ge buffer layers were grown at 300 ^{o}C. Subsequently, Ge layers were grown at the raised growth temperature of 500 ^{o}C. Two Ge layers were prepared to anneal with the thicknesses of 250 and 940 nm. The process pressure was set to 17 mTorr. Source gases were introduced continuously during the temperature ramp.

The surface morphology and roughness of all samples were characterized by non-contact mode AFM in air. The degree of relaxation and the quality of Ge layers were determined by HR-XRD. Threading dislocation densities were measured by counting EPD using Secco etch method and SEM. Cross-sectional TEM

was performed to analyze defect in Ge layer.

3.3 Results and discussion

As mentioned Chap. 1.2.3, two-step growth is advantageous in Ge growth with flat surface. Kim *et al.* already reported that one-step Ge growth on Si(001) at high temperature range of 400 - 550 ^{o}C roughened Ge surface due to the strain relaxation via island formation.[2] Figure 3-1(a) shows the surface morphologies of low temperature (LT) Ge buffer layer grown on Si. By lowering growth temperature to 300 ^{o}C, formation of islands was successfully suppressed, leading to 2-dimmensional growth although thickness of Ge layer was 40 nm. LT growth is advantageous to obtain flat surface in that diffusion length of adatom is reduced at lower temperature and hydrogen acts as a surfactant at the temperature below 500 ^{o}C.[2, 3] When high temperature (HT) Ge layer is grown on flat, 2-dimensional LT Ge buffer layer, Ge is grown like homoepitaxy. Thus, by using two-step growth, flat Ge layers can be obtained with low RMS roughness of 1.32 nm as shown in Fig. 3-1(b).

In order to investigate the thickness effect on threading dislocation density (TDD), it was measured by counting EPD. Fig. 3-2(a) and (b) are the plan-view SEM images of 250 and 900 nm-thick Ge layers after Secco etching. TDD is reduced from 2.4 x 10^{9} to 4.3 x 10^{8} cm^{-2} by increasing thickness from 250 to 900 nm. Cross-sectional TEM in Fig. 3-2(c) shows that misfit dislocations are formed at the interface between Si and Ge. Near the interface, few threading dislocations are bent and confined in LT Ge buffer layer since point defects generated by LT growth inhibit the

propagation of threading dislocation.[1] Furthermore, as shown in Fig. 3-2(c), some propagated dislocations meet and are annihilated each other during the growth due to the interaction between two adjacent dislocations.[4] Therefore, as the thickness increases, TDD at top surface decreases. From the above results, it is noted that the reduced TDD in thicker layer is responsible for the improvement of crystal quality.

The structure and quality of two-step grown Ge layer were characterized by HR-XRD. Figure 3-3(a) is HR-XRD results of two-step grown Ge layers of 250 and 900 nm on Si. For both layers, peak positions of Ge layers are positioned at -5513 arc-sec from Si peak position. The peak intensity increased with thickness increasing. Figure 3-3(b) shows the HRXRD rocking curves of same samples. As shown in Fig. 3-3(b), full width at half maximum (FWHM) of Ge layer is reduced from 593 to 202 arc-sec by increasing thickness from 250 to 900 nm. In HR-XRD, the higher intensity and the narrower FWHM mean the better crystal quality, inferring that crystal quality of Ge layer is improved by growing thicker layer.

The threading dislocations in Ge layer affect the device performance. Ishikawa *et al.* reported that lower leakage current in Ge photodiode was obtained by using TDD reduced Ge layer.[5] In multi-junction solar cells fabricated on Si substrates, TDD on the order of 10^8 cm^{-2} resulted in the V_{oc} drop in I-V characteristics.[6] Therefore, TDD in Ge layer should be more lowered for the fabrication of devices with better performance.

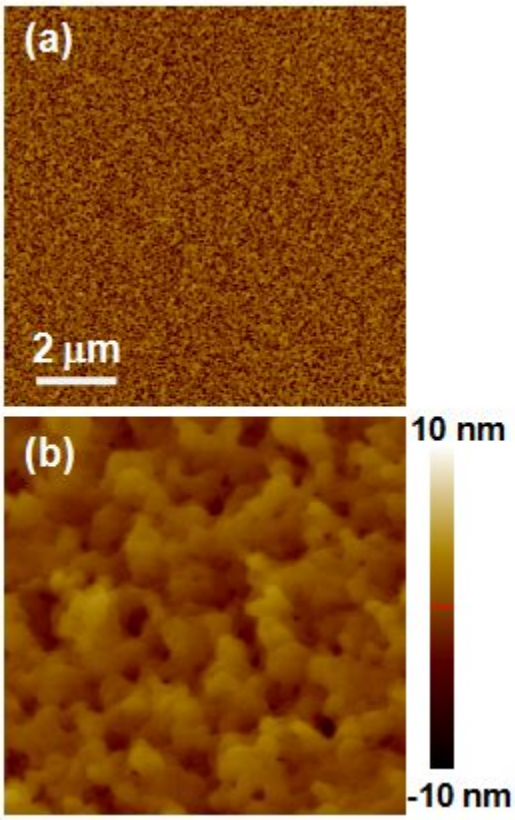

Fig. 3-1. 10 x 10 μm^2 AFM images of (a) LT Ge buffer layer and (b) two-step grown Ge layer on Si(001) substrates. RMS roughnesses are 2.06 and 1.32 nm, respectively.

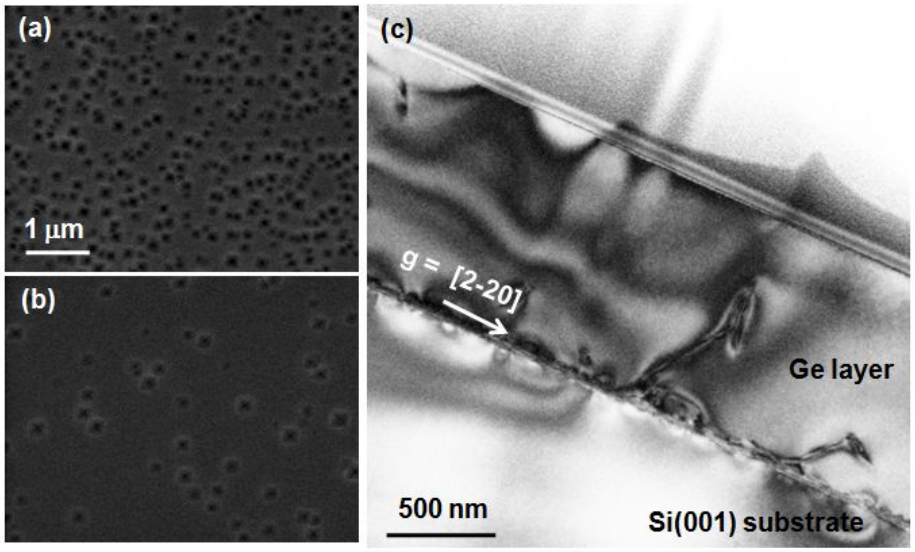

Fig. 3-2. Plan-view SEM images of Ge layers of (a) 250 and (b) 900 nm after Secco etching. (c) Cross-sectional TEM image of Ge layer of 900 nm.

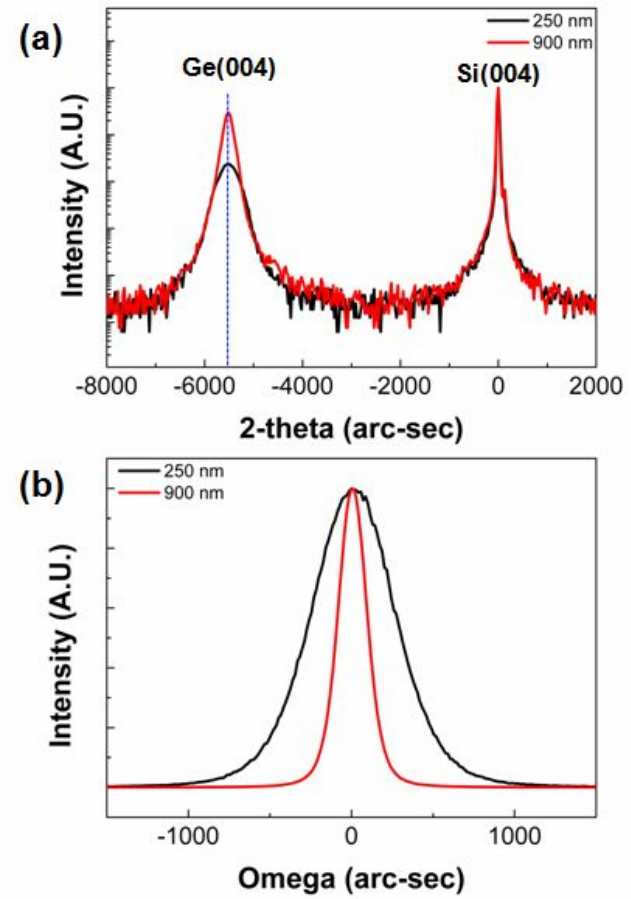

Fig. 3-3. HR-XRD (a) ω-2θ and (b) rocking curves of (004) peak of Ge two-step grown Ge layers on Si(001) substrates.

3.4 Summary

In summary, Ge layers were grown on Si(001) substrates using UHV-CVD. By using two-step method, pure Ge layers with flat surfaces were successfully grown on Si with low RMS roughness of 1.3 nm. When thickness of Ge layer increases, TDD is reduced and TDD of 4.3 x 10^8 cm^{-2} was obtained when 900 nm-thick Ge layer was grown. The reduced TDD with thicker Ge layer leaded to the improvement of crystal quality. However, more TDD reduction is required to adapt Ge layers on Si to devices.

3.5 References

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Chapter 4. Post RTA of Ge grown on Si(001)

4.1 Post RTA of Ge grown on nominal Si(001)

4.1.1 Introduction

There have been many efforts to reduce TDD in heteroepitaxial layers. Most were focused on the usage of strained-layer superlattice and/or graded buffer layers.[1,2,3] Another way to reduce TDD is post thermal treatment without excess source consumption. The mobility of dislocation is raised at the high annealing temperature, resulting in the annihilation of dislocations. Two decades ago, studies of post thermal annealing were reported by many groups in the cases of the III-V on Si.[4,5,6] They reported that TDD of III-V layers were reduced from 10^9 to 10^7 cm^{-2} order and crystal quality of III-V layers were improved by post annealing. The effects of post annealing on Ge layer on Si were also investigated.[7,8,9,10] Luan *et al.* suggested the cyclic thermal annealing and reduced TDD from 9.5 x 10^8 to 2.3 x 10^7 cm^{-2} by using 10-cycle annealing.[7] Nayfeh *et al.* reported that hydrogen annealing was also effective in improvement of surface roughness in terms of Ge-H cluster formation.[9] Choi *et al.* proposed the cyclic deposition-annealing processes. They showed that AFM pit density was reduced from 1.3 x 10^8 to 2-6 x 10^6 cm^{-2} by using 4-cycle deposition-annealing.[10] Those post annealing processes were generally performed in growth chamber or conventional furnace annealing.

However, conventional annealing is not desirable because the

annealing time longer than 30 min at high temperature allows Ge and Si to intermix at the hetero-interface.[8] Such problem should be avoided.

The potential advantage of RTA over conventional furnace annealing is the short annealing time which is generally few sec. RTA has been used for the activation of dopants and formation of silicide or germanide.[11,12,13,14] In addition to those applications, RTA can be used for TDD reduction. Sun *et al.* reported that they performed RTA of Ge epitaxial layer on Si for dopant activation and defect reduction.[15] However, the effects of RTA on TDD reduction of Ge layers on Si has been almost never reported until now. I thought that RTA could be another choice to lower TDD in Ge layer grown on Si with reduced annealing time.

Therefore, I did post annealing of Ge layers grown on Si(001) substrates using RTA and characterized the effects of RTA conditions on surface morphologies, structure and defect reduction of Ge layers.

4.1.2 Experimental details

All Ge layers were grown on B-doped Si(001) wafers (15 cm in diameter, resistivity = 1~10 Ω-cm) by UHV-CVD. The growth condition can be found in Chap. 3.2. 200 nm-thick SiO_2 capping layers were deposited on Ge surfaces by plasma enhanced chemical vapor deposition (PECVD) before RTA. Post annealing was performed using rapid thermal annealing (RTA) under N_2 ambient. Annealing temperature was varied from 650 to 850 ^oC,

fixing time at 30 and 90 sec and the ramping rate was 80 ^{o}C/sec. Working pressure was set to 3.5 mtorr. Cyclic RTA was progressed at 800 ^{o}C for 30 sec per each cycle. Cycle was varied from 1 to 20. SiO_2 layers were then removed after RTA using HF.

The surface morphology and roughness of all samples were characterized by non-contact mode atomic force microscopy (AFM) in air. The structure and the quality of Ge layers were determined by high-resolution X-ray diffraction (HR-XRD). Threading dislocation densities were measured by plan-view transmission electron microscopy (TEM) and by counting the etch pit density (EPD) using Secco etch method with scanning electron microscopy (SEM).

4.1.3 Results and discussions

The surface morphologies of Ge layers after RTA were observed by AFM and SEM. In order to investigate the effect of SiO_2 as a capping layer, Ge layers with and without 200 nm-thick SiO_2 layers were used. RTA was performed for 30 sec, varying the annealing temperature from 650 to 850 ^{o}C. Figure 4-1(a) is the 10 x 10 μm^2 AFM image of as grown Ge layer on Si and Fig. 4-1(b)-(f) show surface morphologies of Ge layers without SiO_2 layers after RTA at 650-850 ^{o}C for 30 sec. As-grown Ge layer has flat surface with low RMS roughness of 1.75 nm. After RTA, pits are formed when annealed at 650-800 ^{o}C. In this RTA temperature range, surfaces are roughened due to the pit formation, leading to higher RMS roughness of 5-11 nm. The density and size of pits were plotted as a function of RTA temperature as presented in Fig. 4-1(g). As the RTA temperature increases, density of pit decreases

from 7.2 to 0.43 x 10^8 cm^{-2} and their lateral size and depth tend to increase from 225 to 479 nm and 44 to 71 nm, respectively. The pits are originated from the thermal defect etching or damage by thermal radiation. The defect reduction at higher temperature RTA might be responsible for the decrease of pit density. When Ge layer is annealed at 850 ^oC, very rough surface is obtained with high RMS roughness of 70 nm as shown in Fig. 4-1(f). The inset of Fig. 4-1(f) is the bird's eye view SEM image of corresponding sample. The inset image shows that Ge layer became thinner, indicating that sublimation occurred actively during annealing. Because the melting temperature of Ge is around 938 ^oC, Ge is easily sublimated at 850 ^oC and non-uniform sublimation results in the rough surface. Above results confirm that the RTA at high temperature damages Ge layer.

To avoid damage by RTA, 200 nm-thick SiO_2 layers were deposited on Ge surfaces before RTA. Figure 4-2(b)-(f) is the 10 x 10 μm^2 AFM images of Ge layers with SiO_2 after RTA. In these cases, SiO_2 layers were removed by HF after RTA. As shown in Fig. 4-2(b)-(f), flat surfaces can be maintained without hole formation after RTA by depositing SiO_2 layers on Ge surfaces. RMS roughnesses of all RTA samples are around 1.66-1.91 nm which is similar to that of as-grown sample (Fig. 4-2(a)). Although relatively flat surface can be obtained with slightly higher RMS roughness of 4.33 nm by RTA at 850 ^oC with SiO_2 layers in Fig. 4-2(f), inset image shows that large holes are formed with the diameter of 20 μm and such hole is formed from the interface between Ge and Si.

Figure 4-2(g) is the RMS roughness of Ge layers after RTA

with and without SiO_2 layers as a function of RTA temperature. The increase of RMS roughness can be suppressed by depositing SiO_2 layer at 650-800 ^oC. Because SiO_2 has the higher melting temperature of 1600 ^oC than that of Ge (938 ^oC), damage by RTA can be prevented by the action of SiO_2 as a capping layer at RTA temperature range from 650 to 800 ^oC. However, both Ge layers with and without SiO_2 are roughened with high RMS roughness by RTA at 850 ^oC due to the sublimation.

The HR-XRD analysis was performed to investigate the effects of RTA temperature on structure and quality of the Ge layers. Figure 4-3(a) shows the HR-XRD theta-2theta curve of (004) Bragg peaks Ge layers with SiO_2 capping layer after RTA for 30 sec. In Fig. 4-3(a), the peak positions of as-grown Ge layers appear at the position about -5516 arc-sec, compared to the Si substrate peaks. When Ge layers are annealed at the temperature from 650 to 800 ^oC using RTA, no diffuse shoulder peaks are observed which means no SiGe alloys were formed at the interface. However, peaks were broadened and their intensities were reduced after RTA at 850 ^oC. Shoulder peaks are observed at the SiGe peak position and the peak position is shifted by 300 arc-sec, implying the SiGe alloy formation in the Ge layer during RTA at 850 ^oC. The Si-Ge alloying is mainly attributed to the appearance of Si surface during RTA as shown in inset of Fig. 4-2(f) since the surface diffusion and intermixing between Si and Ge are dominant at high temperature.

RTA temperature influences the quality of Ge layers. Figure 4-3(b) is the HR-XRD rocking curve of Ge layers annealed by RTA for 30 sec at the temperature of 650-850 ^oC. When Ge layers are

annealed at 650-800 ^{o}C using RTA, narrower curves are obtained compared to as-grown Ge layer. In addition, as the RTA temperature increases from 650 to 800 ^{o}C, the FWHM decreases from 197.6 to 170.7 arc-sec. In HR-XRD rocking curve, the FWHM indicates the crystal quality. Thus, crystal quality of Ge layer is improved by RTA and the higher temperature is desirable for the better quality. However, rocking curve is broadened with the higher FWHM of 293.2 arc-sec after RTA at 850 ^{o}C, meaning that crystal quality is worsened. From the AFM and HR-XRD results, we note that capping layer is required to maintain flat surface after RTA but there exists temperature limitation to anneal Ge layer at which SiO_2 plays a role as a capping layer.

In order to investigate the effects of RTA temperature on TDD reduction in Ge layers, the TDDs were measured by counting the pits formed from the chemical etching with SEM. The Ge samples with flat surfaces were analyzed which were annealed at 650-800 ^{o}C. Figure 4-4(a) is the plot of the TDD of Ge layers on Si as a function of RTA temperature from 650 to 800 ^{o}C. RTA time was fixed at 30 sec. The TDD of as-grown Ge layer is 4.29 x 10^{8} cm^{-2}. As shown in Fig. 4-4(a), TDD of Ge layer is reduced by RTA. As the RTA temperature increases from 650 to 800 ^{o}C, less TDD is obtained and the TDD is lowest at the value of 2.24 x 10^{8} cm^{-2} when annealed at 800 ^{o}C. During thermal annealing at high temperature, dislocations annihilate each other by gliding and interaction. The dislocation velocity at any temperatures can be explained by equation of temperature and stress. Tamaguchi *et al.* reported that dislocation velocity increases as both temperature and stress increase.[16] The Ge layer grown on Si is under tensile stress at room temperature due to the difference of thermal

expansion coefficient between Ge and Si.[17] In my experiment, Ge layers were grown at 500 ^{o}C and the RTA temperature was higher than growth temperature. Therefore, compressive stress is induced into Ge layer during RTA. The stress within Ge layer during RTA was calculated by using Stoney's equation.[18] Stoney's equation is demonstrated as follows:

$$\sigma_{th} = \left[\frac{E_{Ge}}{1-\nu_{Ge}}\right](\alpha_{Si} - \alpha_{Ge})(T_L - T_I) = \left[\frac{E_{Si}}{1-\nu_{si}}\right]\frac{t_{Si}^{\ 2}}{6t_{Ge}R} \qquad (1)[18]$$

where ν_{Si} and ν_{Ge} are Possion's ratios, E_{Si} and E_{Ge} are Young's modulus and α_{Si} and α_{Ge} are thermal expansion coefficients of Si and Ge, respectively. t_{Si} and t_{Ge} are thickness of Si substrate and Ge layer and R is the radius of curvature. In this case, T_L is RTA temperature and T_I is growth temperature. Because the E and α are the function of temperature, equation expressed below was used with the elastic constants included in Table 4-1[19]:

$$\sigma_{th} = \int_{T_I}^{T_L} \frac{E(T)_{Ge}}{1-\nu_{Ge}}(\alpha(T)_{Si} - \alpha(T)_{Ge})dT \qquad (2)[18]$$

The resulting stress calculated by Stoney's equation is plotted in Fig. 4-4(b). Figure 4-4(b) shows that the compressive stress within Ge increases from 61.3 to 121.1 MPa, leading to dislocation velocity increment as the temperature increases from 650 to 800 ^{o}C. Higher RTA temperature with more stress admits

dislocations to more easily glide and annihilate. Thus, less TDD can be obtained with increasing RTA temperature. However, TDD is still on the order of 10^8 cm^{-2} after RTA and should be more lowered in order to apply Ge layer on devices.

For further TDD reduction, RTA was performed at 800 ^oC varying time and the number of cycle. Figure 4-5(a) is the plot of TDD of Ge layers depending on time and the number of cycle of RTA. While the TDD is barely changed with RTA time increasing from 30 to 90 sec, 3 times RTA results in the more reduction of TDD, meaning that the increasing cycle is more effective for the TDD reduction rather than increasing time. Furthermore, TDD tends to be reduced as the cycle of RTA increases and is minimized to 3.5 x 10^7 cm^{-2} by 20 times RTA. Other studies about thermal annealing also showed similar results that more cycle was more effective in TDD reduction than one cycle with longer annealing time.[7, 20] In cyclic annealing, repetitive tensile and compressive stresses are responsible for the TD movement which are induced into Ge layer due to thermal expansion and contraction. The heating, annealing and cooling time of RTA are relatively short compared to other annealing equipments. Thus, TDD of 3.5 x 10^7 cm^{-2} could be achieved by cyclic RTA with reduced process time.

In Fig. 4-5(a), it is also observed that TDD seems to be saturated with cycle increasing to 20. Figure 4-5(b) shows that the average separation between two closest dislocations is getting longer from 0.48 to 1.69 μm by TDD reduction from 4.29 to 0.35 x 10^8 cm^{-2}. When separation between dislocations increases, the interaction energy logarithmically decreases.[21] The lower

interaction energy make it harder for TD to overcome energy barrier. Therefore, the effect of RTA on TDD reduction is lowered as the cycle of RTA increases.

I also annealed 250 nm-thick Ge layers with TDD of 2.4 x 10^9 cm^{-2} by RTA at 800 ^oC varying the cycles and the results are represented in Fig. 4-5(c). The TDD is also reduced as the cycle of RTA increases, similar to RTA results of 900 nm-thick Ge layer. In this case, TDD was still on the order of 10^9 cm^{-2} after 5 times RTA. This result implies that in order for RTA to be more effective, the TDD in as-grown Ge layer should be lowered, since RTA does not have infinite capacity in reducing threading dislocations.

Finally, I studied the compatibility of EPD with TDD by comparing EPD results with plan-view TEM results. Two samples were used: as-grown and 20 times RTA annealed Ge layer grown on Si. For two samples, Secco etching time was set to 30 sec. Figure 4-6(a) and (b) shows the plan-view SEM images of (a) as-grown and (b) 20 times RTA annealed Ge layers after Secco etching and (c) and (d) are corresponding plan-view TEM images of (a) and (b) without Secco etching, respectively. Figure 4-6(e) shows that TDD measured by EPD is slightly lower than that from TEM results for the as-grown Ge layer which is on the order of 10^8 cm^{-2}. The difference between two methods might be originated from the coalescence of some pits during Secco etching. However, EPD result well agrees with TEM result when TDD is on the order of 10^7 cm^{-2}. Those results infer that etching time should be adjusted according to the TDD.

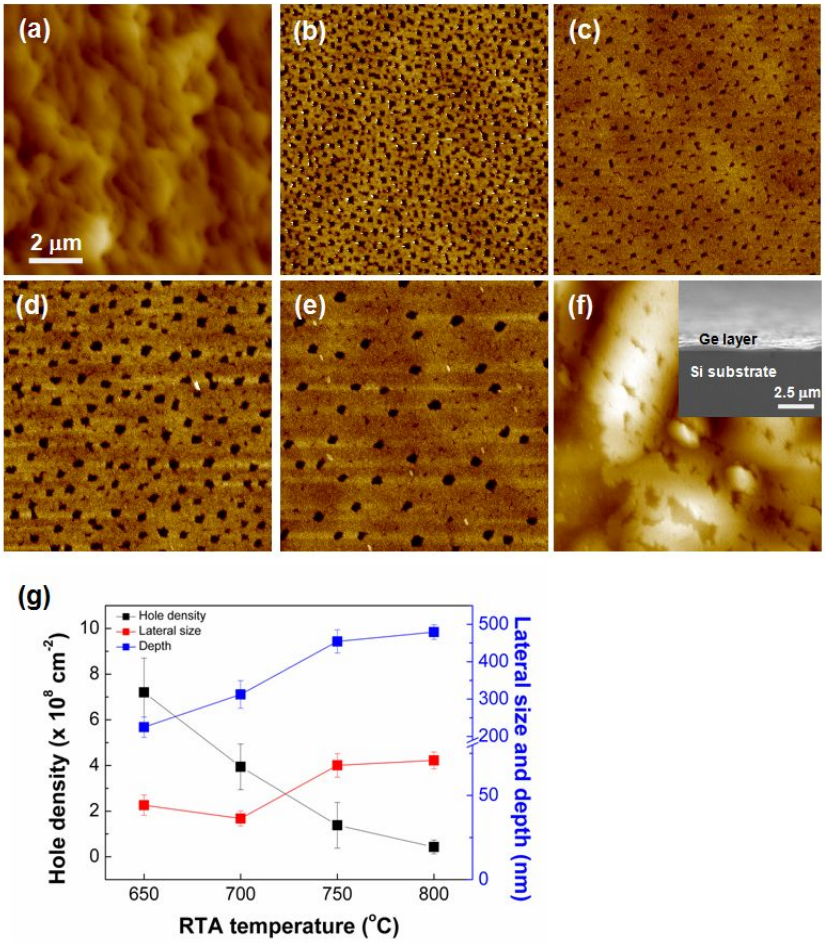

Fig. 4-1 (a)-(f) 10 x 10 μm^2 AFM images of Ge layers grown on Si substrates. (a) As-grown Ge layer. Ge layer after RTA without SiO_2 at (b) 650, (c) 700, (d) 750, (e) 800 and (f) 850 ^oC for 30 sec. The insects of (f) shows bird's eye view SEM images of corresponding samples. The RMS roughnesses are 1.75, 11.12, 5.69, 10.72, 8.77 and 69.75 nm, respectively. (g) The plot of size and density of Ge layers after RTA as a RTA temperature.

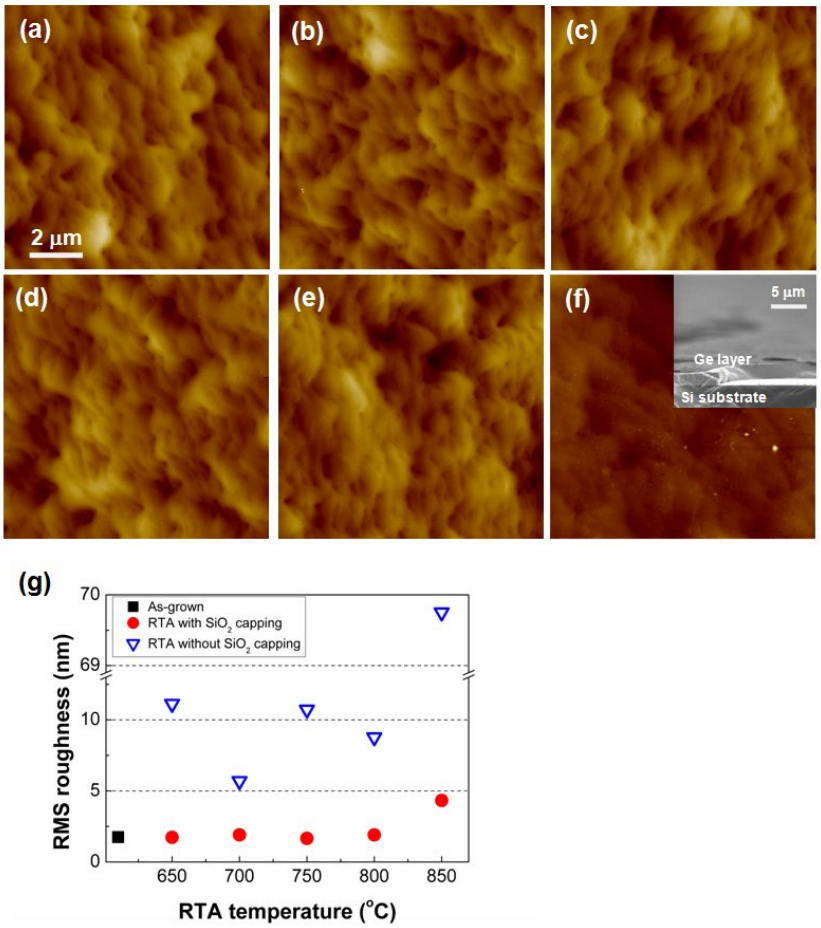

Fig. 4-2 (a)-(f) 10 x 10 μm^2 AFM images of Ge layers grown on Si substrates. (a) As-grown Ge layer. Ge layer after RTA with SiO_2 at (b) 650, (c) 700, (d) 750, (e) 800 and (f) 850 ^oC for 30 sec. The insects of (f) shows bird's eye view SEM images of corresponding samples. The RMS roughnesses are 1.75, 1.73, 1.91, 1.66, 1.91 and 4.33 nm, respectively. (e) The plot of the RMS roughness of Ge layers with and without SiO_2 capping layers depending on the RTA temperature.

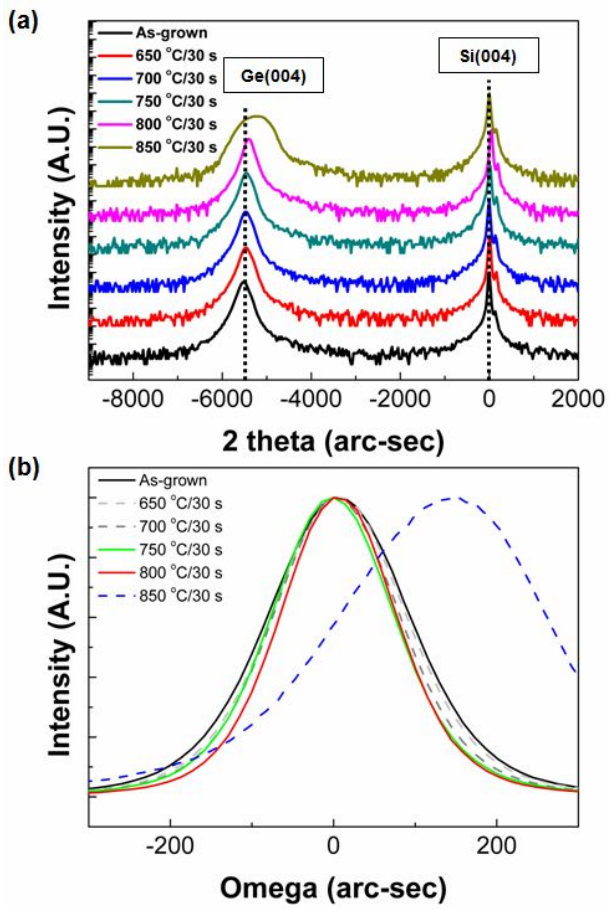

Fig. 4-3. HR-XRD (a) ω-2 θ and (b) rocking curves of symmetric (004) Bragg peaks from the Ge layers using on Si substrates after RTA for 30 sec. The RTA temperatures are varied from 650 to 850 ^{o}C.

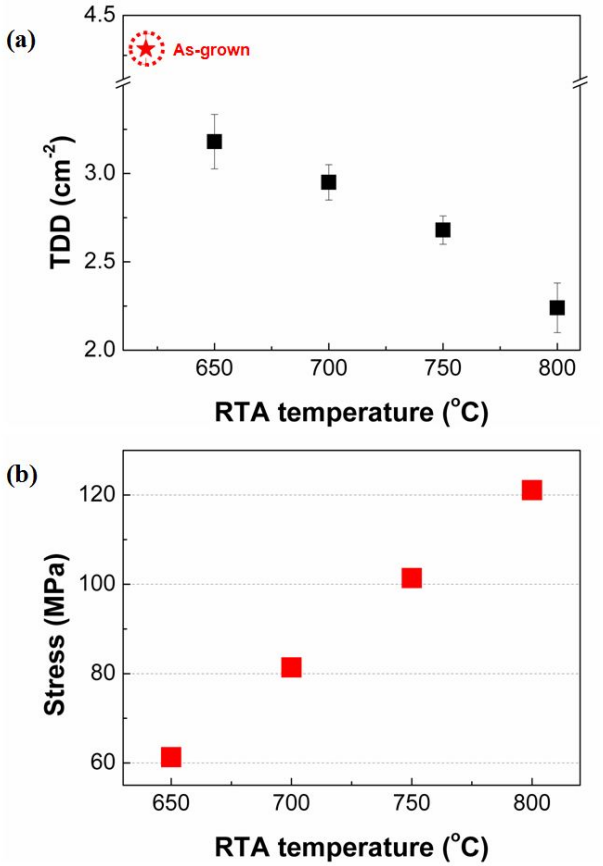

Fig. 4-4. (a) The plot of TDD of Ge layers after RTA for 30 sec as a function of RTA temperature. (b) Plot of stress in Ge calculated by Stoney equation during RTA with temperature.[17]

Table 4-1 Elastic constants of Si and Ge.[18]

	Young's modulus (GPa)	Possion's ratio	Thermal expansion coefficient (10^{-6}/K)
Si	130.2	0.277	2.7 + 0.0026T
Ge	102.1	0.273	5.9 + 0.0021T

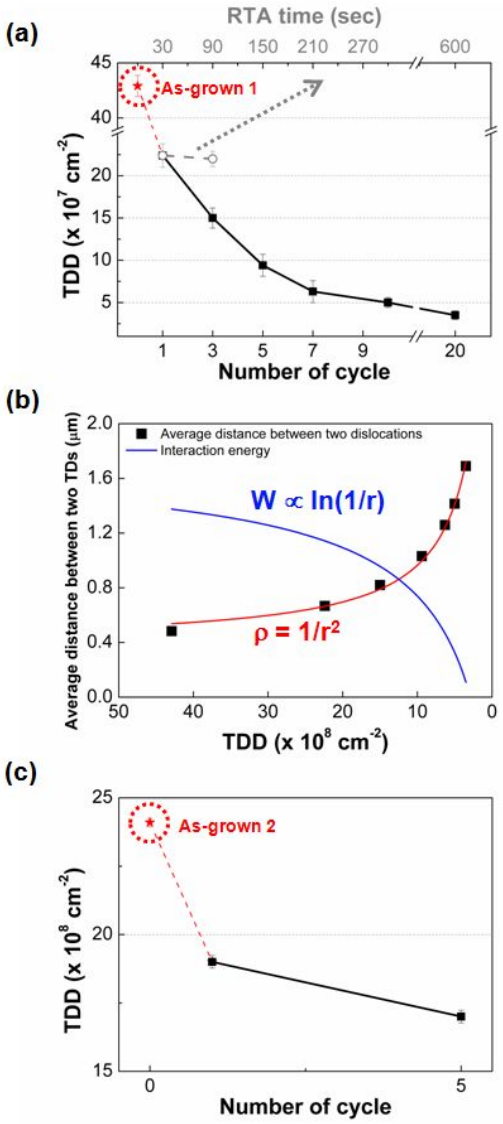

Fig. 4-5. Changes in TDD of (a) 900 and (c) 250 nm-thick Ge layers with the number of cycle and time of RTA, where the process time per each cycle is 30 sec. (b) Plot of average distance and interaction energy between two neighbor TDs as a function of TDD.[21]

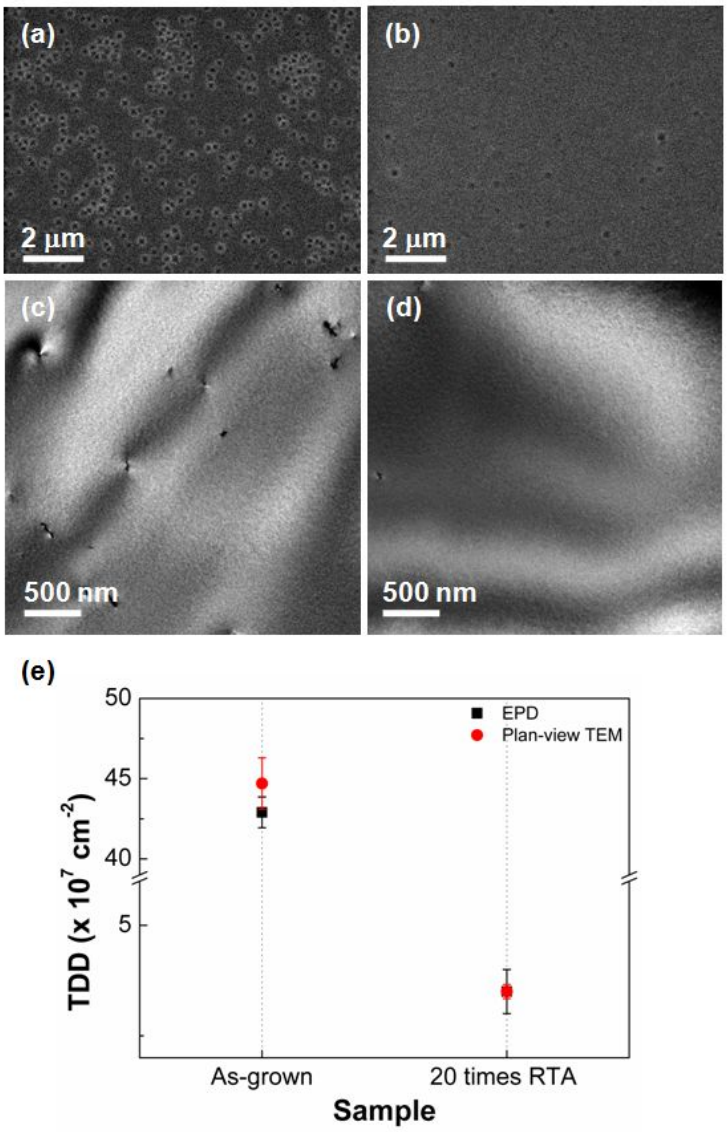

Fig. 4-6. EPD results of (a) as-grown and (b) 20 times RTA annealed Ge layers. (c) and (d) are plan-view TEM images corresponding to (a) and (b), respectively. (e) TDD of as-grown and 20 times RTA annealed Ge layers measured by EPD and plan-view TEM.

4.2 Post RTA of Ge grown on vicinal Si(001)

4.2.1 Introduction

III-V growth on Si has been widely studies due to the merit of cost, compatibility with Si based technologies. Ge has a similar lattice constant with GaAs or $Ga_{0.45}In_{0.55}P$, Ge and native GeO_x is more easily desorbed at lower temperature than that of SiO_2.[22,23,24,25] Thus, Ge is one of the promising buffer layer for III-V growth on Si. However, when III-V material is epitaxially grown on a group IV substrate, besides threading dislocation, stacking fault and twin boundary, another defect is generated from the III-V/IV interface although they have similar lattice constant. We called it anti-phase boundary (APB) and the formation of APBs is illustrated in Fig. 4-7(a).[26,29] APB is known to be originated from the surface steps of group IV substrate. The Ge and Si have a number of dangling bonds on (001) surface and they are reconstructed to reduce surface energy. Generally, (2 x 1) and (1 x 2) reconstructions are yielded as shown in Fig. 4-8 which are rotated 90^o. At that time, four-type steps exist on the surface named S_A, S_B, D_A and D_B.[27] When III-V material is grown on group IV surface, V-V and III-III bonds are formed from the surface due to the single layer step in Fig. 4-7(a). The APBs lack the charge neutrality in III-V layer and acts as a non-radiative recombination center so that they worsen the materials properties of grown III-V materials as shown in Fig. 4-8.[26] Furthermore, III-V growth with APBs roughened surfaces as shown in inset of Fig. 4-7(a). In order to avoid APB, III-V material should be grown on surfaces with double steps shown in Fig. 4-7(b). D_B type double steps are easily formed by the reaction between S_A and S_B step by thermal

treatment because D_B is energetically more favorable than S_A and S_B.[27] However, after the thermal treatment, single steps still exist on the surface.[30] The one of the solutions is the usage of vicinal (001) substrates. It is known that high index surface has double steps with high density and they can be increased by thermal annealing.[30,31] Therefore, III-V can be grown on group IV without APB by using vicinal (001) substrates with offcut angle of 4 or 6^o.[26] Figure 4-7(b) and 4-9(b) shows that APB formation is suppressed by growing on vicinal substrate, improving the surface and optical properties of III-V layers.[28]

When Ge layer is grown on vicinal Si(001) as a buffer layer for III-V growth, the quality of Ge layer is crucial. Since the threading dislocations existed on a Ge surface propagate to the III-V surface, TDD in Ge layer determines the TDD and thus quality of III-V layer. Therefore, TDD in Ge layer grown on Si should be lowered to obtain III-V layer with low TDD.

In this study, I grew Ge layers on vicinal Si(001) substrates in a two-step. Then, Ge layers were thermally annealed by cyclic RTA. By comparing nominal Si(001) with vicinal Si(001), the effect of substrate orientation on TDD reduction by RTA was investigated. In order to define the effects of surface orientations on dislocation generation, TEM analyses were performed. Finally, GaAs layers were grown on as-grown and RTA annealed Ge/Si and their qualities were analyzed.

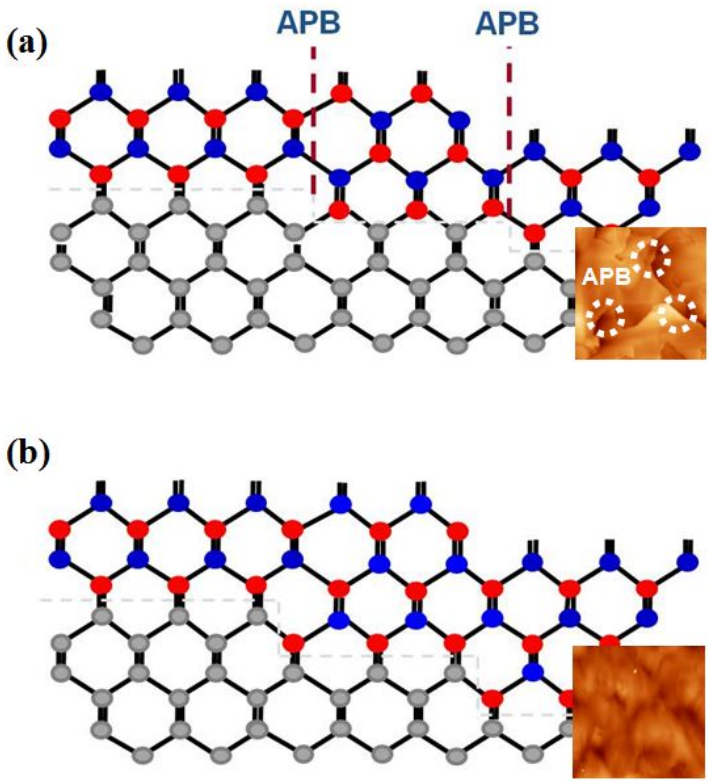

Fig. 4-7. Schematic illustrations of polar materials growth on (a) nominal and (b) vicinal non-polar substrates.[26] The insets are 10 x 10 μm^2 AFM images of InP grown on (a) nominal and (b) vicinal Si(001) substrates.[29]

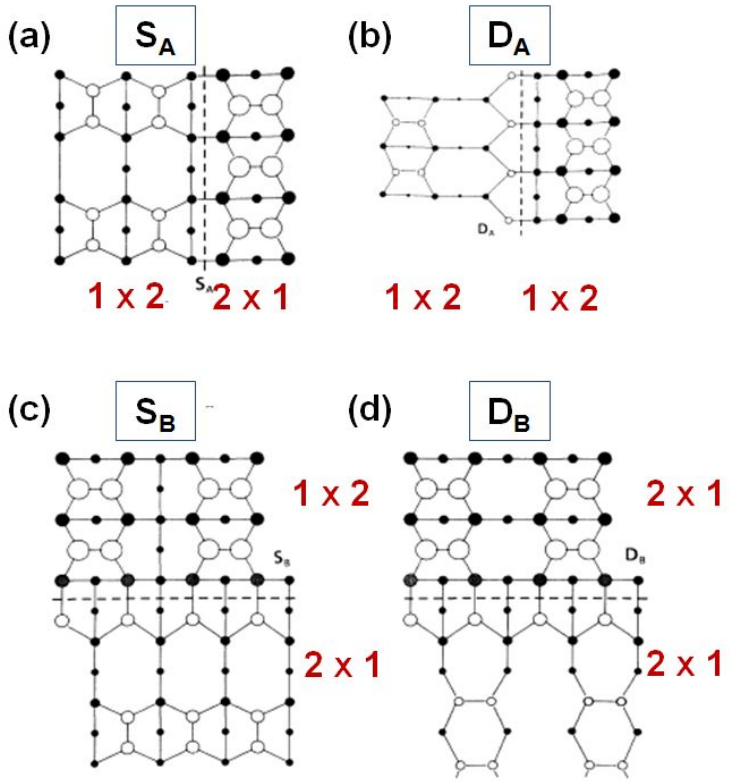

Fig. 4-8 Schematic plan view of (a) type A single, (b) type A double, (c) type B single and (d) type B double steps.[27]

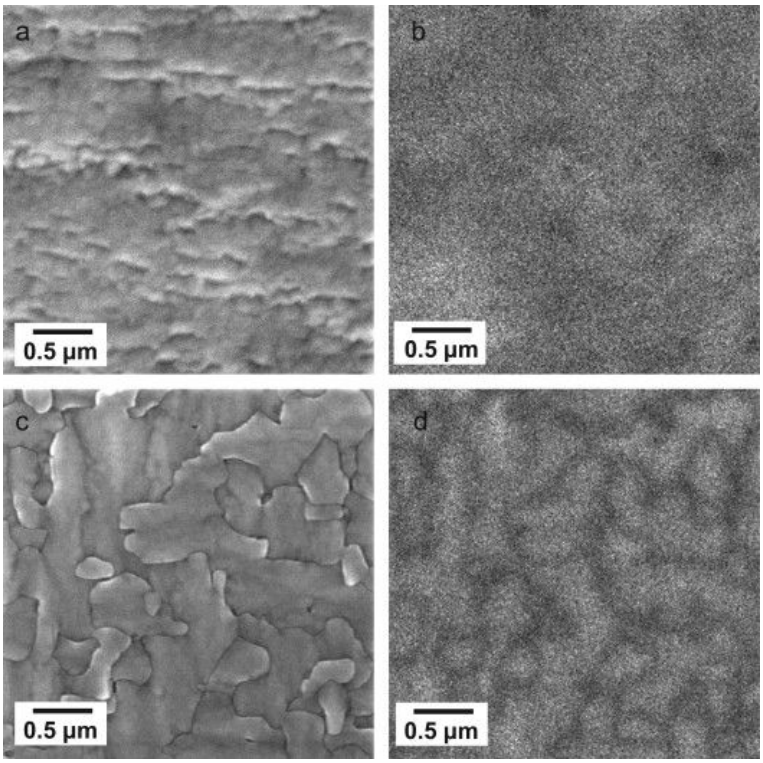

Fig. 4-9. Plan-view SEM images of GaInP grown on (a) nominal and (c) vicinal Ge/Si(001) substrates. (b), (d) CL images of corresponding regions of (a) and (c), respectively.[28]

4.1.2Experimental details

All Ge layers were grown on B-doped vicinal Si(001) wafers (15 cm in diameter, resistivity = 1~10 Ω-cm) by UHV-CVD. The Si(001) wafers 6^{o} offcut toward <111> were used. The growth proceeded in a two-step. 60 nm-thick Ge buffer layers were grown at 300 ^{o}C. Subsequently, Ge layers were grown at the raised growth temperature of 500 ^{o}C. The total thickness of Ge layer was set to 1.2 μm. The process pressure was fixed at 17 mTorr. Source gases were introduced continuously during the temperature ramp. The Ge layers grown on nominal Si(001) were used for the comparison.

200 nm-thick SiO_2 capping layers were deposited on Ge surfaces by plasma enhanced chemical vapor deposition (PECVD) before RTA. 10 times cyclic RTA was performed at 800 ^{o}C for 30 sec per each cycle under N_2 ambient. SiO_2 layers were then removed after RTA. The different growth conditions for sample A, B, C and D are summarized in Table 4-2.

GaAs layers were grown on vicinal Ge/Si substrates in metalorganic chemical vapor deposition (MOCVD). As-grown and 10 times RTA annealed Ge/Si substrates were used for GaAs growth. After sample loading into MOCVD reactor, they were thermally cleaned at 730 ^{o}C for 5 min. Then, 1 μm-thick GaAs layers were grown at 670 ^{o}C. V/III ratio was set to 68 during growth.

TDDs in Ge layers were measured by counting EPD using Secco etch method and AFM. The defects were also analyzed by

TEM. AFM was used to study the surface morphologies of Ge and GaAs layers. The crystal qualities of GaAs layers were characterized by XRD and CL.

Table 4-2 Description of sample A, B, C and D.

	Substrate	Thickness (nm)	Post thermal treatment
A	(001)	900	No
B	(001)	900	20 times RTA
C	(001) 6^{o} offcut toward <111>	1200	No
D	(001) 6^{o} offcut toward <111>	1200	10 times RTA

4.2.3 Results and discussions

In order to investigate the effects of RTA on the TDD reduction of Ge layers grown on vicinal Si(001) substrates, 10 times RTA was performed. Figure 4 show the 10 x 10 μm^2 AFM images of (a) as-grown and (b) 10 times RTA Ge layers grown on vicinal Si(001) substrates after Secco etching. Figure 4 reveals that (a) the TDD of as-grown Ge layer was 3.36 x 10^8 cm^{-2} and (b) TDD was reduced to 1.96 x 10^8 cm^{-2} by 10 times RTA. The TDD reduction ratio by 10 times RTA decreased from 88.3 to 41.7% by replacing nominal Si(001) substrate with vicinal one.

Threading dislocations glide under shear stresses and the change of surface orientation affects the status of shear stress in Ge layer. Thus, shear stresses for various slip systems in both Ge on nominal and vicinal substrates were considered. Table 4-3 show the shear stresses induced to Ge layer grown on both nominal and vicinal Si(001) substrate for various slip systems. In order to calculate the shear stress, loading axes were assumed to (001) and (2 2 27) for nominal and vicinal Si(001), respectively. As shown in table 4-3, there are little changes in shear stress for most slip systems. For four slip systems, vicinal substrate shows larger shear stress compared to nominal one, but there are slip systems in which smaller shear stress is induced to vicinal substrate. In addition, the differences in shear stresses are not that large for both orientations. Therefore, I thought that change of shear stress was not the main reason why cyclic RTA less affects on TDD reduction for the Ge layer grown on vicinal Si(001) substrate.

Next, I thought that the there might be difference in type of dislocations for both Ge layers grown on nominal and vicinal Si(001) substrates that influenced the glide of dislocation. TEM g · b analyses were performed to identify the threading dislocations of Ge layers. Figure 4-11 shows the cross sectional TEM images of Ge layers grown on (a), (b) nominal Si(00) and (c), (d) vicinal Si(001) substrates, respectively. The g vectors were set to (a), (c) [2-20] and (b), (d) [00-4], respectively. In the case of the Ge layers grown on nominal Si(001), no invisible dislocations are observed for both g vectors. However, Fig. 4-11(d) shows that some dislocations are disappeared when g = [00-4] for the Ge layer grown on vicinal Si(001). Same dislocations disappeared are marked with arrows in Fig 4-11(c) and Fig. 4-11(d). The invisible criterion at g = [00-4] confirms that disappeared dislocations have b = ± a/2[110] and those dislocations exists in the Ge layer grown on vicinal Si(001). The cross sectional TEM images of Ge layers after 10 times RTA are presented in Fig. 4-12. For both RTA annealed Ge layers, dislocations are not found in TEM images from the two reasons: First, the cross sectional TEM shows only small area of sample. Second, TDD decreased by RTA. Thus, chance to contain dislocation in cross sectional TEM sample is reduced for the lower TDD Ge layer.

In Ge layer, edge dislocation has b = ± a/2<110> and burger's vectors of mixed dislocation are b = ± a/2<011> and b = ± a/2<101>.[32] Edge dislocations with b = ± a/2<110> are on the (001) plane parallel to the Ge/Si interface. Because they are not on the slip planes, edge dislocations are immobile. It is known that edge dislocations are generally formed from surface step not from terrace. The vicinal Si(001) substrate has higher step density

than that of nominal Si(001) substrate so that more edge dislocations are generated on vicinal Si(001).[32] Furthermore, edge dislocations can be formed by reaction between two mixed dislocations. Such edge dislocations are not affected to the stress field.[32] Therefore, dislocation annihilation via glide is more difficult in the Ge layers grown on vicinal Si(001) with more edge dislocations, resulting in the higher TDD on the order of 10^8 cm^{-2} in spite of 10 times RTA in comparison with Ge layer grown on nominal Si(001).

Finally, GaAs layers of 1 μm were grown by MOCVD on two Ge layers grown on vicinal Si(001): As-grown and 10 times RTA annealed Ge layers. Figure 4-13 shows the AFM images of (a) as-grown and (b) 10 times RTA annealed Ge layers grown on vicinal Si(001). Figure 4-13(c) and (d) represent the surface morphologies of GaAs layers grown on (a) and (b), respectively. Cross-hatch patterns are shown and hole density of Ge layer was reduced after 10 times RTA, leading to the decrease of RMS roughness from 1.88 to 1.55 nm in Fig. 4-13(a) and (b). The improvement of surface by thermal treatment has been reported.[9,33] It is suggested that enhancement of atom mobility on surface promotes the redistribution of surface atoms, flattening surface.[33] The surface of Ge layer affects the surface of GaAs layer. Figure 4-13(c) and (d) indicate that flat GaAs layers are grown on Ge/Si due to the similar lattice constant of Ge with GaAs and the usage of vicinal Si(001) results in the GaAs layer without APBs. The improvement of Ge surface also improves the GaAs surface. While the RMS roughness of GaAs layer grown on as-grown Ge/Si is 5.82 nm, lower RMS roughness of 2.69 nm is obtained by growing on RTA annealed Ge/Si.

The crystal qualities of GaAs layers were characterized by HR-XRD. Figure 4-14(a) is the XRD curves of as-grown and 10 times RTA annealed Ge layers grown on vicinal Si(001) substrates. After 10 times RTA, shoulder peak is appeared meaning Si-Ge alloying and peak position of Ge(004) is shifted toward low angle. The Ge layer grown on Si is under tensile stress due to the difference of thermal expansion coefficient between Si and Ge. It is thought that stress in Ge layer is partly relieved by Si-Ge alloying during cyclic RTA. The peak shift of Ge(004) by cyclic RTA affected the growth of GaAs layer on Ge/Si. Figure 4-14(b) is the XRD curves of GaAs layers grown on both as-grown and 10 times RTA annealed Ge/Si substrates. While the peak position of GaAs(004) grown on as-grown Ge/Si is located at -5450 arc-sec from Si(001), that of GaAs(004) shifted by -200 arc-sec when grown on 10 times RTA annealed Ge/Si. Furthermore, the results of XRD rocking curves revealed that the FWHM of GaAs peak is reduced from 160 to 140 arc-sec by growing GaAs layer on 10 times RTA annealed Ge/Si.(Not shown here)

The optical properties of GaAs layers were analyzed by cathodoluminescence (CL) at room temperature in order to investigate the effects of Ge layers on GaAs growth. Figure 4-15 is the CL results of GaAs layers grown on two Ge layers. In Fig. 4-15(b), dark spots exist for the GaAs layer grown on as-grown Ge/Si and it seems that they are originated from the rectangular shape features, which can be observed from Fig. 4-13(c). In CL image, dark spot indicates the non-radiative regions. Dark spot-free CL image is obtained by growing GaAs layer on 10 times RTA annealed Ge/Si as presented in Fig. 4-15(d). CL spectra also show that optical property of GaAs layer is affected by RTA

annealing of Ge/Si. Figure 4-15(e) is the CL spectra of GaAs layers grown on both Ge/Si. Band-to-band (B-to-B) transition peak of GaAs layer is slightly shifted from 1.437 to 1.442 eV by 10 times RTA annealing of Ge/Si. The change of B-to-B transition peak is attributed to the change of strain status in GaAs as shown in Fig. 4-14(b). Furthermore, it is clearly shown that CL intensity is doubled by growing GaAs on 10 times RTA annealed Ge/Si. The threading dislocations act as non-radiative recombination centers. Although the effect of RTA was lowered for the Ge layer grown on vicinal Si(001), TDD reduction in Ge layer by 10 times RTA leads to 2 times higher CL intensity of GaAs layer.

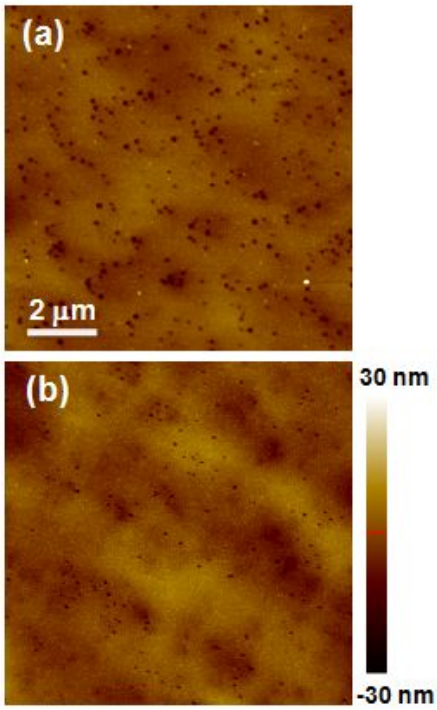

Fig. 4-10. 10 x 10 μm^2 AFM images of Ge layers grown on vicinal Si(001) substrates (a) without and (b) with 10 times cyclic RTA after Secco etching.

Table 4-3 Shear stress induced to Ge layer grown on both nominal and vicinal Si(001) substrate for various slip systems.

Slip plane	**Slip direction**	**Shear stress**	
		Nominal	**6^{o} offcut**
(111)	[10-1]	0.408σ	0.429s
	[01-1]	0.408σ	0.429σ
	[1-10]	0	0
(-111)	[101]	0.408σ	0.433σ
	[01-1]	0.408σ	0.374σ
	[110]	0	0.06σ
(1-11)	[10-1]	0.408σ	0.374σ
	[011]	0.408σ	0.433σ
	[110]	0	0.06σ
(11-1)	[101]	0.408σ	0.369σ
	[011]	0.408σ	0.369σ
	[1-10]	0	0
(001)	[110]	0	0
	[1-10]	0	0.07σ

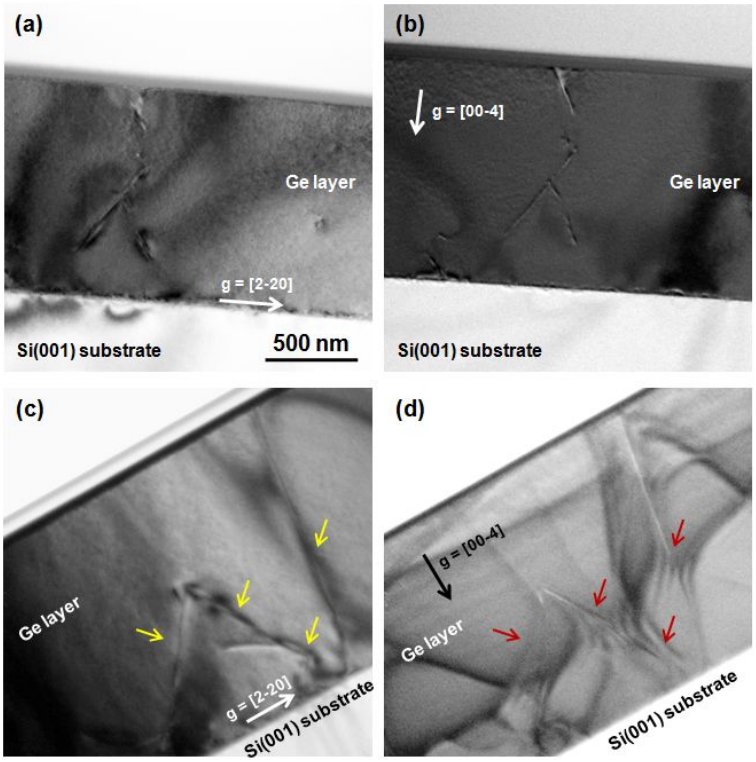

Fig. 4-11. Cross-sectional TEM images of Ge layers grown on (a), (b) nominal and (c), (d) vicinal Si(001) substrates. g vectors are (a), (c) [2-20] and (b), (d) [00-4]. In (c) and (d), same dislocations are marked with yellow and red arrows, respectively.

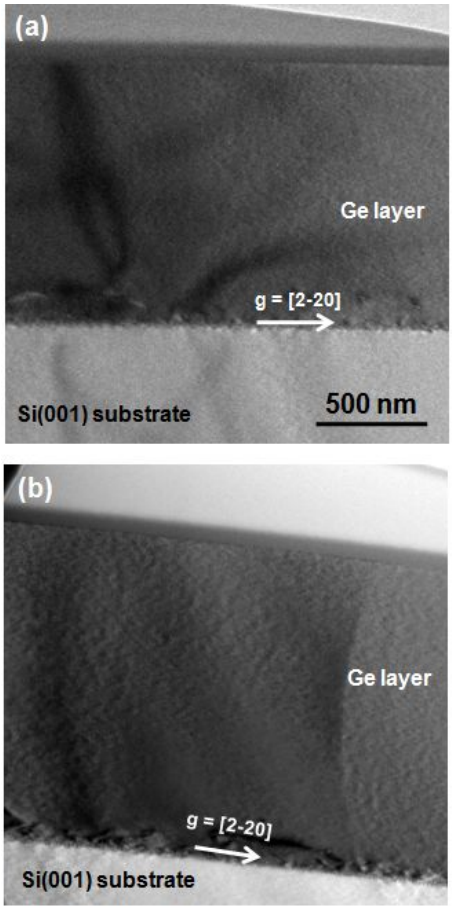

Fig. 4-12. Cross-sectional TEM images of Ge layers grown on (a) nominal and (b) vicinal Si(001) substrates after 20 and 10 times RTA, respectively.

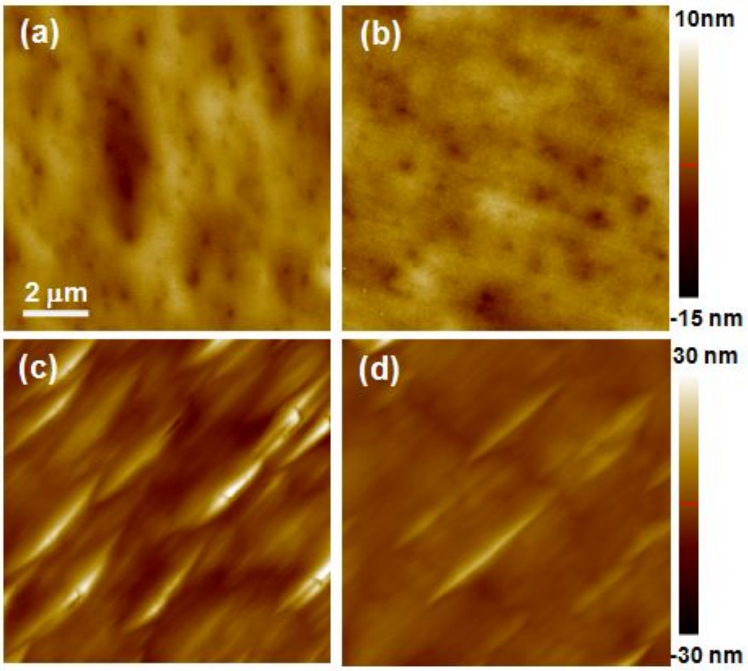

Fig. 4-13. 10 x 10 μm^2 AFM images of (a) as-grown and (b) 10 times RTA annealed Ge layer grown on vicinal Si(001). (c) and (d) are surface morphologies of GaAs layers grown on (a) and (b), respectively. RMS roughnesses are 1.88, 1.55, 5.82 and 2.69 nm, respectively.

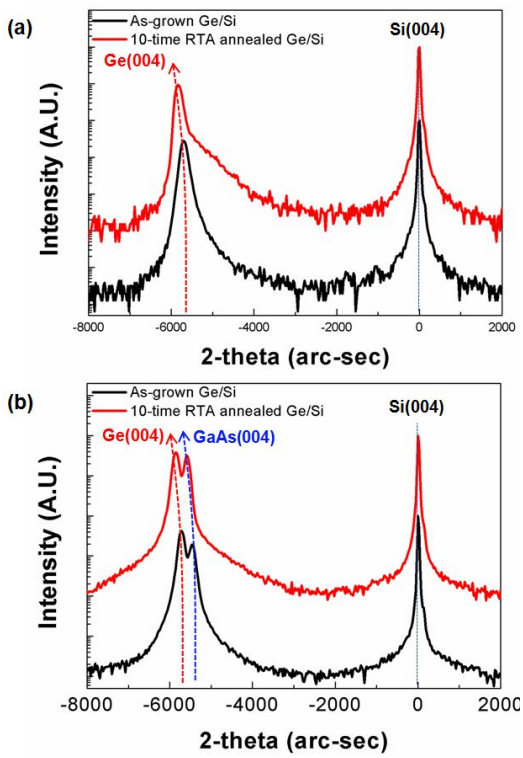

Fig. 4-14. XRD curves of (a) as-grown and 10 times RTA annealed Ge layers grown on vicinal Si(001) substrates and (b) GaAs layers grown on both Ge/Si substrates.

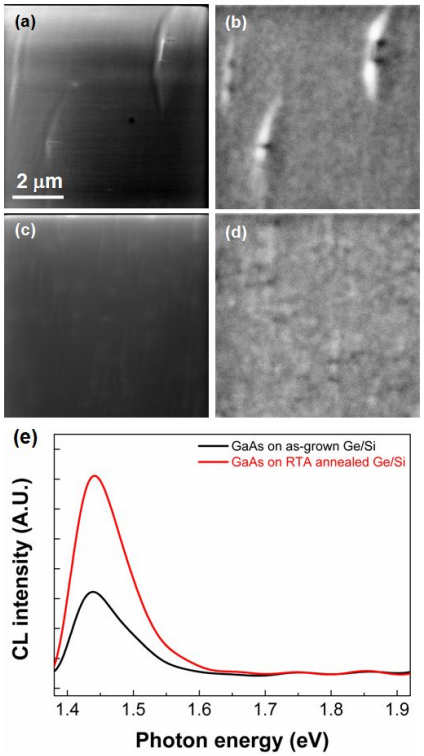

Fig. 4-15. (a) and (c) shows the plan-view SEM images of GaAs layers grown on (a) as-grown and (c) 10 times RTA annealed Ge layers on vicinal Si(001). (b) and (d) are corresponding cathodoluminescence (CL) images of (a) and (c), respectively. (e) CL spectra of GaAs layers grown on both Ge/Si.

4.3 Summary

We investigated the influences of the RTA on Ge layers grown on Si(001) substrates. By depositing SiO_2 layers on Ge surfaces as capping layers, surface roughening could be suppressed when annealed at 650 – 800 ^oC. However, Ge layers were roughened with large hole formations and intermixing between Si and Ge occurred by RTA at 850 ^oC, meaning that SiO_2 does not act as a capping layer. As the RTA temperature increased from 650 to 800 ^oC, the XRC FWHM decreased with the lower TDD, indicating that the higher RTA temperature was more effective in better crystal quality. For further TDD reduction, the number of RTA cycle was varied. As the number of cycle increased from 1 to 20, TDD decreased and the minimum value of 3.5 x 10^7 cm^{-2} was obtained. The movement of threading dislocations is attributed by repetitive stress induction into Ge layer by temperature change, resulting in the annihilation.

In order to adapt Ge layers to III-V growth, Ge layers grown on vicinal Si(001) were annealed by cyclic RTA. Unlike Ge layer on nominal Si(001), the TDD was still on the order of 10^8 cm^{-2} after 10 times RTA. TEM analyses shows that Ge layer grown on vicinal Si(001) has more edge dislocations compared to Ge layer grown on nominal Si(001). The edge dislocation in Ge layer is known to be immobile. Therefore, it is hard for edge dislocations to glide and annihilate by RTA. The surface improvement of Ge layer by cyclic RTA leads to smoother surface of GaAs layer which is grown on Ge/Si. The FWHM of XRC of GaAs layer was reduced from 160 to 140 arc-sec and CL intensity was doubled by growing GaAs on RTA annealed Ge/Si. Overall, better quality GaAs layer with

enhanced optical property was obtained by growing on RTA annealed Ge/Si.

4.4 References

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Chapter 5. Ge regrowth on silica nano-sphere integrated Ge/Si templates

5.1 Introduction

Blocking the movement or glide of threading dislocation by barrier is a well-known technique. The combination of patterning and lateral overgrowth is base on this approach.[1] When Ge layer is grown within SiO_2 pattern, the glide of threading dislocation is interrupted by SiO_2 sidewall as shown in Fig. 1-14(a), leading to the no defects on the top surface. Ghosh *et al.* suggested the Ge regrowth on patterned Ge/Si templates to reduce TDD. After SiO_2 patterning on Ge/Si, some dislocations are located below SiO_2. Such dislocations cannot thread any more, resulting TDD reduction. They reported that defect density was reduced from 9 x 10^{10} to 4.4 x 10^7 cm^{-2}.[2] This group also proposed Ge regrowth using SiO_2 lined etch pits. They blocked etch pits selectively with SiO_2 which were originated from the threading dislocations as shown in Fig. 1-15(a). Total defect density was reduced from 2.6 x 10^8 to 8.7 x 10^6 cm^{-2}.[3] The main advantage of this method is that dislocation can be blocked by lined SiO_2 one by one. However, the process to make selectively SiO_2 coated Ge/Si templates is complex. Furthermore, 3-dimensional growth with facet formation needs the planarization process.

In the recent study of GaN growth on sapphire substrate, Park *et al*. reported similar growth process.[4,5] They used silica nano-sphere (NS) to block TD in initial GaN layer and the process flow

is shown in Fig. 5-1. By using this method, they reduced TDD in GaN from 5 x 10^9 to 3 x 10^7 cm^{-2}. The main advantage of this method is more simple way to mask TDs in GaN layer, reducing regrowth process steps. Based on this concept, I thought that silica NS could be used as a mask to prevent the propagation of TDs in Ge layer grown on Si.

In this study, Ge layers were grown on silica NSs integrated Ge/Si templates with following process steps. First, initial Ge layers were grown on Si in a twp-step, followed by defect etching by Secco etchant. Then, silica NSs were selectively integrated into etch pits using spin-coater. Finally, Ge layers were regrown on silica NSs integrated Ge/Si templates.

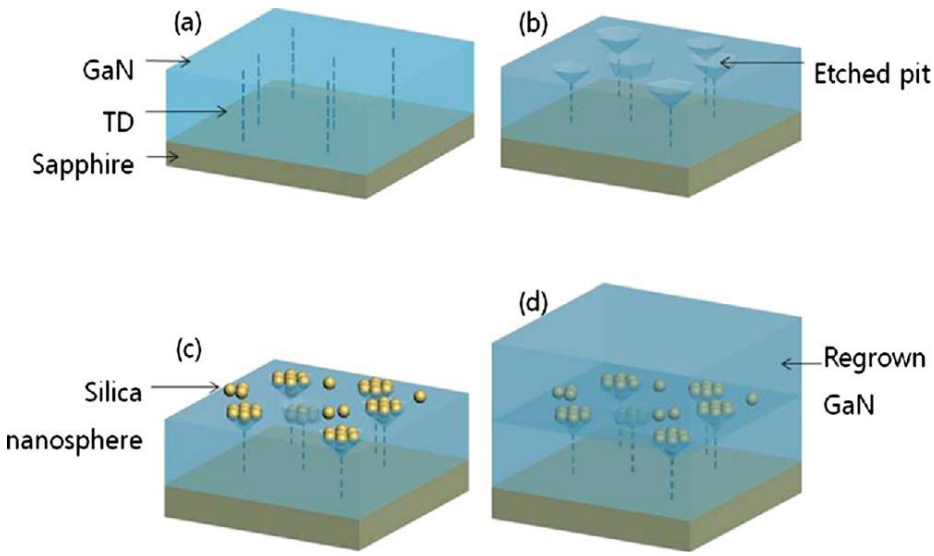

Fig. 5-1. Schematic depiction of steps involved in the process of selective defect blocking by self-assembled silica NSs. (a) Initial GaN growth on sapphire. (b) Defect etching using H_3PO_4. (c) Self-assembled silica NSs on the selective defect etched GaN. (d) Regrowth of GaN on silica NS integrated GaN templates.[4]

5.2 Experimental procedures

Ge regrowth was proceeded as follows: First, initial Ge layers of 500 nm were grown on Si substrates using two-step method in UHV-CVD. After the growth, defects were selectively etched using Secco etchant composed of 2HF : 1$K_2Cr_2O_7$ (0.15 M).[6] In order to optimize etch condition, etch time was varied from 30 to 180 sec. silica NSs of 50 nm were used for integration into etch pits. Silica NSs were dispersed in ethanol and the concentration was varied from 9/16 to 9 mg/ml. Silica NSs were integrated on 6-inch, defect etched Ge/Si substrates using spin coater followed by 2 times rinsing with ethanol. RPM was set to 2000 and coating time was 40 sec for each step.

Ge layers were regrown on silica NSs integrated Ge/Si templates in UHV-CVD. Before epitaxy, templates were thermally cleaned at 650 ^{o}C for 30 min to remove native oxide.[7] First, Ge layers were grown at 350-500 ^{o}C for 2 h, fixing the pressure at 17 mtorr. Then, two-step Ge layers were grown on templates as follows: first layers were grown at 350 ^{o}C for 4 hour followed by growth at 550 ^{o}C for 4 h 30 min.

The thickness and surface of Ge layers were characterized in SEM. AFM analyses were carried out to observe etch pits on the surfaces. The TDD was measured by SEM combined with Secco etching. The defects were examined by TEM.

5.3 Results and discussion

5.3.1 Fabrication of templates

In order to fabricate the silica NSs integrated templates, defects on Ge surfaces were preferentially etched by Secco etchant. Secco etching is progressed in a two-step: First, Ge surface is oxidized by oxidant such as $K_2Cr_2O_7$. Then, oxide is removed by HF. During the etch process, defect area is oxidized and removed at faster or slower rate than surrounding area, resulting in the pit formation.[8,9] Figure 5-2(a)-(d) show the AFM images of Ge layers after Secco etching for 30-180 sec. As shown in Fig. 5-2(a) and (b), pits with inverted pyramid shape are formed and the density of pit is 6.44 x 10^8 cm^{-2}. The each plane of pits has {113} facet. Furthermore, both the lateral size and depth of etch pits increase with etch time. However, beyond 120 sec, the edges of etch pits begin to intersect in Fig. 5-2(c) and flat regions are almost disappeared by 180 sec etching (Fig. 5-3(d)). Figure 5-2(e) shows the plot of size of etch pits as a function of etch time. At the initial stage, both lateral size and depth of etch pits linearly increase but over-etch by longer time etch reduces size of etch pits and they are saturated.

The silica NSs were integrated on 60 sec etched Ge/Si substrates by spin coater varying the concentration of silica NSs in ethanol. The lateral size and depth of 60 sec etched pits are around 200 and 40 nm, respectively in Fig 5-3(a). Figure 5-3(c)-(f) shows the plan-view SEM images of Ge surfaces after silica NSs integration by spin coater. The silica NSs show darker on the etch pits than those on the planar regions. When the concentration is 9

mg/ml, silica NSs coat not only etch pits but flat surfaces. The area covered by silica NSs are reduced by decreasing concentration of silica NSs and NSs are selectively integrated into only etch pits by using 9/8 mg/ml colloid.(Fig. 5-3(d) and (e)) However, most pits remain unfilled by using not enough concentration of 9/16 mg/ml as shown in Fig. 5-3(f).

Before spin coating, colloid is uniformly dispersed on the whole Ge surface. In spin coating, the first step of spin coating is dominated by centrifugal forces, which cause the solution to flow toward the edge of substrate. Second step is governed by solvent evaporation.[10] When the height of solvent is near the diameter of silica NSs, they move on the flat surface by centrifugal and immersion capillary forces. In addition to those two forces, gravity force is also induced to silica NSs. Near the etch pit, the direction of net force is toward etch pits, easily moving silica NSs into etch pit as illustrated in Fig. 5-3(b).[11,12] Once silica NSs fill the etch pit, they cannot escape because each wall of etch pit act as a barrier. As a result, silica NSs are captured in etch pits. If the concentration of silica NSs is high, excess silica NSs which do not fill the etch pits are remained on surface as shown in Fig. 5-3(c). On the other hand, too low concentration of silica NSs is not enough to fill all pits (Fig. 5-3(f)). Thus, in order to selectively integrate silica NSs into only etch pits, the concentration of solution should be optimized. Finally, silica NSs integrated Ge/Si templates was fabricated using colloid of 9/8 mg/ml on which silica NSs were located on only etch pits and Ge layers were grown on those templates.

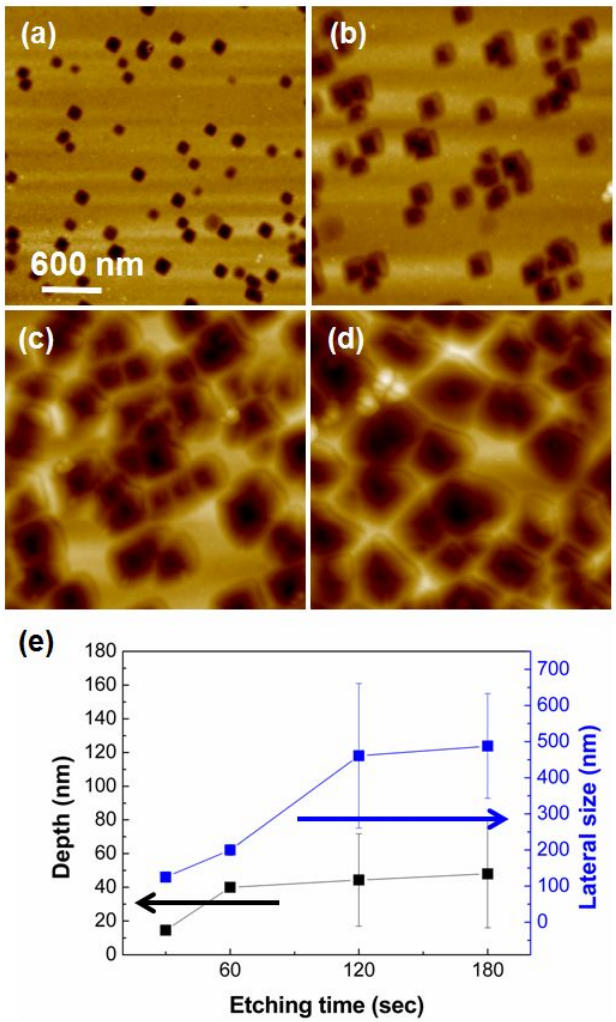

Fig. 5-2. (a)-(d) 3 x 3 μm^2 AFM images of Ge layers grown on Si substrates after Secco etching. The etching times were (a) 30, (b) 60, (c) 120 and (d) 180 sec. (e) The plot of depth and lateral size of etch pits as a function of etching time.

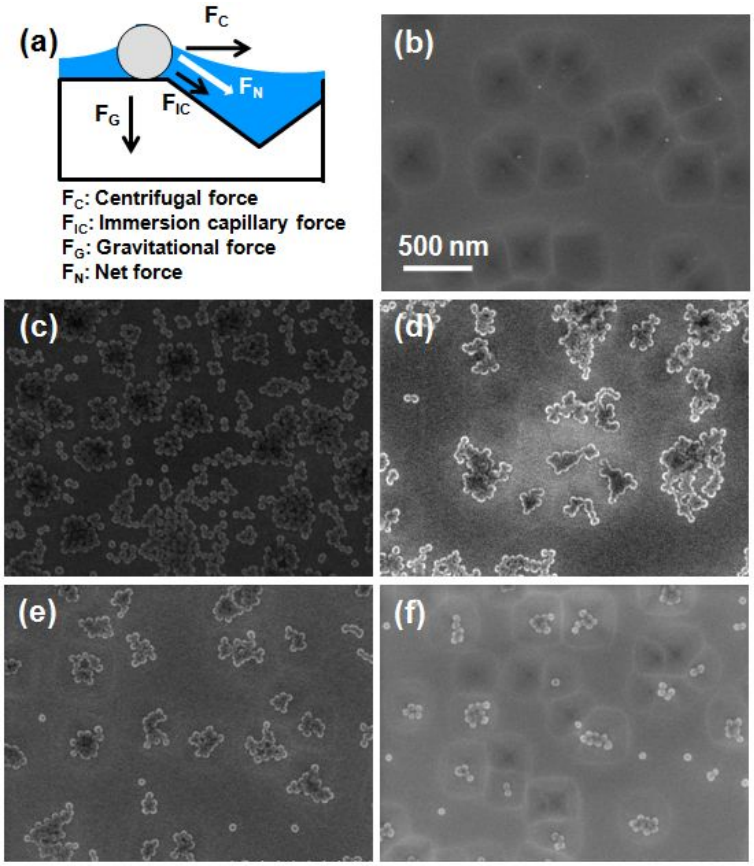

Fig. 5-3. (a) Schematic illustration of silica NSs near the etch pit. Plan-view SEM image of (b) as-etched and (c)-(f) silica NSs integrated Ge layers grown on Si using spin coater. The concentrations of silica in colloid were (c) 9, (d) 9/4, (e) 9/8 and (f) 9/16 mg/ml.

5.3.2 Regrowth of Ge on silica NS integrated Ge/Si templates

Ge layers were grown on silica NSs integrated Ge/Si templates varying the growth temperature from 350 to 500 ^{o}C. In order to investigate the effect of growth temperature on growth behavior, growth pressure and time were fixed at 17 mtorr and 2 h, respectively. Figure 5-4 shows the cross-sectional SEM images of regrown Ge layers. In Fig. 5-4, silica NSs are not observed because silica NSs at the sample edge are easily removed during sample cutting for SEM analysis. For all samples, Ge layers are grown 3-dimensionally with islands within silica NSs and no fully coalesced Ge regions are observed. {113} facet is dominant for most planes of islands which is typical for group IV windows along [110] direction and (001) plane is barely observed. Moreover, additional {111} facets appeared for the samples grown at 450 and 500 ^{o}C as shown in Fig. 5-4(a) and (b). As the growth temperature decreased from 500 to 450 ^{o}C, the length of {111} facets decreased and {110} facets are developed. Ge layers begin to laterally grow over silica NSs, suppressing formation of {111} facets by growing at 400 ^{o}C (Fig. 5-4(c)). More reduction of growth temperature to 350 ^{o}C leads to the more lateral overgrowth as shown in Fig. 5-4(d).

Actually, in this experiment, the distances between two nearest pits with silica NSs are different and the number of silica NSs covering each pits are not same for all pits. Thus, it is hard to discuss in detail about the mechanism of facet evolution on the silica NSs selectively integrated Ge/Si templates unlike conventional selective epitaxial growth (SEG) using periodic SiO_2 pattern. However, the Ge growth on silica NSs integrated Ge/Si

templates might be followed by principles based on the SEG of group IV.

First, when GeH_4 is injected onto silica, the chemical reaction between GeH_4 and silica is:[13,14]

$$GeH_4 \rightarrow Ge + 2H_2 \quad (1)$$

$$Ge + SiO_2 \rightarrow GeO_2 + Si \quad (2)$$

$$GeO_2 + Ge \rightarrow 2GeO \quad (3)$$

In the above equations of chemical reaction, GeO, resulting by-product is known to be volatile, so Ge is not deposited on the silica NSs. This implies that the adsorption site for Ge growth is only the open Ge surface.

In the case of SEG of group IV materials on a patterned Si substrate, epitaxial layer is typically 3-dimensionally grown with islands and the planes of islands are composed of the facets of {001}, {113} and {111} or their combinations.[15,16,17,18,19] Moreover, the principle for the growth competition of facets is that the inter-facet mass transport occurred from the facet with low growth rate to the facet with high growth rate. Generally, the growth rates of three facet plane is as follows: R(001) > R(113) > R(111).[16,17,18] Thus, mass on facet plane moves from {113} to {001}, from {111} to {113} and from {111} to {001}.

At the initial SEG stage, {113} facets are formed near the SiO_2 side wall, which are known to be facets with minimal total free energy and (001} facet also formed from the open Ge surface.[15,17] When the diffusion length of adatom on {113} is longer than facet length, the atoms are diffused from {113} to

{001}, reducing the area of {001} plane. The increase of {113} facet area also raises the total free energy, allowing {113} facet to be energetically unfavorable. At that time, {111} facets begin to appear which have lowest surface energy.[20] Finally, {111} facet is rapidly extend, replacing other facets. However, if the diffusion length of adatom on {113} is shorter than facet length, atoms cannot diffuse anymore and they are accumulated on the facet plane, leading to the facet growth.

Based on the principle of SEG, the Ge regrowth procedures on the silica NSs integrated Ge/Si templates are schematically illustrated in Fig. 5-5. Figure 5-5(a) and (b) briefly show the regrowth at high temperature of 500 ^{o}C and the low temperature of 350 ^{o}C, respectively. In this experiment, the distance between two pits are few hundred nm and {113} facet is already developed before growth due to the defect etch process. Thus, {001} facet is more rapidly replaced with {113} facet at the higher temperature growth in the initial growth stage due to the enhanced adatom mobility on the facet plane. Then, {111} facet is appeared instead of accumulation on the {113} facet due to the unstable interface between Ge and SiO_2 with high energy as shown in Fig. 5-4(a).
The reduced growth temperature shortens the diffusion length of adatom so that atoms are easily accumulated on the facet surface, kinetically suppressing the formation of {111} facet. At that time, meta-stable {110} facets begin to appear at the Ge/SiO_2 interface and more growth results in the lateral growth over silica NSs in Fig. 5-5(b). It is inferred that when Ge is grown at higher temperature of 500 ^{o}C, longer growth time is required to obtain fully coalesced Ge layer compared to lower temperature growth of 350 ^{o}C. Furthermore, fully overgrown Ge layer has more {111}

facet at higher temperature. The angles between (111) and (001) and (113) and (001) are 55 and 25^{o}, respectively. Above results and discussions indicate that the lower temperature is desirable to grow relatively thin and flat Ge layer over silica NSs. However, high temperature growth is also required in order to obtain high quality Ge layer.

In order to obtain perfectly ELO Ge layer with high quality, two-step Ge regrowth was performed. First regrown layers were grown on silica NSs integrated Ge/Si templates at 350 ^{o}C for 4 h, followed by second layer growth at 550 ^{o}C for 4 h 30 min. Figure 5-6(a) and (b) show the plan-view and cross-sectional SEM images of Ge regrown layers in two-step. Fully coalesced Ge layer is obtained which is caused by longer time growth at 350 ^{o}C as shown in Fig. 5-6(a). However, Fig. 5-6(a) and (b) reveal that the surface of regrown Ge layer is very rough since the Ge growth on silica NSs started after the coalescence.

In order to study the effect of silica NSs on TDD reduction, regrown Ge layer was analyzed by TEM. Figure 5-6(c) and (d) show cross sectional TEM images of two different regions of Ge regrown layer over silica NSs integrated Ge/Si templates. TEM images show that silica NSs are successfully coated with monolayer and Ge is coalesced over silica NSs without void formations. It is also observed in Fig. 5-6(c) that the threading dislocation is terminated by silica NSs and does not propagate toward the surface. However, Fig. 5-6(d) indicates that there exist threading dislocations generated from silica NSs in some regions. The formation of threading dislocations on the silica might be originated from the fact that the growth error occurred during

coalescence. Figure 5-6(e) shows a plan-view SEM image of the resulting Ge layer after Secco etching. The TDD is reduced from 6.44 x 10^8 to 6.94 x 10^7 cm^{-2} by integrating silica NSs and regrowth. When epitaxial lateral overgrowth (ELO) is proceeded with SiO_2, it has been reported that planar defects are generated on the SiO_2 during ELO such as twin boundary or stacking fault.[1,2,3] Leonhardt *et al.* suggested that planar defects were also attributed to the coalescence of the Ge ELO layer over SiO_2 due to atomic-scale roughness of SiO_2, width of SiO_2 which was not integer multiple of Ge lattice spacing and thermal stress.[3] However, there were no evidence of planar defect formations in my regrown Ge layer from TEM and EPD analyses. The stacking fault or twin boundary is created by disturbance of normal layer sequence on the closed packed plane and typically lies on {111} plane for the diamond structure. Therefore, adsorption of atoms on {111} facet might be responsible for the planar defects. Such mechanism about planar defect formations was also proposed for the SEG and III-V growth on Si.[21,22] In my experiments, ELO Ge layers with {113} facets were coalesced without {111} facets by growing at low temperature of 350 ^oC. It is thought that the suppression of {111} facet leaded to no planar defect formation in regrown Ge layer.

For further TDD reduction, regrown Ge layer was thermally annealed by RTA. 10 times cyclic RTA was performed at 800 ^oC and the annealing time of each RTA was 30 sec. The TDD is reduced to 1.67 x 10^7 cm^{-2} by post RTA as represented in Fig. 5-6(f). However, rough surface of regrown Ge layer requires additional planarization process in order to adapt the regrown Ge layers to devices.

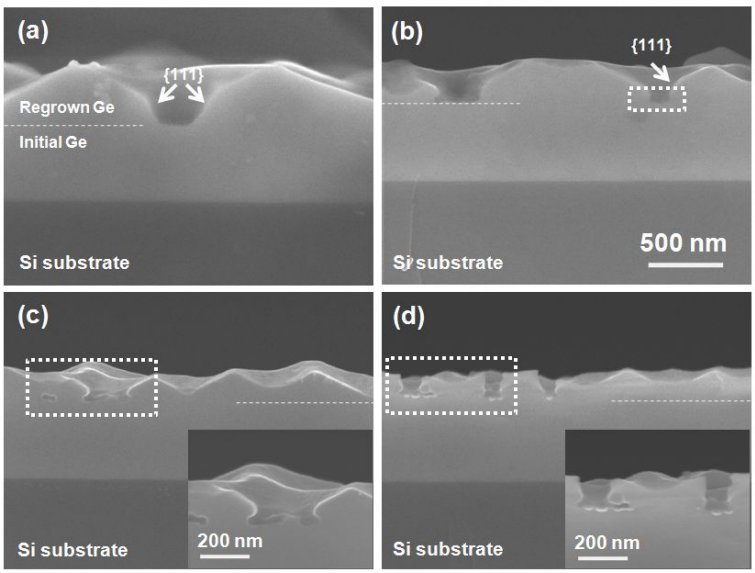

Fig. 5-4. Cross-sectional SEM images of regrown Ge on silica NSs integrated Ge/Si templates at (a) 500, (b) 450, (c) 400 and (d) 350 ^{o}C for 2 h.

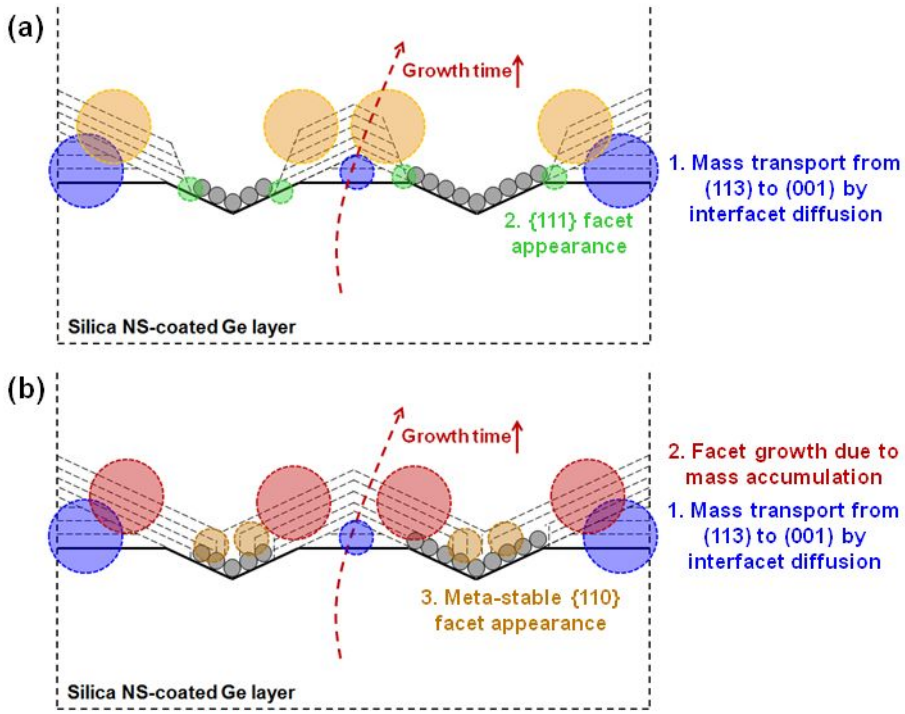

Fig. 5-5. Schematic drawing of Ge growth on silica NSs integrated Ge/Si surfaces at (a) 500 and (b) 350 ^{o}C.

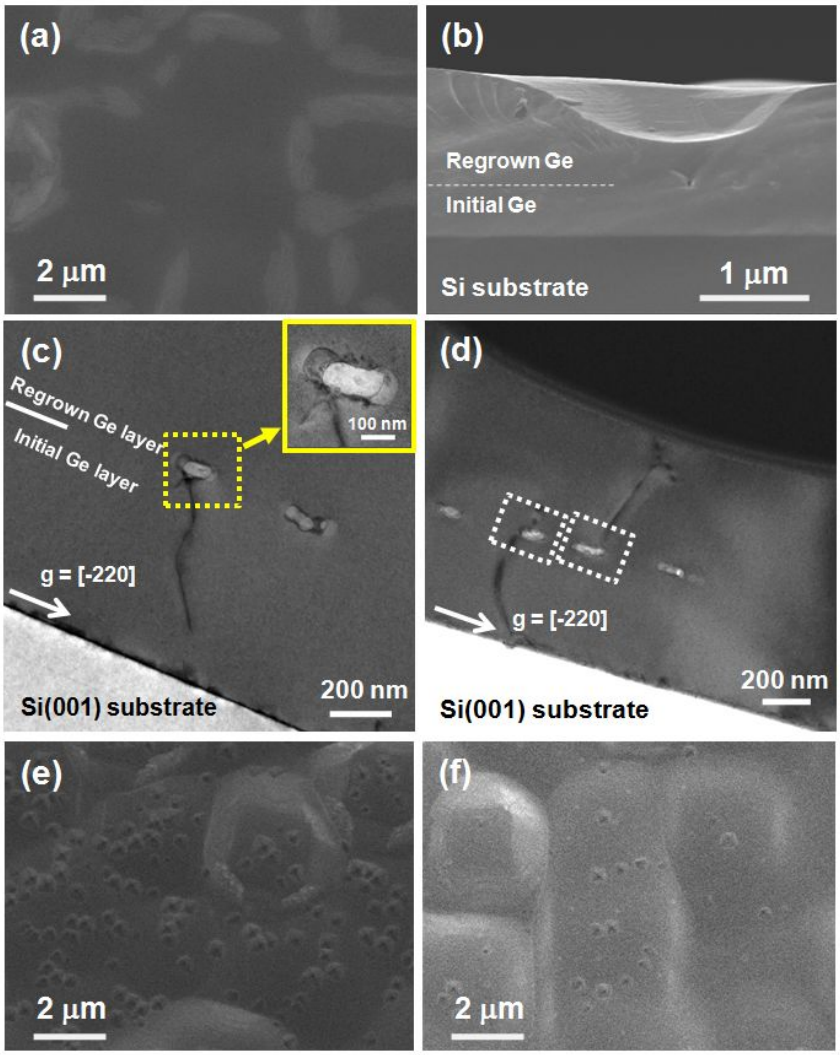

Fig. 5-6. (a) Plan-view and (b) cross sectional SEM images of two-step regrown Ge layers on silica NSs integrated Ge/Si templates. (c), (d) Cross-sectional TEM image of regrown Ge layers. Plan-view SEM images of regrown Ge layers (e) without and (f) with 10 times cyclic RTA after Secco etching.

5.4 Summary

Ge layers were grown on the silica NSs integrated Ge/Si templates. For the fabrication of templates, initial Ge layers were defect-etched using Secco etchant. Then, silica NSs were selectively integrated on the etch pits by using spin coater. The regrown Ge layers were very roughened with island formation and no coalescence was progressed at the growth temperature range of 350 – 500 ^{o}C. However, lower temperature was more desirable to obtain ELO Ge layer over silica NSs. Fully coalesced Ge layer was obtained by using two-step growth. The silica NSs successfully blocked the propagation of threading dislocations but some threading dislocations were generated from the silica NSs. The Ge regrowth using silica NSs resulted in the reduction of TDD from 6.44 x 10^{8} to 6.94 x 10^{7} cm^{-2}. Finally, TDD of 1.4 x 10^{7} cm^{-2} was obtained by post cyclic RTA. However, rough surface due to 3-dimensional growth requires the additional planarization process.

5.5 References

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Chapter 6. Conclusions

Pure Ge layers were grown on Si(001) substrates in a two-step using UHV-CVD for the application of solar cell application. In order to reduce TDD, two methods were proposed: post RTA and regrowth using silica NSs.

First, Ge layers were grown on Si(001) substrates using two-step method. By growing Ge buffer layer as the low temperature of 300 ^{o}C, flat Ge layer could be grown on Si substrate with low RMS roughness of 1.3 nm. The FWHM of XRC decreased by increasing layer thickness, indicating that the crystal quality of Ge was improved. The threading dislocation density (TDD) in Ge layer was decreased from 2.4 x 10^{9} to 4.3 x 10^{8} cm^{-2} by increasing the layer thickness from 250 to 900 nm due to the annihilation of dislocations during growth.

In order to reduce the TDD in Ge layer, I annealed Ge layers by using RTA. When Ge layers were annealed at 650-800 ^{o}C by RTA, surfaces were roughened with pit formations. 850 ^{o}C RTA resulted in the sublimation of Ge. The surface roughening was avoided by depositing 200 nm-thick SiO_2 on Ge surface. However, SiO_2 could not act as a capping layer at 850 ^{o}C, forming large holes with the diameter of 20 μm, limiting the temperature of RTA. As the RTA temperature increased from 650 to 800 ^{o}C, crystal quality was improved with the lower FWHM of XRC. 850 ^{o}C annealing worsened the crystalinity of Ge layer due to the sublimation. TDD was also reduced by RTA and higher temperature leads to the lower TDD. After RTA at 800 ^{o}C, TDD of 2.24 x 10^{8} cm^{-2} was obtained. Stress during RTA allows dislocations to move. Stress increases as the RTA temperature

increases. Thus higher temperature reduced more dislocations. In order to obtain less TDD, I did cyclic RTA. Repetitive tensile and compressive stresses are induced in Ge layer during cyclic RTA. Increasing the number of cycle was more effective rather than increasing time and lowest TDD was obtained of 3.5 x 10^7 cm^{-2} by 20 times RTA. The average distance between two nearest dislocations increases after each RTA cycle since TDD decreases. Therefore, the amount of TDD reduction per each cycle decreased as the number of cycle increased. For the thin Ge layers with high TDD on the order of 10^9 cm^{-2}, TDD was still high after 5 times RTA due to the limited capacitance to move dislocations.

Then, Ge layer grown on vicinal Si(001) substrate was annealed by cyclic RTA for the MJSC application. In this case, TDD decreased from 3.36 to 1.96 x10^8 cm^{-2} even after 10 times RTA. The effects of RTA was reduced when Ge layers grown on vicinal Si(001) substrates. It is observed that more threading dislocations of pure edge type existed in Ge layers grown on vicinal Si(001) than those of Ge layers grown on nominal Si(001) from TEM analyses. Burgers vector of pure edge dislocation is a/2[1-10] which lies on (001) plane. Because (001) is not the slip plane in Ge, edge dislocations cannot move even under stress. Since Ge layers grown on vicinal Si(001) has more immobile edge dislocations, more dislocations were remained in the Ge layer after cyclic RTA. TDD reduced Ge/Si substrate improved the optical properties of GaAs grown on Ge/Si by cathodolumineascence.

Finally, Ge was regrown on silica NSs integrated Ge/Si templates which act as a mask to block the propagation of threading dislocations. The templates were fabricated as follows: initial Ge layer growth in a two-step, selective defect etching by Secco etchant and filling silica

NSs into etch pits. Pits were formed with inverted pyramidal shape by using Secco etchant which were originated from the dislocations and each plane of etch pit has {113} facets. The etch pit density of initial Ge layer was 6.44 x 10^8 cm^{-2}. Both lateral size and depth of etch pits increased as etch time increased from 30 to 120 sec. Beyond 120 sec, the pit size was slightly decreased and saturated by the intersection of nearest etch pits, roughening surfaces. Then, silica nano-spheres were coated on the 60 sec etched Ge/Si substrates by spin coater. As the concentration of silica in ethanol decreased from 9 to 9/8 mg/ml, silica NSs on the planar surface decreased. By using 9/8 mg/ml colloid, silica NSs can be preferentially integrated into only etch pits not on the planar surface. However, colloid with less concentration did not fill all etch pits.

3-dimensional growth was observed when Ge was grown on the silica NSs at 350-500 ^oC for 2h, like selective epitaxial growth on patterned substrates. Most plane of islands have {113} facet for all cases. The lower temperature growth suppressed the formation of {111} facet and enhanced lateral overgrowth. By regrowing Ge in a two-step, fully coalesced Ge layer was obtained but surface was roughened due to the facet growth. TEM analysis confirmed that dislocations were not propagated toward surface since they were blocked by silica NSs. On the other hands, there were dislocations generated from the silica NSs at some regions due to the growth error during epitaxial lateral growth over silica NSs. In this experiment, no planar defects were observed because {111} facet formation was suppressed by low temperature growth of 350 ^oC. Dislocation blocking by silica NSs results in TDD reduction to 6.94 x 10^7 cm^{-2}. TDD could be decreased to the value of 1.4 x 10^7 cm^{-2} by 10 times RTA. However, additional planarization process is needed to apply regrown Ge layers on devices.

초 록

이 연구의 목표는 광검출기 및 다중접합 태양전지 등으로 응용 가능한 고품질의 게르마늄 에피층을 실리콘 기판 위에 성장하는 것이다. 목표의 달성을 위한 실험은 다음과 같이 진행되었다. 우선 2단계 성장법을 이용하여 평탄한 표면을 갖는 게르마늄 에피층을 성장하였다. 이때에 성장 조건이 에피층의 물성에 미치는 영향을 알아보았다. 그리고 성장한 게르마늄 에피층 내부에 존재하는 관통전위 밀도를 줄이기 위하여 후속공정으로 급속 열처리를 이용한 열처리를 진행하였다. 이때에 열처리 온도, 시간 등 열처리 조건이 게르마늄 에피층에 미치는 영향을 알아보고, 최적화하였다. 마지막으로 실리카 나노구체를 이용한 재성장방법을 통하여 결함밀도가 감소한 게르마늄 에피층을 얻고자 하였다.

첫째, 2단계 성장법을 이용하여 게르마늄 에피층을 실리콘 기판 위에 성장하였다. 저온에서 순수 게르마늄 완충층을 성장함으로써, 3차원 적인 성장이 억제된 2차원적으로 성장한 평탄한 에피층을 얻을 수 있었다. 게르마늄 에피층의 결정성은 에피층의 두께가 증가함에 따라서 향상되는 양상을 보였으며, 관통전위밀도 역시 두께가 증가함에 따라서 감소하는 것을 확인할 수 있었다. 900 nm 성장한 게르마늄 에피층에서 4.3 x 10^{8} cm^{-2} 의 관통전위밀도를 얻을 수 있었으며, 이는 고온 성장 중 관통전위들이 이동하면서 만나서 소멸되었기 때문이다. 이러한 두께증가에 따른 관통전위 밀도감소가 결정성의 향상의 원인으로 작용하였다. 실리콘 기판 위 성장한 게르마늄 에피층을 이용하여 제작한 2중접합태양전지의 효율은 10.3%로 게르마늄 기판을

이용하여 제작한 태양전지에 비해서 감소된 효율이었다. 이러한 효율 감소의 원인은 10^8 cm^{-2} 수준의 결함밀도에서 기인 한 것으로 결함 밀도 감소를 위해 후속 열처리를 진행하였다.

후속 열처리는 급속열처리장비를 이용하여 진행하였다. 30초의 짧은 시간동안 열처리를 진행하였지만 게르마늄 표면에 높은 밀도의 구덩이가 형성되면서 표면이 거칠어지는 것을 확인하였다. 이는 결함식각 및 열에너지에 의한 손상 때문이며, 게르마늄 표면에 이산화규소 박막을 증학함으로써 이러한 손상을 억제할 수 있었다. 하지만 850 ^oC 에서는 게르마늄이 쉽게 승화하기 때문에 매우 큰 구덩이가 형성되면서 이산화규소 박막이 보호층으로써의 역할을 하지 못한다는 것을 확인할 수 있었다. 열처리 온도가 증가함에 따라서 결정성이 향상되고, 결함밀도가 감소하는 것을 확인할 수 있었다. 열처리 시 게르마늄과 실리콘간의 열팽창 계수차이 때문에 게르마늄 에피층 내부에 응력이 걸리며, 이 응력은 열처리 온도가 증가함에 따라서 증가하기 때문에 고온에서 열처리를 증가할수록 전위가 더 쉽게 이동하여 소멸할 수 있다. 따라서 800 ^oC 에서 열처리 시 가장 낮은 2.2 x 10^8 cm^{-2} 의 전위밀도를 얻을 수 있었다. 결함밀도를 더 줄이기 위해서 주기적인 급속열처리를 진행하였다. 주기를 증가함에 따라서 결함밀도가 감소하는 경향을 보였고, 20번 반복하였을 때 3.5 x 10^7 cm^{-2} 의 결함밀도를 얻을 수 있었다. 주기적인 열처리를 진행할 경우, 반복적인 인장, 압축응력이 게르마늄 에피층에 가해지기 때문에 결함의 이동이 활성화 되어 결함이 지속적으로 감소하게 되는 것이다. 주기적인 급속 열처리방법을 사용함으로써 짧은 시간에 결함밀도를 줄일 수 있었다.

태양전지 응용 및 3-5족 물질 성장을 위하여 6도 기울어진 실리콘 기판 위에 성장한 게르마늄 에피층에 주기적인 급속 열처리를 진행하였다. 10회 진행하였을 때, 에피층의 관통전위 밀도는 여전히 10^8 cm^{-2} 였다. 투과전자현미경을 이용하여 전위를 관찰해본 결과, 6도 기울어진 실리콘 기판 위에 성장한 게르마늄 에피층 내부에는 움직이지 못하는 칼날전위가 다수 존재하는 것을 확인할 수 있었다. 칼날전위의 버거의 벡터는 최밀집면이 아닌 (001) 면상에 있기 때문에 이 전위는 움직일 수 없다. 따라서 열처리에 의한 이동이 불가능하기 때문에 열처리후에도 다수의 전위가 에피층 내부에 남아있는 것을 알 수 있었다. 하지만 결함밀도의 감소는 상부에 성장한 비화갈륨 에피층의 광학성질을 향상시켰다.

마지막으로 실리카 나노구체를 이용한 게르마늄 재성장을 진행하였다. 세코식각법을 이용하여 선택적으로 게르마늄 에피층의 결함을 식각하였다. 초기성장 게르마늄 에피층의 결함밀도는 6.44 x 10^8 cm^{-2} 이며, 식각구덩이의 크기는 식각시간에 비례하여 증가하였으며, 과식각 시 식각구덩이들끼리 만나면서 표면이 거칠어 지는 것을 확인하였다. 60초동안 결함식각한 게르마늄 에피층 표면에 실리카 나노구체의 집적을 진행하였다. 실리카 나노구체가 분산되어있는 콜로이드 내부의 실리카 나노구체의 농도를 감소함에 따라서 식각구덩이가 아닌 평탄한 면상에 존재하는 실리카 나노구체의 양이 감소하였으며, 농도가 9/8 mg/ml 인 콜로이드 사용 시 식각구덩이에만 선택적으로 실리카 나노구체를 집적할 수 있었다. 실리카 나노구체가 선택적으로 집적된 형판 우에 게르마늄 재성장을 진행하였다. 350-500 ^oC 의 성장온도에서 성장 시 모든 온도에서 3차원적인 성장을 하였다. 성장온도를 감소함에 따라서 {111} 면

성장이 억제되었으며, 실리카 나노 구체 위로 측면과성장이 진행되는 것을 확인하였다. 최종적으로 2단계 성장을 진행하여 실리카 나노구체를 모두 덮은 게르마늄 에피층의 성장이 가능하였다. 하지만 3차원적인 성장으로 인하여 매우 거친 표면이 얻어졌다. 투과전자현미경을 이용한 분석을 통하여 실리카 나노구체가 관통전위의 진행을 막았음을 확인할 수 있었지만, 실리카 나노구체에서부터 생성되는 관통전위도 관찰할 수 있었다. 이는 실리카 나노구체 위로 과성장하는 게르마늄들이 만날 때 오류가 발생하여 생성된 것으로 보인다. 하지만 최종적인 게르마늄 재성장 에피층의 전위밀도는 6.94 x 10^7 cm^{-2} 로 감소하였으며, 10번의 주기적인 급속열처리를 통하여 1.4 x 10^7 cm^{-2}로 결함밀도가 감소한 게르마늄 에피층을 얻을 수 있었다. 하지만 재성장한 게르마늄 에피층을 소자에 응용하기 위해서는 후속평탄화 과정이 필요할 것으로 생각된다.

주요어: 초고진공화학기상증착법 (UHV-CVD), 게르마늄 (Ge), 2단계 성장 (two-step growth), 급속 열처리 (RTA), 실리카 나노구체 (silica nano-sphere)

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