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Ph.D. DISSERTATION

Characterization of Atomic Layer Deposited Lanthanum Silicate Films for a Gate Oxide of Si and Ge Devices

by

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February 2014

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Characterization of Atomic Layer Deposition Lanthanum Silicate Films for a Gate Oxide of Si and Ge Devices

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Abstract

The effect of oxygen sources, i.e. O_3 or H_2O, on chemical composition, dielectric constant and leakage current density of atomic-layer-deposited La-silicate films on Si substrate was examined. The dielectric constant of La-silicate films grown on Si substrate using O_3 was ~ 8.0, which was lower than that of La-silicate films grown using H_2O, ~ 11.7 due to the higher Si concentrations. However, leakage current density of La-silicate films grown using O_3 was about 3 orders of magnitude lower than that of La-silicate films grown using H_2O at an identical capacitance-equivalent-thickness (but almost half the physical thickness), due to the higher Si concentrations and less La-carbonate formation.

We have investigated the effects of Si concentrations in La-silicate film formed by ALD on Ge substrate of the electric property especially in reduction of C-V hysteresis. La-silicate film with Si concentration increment (~ 25 % to ~ 35 %) on Ge substrate effectively reduced C-V hysteresis due to suppression of Ge sub-oxide generation calculated from XPS analysis.

La-silicate film with very thin Al_2O_3 interface passivation layer on Ge substrate obtained smaller C-V hysteresis as ~238 mV due to lower interface state density by suppression of Ge sub-oxide formation. BEMAS-SiO_2 capping La-silicate film with Al_2O_3 interface passivation layer showed smaller Ge sub-oxide formation as smaller C-V hysteresis shown.

Al_2O_3 interface passivation La-silicate film and SiO_2 capping La-silicate film with Al_2O_3 interface passivation layer has tendency of low leakage current density. It is also found that the Al_2O_3 thickness of 1– 2 monolayer and SiO_2 capping is critical for the reduction of the

interface state density.

In conclusion, the ALD-Al_2O_3 interfacial passivation layer and SiO_2 capping, whose thickness can be precisely controlled, is effective for controlling the formation of Ge oxides at high-*k*/Ge interfaces.

Keywords : high-κ, ALD, La-silicate, La_2O_3, Al_2O_3, SiO_2, Si, Ge, deposition behavior, Ozone, leakage current mechanism, XPS

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1. Introduction

Since the invention of Si-based metal-oxide-silicon field effect transistor (MOSFET) [1, 2], there has been an unprecedented evolution in semiconductor industry shown as Fig. 1. For complementary metal oxide semiconductor (CMOS) scaling beyond the 45/32 nm technology node, HfO_2 as a high dielectric constant (high-*k*) material is used to replace SiO_2 or oxynitrides, because of excessive leakage current and reliability concerns. [3] The thickness shrinkage of the dielectric layer for a higher capacitance produces problems of a high leakage current by electron tunneling and device instability. [4, 5] To circumvent above mentioned problems, metal oxides with higher dielectric constants (*k*) than those of SiO_2 or Si_3N_4 have been investigated intensively since the same capacitance was obtained from thicker film of high-*k* materials with tunneling current reduction. It is an urgent task to find a proper high-*k* material to replace SiO_2 as the gate dielectric in order to further improve the performance of CMOS devices

High-*k* materials, such as Al_2O_3, HfO_2, ZrO_2, HfSiO, La_2O_3, $LaAlO_3$ and LaSiO have been attracted a great deal of interest as the gate dielectrics of the application to CMOSFET. [6-11] The equivalent oxide thickness (EOT) of high-*k* thin films should fall below 1 nm with the guarantee of dielectric reliability in both applications and an acceptable interface quality with Si for device working and controllability of threshold voltage are needed for the gate dielectric in the CMOSFET. [12-14]

Atomic layer deposition (ALD) is known as the most feasible and competitive process in fabrication of high quality gate dielectric thin films with conformal deposition and high

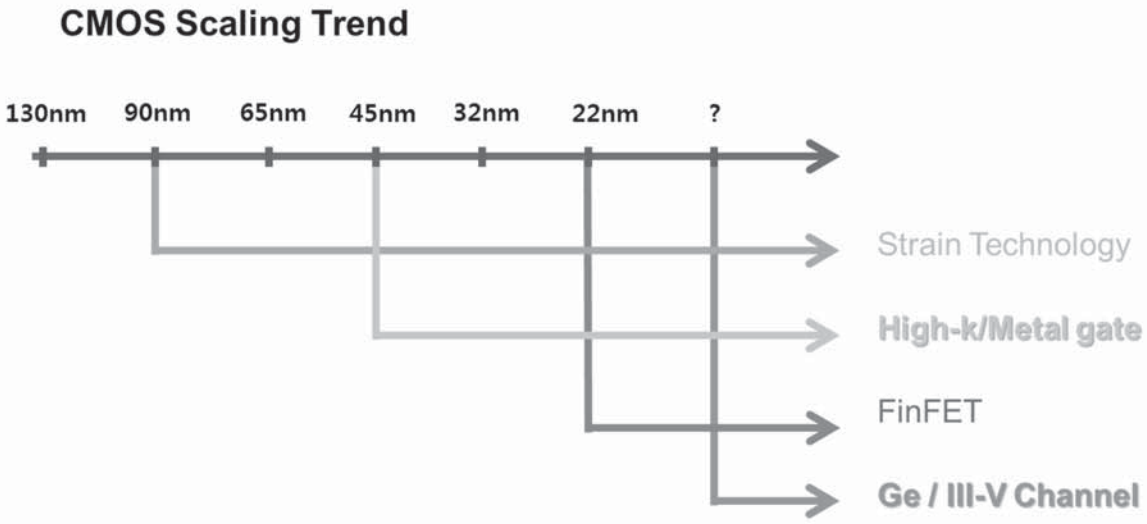


Figure 1-1. Schematic diagram of CMOS scaling trend.

accuracy in thickness control, making it excellently compatible with the semiconductor fabrication technology for mass-production. As the next generation high-*k* dielectric film as well as the threshold voltage control layer [13, 14], La_2O_3 film are attracting much attention nowadays due to their high dielectric constant (~30) [2, 15] and large conduction band offset (CBO) with Si (~2.3 eV). [2] However, ALD of La-containing films have several challenges such as the limited selection of precursors and inducement of unstable film growth due to its hygroscopic behavior. [16] Additionally, serious Si diffusion from the substrate into the La_2O_3 film during deposition has been reported. [17]

The use of Si-containing Tris[bis(trimethylsilyl)amino]lanthanum, $La[N(SiMe_3)_2]_3$, as a La precursor was reported as the promising way to intentionally incorporate Si in La_2O_3 film to prevent the diffusion of Si from Si substrates. [18] Since, significant Si diffusion during ALD of La_2O_3 film and post-deposition annealing degrades the gate controllability by increasing permittivity of the gate oxide films, the use of La-silicate film instead of La_2O_3 film is more attractive. Even though the chemical properties of ALD La-silicate films using $La[N(SiMe_3)_2]_3$ and H_2O were reported [19-22], a systematic study on the influence of the type of oxygen source, H_2O or O_3, on the growth behavior and electrical properties of La-silicate films using $La[N(SiMe_3)_2]_3$ has been rarely reported. [23]

Furthermore, the carrier injection velocity of Si-based channel is going to saturate, which determine the drive current in the devices and difficult to improve more by conventional scaling technology due to the relatively low carrier mobility of Si, thus many researches have been exploring other channel materials with high carrier mobility such as Ge or III-V compound substrate to replace Si substrate shown as Fig.1. Ge is a one of candidate to replace Si as the channel material of MOSFET for beyond 14 nm

technology nodes due to its higher electron (twice) and hole (four times) mobilities than Si. [24, 25]

Similar to SiO_2/Si in Si-MOSFET, GeO_2/Ge has been generally regarded as the most fundamental interface in Ge MOSFET. [26-29] Nonetheless, the lack of thermodynamic stability at the GeO_2/Ge interface hampers the development of Ge MOSFET. Many previous studies have demonstrated that the GeO_2/Ge interface degrades due to the GeO desorption or GeO volatilization upon thermal annealing above 420°C in vacuum or N_2 ambient owing to interfacial reaction. [28, 29] A typical example of electrical degradation by GeO desorption is very large hysteresis in the capacitance-voltage (C-V) curves which is attributed to the electrically active defects near the interface. [29]

In contrast, thermodynamic calculation shows that the GeO_2 + Ge have a lower Gibbs free energy than 2 GeO at typical processing temperature and pressure, suggesting that effective isolation of the GeO_2/Ge system from the atmosphere could suppress the adverse interfacial reaction which is called GeO proportionation. [30, 31] Considering these factors, there could be two possible solutions to solve the interfacial reaction problem; one is to adopt the capping layer, and the other is to adopt interfacial passivation (or barrier layer) to separate the GeO_2 and Ge physically. There have been many reports on the various interfacial passivation layers, such as the ultra-thin Si capping layers [32], Ge nitride interfacial layers [33, 34], AlN_x [35] and La_2O_3 dielectric interlayers [36, 37], high quality GeO_2 interfacial layer formed by plasma oxidation or high pressure oxidation. [38] Among the various passivation techniques, Si capping layer on a Ge substrate has drawn a great deal of attention due to its superior electrical performance.

Cheng et al. reported that the Si capping layer on a Ge substrate retards GeO

volatilization and suppresses the C-V hysteresis of the HfO_xN_y gate dielectric films in the MOS structure. The reduced C-V hysteresis by the Si capping layer was explained by the fact that Si-O bonds have larger Gibbs free energies and higher thermodynamic stabilities than Ge-O bonds, so that the reaction between the oxide and Ge substrate could be efficiently suppressed. [39] In most of the previous studies, Si capping layer on a Ge substrate was formed by either epitaxial growth of several mono-layers of Si or annealing in a SiH_4 (or Si_2H_4) ambient. [32] However, not much of the studies related to the ALD Si-containing passivation layers on a Ge substrate have been reported.

Houssa et al. simulated the atomic configuration of the interface between various rare-earth oxide material and Ge by first principles calculation. [40] This result gives feasibility of La_2O_3 and Al_2O_3 as effective passivation layer on Ge to suppress dangling bonds than HfO_2. Kato et al. reported an Al_2O_3 interlayer effectively suppresses the formation of a Ge oxide interlayer in a La-oxide/Al_2O_3/Ge gate stack structure. The formation of GeO_x is suppressed with increasing thickness of the Al_2O_3 interfacial layer up to 1 nm. [41] In contrast, the adoption of capping layer, which could suppress the volatilization of GeO from the GeO_2 surface, and, thus, the accompanying interfacial reaction, has not been well studied compared with the interfacial passivation layer approach.

In this study, the ALD behavior and electrical properties of La-silicate films on Si substrate according to the type of oxygen source were examined. In particular, leakage current properties depends on the changes in Si concentration of the ALD La-silicate film grown on Si substrate using the Si contained La precursor $La[N(SiMe_3)_2]_3$ were focused.

The ALD ultra-thin Al_2O_3 and SiO_2 layers were adopted as the interfacial passivation

and capping layers, respectively, for the La-silicate film on Ge substrate. During deposition of La-silicate films, $SiH_2(NC_2H_5CH_3)_2$, (BEMAS) and $SiH_2(N(C_2H_5)_2)_2$, (BDEAS) were additionally injected in order to control the Si concentrations (Si/(La+Si)) in the high-*k* film and its effect on electrical properties.

An ultrathin interfacial Al_2O_3 layers of which thickness was controlled by deposition cycles (~2, 3, 5, 10 cycles) were formed between the La-Silicate film and Ge substrate by another ALD.

Additionally, ALD SiO_2 was chosen as the material for the capping layer on La-silicate film. The multi stack of Al_2O_3 passivation, high-*k* La-silicate, and capping SiO_2 layers was effectively decreased the C-V hysteresis down to 80 mV, which is one of the best results reported up to date.

2. Literature Review

2.1. Scaling limit for Si-based gate oxide

The current gate dielectric SiO_2 thickness decreased less than 1 nm but there are several problems induced by gate dielectric oxide thickness reduction such as a high leakage current and reliability aspects. In ultrathin SiO_2 gate dielectrics, charge carriers flow through the dielectric film by direct tunneling process. [9, 10] Since the tunneling probability increases exponentially as the SiO_2 layer thickness decreased, the decrease of SiO_2 layer results in large increase of the gate leakage current.

$$I_{D,sat} = \frac{W}{L}\mu C\frac{(V_g - V_t)^2}{2} \quad (1)$$

Another issue related to SiO_2 thickness scaling concerns reliability aspects. During the operation of MOSFET in integrated circuits, charge carriers flow through the device, resulting in the generation of defects in the SiO_2 gate layer and at the Si/SiO_2 interface. [42-44] When a density of defects reaches to the critical level, breakdown (or quasi-breakdown) of the gate layer occurs, resulting in the failure of the device. [45-47] It was shown by Degraeve et al. that the time-to-breakdown distributions of ultrathin SiO_2 layers could be quite well reproduces by a percolation approach, assuming that breakdown occurred via the formation of a percolation path between defects generated during the electrical stress. [45]

The maximum gate voltage $V_{G,max}$ that can be applied to a MOSFET is presented in Fig. 2-1 as a function of the SiO_2 gate layer thickness at different temperatures and for the following specifications [ref 14]: gate dielectric lifetime fixed at 10 years, failure rate

fixed at 0.01% and chip area of 0.1 cm^2. These curves (solid line in Fig. 2-1) were obtained from extrapolations of time-dependent dielectric breakdown measurements performed at high stress voltages, according to gate voltage, failure percentile and area scaling laws. [45, 48]

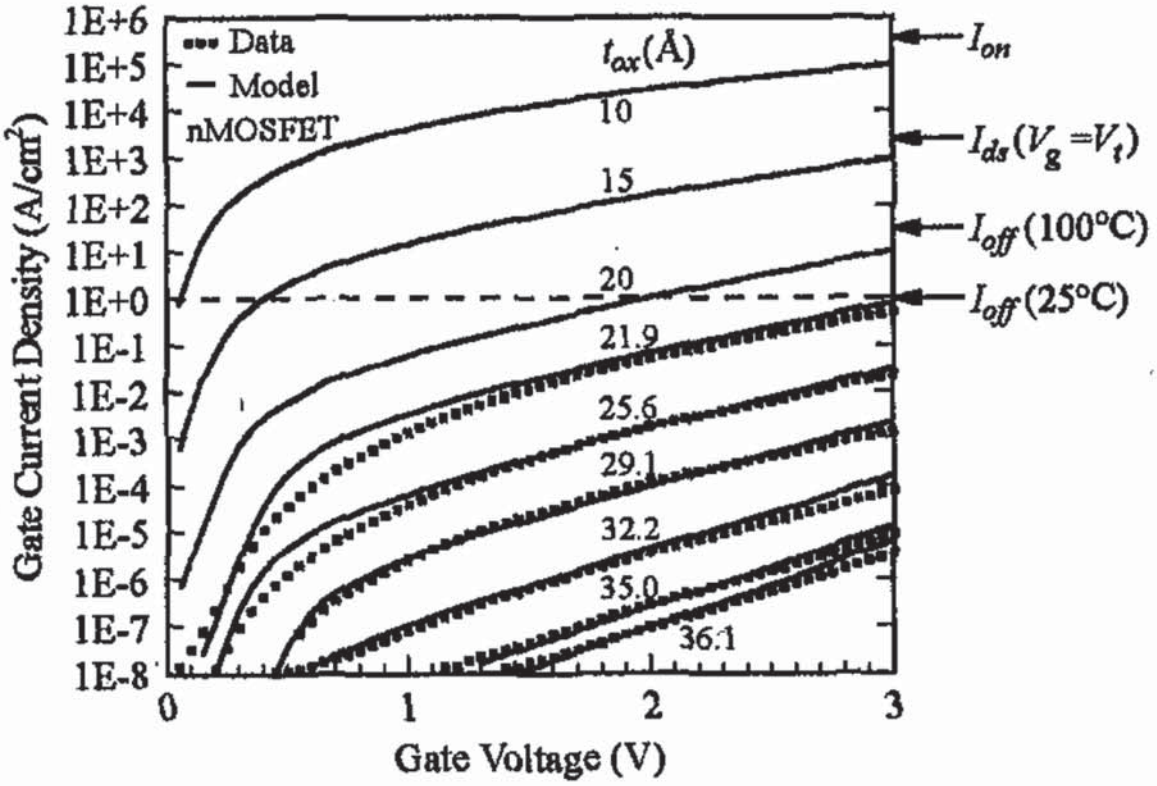


Figure 2-1. Measured and calculated oxide. Tunneling current versus Gate voltage for different oxide thicknesses.

2.2. High-*k* gate dielectric

2.2.1. Necessity for high-*k* dielectric

In the case of increasing the gate capacitance, consider a parallel plate capacitor,

$$C = \kappa\varepsilon_0 \frac{A}{t} \qquad (2)$$

where k is the dielectric constant of the material, ε_0 is the permittivity of free space (= 8.85 X 10^{-14} F/cm), A is the area of the capacitor, and t is the thickness of the dielectric. This expression for C can be rewritten in terms of capacitance equivalent oxide thickness (CET) and k_{ox} (= 3.9, dielectric constant of SiO_2) of the capacitor. The term CET represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric. The physical thickness of an alternative dielectric employed to achieve the equivalent thickness of CET = 1 nm can be obtained from the simple expression,

$$t_{high-k} = \frac{\kappa_{high-k}}{3.9} CET \qquad (3)$$

A dielectric with a relative permittivity of 16 therefore affords a physical thickness of ~ 4 nm to obtain CET = 1 nm.

Interface engineering schemes have been developed to form oxynitrides and oxide/nitride reaction barriers between these high-*k* metal oxide materials and Si in an attempt to prevent or at least minimize reaction with the underlying Si. The passivating properties of such reaction barriers are widely reported. [49] In most cases, this amounts to further scaling the approaches used to form oxynitrides, discussed in the previous

section. These barrier layers have been shown to reduce the extent of reaction between the high-*k* dielectric and Si, as well as to help maintain high channel carrier mobility.

It is important to note, however, that using an interfacial layer of SiO_2 or another low permittivity material, will limit the highest possible gate stack capacitance, or equivalently, the lowest achievable t_{ox} value. In addition, the increased process complexity for the deposition and control of additional ultrathin dielectric layers, as well as scalability to later technology nodes, remains a concern. This effect of reduced capacitance can be seen by noting that when the structure contains several dielectrics in series, the lowest capacitance layer will dominate the overall capacitance and also set a limit on the minimum achievable t_{ox} value. For example, the total capacitance of two dielectrics in series is given by

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2} \tag{4}$$

where C_1 and C_2 are the capacitances of the two layers, respectively. If one considers a dielectric stack structure such that the bottom layer (layer 1) of the stack is SiO_2, and the top layer (layer 2) is the high-*k* alternative gate dielectric, Eq. (4) is simplified (assuming equal areas) to

$$t_{eq} = t_{SiO_2} + \frac{k_{ox}}{k_{high-k}} t_{high-k} \tag{5}$$

It is clear from Eq. (5) that the minimum achievable equivalent oxide thickness [defined as t_{ox} in Eq. (5)] will never be less than that of the lower-*k* (in this case pure SiO_2) layer. Therefore, much of the expected increase in the gate capacitance associated with the high-*k* dielectric is compromised. The implications of current transport through such

stacked structures will be considered further later.

2.2.2. La-based oxide films

Lanthanum oxide (La_2O_3) is considered as a promising material which can offer better dielectric performance than Hf-based materials due to its larger conduction band offset (~ 2.3 eV) although it has a marginally higher dielectric constant (~ 30). [2, 3, 50, 51] Table 2-1 and table 2-2 shows comparison of relevant properties for high-*k* candidates. Yeo et al. simulated the theoretical direct tunneling current densities modeled by semi-empirical equation. [51] La_2O_3 films are attracting much attention nowadays as the next generation high-*k* dielectric film as well as the threshold voltage control layer. [9, 10] Figure 2-2 shows the gate current density at a fixed V_G as a function of t_{ox}. La_2O_3 film shows lowest current density at same EOT. This theoretical value was calculated considering dielectric constant, effective electron mass and barrier height, thus the leakage current characteristic of La_2O_3 film is attribute to large conduction band offset and dielectric constant. [51]

Table 2-1. Conduction band offset to conduction band of Si (Φ_b), tunneling effective masses (m_{eff}), and relative permittivities (k) for several gate dielectrics. [2]

Material: Tunneling mechanism[b]	La_2O_3	Al_2O_3	HfO_2	JVD-Si_3N_4	RPN[f]-SiON	SiO_2
	ECB	ECB	ECB	HVB	ECB	ECB
Φ_b (eV)	2.30[c]	2.80[c]	1.13[d]	1.90[e]	3.04[f]	3.10
m_{eff} (m_0)	0.26	0.35	0.17	0.41[e]	0.21	0.40
α[g]	0.1	0.6	0.8	1.0[e]	0.4	0.6
κ	27	10	24	7	5.08[f]	3.9

Table 2-2. Electric characteristics of La_2O_3 and HfO_2, dielectric constant (k), bandgap (E_g), conduction band offset (CBO), merits and drawbacks.

Dielectric	k	Eg	CBO	merits	Drawbacks
La_2O_3	~27	5.8	2.3	Higher-k Large conduction band offset	Moisture absorption
HfO_2	~20	5.6~5.7	1.3~1.5	Most suitable compare to other candidates	crystallization, silicate and silicide formation

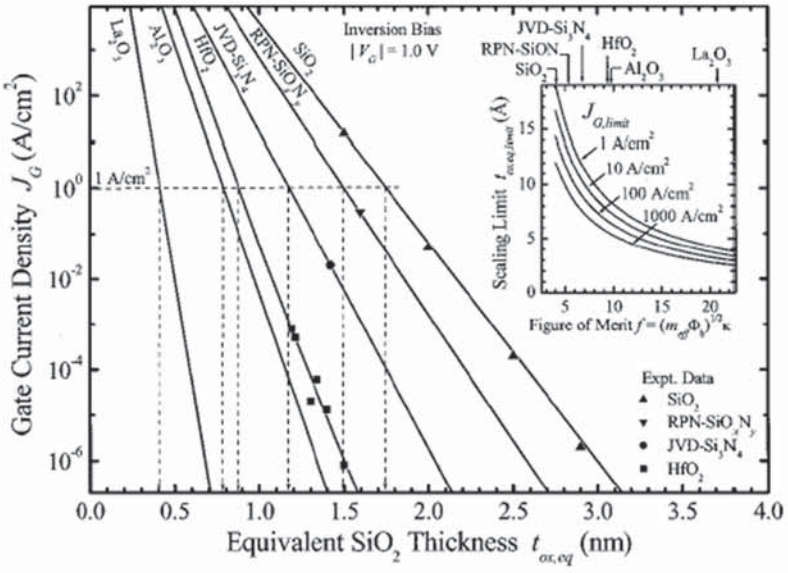


Figure 2-2. Gate current density J_G at a fixed inversion gate bias as a function of the equivalent oxide thickness $t_{ox,eq}$ for five different gate dielectrics. Solid lines are from the model, Extraction of gate dielectric scaling limits is also shown based on a maximum tolerable gate leakage J_{Glimit} of 1 A/cm^2 and the supply voltage V_{DD} of 1 V. Scaling limits as a function of the gate dielectric figure of merit is described in the inset. [51]

2.3. High mobility channel Ge

As the aggressive scaling of Si-based complementary metal-oxide semiconductors (CMOS) approaches the fundamental limit, various attempts such as modified channel materials have been investigated in attempts to improve device performance by enhancing the carrier mobility in the channel region. One possible modification of the channel region being considered at present involves replacing the conventionally used Si by alternative semiconductor materials such as Ge and III-V compound semiconductors. Ge or III-V compound substrate has been considered as a promising candidate as channel material for future technology nodes because of its lower effective conductivity mass. Large drive current is highly favorable for applications, because it determines the switch time of CMOS devices, which is believed to be limited by the velocity of carrier injection from the source into the channel in short channel devices. [52] One way of increasing the drive current is the conventional scaling technology. However, as mentioned previously, this Si-based dimension shrinkage is approaching its limitation, and high-*k* dielectrics are needed for further scaling. It was reported that Ge substrate has two times higher electron mobility and four times higher hole mobilities compared to the Si substrate. [27, 40] Therefore, the higher mobility as well as smaller band gap of Ge as a channel material has advantages owing to the improvement in injection current density and the scaling of the supply voltage, which results in high speeds and a low power consumption. The replacement of the conventional channel material Si with a higher carrier mobility channel material like Ge can also allow for further improvement of the drive current.

The integration of high-*k* dielectrics on Ge-FET Scaling technology plays important roles for further improving the performance and reducing costs of CMOS devices,

together with the replacement of Si substrate with high mobility channel materials such as Ge substrate. Since further scaling caused large tunneling current in Si-based devices is due to the relative smaller dielectric constant of SiO_2 ($k > 3.9$), a new insulating material with high-k is highly desirable for Ge-based CMOSFET.

Ge-FET has attracted much attention due to their excellent electrical properties. Ge substrate has higher carrier mobility compared with Si substrate. The low-field electron mobility in Ge is more than double that of Si (3900 vs. 1500 cm^2/V-sec) and the increase is four-fold for holes (1900 vs. 450 cm^2/V-sec). [24, 25] This advantage makes Ge attractive for high speed circuit applications. The mobility of electron and hole is also more symmetric in Ge than in Si, and this means that the area of *p*-MOSFET can be reduced, and allow for more CMOS logic gates to be integrated in one unit clip.

As a part of mobility compensation scheme, the replacement of Ge substrate has lots of merits. However, it also induce the increase of reverse current density of a pn-junction in Ge. Table 2-3 summarized the characteristics of several potential channel materials at 300 K. Compared to the other Group IV and III-V semiconductor materials, the bulk hole mobility of Ge shows the highest values. Furthermore, the much lower melting point of Ge indicates that it is possible to fabricate Ge-based transistors with lower thermal budget processes, and requirements for thermal stability can be relaxed to some extent to integrate novel materials like metal gate electrode and high-k dielectrics into advanced transistors. [53, 54] In comparison with Si, Ge has as smaller band gap, which is related to a smaller supply voltage in applications. This is more compatible with the trend of scaling of the supply voltage as specified in ITRS. [3] The electrical performance of Ge *n*-MOSFET, and electrically active carrier concentration in the *n*-type diffusion layer is at

present not enough to reach the level required for the 14 nm node in the ITRS. Therefore, it may be useful to investigate the feasibility of III-V MOSFETs because bulk electron mobility in most III-V materials is higher than in Ge.

Besides, it is possible to realize the systematical integration of electronic, microwave, and photonic devices on Ge-based technology, since Ge has a small lattice mismatch with GaAs photonic material. The fact that the lattice constant of Ge is close to that of GaAs is expected to facilitate integration of III-V *n*-MOSFET and optical devices on Ge substrates in the future. Despite the above advantages of using Ge-based technology, Ge has not established a strong presence as an electronic material for ubiquitous microelectronic applications because it does not have a stable gate dielectric, which is critical for gate stacks formation.

Although Ge has the excellent properties, the lack of a stable passivation oxide and the necessity of a lower temperature process have hindered the fabrication of Ge-based devices. Ge has lower thermal stability, it starts to melt at 938°C, which sets the maximum temperature that can be used in a Ge containing process. In addition, Ge is easily oxidized in various environments and form an oxide layer consisting of a mixture of mainly mono oxide (GeO) and dioxide (GeO_2) species. Material characteristics of Ge oxide and Si oxide are summarized in Table 2-4. GeO_2 is a polymorph, and the characteristics of GeO_2 obviously depend on the oxidation state and crystallinity. GeO_2 is transformed from hexagonal phase to tetragonal phase at 1033°C by annealing. Since hexagonal or amorphous GeO_2 is a major phase at room temperature, GeO_2 is soluble in water. In contrast, GeO(s) is insoluble. The most important reaction is GeO_2 + Ge → 2 GeO (s) or 2 GeO (g), which indicates that GeO_2 consumes Ge at the interface. Moreover,

GeO_2 on Ge not only decomposes into GeO(s) but also desorbs as gas-phase GeO(g). In other words, the narture of the interface between the Ge oxide and Ge substrate gives a decrease in the desorption temperature. Since GeO(g) has the nature of a reducing agent, this reaction can degrade the electrical properties of a high-*k*/Ge gate stack. Since the dielectric constant of Ge oxide is as low as 6, complete absence of Ge oxide at the high-*k*/Ge interface is likely to be necessary in achieving a thin equivalnet oxide thickness (EOT) below 0.5 nm, as required in the ITRS. [3] One of the effective methods to decrease the amount of Ge oxide prior to high-*k* film deposition on the Ge substrate is HF pretreatment. However, a certain amount of Ge suboxide (GeO_x, $x < 2$) remains even after the pretreatment.

Therefore, how to passivate Ge surface is one of the most important issues for fabricating high performance Ge-FET. Intensive studies have been carried out to find an appropriate passivation material for Ge surface. Many different passivation methods have been proposed such as oxidation, hydrogen (H), sulfur (S), and Fluorine (F) passivation, and nitridation.

Table 2-3. The characteristics of several potential channel materials at 300 K.

	Ge	Si	GaAs	InSb	InP
Bandgap, E_g(eV)	0.66	1.12	1.42	0.17	1.35
Electron affinity, χ(eV)	4.05	4.0	4.07	4.59	4.38
Hole mobility, μ_h($cm^2V^{-1}s^{-1}$)	1900	450	400	1250	150
Electron mobility, μ_e($cm^2V^{-1}s^{-1}$)	3900	1500	8500	80 000	4600
Effective density of states in valence band, N_V(cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}	7.3×10^{18}	1.1×10^{19}
Effective density of states in conduction band, N_C(cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	4.2×10^{16}	5.7×10^{17}
Lattice constant, a(nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant, k	16.0	11.9	13.1	17.7	12.4
Melting point, T_m(°C)	937	1412	1240	527	1060

Table 2-4. Material characteristics of Ge oxide and Si oxide.

	GeO	GeO_2			SiO_2
Crystallinity	Amorphous	Hexagonal	Tetragonal	Amorphous	Amorphous
Dielectric constant	–	7	12	–	3.9
Solubility (g/100g H_2O)	insoluble	0.453 @25°C	0.00023 @25°C	0.5184 @30°C	insoluble
Density (g/cm^3)	–	4.228	6.239	3.637	2.2
Transition temperature (°C)	–	1033	1033	–	867
Melting point (°C)	710	1116	1116	–	~1600
Sublimation Temperature (°C)	700	–	–	–	–

2.3.1. Desorption and disproportionation characteristics of Ge oxide

The GeO desorption mechanism was researched by Toriumi groups. [26, 29, 55] In order to investigate GeO desorption, GeO_2 films were deposited by sputtering system, and the changes in the thickness of sputtered-GeO_2 films after annealing were addressed as shown in Fig. 2-3 (a). There was no GeO_2 thickness change on the Ge substrate until ~ 400°C, but the GeO_2 thickness decreases significantly at 400 to 600°C. However, the GeO_2 thickness on a thermally oxidized Si substrate shows the negligible change even at temperatures at 700°C. These results indicate that the GeO desorption over 400°C is mainly due to the interface reaction at GeO_2/Ge. The schematic was also shown in Fig. 2-3 (b).

The diffusion species generation at the interface at the GeO_2/Ge substrate causes the gradient of diffusion species concentration from the interface to the surface. Redox reaction at GeO_2/Ge interface generates diffusion species at the interface, which triggers Ge atoms or ions or oxygen vacancy (V_o) diffusion in film. Diffusion of Ge or V_o in GeO_2 will causes a Ge rich or oxygen poor region at the GeO_2 surface, where volatile GeO is generated, which was schematically shown in Fig. 2-4.

On the basis of comparing GeO desorption in GeO_2/Ge and GeO_2/SiO_2/ Si stacks, S. K. Wang et al. suggested there is a reversible reaction called GeO proportionation at the GeO_2/Ge interface. [56] Thermodynamic calculation shows that the GeO_2 + Ge have a lower Gibbs free energy than 2 GeO at typical processing temperature and pressure (disproportionation reaction of GeO_2 + Ge → 2 GeO has a positive Gibbs free energy change), suggesting that effective isolation of the GeO_2/Ge system from the atmosphere could suppress the adverse interfacial reaction. The result of XPS Ge 3*d* spectra as a

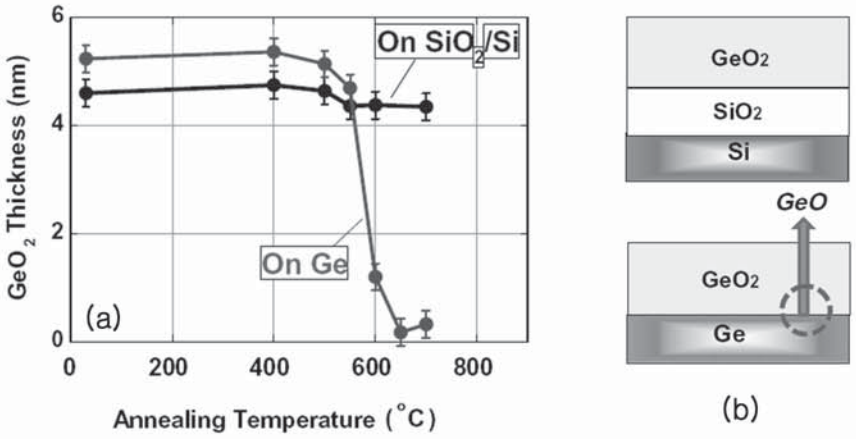


Figure 2-3. (a) GeO_2 thickness changes on Ge and on SiO_2/Si as a function of annealing temperature and (b) Schematic view of GeO desorption in GeO_2/SiO_2/Si stack vs. GeO_2/Ge stack. [55]

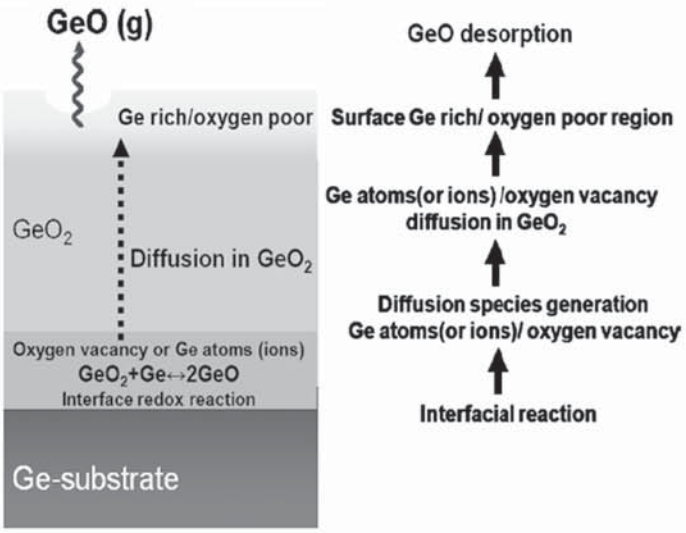


Figure 2-4. Schematics of GeO desorption mechanism from GeO_2/Ge stacks. [56]

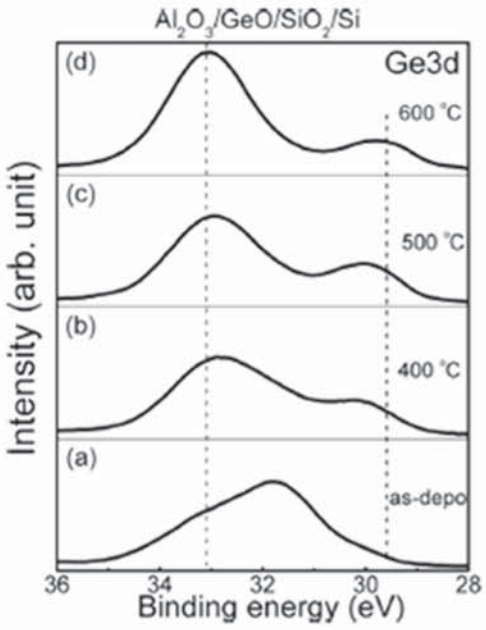


Figure 2-5. XPSpectra Ge 3*d* peak core spectra for Ge disproportionation effect for GeO generate GeO_2 + Ge in terms of annealing temperature. [30, 31]

function of annealing temperature is shown on Fig. 2-5.

The comparision of the thermal decomposition pathway for a ultrathin oxide layer on surface of Ge (100) and Si (100) substrate was also reported. [28] Figures 2-6 (a) and (b) shows Ge 3*d* and Si 2*p* spectra as a function of temperature for the ultra thin oxide layers on the Ge and Si surface, respectively. As-prepared oxide layer consists of a mixture of oxides (sub oxides) and dioxides, on both the surfaces. The oxide layers decompose and desorb as monoxides. However, the decomposition pathways are different from each other. On annealing of Ge oxides, GeO_2 species transform to GeO and remain at the surface and desorb at about 420°C, and complete desorption was took place at 430°C, leading to the formation of a clean surface. In contrast, annealing of Si oxides results in the transformation of SiO to SiO_2 up to temperatures of about 780°C close to the desorption. At high temperatures auch as above 700 to 800°C, SiO_2 decomposes and desorbs, implying a reverse transformation to volatile SiO species.

The effect of GeO desorption on C-V characteristics were widely reported. [26, 55] Figure 2-7 shows the bidirectional C-V characteristics of sputter deoposited GeO_2 metal oxide semiconductor capasitors (MOSCAP) on Ge, Si, and thermally oxidized Si substrates, fabricated by a conventional PDA at 600°C. The capacitor fabricated on the Ge substrate shows the characteristics of huge hysteresis and stretch-out, while quite good electric characteristics are obtained from the capacitors on Si and SiO_2/Si substrates. It is believed that the deterioration of the C-V characteristics of the GeO_2/Ge MOSCAP originated from the interface reaction to drive GeO volatilization. This suggest that GeO desorption should leave huge amount of interface states density or traps at the interface. These C-V distortion was also observed when ALD-HfO_2 was deposited onto the Ge

substrate.

Figure 2-8 shows large C-V hysteresis was observed for $HfO_2/GeO_2/p$-Ge [28], which can be explained by the fact that oxidant during the initial ALD cycles may induce an intermixing reaction with the uncovered Ge surface and the adsorbed Hf pecursors before the formation of a continuous HfO_2 film, which resulted in a non-uniform interface and more intermixing between HfO_2 and Ge substrate, and occured large C-V hysteresis.

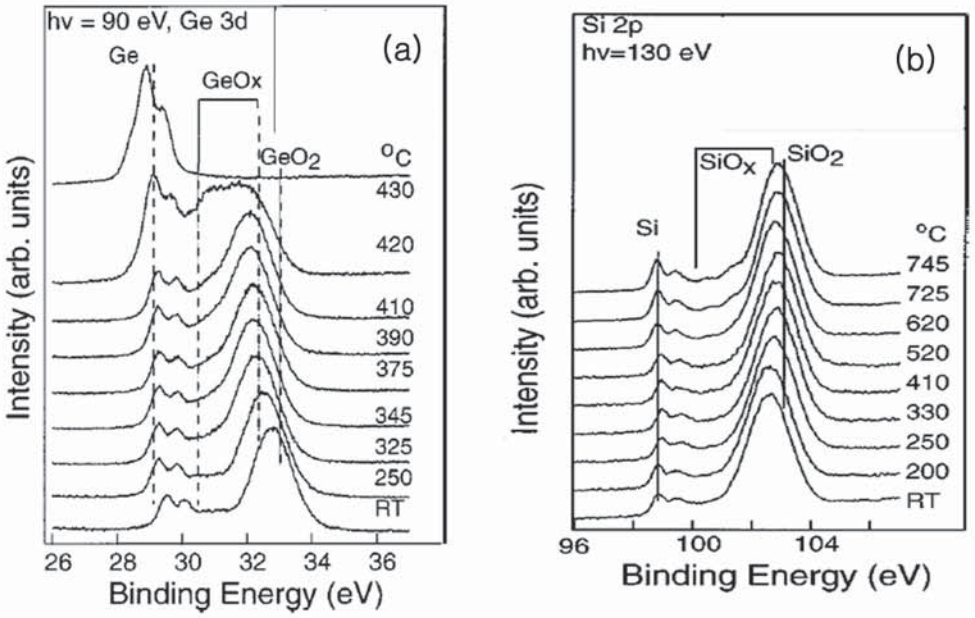


Figure 2-6. XPSpectra of (a) Ge 3*d* and (b) Si 2*p* core level spectra as a function of annealing temperature for the ultra thin oxide layers on the Ge and Si surface, respectively. [28]

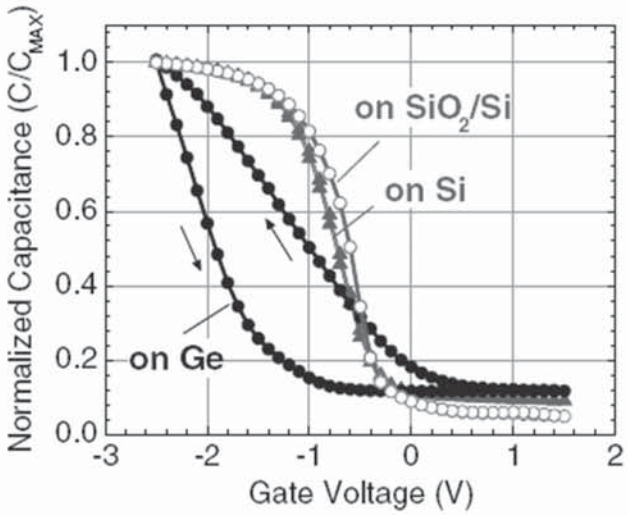


Figure 2-7. Bidirectional C-V characteristics of GeO_2 MOSCAP on Ge, Si, and thermally oxidized Si substrates, fabricated by a conventional PDA treatment at 600°C. [55]

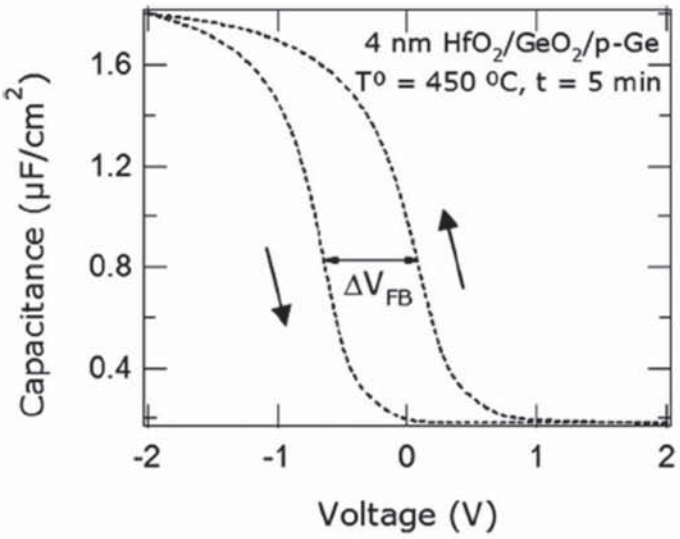


Figure 2-8. Large C-V hysteresis for $HfO_2/GeO_2/p$-Ge. [28]

2.3.2. Introduction for Ge Passivation Techniques

Due to aggressive down-scaling of the MOSFET devices, the introduction of alternative substrate materials such as Ge is necessary. High carrier mobilities and a low dopant activation temperature are the main advantages of Ge substrates compared to Si substrate. Despite of the successful realization of Ge based MOSFET and numerous improvements, the device performance reported still below theoretical predictions, mainly due to insufficient Ge oxide interface passivation. Therefore several capable approaches for Ge surface passivation techniques have been reported.

Various passivation techniques have attracted attention for the Ge interface passivation. Some studies have been carried out to explore the use of hydrogen (H) to passivate Ge surface. [57-59] H terminated Ge surface exhibits oxide free surface [59], but the surface is rough and unstable when exposed to the ambient. [58, 60] Some researchers studied the electrical properties of sulfur (S) passivated Ge surface. [61, 62] Frank et al. reported that $HfO_2/GeO_xS_y/Ge$ stacks exhibit lower fixed charge and interface state density than conventional HfO_2/GeO_xS_y /Ge stacks. [61] Xie et al. further found that the S passivated Ge surface can improve thermal stability of HfO_2/GeO_xS_y /Ge stacks while maintaining the low gate leakage current. [63] Some studies also used Chloride (Cl) [60, 64, 65] and fluorine (F) [66, 67] as Ge interface passivation. Lu et al. reported that Cl terminated Ge surface is stable, but that Cl cannot passivate Ge surface effectively, and some oxygen or carbon will be incorporated on the surface. [64] For F passivated Ge surface, Lee et al. showed that the interface defect states at HfO_2/Ge interface can be effectively passivated by F incorporation. [67] Xie et al. reported that Ge-based MOS structures incorporated with F exhibit good electrical properties and low interface state density. [66, 68] In

addition, Ba passivation [69], As passivation [70] and Si thin passivation layer [71] have been proposed to Ge passivation techniques.

However, a good quality interface layer is required before the deposition of a high-*k* dielectric. Hole mobility above 300 cm^2 V^{-1} s^{-1} was demonstrated for Ge PMOS with GeON passivation. Ge NMOS exhibited poor drive current and low mobility both in our experiments and by several demonstrations worldwide. [72-75] Better characterization and understanding of interface traps can be helpful to investigate Ge NMOS problem. An interfacial passivation layer with low interface state density and good electrical quality is required before the deposition of a high-*k* dielectric to improve PMOS performance and to solve Ge NMOS problem.

Ge interface passivation has been a critical challenge. Direct deposition of a high-*k* dielectric on Ge has exhibited poor electrical characteristics. Many attempts have been made with different high-*k* materials including HfO_2 [33], ZrO_2 [76], Al_2O_3 [74] and $LaAlO_3$ [75] to find a suitable dielectric materials for Ge.

2.3.3. Oxidation treatment

Among several passivation methods, oxidation, nitridation or their combination GeO_xN_y has attracted much more interest because they are compatible to current fabrication processes. In contrast, extensive applications of SiO_2 in Si based technology; Ge oxides have not received much attention as gate dielectrics for Ge based MOS devices because they were thought thermally and chemically instable previously. [77] More recently, attention has been paid gradually on using GeO_2 to passivate Ge surface due to the fact of the unavoidable formation of GeO_x during growth of high-*k* oxides on Ge surface directly. [78-85] Various oxidation processes have been proposed. [79-81, 83-85] Some papers reported that GeO_2 can also acts as a promising electrical passivation layers for high-*k* gate dielectric deposited by the ALD. However large C-V hysteresis was observed for the HfO_2 or ZrO_2 gate stacks by using thermally grown GeO_2 passivation layers [86, 87], recently, a high quality of GeO_2 was obtained by using high pressure oxidation (HPO) and oxygen plasma oxidation. [78, 88] C. H. Lee et al. reported that the HPO of Ge, in terms of controlling the Ge desorption, and demonstrated the significant improvement in electical properties of GeO_2/Ge MOSCAP. [38, 88] Although GeO_2 in this paper was not used as the passivation layers, it was addressed that GeO desortion from GeO_2/Ge stacks could be efficiently suppressed HPO. Figure 2-9 shows C-V curves of Au/GeO_2/*p*-Ge structure. GeO_2 grown by atmosperic pressure oxidation shows large amounts of C-V hysteresis, which means the huge amount of interface and bulk traps, while in the case of GeO_2 grown by HPO shows significant reduction of C-V hysteresis and frequency dispersion. Therefore calcurated interface state density of Au/GeO_2/*p*-Ge was 2 x 10^{11} eV^{-1} cm^{-2}. This means GeO_2 grown by high pressure oxidation can be used

for the passivation layer between high-*k* gate dielectrics and Ge substrate.

Afanas'ev et al. reported that Ge oxide layers were formed when using ALD to grow HfO_2 on Ge, and found that the band alignment at GeO_x/Ge (001) interface determined by internal photoemission (IPE) spectroscopy is large enough to minimize possible carrier tunneling. [79, 84] Molle et al. compared three oxidation processes, and showed that a large percentage (~ 98 %) of GeO_2 in GeO_x layer was formed using atomic oxygen source at 300°C. [80] Delabie et al. used pure O_2 to oxide Ge surface in the atmospheric pressure at 350°C, and found that GeO_2 passivated Ge MOS structures showed well-behaved C-V characteristics. [81] Matsubara et al. reported thermally oxidized Ge surface using pure O_2 at the atmospheric pressure, and found a low interface trap density in GeO_2/Ge MOS structures, with the minimum trap density that is lower than ~ 10^{11} cm^2 eV^{-1} at 575°C. [85]

Q. Xie et al. reported that C-V hysteresis was substantially reduced from 900 to 50 mV for the HfO_2/Ge gate stacks by using in situ O_2 plasma passivation. [78] Figure 2-10 shows C-V hysteresis characteristics for the Pt/HfO_2/GeO_2/*p*-Ge MOSCAP without and with surface passivation. Very large C-V hysteresis (~ 900 mV) was observed for the sample without surface passivation independent of the measured frequency, while O_2 plasma pretreated sample shows much narrower hysteresis (~ 50 mV) was obtained although the HfO_2 deposition process is similar when compared to the MOSCAP without passivation. The reduction of C-V hysteresis was explained by the more uniform and stable GeO_2 interfacial layer created by O_2 plasma treatment when it is conducted directly prior to the ALD process. For the MOSCAP without O_2 plasma pretreatment, the O_2 plasma during the initial ALD cycles may induce an intermixing reaction with the uncovered Ge surface and also the adsorbed Hf metal precursors before the formation of a

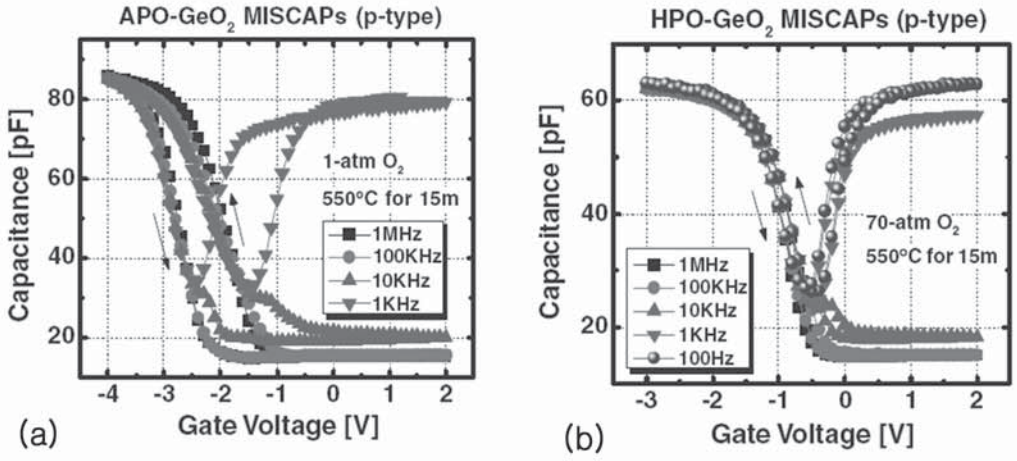


Figure 2-9. Bidirectional C-V curves of Au/GeO_2/p-Ge MOS capacitor, where GeO_2 was grown by atmosperic pressure oxidation and high pressure oxidation at 550°C for 15min. [88]

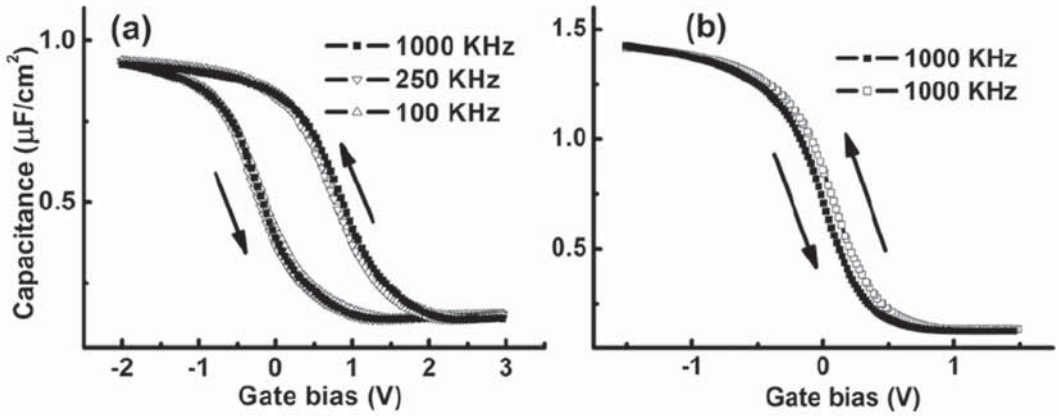


Figure 2-10. C-V hysteresis of HfO_2/*p*-Ge (100) gate stack with Pt as top electrode: (a) without O_2 plasma passivation and (b) with O_2 plasma passivation. [78]

continuous HfO_2 film. This results in a nonuniform interface and more intermixing between HfO_2 and Ge substrate and, therefore, a larger C-V hysteresis.

Afanas'ev et al. studied electronic properties of GeO_x/Ge stack, and noted that the band gap of Ge sub oxide is significantly lower than that of GeO_2, resulting in an insufficient barrier height to block carrier tunneling. [84] Although GeO_2 has been extensively studied, there are still some issues remain. For example, the growth of good quality of GeO_2 is still challenging, which is of importance for applications since the electronic properties of GeO_x is dependent on its oxidation states. Moreover, the value of valance band offset (VBO) obtained by Afanas'ev et al. using IPS [79, 84] is much smaller than that determined by XPS directly [83], and the mechanism has not been well studied yet.

2.3.4. Nitridation

GeON has been widely used to passivate germanium and fabricate MOSFETs. [72, 73, 89-92] The advantage of GeON over Ge oxides is the improved chemical and thermal stability. Nitrogen can be incorporated by either thermal [72] or plasma nitridation. [90, 93] However, it was shown that interface state density was high and MOSFET had mobility degradation due to Coulomb scattering. [94] Interface state density above ~ 10^{12} cm^{-2} eV^{-1} and even as high as ~ 10^{13} cm^{-2} eV^{-1} of GeON was measured using *n*- and *p*-type Ge substrate. Nitrogen incorporation in GeON films was less than 30%. Figure 2-11 shows that forming gas annealing helps to reduce interface state density. However, the effect of H passivation seems to be minor compared to the H passivation of Si dangling bonds, widely used in CMOS technology.

Ge_3N_4 has been studied as a promising alternative surface passivation material for Ge-FET due to its excellent mechanical, thermal, and electronic properties. [95] For examples, Van Elshocht et al. found Ge MOS structures with surface pretreatments in NH_3 ambient may result in smoother films with strongly reduced diffusion of Ge in the HfO_2 film, and this also leads to a much better electrical performance. [96] Maeda et al. used plasma N source to nitride Ge surface, and fabricated MOS structures with a smooth interface layer and good electrical properties. [97] Nitridation processes with atomic N source have also been proposed. Maeda et al. reported a method for growing high quality Ge_3N_4 on Ge surface using atomic N source at low temperature. [98]

In a later study, they also fabricated a Ge-MOS structure with Ge_3N_4 as the gate dielectrics, and found that the interface trap density is as low as 1.8 x 10^{11} cm^{-2} eV^{-1}. [92] Furthermore, Wang et al. investigated nitrided Ge surface using atomic N source also, and

determined the band alignments and thermal stability of Ge_3N_4/Ge (001) interface using XPS measurement. [99] Besides, Lieten et al. found that mono-crystalline Ge_3N_4 can be formed on Ge (111) surface using plasma N source at atmospheric pressure at 800°C, and it has high thermal stability. [100]

However, although many researches have been carried on the possibility of using Ge_3N_4 to passivate Ge surface, the studies on electronic properties of Ge_3N_4 are still limited, and the optical dielectric and intrinsic defect properties of Ge_3N_4 have not been well understood yet. Moreover, it is highly favorable to obtain more information about the interface properties of Ge_3N_4/Ge such as atomic interface structures, interface stability, and band alignments.

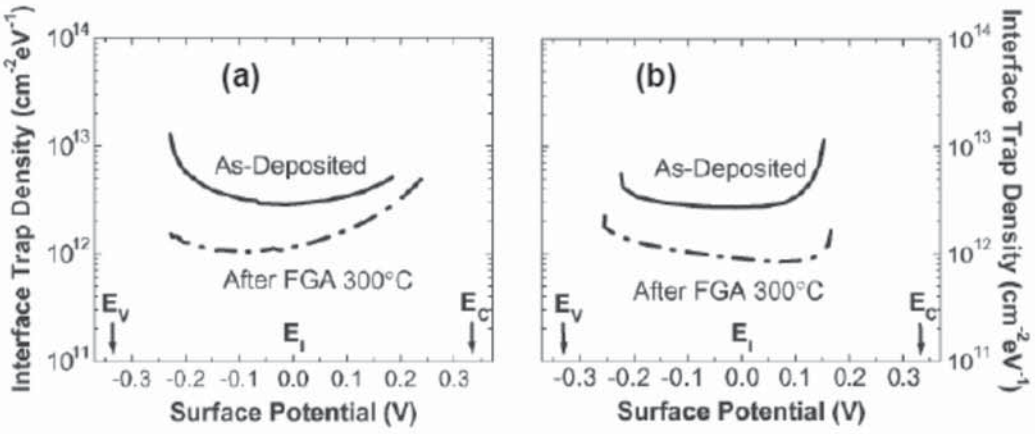


Figure 2-11. Interface state density of GeON films extracted by quasi C-V techniques with and without F.G. annealing treatment at 300 °C **(a)** *p*-type **(b)** *n*-type Ge substrates. [94]

2.3.5. Direct Deposition of high-*k* Dielectrics

High-*k* dielectrics have been under research in the last two decades to replace SiO_2 in CMOS technology. Significant progress has been made to improve the electrical quality of high-*k* dielectrics by academia and industry. In early 2007, Intel announced the deployment of Hf-based high-*k* dielectrics in conjunction with a metallic gate for components built on 45 nm Si CMOS technology node. A broad range of high-*k* dielectrics have also been tried on Ge to find a suitable gate dielectric for CMOS applications. Rare earth oxides also pay attention to the good passivation layers of Ge devices because these oxides has compatibility with Ge, which produce well behaving Ge device characteristics. A possible reason for this behavior is that rare earth oxides react strongly with the substrate resulting in catalytic oxidation of Ge and in the spontaneous formation of stable interfacial layers. [101] HfO_2 [33], ZrO_2 [102], Al_2O_3 [74] and $LaAlO_3$ [75] were deposited directly on Ge substrate after chemical cleaning. Native oxide was removed from Ge surface mostly by DI water or HF, or a repetitive application of both. MOS capacitor results show that interface state density is high and gate leakage is prominent for those devices. Besides, Ge MOSFET with the gate stacks of high-*k* dielectric directly deposited on Ge exhibits even lower mobilities than Si MOSFET. Thus, with thicker physical thickness for the same EOT, high-*k* materials can reduce leakage current flowing from devices greatly. Similar to the requirements of its integration on Si-based FETs, however, the alternative high- *k* material on Ge FET should also have to satisfy thermal stability, large band gap (E_g), CBO, VBO and low D_{it}.

Based on these requirements, intensive studies have been carried out to find the appropriate high-*k* materials either in amorphous or epitaxial growth on Ge substrate.

Amorphous high-*k* dielectrics are favorable because they are isotropic and can avoid grain boundaries at the interface with substrate. The grain boundary at the interface is believed to be the current tunneling path, which can lead to larger leakage current in devices. Various amorphous high-*k* dielectrics such as HfO_2 [103, 104], ZrO_2 [102, 105, 106], and Al_2O_3 [107] have been grown on Ge by using different methods, and their electrical properties were studied. One of the candidate for the rare earth oixde is CeO_2 [104, 105], CeO_2 reduces the density of states to ~ $10^{12}\,cm^{-2}\,eV^{-1}$ or below. However, it suffers from high leakage due to the low energy gap of CeO_2 (~ 3.3 eV) and its scalability to low EOT values. It was reported that HfO_2 on CeO_2 passivating layer can overcome leakage current issues. [102, 106] Gd_2O_3 also has attracted interest mainly because it can be grown in crystalline form on Ge with abrupt interfaces. [102] However, there is not enough evidence at the moment about its dielectric quality and its suitability as a gate dielectric for Ge devices. It was found that the leading high-*k* dielectric in Si substrate, HfO_2, is not suitable for Ge substrate directly, because it can react with Ge substrate, and form Germanide, which is unstable and would lead to the large leakage current in devices. [103, 108] In contrast, although Zr-related high-*k* dielectrics were screened as gate dielectrics on Si-based FET due to the fact that they would react with Si to form unstable Silicides, Ge-MOS structures with Zr-related high-*k* dielectrics exhibit good electrical properties [105, 109], and there is no interfacial layer at ZrO_2/Ge interface. [110] Moreover, it is noted that that gate dielectrics on Ge that have good electrical performance are GeON [33, 34], GeAlON [35], GeZrO [76], and GeZrSiO [111].

However, the formation of Ge oxides during the annealing process is a serious problem for integrating amorphous high-*k* oxides on Ge substrate directly due to the thermal

instability of Ge oxides [77], although it was found that they can be slightly reduced with incorporated Al into high-*k* oxides during the growth process. [112] Ge might diffuse into high-*k* oxides, which would also lead to interior interface properties. [113] In addition, La_2O_3 on Ge is also an alternative route to obtain good passivation and nearly ideal C-V characteristics although the reason for this good behavior is not understood at present. [114, 115] Houssa et al. reported the structural and electronic porpoerties of $Ge(M)O_2/Ge$ interface, with M = Al, La or Hf, using density function theory. [36] Table 2-5 shows coordination of the different metals in the GeO_x matrix after geometry relaxation of $Ge(M)O_2/Ge$ (100) structures, and Fig. 2-12 shows electronic density of states of the relaxed $Ge(M)O_2/Ge$ (100) structures as a function of energy relative to the valence band edge (E_v) of the Ge slab. This simulations results suggest that because La is 4 fold co-ordinated in $LaGeO_x$, it produces state-free interfaces with Ge, which could explain the experimentally estimated low D_{it} values. This should be contrasted with the HfO_2 /Ge case where Hf is 5 fold co-ordinated, giving rise to interface states peak near the conduction band, which, in turn, hampers the electrical performance of Ge devices. In addition, it was also commented that other rare-earth elements like Ce, Gd, Dy, and Lu have a partially filled 4 *f*-electron shell that has to be included as valence states in the structural and electronic computationof the slab models, which is not straightforward using a classical density function theory (DFT) approach. However, since all these elements tend to be 6 fold co-ordinated in their bulk metal-oxide phase, like La_2O_3, it was expected that they would also adopt a 4 fold co-ordination in the GeO_x interlayer for typical metal concentration below about 10 at.%. Consequently, these rare-earth elements, in contact with Ge, would also lead to a surface-state free Ge energy band gap.

The role of La surface chemistry in the passivation of Ge was also reported by measuring in situ XPS. [116] Upon exposure to O_2, clean bare Ge and Hf-covered or Al-covered Ge surfaces show no Ge-O bond formation. On the contrary, a La-covered Ge surface strongly reacts with O_2 forming a stable germanate $LaGeO_x$ compound. This has a beneficial side effect for the interface because the formation of volatile GeO is suppressed, resulting in the good passivating properties of $LaGeO_x$. This means that La changes drastically the surface chemistry of Ge and by producing a stable La_2O_3-GeO_2 mixture prevents the volatilization of GeO preserving also the interface integrity. Comparing with the different behavior exhibited by Hf and Al, oxygen densification in the compound could be the driving force for the formation of $LaGeO_x$. [116]

Table 2-5. Co-ordination of the different metals in the GeO_x matrix after geometry relaxation of $GeMO_2$/Ge (100) structures. [36]

Metal	Coordination	M–O bond length (Å)	M–Ge bond length (Å)
Al	4	1.75	···
La	4	2.43	···
Hf	5	2.04	2.77

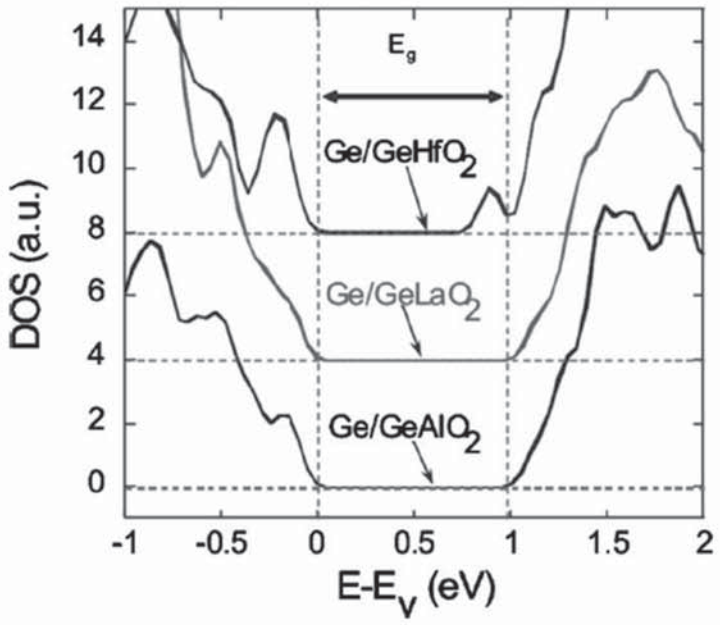


Figure 2-12. Electronic density of states of the relaxed Ge(M)O_2/Ge (100) structures vs. energy relative to the valence band edge (E_v) of the Ge slab. [36]

2.3.6. Si-Passivation

Si-passivation was suggested as an alternative way of forming a high quality gate dielectric for Ge. The intention of Si-passivation is to insert a SiO_2/Si interface into a high-*k*/Ge gate stack to bypass the interface passivation issues. Si can be successfully grown on Ge by epitaxy, as long as the thickness does not exceed the critical limit. Si interlayer technique, with several monolayers of Si grown between the dielectric and the substrate, has been applied on Ge, GaAs and other III-V compound semiconductors to improve the interface quality. [117, 118] With even a very thin Si incorporated into the high-*k*/Ge interface by SiH_4 or Si_2H_6 surface annealing enhanced hole mobility has been reportd. [39, 119] Si thicknesses in the range of a few monolayers are deposited, then partially oxidized to form SiO_2 passivation and capped with a high-*k* dielectric. The control of Si deposition and oxidation in monolayer sensitivity is very difficult and can result in a lot of variation issues, especially if this method would be applied to mass production. Si interlayer deposited by PVD also dramatically improve C-V hysteresis, interface states densities, and device performance shown on Fig. 2-13. The reason for electric properties improvement was explained by the supression of GeO_x at the interface by SiO_x layer. [32] Si-passivation was investigated by several research groups. [120-125] Taoka et al. reported improvement in inversion hole mobility is attributed to the reduction in interface charges and separation of mobile carriers and interface charges by increasing the Si passivation layer thickness. [123] However, that creates a trade-off between device performance and scalability of gate dielectric. Detailed interface state characterizations revealed asymmetric interface state density distribution across Ge bandgap. Interface state density reaches to 10^{14} cm^{-2} eV^{-1} close to conduction band edge. [125] That is a potential

problem which can degrade Ge NMOS inversion formation and drive currents. Hence, Ge NMOS devices fabricated using this passivation technique exhibited electron mobility less than 100 cm^2/Vs.

Figure 2-14 (a) shows Ge 2*p* spectra of $Pt/HfO_xN_y/Ge$ gate stacks before and after annealing. [39] The nonannealed high-*k* dielectric sample exhibited a severe degree of Ge diffusion into the top HfO_xN_y film. The GeO_x species detected in the Ge 2*p* spectrum arose possibly through one of two incorporation mechanisms: outdiffusion of gaseous GeO species from the substrate and downward into the high-*k* layer through airborne transportation and GeO volatilization from the interfacial layer and top surface of the Ge substrate. Figure 2-14 (b) shows bidirectional sweep of C-V curves for $Pt/HfO_xN_y/Ge$ gate stacks lacking and containing a Si capping layer. The Ge diffusion into HfO_2 deterioate the C-V characteristics, and Si capping was sucessfully suppress the Ge diffusion, as a result, C-V hysteresis was dramatically decreased. This phenamena was explained by that it is more likely that SiO_x and its silicate will form, rather than GeO_x, after deposition and annealing when the Si capping layer is present because Si-O bonds have larger Gibbs free energies and higher thermodynamical stabilities. Therefore, the formation of GeO at the interface and its outdiffusion are suppressed significantly upon increasing the thickness of the Si layer. Also, the exacerbated hysteresis width might be due to the high density of charge trapping sites at the high-*k*/GeO_x interface and within the defective GeO_x interfacial layer. [39]

Recently IMEC announced that important progress has been made in the passivation of Ge/gate dielectric interfaces by using the Si capping layer on Ge substrate. The EOT is ~1.5 nm and D_{it} values are $2x10^{11}$ cm^{-2} eV^{-1}. [126, 127] It was empasized the process

optimization. Si capping process requires a careful deposition of Si on Ge in an epitaxial fashion, such that all Ge dangling bonds are tied up to a Si atom. In other words, Ge-Si interface is fully passivated with covalent bonds and should not introduce any states in the bandgap. Therefore a too thick Si layer will relax due to the lattice mismatch which will create numerous misfit dislocations at the interface and add to the EOT. If too thin, the Si layer will be fully oxidized during the gate oxide deposition, and the interface will reach again the Ge substrate. The reported process condition is that a thin (4 ~ 6 mono layers) epitaxial layer of Si is grown from SiH_4 at 500°C on the Ge substrate after a 650°C bake in H_2 to remove the native oxide. Layers much thicker than six or seven monolayers exceed the critical thickness (due to the lattices misfit of 4 %) and thus are prone to defect formation upon relaxation, which can be seen as pronounced bumps in CV behavior. A treatment in a dilute aqueous ozone solution produces a thin 1 nm ″wet chemical Si oxide″ covered by numerous OH groups, which allows the deposition of a high quality of high-*k* gate dielectrics (4 nm of HfO_2) by ALD.

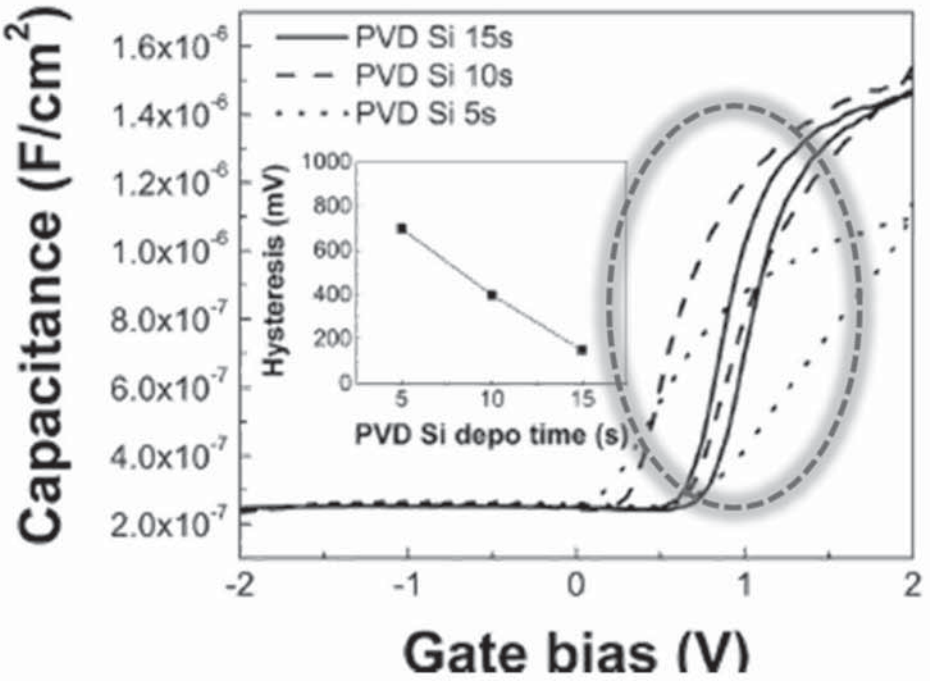


Figure 2-13. Reduction of bidirectional sweep C-V hysteresis function of PVD Si depo time. [32]

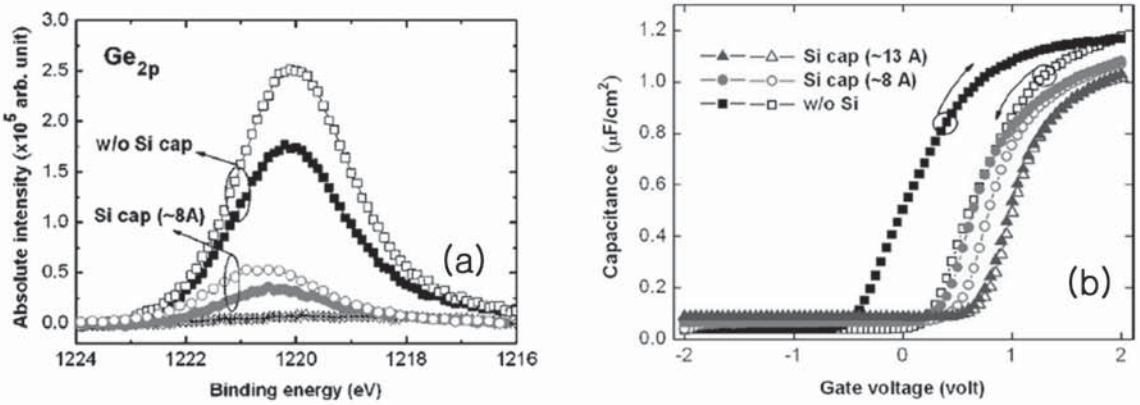


Figure 2-14. XPS (a) Ge 2*p* spectra of Pt/HfO_xN_y/Ge gate stacks before (solid symbols) and after (open symbols) dielectric annealing at 500°C for 5 min, (b) Bidirectional sweep C-V curves of Pt/HfO_xN_y /Ge gate stacks lacking and containing a Si capping layer. [39]

2.3.7. Sulfur Passivation

Sulfur (S) was proposed as strong passivation treatment to prevent uncontrolled interface reactions. [61, 128-130] S is one of attractive passivation materials, since S passivation successfully electrically improved with III-V compound substrate [61, 128] and poly crystalline Ge. [129] S passivation was achieved using aqueous ammonium sulfide ($(NH_4)_2S$). [61] S-termination on Ge surfaces is one of the candidates for the surface state prior to gate dielectrics deposition because of its improved oxidation resistance [58] and ease of preparation. [58, 61, 63, 131] Usually S-passivation on a Ge surface was carried out by preparing an aqueous $(NH_4)_2S$ solution [58, 61, 63, 131] or by gaseous H_2S. [132, 133] Although there is a difference in the temperature, S-termination desorbs from the Ge surface at an elevated temperature. In addition, while there is very limited research on the electrical characteristics of the S termination itself and of the gate stack on this termination, it has been reported that a lower Schottky barrier height for electrons, and improved uniformity on the diode are obtained on a Ge surface. [134] It was also observed that S termination produced a lower fixed charge and interface state density, as compared to the NH_3-annealed Ge surface. Therefore, the improved electrical properties of the stack and the robustness of S-termination on Ge surfaces motivate the introduction of Stermination on Ge as a surface state prior to gate dielectrics deposition. [61] The S passivation layer was preserved after the atomic layer deposition of HfO_2, acting like a barrier between Ge and HfO_2 to prevent inter-diffusion and interactions. However, an intermixed GeOS layer formation was observed. Also, interface state density measured by conductance technique shows D_{it} higher than 10^{12} $cm^{-2}eV^{-1}$, proving the poor electrical quality of interface.

2.4. Interface characterization techniques

Capacitance and conductance based techniques are extensively used in Si CMOS technology to characterize parameters of Si MOSFET and MOS capacitors such as the flat band voltage (V_{fb}) shift, EOT, work function, fixed charge, doping level and D_{it}. D_{it} is very critical to quantify the electrical quality of dielectric/ semiconductor (gate dielectric/channel) interface. Surface passivation of Ge is a key challenge to obtain excellent gate channel/dielectric interface and to achieve high performance Ge MOSFETs. Deeper understanding of surface passivation is needed to address interface related performance problems, especially for NMOS transistors [61, 91, 92, 123, 124, 135-137]. However, the conventional D_{it} extraction techniques cannot be directly applied to Ge. The low E_g of Ge makes the electrical interface characterization a big challenge.

2.4.1. Conductance Method

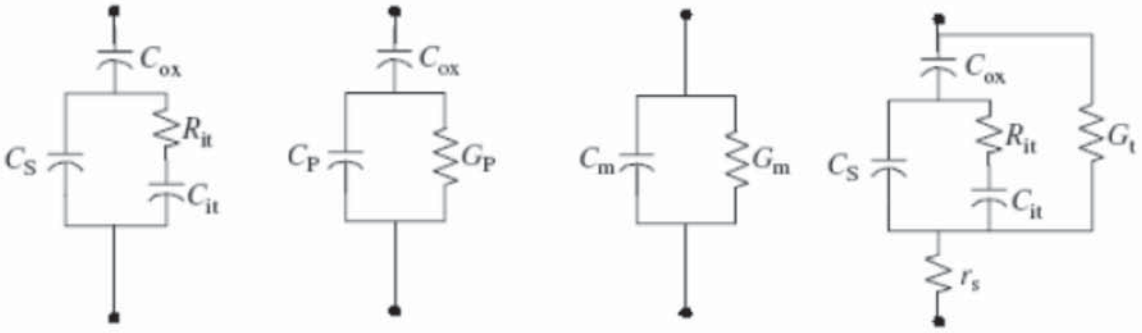
The conductance method, proposed by Nicollian and Goetzberger in 1967, is one of the most sensitive methods to determine D_{it}. [61, 91, 92, 123, 124, 135-137] Interface trap densities of 10^9 $cm^{-2}eV^{-1}$ and lower can be measured. [138] It is also the most complete method, because it can determine D_{it} in depletion and weak inversion portion of the E_g, capture cross sections of majority carriers, interface trap time constants and surface potential fluctuations. The method is based on measuring equivalent parallel conductance (G_p) of a MOS capacitor as a function of gate bias and frequency.

The conductance is measured as a result of the loss due to interface trap capture and emission of carriers. The magnitude of the conductance peaks relates to the interface trap density. The equivalent circuit for a MOS capacitor is shown in Fig. 2-15 (a). It consists of oxide capacitance (C_{ox}), semiconductor capacitance (C_s), and interface trap capacitance (C_{it}). The loss capture-emission process of carriers is modeled as a resistor (R_{it}) in series with C_{it}. The circuit can be simplified as in Fig. 2.14 (b), where

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau t_{it})^2} \qquad (6)$$

Where $C_{it}= q^2D_{it}$, $\omega=2\pi f$, f is measurement frequency and T_{it} is the interface trap time constant.

Figure 2-15 (c) shows the measured circuit diagram, C_p and G_p can be extracted from measured values of C_m and G_m, once C_{ox} is known. Parasitic series resistance arising from low substrate doping or contact resistances or leakage through gate dielectric, can contribute measured admittance. They need to be included in the equivalent circuit model as rs and G_t to extract the accurate value of interface trap conductance and capacitance.



(a) (b) (c) (d)

Figure 2-15. Equivalent circuit models for conductance measurements; (a) MOS capacitor with interface traps, (b) simplified circuit of MOSCAP, (c) measured circuit and (d) including series resistance and tunnel conductance due to gate leakage. [138]

Eq. (6) is valid for an interface trap with single energy level in the E_g. However, interface traps are continuously distributed across the E_g. If the time constant dispersion and trap energy level distribution across E_g is considered:

$$\frac{G_p}{\omega} = q\frac{D_{it}}{2\omega\tau_{it}} In[1 + (\omega\tau_{it})^2] \quad (7)$$

Eq. (7) shows that conductance method is easier and more direct way of extracting D_{it} than capacitance based methods, which require semiconductor capacitance, C_s. When G_p/ω is plotted as a function of ω, it shows a maximum at $\omega=1.98/T_{it}$ and at that maximum

$$D_{it} = \frac{2.5G_p}{q\omega} \quad (8)$$

Gp/ω plots are repeated at different gate voltages to scan trap energies to obtain an interface state density distribution across the E_g.

Generally experimental Gp/ω versus ω curves are broader than predicted due to surface potential fluctuations arising from non-uniformities in doping, fixed charge, etc. When surface potential fluctuations are taken into account:

$$\frac{G_p}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau_{it}} In[1 + (UT_{it})^2]P(U_s)dU_s \quad (9)$$

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{(U_s-\overline{U}_s)^2}{2\sigma^2}\right) \quad (10)$$

P(Us) is the probability distribution of surface potential fluctuation, is the normalized mean surface potential and σ is the standard deviation. Conductance technique, developed

by Nicollian and Goetzberger, has been intensively studied on semiconductor insulator interfaces. Conductance technique has several advantages over other interface characterization techniques, Sensitivity, Simplicity and easy implementation, It can measure both low and high levels of D_{it}, It doesn't require to fabricate MOSFET, a simple MOSCAP is sufficient. When conductance technique is used at room temperature, it is valid in the depletion regime and it requires multi-frequency C-V and conductance (G-V) measurements. However, in case of low E_g semiconductors, low temperature measurements are needed to suppress the thermal generation affecting C-V and G-V measurements.

3. Experiments and Analysis

3.1. Atomic Layer Deposition of La-based oxide

3.1.1. Deposition of La-silicate thin films using $La[N(SiMe_3)_2]_3$ precursor with liquid injection system

La-silicate films were grown on a HF-cleaned *p*-type (100) Si substrate at a wafer temperature of 310°C in a traveling-wave type 4-in. thermal ALD reactor with a liquid delivery system shown on Fig. 3-1 using Tris[bis(trimethylsilyl)amino]lanthanum, $La[N(SiMe_3)_2]_3$ as the metal precursor. Vapor pressure and melting point for La precursors are shown on Table 3-1 and Fig. 3-2. The molecular structure and properties of $La[N(SiMe_3)_2]_3$ are shown in Table 3-2 and Fig. 3-3. An O_3 of 110 g/Nm^3 and H_2O at room temperature were used as the oxygen sources for O_3-La-silicate and H_2O-La-silicate films, respectively.

$La[N(SiMe_3)_2]_3$ precursor was vaporized at 190°C and delivered to the reactor with the Ar carrier gas of 200 sccm. The injection time of $La[N(SiMe_3)_2]_3$ dissolved in hexane was controlled in milliseconds to precisely deliver it to a vaporizer. The injection time for La source, H_2O and O_3 was fixed at 0.1ms, 1s and 5s, respectively. The base pressure of the ALD chamber was maintained below 0.01 torr.

The La-silicate films were deposited on *p*-type Si (100) wafers, which were cleaned by diluted HF solution ($HF:H_2O$ = 1:100) for the purpose of removing the native oxide. The chamber wall temperature was maintained at 125°C to facilitate the desorption of the source and oxidant from the wall surface during the purge sequence. The substrate

temperature was at 310°C. The La source and reactant were injected alternately and the residual gas was purged with Ar between the injections. The flow rate of the Ar purge was fixed at 200 sccm, and the chamber pressure was maintained below 0.3 torr. Process conditions of thermal ALD grown La-silicate film is shown on Table 3-3.

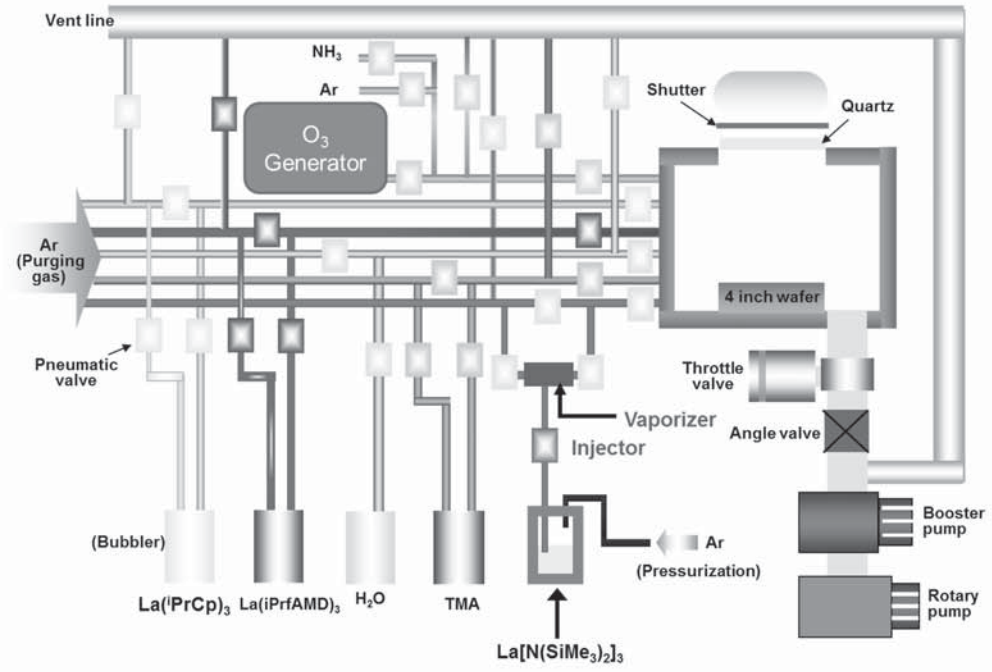


Figure 3-1. Schematic diagram of thermal-ALD system used in these experiments with direct liquid injection system and bubbler system for La-precursors.

Table 3-1. Vapor Pressure and Melting point for La metal precursors.

La Precursor	Vapor Pressure	Melting Point
$La(^{i}PrCp)_3$	0.01 Torr/155 °C	-
$La(EtCp)_3$	0.2 Torr/174 °C	95 °C
$La(MeCp)_3$	0.05 Torr/220 °C	155 °C
$La[N(SiMe_3)_2]_3$	0.01 Torr/102 °C	160 °C
$La(THD)_3$	0.2 Torr/210 °C	230 °C
$La(^{i}PrfAMD)_3$	0.05 Torr/100 °C	195 °C
$La(EDMDD)_3$	0.1 Torr/197 °C	150 °C

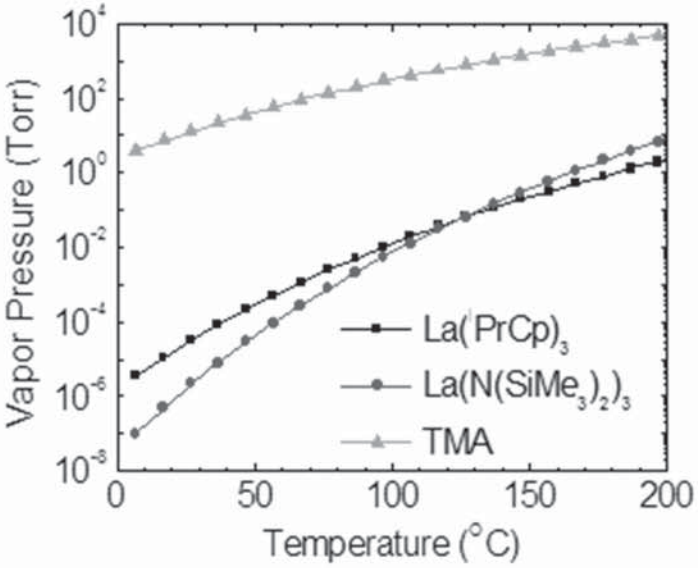


Figure 3-2. The Vaporize Pressure of $La(iPrCp)_3$, $La[N(SiMe_3)_2]_3$ and TMA precursors.

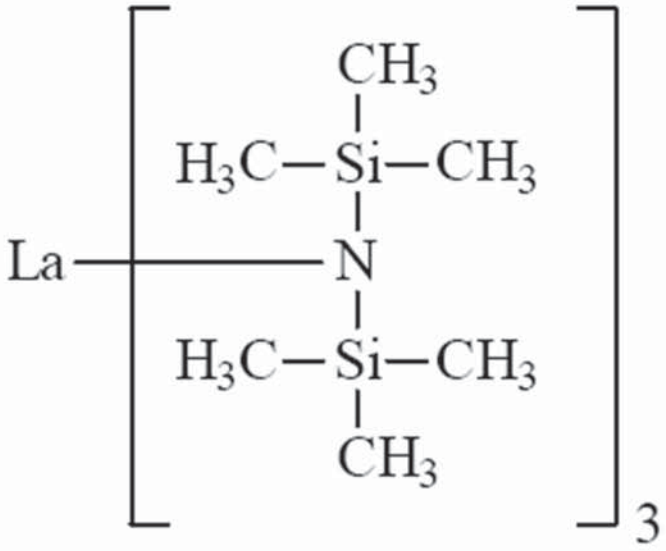


Figure 3-3. The molecular structure of $La[N(SiMe_3)_2]_3$.

Table 3-2. Physical and chemical properties of $La[N(SiMe_3)_2]_3$ precursor.

	$La[N(SiMe_3)_2]_3$
Appearance	White Powder
Vapor pressure	Log P (torr) = 12.3 - 5389/ T(K)
stability	Hydrolysis in air
Molecular weight	618.91
Molecular formula	$La[N(Si(CH_3)_3)_2]_3$

Table 3-3. Process conditions of thermal ALD grown with $La[N(SiMe_3)_2]_3$.

Substrate temp.	310°C
Substrate	*p*-type Si
La source temp.	Room Temperature
La injector temp.	190°C
H_2O temp.	Room Temperature
Wall temp.	125°C
Carrier Ar flow	200 sccm
Purge Ar flow	200 sccm

3.1.2. Deposition of La-oxide thin films using $La(iPrCp)_3$ with bubbler system

Tris(isopropyl-cyclopentadienyl)lanthanum, [$La(iPrCp)_3$] and O_3 were used as the reactants for the La-oxide deposition process. The molecular structure and chemical properties of $La(iPrCp)_3$ precursor are shown in Fig. 3-4 and Table 3-4.

The injection of the La source and the reactant was controlled automatically by air-operated valves, which enable the alternate injection of the reactants. The temperature of the La source was set to 160°C for the bubbler system. The La source was injected into the reaction chamber with 200 sccm of Ar carrier gas, while O_3 was injected without carrier gas. The injection time for La source and O_3 was fixed at 10s and 5s, respectively. The base pressure of the ALD chamber was maintained below 0.01 torr.

The films were deposited on *p*-type Ga-doped Ge(100) wafers, which were cleaned by diluted HF solution ($HF:H_2O=1:100$) with cyclic cleaning for the purpose of removing the native oxide. The chamber wall temperature was maintained at 125°C to facilitate the desorption of the source and oxidant from the wall surface during the purge sequence. The substrate temperature was at 310°C.

The La source and reactant were injected alternately and the residual gas was purged with Ar between the injections. The flow rate of the Ar purge was fixed at 200 sccm, and the chamber pressure was maintained below 0.3 torr. To completely remove the residual source or reactants, the reaction chamber was purged with Ar for more than 30 s between the injections. Process conditions of thermal ALD grown La-oxide film is shown on Table 3-5.

Figure 3-4. The molecular structure of $La(iPrCp)_3$.

Table 3-4. Physical and chemical properties of $La(iPrCp)_3$.

	$La(iPrCp)_3$
Appearance	Viscous pale-yellow liquid
Vapor pressure	Log P (torr) = 8.7 - 3956/ T(K)
stability	Hydrolysis in air
Molecular weight	460.43
Molecular formula	$(C_3H_7C_5H_{4)})_3La$

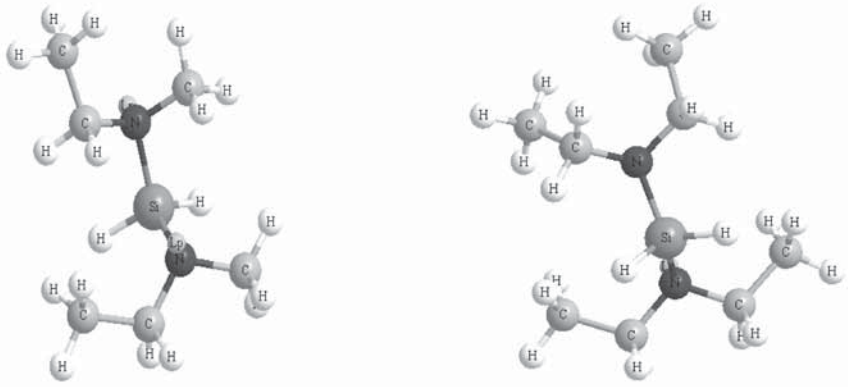
Table 3-5. Process conditions of thermal ALD grown with $La(iPrCp)_3$.

Substrate temp.	310°C
Substrate	*p*-type Si
La source temp.	160°C
H_2O temp.	Room Temperature
Wall temp.	125°C
Carrier Ar flow	200 sccm
Purge Ar flow	200 sccm

3.2. Atomic Layer Deposition of various passivation interfacial layers and capping layers

3.2.1. La-silicate thin films as a bulk layer on Ge and as a passivation interface layer of HfO_2 film using $La[N(SiMe_3)_2]_3$, BEMAS and BDEAS-SiO_2 precursor.

In order to improve electric property of Ge MOSCAP, La-silicate films were deposited as passivation layer for HfO_2 film. To compare with La-silicate film, SiO_2 thin films using either Bis(ethylmethylamino)Silane (BEMAS), $SiH_2(NC_2H_5CH_3)_2$ (Molecular structure, physical and chemical properties shown on Fig. 3-5 (a) and Table 3-6) or Bis(diethylamino) Silane (BDEAS), $SiH_2(N(C_2H_5)_2)_2$ (Molecular structure, physical and chemical properties shown shown on Fig. 3-5 (b) and Table 3-6) precursors were deposited on a cyclic HF cleaned Ga-doped *p*-type (100) Ge substrate as passivation layer. Thickness of ~ 6.0 nm HfO_2 thin film was deposited right-after La-silicate or SiO_2 interface passivation later deposition by thermal-ALD (Quros, PLUS 200) at a wafer temperature of 200°C using Tetrakis(ethylmethylamino)Hafnium (TEMAHf), $Hf[N(CH_3)C_2H_5]_4$ precursor. An O_3 having a concentration of 170 g/Nm^3 was used as the oxygen sources and canister temperature was set to 60°C for HfO_2 films. An O_3 having a concentration of 110 g/Nm^3 was used as the oxygen sources for La-silicate and SiO_2 films. The precursor injection time for La-silicate, SiO_2 sources and O_3 was fixed at 0.01s, 1s, and 5s, respectively. The base pressure of the ALD chamber was maintained below 0.01 torr. Process flow is shown on Fig. 3-6.



(a) (b)

Figure 3-5. The molecular structure of (a) $SiH_2(NC_2H_5CH_3)_2$ (BEMAS) precursor and (b) $SiH_2(N(C_2H_5)_2)_2$ (BDEAS) precursor.

Table 3-6. Physical and chemical properties shown of $SiH_2(NC_2H_5CH_3)_2$ (BEMAS) and $SiH_2(N(C_2H_5)_2)_2$ (BDEAS) precursor.

Chemical name	**Bis-diethylamino-silane (BDEAS)**	**Bis-ethylmethylamino-silane (BEMAS)**
Chemical Formula	$H_2Si[N(C_2H_5)_2]_2$	$H_2Si[N(C_2H_5)(CH_3)]_2$
Vapor pressure	**1.3 Torr** at 20°C	**5 Torr** at 20°C
Boiling point	188°C (Melting point : -10°C)	134°C
Density	174.4 g/mol	146.31 g/mol
Physical state	Colorless Liquid	Colorless Liquid
Features	Highly reactive with water	Highly reactive with water

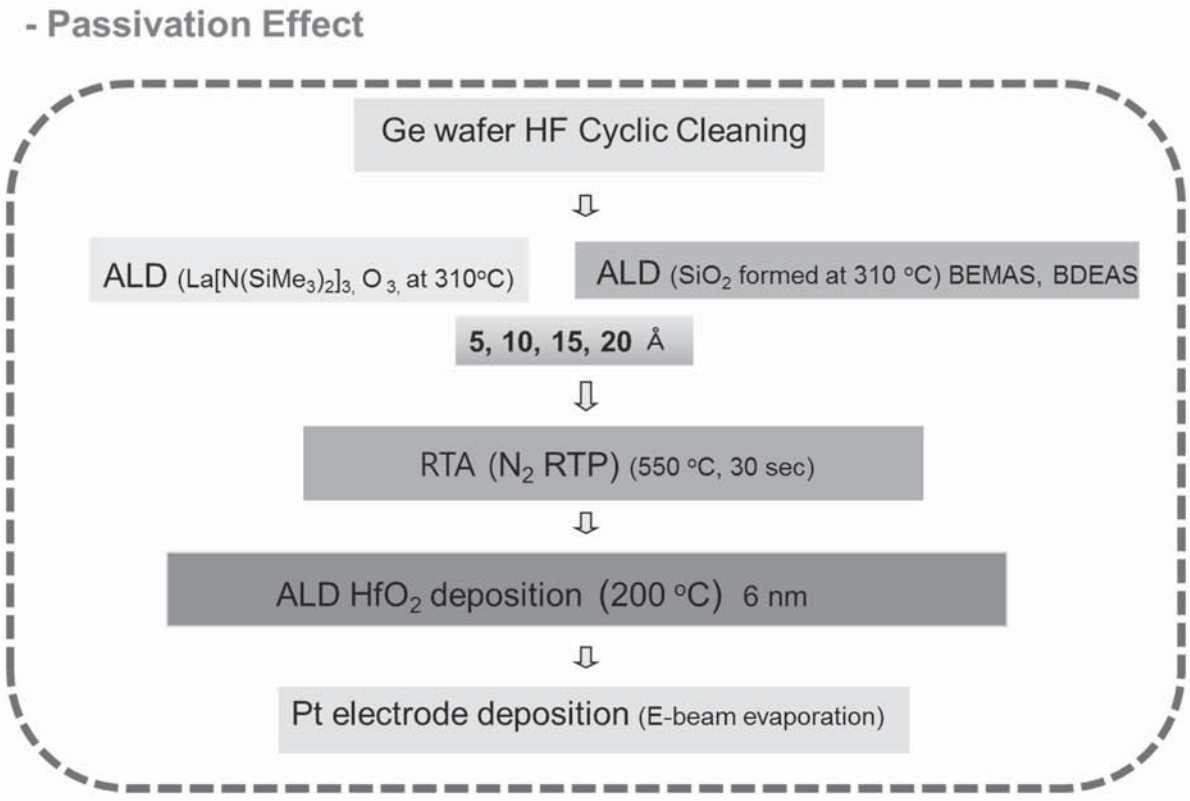


Figure 3-6. Experimental flow for La-silicate and SiO_2 thin film as a passivation interface layer of HfO_2 film.

3.2.2. Deposition of Si concentration controlled La-silicate thin films using $La[N(SiMe_3)_2]_3$, BEMAS and BDEAS-SiO_2 precursor.

In order to control Si concentrations of La-silicate films, SiO_2 precursor was injected alternately during the La-silicate film deposition. La-silicate films were deposited by thermal ALD on a cyclic HF cleaned Ga-doped *p*-type (100) Ge substrate at a wafer temperature of 310°C. $La[N(SiMe_3)_2]_3$ dissolved in hexane, BEMAS-SiO_2 $SiH_2(NC_2H_5CH_3)_2$ and BDEAS-SiO_2 $SiH_2(N(C_2H_5)_2)_2$ precursors were used as the metal precursors for Si concentration controlled La-Silicate, respectively. An O_3 having a concentration of 110 g/Nm^3 was used as the oxygen sources for La-silicate and SiO_2 films. The precursor injection time for La-silicate, SiO_2 sources and O_3 was fixed at 0.01s, 1s, and 5s, respectively. The base pressure of the ALD chamber was maintained below 0.01 torr.

Si concentration in La-silicate film was controlled by deposition cycle numbers alternately injected SiO_2 precursors BEMAS and BDEAS during La-Silicate film. Si concentrations is defined as [Si/(La+Si)] in this experiment. Si concentrations for pure La-oxide, pure La-silicate and SiO_2 were considered as 0%, 25% and 100%. The ratios of [Si/(La+Si)] for Si concentration controlled La-silicate film were ~ 30% and ~ 35 % for the both SiO_2 precursor. The chamber wall temperature was maintained at 125°C to facilitate the desorption of the source and oxidant from the wall surface during the purge sequence.

The La and SiO_2 sources and reactant were injected alternately and the residual gas was purged with Ar between the injections. The flow rate of the Ar purge was fixed at 200 sccm, and the chamber pressure was maintained below 0.3 torr. Process conditions of thermal ALD grown Si controlled La-silicate film is shown on Fig. 3-7.

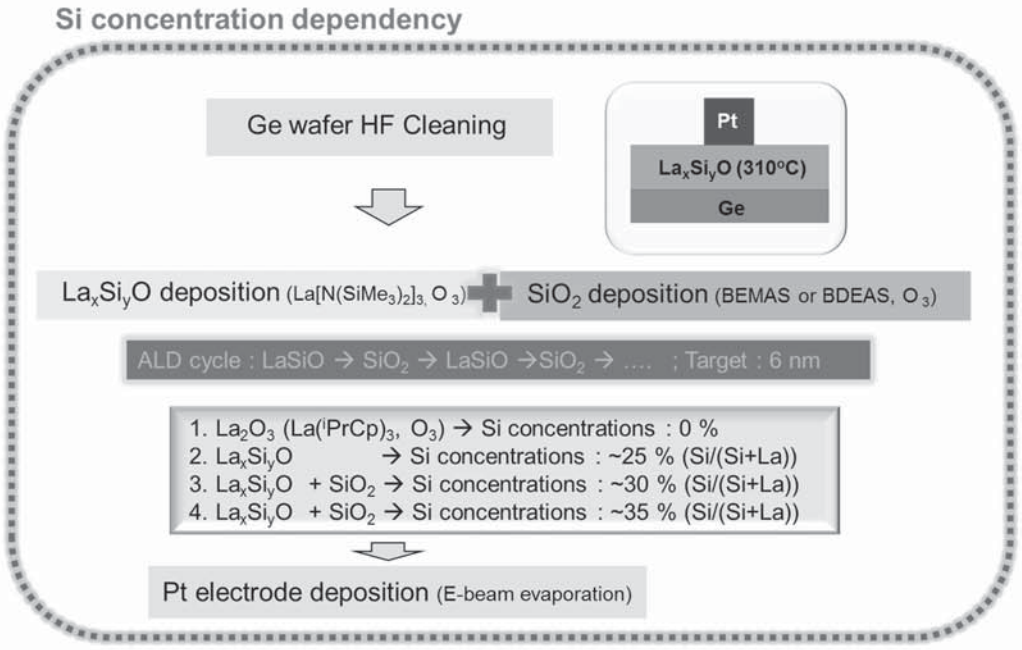


Figure 3-7. Experimental flow for Si concentration controlled La-silicate thin films.

3.2.3. Deposition of SiO_2 and Al_2O_3 passivation interface layers and capping layers for La-Silicate thin film.

Various passivation interfacial layers and capping layers, such as Al_2O_3 and SiO_2 were deposited by thermal ALD on a cyclic HF cleaned Ga-doped *p*-type (100) Ge substrate at a wafer temperature of 310°C. TMA $Al(CH_3)_3$, BEMAS $SiH_2(NC_2H_5CH_3)_2$ and BDEAS $SiH_2(N(C_2H_5)_2)_2$ were used as the metal precursors for Al_2O_3 and SiO_2, respectively. An O_3 having a concentration of 110 g/Nm^3 was used as the oxygen sources for Al_2O_3 and SiO_2 films. The precursor injection time for SiO_2 and Al_2O_3 sources and O_3 was fixed at 1s, 1s, and 5s, respectively. The base pressure of the ALD chamber was maintained below 0.01 torr.

Thickness of passivation interfacial layers and capping layers were deposited 0, 1, 2 and 3 nm on or beneath 5 nm of La-silicate film, respectively. The La, Si and Al sources and reactant were injected alternately and the residual gas was purged with Ar between the injections. The flow rate of the Ar purge was fixed at 200 sccm, and the chamber pressure was maintained below 0.3 torr. The process conditions of thermal ALD grown La-silicate film with various passivation interface layers and capping layer is shown on Fig. 3-8 and Fig. 3-9.

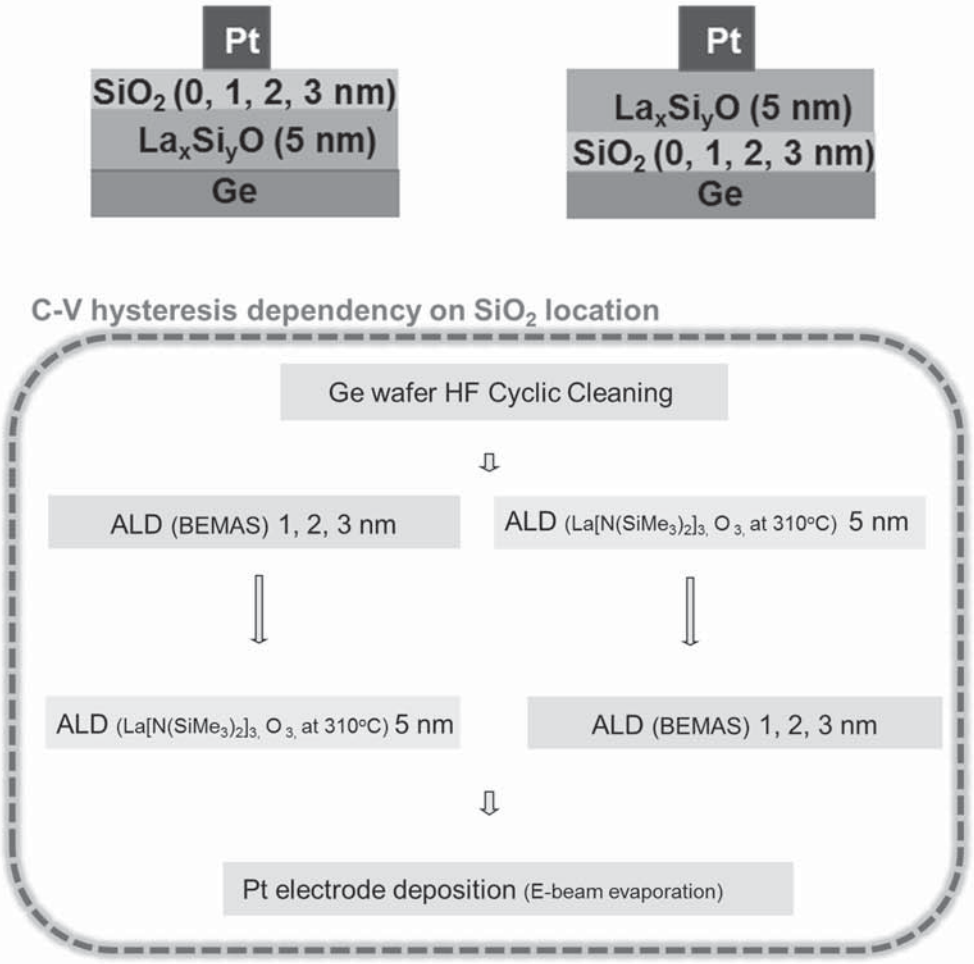


Figure 3-8. Experimental flow and schematic diagrams for thermal-ALD grown La-silicate film with SiO_2 passivation interface layer and capping layer.

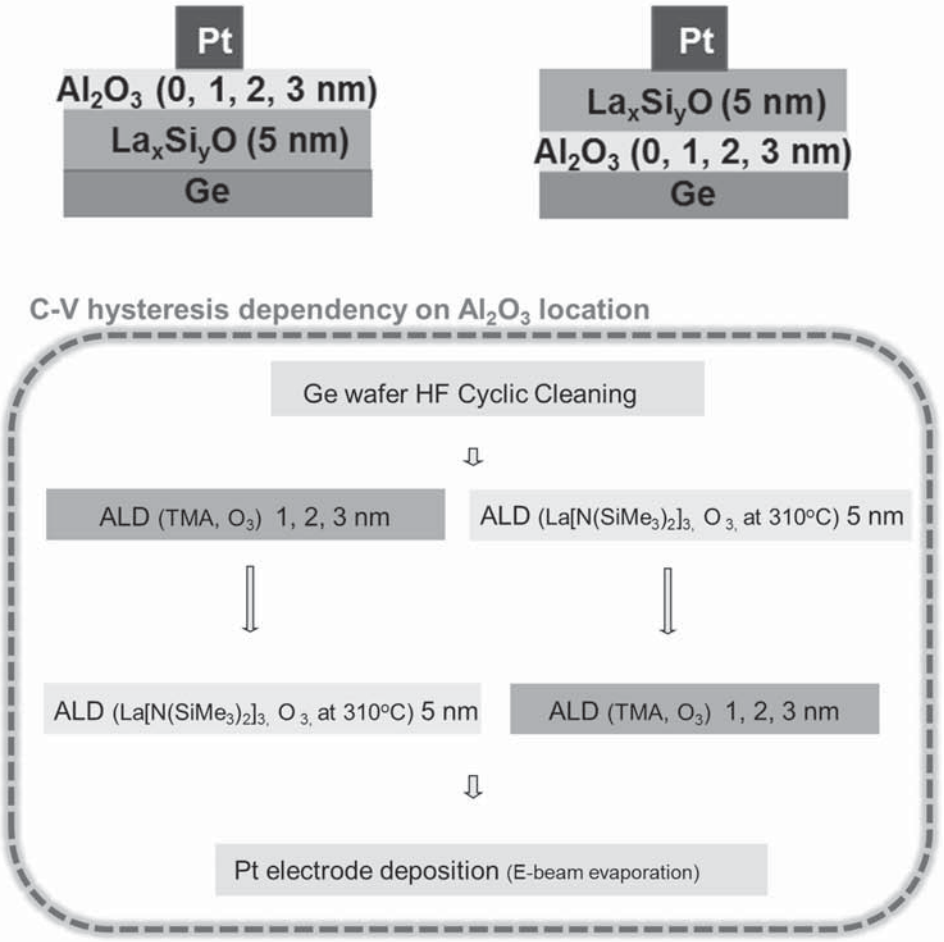


Figure 3-9. Experimental flow and schematic diagrams for thermal ALD grown La-silicate film with Al_2O_3 passivation interface layer and capping layer.

3.2.4. Deposition of ultra-thin Al_2O_3 passivation interface layers for La-Silicate thin film.

An ultra-thin Al_2O_3 passivation interfacial layer beneath La-silicate film were deposited by thermal ALD on a cyclic HF cleaned Ga-doped *p*-type (100) Ge substrate at a wafer temperature of 310°C. An O_3 having a concentration of 110 g/Nm^3 was used as the oxygen sources for La-silicate and Al_2O_3 films.

The thickness of Al_2O_3 passivation layer was controlled by deposition cycles ranging from 2 cycles to 10 cycles shown on Fig. 3-10. The TMA deposition cycles of 10 are deposited ~ 1 nm of Al_2O_3 thin film. The other deposition conditions were same as above La-silicate film.

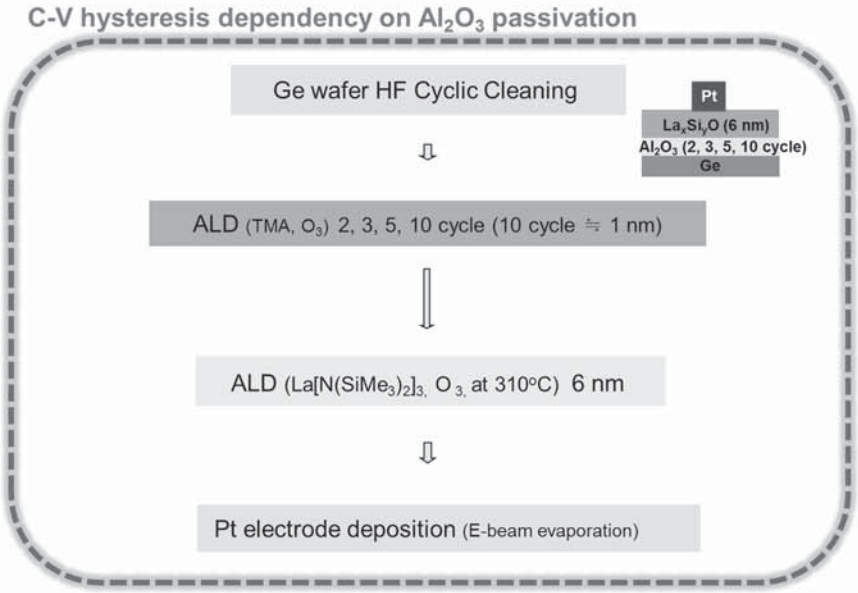


Figure 3-10. Experimental flow and schematic diagrams for thermal ALD grown La-silicate film with an ultra-thin Al_2O_3 passivation interface layer.

3.2.5. Deposition of Multi-stack La-silicate thin film. (Ultra-thin Al_2O_3 passivation interface layers and SiO_2 capping layer)

Multi-stack La-silicate film is defined by La-silicate film with an ultra-thin Al_2O_3 passivation interfacial layers and 2 nm SiO_2 capping layers. There films were also deposited by thermal ALD on a cyclic HF cleaned Ga-doped *p*-type (100) Ge substrate at a wafer temperature of 310°C.

The thickness of La-silicate film was fixed to 5 nm. The thickness of Al_2O_3 passivation layer was controlled by deposition cycles ranging from 2 cycles to 10 cycles (~1 nm) and that of SiO_2 capping layer was fixed to 2 nm shown on Fig. 3-11. SiO_2 film was deposited using either BEMAS or BDEAS SiO_2 precursors to eliminate precursor effect. The other deposition conditions were same as other La-silicate film.

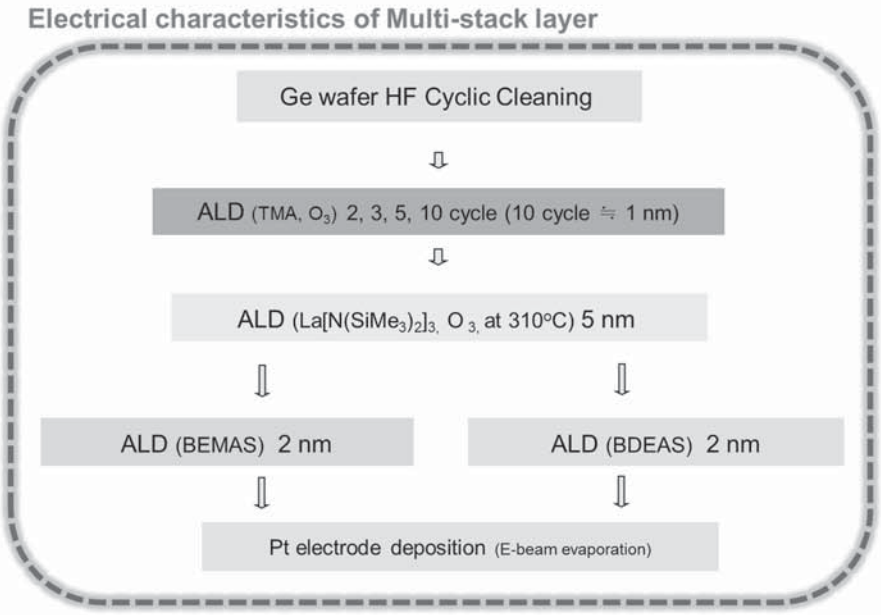


Figure 3-11. Experimental flow and schematic diagrams for thermal ALD grown multi-stack La-silicate film (with an ultra-thin Al_2O_3 passivation interface layer and 2.0 nm thickness of SiO_2 capping layer).

3.3. Sample preparation and analyses of the deposited films

Film thicknesses were measured by an ellipsometer (Gaertner Scientific$^{Co.}$, L116 D), Spectroscopic Ellipsometer (S.E., J.A. Woollam$^{Co.,Inc.}$, ESM-300), X-ray reflectivity (XRR, PANalytical, X'Pert PRO MPD) and confirmed by high-resolution transmission electron microscopy (HRTEM, JEOL, JRM 2100F). The depth profiles of elements in the films were examined by Auger electron spectroscopy (AES, Perkin-Elmer 660), and the chemical states and electronic structures of the films were analyzed by x-ray photoelectron spectroscopy (XPS, SIGMA PROBE) using monochromatic Al *Kα* as the x-ray source. Composition analysis for Ge interface was examined by HRTEM Energy Dispersive Spectrometer (EDS).

For MOS fabrication, Pt top electrodes were deposited by electron-beam evaporation using a shadow mask. Forming gas annealing at 400°C was followed in dilute H_2 (N_2 + 5% H_2) ambient for 30 min for Si substrate.

Capacitance-voltage (C–V) and leakage current density-voltage (J_g–V) characteristics were measured using an HP 4194 impedance analyzer and HP 4140B picoammeter/dc voltage source, respectively for Si substrate. C-V curves, constant-voltage-stress (CVS), interface state density (D_{it}), evaluated by conductance method, and leakage current density-voltage (J_g–V) characteristics were measured using an HP 4284 LCR meter, and HP 4140B picoammeter/dc voltage source, respectively for Ge substrate. The capacitance equivalent thickness (CET) was calculated from the accumulation capacitances measured at at 100 kHz for Si substrate and 1 MHz for Ge substrate considering quantum mechanical effects. The voltage was applied to the Pt top electrode while the Ge substrate was grounded via the In-contact.

4. Results and Discussions

4.1. La-Silicate thin film on Si substrate

4.1.1. Introduction

As the next generation high-*k* dielectric film as well as the threshold voltage control layer, La_2O_3 film are attracting much attention nowadays due to their high dielectric constant (~30) [2, 15] and large conduction band offset (CBO) with Si (~2.3 eV). [2] However, atomic layer deposition (ALD) of La-containing films has several challenges such as the limited selection of precursors and inducement of unstable film growth due to its hygroscopic behavior. [16] Additionally, serious Si diffusion from the substrate into the La_2O_3 film during deposition has been reported. [17, 18]

The use of Si-containing Tris[bis(trimethylsilyl)amino]lanthanum, $La[N(SiMe_3)_2]_3$, as a La precursor was reported as the promising way to intentionally incorporate Si in La_2O_3 film to prevent the diffusion of Si from Si substrates. [139] Since, significant Si diffusion during ALD of La_2O_3 film and post-deposition annealing degrades the gate controllability by increasing permittivity of the gate oxide film, the use of La-silicate film instead of La_2O_3 film is more attractive. Even though the chemical properties of ALD La-silicate films using $La[N(SiMe_3)_2]_3$ and H_2O were reported, [20-22, 139] systematic study on the influence of the type of oxygen source, H_2O or O_3, on the growth behavior and electrical properties of La-silicate films using $La[N(SiMe_3)_2]_3$ has been rarely reported. [23]

The chemical vapor deposition (CVD) techniques, metal organic chemical vapor

deposition (MOCVD) and atomic layer deposition (ALD), are considered to be more promising and competitive approaches to the fabrication of high quality thin films with conformal deposition and high throughput, producing films which exhibit excellent compatibility with semiconductor technology. However, there are several problems which need to be overcome in order to apply high-*k* films, deposited by the CVD method, can be used for gate dielectrics. Most vapor-phase grown high-*k* thin films appear to have interfacial layers having a lower-*k* value at the interface with the Si substrate, due to the presence of excess oxidizing elements, [7, 19] and the concurrent Si-diffusion into the films during deposition and thermal annealing. [140] This reduces the overall capacitance density, and should therefore be minimized in order to enhance the high-*k* characteristics.

In this study, the ALD behavior and electrical properties of La-silicate films according to the type of oxygen source were examined. In particular, the changes in Si concentration of the ALD La-silicate film grown using the $La[N(SiMe_3)_2]_3$ precursor were focused.

4.1.2 Deposition characteristics and Electrical properties of La-silicate

La-silicate films were grown on a diluted HF-cleaned *p*-type (100) Si substrate at a wafer temperature of 310°C in a traveling-wave type 4-in. thermal ALD reactor with a liquid delivery system using $La[N(SiMe_3)_2]_3$ as the metal precursor. An O_3 of 110 g/Nm^3 and H_2O at room temperature were used as the oxygen sources for O_3-La-silicate and H_2O-La-silicate films, respectively.

Figures 4-1 and 4-2 show the self-limiting growth characteristic of La-silicate films with different oxidants. Figs. 4-1 (a), (b) and (c) shows film growth rate depending on $La[N(SiMe_3)_2]_3$ precursor feeding time, purge time and the deposition temperature, respectively. The growth rate of H_2O-La-silicate film did not saturate as seem in Fig. 4-1 (a), but H_2O-La-silicate film obtained narrow ALD window at 300 to 310°C. The growth rate of the H_2O-La-silicate film in ALD window was obtained ~ 0.035 nm per cycle.

The self-limiting growth characteristic of $La[N(SiMe_3)_2]_3$ precursor and Ozone were shown on Figs. 4-2. Figure 4-2 (a), (b), (c) and (d) shows film growth rate depending on $La[N(SiMe_3)_2]_3$ precursor feeding time, purge time, ozone feeding time and purge time, respectively. The growth rate of O_3-La-silicate film was obtained about 0.18 nm per cycle at deposition temperature of 310°C. O_3-La-silicate films shows about five times faster growth rate than H_2O-La-silicate films.

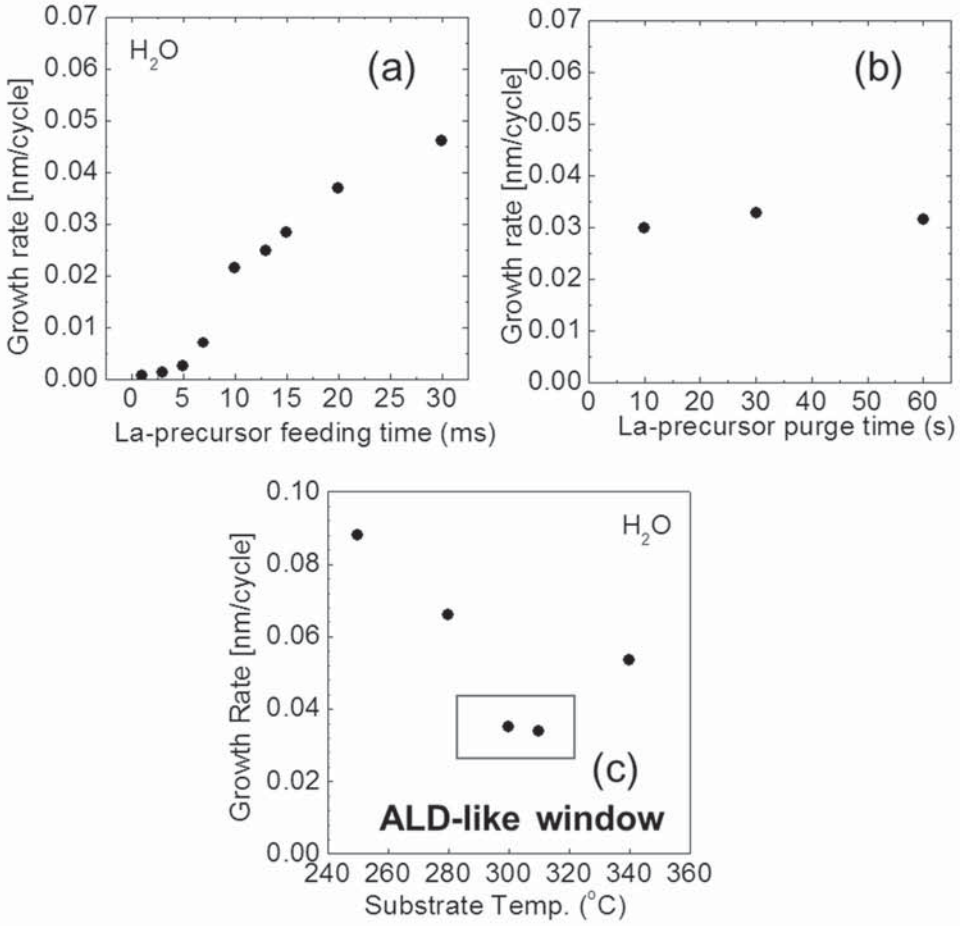


Figure 4-1. The film growth rate depending on $La[N(SiMe_3)_2]_3$ precursor (a) feeding time, (b) purge time and (c) the deposition temperature, respectively.

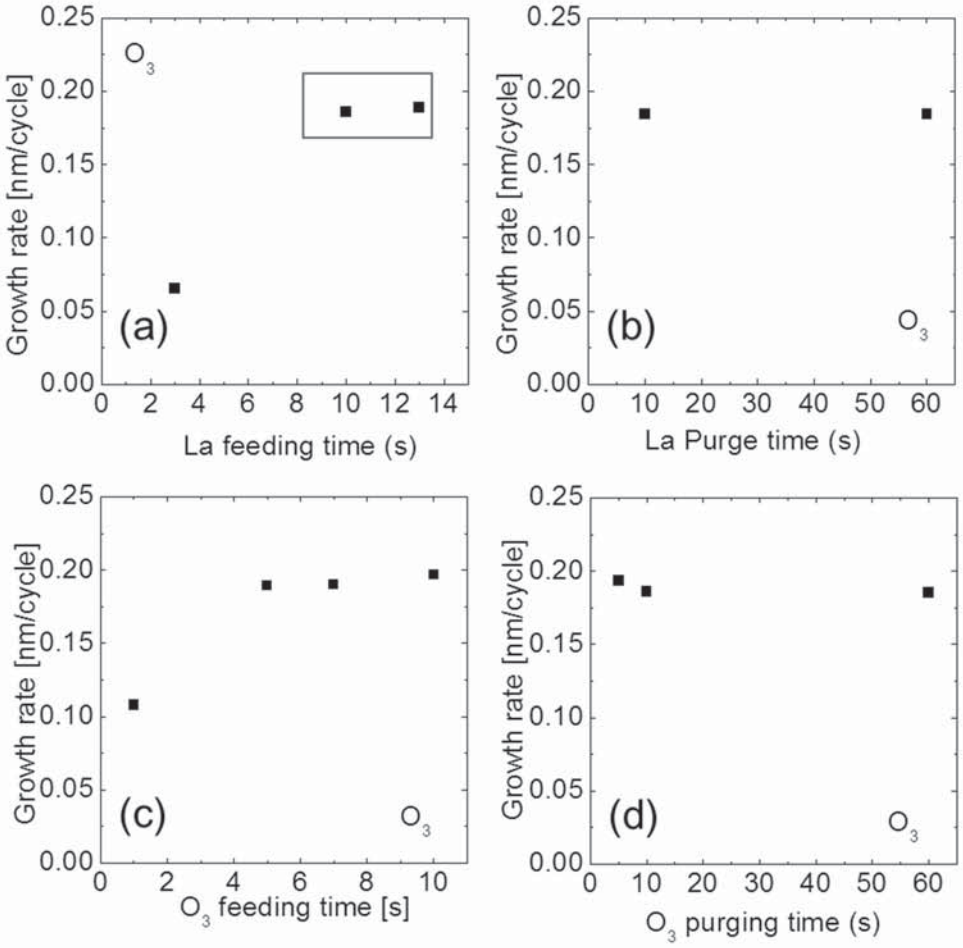


Figure 4-2. The film growth rate depending on $La[N(SiMe_3)_2]_3$ precursor (a) feeding time, (b) purge time, (c) ozone feeding time and (d) purge time, respectively.

4.1.3. MOSCAP fabrication

The thickness of ~ 6.0 nm La-silicate films were grown on a HF-cleaned *p*-type (100) Si substrate at a wafer temperature of 310°C in a traveling-wave type 4-in. thermal ALD reactor with a liquid delivery system using $La[N(SiMe_3)_2]_3$ as the metal precursor.

Film thicknesses were measured by an ellipsometer and confirmed by X-ray reflectivity. The depth profiles of elements in the films were examined by Auger electron spectroscopy. The chemical states and electronic structures of the films were analyzed by XPS using monochromatic Al *Kα* as the x-ray source.

For MOSCAP fabrication, Pt top electrodes were deposited by electron-beam evaporation using a shadow mask. Schematic diagram of fabricated MOSCAP shows on Fig. 4-3. Forming gas annealing at 400 °C was followed in dilute H_2 (N_2 + 5% H_2) ambient for 30 min.

Capacitance-voltage (C–V) and leakage current density-voltage (J_g–V) characteristics were measured using an HP 4194 impedance analyzer and HP 4140B picoammeter/dc voltage source, respectively. The capacitance equivalent thickness (CET) was calculated from the accumulation capacitances measured at 100 kHz considering quantum mechanical effects.

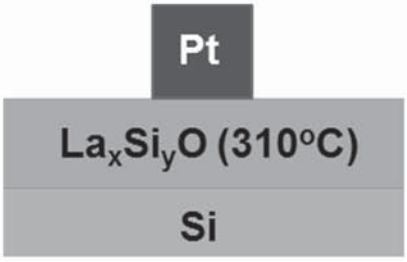


Figure 4-3. The schematic diagram of fabricated MOSCAP with deposited La-silicate film for this experiment.

4.1.4. Electrical and Chemical Analysis of La-silicate film with different oxidants

Figure 4-4 shows the CET variation of H_2O- and O_3-La-silicate films as a function of their physical thickness. The dielectric constants of H_2O- and O_3-La-silicate films were ~ 11.7 and ~ 8, respectively, which were lower than the reported values of La_2O_3 [2] due to the higher Si concentration originated from the precursor molecules. Kukli et al. reported that ALD Pr_2O_3 films grown using $Pr[N(SiMe_3)_2]_3$ precursors showed high Si concentrations. [141] The O_3-La-silicate film showed a lower dielectric constant than the H_2O-La-silicate film due to the higher Si concentration in the O_3-La-silicate films, which was confirmed by the AES depth profiles shown in Figs. 4-5 (a) and (b). The ratios of [Si/(La+Si)] were ~ 21 and ~ 39 % for the H_2O- and O_3-La-silicate films, respectively. The ratios were obtained using the average concentrations of La and Si through the oxide layer in AES results.

Figure 4-5 (c) shows calculated Si concentrations in H_2O-La-silicate films as a function of deposition temperature from the XPS measurement. As higher deposition temperatures, H_2O-La-silicate film obtained higher Si concentrations. The ratios of [Si/(La+Si)] were ~ 47 % for the H_2O-La-silicate films at deposition temperature of 310°C within an ALD window. The CET of the interface layer (IL) extracted from the y-intercept of curve (Fig. 4-4) was similar, ~ 0.5 nm for the both cases. The previous report by Park et al. expected the slightly thicker IL in the La_2O_3 film grown using O_3 compared to La_2O_3 film grown using H_2O based on the XPS results. [17]

However, the La precursor used in their work does not contain Si resulting in La_2O_3 film, not La-silicate film, and the expectation based on the chemical analysis could be different from that based on the electrical measurements. [17]

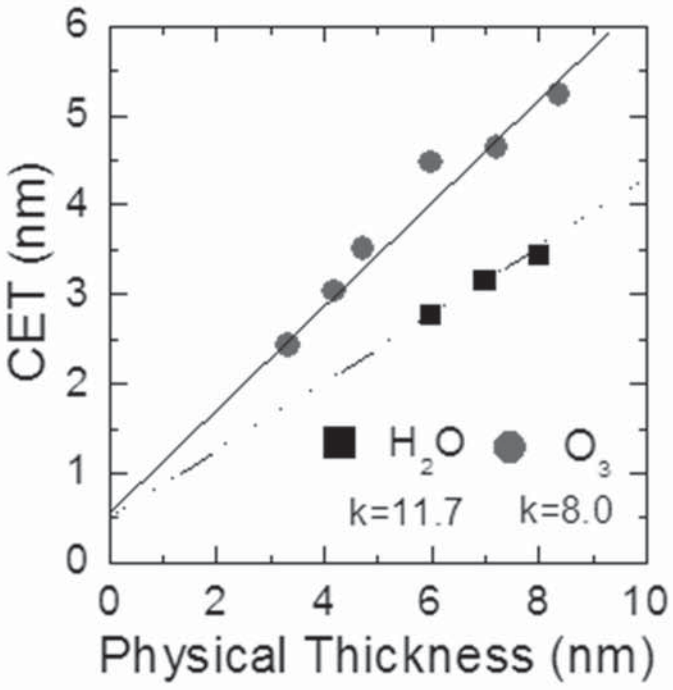


Figure 4-4. CET vs. physical thickness of deposited La-silicate film with different oxidants water and ozone.

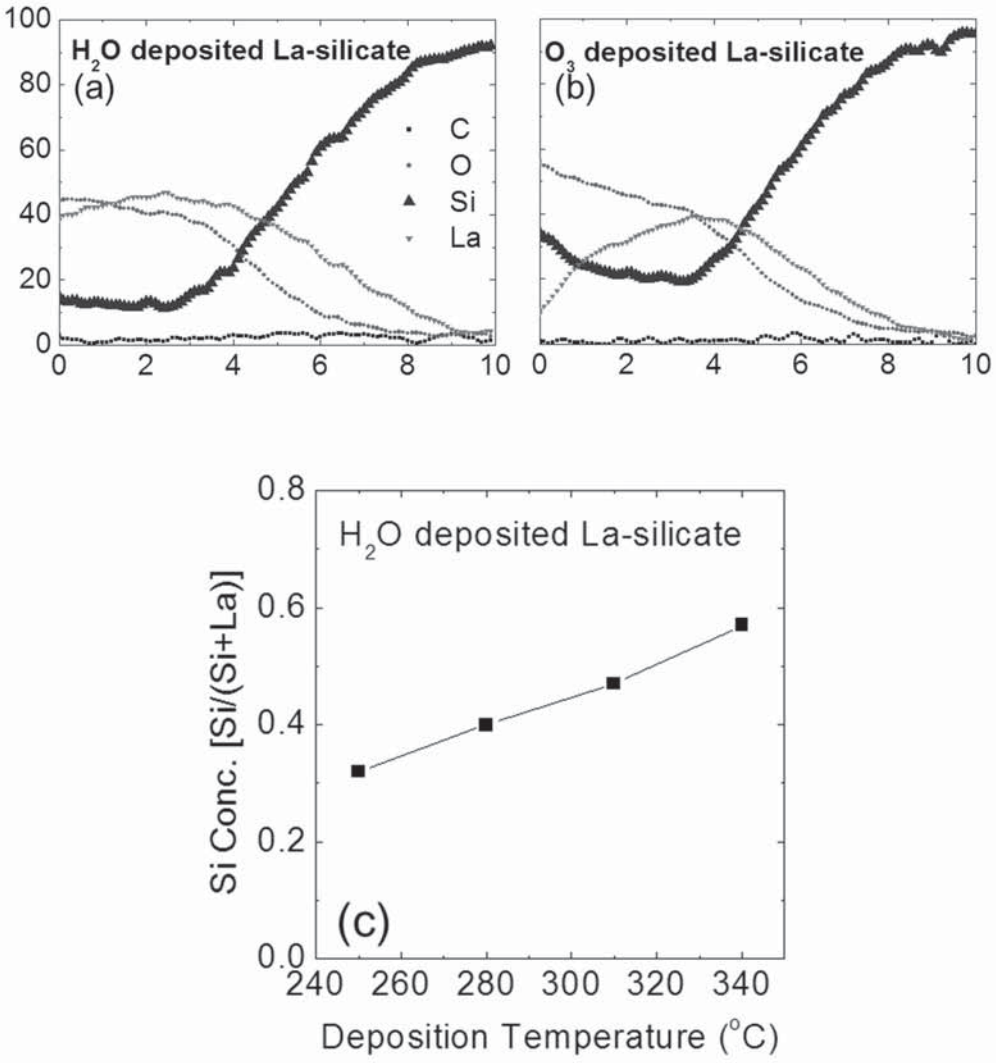


Figure 4-5. AES depth profiles of the La-silicate films grown with (a) H_2O, (b) O_3 and (c) Si concentrations of La-silicate film grown H_2O as a function of deposition temperature calculated from XPS measurement.

Considering that the physical thickness of IL in La-based films is hard to be defined due to no distinct contrast in a high-resolution transmission electron microscopy image [142], and the IL consists of mainly SiO_2, the similar electrical thickness of IL suggests that the difference in the physical thickness of the IL by the type of oxygen source might not be considerable.

Figure 4-6 (a) shows the O 1*s* core level XPS spectra for the H_2O- and O_3-La-silicate films with thickness of ~ 4 nm. The two peak features reflect that both silicate films consist of mixtures of SiO_2 phase (at a BE of ~533.0 eV [143]) and La_2O_3 phase (at a BE of ~531 eV [143]).

It can be understood that the SiO_2 phase dominates in the O_3-La-silicate film whereas the concentrations of La_2O_3 is slightly higher than that of SiO_2 in H_2O-La-silicate film. Since the difference in the IL thicknesses, which consists of mainly SiO_2, is not considerable as discussed above, the large difference in the peak intensity corresponding to SiO_2 phase implies that the Si concentration in the O_3-La-silicate film should be greater than that in the H_2O-La-silicate film. Si 2*s* core level spectra in Fig. 4-6 (b) confirmed the higher Si concentration of the O_3-La-silicate film than that of the H_2O-La-silicate film. The lower La 3*d* peak intensity in Fig. 4-6 (c) reflects the lower La concentration in the O_3-La-silicate film, and the higher BE shift and broadness of the La 3*d* peak might be attributed to the relatively less electron-donating nature of the second nearest-neighbor, i.e. Si–O bonding than La–O bonding due to the different electronegativity in the O_3-La-silicate film with the higher SiO_2 concentration. [144]

The higher Si concentration in the O_3-La-silicate film can be explained as follows. When the $La[N(SiMe_3)_2]_3$ molecules react with the surface hydroxyl group during their

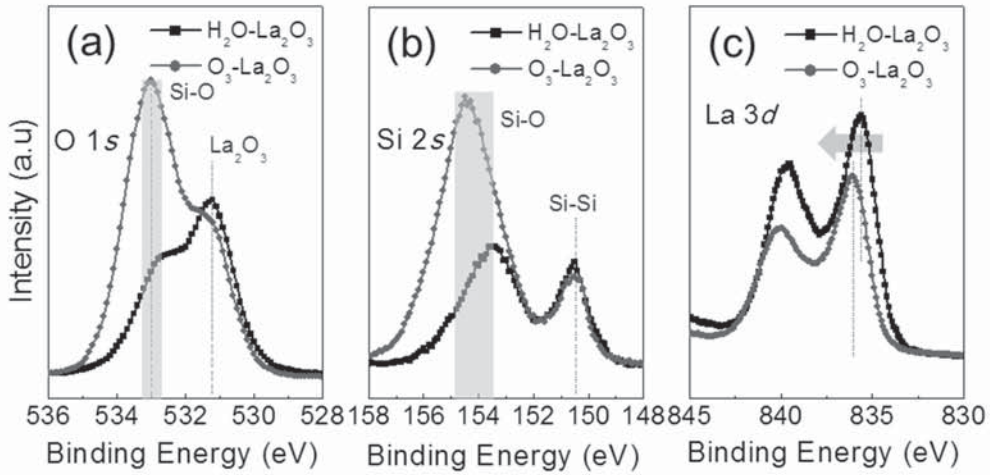


Figure 4-6. XPS spectra of (a) O 1*s*, (b) Si 2*s* and (c) La 3*d* core level of the La-silicate films grown with oxidants as a H_2O and an O_3.

pulse step or with the oxygen sources during the oxygen source pulse step, [–$N(SiMe_3)_2$] ligands are eliminated from the $La[N(SiMe_3)_2]_3$. The La bonding with the [–$N(SiMe_3)_2$] ligands is weak enough to be broken by the reaction with both oxygen sources. This was confirmed by N 1*s* core level spectra of Fig. 4.7 (a), which shows no bonding corresponding to the metal (La)–N phase (at a BE of ~397.8 eV [17]) for both of the O_3- and H_2O-La-silicate films.

The rather bulky nature of the [–$N(SiMe_3)_2$] ligand and the less affinity between the [–$N(SiMe_3)_2$] ligand and H (from OH group) could result in the re-adsorption of the ligand on the surface. There could be other by-products, such as CH_4, $OH(SiMe_3)$, as well as NH_3, but these can be easily removed during the purge step. [20, 23, 145, 146]

When active O_3 is pulsed, the remaining ligands may react with the O_3 or the O radical derived from O_3 to form non-volatile SiON and SiO_x species, which could be incorporated into the film despite of the following purge step. However, the weaker chemical activity of H_2O cannot induce the same reaction, so the remaining ligands are either removed during the following purge step or part of them are retained in the film, in which case contamination would result. This result is supported by N 1*s* core level spectra of Fig. 4-7 (a), where the O_3-La-silicate film shows an obvious peak at BE of ~ 400 eV corresponding to SiON and the H_2O-La-silicate film shows no peak at the BE. Therefore, the O_3-La-silicate film shows higher Si concentrations than the H_2O-La-silicate film as discussed above.

Figure 4-7 (b) shows the C 1*s* core level XPS spectra for H_2O- and O_3-La-silicate films. The peaks at BEs of ~ 285 and 290 eV correspond to adventitious C–C bonding (surface contamination) and La–CO_3 (from La-carbonate), respectively. [18] The peak intensity

corresponding to adventitious C–C bonding could be different between the O_3-La-silicate film and the H_2O-La-silicate film, because the film surfaces were occasionally contaminated by various organic contaminants when the samples were exposed to the atmosphere before loading into XPS analysis chamber. [18] Therefore, this difference in the peak intensity does not reflect the chemical structure of the film. The O_3 oxygen source effectively suppressed the accumulation of the La-carbonate phase in the film during ALD compared to H_2O, because the strong oxidation power of O_3 burned out the C-related residue, which was released from the ligands as a volatile CO_x. The dielectric performance of a film would be degraded by the La-carbonate phase, which would act as a conducting path through a film.

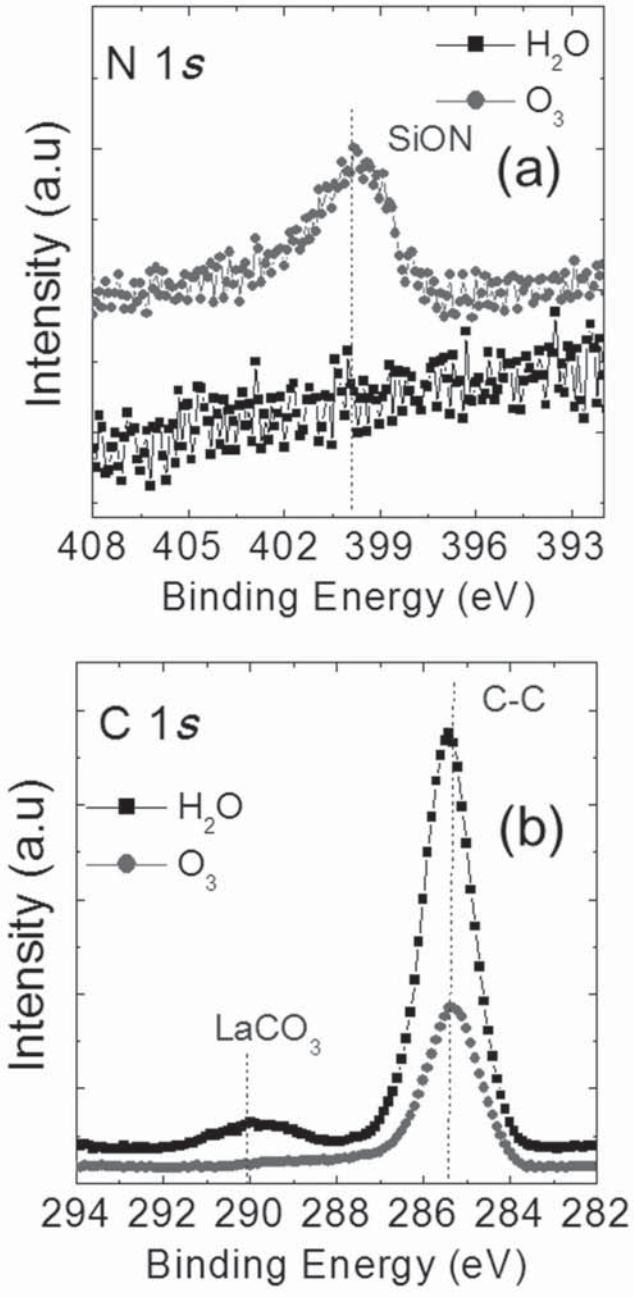


Figure 4-7. XPS spectra of (a) N 1*s* and (b) C 1*s* core level of the La-silicate films grown with H_2O and O_3.

4.1.5. Band gap Analysis of La-silicate film with different oxidants

The band structures of O_3- and H_2O-La-silicate films were examined by valence band XPS and O 1*s* XPS loss spectra. The valence band offset (VBO) was calculated by estimating the difference in energy between the valence bands of high-*k* gate dielectrics and Si (Fig. 4-8). [147] The deduced VBO values of H_2O- and O_3-La-silicate films were ~ 2.75 and ~ 2.99 eV, respectively. The band gap energy of the H_2O- and O_3-La-silicate films were estimated from the O 1*s* XPS loss spectra [148], as shown in Fig. 4-9. The band gap energy of H_2O- and O_3-La-silicate films was estimated to ~ 6.35 and ~ 6.92 eV, respectively. Based on this result, the band structures of the H_2O- and O_3-La-silicate films on a Si substrate could be reconstructed as shown in Fig. 4-10 and summarized at Table 4-1. The conduction band offset (CBO) of H_2O- and O_3-La-silicate films was ~ 2.48 and ~ 2.81 eV, respectively. The barrier height of the O_3-La-silicate film was higher than that of the H_2O-La-silicate film by ~ 0.33 and ~ 0.24 eV for electron and hole, respectively. It is natural that the O_3-La-silicate film has the higher band energy due to the higher Si concentration in the film.

Figure 4-11 shows a plot of CET vs. J_g measured at V_{FB} -2 V for the H_2O- and O_3-La-silicate films. The O_3-La-silicate film shows the superior dielectric performance over the H_2O-La-silicate film despite the higher Si concentration in the film and the lower *k* value. The J_g of the O_3-La-silicate film was approximately 3 orders of magnitude lower than that of the H_2O-La-silicate film at a similar CET value even though the O_3-La-silicate film was much thinner (~3-5 nm) than the H_2O-La-silicate film (~6-8 nm) [see Fig. 4-4].

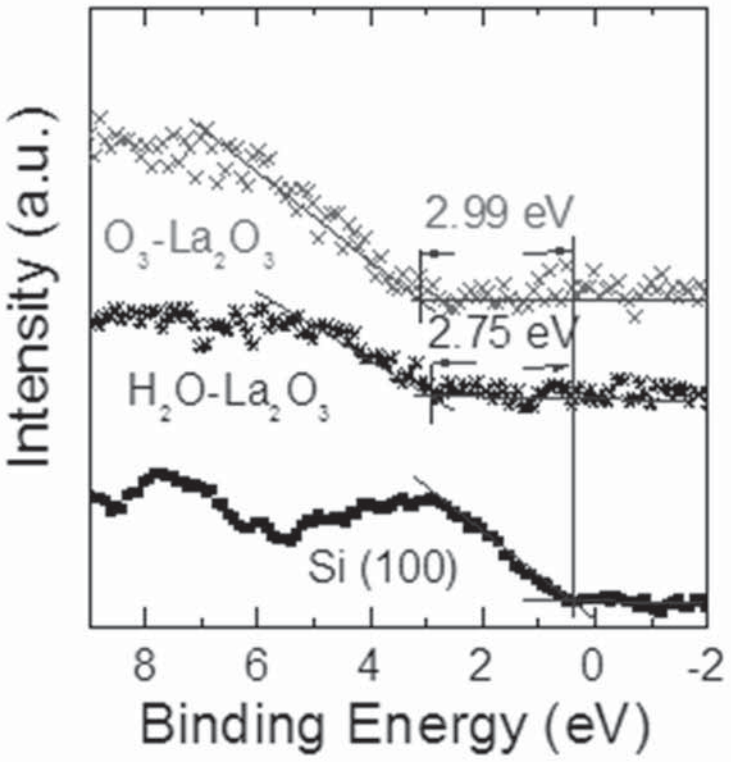


Figure 4-8. XPSpectra of Valence band for Valance Band Offset of La-silicate film grown H_2O and O_3.

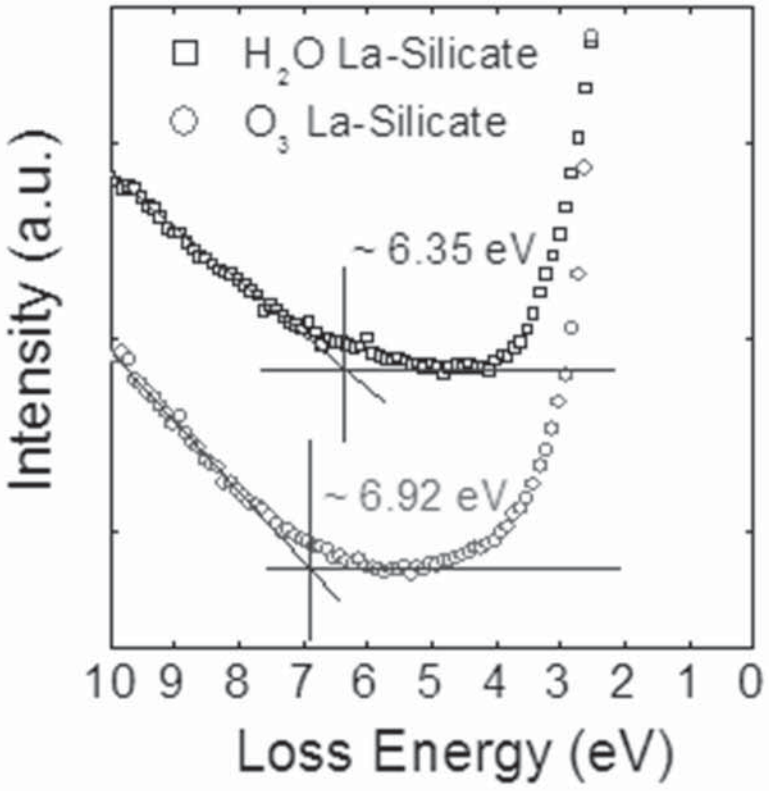


Figure 4-9. O 1*s* loss spectra for bandgap energy of La-silicate film grown H_2O and O_3.

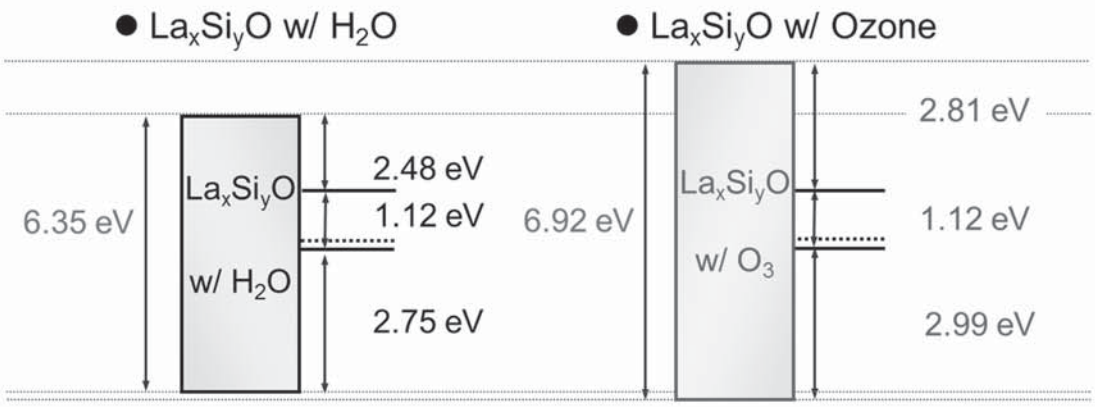


Figure 4-10. Reconstructed band structures for La-silicate films grown with H_2O and O_3.

Table 4-1. The deduced VBO, E_g and CBO of La-silicate grown with H_2O and O_3.

	VBO by XPS	**Band gap**	**CBO** = E_g - 1.12eV – VBO
La_xSi_yO + H_2O	**2.75 eV**	***6.35* eV**	**2.48 eV**
La_xSi_yO + O_3	**2.99 eV**	***6.92* eV**	**2.81 eV**

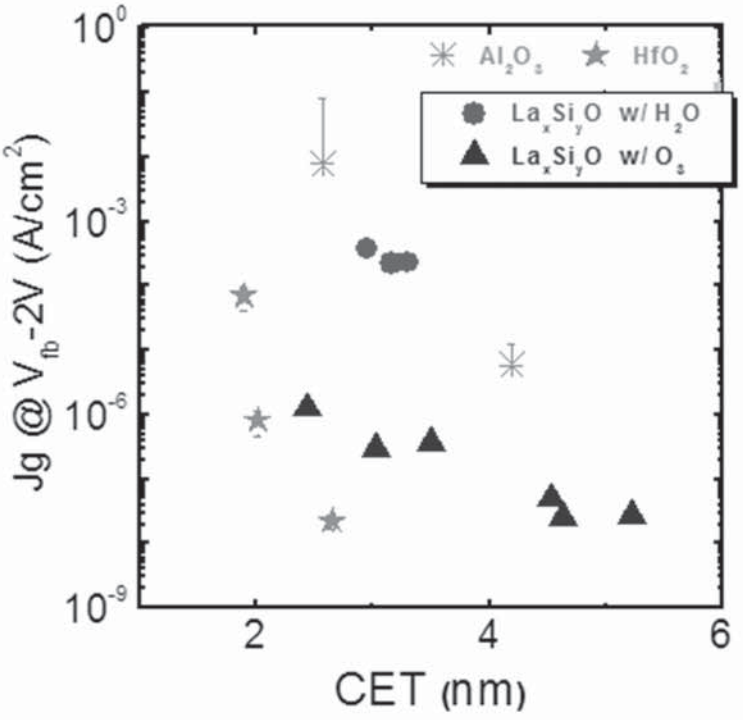


Figure 4-11. Insulating properties of La-silicate films grown with H_2O and O_3, references for ALD Al_2O_3 and ALD HfO_2 film were inserted.

4.2. La-silicate film on Ge on substrate

4.2.1. Introduction

Future dimensional scaling of CMOS devices requires the adoption of new materials to overcome the fundamental limitations of physical scaling. In concurrence with this trend, the conventional SiO_2 gate dielectrics with poly-Si gate electrodes have recently been replaced by Hf-based gate dielectrics with a metal gate in mass production. Moreover, to achieve further increased transistor performance, high-*k* gate dielectrics combined with the high mobility channel materials such as Ge and III-V compound semiconductors have attracted lots of attention. Of these candidates, Ge substrate is of particular interest for the future CMOS devices due to its higher electron (x 2) and hole (x 4) mobility compared to Si substrate.

The implementation of atomic layer deposited high-*k* dielectrics on Ge substrates has the potential to become a mass production compatible process. However, atomic layer deposition (ALD) is only possible in certain temperature ranges, the so called ALD windows. It was reported that when high-*k* oxide such as HfO_2 films are grown on a Ge substrate by ALD, they react with the substrate during the deposition process, which results in the degradation of structural and electrical properties. [81, 149]

A typical example of this degradation is the very large hysteresis in the C-V property. This originates from the intermixing between high-*k* oxide such as HfO_2 and the oxidized Ge substrate, which creates electrically active defects near the interface. [81, 149] Moreover, Ge oxides thermally decompose and easily desorb from the surface at

relatively low temperatures [28], and these unstable Ge oxides also form trap sites at the surface, leading to the further degradation of electrical properties. In order to suppress the formation of these defective Ge oxides, various surface passivation techniques such as surface nitridation [108], Si passivation layers [39], plasma oxidation [126], and high pressure oxidation [78] have been reported. However, these passivation layers were failed fully prevent the formation of defective Ge oxides during the following annealing processes, which results in the degradation electrical properties.

Among the various passivation techniques, Si capping layer on a Ge substrate has drawn a great deal of attention due to its superior electrical performance. Cheng et al. reported that the Si capping layer on a Ge substrate retards GeO volatilization and suppresses the C-V hysteresis of the HfO_xN_y gate dielectric films in the MOS structure. The reduced C-V hysteresis by the Si capping layer was explained by the fact that Si-O bonds have larger Gibbs free energies and higher thermodynamic stabilities than Ge-O bonds, so that the reaction between the oxide and Ge substrate could be efficiently suppressed. [39] In most of the previous studies, Si capping layer on a Ge substrate was formed by either epitaxial growth of several mono-layers of Si or annealing in a SiH_4 (or Si_2H_4) ambient. [40] However, not much of the studies related to the atomic layer deposited Si-containing passivation layers on a Ge substrate have been reported. [32]

Houssa et al. simulated the atomic configuration of the interface between various rare-earth oxide material and Ge by first principles calculation. [36] This result gives feasibility of La_2O_3 and Al_2O_3 as effective passivation layer on Ge to suppress dangling bonds than HfO_2. Kato et al. reported an Al_2O_3 interlayer effectively suppresses the formation of a Ge oxide interlayer in a lanthanum (La) oxide/Al_2O_3/Ge gate stack

structure. The formation of GeO_x is suppressed with increasing thickness of the Al_2O_3 interfacial layer up to 1 nm. In contrast, the adoption of capping layer, which could suppress the volatilization of GeO from the GeO_2 surface, and, thus, the accompanying interfacial reaction, has not been well studied compared with the interfacial passivation layer approach. [41] In this study, therefore, the atomic layer deposited ultra-thin Al_2O_3 and SiO_2 layers were adopted as the interfacial passivation and capping layers, respectively, for the lanthanum-silicate (La-silicate) film high-*k* film on Ge substrate. The La-silicate films were atomic layer deposited by sequential injection of the Si containing Tris[bis(trimethylsilyl)amino]lanthanum ($La[N(SiMe_3)_2]_3$) and Ozone (O_3) as La-precursor and oxygen source, respectively. Atomic layer deposition (ALD) are known as the most feasible and competitive process in fabrication of high quality gate dielectric thin films with conformal deposition and high accuracy in thickness control, making it excellently compatible with the semiconductor fabrication technology for mass-production. During deposition of La-silicate films, $SiH_2(NC_2H_5CH_3)_2$ (BEMAS) and $SiH_2(N(C_2H_5)_2)_2$ (BDEAS) were additionally injected in order to control the Si concentrations (Si/(La+Si)) in the high-*k* film and its effect on electrical properties. An ultrathin interfacial Al_2O_3 layers of which thickness was controlled by deposition cycles (~2, 3, 5, 10 cycles) were formed between the La-Silicate film and Ge substrate by another ALD. Additionally, ALD SiO_2 was chosen as the material for the capping layer on La-silicate film. The multi stack of Al_2O_3 passivation, high-*k* La-silicate, and capping SiO_2 layers was effectively decreased the C-V hysteresis down to 80 mV, which is one of the best results reported up to date.

4.2.2. Effects of La-silicate film as passivation layer of HfO_2 film

The structure and electrical properties of single layer La-silicate films were examined first for the different Si concentrations. Figure 4-12 shows the CET variation of as-deposited La-silicate films on Ge substrate as a function of their physical thickness. The dielectric constant of as-deposited La-silicate films with only $La[N(SiMe_3)_2]_3$ precursor was ~14.2.

Effect of La-silicate film as passivation layer thickness dependence on C-V hysteresis is shown as Fig 4-13 (b). The 6 nm thickness of HfO_2 film was deposited at 200°C after either of La-silicate, BEMAS SiO_2 or BDEAS SiO_2 interface passivation layer deposition at 310°C, MOSCAP formed as Fig. 4-13 (a). Various thickness for passivation layer were deposited as 0 ~ 2.0 nm controlled by ALD deposition cycles. As increasing in La-silicate passivation interface layer thickness C-V hysteresis decreased but there was an inconsequent effect of SiO_2 as passivation layer thickness dependence.

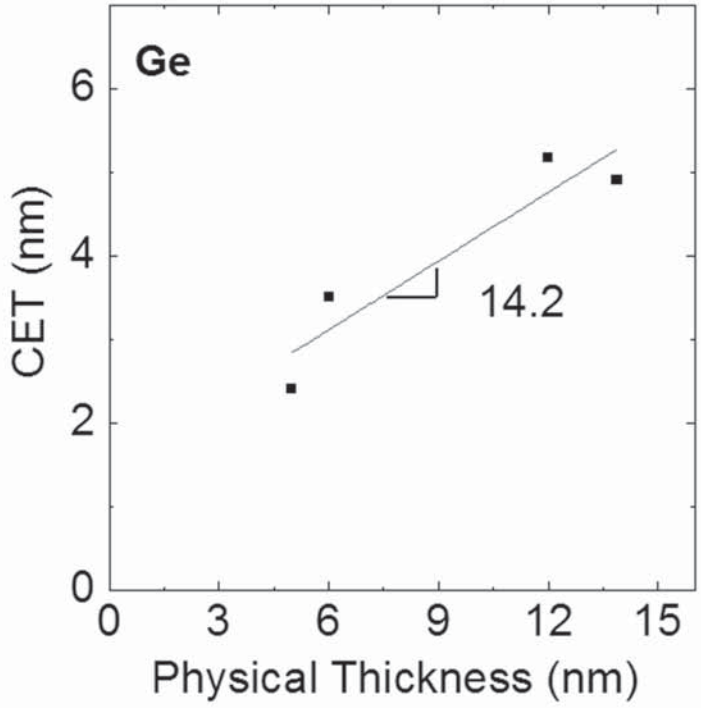


Figure 4-12. CET vs. physical thickness of deposited La-silicate film on Ge substrate.

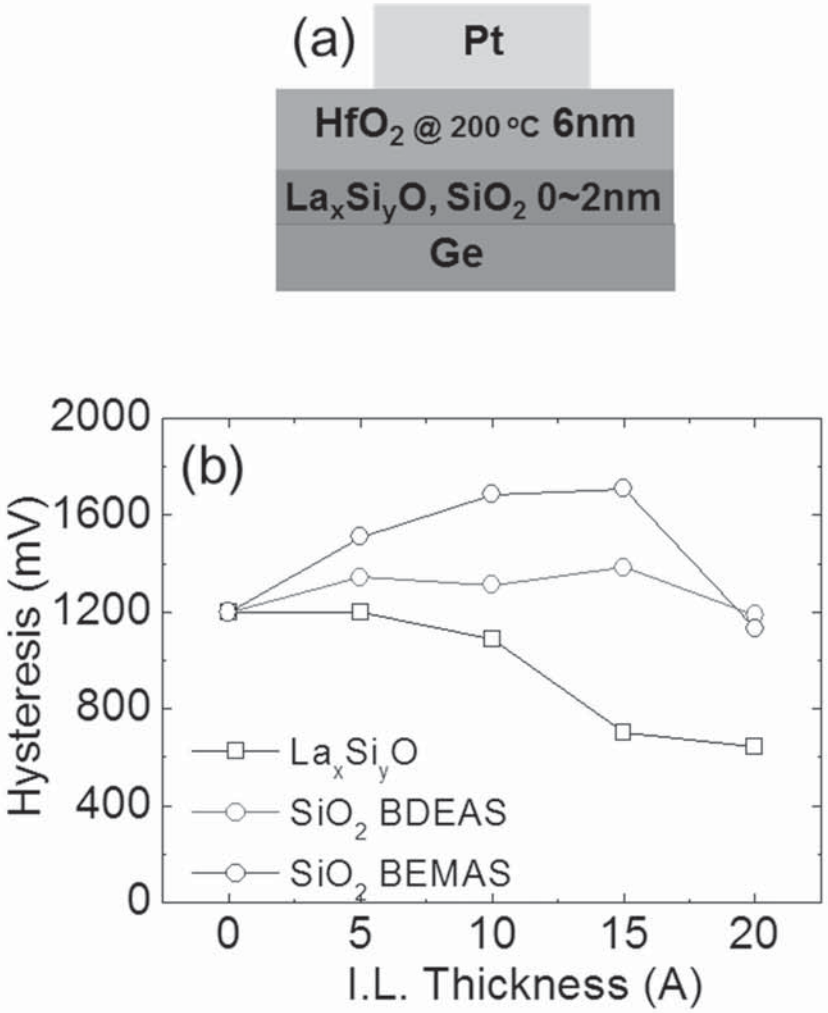


Figure 4-13. (a) Schematic view and (b) C-V hysteresis change of La-silicate, BEMAS and BDEAS SiO_2 film as passivation layer for HfO_2 on Ge substrate as a function of interface passivation layer thickness.

4.2.3. Effects of Si concentrations in La-based oxide film

In this set of experiments, the La_2O_3 film was deposited using $La(^iPrCp)_3$ precursor, La-silicate film was deposited using Si-containing La precursor $La[N(SiMe_3)_2]_3$ and Si concentrations controlled La-silicate film was deposited by $La[N(SiMe_3)_2]_3$ precursor and SiO_2 precursors such as BEMAS or BDEAS. BEMAS or BDEAS was used as the Si-precursor to dope the La-silicate film with Si. The Si concentrations in as-deposited La-silicate films by only $La[N(SiMe_3)_2]_3$ precursor were ~ 25 % which is confirmed by Auger depth profile as shown in Fig. 4-14 (b). Figure 4-14 (a) shows that the Si concentration for non-doped La_2O_3 is indeed below the detection limit of AES (< ~1%). The diffusion of Ge into the La_2O_3 film was also minimized under this condition.

The ALD cycle ratio of SiO_2 and La-silicate was controlled to be ~30 % (data not shown) and ~ 35 % (Figs.4-14 (c) and (d)) with the ratios of [Si/(La+Si)], respectively. Here, BEMAS and BDEAS was adopted as the Si-precursor and the results with those Si-precursor were almost identical in the films as shown in Figs. 4-14 (c) and (d).

Figure 4-14 (e) shows the AES depth profile result of ALD SiO_2 film using BEMAS precursor, which reveals that the Ge concentration in ALD SiO_2 was almost negligible. The Si ratios were obtained using the average concentrations of La and Si through the oxide layer in AES results. An interesting finding is that the Ge concentration in the La-silicate film was much higher than the non-doped La_2O_3 film and SiO_2 film while the Ge concentration is almost independent of the Si concentration under these experimental conditions.

To understand the influence of these chemical changes in the films, C-V measurements were performed for a given oxide film thickness of ~6 nm, which includes the possible

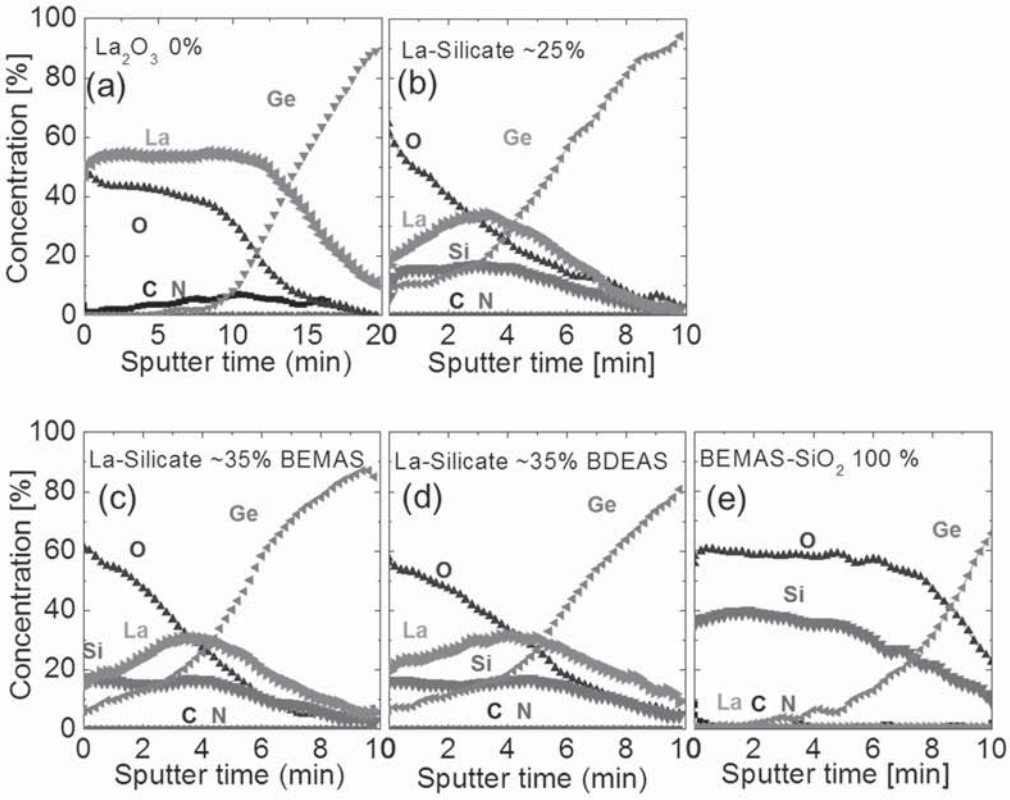


Figure 4-14. AES depth profiles of (a) La_2O_3 thin film, (b) La-silicate thin film, Si concentrations controlled La-silicate film by (c) BEMAS-Si precursor, (d) BDEAS-Si precursor and (e) SiO_2 thin film by BEMAS precursor.

interfacial layer thickness.

The C-V hysteresis and CET values were examined from the C-V curves when the gate voltage is swept from depletion (positive voltage) to accumulation (negative voltage) and back to depletion regions. The C-V hysteresis was extracted from the flat band voltage difference in the two C-V curves during the forward and reverse sweeps. Figure 4-15 shows the variations in the C-V hysteresis voltage (left hand ordinate) and CET (right hand ordinate) of the oxide films as a function of Si concentrations. The CET increases slightly with increasing Si concentrations in La-silicate film due to the decreased *k*-value of the oxide layer. However, the variation was not large compared with the hysteresis voltage. This suggests that the non-doped film undergoes more serious interfacial reaction resulting in the thicker interfacial layer thickness, which has a lower *k* value compared with the La_2O_3 film. When the La_2O_3 film was deposited directly onto the HF cleaned Ge substrate, a significantly large C-V hysteresis of ~ 1000 mV was observed, suggesting that a high density of electrically active defects were created near the interface. [29] The almost negligible Ge concentration in the La_2O_3 film suggests that the La_2O_3 layer cannot prevent the volatilization of GeO produced by the disproportionation reaction at the interface, which could cause the high interfacial defect density. This must be also the case for the ALD SiO_2 film, suggesting that the non-doped ALD single layer cannot prevent the deleterious interfacial reaction.

In contrast, when Si concentration of La-silicate film was increased from 0% to ~ 35%, C-V hysteresis was decreased by ~ 40%, and the hysteresis voltage became ~ 600 mV, when the Si concentration was ~ 35%. The relatively high Ge concentration in the film suggests that the volatilization of GeO from the film surface was suppressed to certain

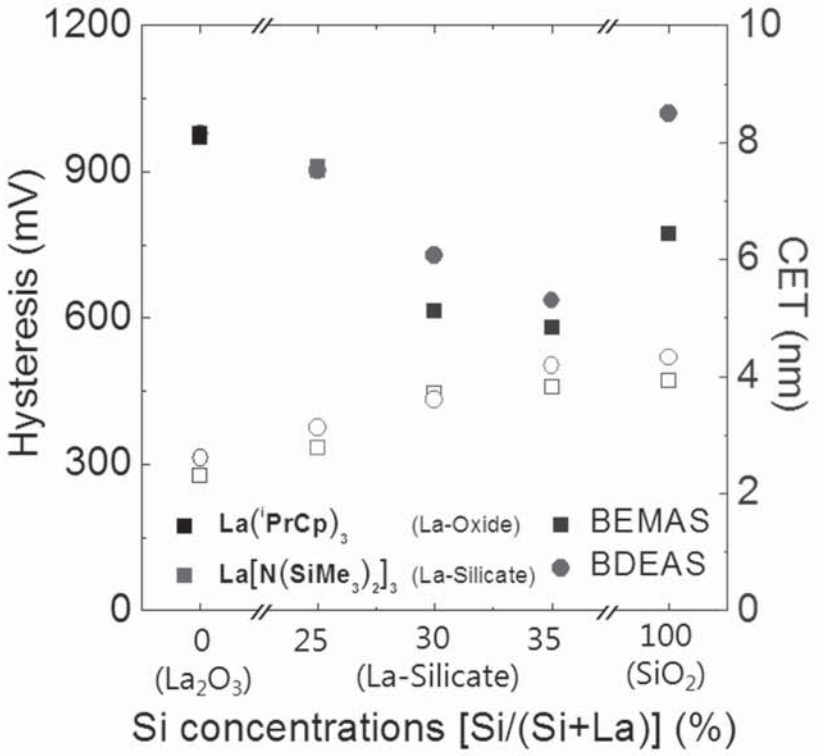


Figure 4-15. C-V Hysteresis and CET as a function of Si concentrations of La-based oxide films.

degree, which induced less interfacial reaction with the Ge substrate.

In order to achieve a better understanding on these behaviors, the chemical bonding states of various La-silicate films on Ge substrate were examined by XPS. The degree of formation of Ge oxides is especially focused in XPS. Figure 4-16 (a) shows Ge 3*d* spectra of pure- La_2O_3 and pure- La-silicate film with a Si concentration of ~ 25%. The energy scale was calibrated by fixing the Ge 3*d* line of the bulk Ge at a binding energy (BE) of 29.4 eV, which could be clearly observed by the thin thickness of the films. The clear emergence of bulk Ge 3*d* spectra suggests that the Ge 3*d* signal originated from not only the oxide layer but also interfacial layer. A clear peak at BE higher than that of bulk Ge was observed, and the spectra related to Ge oxide could be deconvoluted into four Ge oxide peaks (Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+}) with BE shifts of 0.8, 1.8, 2.6, and 3.4 eV, respectively summarized as Table 4-2. [77, 150]

While the explicit deconvolution was not attempted in Fig. 4-16 (a), the lower BE shift of 2.91 eV of the Ge-oxide peak for the case of La_2O_3 suggests that the Ge ions in Ge-oxide layer have mixed valences of Ge^{4+} and Ge^{3+}. The lack of Ge-signal in the La_2O_3 layer in Fig. 4-16 (a) reveals that the Ge-oxide layer in this film mainly located that the interface between the La_2O_3 film and Ge substrate. The generation of Ge^{3+} components can be considered to contribute to the large hysteresis voltage in the C-V curves as well as the D_{it} even at the cost of increasing the CET. [29] The peak component related to the Ge oxides of La-silicate film have ~ 0.12 eV higher BE than that of La_2O_3 film.

The explicit deconvolution for Ge-oxide peak for both La_2O_3 and La-silicate film were attempted in Fig. 4-17. La_2O_3 film have more Ge sub oxide peak (sum of Ge^{1+}, Ge^{2+} and Ge^{3+}) peak (Fig. 4-17 (a)) than La-silicate film shown on Fig. 4-17(b).

In addition, also the oxide peak intensity was much lower than that of La_2O_3 film despite the fact that the oxide peak could be contributed by the Ge-oxide in the La-silicate film (Fig. 4-14 (b)). This result suggests that La-silicate film has suppressed generation of Ge oxide at the Ge interface.

Table 4-2. Ge 3*d* spectra related to Ge oxide (Ge^{1+}, Ge^{2+}, Ge^{3+} and Ge^{4+}) with BE shifts of 0.8, 1.8, 2.6, and 3.4 eV from Ge bulk peak.

Ge 1: Bulk Ge - Ge_2O : 0.8 eV
Ge 2: Bulk Ge - GeO : 1.4 - 1.8 eV
Ge 3: Bulk Ge - Ge_2O_3 : 2.6 - 2.7 eV
Ge 4: Bulk Ge - GeO_2 : 3.2 - 3.4 eV

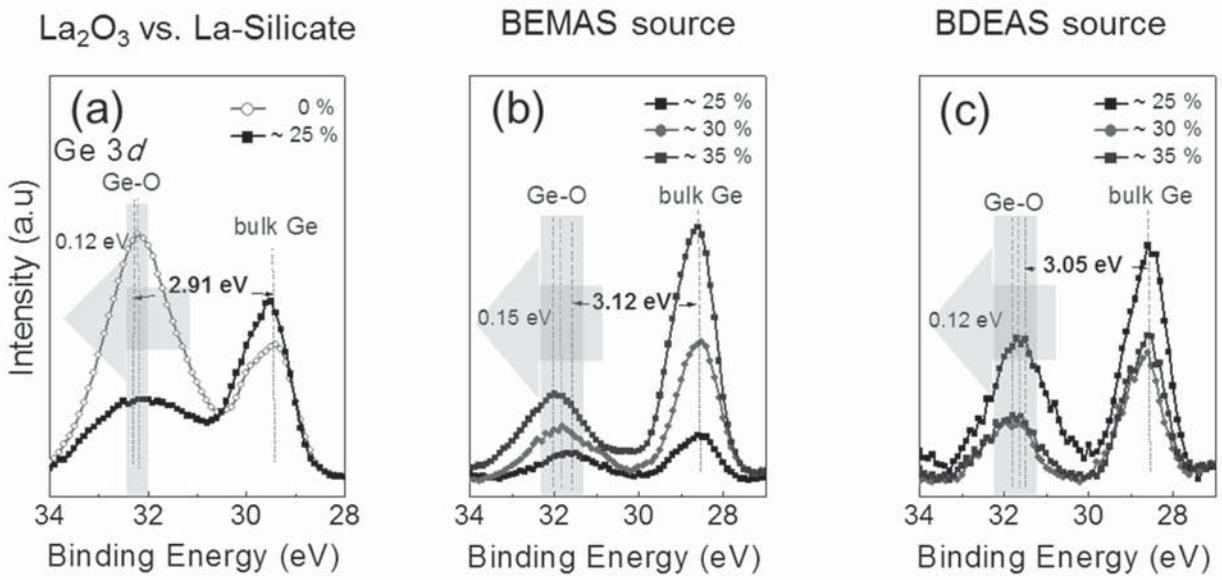


Figure 4-16. Ge 3*d* core level of (a) pure- La-oxide and pure- La-silicate film with a Si concentration of ~ 25%, (b) Si concentrations controlled La-silicate film using BEMAS precursor and (c) Si concentrations controlled La-silicate film using BDEAS precursor.

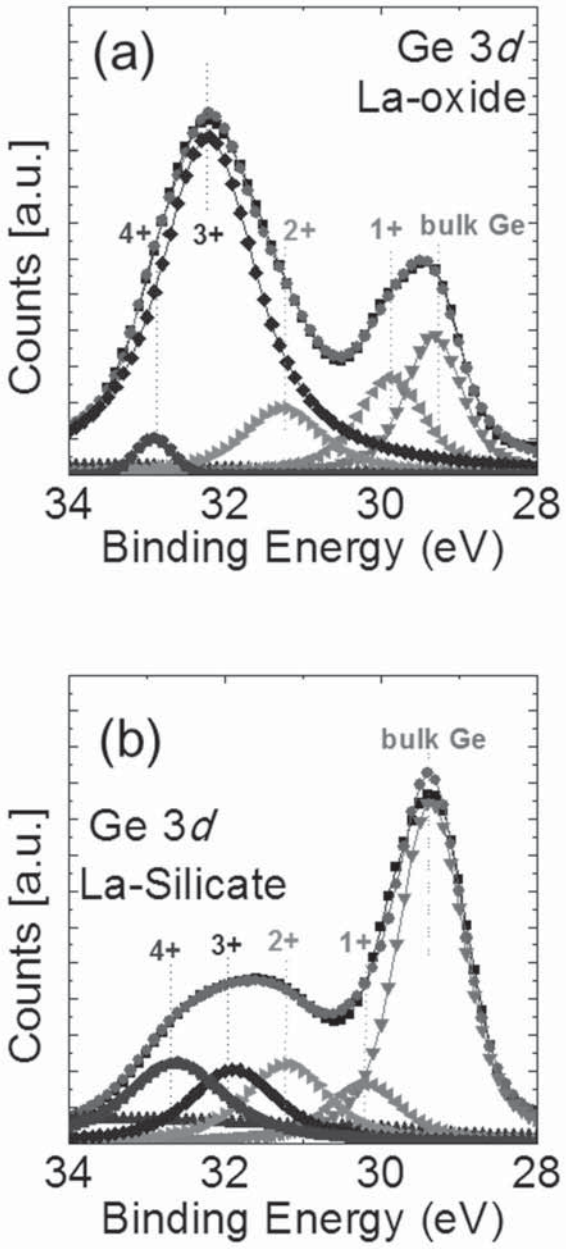


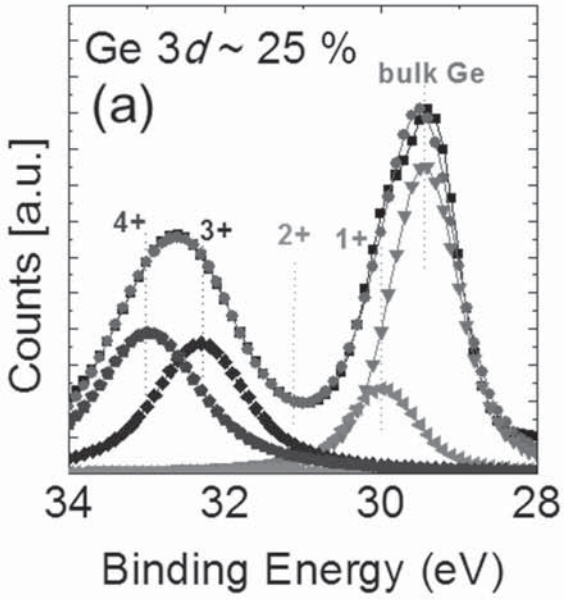
Figure 4-17. Ge 3*d* core level for the explicit deconvolution for Ge-oxide (a) pure- La-oxide and (b) pure- La-silicate film (with a Si concentration of ~ 25%).

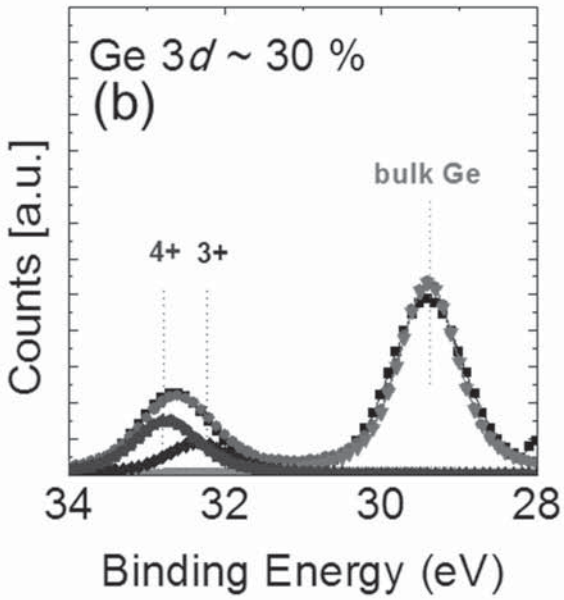
Spectra in Figs. 4-16 (b) and (c) were obtained from Si concentrations controlled La-silicate films with BEMAS Si precursor and BDEAS Si precursor, respectively. Here, $La[N(Si(CH_3)_3)_2]_3$ was adopted as the La-precursor, which resulted in the Si concentration of 25 % shown as Fig 4-14 (b) when no additional BEMAS or BDEAS pulse steps were added.

The BE shift of Ge 3*d* peak from the the La-silicate films with Si concentration of ~25% was 3.12 eV and 3.05 eV in Figs. 4-16 (b) and (c), respectively, which are in reasonable accordance with the result in Fig. 4-16 (a). It was increased by ~ 0.15 eV and 0.12 eV in Figs. 4-16 (b) and (c), respectively, when the Si concentration increased to ~ 35 %.

The explicit deconvolution of Ge-oxide peak for Si controlled La-silicate film by BEMAS Si precursor was attempted in Figs. 4-18. Ge dioxide concentration is defined as GeO_2 (Ge^{4+}) / Ge sub oxide peak (sum of Ge^{1+}, Ge^{2+} and Ge^{3+}). Ge dioxide concentration was increased by 40.4 %, 61.6 % and 67.8 % in Figs. 4-18 (a), (b) and (c) respectively, when the Si concentration increased to ~ 25 %, ~ 30% and ~35 %. Figure.4-19 shows the explicit deconvolution for Ge-oxide peak of Si controlled La-silicate film by BDEAS Si precursor. Ge dioxide concentration was increased by 43.7 %, 59.4 % and 66.6 % in Figs. 4-19 (a), (b) and (c) respectively, when the Si concentration increased to ~ 25 %, ~ 30% and ~35 %. As increasing Si concentration in La-silicate film with either BEMAS or BDEAS source, higher Ge dioxide peak was shown in both La-silicate films.

These results commonly suggest that higher Si concentrations in La-silicate films suppressed Ge sub-oxide formation on Ge interface and accompanying disproportionation reaction which was effective in decreasing the C-V hysteresis voltage.


Ge 3d ~ 25 %
(a)
bulk Ge
4+
3+
2+
1+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)


Ge 3d ~ 30 %
(b)
bulk Ge
4+
3+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)

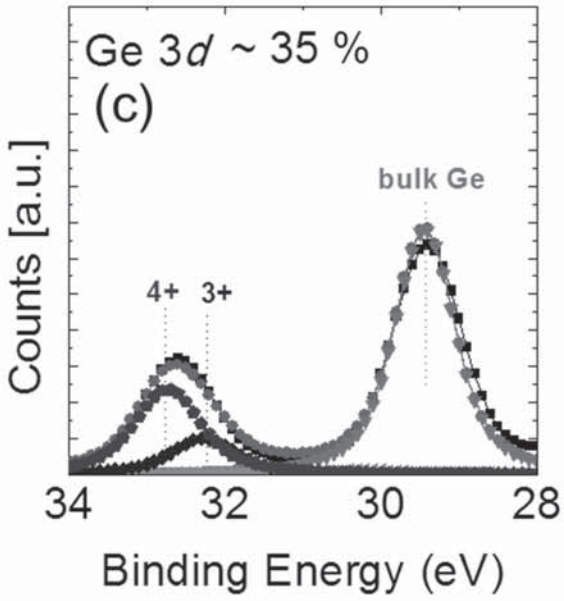
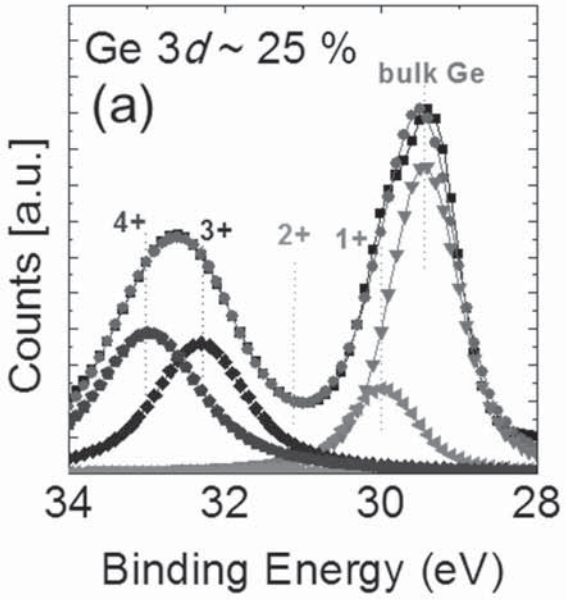
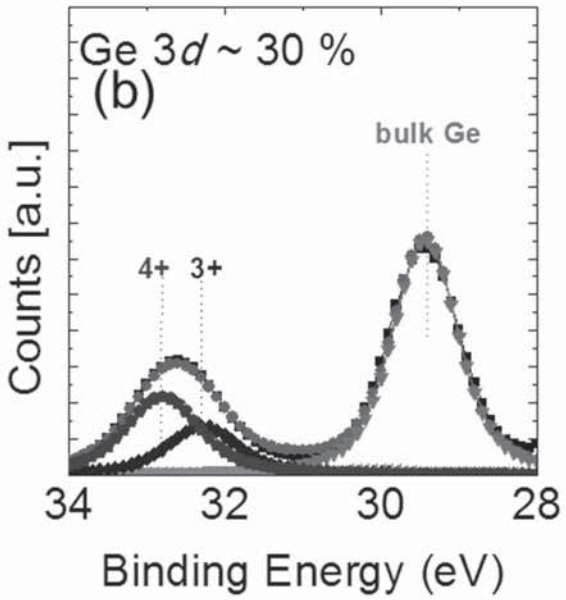


Figure 4-18. Ge 3*d* core level for the explicit deconvolution for Ge-oxide (a) pure-La-silicate film with a Si concentration of ~ 25%, La-silicate film with a Si concentration of (b) ~ 30% and (c) ~35 % using BEMAS precursor.


Ge 3d ~ 25 %
(a)
bulk Ge
4+
3+
2+
1+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)


Ge 3d ~ 30 %
(b)
bulk Ge
4+
3+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)

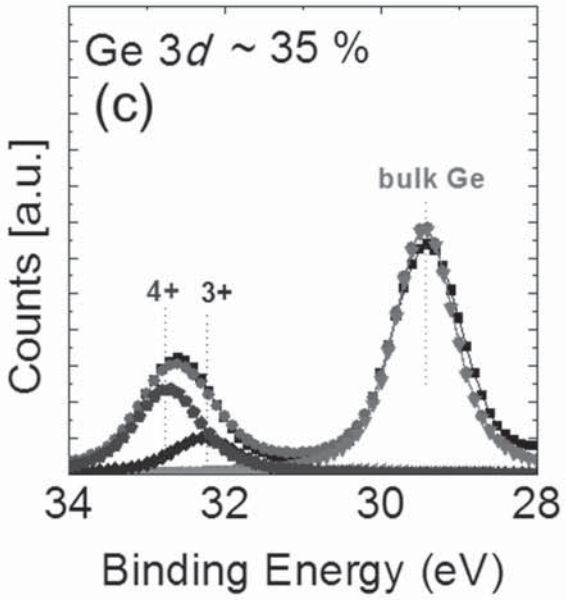


Figure 4-19. Ge 3*d* core level for the explicit deconvolution for Ge-oxide (a) pure-La-silicate film with a Si concentration of ~ 25%, La-silicate film with a Si concentration of (b) ~ 30% and (c) ~35 % using BDEAS precursor.

Figure 4-20 shows the C-V curves for CVS (with a gate stress voltage of -2.5 V) on MOS capacitor with the structures of (a) Pt/La-oxide/*p*-Ge and (b) Pt/La-silicate (~ 25 % Si concentration)/*p*-Ge. The C-V curves are recorded for fresh samples under forward and reverse bias sweeps with a gate voltage sweep rate of 50 mVs^{-1}, and after 8 successive stresses (0, 1, 4, 10, 32, 100, 317, 1000 s). The flat-band voltage shift (ΔV_{FB}), which is related to the fixed charge trapping in the devices, and the slope change of C-V curve, which is related to the generation of fast interface trap states, could be noted in the figure.

The La-oxide film shows large ΔV_{FB} into the negative voltage direction as well as the changes in the slopes of the C-V curves, while the La-silicate film shows notable change in only slopes of the C-V curves. This suggests that the deterioration of bulk properties for La-oxide film (fixed charge generation) is higher than La-silicate film.

Larger C-V hysteresis of La-oxide film than La-silicate film, therefore, was due to larger bulk trap charge and its interface trap density. The XPS and CVS results suggest that higher Si concentrations in La-based films suppressed Ge sub-oxide formation on Ge interface and bulk traps in the films, which was effective in decreasing the C-V hysteresis. Figure 4-21 shows TEM images for (a) La-oxide and (b) La-silicate films. Thickness for deposited La-oxide and La-silicate film was confirmed by ~ 6.0 nm.

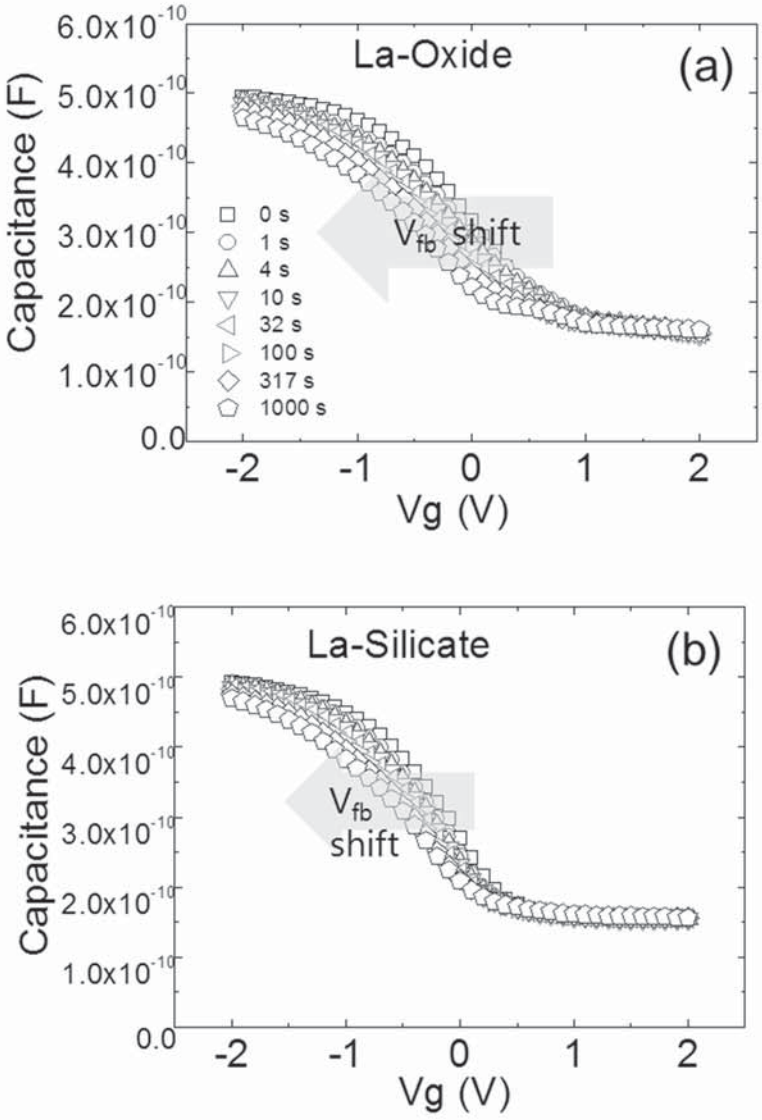


Figure 4-20. C-V curves for CVS (with a gate stress voltage of -2.5 V) on MOS capacitor with the structures of (a) Pt/La-oxide/*p*-Ge and (b) Pt/La-silicate (~ 25 % Si concentration) /*p*-Ge.

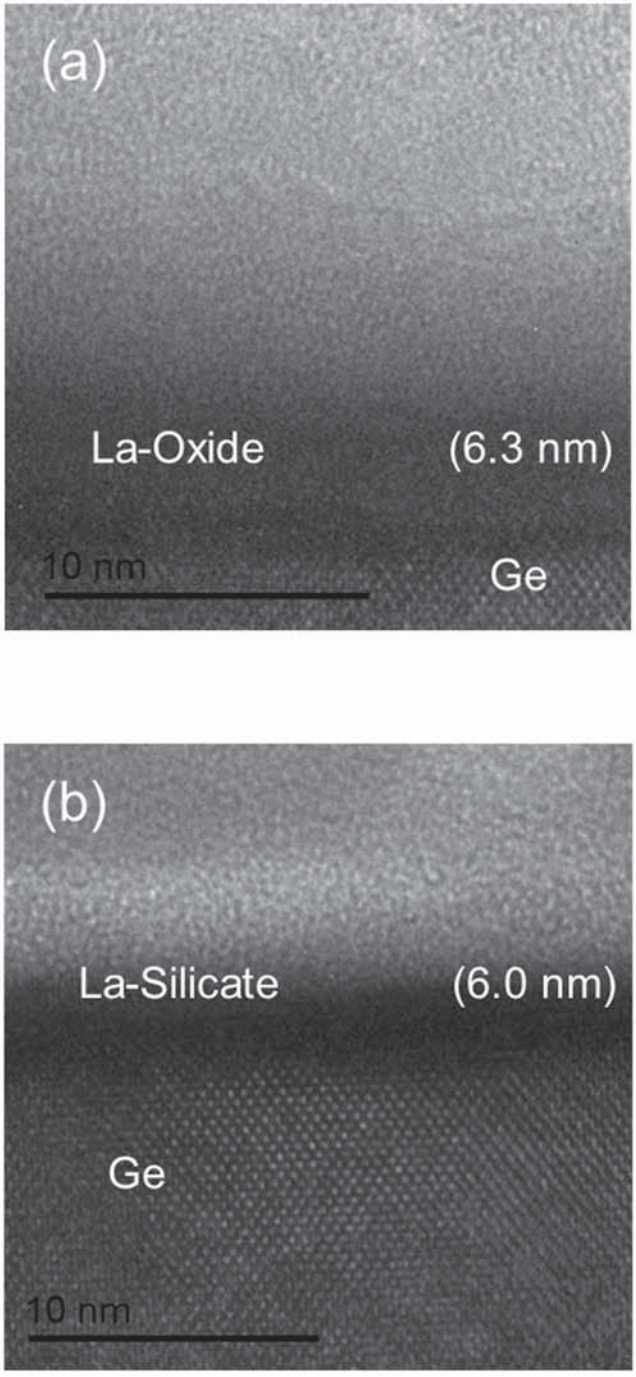


Figure 4-21. TEM images for (a) La-oxide and (b) La-silicate films on Ge.

4.2.4. Effect of SiO_2 and Al_2O_3 as passivation interface layer and capping layer of La-silicate film.

In order to further improve the interface quality and thus decrease the C-V hysteresis, various thickness of SiO_2 and Al_2O_3 thin film were capped on La-silicate film (~ 25% for Si concentration) shown as Fig. 4-22 (a) and 4-23 (a) or intervened between the La-silicate film and Ge substrate shown as Fig. 4-22 (b) and 4-23 (b).

Capping SiO_2 was successfully decreased C-V hysteresis as SiO_2 thickness increased, but SiO_2 passivation layer was not appropriate for reducing C-V hysteresis shown in Fig. 4-22 (c) due to its interface relationship with Ge substrate. On other hands, SiO_2 film as capping layer was effective to reduce C-V hysteresis. Especially 2-3 nm of SiO_2 capping layer reduced C-V hysteresis. Figure 4-24 (a) schemed possibility for Ge disproportionation effect in SiO_2 capping system. Somehow, SiO_2 capping layer on La-silicate film form "closed system" to enhance Ge interface density to improve electrical property.

Al_2O_3 passivation layer was successfully decreased C-V hysteresis as Al_2O_3 thickness increased, but Capping Al_2O_3 was not shown as Fig. 4-23 (c). Al_2O_3 passivation layer was most effective to reduce C-V hysteresis until thickness of ~ 1 nm, due to Ge and Al_2O_3 interface characteristic. Figure 4-24 (b) was contrived possibility for suppressing GeO desorption from Ge substrate by Al_2O_3 passivation interface effect. C-V measurement was converted to electric field to eliminate effect of physical thickness.

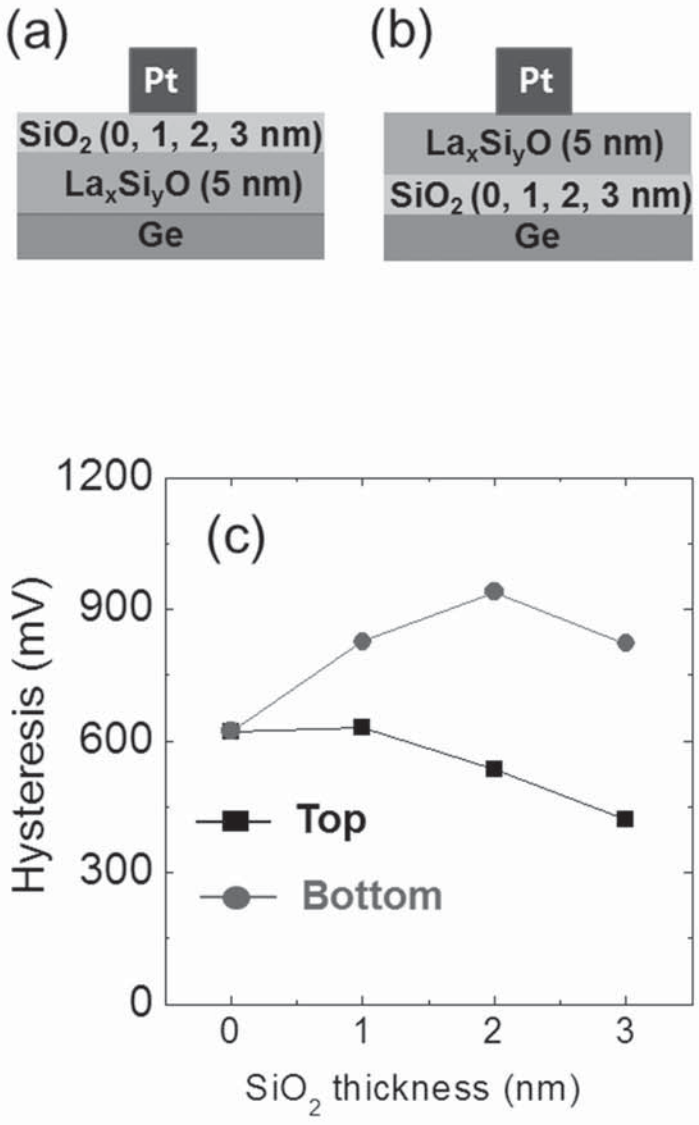


Figure 4-22. Schematic diagrams of La-silicate MOSCAP for (a) SiO_2 capping, (b) SiO_2 passivation interface layer and (c) C-V hysteresis change as a function of SiO_2 thickness change.

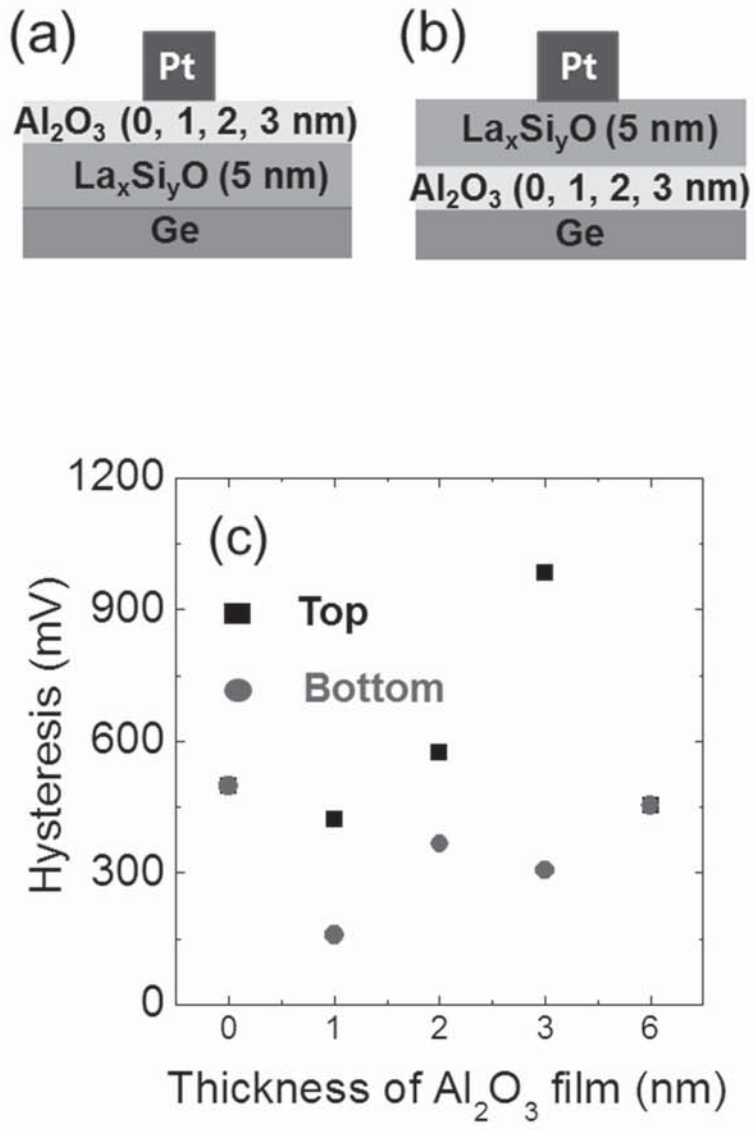


Figure 4-23. Schematic diagrams of La-silicate MOSCAP for (a) Al_2O_3 capping, (b) Al_2O_3 passivation interface layer and (c) C-V hysteresis change as a function of Al_2O_3 thickness change.

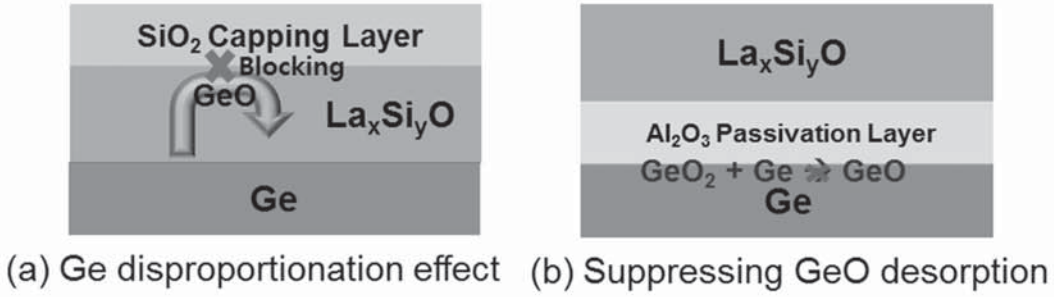


Figure 4-24. Schematic views for (a) SiO_2 capping effect as Ge disproportionation and (b) Al_2O_3 passivation layer effect as suppressing GeO desorption.

4.2.5. Adoption of Al_2O_3 interface passivation layer

In order to further improve the interface quality and thus decrease the C-V hysteresis, thin Al_2O_3 layer was intervened between the La-silicate film (25% for Si concentration) and Ge substrate. The thickness of Al_2O_3 was varied by varying the deposition cycles from 2 to 10 cycles with the deposition cycles of 10 being coincident with 1 nm thickness of Al_2O_3 thin film. MOSCAP for ~6 nm of La-silicate film with ultra-thin Al_2O_3 passivation layer was fabricated as shown in Fig. 4-25 (a).

The C-V curve shifted toward the positive voltage direction progressively with increasing Al_2O_3 deposition cycles since negative fixed charges are introduced into Al_2O_3 films. [12, 151] Figure 4-26 shows flat band voltage shifted toward to positive direction as Al_2O_3 deposition cycles increased. From this results, Al_2O_3 layer as passivation layer deposited with cycle number was confirmed.

Figure 4-25 (b) shows the variations in the C-V hysteresis voltages of La-silicate film as a function of Al_2O_3 deposition cycles and that of Al_2O_3 film. When deposition cycles of 2 and 3 cycles of Al_2O_3 passivation interface layer was inserted between La-silicate and Ge substrate, the C-V hysteresis showed lowest value (~250 mV), whereas further increased Al_2O_3 cycles increases the value to ~350mV when 10 cycles were adopted. The C-V hysteresis of ~ 6-nm-thick Al_2O_3 layer was ~550 mV, suggesting that the appropriate combination of the La-silicate layer and interfacial passivation Al_2O_3 layer (2 ~ 3 cycles) is required to decrease the C-V hysteresis shown in Fig. 4-25 (b).

Figure 4-27 (a) - (c) show the AES depth profile results of the samples shown in Fig. 4-24. La-silicate film has higher La and lower Ge concentrations than that of La-silicate film with Al_2O_3 passivation layer. GeO desorption modeling suggested that V_o made at

interface of Ge substrate, that V_o is possible to exchange with La and make La-Ge-O bonding which suggest high La concentrations inside of Ge substrate in Fig. 4-27 (b).

Also, It might suggest that La-silicate film with Al_2O_3 passivation layer has suppressed GeO desorption than La-silicate film due to residual Ge concentration in the La-silicate layer.

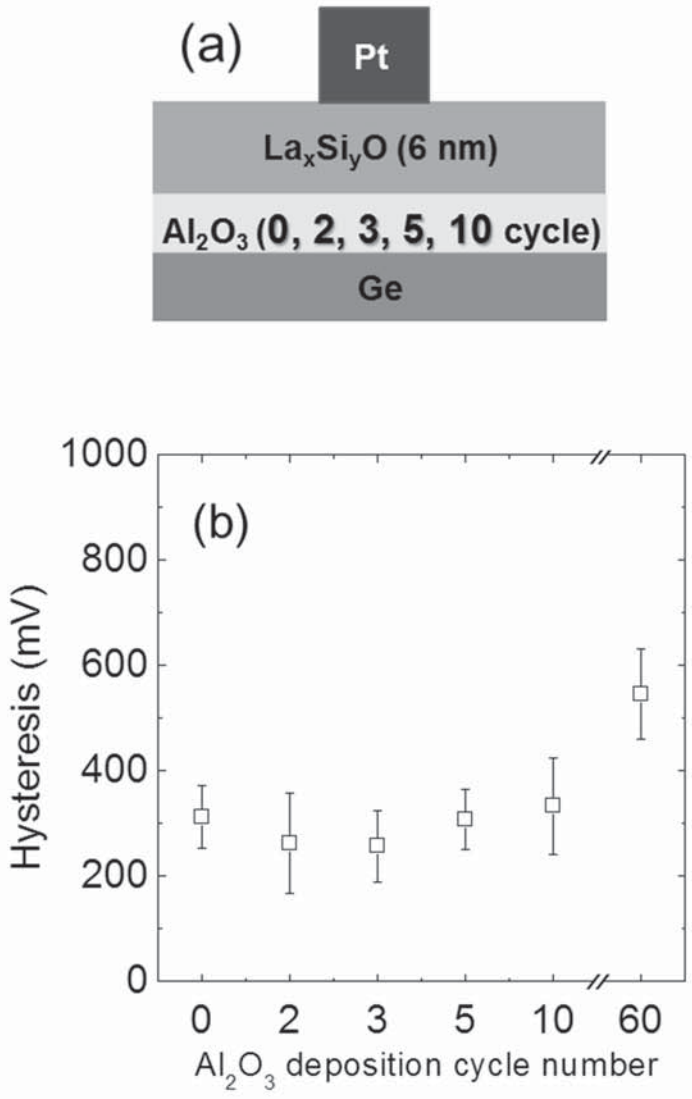


Figure 4-25. (a) Schematic diagrams of La-silicate MOSCAP with ultra-thin Al_2O_3 passivation interface layer and (c) C-V hysteresis as a function of Al_2O_3 deposition cycles.

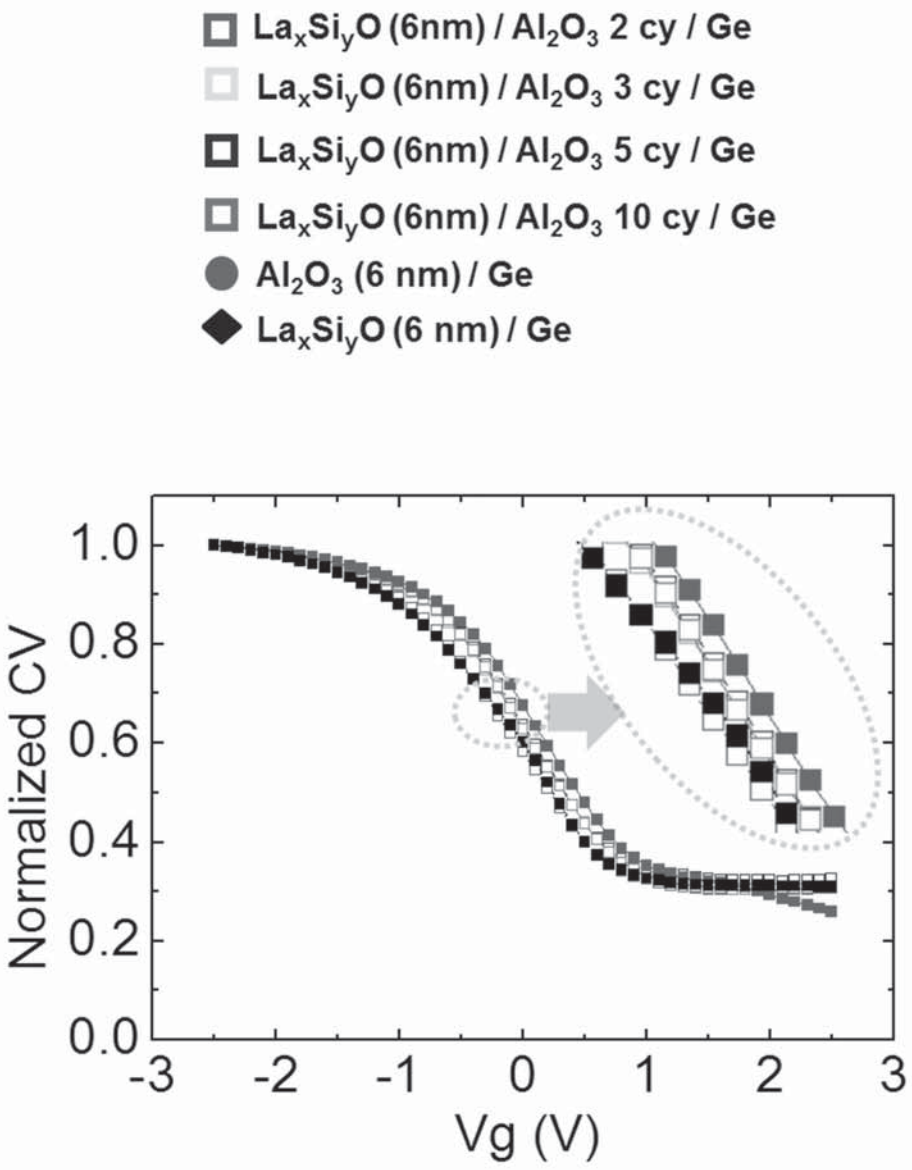
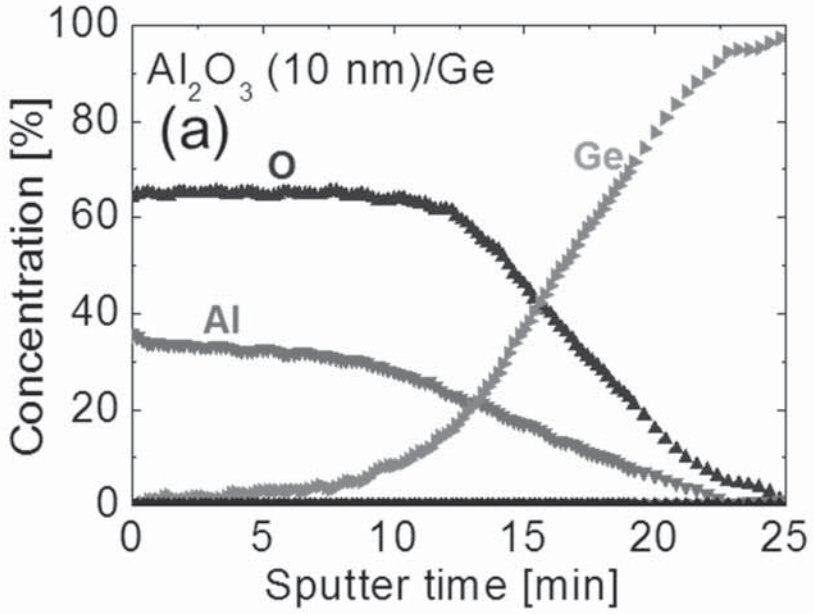
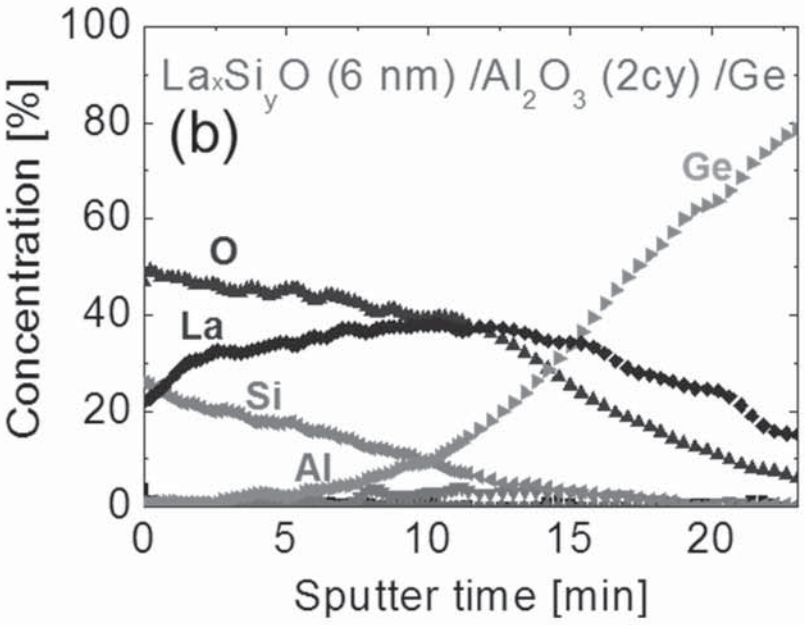


Figure 4-26. Normalized C-V curves of La-silicate film with ultra-thin Al_2O_3 passivation interface layer as a function of Al_2O_3 deposition cycles.


Al2O3 (10 nm)/Ge
(a)
O
Ge
Al
Concentration [%]
Sputter time [min]
0
20
40
60
80
100
0
5
10
15
20
25


LaxSiyO (6 nm) /Al2O3 (2cy) /Ge
(b)
Ge
O
La
Si
Al
Concentration [%]
Sputter time [min]
0
20
40
60
80
100
0
5
10
15
20

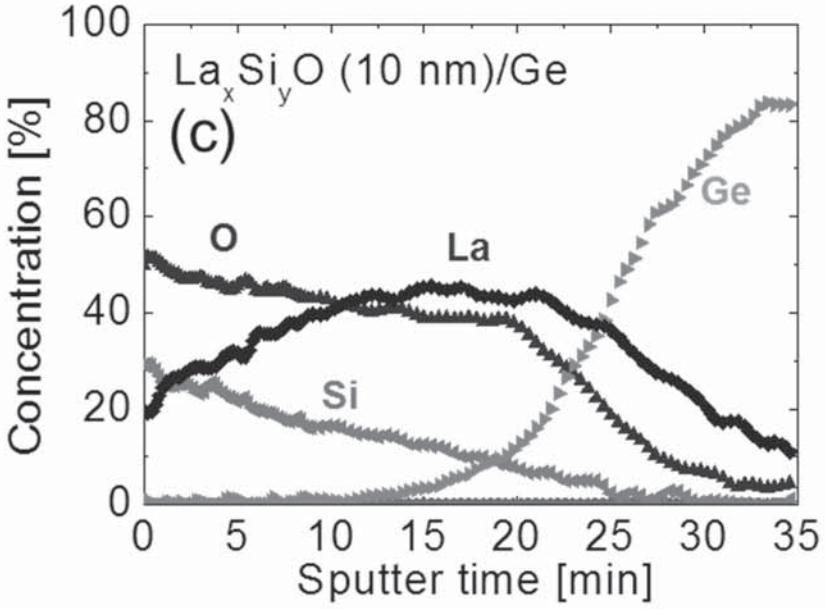


Figure 4-27. AES depth profiles of (a) Al_2O_3/ *p*-Ge, (b) La-silicate/ Al_2O_3 (2 cycles)/ *p*-Ge and (c) La-silicate/ *p*-Ge.

The chemical states of the films were further examined by the XPS shown in Fig. 4-28. An interesting finding can be made from the BE shift of the Ge 3*d* peak of the oxidized Ge. The BE shift of single La-silicate and Al_2O_3 layers was 2.91 eV and 2.63 eV, respectively, suggesting that the Ge ions in the Ge-oxide have mixed valences of Ge^{4+} and Ge^{3+}. However, when the 2 cycles of Al_2O_3 passivation layer was adopted, the BE shift was increased to 3.02 eV, meaning that the oxidation state of Ge ions in the Ge-oxide has more 4^+ state. As the cycle numbers of Al_2O_3 passivation layer increases to 10, the BE shift (2.69 eV) decreases and almost identical to that of Al_2O_3 single layer as summarized in Table 4-3. This strongly suggests that the oxidation state of Ge ions in the Ge-oxide has a strong correlation with the C-V hysteresis; the closer the oxidation state to 4^+, the smaller the C-V hysteresis.

The explicit deconvolution of Ge-oxide peak for La-silicate film with Al_2O_3 passivation layer as a function of Al_2O_3 deposition cycles is shown in Figs. 4-29. Ge dioxide concentration [GeO_2 (Ge^{4+})/ Ge sub oxide peak (sum of Ge^{1+}, Ge^{2+} and Ge^{3+})] was decreased by 46 %, 42 %, 39 % and 35 %, respectively, when Al_2O_3 deposition cycles increased to 2 - 10 cycles in Figs. 4-29 (a), (b), (c) and (d). As Ge oxide BE shift was approached to Ge bulk peak, ratio of Ge dioxide area intensity was decreased and C-V hysteresis was increased. From these facts, it is possible to assume that ultra-thin Al_2O_3 passivation layer improves Ge interface property.

Hinkle et al. and Milojevic et al. reported that the thickness of the native oxide formed on GaAs and Ge substrates decreases after Al_2O_3 deposition by the ALD method using TMA and H_2O. These papers also report that the decrease in the thickness of oxide interlayers is caused by the strong reduction effect of TMA precursor. [152, 153]

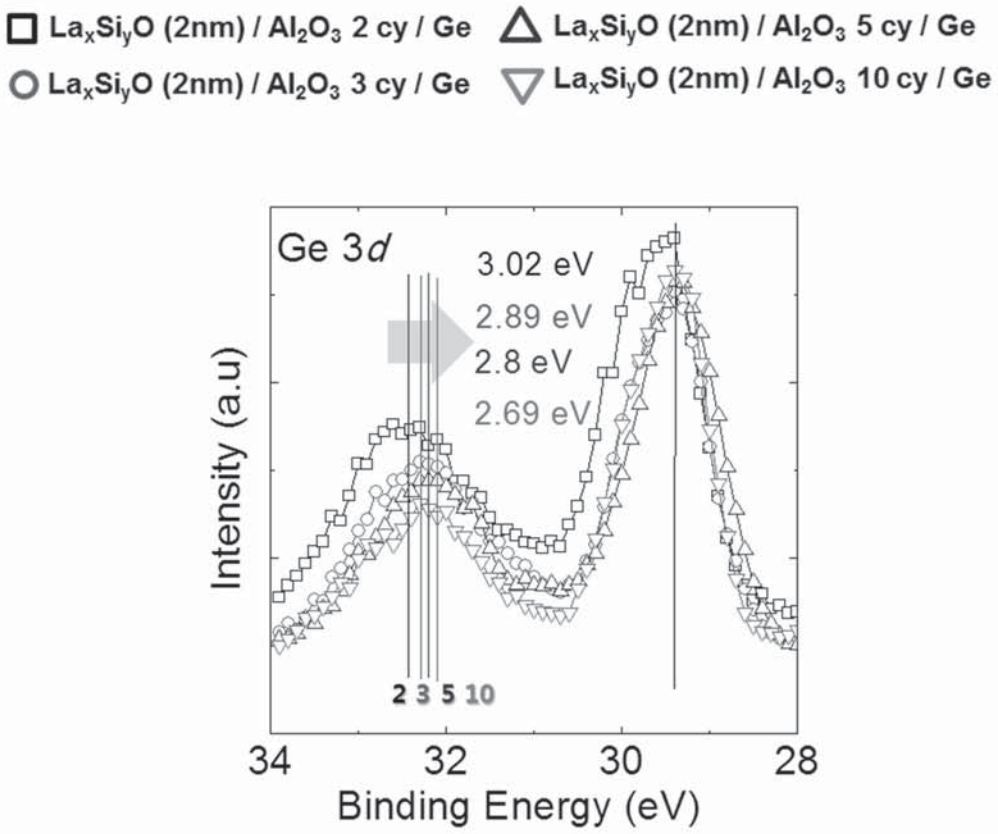
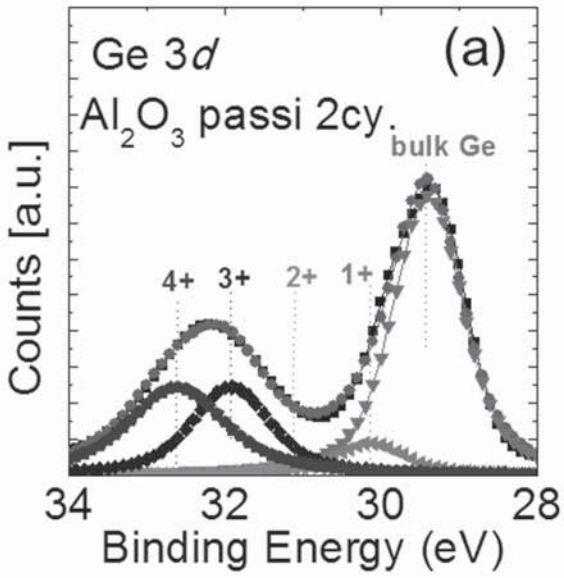
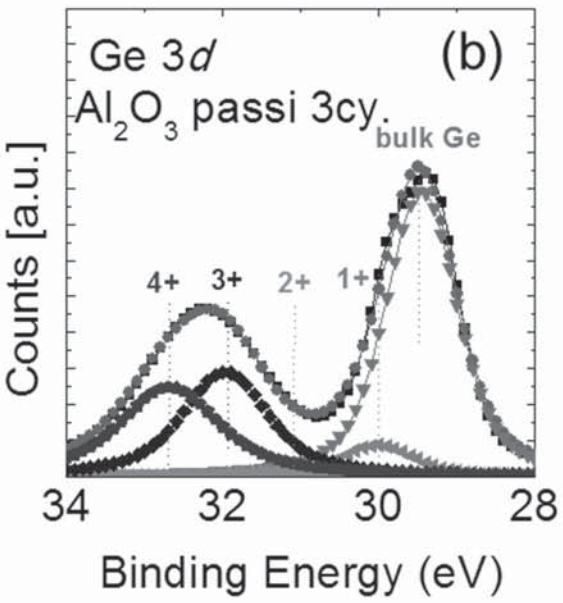


Figure 4-28. Ge 3*d* core level for the La-silicate film with various deposition cycles of ultra-thin Al_2O_3 passivation interface layer.

Table 4-3. Ge 3*d* core level for the La-silicate film with various deposition cycles of ultra-thin Al_2O_3 passivation interface layer related to Ge oxide with BE shifts from Ge bulk peak.

	Ge-O (eV)
La_xSi_yO	2.91
2 cycle	3.02
3 cycle	2.89
5 cycle	2.8
10 cycle	2.69


Ge 3d
(a)
Al2O3 passi 2cy.
bulk Ge
4+
3+
2+
1+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)


Ge 3d
(b)
Al2O3 passi 3cy.
bulk Ge
4+
3+
2+
1+
Counts [a.u.]
34
32
30
28
Binding Energy (eV)

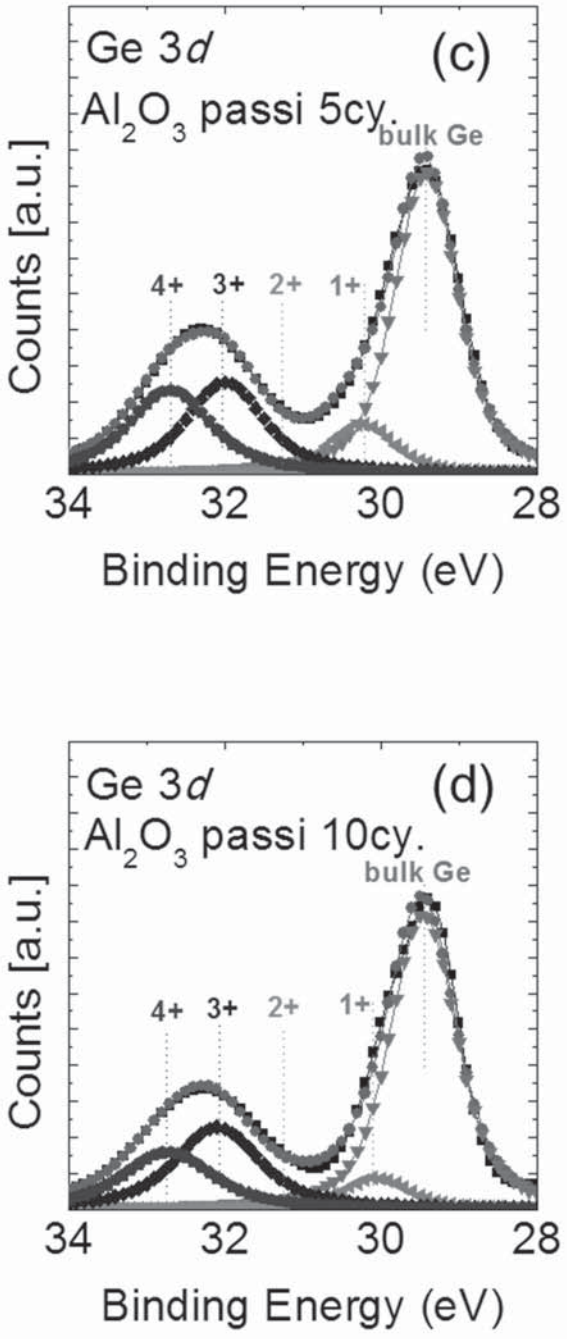


Figure 4-29. Ge 3*d* core level for the explicit deconvolution for Ge-oxide (a) La-silicate/Al_2O_3 (2 cycles)/*p*-Ge, (b) La-silicate/ Al_2O_3 (3 cycles)/ *p*-Ge,(c) La-silicate/ Al_2O_3 (5 cycles)/ *p*-Ge and (d) La-silicate/ Al_2O_3 (10 cycles)/ *p*-Ge.

For a study of the interfacial properties of La-silicate film, Al_2O_3 passivation (2 cycles) interface La-silicate film and Al_2O_3 film on Ge substrate, D_{it} was extracted by using a conductance method. Figure 4-30 shows the D_{it} of the three samples as a function of the V_g-V_{FB}. Al_2O_3 passivation La-silicate film showed smallest D_{it} among those films suggesting that the ultra-thin Al_2O_3 passivation film effectively reduced interfacial state density.

Figures 4-31 (a), (b) and (c) shows TEM images and composition analysis for interface between Al_2O_3 film, La-silicate film with Al_2O_3 passivation layer and La-silicate film on Ge. The thickness of Al_2O_3 and La-silicate film was confirmed as ~ 6 nm.

The CVS test with -2.5 V of V_g was performed for the these samples, and Fig. 4-32 shows the results; (a) Pt/La-silicate/*p*-Ge, (b) Pt/La-silicate with Al_2O_3 passivation (deposition cycle of 2) /*p*-Ge (c) Pt/Al_2O_3/*p*-Ge. While the single layer La-silicate and Al_2O_3 film shows mostly D_{it} degradation (decreasing slope) and positive charge trapping (parallel shift of C-V curve into negative direction) the 2 cycles of Al_2O_3 passivated La-silicate film showed an improved reliability characteristics; it does not show any notable change in V_{FB} whereas the D_{it} degradation was still persistent. This results indicates that Al_2O_3 film has high bulk trap density which induced the large C-V hysteresis irrespective of interface property with Ge substrate, and the C-V hysteresis was mainly govern by both interface property with Ge substrate and oxide bulk trap density. As seem in Fig. 4-27, AES profiles, La-silicate film with Al_2O_3 passivation layer suppressed GeO desorption than Al_2O_3 or La-silicate film resulted by residual Ge concentration which is identical to result from electrical property.

C-V hysteresis, XPS GeO BE shift from Ge bulk peak, D_{it} and V_{fb} shift from CVS

measurement for La-silicate and La-silicate film with Al_2O_3 (2 cycles) passivation layer summarized in Table 4-4.

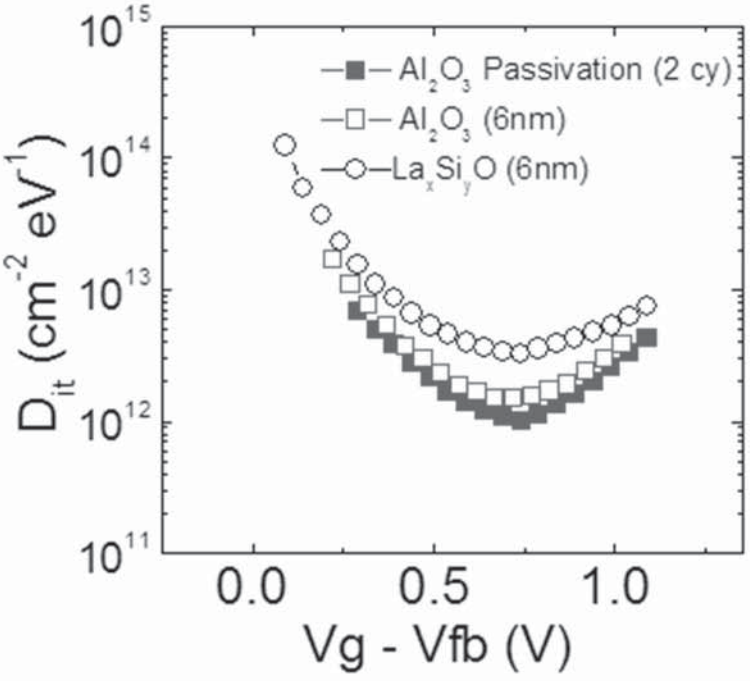
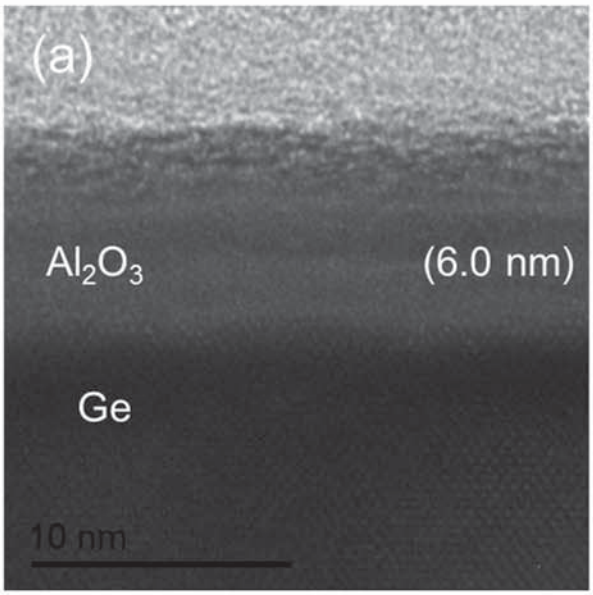
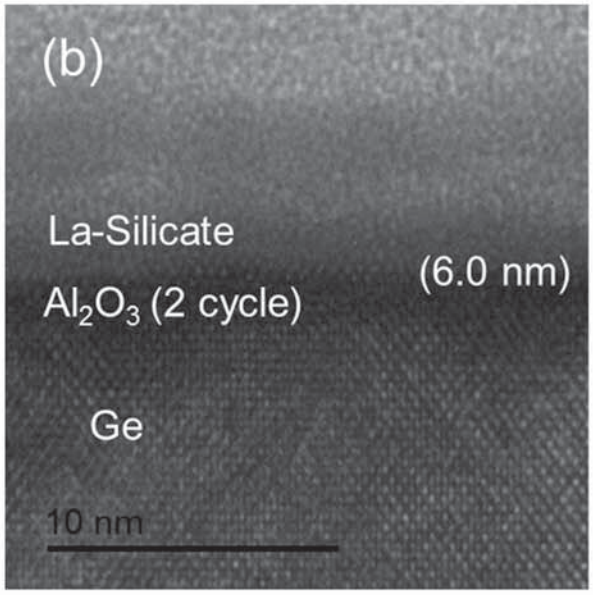


Figure 4-30. Interface state density vs. V_g-V_{fb} of Al_2O_3/Ge, La-silicate/Al_2O_3 (2 cycles)/Ge and La-silicate/Ge.


(a)
Al_2O_3
(6.0 nm)
Ge
10 nm


(b)
La-Silicate
Al_2O_3 (2 cycle)
(6.0 nm)
Ge
10 nm

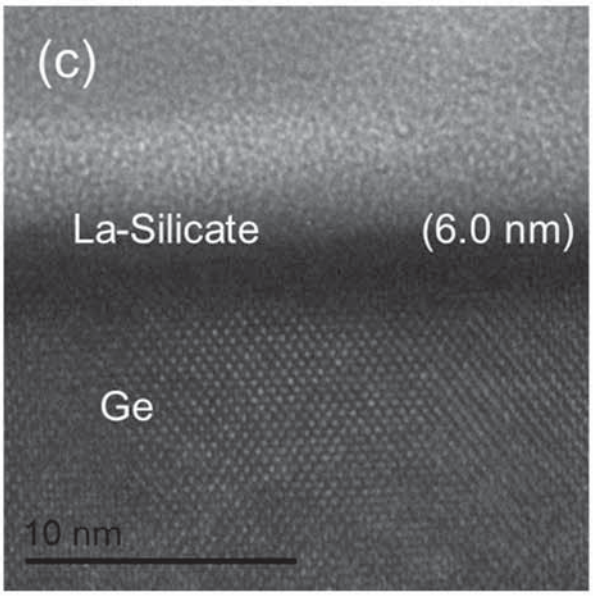


Figure 4-31. TEM images for (a) Al_2O_3/Ge, (b) La-silicate/Al_2O_3 (2 cycles)/Ge and (c) La-silicate/Ge.

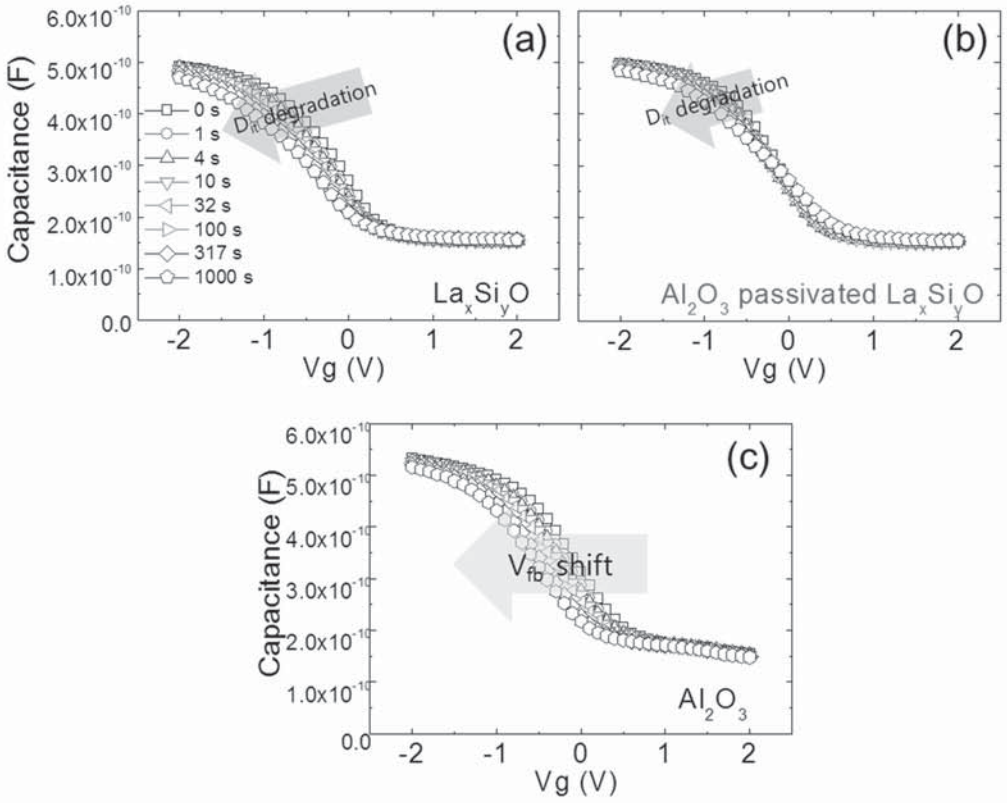


Figure 4-32. C-V curves of CVS for (a) Al_2O_3/Ge, (b) La-silicate/Al_2O_3 (2 cycles)/Ge and (c) La-silicate/Ge.

Table 4-4. C-V hysteresis, XPS GeO BE shift from Ge bulk peak, D_{it} and V_{fb} shift from CVS measurement for La-silicate/Ge and La-silicate/Al_2O_3 (2 cycles)/Ge.

	Hysteresis	XPS (GeO-Ge)	D_{it}	ΔV_{fb} (CVS@-2.5V)
La_xSi_yO	~339 mV	~2.91 eV	High	~383 mV (interface effect)
La_xSi_yO/ Al_2O_3 2cy	~238 mV	~3.02 eV	Low	~209 mV (interface effect)

4.2.6. Multi stack layer: La-silicate film with Al_2O_3 passivation and SiO_2 capping layer

The influence of SiO_2 capping layers on the electric properties of the La-silicate films with Al_2O_3 interface passivation layer was also investigated. The thicknesses of SiO_2 capping layer and La-silicate film (25% Si concentration) were fixed to ~ 2 nm, ~ 5 nm, respectively (Fig. 4-33 (a)). The SiO_2 layer was deposited using BEMAS and BDEAS Si sources to examine possible effects from the different ligands in the Si source.

Figure 4-33 (b) shows the variations in the C-V hysteresis of the three sets of samples as a function of Al_2O_3 ALD cycles; La-silicate with only Al_2O_3 passivation layer, two different types of SiO_2 capping layer with Al_2O_3 passivated La-silicate. Data for La-silicate with only Al_2O_3 passivation layer were reproduced from Fig. 4-25 (b) for the sake of comparison. The SiO_2 capping was a generally effective method in decreasing the C-V hysteresis voltage. The adoption of BEMAS Si precursor was especially effective in decreasing the C-V hysteresis and a minimum value of ~ 100 mV was observed at the optimum Al_2O_3 cycle number of 2. Among the many samples tested under this condition for the statistically meaningful data, one sample showed a hysteresis voltage as small as 50 mV. Therefore, SiO_2 capping in combination with Al_2O_3 passivation with optimum cycle number is a highly promising method to decrease the C-V hysteresis of the high-*k* gate stack film on Ge substrate shown in normalized C-V curves in Fig. 4-34.

Figure 4-35 shows AES depth profiles for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycle) interface passivation layer on Ge. Compositions of deposited films are almost identical for both SiO_2 capping multi stack layer. Though, BEMAS SiO_2

capped multi stack layer contains slightly more Ge concentrations in the deposition layer than BDEAS SiO_2 capped multi stack layer. This result might present that somehow similar to Al_2O_3 passivation effect, SiO_2 capping layer suppressed GeO formation in the film due to either GeO suppression or GeO proportionation effect.

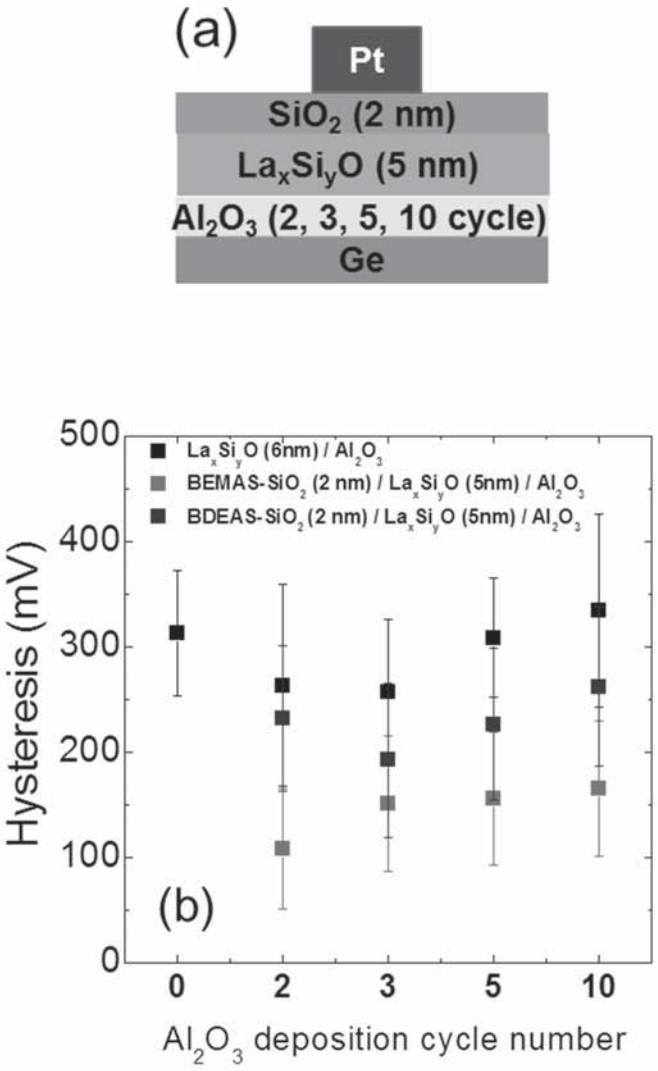


Figure 4-33. (a) Schematic diagrams of La-silicate MOSCAP with BEMAS- and BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge and (b) C-V hysteresis as a function of Al_2O_3 deposition cycles.

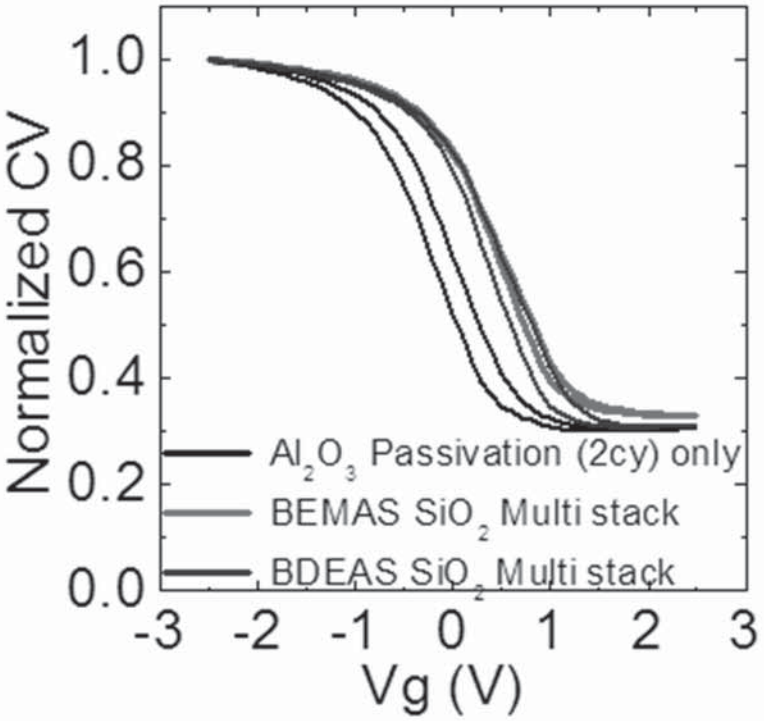


Figure 4-34. Normalized C-V curves for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge.

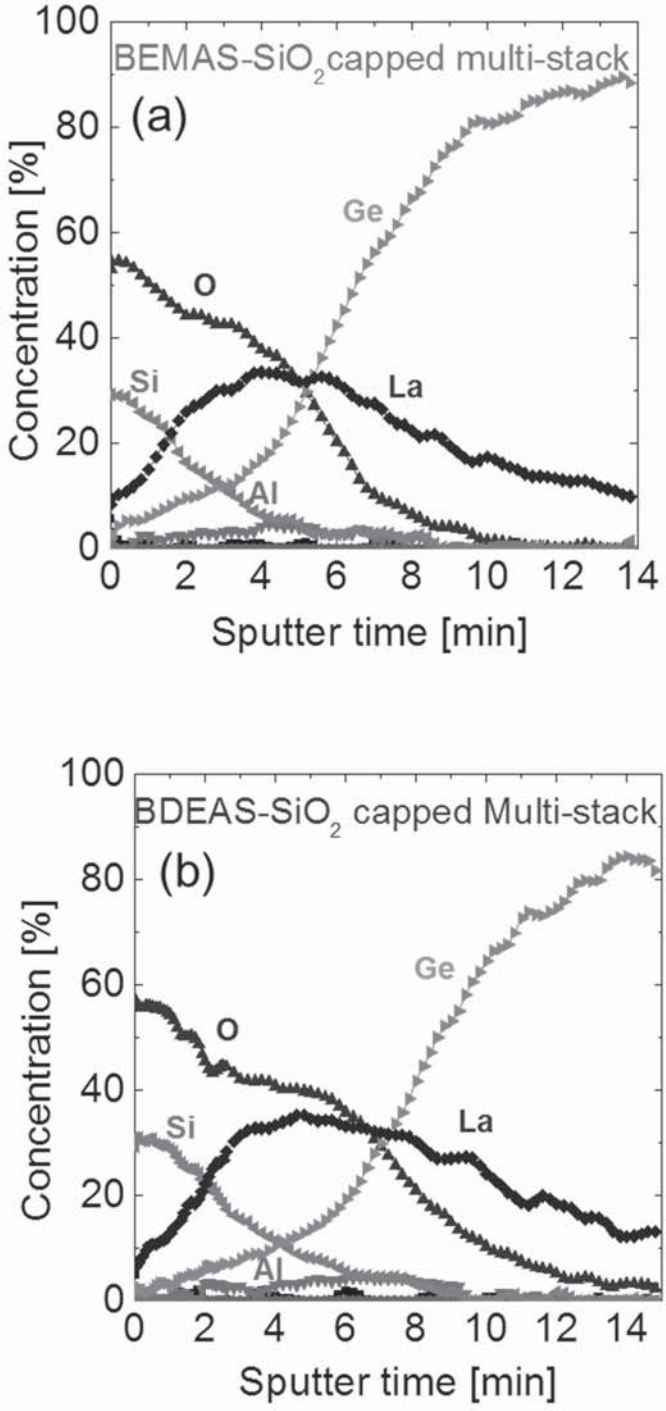


Figure 4-35. AES depth profiles for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge.

Figure 4-36 shows the D_{it} of BEMAS and BDEAS SiO_2 capping La-silicate with Al_2O_3 interface passivation film as a function of the V_g-V_{FB}. BEMAS-SiO_2 capping La-silicate with Al_2O_3 interface passivation film showed smaller D_{it} than BDEAS- SiO_2 capping La-silicate with Al_2O_3 interface passivation film. A minimum D_{it} lower than 10^{12} $cm^{-2}eV^{-1}$ could be achieved for the best condition.

Figure 4-37 shows TEM images for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge. Deposition thickness of 7 nm for both SiO_2 capped multi stack layer were confirmed.

The C-V curves for during the CVS test on Pt/BEMAS SiO_2 2nm/La-silicate 5nm/ Al_2O_3 (2 cycles)/*p*-Ge and Pt/BDEAS SiO_2 2nm/La-silicate 5nm/ Al_2O_3 (2 cycles)/*p*-Ge are shown in Figs. 4-38 (a) and (b), respectively. BEMAS SiO_2capped multi stack layer shows smaller slope changes of C-V curves suggesting that the D_{it} degradation is minimized in this sample, while that in the BDEAS SiO_2 capped sample shows a slightly severer slope change. The C-V hysteresis after the CVS test for 1000 s for the BEMAS SiO_2 capped sample was remained identical V_{fb} shift than initial position that suggesting the robustness of the sample against the electrical stress.

Figure 4-39 shows C-V curves of La-oxide film using La(^{i}PrCp)$_3$ precursor for CVS measurement. La-oxide and La-oxide with Al_2O_3 (2 cycles) passivation interface layer and (c) BEMAS-SiO_2 capped La-oxide Al_2O_3 (2 cycles) passivation interface layer. BEMAS SiO_2capped multi stack layer shows smaller slope changes of C-V curves suggesting that the D_{it} degradation is minimized in this sample, while that in the BDEAS SiO_2 capped sample shows a slightly severer slope change.

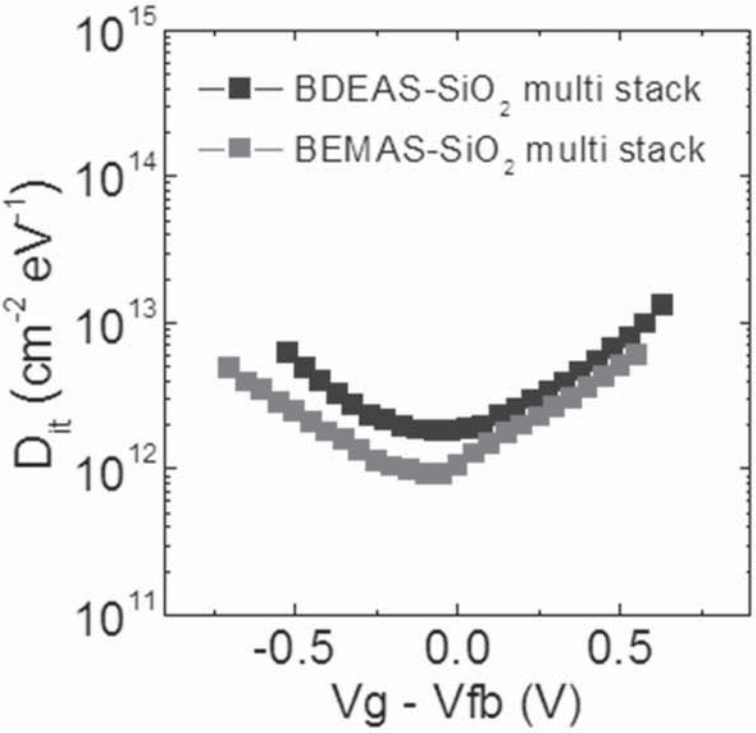


Figure 4-36. Interface state density vs. V_g-V_{fb} for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge.

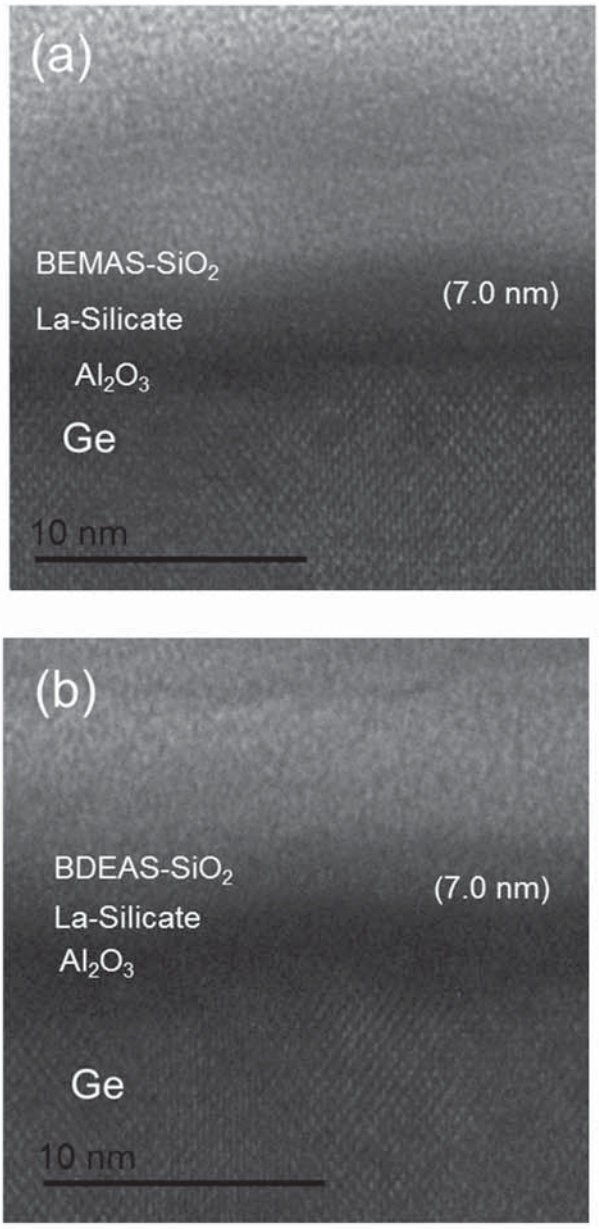


Figure 4-37. TEM images for (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge.

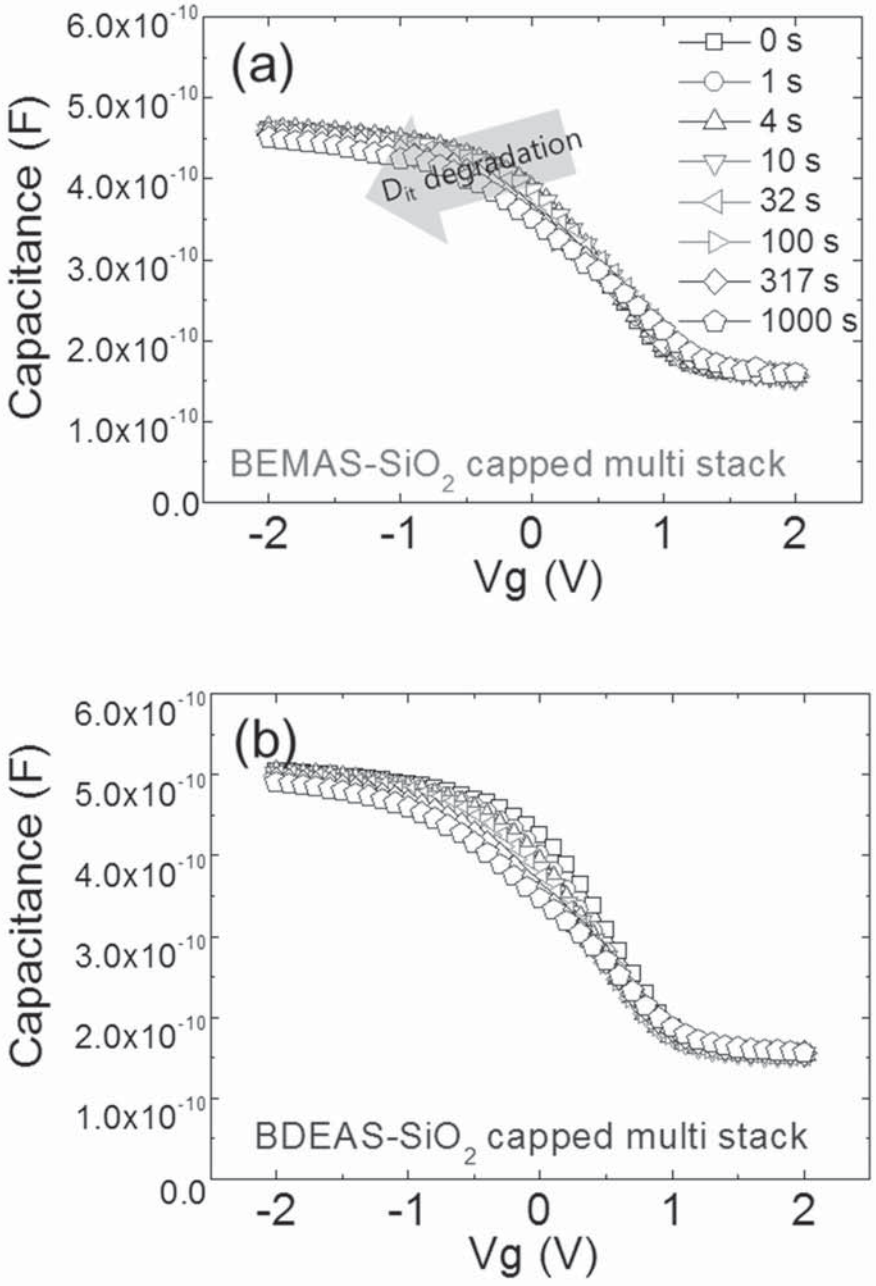


Figure 4-38. C-V curves for CVS (a) BEMAS- and (b) BDEAS SiO_2 capped La-silicate with Al_2O_3 (2 cycles) interface passivation layer on Ge.

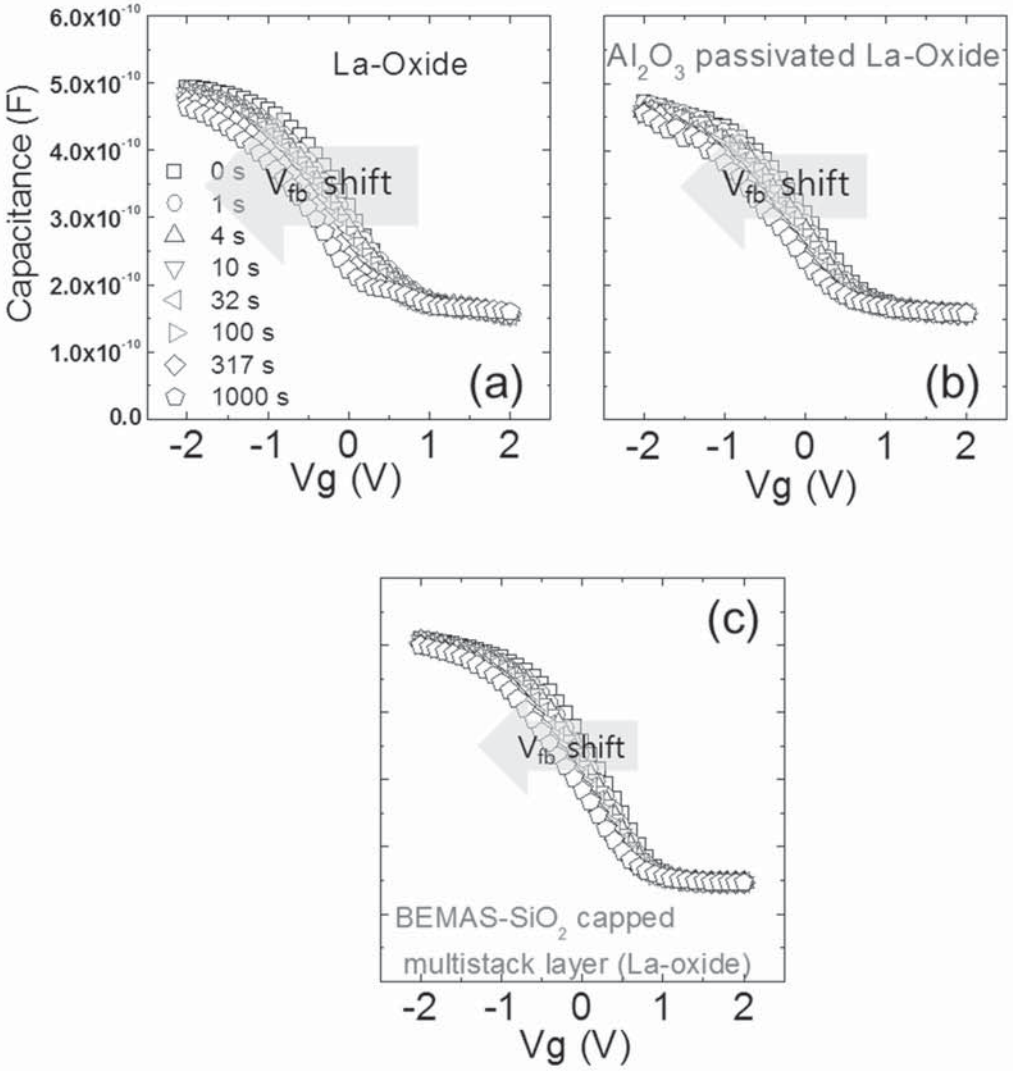


Figure 4-39. C-V curves for CVS (a) La-oxide, (b) La-oxide with Al_2O_3 (2 cycles) passivation interface layer and (c) BEMAS-SiO_2 capped La-oxide with Al_2O_3 (2 cycles) passivation interface layer.

Figure 4-40 shows a summary of J_g vs CET of the various samples discussed in this work. Because of the generally quite high physical thickness and the accompanying CET, this does not have significant importance in estimating the dielectric performance of the samples. However, it can be confirmed that the multi-stack sample having BEMAS SiO_2 capping layer showed at least very stable leakage current at a CET of 5 nm, which is not necessarily the case for Al_2O_3 or BDEAS SiO_2 capped samples.

Oh et al. reported the SiO_2 cap layer blocked the absorption of oxygen and prevented further oxidation of the Ge. [150] From these results, it is concluded that the deterioration of the C-V characteristics of the GeO_2/Ge MIS capacitors originates from the interface reaction to drive GeO volatilization. This is a reasonable conclusion since it is easily expected that GeO desorption should leave a huge amount of interface states or traps at the interface.

Table 4-5 summarized C-V hysteresis, XPS GeO BE shift from Ge bulk peak, D_{it} and V_{fb} shift from CVS measurement for BEMAS- and BDEAS SiO_2 capped La-silicate with Al_2O_3 (2 cycles) interface passivation layer on Ge.

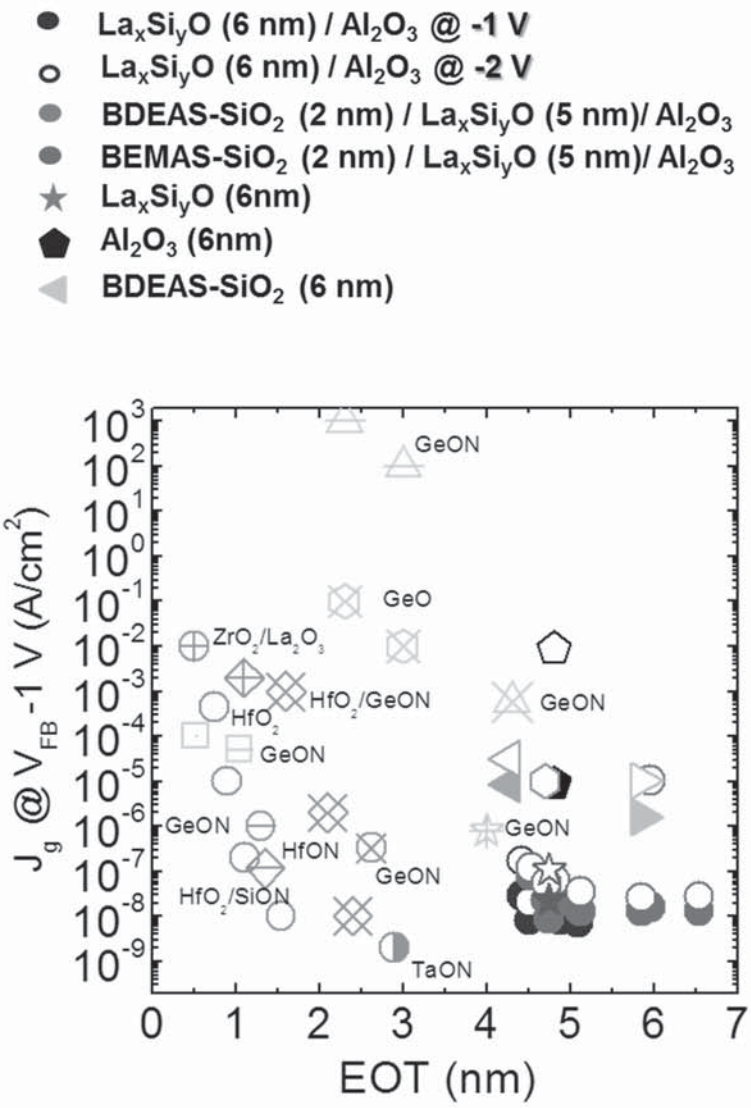


Figure 4-40. Insulating properties for various high-*k* thin films deposited by thermal ALD. [154]

Table 4-5. C-V hysteresis, XPS GeO BE shift from Ge bulk peak, D_{it} and V_{fb} shift from CVS measurement for BEMAS- and BDEAS SiO_2 capped La-silicate Al_2O_3 (2 cycles) interface passivation layer on Ge.

	Hysteresis	D_{it}	V_{fb} (CVS@-2.5V)
BEMAS cap	~118 mV	Low	~193 mV (interface effect)
BDEAS cap	~263 mV	high	~449 mV (interface effect)

5. Conclusion

For CMOS scaling beyond the 45/32 nm technology node, HfO_2 as a high-*k* material is used to replace SiO_2, because of excessive leakage current and reliability concerns. As the next generation high-*k* dielectric film as well as the threshold voltage control layer, La_2O_3 film are attracting much attention nowadays due to their high dielectric constant and large conduction band offset (CBO) with Si. Furthermore, the carrier injection velocity of Si-based channel is going to saturate, which determine the drive current in the devices and difficult to improve more by conventional scaling technology due to the relatively low carrier mobility of Si, thus many researches have been exploring other channel materials with high carrier mobility such as Ge or III-V compound substrate to replace Si substrate. Ge is a one of candidate to replace Si as the channel material of MOSFET for beyond 14 nm technology nodes due to its higher electron (twice) and hole (four times) mobilities than Si.

In summary, the chemical and electrical properties of La-silicate films on Si substrate that use $La[N(SiMe_3)_2]_3$ as precursors and two oxygen sources (H_2O and O_3) were systematically examined. The calculated bulk dielectric constants of H_2O- and O_3-La-silicate films on Si substrate were low, ~11.7 and ~8.0, respectively. From XPS analysis and AES analysis, the O_3-La-silicate film showed higher Si concentrations and lower La carbonate bonding than the H_2O-La-silicate film. This difference in the chemical composition was explained by the presence of ligands that remained on the surface and their preferential reaction with O_3 rather than H_2O. Although the O_3-La-silicate film had a lower bulk dielectric constant and thinner thickness for the same CET

compared to the H_2O-La-silicate film, it showed 3 orders of magnitude lower leakage current properties than the H_2O-La-silicate film due to its larger CBO and VBO values which originated from the higher Si concentration, and lower La-carbonate phase in the film.

Similar to SiO_2/Si in Si-MOSFETs, GeO_2/Ge has been generally regarded as the most fundamental interface in Ge-MOSFETs. Nonetheless, the lack of thermodynamic stability at the GeO_2/Ge interface hampers the development of Ge-MOSFETs. Many previous studies have demonstrated that the GeO_2/Ge interface degrades due to the GeO desorption upon thermal annealing above 400°C in vacuum or N_2 ambient owing to interfacial reaction. In atomic force microscopy and thermal desorption spectroscopy studies, it has been observed that the Ge substrate underneath the GeO_2 layer is consumed during GeO desorption. A typical example of electrical degradation by GeO desorption is the very large hysteresis in the C-V curves which is attributed to the electrically active defects near the interface.

We have investigated the effects of Si concentrations in La-silicate film on Ge substrate formed by thermal ALD on the electric property especially in reduction of C-V hysteresis. La-silicate film with Si concentration increment (~ 25 % to ~ 35 %) effectively reduced C-V hysteresis due to suppression of Ge sub-oxide generation from XPS analysis.

La-silicate film with very thin Al_2O_3 interface passivation layer obtained smaller C-V hysteresis as ~238 mV due to lower interface state density by suppression of Ge sub-oxide formation from XPS analysis.

Finally, BEMAS-SiO_2 capped La-silicate film with Al_2O_3 passivation interface layer showed smaller Ge sub-oxide formation as smaller C-V hysteresis (~less than 100 mV)

shown. La-silicate film with Al_2O_3 interface passivation layer and SiO_2 capped La-silicate film with Al_2O_3 passivation interface layer has tendency of low leakage current density. It is also found that the Al_2O_3 thickness of 1– 2 monolayer and SiO_2 capping is critical for the reduction of the interface state density.

In conclusion, the ALD-Al_2O_3 interfacial passivation layer and SiO_2 capping, whose thickness can be precisely controlled, is effective for controlling the formation of Ge oxides at high-*k*/Ge interfaces.

6. References

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국문 초록

반도체 소자의 성능을 향상시키기 위해서는 트랜지스터 크기의 수평적, 수직적인 scaling이 필요하다. 기존 실리콘 산화막의 경우, 지속적인 scaling 과정에서 누설전류가 증가하여 소자 조절 능력이 감소하는데, 이를 해결하기 위해 등가 산화막 두께를 유지하면서 물리적인 두께를 증가시킬 수 있는 고유전율 물질로 실리콘 산화막을 대체하는 연구가 오랫동안 진행되었다. 반도체 제조사로는 최초로 Intel이 45nm technology node에서 고유전율 게이트 산화막으로 HfO_2를 적용하여 반도체 양산에 성공하였다. 비록 HfO_2가 제품화에는 성공 하였지만, 신뢰성 및 유전특성 향상에는 지속적인 연구가 필요한 상황이다.

이 연구에서는 Si 기판에 원자층 증착법을 이용하여 La-silicate 박막을 증착하였으며, 이때 산화제로 사용한 O_3와 H_2O에 따른 성분분석, 유전상수 및 누설전류 특성을 비교 분석하였다. 산화제로 O_3을 이용하여 증착한 La-silicate 막의 유전상수는 ~8.0인 반면, H_2O을 이용하여 증착한 La-silicate 막의 유전상수는 ~11.7를 얻었다. 이는 이론적으로 알려진 것 보다 낮은 값이며 증착시 박막 내에 포함된 높은 Si 함량에 의한 것으로 확인되었다. O_3을 이용하여 증착한 박막의 경우 H_2O을 사용한 막 대비 더 높은 Si 함량과 낮은 La-carbonate를 형성하였으며, 이로 인해 동일한 CET에서 누설전류가 약 1/1000 이하로 감소하는 특성을 보였다.

Si 반도체 기판의 낮은 이동도는 차세대 소자에서 요구되는 특성을

확보하는데 한계로 지적되고 있다. 이러한 문제를 해결하기 위해서 고이동도 채널 물질로서 Ge 소자가 각광을 받고 있는데, 이는 Ge이 Si 대비 전자의 이동도는 2배, 정공의 이동도는 4배가 높기 때문이다. 그러나 Ge의 경우는 Si과 달리 안정적인 산화막이 존재하지 않기 때문에, Ge 기판 위에 원자층 증착법으로 산화막을 증착하는 경우는 1.5V 내외의 매우 큰 C-V hysteresis를 보이는 등 전기적 특성을 열화시키는 문제점이 있다.

이러한 문제점을 해결하기 위해 여러 종류의 passivation 박막에 관한 연구가 많이 진행되고 있다. 본 연구에서는 La-silicate 박막 증착시 별도의 Si 소스를 주입하여 25 % ~ 35% 범위에서 Si 함량을 조절하였으며, 이에 따른 C-V hysteresis 평가를 진행하였다. 이 결과 La-silicate 박막의 Si 함량이 높아짐에 따라 C-V hysteresis가 400mV 감소하는 것을 확인하였다. 이러한 개선 효과는 XPS 분석한 결과, Si 함량이 높아지면서 Ge 계면에 불안정한 Ge sub-oxide 생성이 억제된 것에서 비롯되었음이 확인되었다.

다음으로 Al_2O_3의 계면 passivation 효과를 평가하기 위해 Ge 기판에 매우 얇은 Al_2O_3 막을 증착한 후 La-silicate 막을 증착하였다. Al_2O_3를 원자층 증착법으로 2 사이클 증착한 경우 ~238mV 라는 매우 우수한 C-V hysteresis 특성을 얻었다. 수 사이클 수준의 매우 얇은 Al_2O_3 계면 passivation 막을 사용하는 경우, 낮은 interface state density 를 가지게 되는데, 이는 Ge 계면에 Ge sub-oxide 생성을 억제되었기 때문이며 이로 인해 C-V hysteresis 특성이 개선된 것임을 확인하였다.

또한 Ge 기판에 2 사이클의 Al_2O_3 계면 passivation 막과 La-silicate 막을 증착한 뒤 BEMAS 소스를 이용하여 SiO_2 막을 capping 한 경우 ~100mV 이하의 매우 우수한 C-V hysteresis 특성을 확보하였다. SiO_2 막으로 capping 한 경우 Ge sub-oxide 생성이 억제하여 C-V hysteresis 특성이 개선된 것임을 규명하였다.

1–2 monolayer 정도 Al_2O_3 passivation 막과 La-silicate 막, 그리고 SiO_2 capping 막을 증착한 경우 interface state density 를 낮게 할 수 있으며 우수한 누설전류 특성을 얻을 수 있는 것을 확인하였다.

주요어 : high-κ, ALD, La-silicate, La_2O_3, Al_2O_3, SiO_2, Si, Ge, deposition behavior, Ozone, leakage current mechanism, XPS

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