공학박사학위 논문

A Study on Structure and Electrical Properties in MILC Poly Si TFT

금속 유도 측면 결정화에 의한 저온 다결정 실리콘 박막 트랜지스터의 구조 및 전기적 특성에 관한 연구

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Abstract

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LCD companies are turning to AMOLED where low temperature polycrystalline silicon (LTPS) TFT substrates are usually used as back planes. This is mainly because TFT back planes need high mobility and high reliability, since OLED displays require high brightness and long life time. But conventional LTPS back plane has a top gate structure and some difficulties in manufacturing for a large glass substrate. One of the reasons of

this difficulties is the process complexity of LTPS, and the other is that the development of such manufacturing apparatus as eximer laser annealing(ELA) equipment or ion implantation equipment that also faces difficulties for large substrate application. Conventional amorphous silicon TFT has a bottom gate structure that is more easily manufactured for larger glass substrate. However, the performance of the electrical properties, especially the reliability, is insufficient for OLED displays. In order to obtain uniform TFT characteristics and methods have been proposed. Among several crystallization methods, solid phase crystallization (SPC) of amorphous silicon (a-Si) has some advantages of low-cost and good uniformity compared to ELC poly-Si. Recently, a high-quality poly Si related with Ni-mediated crystallization has been demonstrated such as metal induced lateral crystallization (MILC), continuous grain silicon (CGS). Due to this reason, Poly Si bottom gate TFT by non laser crystallization method must be necessary in LCD line. LCD Company can fabricate AMOLED panel by adding annealing process. Bottom gate TFT can be made by in-situ deposition. In this paper, we studied on process optimization of bottom gate P-channel poly Si TFT applicable to LCD line.

Also the external stress effects were investigated. This thesis is organized with flowing 2 parts.

Part. 1 Process optimization in Poly-Si TFT

(Chapter3, 4, 5, 6)

Part. 2 External stress effects on Poly-Si TFT

(Chapter7, 8)

In part 1, Process optimization is discussed. Process optimization includes channel thickness, gate insulator thickness, overlap distance between S/D and gate, and Channel doping. In the bottom gate structure, channel thickness was changed from 100Å to 900 Å. In 400~600 Å channel thickness, electrical performance is better than other thickness. The thinner channel, the lower mobility. In gate insulator, 1000Å is adequate for TFT. The more in gate insulator thickness, the worse in slope and on currents due to reduction capacitance. In overlap effects, Overlap in source and offset in drain region is desirable structure for electrical performance. Overlap in drain region has effects on the leakage currents due to lateral field between

S/D and gate. And vertical field effects were investigated changing each layer. Layers between S/D and gate have effects in vertical field. Channel doping wad done in top gate poly Si TFT. Various lightly doping methods were tried. In N-TFT, the reduction in the leakage currents was confirmed using PECVD doping. Also, the improvement in slope was done changing structure in Mosfet. Channel path effects slope and I_{on} in the electrical performance. If the structure is applicable to Poly –Si TFT, it is expected to be steep slope.

In part 2, External stress effects on Poly-Si TFT are discussed. External stress means mechanical stress and thermal stress. In mechanical stress, glass substrate was stretched to apply tensile stress. In thermal stress, different substrate was used. During annealing, bare glass is shrinkaged. This stress has compressive stress properties. In this point, external stress effects on poly-Si TFT were investigated. In tensile stress, main changes are mobility and off currents. And aspect in P-type and N-type TFT, phenomenon is different. Regardless of direction in tensile stress, mobility increase in P-TFT. But in N-TFT, mobility increase in parallel direction to channel. In vertical direction, Mobility decrease. The case in N-type is explained from Mosfet

theory. Contrary to tensile stress, Mobility in thermal stress is reduced. During MILC and activation annealing, bare glass is schrinkaged. At this time, Nitride has cracks. In bare glass, TFT doesn't have operation for switching. Thermal stress induce crack in gate insulator. So it is important to do compaction process in LTPS (>500ºC).

Keyword: metal-induced lateral crystallization (MILC), polycrystalline silicon (poly-Si), thin film transistor (TFT), Overlap, Offset, Bottom gate TFT, tensile stress, compressive stress, compaction, mobility, leakage currents, slope

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Contents

List of Figures

Chapter 1

Chapter 2

Chapter 6

Chapter 7

List of Tables

Chapter 1

Introduction

1.1 Application of Thin Film Transistor

Recently display industry became one of key industries in most of developed countries. The cathode ray tubes (CRTs) still remain the information display terminal for television and computers. However, the CRTs are gradually being replaced by the emerging technology of flat-panel displays (FPDs). The advantages of FPDs are obvious, especially for portable applications such as laptop computers, medical imaging X-ray sensors and avionic displays. The main reason for FPDs' not having taken over the CRTs market is that they cost more than CRTs, but the gap has been closing every year and the FPD market has been similar to the CRT market.

Among various FPDs, the dominant product on the market is liquid crystal displays (LCDs). The LCD consists of an array of liquid crystal pixel and each pixel has LC material sandwiched between two electrodes that are covered with polarizers staggered by 90°. The LC molecular orientation can be controlled by the electric field that is applied between the two electrodes and it

changes the polarization state of the light that enters the LC cell through one of the two polarizers. Therefore, depending upon the "twist" imposed on the polarization of the incoming light, it will either be allowed to pass through or be blocked by the polarizer at the opposite side of the cell. [1]

There are two types of LCDs : passive matrix (PM) and active matrix (AM) ; the advantages of the former lay in its low cost, however, PM is typically restricted to small display size due to issues with image quality (i.e., contrast ratio and crosstalk) that arise as the size and resolution of the display increase, while AM enables high resolution displays. AM addressing uses independent electronic switches to individually control the state of each pixel. In this manner, the display performance is decoupled from the shortcomings of PM and becomes a function of the type and performance of the pixel electronic switch.

For active-matrix LCDs, silicon (amorphous or poly-crystalline) thin-film transistors (TFTs) serve as the key pixel electrode-switching element. Hydrogenated amorphous silicon is well suited for AMLCDs, until now, because it can easily be deposited over large areas at low temperatures that are fully compatible with glass. In addition, it has a high dark resistivity, leading to TFTs with low leakage currents. Finally a-Si:H technology has become the dominant player in the active matrix display. [2, 3]

1.2 Low Temperature Polycrystalline Silicon

Poly-Si presents advantages over a-Si technology on the achievable size-versus-resolution limits for the display, as well as the opportunity to monolithically integrate additional functionality on the panel. The advantages of poly-Si are the significant performance gains of poly-Si TFTs over a-Si TFTs and its compatibility with CMOS fabrication. CMOS technology enables monolithic integration of peripheral drivers on panel, as well as opportunities for the addition of other value-added components on the display. [4, 5]

In addition, many researches are concentrated on the active-matrix Organic Light Emitting Display (OLED) [6, 7] because of its low cost, low power consumption, wide viewing angle, and the possibility to be made on flexible substrates. For the pixel element of OLED, poly-Si TFTs are better than a-Si:H TFTs, because OLED is current-driving type and needs more current, while LCD is voltage-driving type.

Unlike MOSFET devices, the TFT active layer needs to be formed on such amorphous host material and that the temperature of all associated processing has to be constrained within the allowable rage prescribed by the materials characteristics of the substrate. For current display-glass substrates, the

maximum processing temperature needs to be kept below ~650℃. To form poly-Si TFTs on the commercial glass substrates, a number of researches have been carried on some methods.

Poly-Si thin films can directly be deposited on glass over 600℃ by PECVD but their electrical properties are inadequate for TFTs. [8] Therefore most of research groups have focused on the methods to crystallize a-Si thin films below 650℃. The most direct method of obtaining poly-Si films from a-Si films is via solid-phase crystallization (SPC). However, it needs for SPC long time annealing during over 20hrs at 600℃ and quality of poly-Si is not enough to make high performance TFTs. [9]

Excimer Laser Crystallization (ELC) uses excimer laser as a type of gas laser from an inert atom and halide atom. a-Si films are melted by laser irradiation during very short period, ~220 ns, and they are crystallized simultaneously with the solidification. [10] This method is also allowable to flexible substrate and can make high mobility poly-Si TFTs, but there are some problems on the productivity, surface roughness, non-uniformity of poly-Si.

Recently, many researches are concentrated on the MILC (metal induced lateral crystallization) and MIC (metal induced crystallization). They will be commented at following chapter.

1.3 Metal-Induced Lateral Crystallization

The crystallization temperature of a-Si can be lowered by the addition of some metals into a-Si and it is called as metal-induced crystallization (MIC). Metal induced crystallization (MIC) is induced by some metals such as Au, [11] Al, [12] Sb, [13] and In, [14] which form eutectics with Si, or metals such as Pd, Ti, and Ni, [15, 16] which form silicides with Si. These metals have been added to a-Si to enhance the nucleation rate. Some of these cases were reported to be successful in lowering the crystallization temperature down to 500℃. The MIC process, however, has a serious drawback of undesirable incorporation of metal impurities into Si, so that it has not been applicable to the fabrication of TFTs. For example, the crystallization temperature of Al-Si is reported to be as low as 170℃, but Al is an acceptor-type dopant within Si. [17]

Hence, it is of great significance to minimize the amount of metal incorporation into Si while a lower crystallization temperature is preferable. Liu and Fonash first showed that MIC can be applied to the fabrication of poly-Si TFTs, where they tried to minimize the metal contamination by depositing an ultra-thin Pd layer under a-Si films. Though they were able to reduce the crystallization annealing time, the crystallization temperature was still kept at

600℃.

More recently, a different crystallization phenomenon has been reported, where MIC could be extended laterally into the metal-free areas over 100 ㎛ and this metal-induced lateral crystallization (MILC) has been known to take place for Pd, Ni, at temperatures lower than 500℃. [18, 19] MILC can provide large-grained poly-Si films as well as low-temperature crystallization. Figure 1-1 briefly shows the MILC process. Also figure 1-2 indicates the microstructures of Pd-induced lateral crystallization and Ni-induced lateral crystallization respectively. A-Si region contact with metal layer is crystallized by MIC and poly-Si grains grow laterally toward a-Si region where doesn't contact with metal layer. Thus MILC poly-Si region has lower metal contamination than MIC region. [20-22]

According to MILC reaction model [23], MILC phenomenon is caused by strain-stress among a-Si, metal-silicide, and c-Si layers. At the tip of the lateral crystallization, there is a silicide of less than 50 Å in thickness, which moves into the amorphous silicon leaving the poly-Si behind, as shown in figure 1-2. In case of Pd-MILC, it is considered that Pd2Si phase is generated and induces crystallization of a-Si by TEM analysis.[24] The schematic drawing for this reaction is illustrated in figure 1-3. For the catalytic phase transformation to

occur, three different atomic fluxes are required in the system. Firstly, the bond breaking of a-Si atoms and migration of each atom towards the interface between a-Si and the silicide designated as /1/ in figure 1-3 (F1). The migrated Si atoms are to be adsorbed at the silicide surface to create the metal vacancies. Secondly, the hopping of the above-mentioned created metal vacancies inside the silicide to reach the interface between the silicide and poly-Si designated as /2/ (F2). Hopping of the metal vacancies should be coupled with the metal ions in the silicide. Finally, the dissociated Si atoms at /2/ are rearranged and attached to the dangling bonds of the poly crystal (F3). Phase transformation of one atomic layer can be completed by the rearrangement of dissociated Si atoms at /2/. In a steady state, F1 should be equal to F2 and F3.

Since there is a volume expansion at /1/ and shrinkage at /2/, corresponding tensile and compressive stresses would be created. In case of a single crystal, the atomic densities of Pd and Si are 6.82×10^{22} /cm^3 and 4.99×10^{22} /cm^3, respectively, and those of Pd and Si in Pd_2Si are 4.72×10^{22} /cm^3 and 2.36×10^{22} /cm^3, respectively. Considering this, it can be readily calculated that Pd of 1 Å^3 reacts with Si of 0.68 Å^3 to form Pd_2Si of 1.44 Å^3. Hence, as shown in Fig. 1.4, the volume is calculated to expand by two times at /2/ and to contract in half at /1/. This strain induces the tensile stress and the stress is about 43GPa.[25] The

tensile stress drives the bond breaking of a-Si and the migration of Si atoms for adsorption at the silicide surface of /1/, while compressive stress built at /2/ would facilitate the atomic rearrangement. [26]

Vacancy motion inside the silicide, which has to be coupled with the metal ions in the reverse direction, can be driven by the thermodynamic equilibrium potential difference between /1/ and /2/. It is known that a-Si can accommodate more metal elements than poly-Si, thermodynamically, so that the charged metal ions have to move toward /1/. [19]

The kinetics of the hopping reaction may change, however, with the presence of an externally applied energy, such as an electric or magnetic field. Flux F3 is expected to occur spontaneously, even though it can be promoted by the compressive stress at /2/. A determination of the rate-controlling step has never been experimented, however, F1 is thought to be the one even though F2 is the most sensitive step upon the external conditions such as an applied stress etc.

Also, MILC reaction model will be analyzed in detail.

A. Silicide formation

When a thick Ni film (> 100 Å) is deposited on a c-Si substrate and annealed, orthorhombic Ni_2Si with the $PbCl_2$ structure is formed by a diffusion

controlled process at temperatures as low as ~ 200 ℃. Annealing at temperatures in the range 350-750 ℃ leads to a diffusion-controlled transformation of Ni_2Si into the monosilicide, NiSi, which is also orthorhombic with the MnP structure. [27] Nickel has been found to be the dominant diffusing species in the formation of Ni_2Si [28, 29] and NiSi. [30, 31] The transport of Si through NiSi has also been studied, although rather poor epitaxial layers of c-Si were observed. [32] At temperatures in the range 450-750 ℃, the NiSi transforms into the thermodynamically favored end phase, $NiSi_2$. [33, 34] The high transformation temperature has been attributed to nucleation-controlled kinetics, and Ni has again been observed to be the fast diffusing species. [35] The disilicide $NiSi_2$ is cubic with the CaF structure and has a very close lattice parameter match to c-Si (-0.4%). Therefore, $NiSi_2$ coherently confirmed on the c-Si layer.

Similar to Ni, Pd forms Pd_2Si phase at low temperature, around 500 ^oC. Pd_2Si has hexagonal structure and it's a and c is 13.055 and 27. 49Å, respectively. And its unit cell is very huge which contains 288 atoms. [36,37] (0001) of Pd2Si can be epitaxy with (111) of c-Si and they show only 1.9 % of lattice mismatch.

B. Nucleation of c-Si

The phase transformation of a-Si to c-Si is mediated by $NiSi_2$ precipitates. Crystalline Si nucleates on one or more of the eight {111} faces of the octahedral $NiSi_2$. $NiSi_2$ is metallic with a very low resistivity of 35 μΩcm and an extremely good lattice match with c-Si. The phenomenon of metal-induced crystallization is thought to be due to an interaction of the free electrons of the metal with the covalent Si bonds at a growing interface. [38] The small misfit (0.4%) between $NiSi_2$ and Si facilitates the formation of epitaxial c-Si on the {111} faces of the $NiSi_2$ precipitates. Localized networks of c-Si trails were often single crystal, despite the observation of $NiSi_2$ precipitates at the leading edge of each trail. Migration of $NiSi_2$ led to epitaxial growth of Si constrained to <111> directions. Impingement of migrating silicide precipitates with stationary precipitates promoted further epitaxial growth on variants of the (111) direction.

C. Growth of MILC epitaxial c-Si

Following nucleation of c-Si on the $NiSi_2$ precipitates, growth always proceeded with a $NiSi_2$ precipitate at the planar advancing growth front. Many

reports confirmed that the growth rate for each individual needle was dependent upon the $NiSi_2$ thickness in the growth direction. Many $NiSi_2$ fanned out, decreased in thickness, and were observed to migrate more rapidly. In general, the trails of c-Si developed a needlelike morphology because lateral growth of the a-Si/c-Si interface via conventional solid phase epitaxial growth occurred much more slowly. The c-Si needles were frequently seen to fan out, with a consequent reduction in the $NiSi_2$ thickness. At the same time, the growth velocity increased with decreasing $NiSi_2$ thickness.

The driving force for the phase transformation is the reduction in free energy associated with the transformation of meta-stable a-Si to stable c-Si. [39] Figure 1-5 shows the schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with a-Si and c-Si. The chemical potential of the Ni atoms is lower at the Nisi/a-Si interface, whereas the chemical potential of the Si atoms is lower at the $NiSi_2$/c-Si interface. For a migrating $NiSi_2$ precipitate consuming a-Si at the leading interface and forming a trail of epitaxial c-Si, there is a driving force for the forward diffusion of Ni atoms through the $NiSi_2$ and a driving force for the diffusion of Si atoms in the reverse direction through the NiS_2.

1.4 MILC poly-Si TFTs

MILC has many advantages such as large grains without defects [24], low temperature processes, smooth surface, high crystalline uniformity and low process cost, etc. Thus, MILC poly-Si TFTs were fabricated by some groups and they showed excellent properties. [19, 22, 24, 40] Their performance is better than that by SPC. [19]

However, it has been reported that the leakage current of poly-Si TFTs using MILC is higher than those of poly-Si TFTs prepared by laser annealing process. [41] The MILC method uses metals, such as Ni and Pd. [42, 43] The crystallization occurs through lateral phase transformation from the MIC region and this lateral crystallization is mediated by silicides which are formed in the MIC regions. In general, needle-shaped crystal Si grains grow toward the a-Si region with the migration of the silicide [44] and the individual crystallites form crystallized networks during MILC process.

Ni-MILC process enables crystallization of a-Si thin films with less micro defects, such as Ni silicides and micro twins, and therefore, most studies have focused on Ni MILC due to the good electrical properties of Ni-MILC TFTs. However, the relatively high leakage current and low field-effect mobility are

regarded as problems for employing this technology and much research related to overcome the problems in MILC TFTs has been undertaken. It has been known that the main reason of referred problems is MILC/MILC boundaries (MMBs), which are defined in the center of channel region.[45] For conventional Ni-MILC TFTs, MMBs are formed inevitably since Ni-MILC progresses from the both sides.

The MMB contains many defects, such as micro twins and metal silicide, which acts as trap sites for high leakage current. These defects seemingly work as a scattering source that considerably reduces field-effect mobility.[46] For this reason, many researchers have been reported that the TFTs which were fabricated using unidirectional Ni-MILC would make better electrical performance than that by bidirectional MILC [46,47] However, such unidirectional Ni-MILC inevitably requires long annealing time since the length of MILC should be doubled. It took more than 20 h to crystallize the channel area at 500 ^{o}C in previous work.[47] To overcome this problem, the higher MILC rate is required.

1.5. Development of MILC Technology

MILC phenomenon was discovered in 1992. In 1995, MILC technology was applied for fabrication of TFT and experimental results was published in IEEE. In 2000, Neo-Poly Inc was founded for fabrication of Poly-Si TFT by MILC. From 1996 to 2013, the characteristics were improved for modification of structure and process. Development in MILC is summarized in Table1-1

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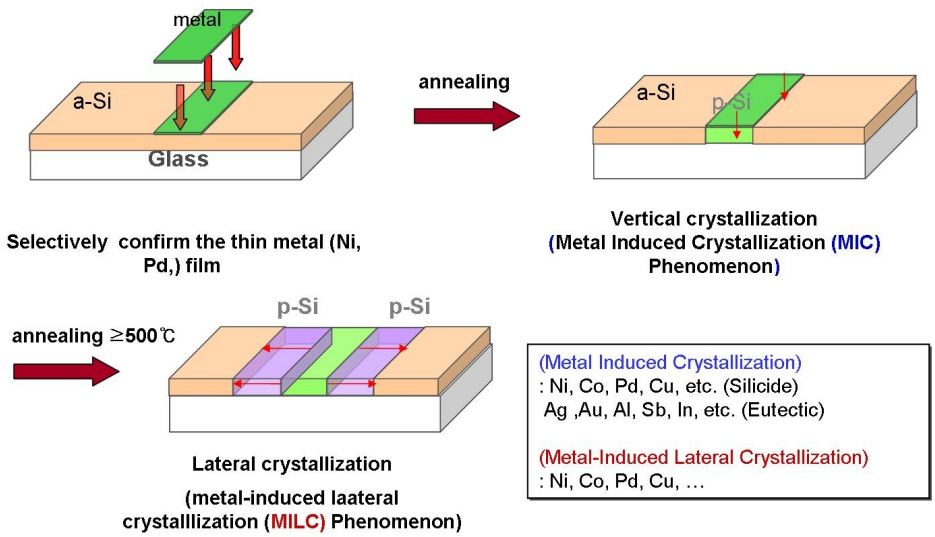

Fig 1-1. The metal-induced lateral crystallization (MILC) process flows.

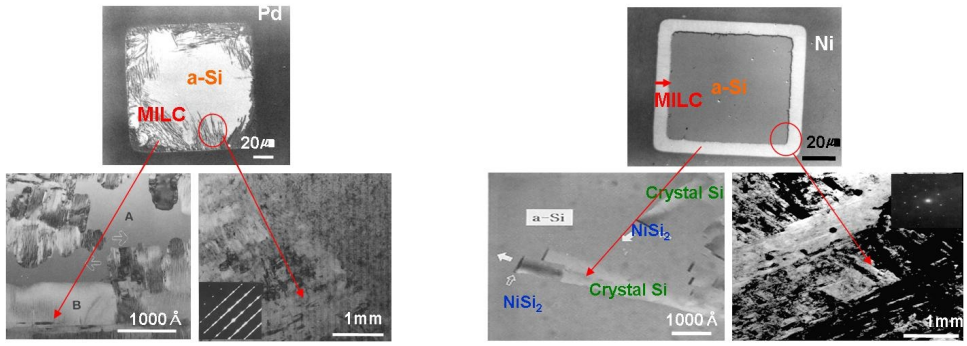

Fig 1-2. The microstructure of (a) Pd-induced lateral crystallization (b) Ni-induced lateral crystallization

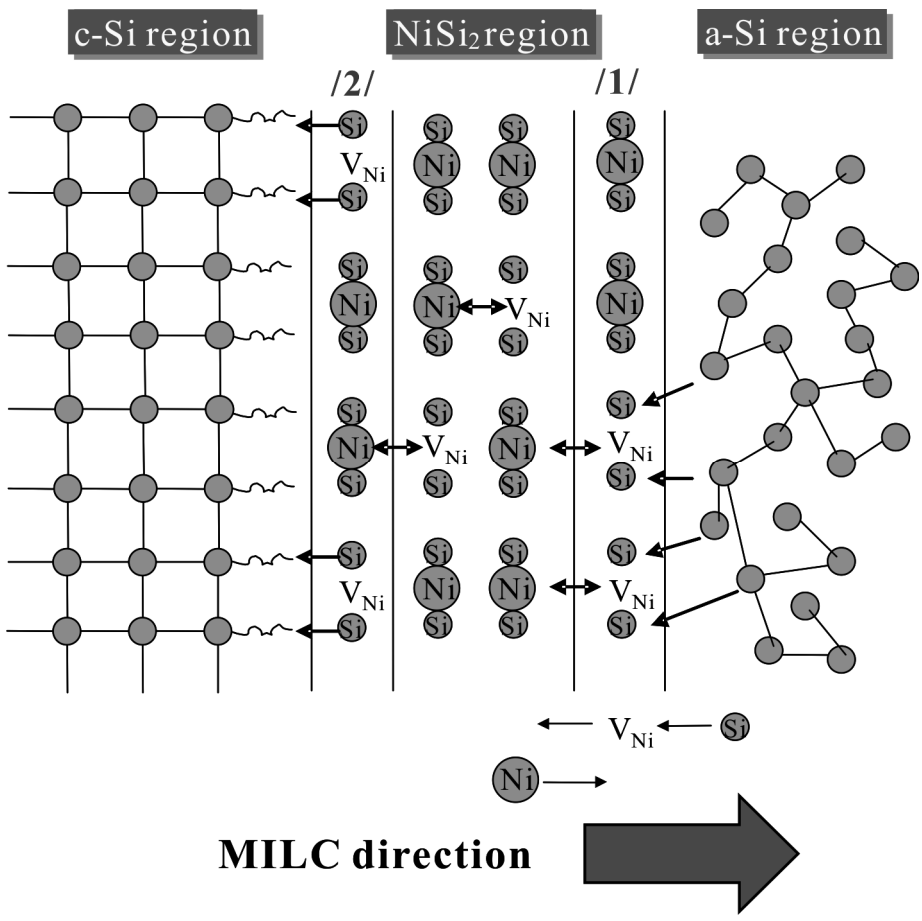

Fig 1-3. Schematic illustrations of the MILC reaction model.

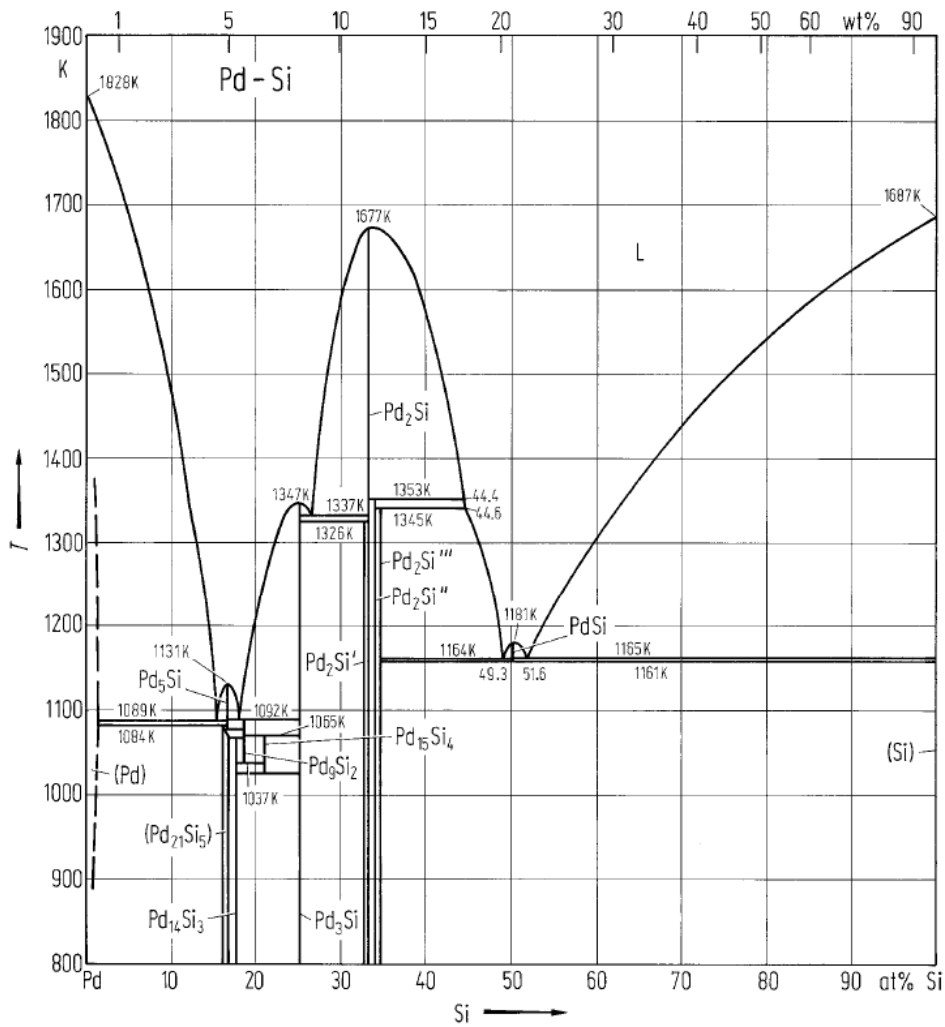

Fig 1-4. Pd-Si phase diagram.

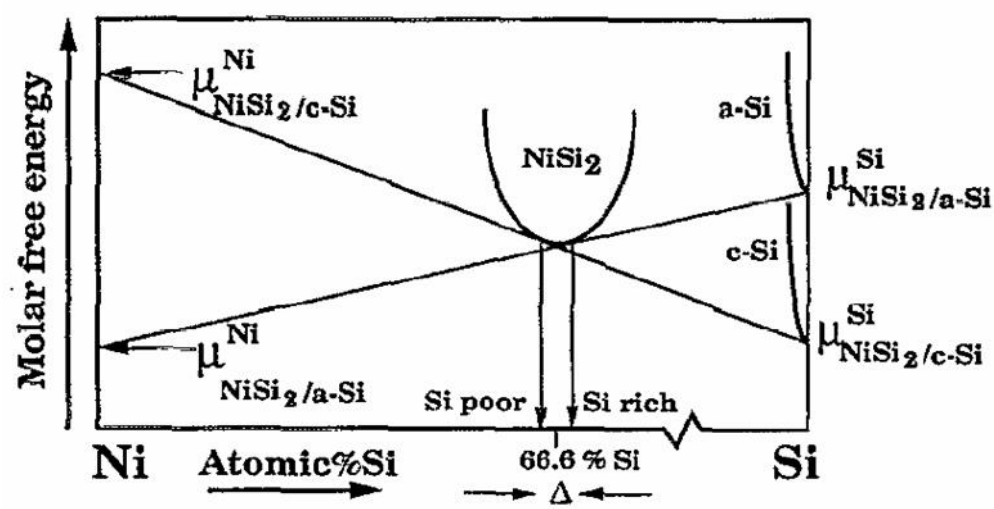

Fig 1-5. Schematic equilibrium molar free-energy diagram for $NiSi_2$ in contact with a-Si and c-Si.

Development in MILC	Reference
Low temperature dopant activation	[48]
Self-align	[49]
Electrical Stress effect	[50]
Offset structure in MILC	[51]
Different annealing method	[52]
Scanning Rapid thermal annealing	[53]
MILC by Ni-Co alloy	[54]
Effect of Pd Addition on NILC	[55]
Crystal Filter	[56]
Bottom gate TFT by MILC	[57]
Gettering	[58]
Copper MILC	[59]
SIC	[60]
Mabon	[61]
LDD	[62]
SILC	[63]
Channel Splitting	[64]
Asymmetry	[65]

Table1-1.Development in MILC Technology

Chapter 2

Experimental

2.1 Sample preparation for MILC observation

A 600 Å thick amorphous silicon (a-Si) thin film was deposited on the buffer SiO_2/glass substrates by low pressure chemical vapor deposition (LPCVD) with SiH_4 at 520 ℃. Corning 1737 glass, which is widely used for TFT-LCD industry, was used for substrate. The buffer layer was deposited by plasma enhanced chemical vapor deposition (PECVD) with SiH_4, Ar, and N_2O gas, and its thickness was 3000 Å. Thickness of a-Si was 600 Å.

To prevent the metal contamination at a-Si region which will be MILC photo resistor (PR) was patterned and native oxide was eliminated with buffered-HF solution. Then, a Ni film of 100 Å thickness was deposited by direct-current magnetron sputtering system at room temperature and PR was removed with PRS-2000 remover at 70 ℃. Thin metal layer on the PR was also eliminated simultaneously during PR strip. It was called as lift-off method. Samples were annealed at 570 ℃ in vacuum ambient and a-Si can be crystallized laterally from a Ni metal and a silicide seed, respectively. MILC length was observed by optical

microscope with Normaski filter.

2.2 The fabrication of MILC poly-Si TFTs

Figure 2-1 shows the process for the fabrication of a conventional MILC poly-Si TFTs. A 3000 Å thick SiO_2 layer was deposited on Corning 1737 glass for a buffer layer. A 600 Å thick a-Si thin film was deposited by LPCVD using SiH_4 gas at 520 ℃ and then, patterned by reactive ion etching (RIE) using SF_6, and O_2 gas. After the native oxide was eliminated by using a buffered-HF solution, PR patterns of wells were formed by conventional lithography for an off-set structure. A Ni film of 100 Å thickness was deposited by direct-current magnetron sputtering at room temperature and Ni islands were manufactured by lift-off methods. Samples were annealed at 570 ℃ for 5 h in H_2 ambient for lateral crystallization, and the remaining Ni was removed by H_2SO_4 solution. A 700 Å thick gate oxide (Gox) was deposited by PECVD using SiH_4 and N_2O gas at 420 ℃, and a MoW gate metal of 2000 Å thickness was formed by sputtering subsequently. The gate metal was etched by $H_3PO_4 + CH_3COOH + HNO_3 + H_2O$ etchant, and the gate oxide was etched by RIE using SF_6, Ar, and CHF_3 gas. The off-set length was 22 ㎛. The source-drain region was doped by an ion mass doping system (IMDS) using B_2H_6 source gas. The process condition of IMDS is

summarized at table 2-1.

The samples were annealed at 500 ℃ for 1h in H2 ambient for dopant activation. The electrical properties of the TFTs were measured by using a pico-ampere meter, HP4140B. The details of process were adjusted at table 2-2.

2.3 Measurement

To observe the microstructures of MIC/MILC regions, the samples were etched by secco etchant and were observed by field-emission scanning electron microscopy (FESEM). The electrical properties of the TFTs were measured using HP4140B. The threshold voltage was defined at a normalized drain current ($I_{DS} \times W/L$) of 0.1㎂ at V_D = 1V. The subthreshold swing, S, defined as the voltage required to increase the drain current by a factor of 10, is given by

$$S = \frac{dV_G}{d(\log I_D)} \tag{2}$$

From the straight line in the transfer curve, S is given by the maximum slope. The field-effect mobility was derived from the transconductance (g_m) in the linear region at V_D = 0.1V, given by

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=const.} = \frac{W}{L} C_i \mu_h V_D \quad (V_D < V_{Dsat}) \tag{3}$$

$$\mu_h = \frac{L}{WC_iV_D} g_m = \frac{L}{WC_iV_D} \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=const.} \quad (V_D < V_{Dsat}) \tag{4}$$

Where, W and L are width and length of channel, C_i is capacitance of insulator. We calculated the field-effect mobility of MILC poly-Si TFTs by equation (3) at every points of gate voltage and we calculated the mobility for maximum values. The maximum on/off ratio was defined at V_D = 10.1V and V_G = -30 to 15V

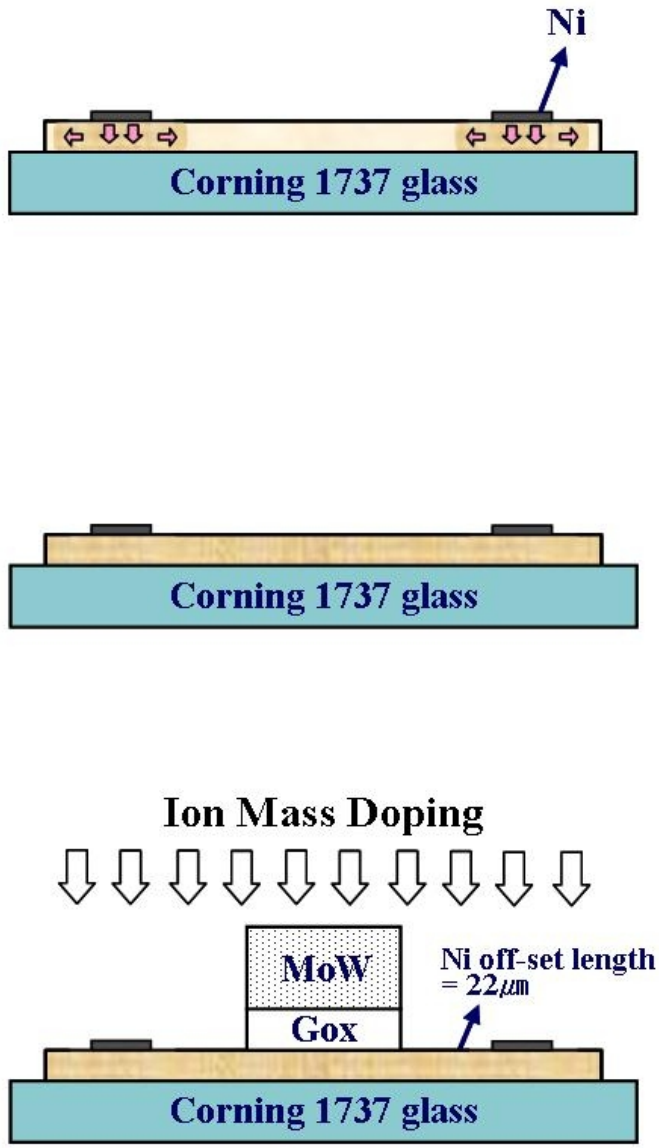

Fig 2-1. Fabrication procedure of conventional MILC poly-Si TFT.

Table 2-1. Ion mass doping conditions

	B_2H_6
Accelerating Voltage	**17 KeV**
RF power	**150 W**
Working Pressure	**5 mTorr**
Doping Time	**10 min**
Source Gas	**3% B_2H_6/H_2**

Table 2-2. Key processes for the fabrication of poly-Si TFT by MILC process

	apparatus	condition
Buffer oxide	**PECVD**	**3000 Å SiO_2 at 420 ℃**
a-Si Depo.	**LPCVD**	**1000 Å at 500 ℃**
Ni Depo.	**Sputter**	**100 Å at R.T**
Si crystallization	**Furnace**	**570 ℃ H_2 ambient**
Gate Oxide	**PECVD**	**1000 Å Nitride**
Gate Metal	**Sputter**	**2000 Å MoW**
S/D formation	**IMD**	**17 KeV, 150 W**
S/D activation	**Furnace**	**500 ℃ H_2 ambient**

Chapter 3

Channel thickness effects in bottom gate TFT

3.1 Introduction

LCD companies are turning to AMOLED where low temperature polycrystalline silicon (LTPS) TFT substrates are usually used as back planes. This is mainly because TFT back planes need high mobility and high reliability, since OLED displays require high brightness and long life time. But conventional LTPS back plane has a top gate structure and some difficulties in manufacturing for a large glass substrate. One of the reasons of this difficulties is the process complexity of LTPS, and the other is that the development of such manufacturing apparatus as eximer laser annealing(ELA) equipment or ion implantation equipment that also faces difficulties for large substrate application. Conventional amorphous silicon TFT has a bottom gate structure that is more easily manufactured for larger glass substrate. However, the performance of the electrical properties, especially the reliability, is insufficient for OLED displays. In order to obtain uniform TFT characteristics and methods have been proposed. Among several crystallization methods, solid phase crystallization (SPC) of amorphous silicon (a-Si) has

some advantages of low-cost and good uniformity compared to ELC poly-Si [1]. Recently, a high-quality poly Si related with Ni-mediated crystallization has been demonstrated such as metal induced lateral crystallization (MILC)[2], continuous grain silicon (CGS)[3]. Due to this reason, Poly Si bottom gate TFT by non laser crystallization method must be necessary in LCD line. LCD Company make AMOLED panel by adding annealing process. Bottom gate TFT can be made by in-situ deposition. In this paper, we studied on improvement of bottom gate P-channel poly Si TFT applicable to LCD line. The effects of the channel thickness were investigated.

3.2 Experiments

In this study, thin film transistors were successfully fabricated on corning 7059 glass substrate by MILC. A-1000Å thick Nitride thin film was deposited as a buffer layer by plasma enhanced chemical vapor deposition (PECVD). MoW (1000Å) was deposited on Corning 1737 glass by DC sputtering for gate metal [4]. After patterning gate metal, SiNx and SiO_2 film was deposited as a gate insulator [5] and a-Si film was deposited as channel by PECVD and LPCVD, respectively In MILC rate, a-Si in LPCVD has higher rate than a-Si in

PECVD.[6] Fig3-2 shows MILC rate between LPCVD Si and PECVD Si. 1000 Å SiO_2 was deposited as etch stopper by PECVD. After patterning etch stopper, 1000 Å thick P+ a-Si was deposited by PECVD. 10nm thick Ni dots as a catalyst metal for MILC were sputter deposited and patterned by lift-off process. MoW (500Å) was deposited as metallization to reduce contact resistance. Additional mask was used to etch P+ layer on channel. Lateral crystallization was carried out at 550℃ for 4hours in H_2 ambient[7]. After annealing, active layer was patterned and etched by RIE. Each layer was indicated in figure 3-1.

3.3 Results and Discussion

Fig3-3 shows I-V curve in different channel thickness of bottom gate TFT. The thinner in channel, the lower in mobility. Surface mobility is lower than the bulk mobility, since the carriers in the channel undergo surface roughness scattering in addition to the bulk scattering mechanisms. At V_d 0.1V, channel thickness must be 400Å to operate switching. The more thick, the more in the I_{on} currents and I_{off} currents. There is no change in slope. As channel thickness increases, Vth decreases. Fig3-4 shows I-V curve in different channel thickness of bottom gate TFT (V_d=5V). If the drain voltage increases from 0.1V to 5V, transistor

operates at 100Å of channel thickness.

Fig3-5 shows length effects in different channel thickness of bottom gate TFT. Length effects are higher in thinner channel. Total graphs were shifted to Y direction. As the channel thickness increases, the differences in the leakage currents reduce. The longer in channel length, the more in I_{on} currents and I_{off} currents. Above 400Å, I_{on} currents and I_{off} currents is not susceptible to length. Fig3-6 shows width effects in different channel thickness of bottom gate TFT. There are no tendencies in width effects. Fig3-7 shows electrical stress effects in different thickness of the bottom gate poly Si TFT. The thinner in channel thickness, the more in stability. Variations in electrical performance indicate the stability. Defect density is related to stability in TFT.

3.4 Summary

In bottom gate poly Si TFTs, channel thickness was investigated for optimization of electrical performance. In thin channel, length has effects on electrical performance due to low mobility. And at high drain voltage, TFT of thin channel operate for switching. In these results, Mobility and Ion currents are related to lateral field. To apply for panel, 400Å~600Å is suitable for switching transistors.

3.5 References

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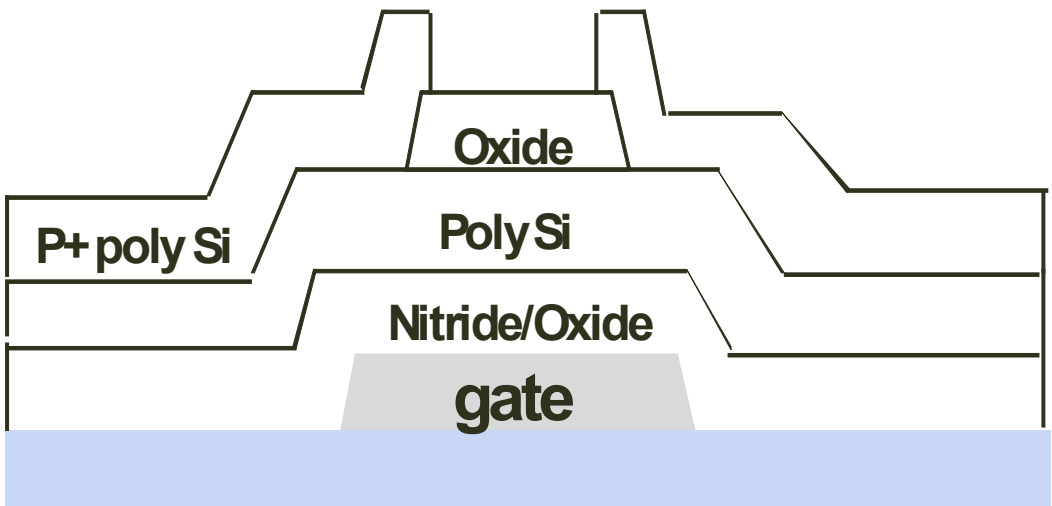

Fig.3-1. Schematic cross-sectional view of a bottom-gate poly Si TFT

with P+ poly Si

	Gate	GI(PE)	I-Si(LP)	P+ Si(PE)	Etch stopper
Material	**MoW(1000Å)**	**Nit700 Å/Ox300 Å**	**100~900 Å**	**1000 Å**	**1000 Å**

Table.3-1. detailed layer in bottom gate poly-Si TFTs.

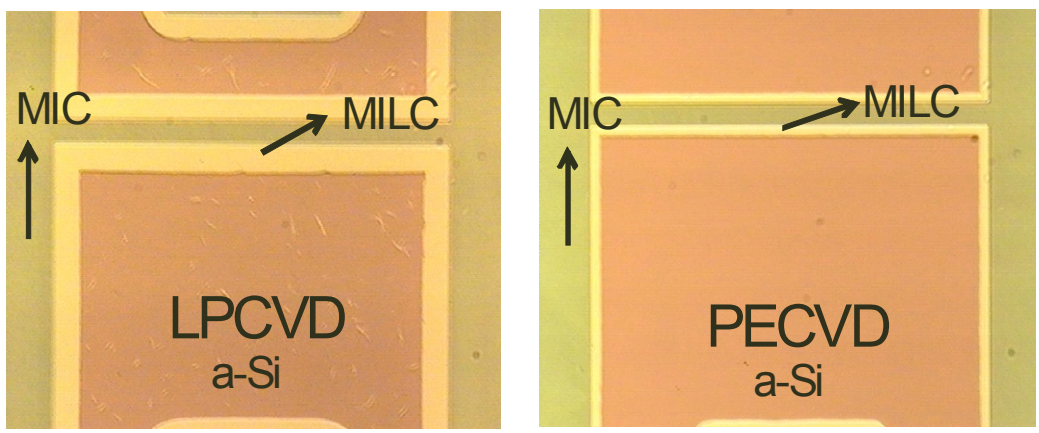

Fig.3-2. Different MILC rate in LPCVD Si and PECVD Si

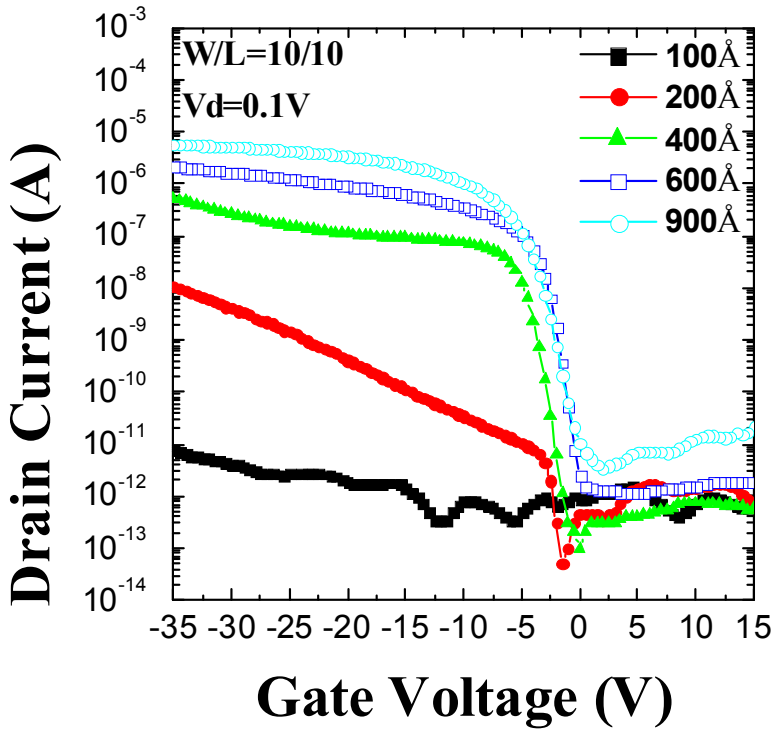

Fig.3-3. I-V curve in different channel thickness of bottom gate TFT

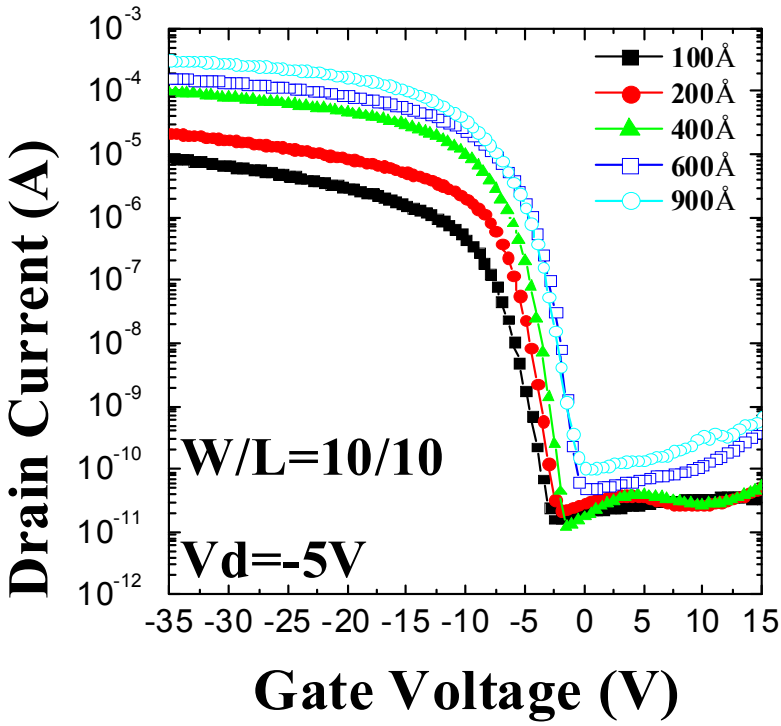

Fig.3-4.I-V curve in different channel thickness of bottom gate TFT

Channel	100Å	200Å	400Å	600Å	900Å
Slope(V/dec)	1.29	0.76	0.67	0.62	0.88
I_{on} ($x10^{-5}$)	0.89	2.21	9.91	16.7	31.9
I_{off} ($x10^{-11}$)	1.05	2.18	1.26	4.94	9.9
Mobility (cm^2/Vs)	0.2	0.5	22	28	72
I_{on}/I_{off} ($x10^6$)	8.5	10	7.8	3.3	3.2
V_{th}(V)	-26.5	-11	6.5	-4.5	-5

Table.3-2. Device parameters in different channel thickness of bottom gate TFT

(V_d= 5V)

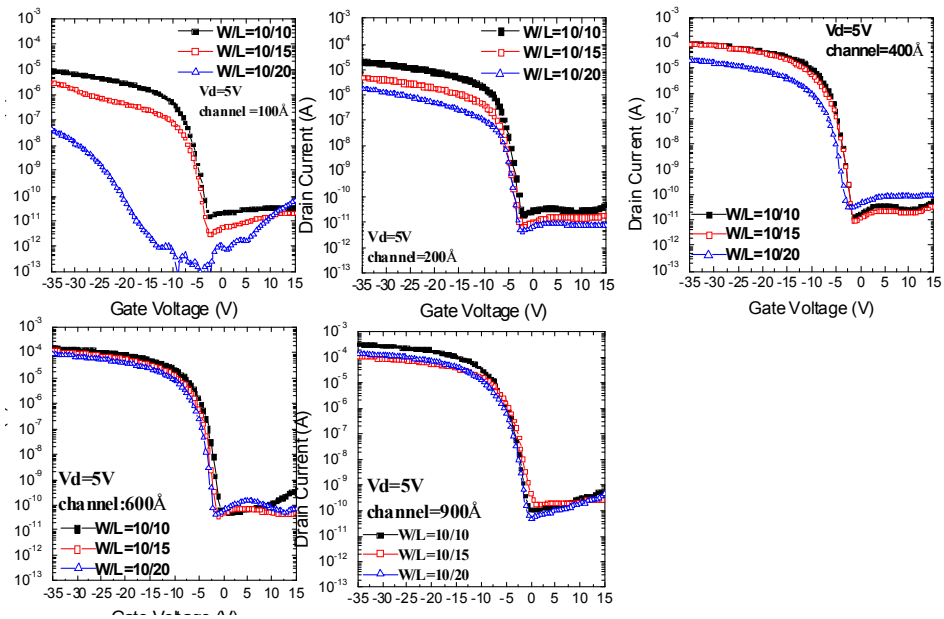

Fig.3-5. Length effects in different channel thickness of bottom gate TFT

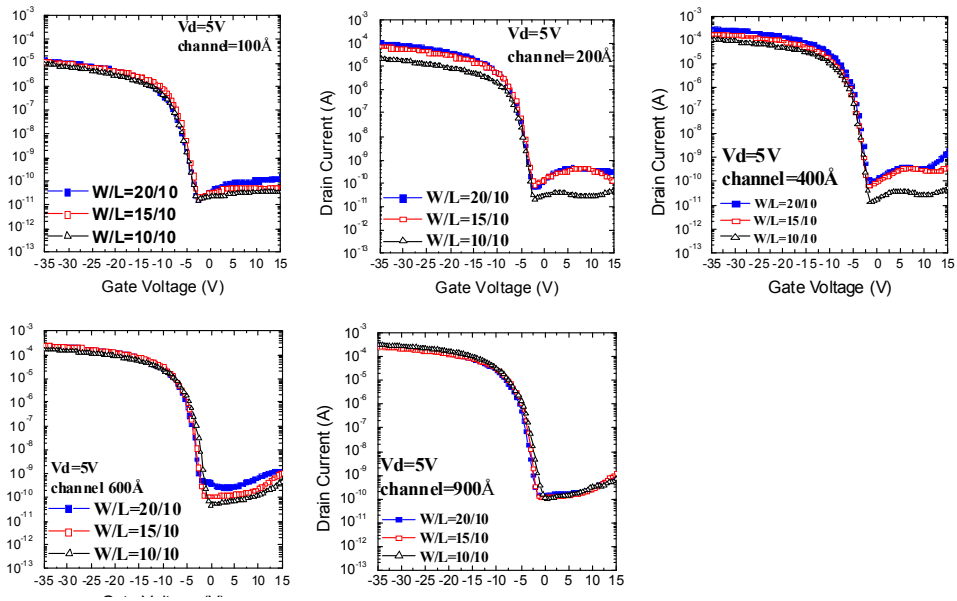

Fig.3-6. Width effects in different channel thickness of bottom gate TFT

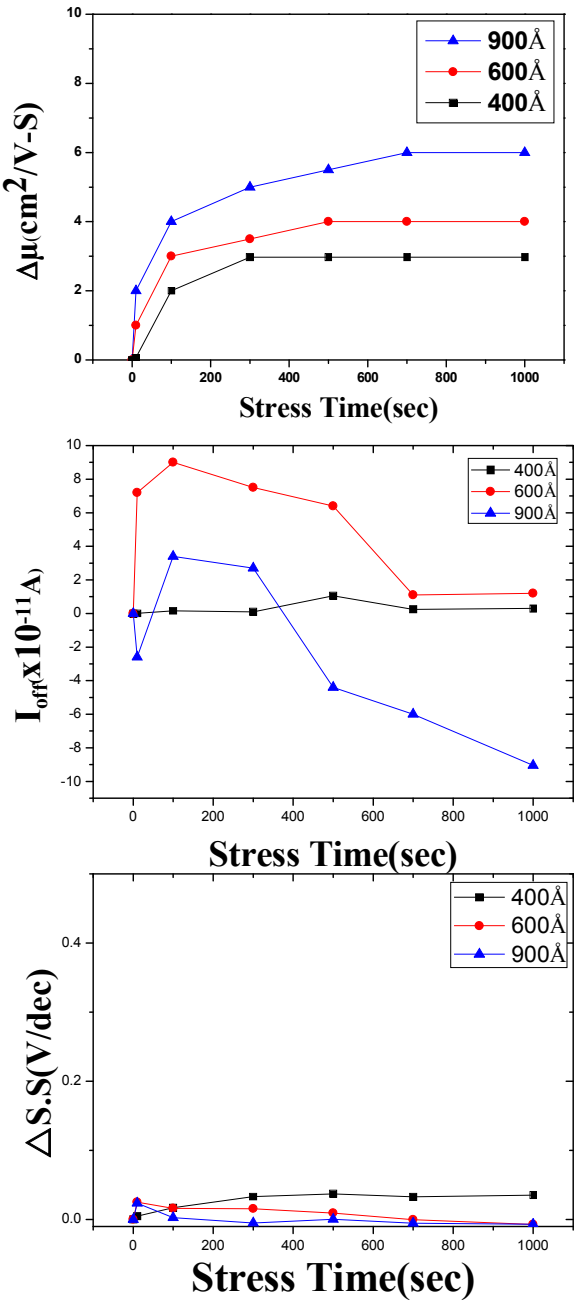

Fig.3-7. electrical stress effects in different thickness of the bottom gate

Poly-Si TFT

Chapter 4

Overlap effects in bottom gate TFT

4.1. Introduction

LCD companies are turning to AMOLED where low temperature polycrystalline silicon (LTPS) TFT substrates are usually used as back panel. This is mainly because TFT back planes need high mobility and high reliability, since OLED displays require high brightness and long life time. In display company, LTPS back plane has a top gate structure and some difficulties in manufacturing for a large glass substrate. One of the reasons of this difficulties is the process complexity of LTPS, and the other is that the development of such manufacturing expensive equipment as eximer laser annealing(ELA) equipment or ion implantation equipment that also faces difficulties for large substrate application. In LCD manufacturing line, amorphous silicon TFT has a bottom gate structure that is more easily manufactured for larger glass substrate. However, the performance of the electrical properties, especially the reliability, is insufficient for OLED displays. In order to obtain uniform TFT characteristics and methods have been proposed. Among several crystallization methods, solid phase

crystallization (SPC) of amorphous silicon (a-Si) has some advantages of low-cost and good uniformity compared to ELC poly-Si [1]. Recently, a high-quality poly Si related with Ni-mediated crystallization has been demonstrated such as metal induced lateral crystallization (MILC) [2], continuous grain silicon (CGS). [3] Due to this reason, Poly Si bottom gate TFT by non laser crystallization method must be necessary in LCD line. LCD Company make AMOLED panel by adding annealing process. Bottom gate TFT can be made by in-situ deposition. In LCD manufacturing line, there is no ion implantation process for source and drain formation. Comparing with top gate structure, Overlap in bottom gate TFT is important. In this paper, we studied on overlapping effects on leakage currents of Poly-Si TFTs. The optimization of each layer was investigated.

4.2. Experiments

Figure4-1 shows the schematic cross-section of a bottom-gate p-channel poly Si TFT with P+ poly Si layer. In this study, thin film transistors were successfully fabricated on corning 7059 glass substrate by MILC. A-1000Å thick Nitride thin film was deposited as a buffer layer by plasma enhanced chemical vapor deposition (PECVD). MoW (1000Å) was deposited on Corning 1737 glass by DC sputtering for gate metal. After patterning gate metal, SiNx and SiO_2 film

was deposited as a gate insulator [4] and a-Si film was deposited as channel by PECVD and LPCVD, respectively In MILC rate, a-Si in LPCVD has higher rate than a-Si in PECVD.[5] 1000 Å SiO_2 was deposited as etch stopper by PECVD. After patterning etch stopper, 1000 Å thick P+ a-Si was deposited by PECVD. 10nm thick Ni dots as a catalyst metal for MILC were sputter deposited and patterned by lift-off process. MoW (500Å) was deposited as metallization to reduce contact resistance. Additional mask was used to etch P+ layer on channel. Lateral crystallization was carried out at 550℃ for 4hours in H_2 ambient. After annealing, active layer was patterned and etched by RIE.

4.3. Results and Discussion

Fig4-2 shows Overlap effects in bottom gate poly Si TFT. TFT has different characteristics due to misalignment. The δ means distance between S/D and gate. The δs is distance from source and gate. The δd is distance from drain and gate. + ,- symbols mean overlap and offset. Table1 summarize the relation between overlap and electrical properties. The structure with overlap in source and offset in drain is the best structure. Ion current drastically decrease in offset of source (>1.5μm). I_{off} current decreases in offset of drain. Above 1.5 μm in offset of drain, there is no difference in leakage currents. Fig4-3 shows the electrical properties

measuring reverse direction. Main change is that transistor doesn't operate in offset of source (>2.5 μm). This graph was not shown. Long offset (>2.5 μm) in source prevent conduction from source to drain. To confirm only overlap effects, channel and gate insulator were fixed at 400Å and 1000Å respectively. At two side overlap, channel length is more shortened than gate length. I_{on} currents increase due to reduction in channel. Offset region in drain have effects on leakage currents. In this point, lateral field causes leakage currents. Fig4-4 shows schematic measuring condition.

Fig4-5 shows drain voltage effects in different overlap distance. Other condition is same in Fig4-2. TFT has high leakage currents in high drain voltage and overlapped drain. At drain 0.1V, TFT with source and drain offset (>1.5 μm), TFT didn't have operating characteristics. For long offset δs (>1.5 μm), TFT works from 2V of drain voltage. It needs lateral field to conduct carrier from source to drain. Regardless of drain voltages, TFTs operate in 0.5 offset of source (<0.5 μm). Fig4-7 shows I-V curve in different overlap (overlap, selfalign, offset). In overlap and selfalign, there is no difference in on currents. In selfalign, leakage currents reduced than overlap structure. In offset structure, on current and off currents is the lowest among the three cases. In this results, distance between drain and gate has effects on leakage currents.

In same overlapping, channel thickness effects were shown in Fig4-9. In thick channel (900Å), leakage currents were reduced. Channel layer exists between P+ layer and gate metal. The distance increased vertically.

Fig4-11 shows gate insulator thickness effects in same overlap structure. The more in gate insulator thickness, the lower in off currents. As the thickness increases, capacitance of gate insulator reduces. So slope increases and Ion current decreases. In this case, only gate insulator thickness was changed. Gate insulator has role in distance between drain and gate. But in this case, capacitance was changed simultaneously. It is difficult to consider only gate insulator thickness effects for reduction in the leakage currents.

4.4. Summary

In this work, effects of lateral field and vertical field were investigated. Distance between S/D and gate is related to on current and off current. Overlap in source has effects on I_{on}. overlap in drain increase the leakage currents. Changing the channel thickness and gate insulator thickness, the leakage currents was changed. Vertical field effects were confirmed. In real panel, signal was transported in two sides. Asymmetry structure is applicable to inverter operation.

4.5. References

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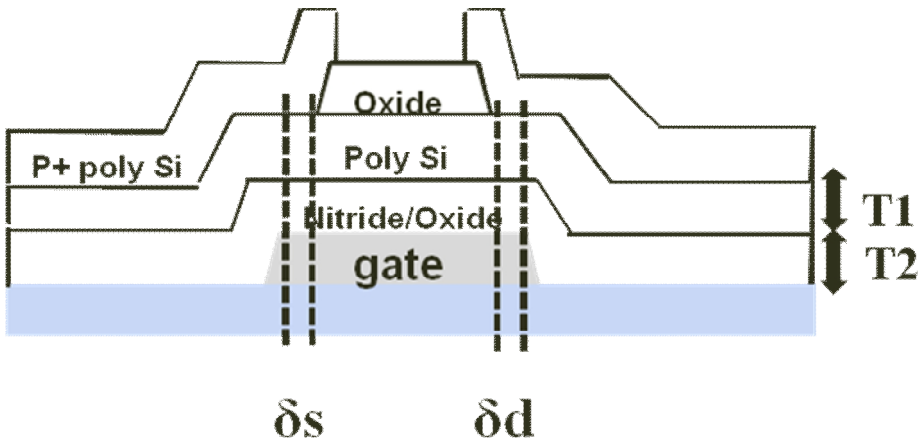

Fig.4-1. Schematic cross-sectional view of a bottom-gate poly Si TFT

with P+ poly Si

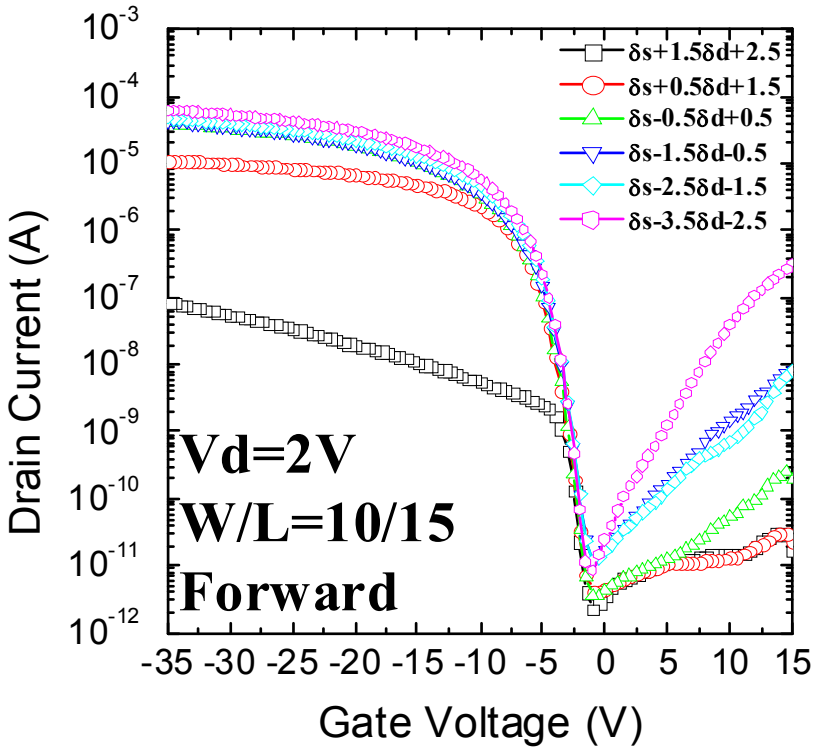

Fig.4-2. Overlap effects in forward direction of measurement.

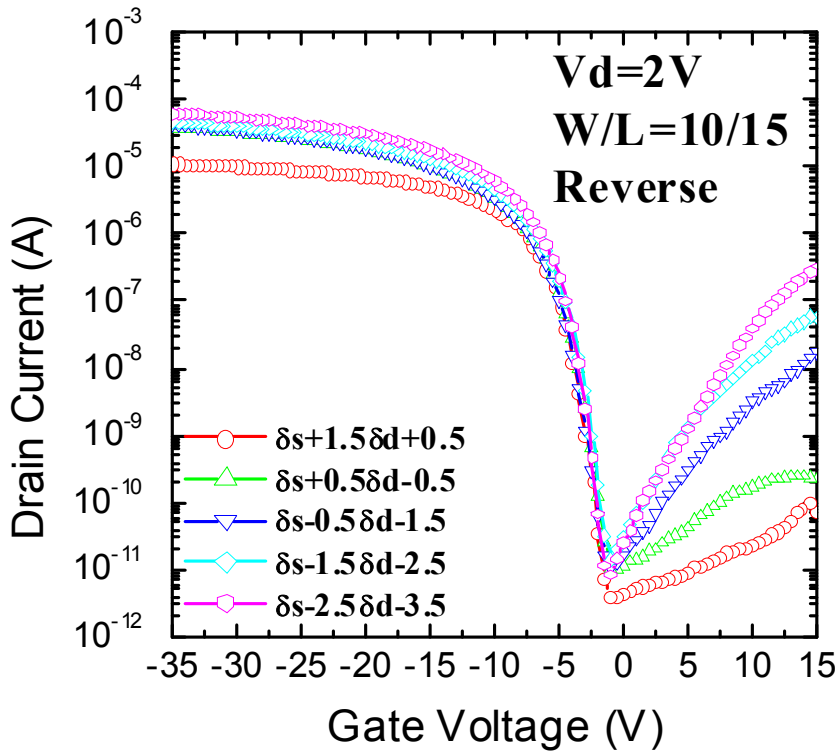

Fig.4-3. Overlap effects in reverse direction of measurement

+ : offset -: overlap	I_{on}	I_{off}
δs(+), δd(+)	↓	↓
δs(-) ,δd(+)	↑	↓
δs(+), δd(-)	↓	↑
δs(-), δd(-)	↑	↑

Table.4-1. the relation between overlap and electrical properties

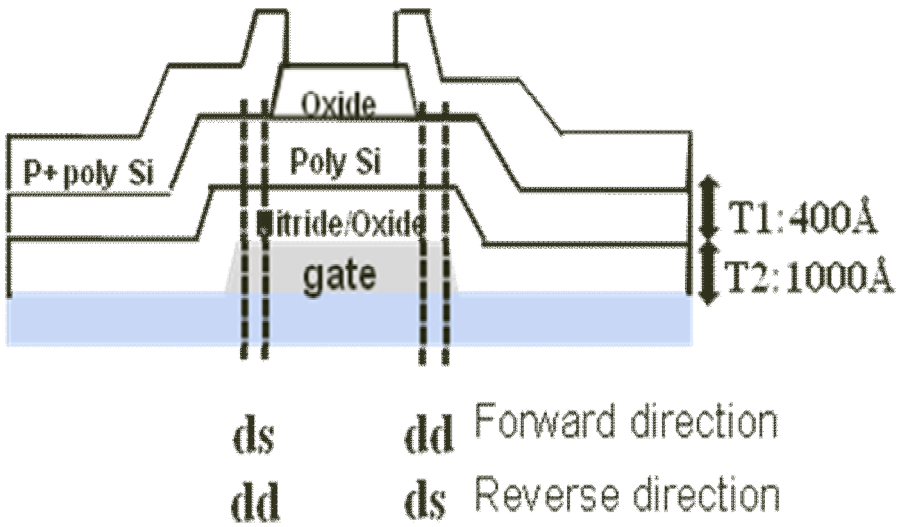

Fig.4-4. Overlap effects in bottom gate TFT

(channel: 400Å, gate insulator: 1000 Å)

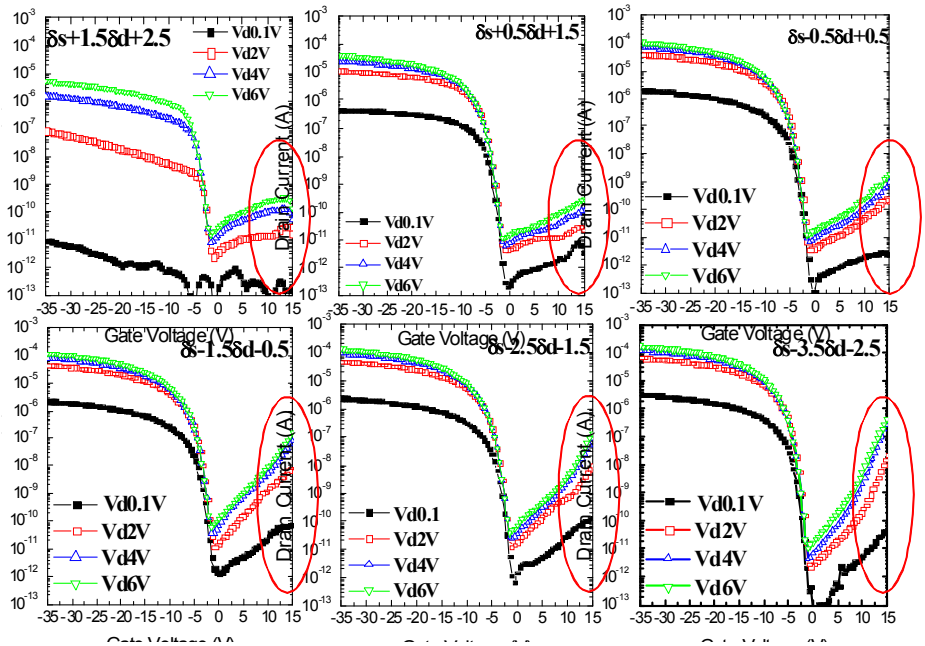

Fig.4-5. Drain voltage effects in different overlap.

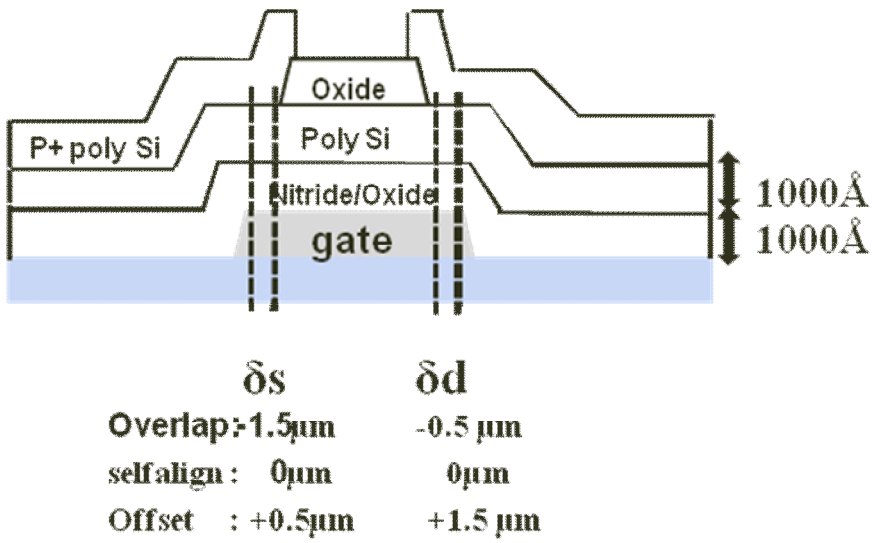

Fig. 4-6.overlap structure in different overlap

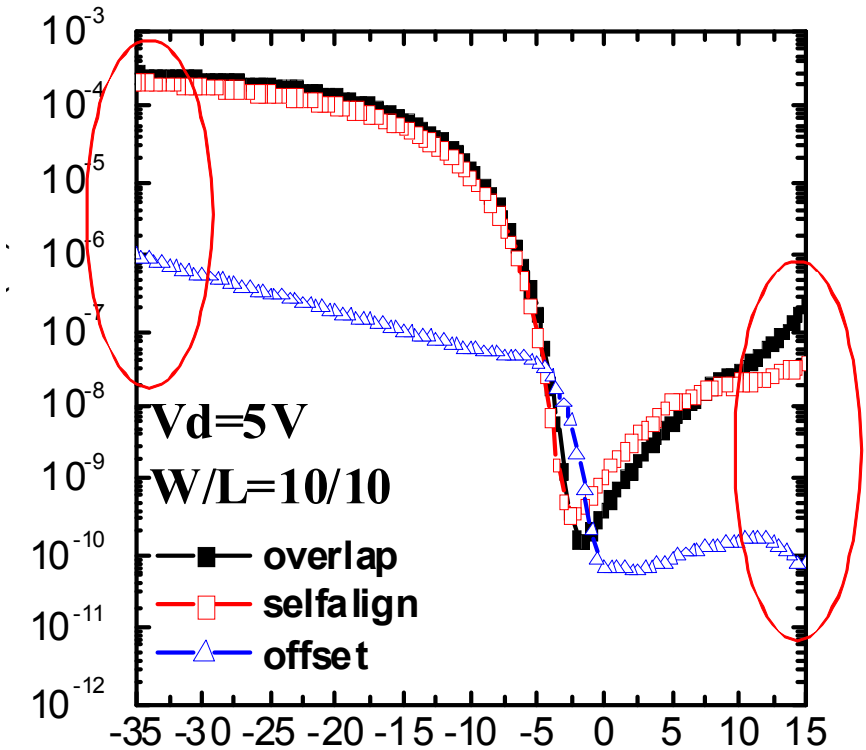

Fig.4-7. I-V curve in different overlap (overlap, selfalign, offset)

	$\mu(cm^2/VS)$	V_{th} (V)	Slope(V/dec)	$I_{on}(x10^{-4}$ A)	$I_{off}(x10^{-10}$ A)
Overlap	66	-6	0.77	3.03	1.07
Selfalign	50	-6.5	0.8	2.4	3.7
offset	2	-35	1	0.007	0.6

Table.4-2. Key parameter in I-V curve in different overlap

(Overlap, self align, offset)

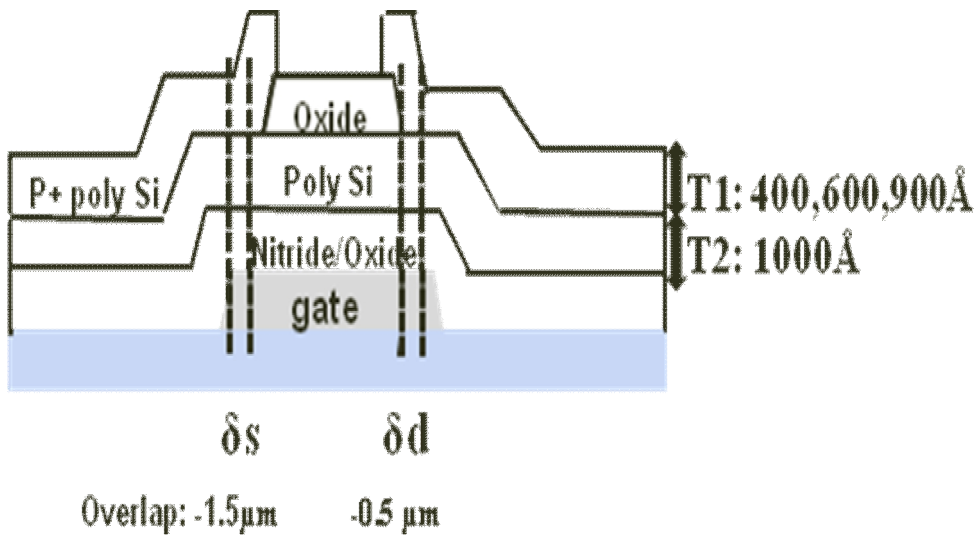

Fig.4-8. Schematic cross-section of a bottom-gate p-channel poly Si TFT for channel thickness effects

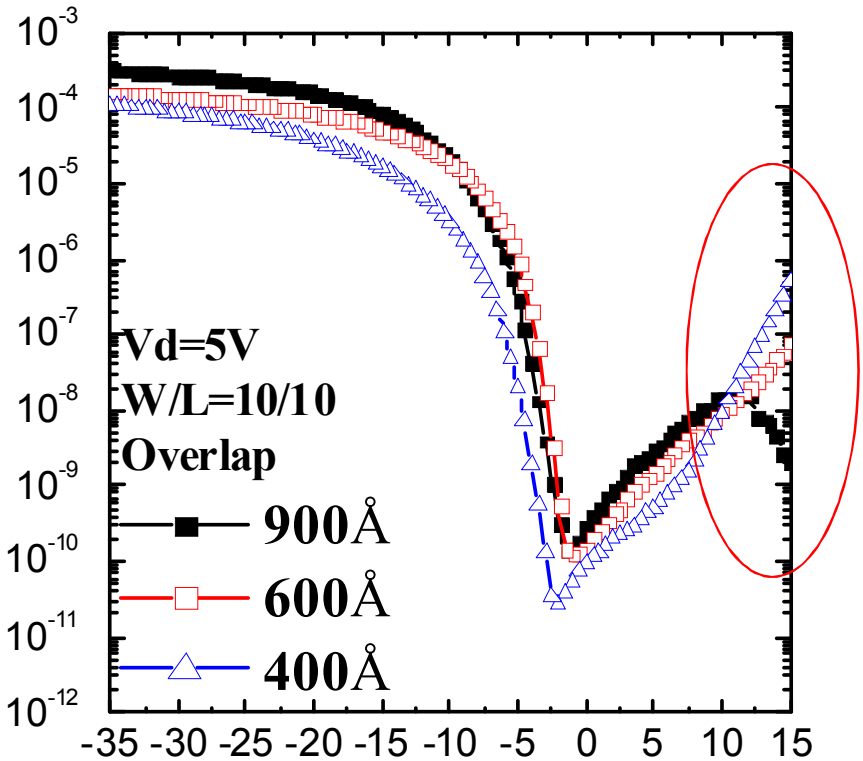

Fig.4-9. Channel thickness effects in same overlap structure

	$\mu(cm^2/VS)$	$V_{th}(V)$	Slope(V/dec)	$I_{on}(x10^{-4}A)$	$I_{off}(x10^{-10}A)$
400Å	24	-8	0.78	1.07	0.32
600Å	49	-5	0.62	2.3	3.69
900Å	72	-6	0.87	3.18	1.44

Table.4-3. Key parameter in I-V curve in different channel thickness

of the same overlapping

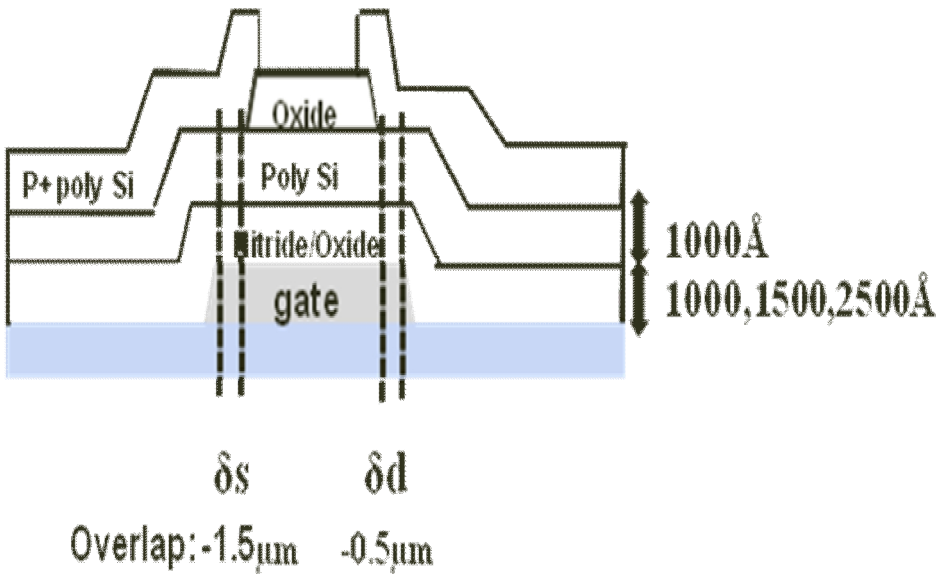

Fig.4-10. Schematic cross-section of a bottom-gate p-channel poly Si TFT

for gate insulator thickness effects

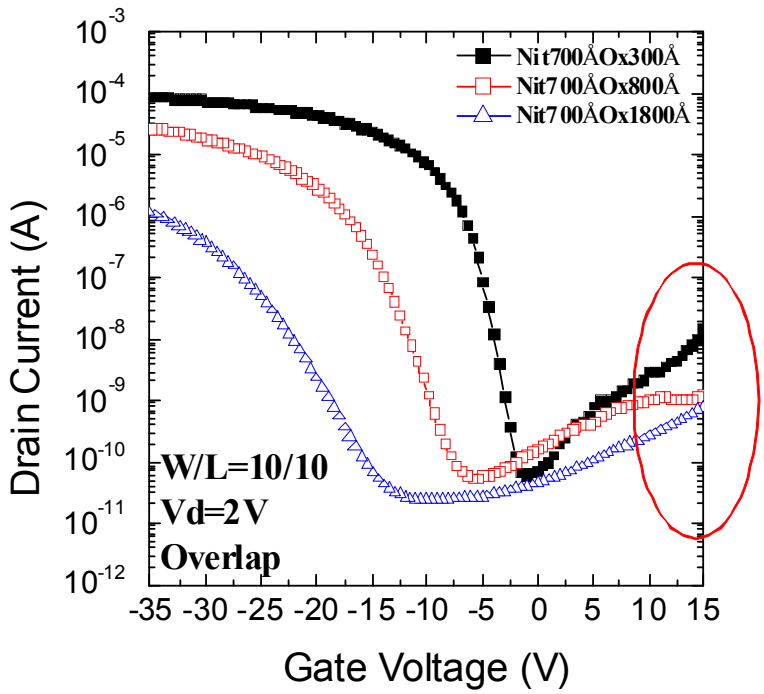

Fig.4-11. Gate insulator thickness effects in same overlap structure

Chapter 5

Channel doping effects

5.1. Introduction

Intensive study on poly-crystalline silicon thin film transistors with high mobility is underway in support of the competition to set the latest trend in high-definition, high speed and large area transistors. In addition to this research, next-generation technology is enabling the commercial use of organic light emitting diode (OLED) displays. Due to the high interest in OLED, the use of poly-crystalline thin film transistors will be necessary. In order to transfer a-Si to poly-silicon, a silicon thin film has to be heated to above 700 ºC to create a so-called Low Temperature Poly Silicon (LTPS), which is needed for a device on a common glass substrate. Laser scanning has been known as the most important LTPS process. However, laser annealing method has many problems, such as expensive cost, poor surface roughness in interface of Si and nonuniformity of the electrical performance. Solid phase crystallization process has lower cost than laser crystallization method. But crystallization temperature (>600ºC) in SPC is high for processing glass substrate. In this aspect, metal induced lateral crystallization (MILC) method has advantages

for other crystallizing method. This process lowered crystallization temperature below 550ºC. The cost is not expensive for processing glass substrate. Although MILC TFT has high mobility, problem remains in leakage currents. The leakage currents must be reduced for operational transistors. In this reason, channel doping[1-3] is done for reducing the leakage currents.

5.2. Experiments

Fig5-1 shows various channel doping method for lightly doping. In process 1, direct channel doping was shown. A-3000 Å thick SiO2 thin film was deposited as a buffer layer by plasma enhanced chemical vapor deposition (PECVD). A-1000 Å thick a-Si thin film was deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C using SiH4 as the precursor. Active region was patterned. On top of active area of Si, Ni mask pattern was formed and Ni sputtering was done. By lift-off process, Ni remains on source and drain(S/D). After lift-off process, Ni was removed by H_2SO_4. After Ni removal process, annealing of MILC (metal induced lateral crystallization) was carried out at 550ºC for 2hours in H_2 ambient. After MILC process, channel doping was done using ion mass doping method. For lightly doping, DC voltage applied from 0.2kv to 0.7kv for 1min. A-1000 Å thick SiNx film was deposited as a gate

insulator and 2000 Å thick MoW film was deposited as a gate electrode by PECVD and sputtering, respectively. After gate electrode definition, lightly doped drain (LDD) region was formed using additional mask. To form source and drain(S/D) region, Ion Mass Doping (IMD) was done. The dopant gases used were PH3 for n-type and B2H6 for P-type. To activate dopant, annealing was processed in H2 ambient at 550 ºC for 2 h. For channel doping type, homo type and hetero type were fabricated in N channel and P channel. In channel doping method 2, channel doping was done by using ion mass doping before MILC annealing. Other processing conditions are the same. In channel doping method 3, SiNx film and thick Si was used for barrier layer. Unlike method 1, DC voltage is 17kV for 10min. and after channel doping, different etching time was applied for controlling dopant concentration. The more time in etch, the lower in concentration of dopant in channel. In channel doping method 4, channel was doped by using PECVD method. After MILC, N+ layer was deposited on poly Si channel. And N+ layer was removed using KOH without additional annealing. In channel doping5, additional annealing was carried out for diffusion of dopants in channel.

5.3. Results and Discussion

Fig5-2 shows I-V curve in P channel TFT. Depending on concentration of dopant in channel, Vth shift was conformed.[4] The more doping in channel, the worse in the characteristics of TFT. Mobility was lowered than conventional TFT. An increase in channel dopant concentration degrades the surface mobility.

Fig5-3 shows I-V curve in N channel TFT. Depending on concentration of dopant in channel, Vth shift was conformed. The more doping in channel, the worse in the characteristics of TFT. Mobility was lowered than conventional TFT. Fig5-4 shows hetero type in P-TFT using channel doping method 1. The more doping, the more degradation in the characteristics of TFT.

Fig5-5 shows hetero type in N-TFT using channel doping method 1. After channel doping, TFT doesn't operate. Regardless of gate voltage, drain currents is constant.Fig5-6 shows homo type in P-TFT using channel doping method 1. The more doping, the more degradation in the characteristics of TFT. Comparing with Fig5-2, switching operational characteristics disappear. Activation behavior of dopant is different in grain and grain boundary.

Fig5-7 shows homo type in P-TFT using channel doping method 3. The more time in etch, the lower dopant concentration in channel. In this case, channel thickness also reduced. As the etching time increased, 'TFT starts to operate. It is

difficult to etch doped Nitride. When nitride was etched, O_2 in the RIE etching condition was used.

Fig5-8 shows homo type in N-TFT using channel doping method 4 and 5. In channel doping method 4, there is no difference in leakage currents. In channel doping method 5, leakage currents are reduced. It needs energy to diffuse dopants.

5.4. Summary

The channel doping was done in Poly Si TFT. In ion mass doping method, it is limited to control dopant concentration. Although lightly doping was carried out, TFT's leakage currents were not reduced. But In channel doping by PECVD, leakage currents is reduced. Channel doping method is important. It is necessary to dope dopant lightly and deeply. And it is confirmed that channel doping has effects on control threshold voltage.

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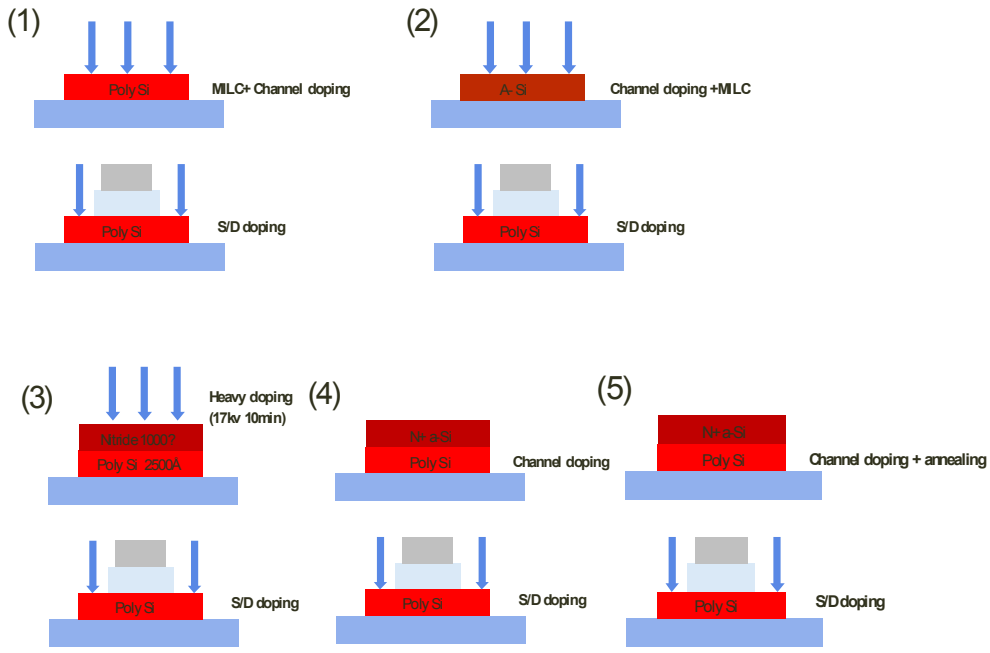

Fig.5-1. various channel doping method for lightly doping

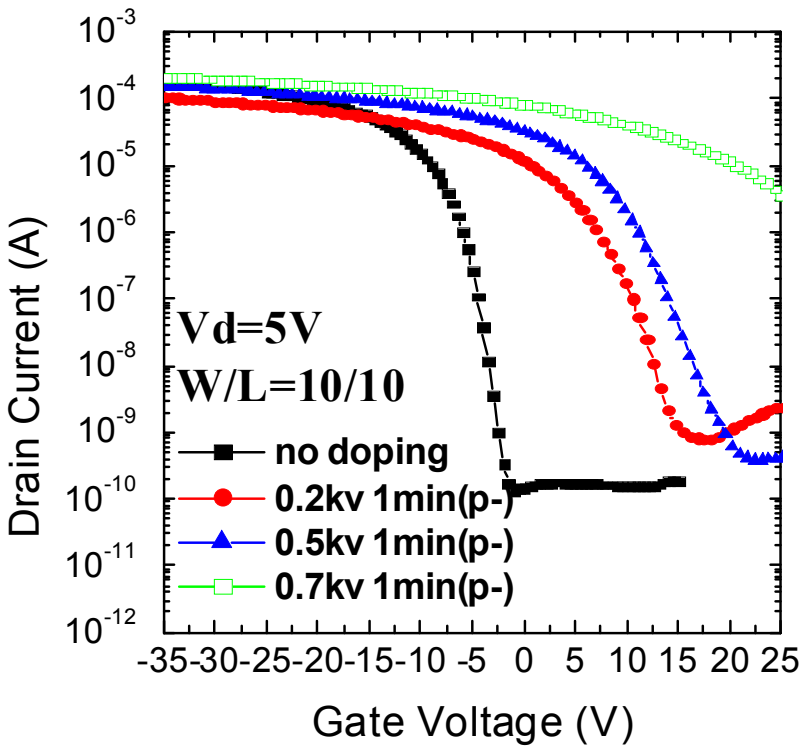

Fig.5-2. Homo type in P-TFT using channel doping method 1.

	μ(cm^2/VS)	V_{th} (V)	Slope(V/dec)	I_{on}(x10^{-4}A)	I_{off}(x10^{-11}A)
Reference(PTFT)	**37**	**-6**	**0.9**	**1.32**	**9**
P-doping(0.2kv)	**13**	**7**	**1.83**	**0.67**	**50**
P-doping(0.5kv)	**20**	**11**	**2.02**	**1.06**	**30**
P-doping(0.7kv)	**17**	**29**	**2.79**	**1.39**	**700**

Table.5-1. Device parameters in homo type p channel poly Si TFT of different dopant concentration.

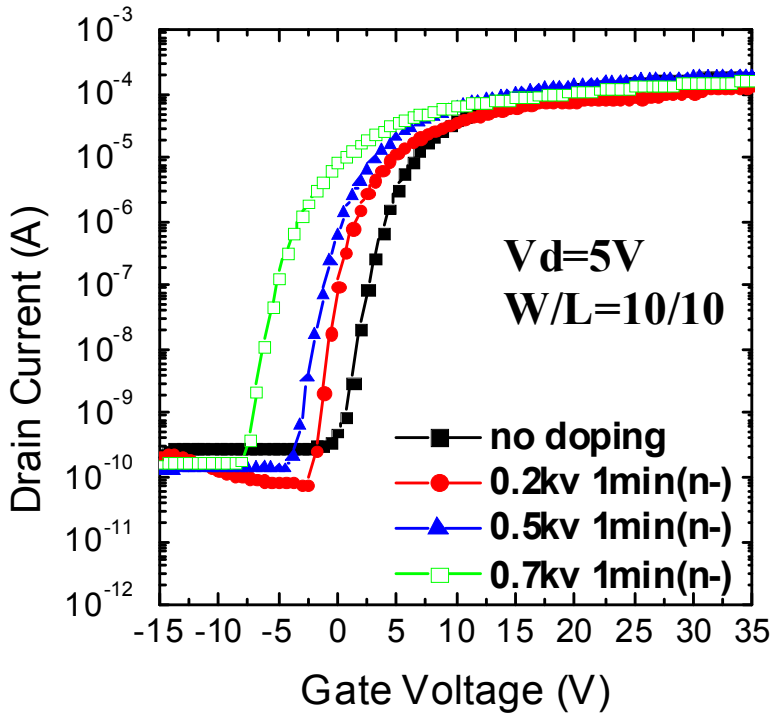

Fig.5-3. Homo type in N-TFT using channel doping method 1.

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}(x10^{-4} A)	I_{off}(x10^{-11} A)
Reference(NTFT)	**62**	**4.38**	**0.86**	**1.54**	**20**
N-doping(0.2kv)	**45**	**1.88**	**0.74**	**0.91**	**6**
N-doping(0.5kv)	**45**	**0.62**	**0.86**	**1.39**	**10**
N-doping(0.7kv)	**32**	**-3.12**	**0.85**	**1.21**	**10**

Table.5-2. Device parameters in homo type N channel poly Si TFT of different dopant concentration.

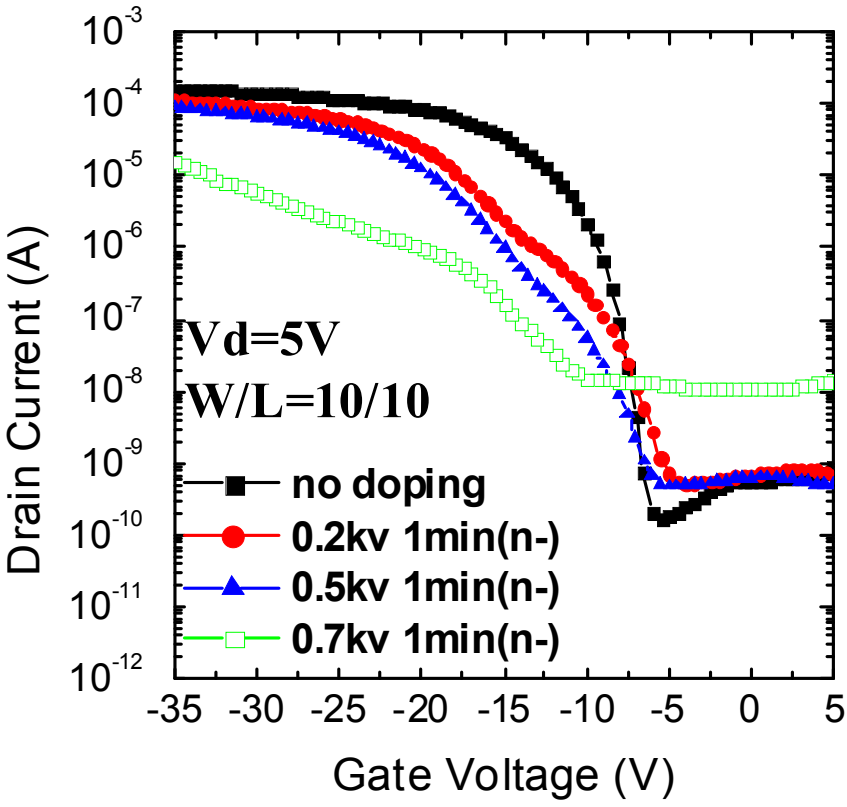

Fig.5-4. Hetero type in P-TFT using channel doping method 1

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}(x10^{-4} A)	I_{off}(x10^{-11}A)
Reference(PTFT)	**50**	**-9**	**0.68**	**1.15**	**9.4**
N-doping(0.2kv)	**33**	**-13.5**	**1.2**	**0.76**	**20**
N-doping(0.5kv)	**28**	**-15**	**1.1**	**0.64**	**20**
N-doping(0.7kv)	**23**	**-23**	**2.3**	**0.14**	**400**

Table.5-3. Device parameters in hetero type p channel poly Si TFT

of different dopant concentration

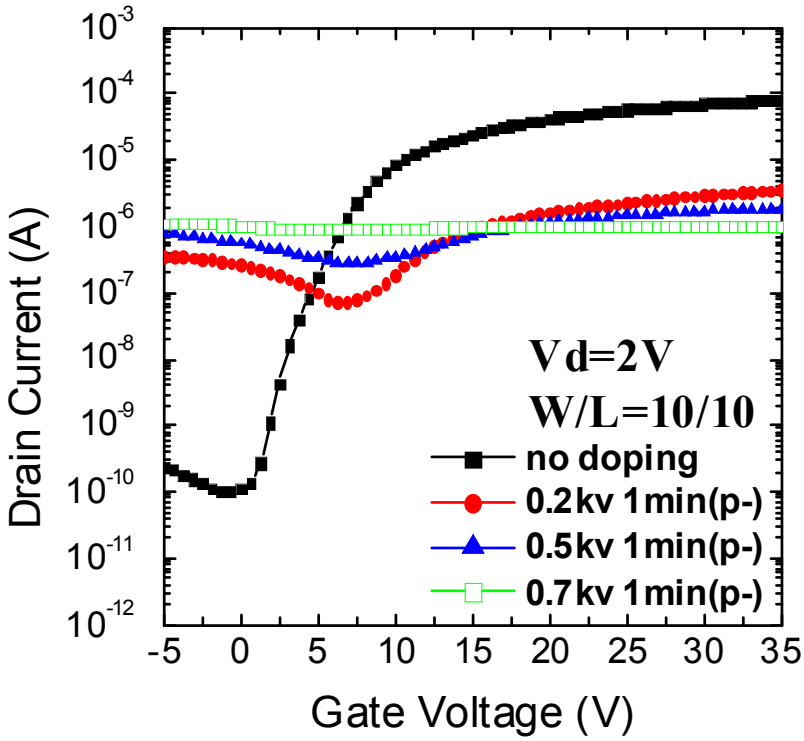

Fig.5-5. Hetero type in N-TFT using channel doping method 1

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}($x10^{-4}$A)	I_{off}($x10^{-11}$ A)
Reference(NTFT)	**25**	**6.88**	**0.98**	**0.91**	**8.19**
P-doping(0.2kv)	**0.8**	**18**	**6.1**	**0.026**	**2000**
P-doping(0.5kv)	**0.9**	**21**	**2.9**	**0.01**	**4000**
P-doping(0.7kv)	**0.92**	**35**	**5.3**	**0.005**	**50000**

Table.5- 4. Device parameters in hetero type N channel poly Si TFT of different dopant concentration.

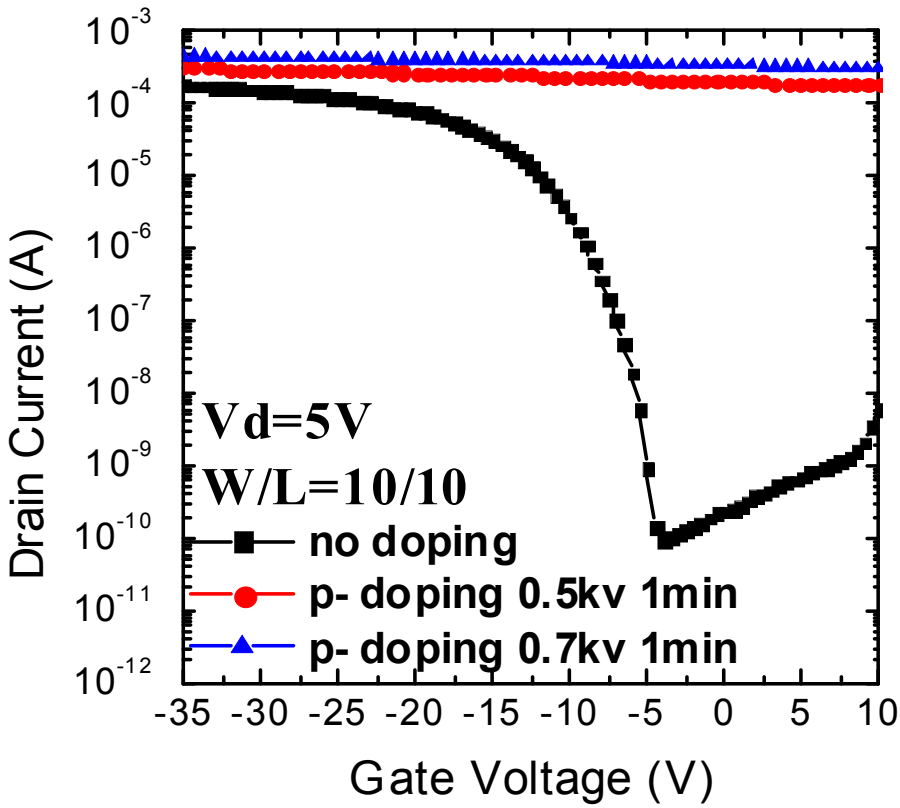

Fig.5-6. Homo type in P-TFT using channel doping method 2

	μ (cm^2 /VS)	V_{th} (V)	Slope (V/dec)	I_{on}(x10^{-4} A)	I_{off}(x10^{-11} A)
Reference(PTFT)	**46**	**-9**	**0.57**	**1.26**	**6.05**
P-doping(0.5kv)	**21**	**40**	**41**	**2.07**	**10000000**
P-doping(0.7kv)	**17**	**40**	**135**	**3.01**	**17000000**

Table.5-5. Device parameters in homo type p channel poly Si TFT of different dopant concentration.

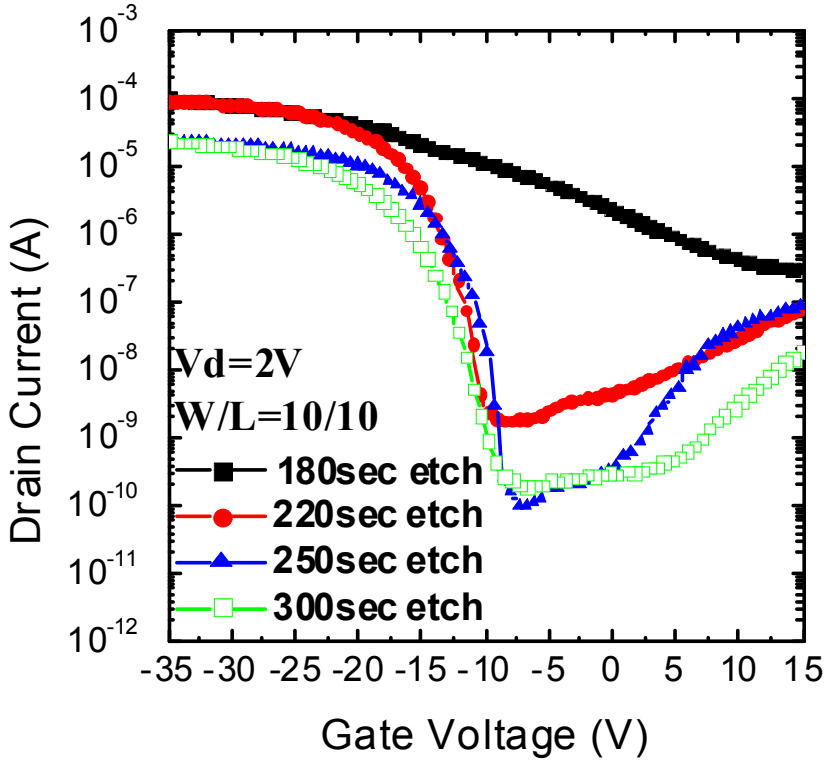

Fig.5-7. Homo type in P-TFT using channel doping method 3

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}(x10^{-4} A)	I_{off}(x10^{-11} A)
180sec etch	106	7	11	1.91	50000
220sec etch	90	-13.4	0.96	1.68	300
250sec etch	23	-13.4	0.7	0.38	10
300sec etch	22	-15.8	0.8	0.32	20

Table.5-6. Device parameters in homo type p channel poly Si TFT

of different dopant concentration

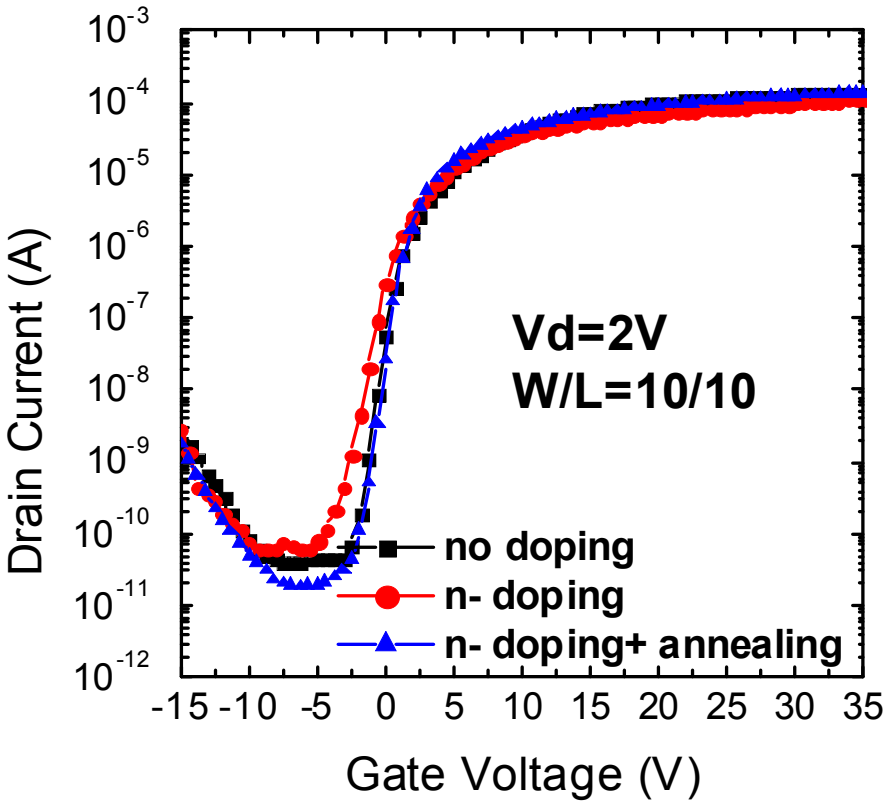

Fig.5-8. Homo type in N-TFT using channel doping method 4 and 5

	μ (cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}(x10^{-4} A)	I_{off}(x10^{-11} A)
Reference(NTFT)	106	1.25	0.72	2.79	4.19
N- doping	64	0.62	0.95	2.23	6.7
N-doping+annealing (550°C 1hour)	81	1.25	0.73	2.71	1.9

Table.5-7. Device parameters in homo type p channel poly Si TFT of different dopant concentration

Chapter 6

Gate oxide Effects outside channel

6.1. Introduction

Intensive study on poly-crystalline silicon thin film transistors with high mobility is underway in support of the competition to set the latest trend in high-definition, high speed and large area transistors. In addition to this research, next-generation technology is enabling the commercial use of organic light emitting diode (OLED) displays. Due to the high interest in OLED, the use of poly-crystalline thin film transistors will be necessary. In order to transfer a-Si to poly-silicon, a silicon thin film has to be heated to above 700 ºC to create a so-called Low Temperature Poly Silicon (LTPS), which is needed for a device on a common glass substrate. Laser scanning has been known as the most important LTPS process. However, laser annealing method has many problems, such as expensive cost, poor surface roughness in interface of Si and nonuniformity of the electrical performance. Solid phase crystallization process has lower cost than laser crystallization method. But crystallization temperature (>600ºC) in SPC is high for processing glass substrate.

In this aspect, metal induced lateral crystallization (MILC) method has advantages for other crystallizing method[1-5]. This process lowered crystallization temperature below 550ºC. The cost is not expensive for processing glass substrate. Although MILC TFT has high mobility, some problems remain. Channel is important in electrical characteristics. In our work, all process was applied in wafer substrate to find material problems. Source in leakage currents was confirmed.

6.2. Experiments

In wafer substrate, transistors with different three structures were fabricated. In no trench type1, a-1000Å Nitride was deposited on wafer. After Nitride deposition, 2000 Å MoW was deposited as gate metal. And source and drain region were patterned. To form source and drain, Ion mass doping was carried out. And activation annealing was done at 550º C for 2hours. In no trench type2, a-1000Å Nitride was deposited on wafer. After Nitride deposition, 2000 Å MoW was deposited as gate metal. Gate was patterned. And a-3000Å Nitride was deposited for forming isolation region. Active was patterned by using negative photo resistor and RIE etching. Contact hole was formed using contact hole mask. To form source and drain, Ion mass doping was carried out. And activation

annealing was done at 550º C for 2hours. In trench type, a-3000Å Nitride was deposited on wafer. Active was patterned. Etching method is not dry etching but wet etching to remain angle of inclination to be 45º. A-1000Å Nitride was deposited as gate insulator. After Nitride deposition, 2000 Å MoW was deposited as gate metal. Gate was patterned. To form source and drain, Ion mass doping was carried out. And activation annealing was done at 550º C for 2hours.

6.3. Results and Discussion

Fig6-4 and Fig6-5 show I-V curve in no trench type 1. Unlike poly Si TFT, this structure has no LDD. In off-state, there is no pinning phenomenon. In N-type and P-type TR, the electrical characteristics are better than that in poly Si TFT. In drain junction, there is no defect due to no grain boundary [6]. It is proof for explaining the leakage currents mechanism. And Slope is the best in single crystal TR. Channel material has effects on slope. Fig6-6 and Fig6-7 show I-V curve in No trench type2 and Trench type. Fig6-8 shows comparison with three structures of transistors. Main difference is I_{on} and slope in electrical properties. In No trench type 1, gate region was large and channel was formed beneath gate. In trench type, channel was not formed outside channel. Gate insulator was thick

(4000Å). It is difficult to form channel. But trench type1 and trench type2 is enough to form channel. Gate insulator thickness is 1000 Å

6.4. Summary

Depending on gate region, channel region was different. And outside channel, Nitride thickness is important to form channel. The more thick in Nitride thickness, the more difficult to apply field. If no trench type is applicable to poly Si TFT, it is expected to be high currents and fast switching speed.

6.5. References

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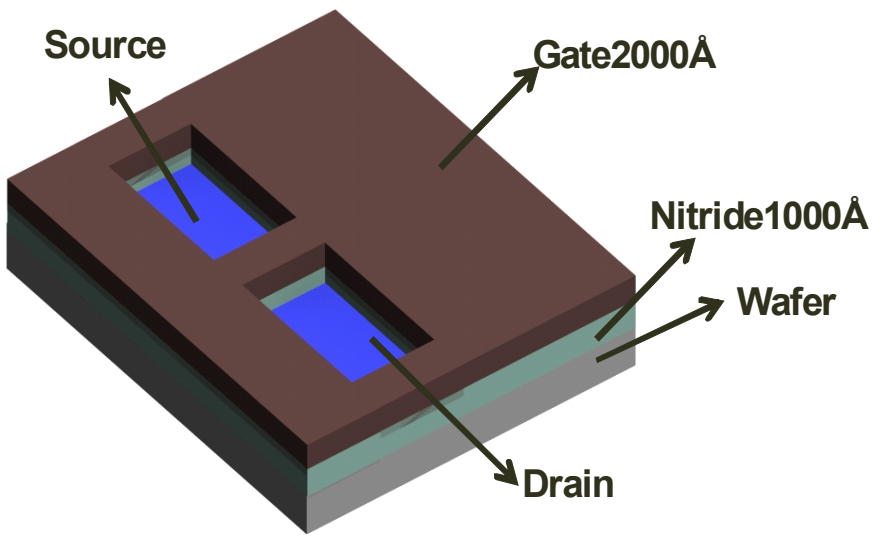

Fig.6-1. No trench type 1

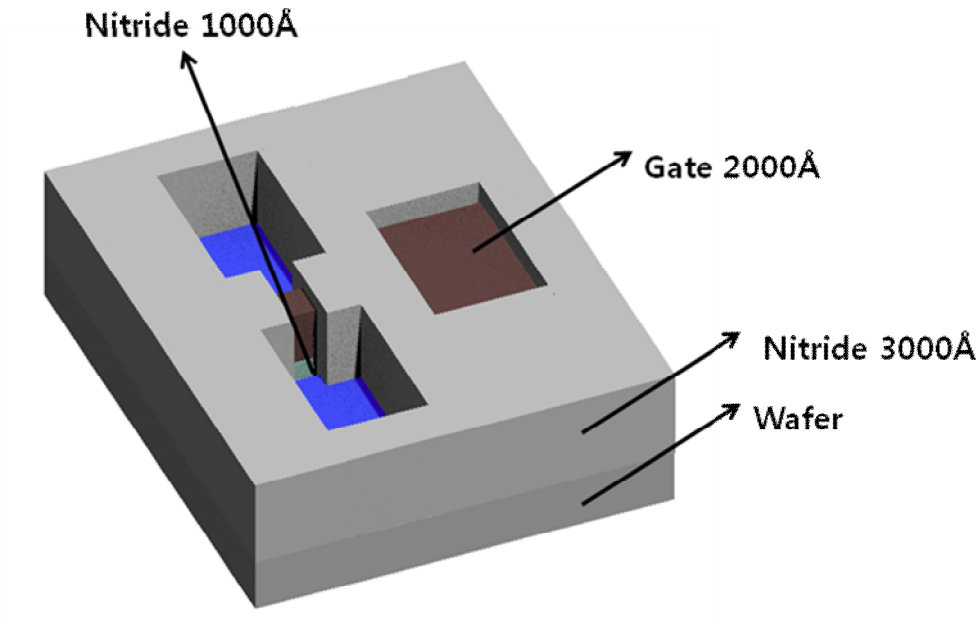

Fig.6-2. No trench type 2

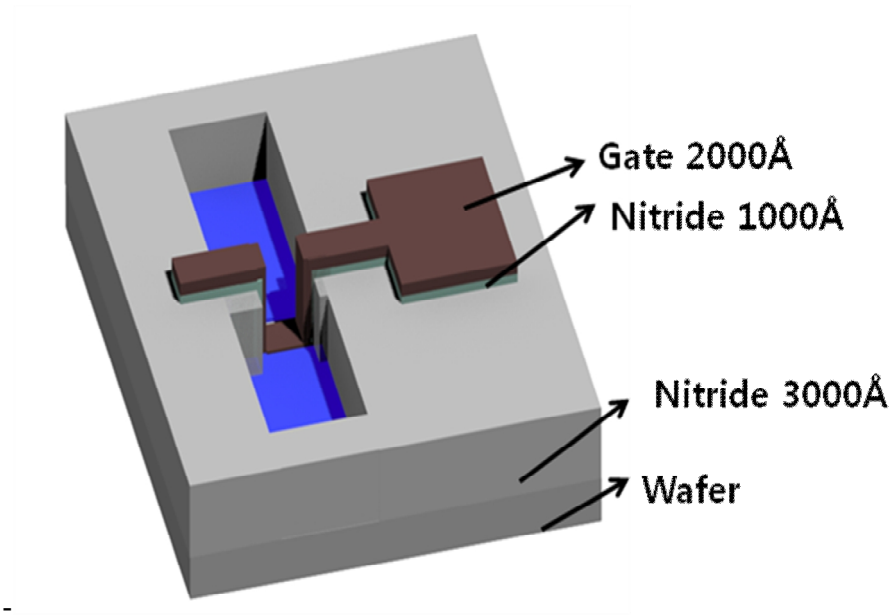

Fig.6-3. Trench type

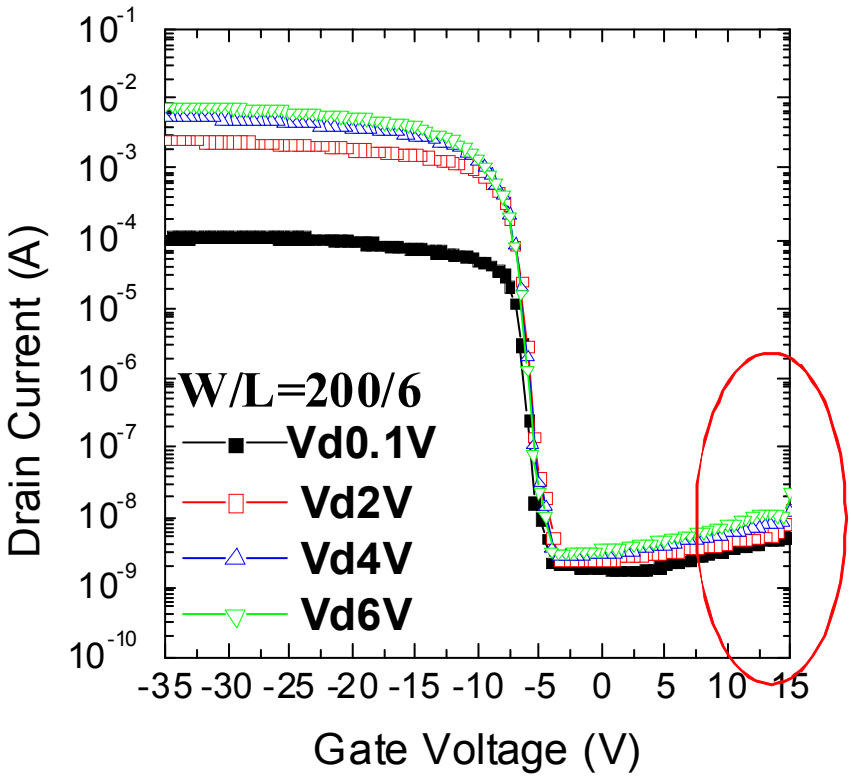

Fig.6-4. I-V curve in p-type TR of no trench type 1

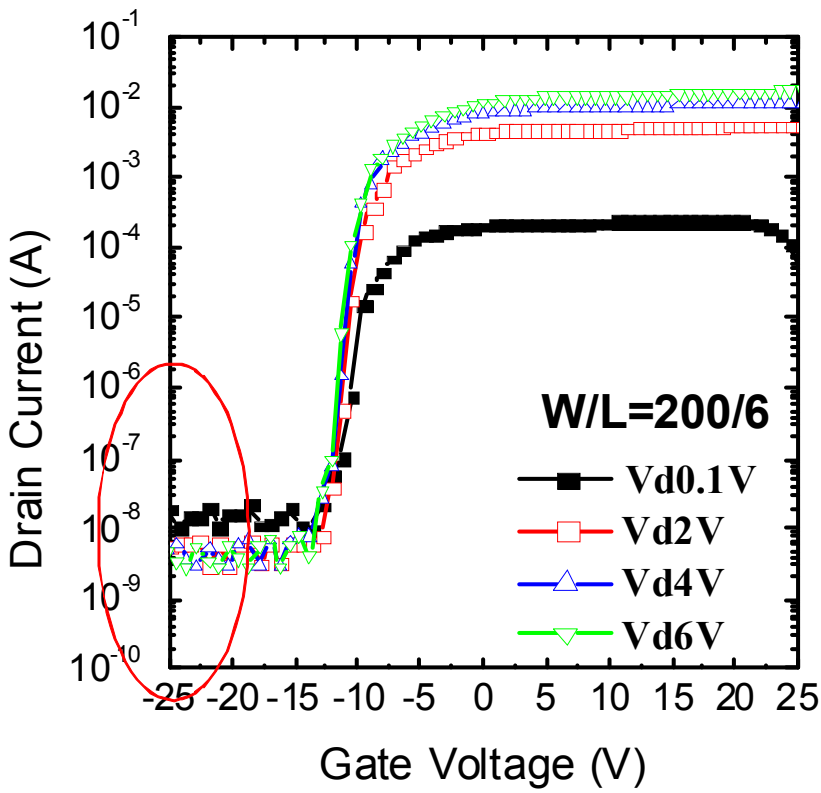

Fig.6-5.I-V curve in N-type TR of no trench type 1

	$\mu(cm^2/VS)$	V_{th} (V)	Slope(V/dec)	$I_{on}(x10^{-4} A)$	$I_{off}(x10^{-10} A)$
P-type	**5402**	**-5.5**	**0.44**	**80**	**30**
N-type	**19146**	**-11.3**	**0.59**	**100**	**20**

Table.6-1. Device parameters in no trench type 1.

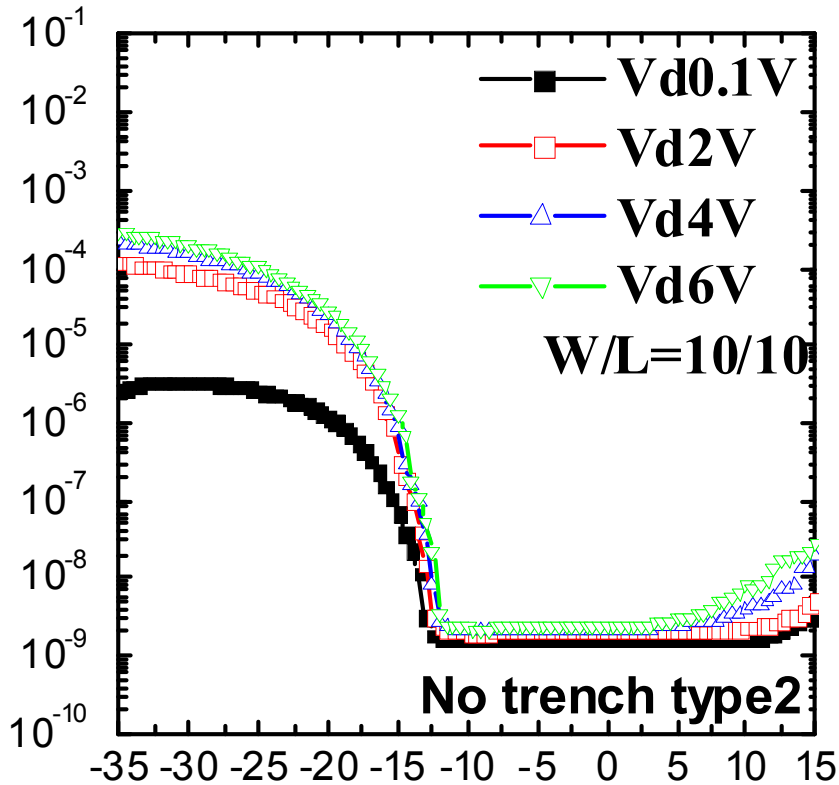

Fig.6-6. No trench type2

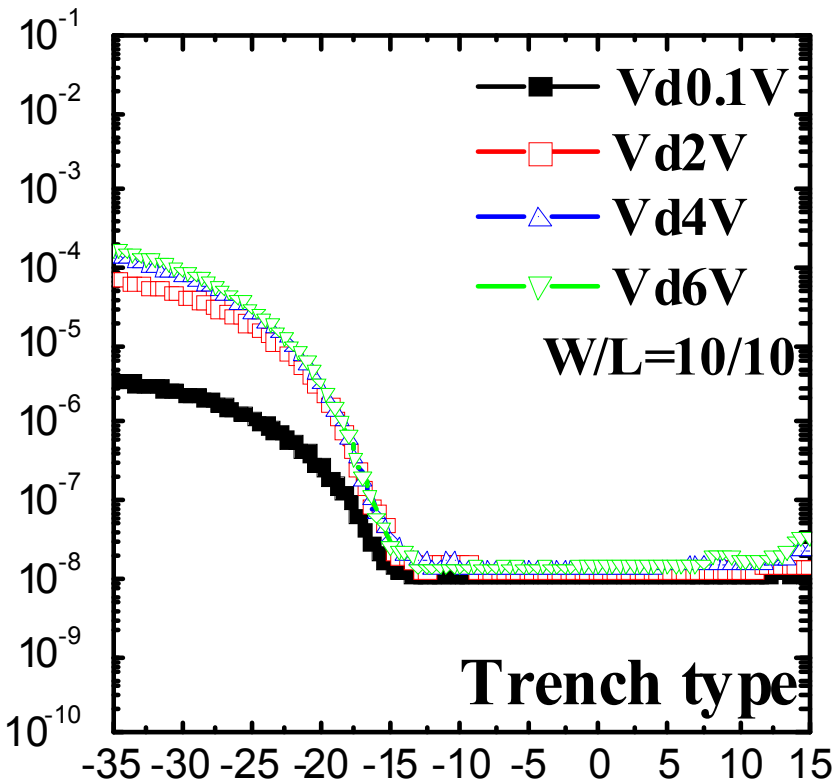

Fig.6-7.Trench type.

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	I_{on}($x10^{-4}$ A)	I_{off}($x10^{-10}$ A)
No Trench type2	**100**	**-15**	**0.9**	**2.8**	**23**
Trench type	**81**	**-18.5**	**1.9**	**1.79**	**138**

Table6-2. Device parameters in no trench type 2 and Trench type.

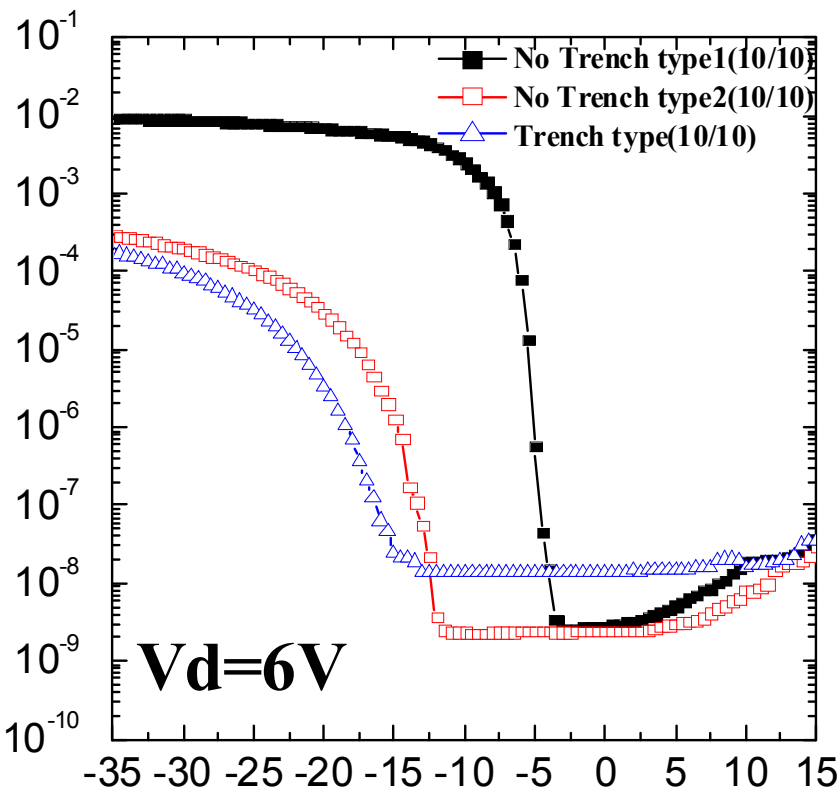

Fig.6-8.Comparison with three structures of transistors.

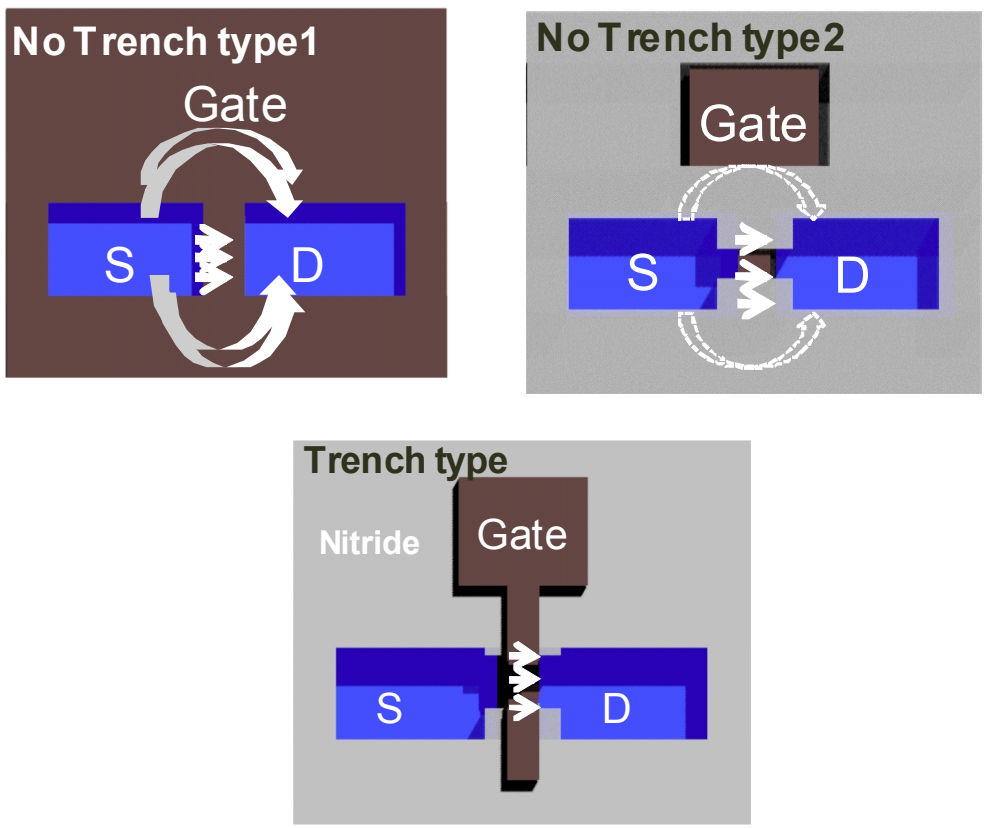

Fig.6-9. Currents flow in different structure.

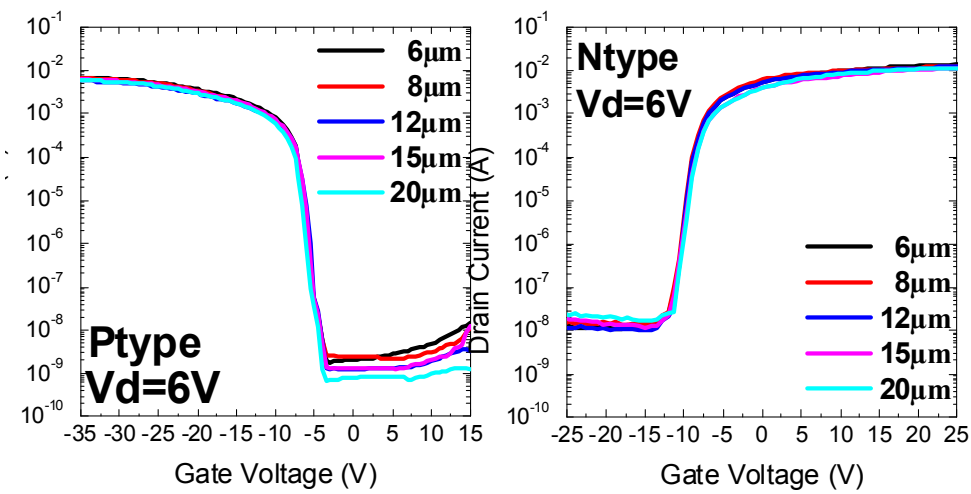

Fig.6-10. Length effects in No trench type1

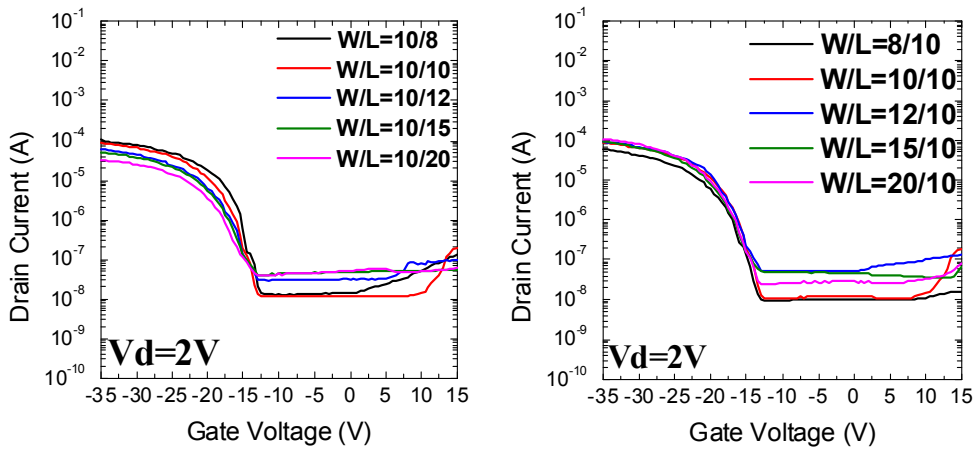

Fig.6-11 length and width effect in No trench type2

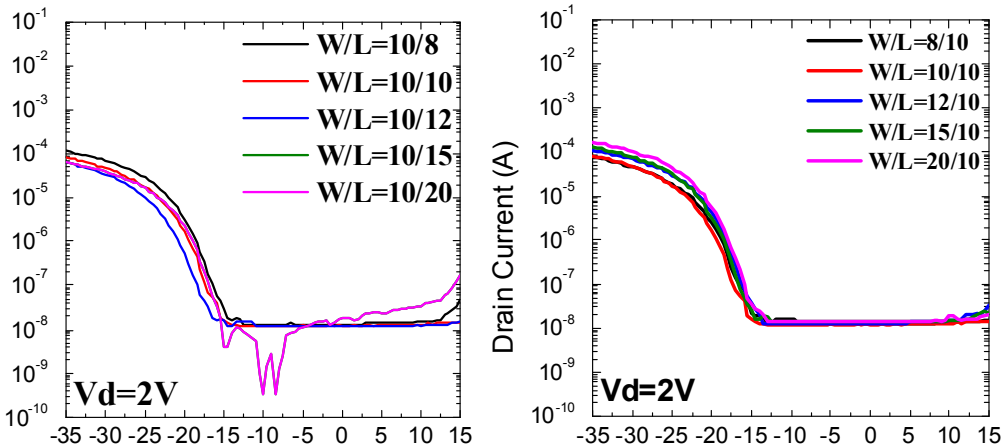

Fig.6-12. length and width effect in trench type.

Chapter 7

Mechanical stress

7.1. Introduction

Recently display market has interests on flexible electronics due to the potential. Researches related to flexible electronics are based on amorphous silicon thin film transistor (a-Si: H TFT) technology. However, it is necessary to research polycrystalline silicon thin film transistor (poly-Si TFT) technology since it offers higher mobility and lower driving voltage. To apply for flexible display, Poly Si TFT can be used for both switching transistor and driving transistor. For various applicable electronics, Poly Si TFT has different level of strain. In this reason, it is important to understand electrical characteristics and operational range of poly-Si TFTs under mechanical stress.

In poly Si TFT, there are three methods to apply stress in flexible substrate. 1. Direct fabrication of poly Si TFT on plastic substrate [1]. 2. Fabrication of poly Si TFT on stainless steel [2]. 3. Transfer process [3-4]. For each method, advantage and the problem are as follows

	advantage	disadvantage
1. direct fabrication[1]	Low temperature process	Poor gate insulator
2. fabrication on stainless steel[2]	High temperature process	Roughness, adhesion
3. transfer process[3]	High temperature process	Handling, extra cost

Glass thinning method is suitable for low temperature process (>500ºC) of poly Si TFT. In this work, we adopt for method thinning glass and investigate stress effects on poly Si TFT.

7.2. Experiments

A-3000 Å thick SiO2 thin film was deposited as a buffer layer by plasma enhanced chemical vapor deposition (PECVD). A-1000 Å thick a-Si thin film was deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C using SiH4 as the precursor. Active region was patterned. On top of active area of Si, Ni mask pattern was formed and Ni sputtering was done. By lift-off process, Ni remains on source and drain(S/D). After lift-off process, Ni was removed by H_2SO_4. After Ni removal process, annealing of MILC (metal induced lateral crystallization) was carried out at 550ºC for 2hours in H_2 ambient. A-1000 Å thick SiNx film was deposited as a gate insulator and 2000 Å thick MoW film was deposited as a gate

electrode by PECVD and sputtering, respectively. After gate electrode definition, lightly doped drain (LDD) region was formed using additional mask. To form source and drain(S/D) region, Ion Mass Doping (IMD) was done. The dopant gases used were PH3 for n-type and B2H6 for P-type. To activate dopant, annealing was processed in H2 ambient at 550 ºC for 2 h. Our etching process sequence is schematically illustrated in Fig7-1

After fabrication of TFTs, A-200μm film was attached, with insertion of a paper between film and the TFT surface. The paper was placed over measuring TFT region to detach the film easily. The glass substrate was etched by three steps etching method. The three steps are following as. After etching process, A-200μm film was attached to backside of glass. To expose measuring TFT region, film and paper were removed using cutting equipment. A-110 μm glass substrate was fabricated successfully. Figure7-2 shows A- 110 μm thick glass. To apply mechanical stress, medium thick glass was used. We use stretching equipment to apply tensile stress. Fig7-3 shows stretching equipments. We investigated the electrical characteristics of poly Si TFT applying tensile stress. The Stress has two types. One is parallel to channel. The other is vertical to channel.

7.3. Results and Discussion

Figure7-4 shows tensile stress effects on I_{on} in N channel poly-Si TFTs. The I_{on} current under uniaxial tensile stress is constant, for stress parallel to the channel. The I_{on} current under uniaxial tensile stress decreases, for stress vertical to the channel. Fig7-5 explains for mechanism of mobility change under tensile stress direction [5]. The I_{on} current under uniaxial tensile stress is constant, for stress parallel to the channel. The I_{on} current under uniaxial tensile stress increases, for stress vertical to the channel. Unlike N channel poly Si TFTs, mobility in vertical direction also was not degraded. In our work, grain size is not 0.3μm. Unlike SLS crystallization method, our crystallization method is MILC (metal induced lateral crystallization) [7]. So it is impossible to apply for our data to Mosfet theory completely. And our TFT has LDD structure. Asymmetrically stress was loaded in drain region. To apply tensile stress stretching the substrate is different from bending substrate.

Fig7-6 and Fig7-7 shows electron mobility change in different tensile stress. Fig7-8 and Fig7-9 shows hole mobility change in different tensile stress. In N channel poly Si TFTs, mobility change was explained easily. But mobility variation of p-channel poly Si TFTs has different tendencies. As mentioned before, our system is different. (Crystallization method (MILC) [7], grain size<

0.3μm [7] , Method for applying stress, LDD structure [6-8]). Particularly, our TFT has LDD structure. In Drain region, asymmetry stress was loaded. In reference 7, additional Oxide layer has effects on stress distribution. Our TFT suffers from asymmetry stress. Fig7-10 and Fig7-11 show leakage current of poly Si TFT under tensile stress. In N channel poly Si TFTs, the minimum leakage current is constant under tensile stress. Fig7-12 and Fig7-13 show leakage current of P channel poly Si TFT under tensile stress. In p channel poly Si TFTs, the minimum leakage current is constant under tensile stress. But pinning phenomenon in P channel poly Si TFT was degraded. In our doping systems, boron doping was more heavily doped than phosphorous doping. At the same thickness of a-1000Å Nitride, p channel TFT has pinning phenomenon. This is not enough for forming LDD (lightly doped drain) region in p channel TFT using a-1000Å Nitride layer. Our LDD structure has not symmetry. More stresses were loaded in drain region. In this reason, the leakage currents of the p channel TFT increase. Fig7-14 and Fig7-15 show change of slope in N channel TFT and P channel TFT. The subthreshold slope of both types of Poly Si is constant. Fig7-16 and Fig7-17 show change of threshold voltage (V_{th}) in N channel TFT and P channel TFT.

Fig7-18 shows I-V curve in P channel TFT and N channel TFT under tensile

stress. In N TFT channel, V_{th} decrease. And in P channel TFT, V_{th} increase. The breakage of weak Si-Si bonds during mechanical strain lead to creation of the dangling bonds and defect traps [8]. The Characteristics of generated defects in MILC TFT have negative charge. Fig7-19 show I-V curve in p channel TFT and N channel TFT after H_2 annealing. Hydrogen annealing was carried at 550ºC for 2hours. Vth shift means defects combine with hydrogen.

7.4. Summary

We investigate tensile stress effects on the performance of the Poly Si TFT. Main phenomenon is change in mobility and leakage current. The generated defects cause Vth shift. Defects related to dangling bond and defect traps. The hole mobility was enhanced regardless of stress direction. But electron mobility was enhanced under stress parallel to channel. In stress of the vertical direction, mobility was degraded. In different width and length, the electrical characteristics of poly Si TFT were investigated.

7.5. References

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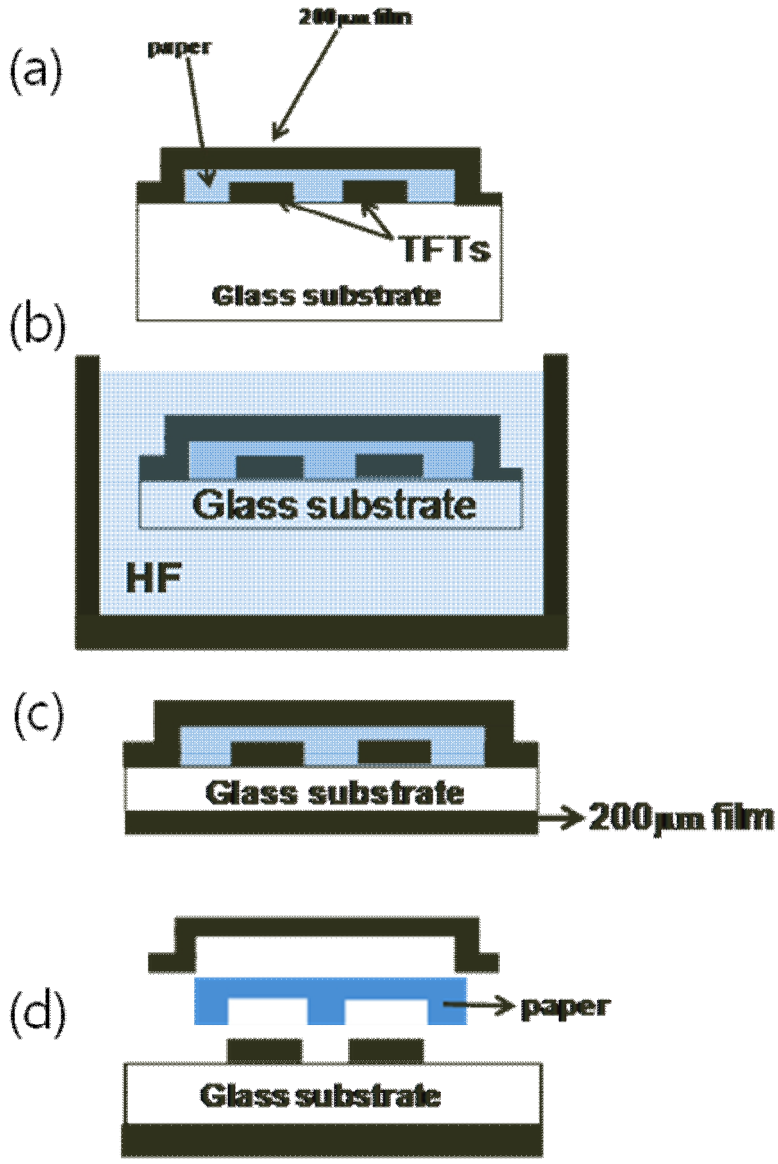

Fig7-1.Our etching process sequence. Ref [4].

Step	concentration	Time
1	49% (HF)	50min
2	1:1.5 (H_2O:HF)	20min
3	5:1 (H_2O:HF)	30min

Table.7-1. Glass thinning condition.

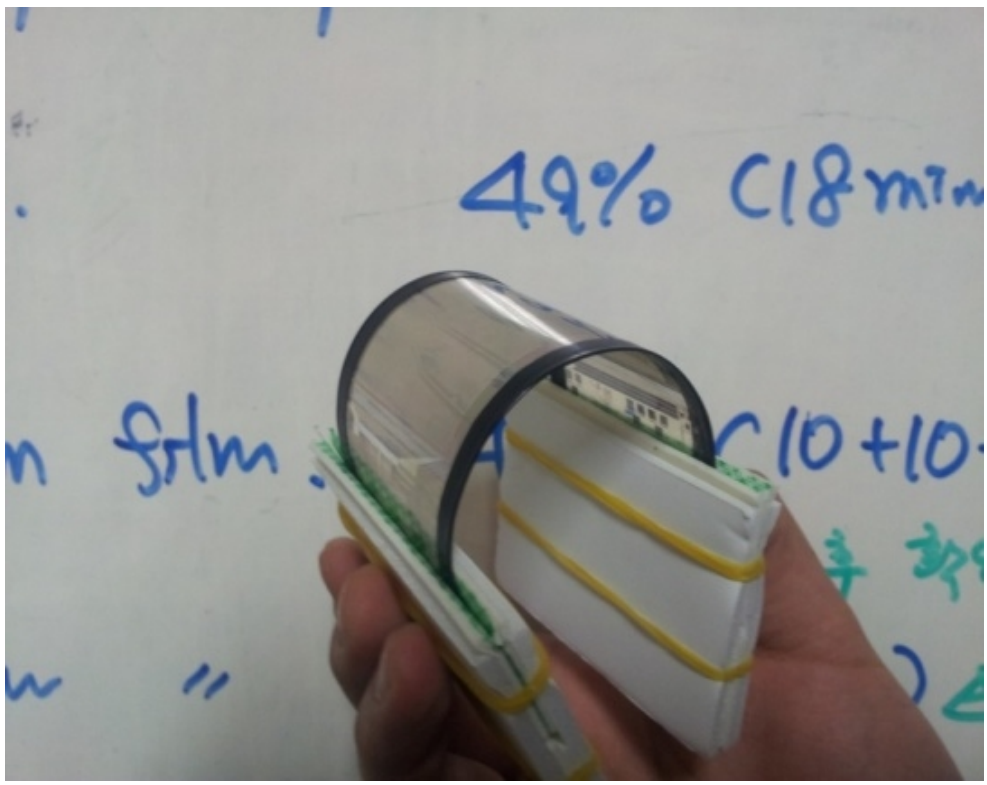

Fig.7-2. A-100 μm thick glass.

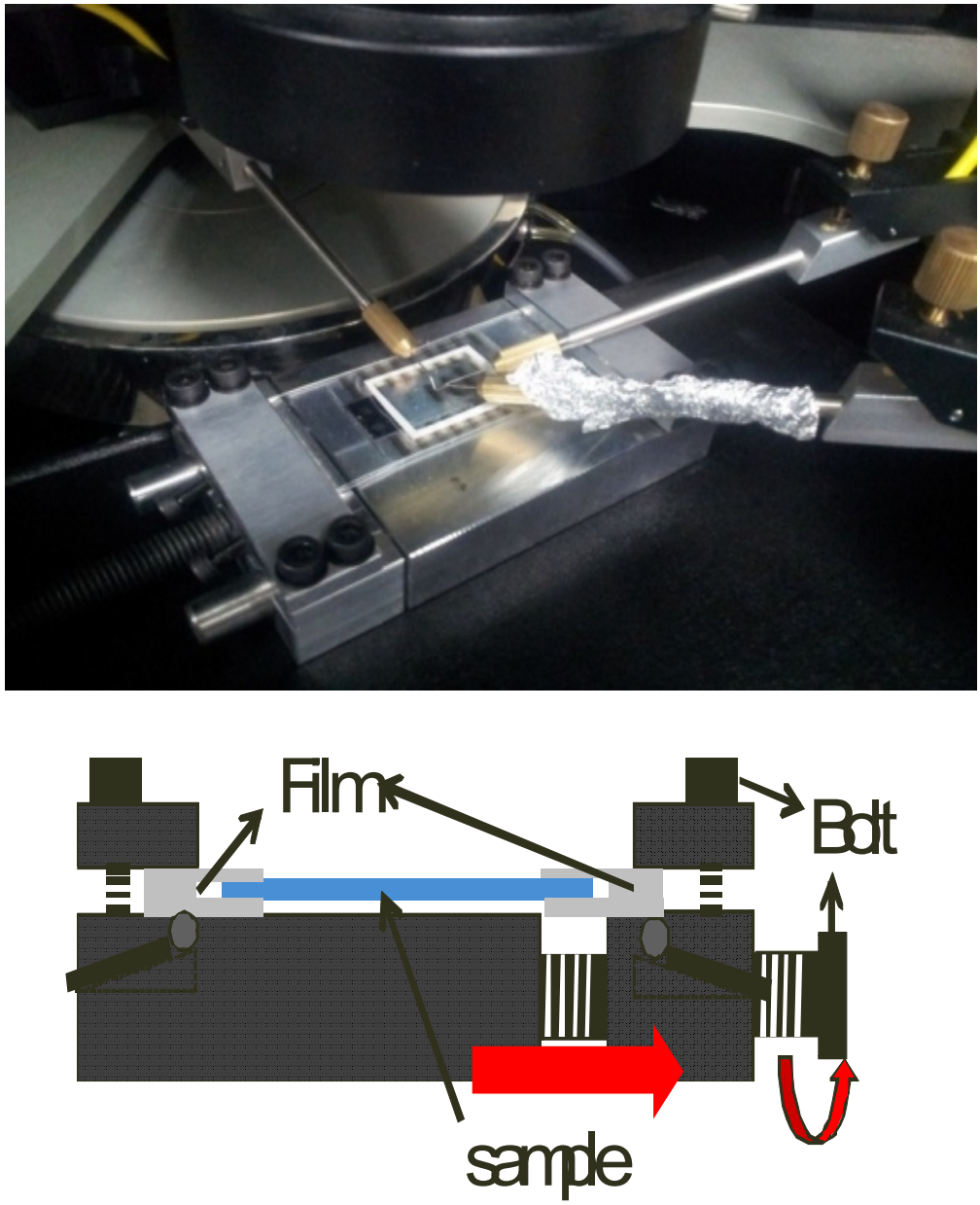

Fig.7-3. Stretching equipment

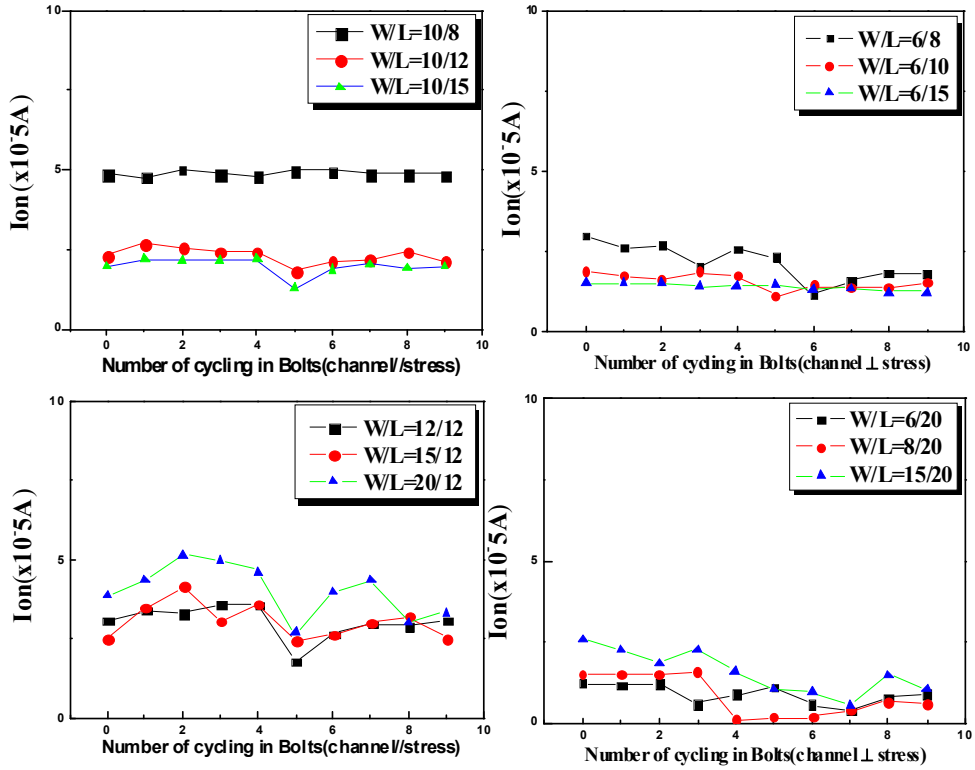

Fig.7-4. I_{on} currents variation of N channel poly Si TFTs under uniaxial tensile stress.

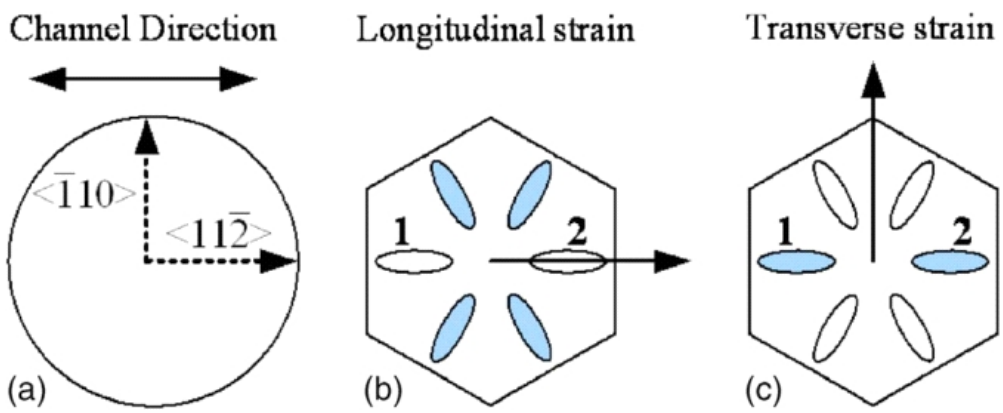

Fig.7-5. (a) Two type channel direction of (111)-oriented Si. The projection of constant-energy contour of (111) Si conduction band under (b)Parallel strain and (c) vertical strain. Ref [5]

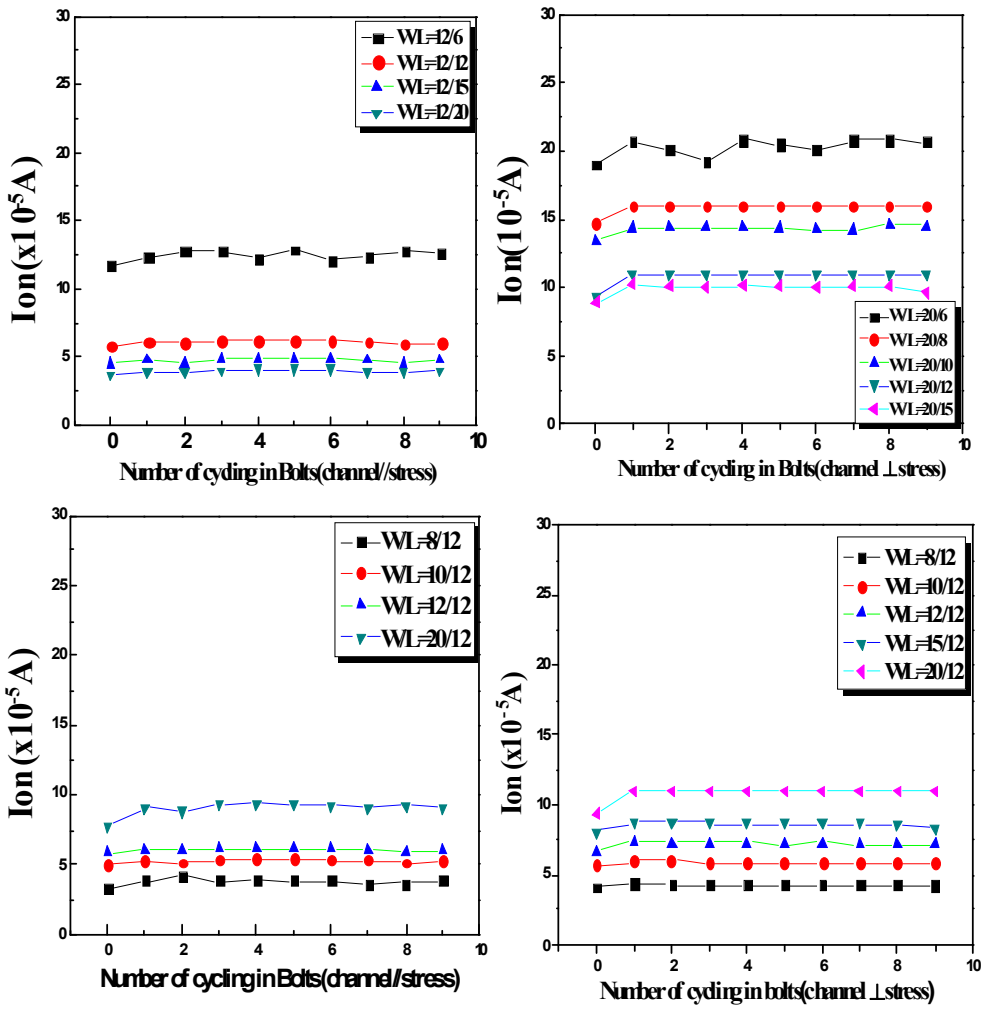

Fig.7-6. Ion currents variation of N-channel poly Si TFTs

under uniaxial tensile stress.

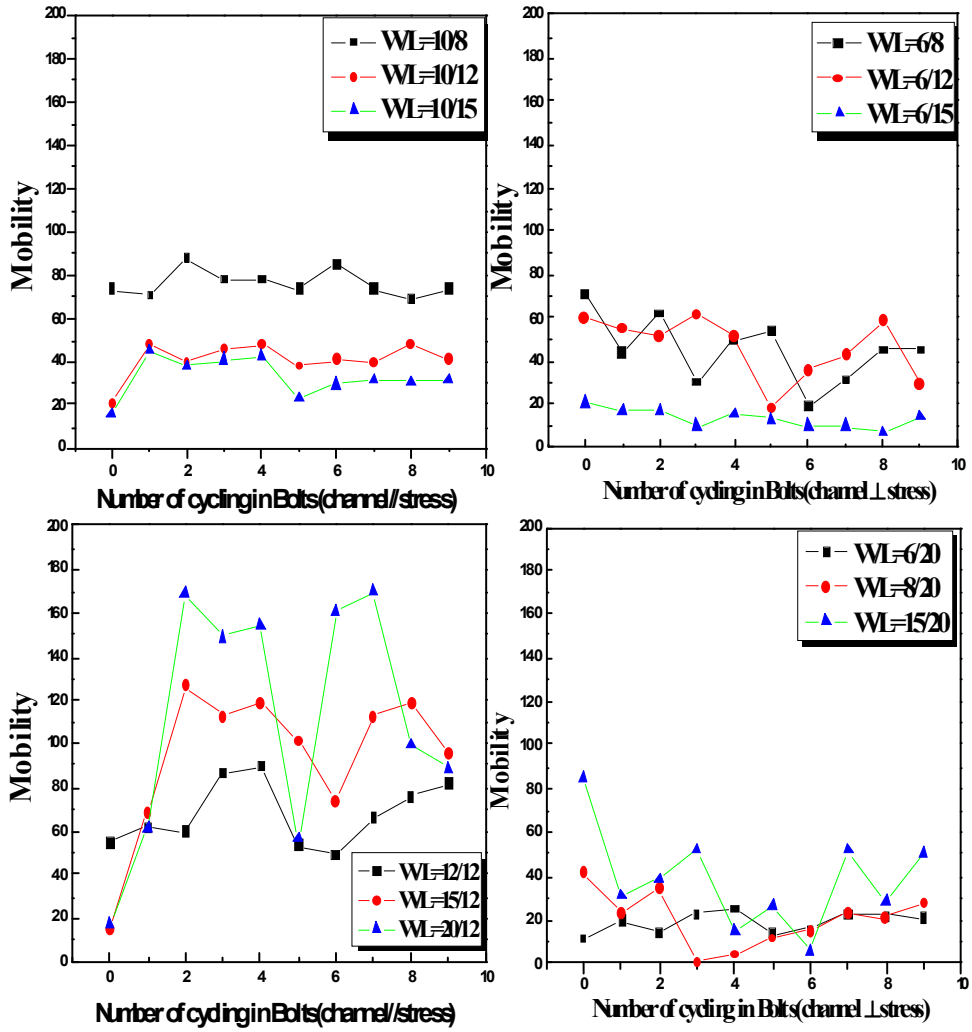

Fig.7-7. tensile stress effects on Mobility in N-TFT.

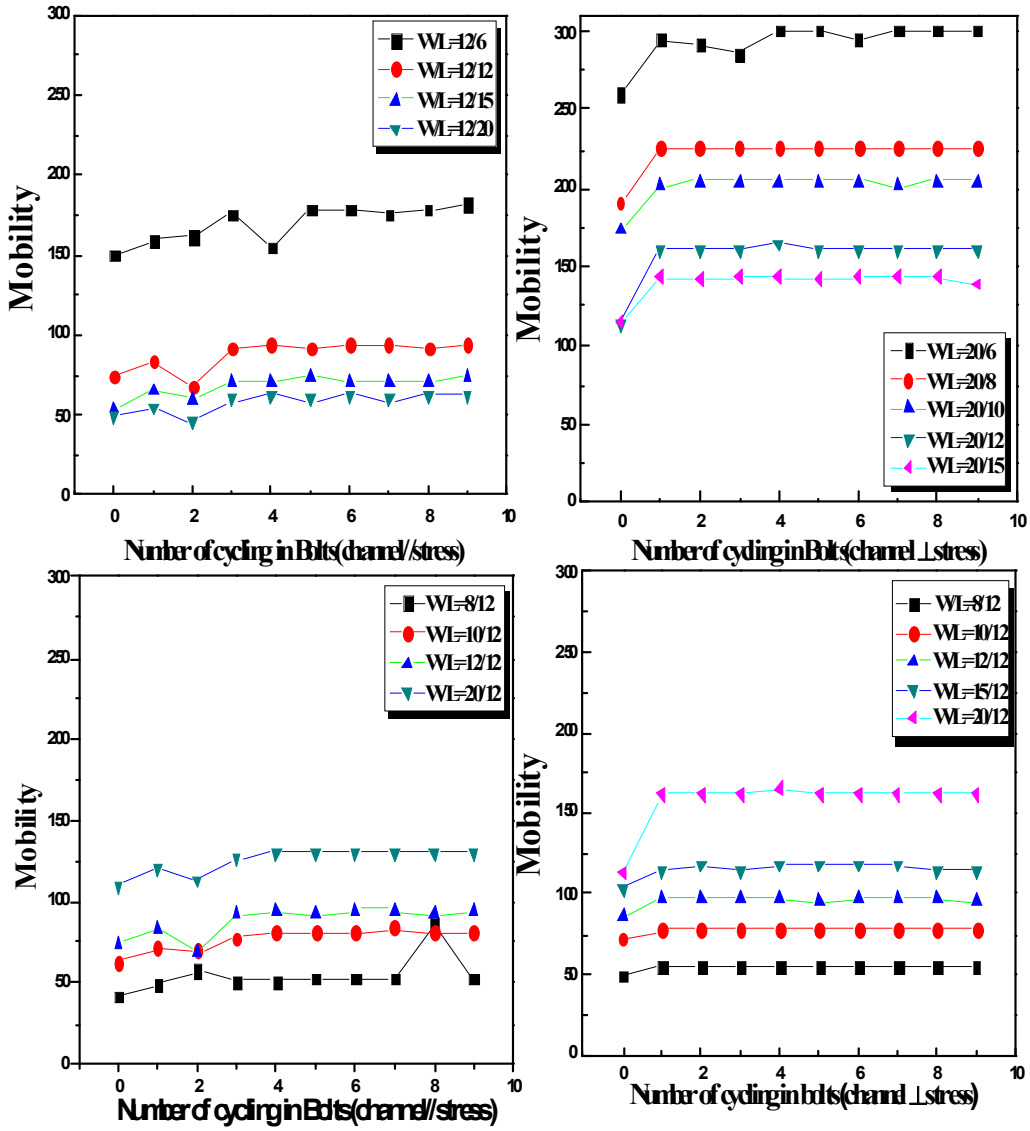

Fig.7-8. tensile stress effects on Mobility in P-TFT.

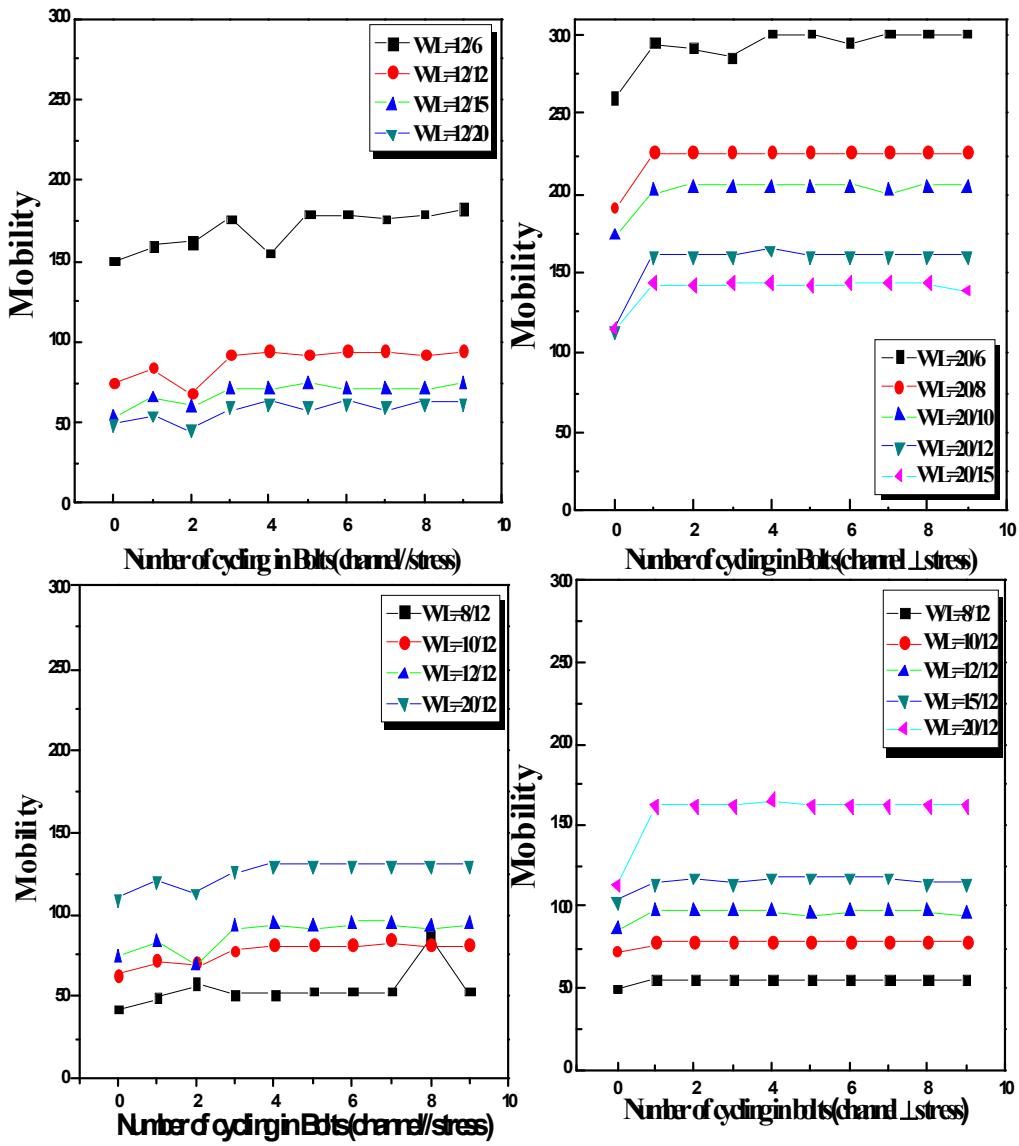

Fig.7-9. tensile stress effects on Mobility in P-TFT

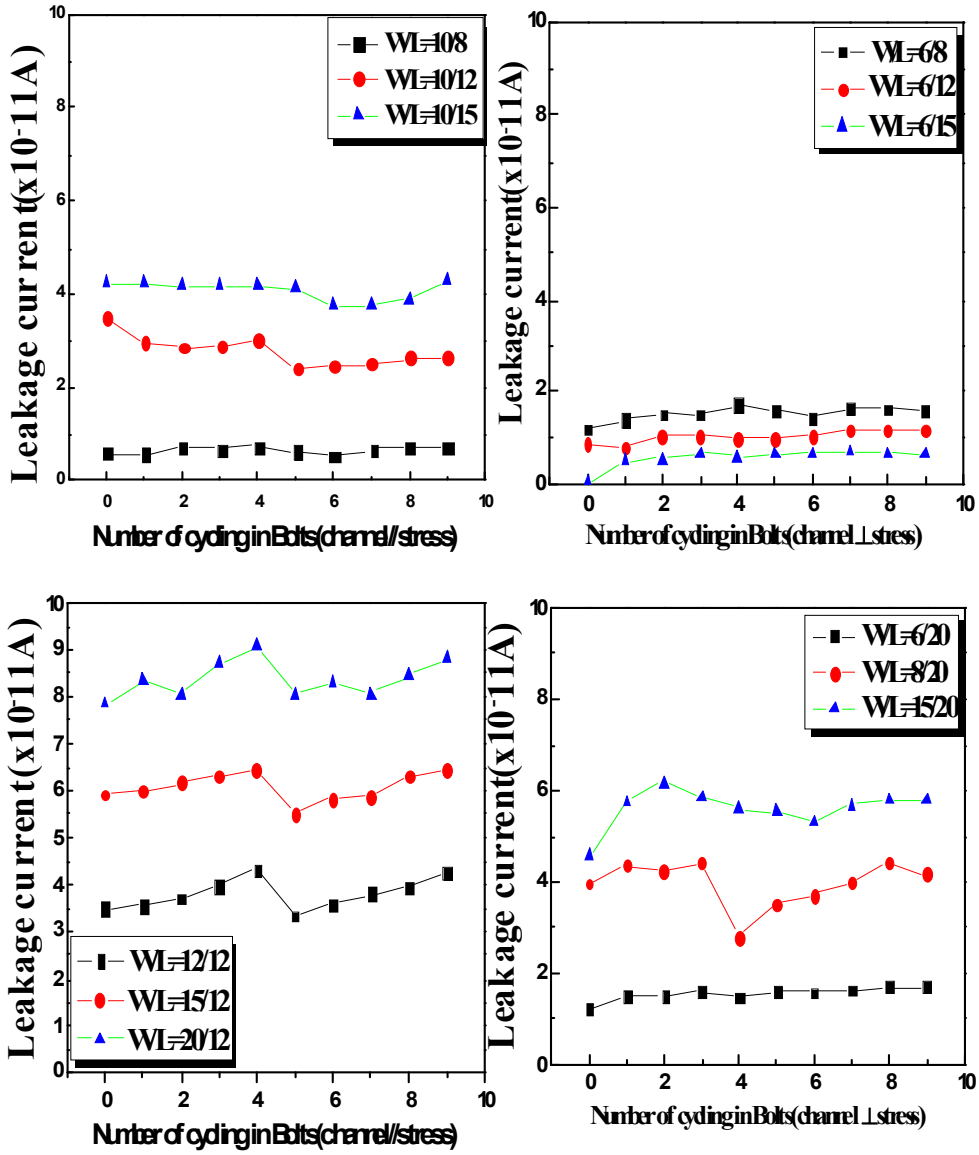

Fig.7-10. tensile stress effects on minimum leakage current in N-TFT

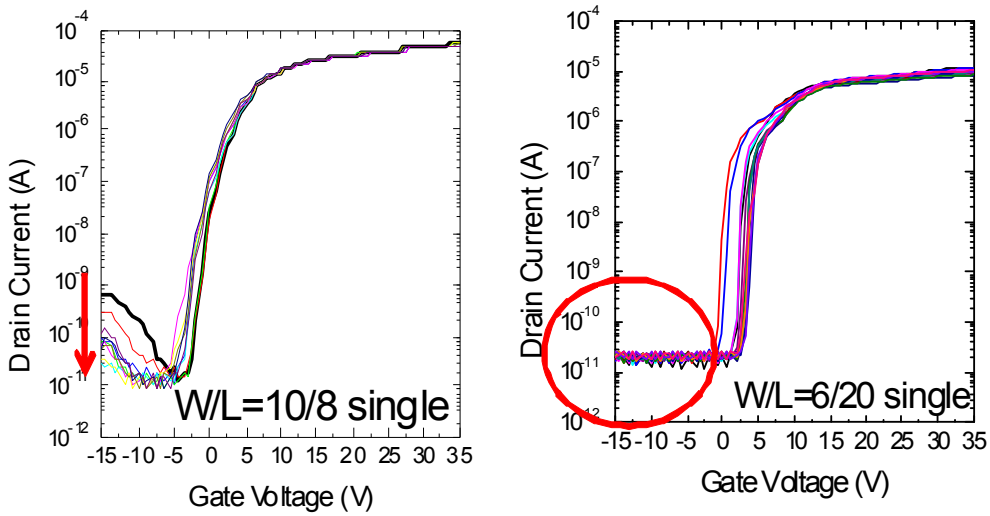

Fig.7-11. I-V curve in N-type poly Si TFTs

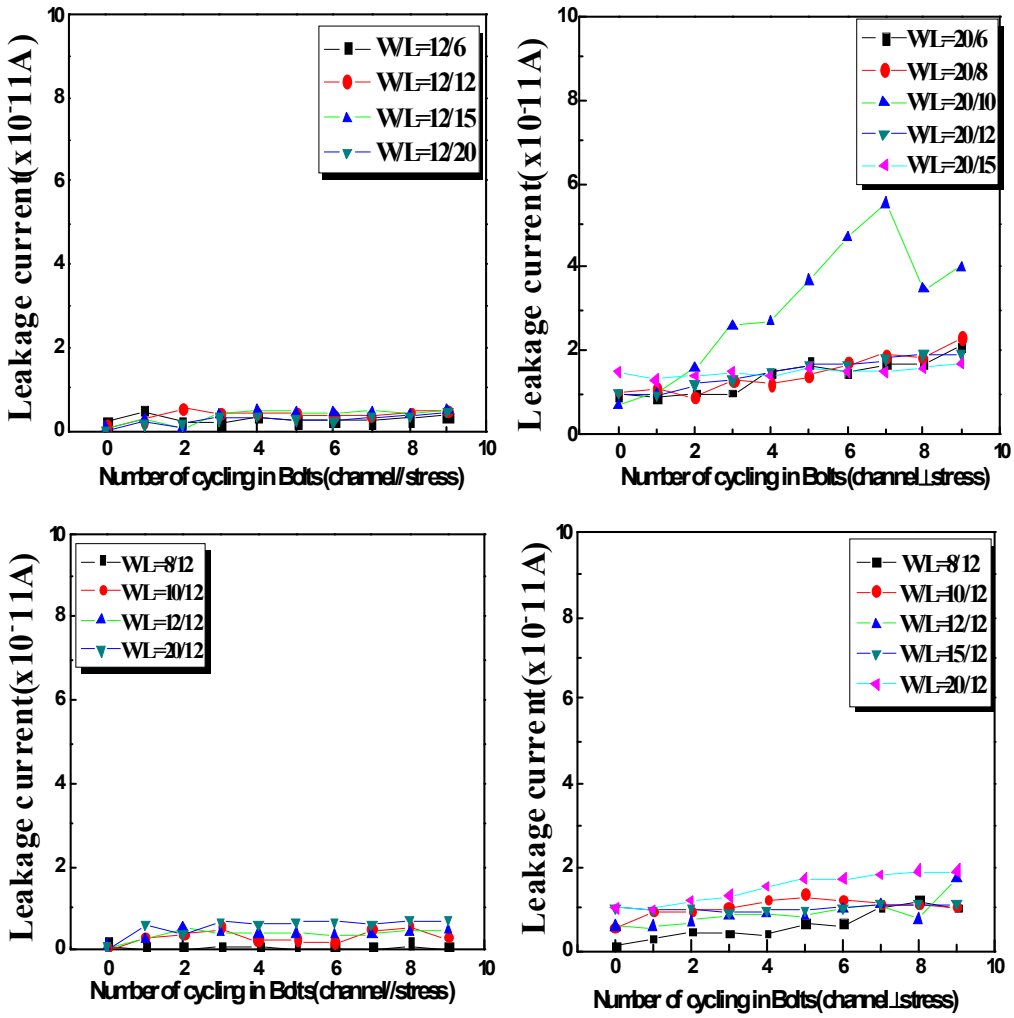

Fig.7-12. tensile stress effects on minimum leakage current in P-TFT

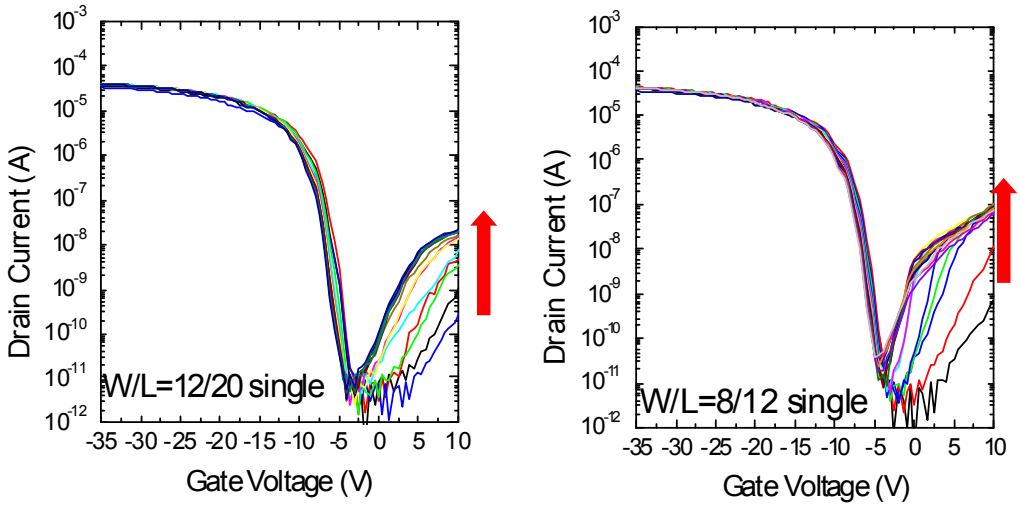

Fig.7-13. I-V curve in P-type poly Si TFTs

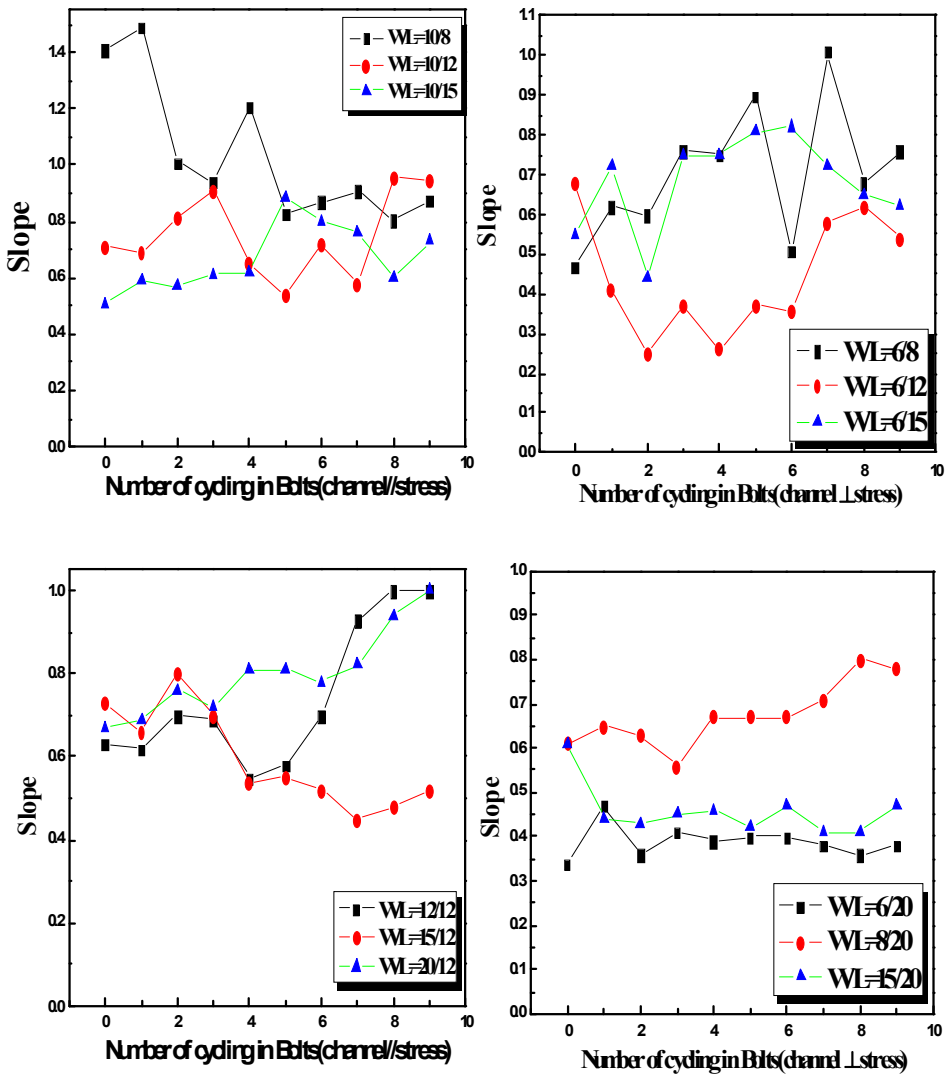

Fig.7-14. tensile stress effects on Slope in N-TFT.

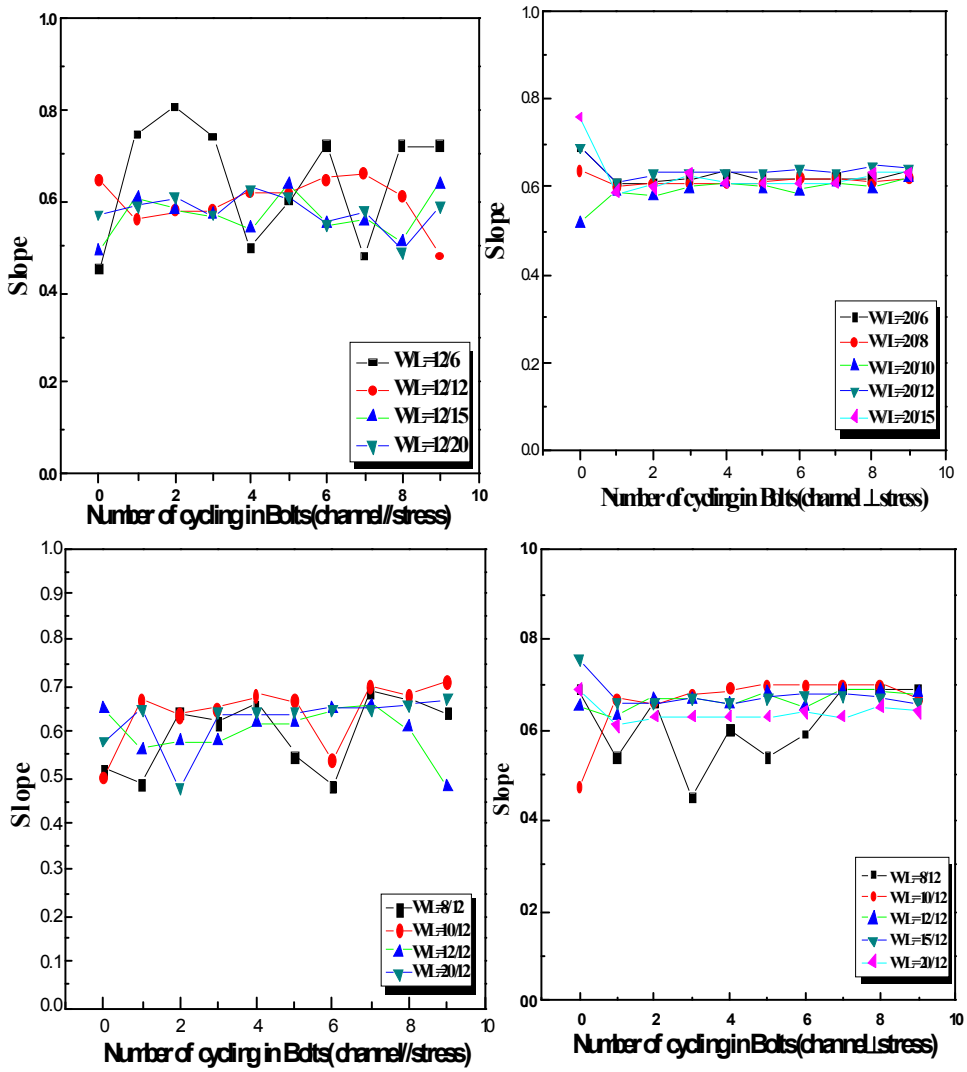

Fig.7-15 tensile stress effects on Slope in P-TFT

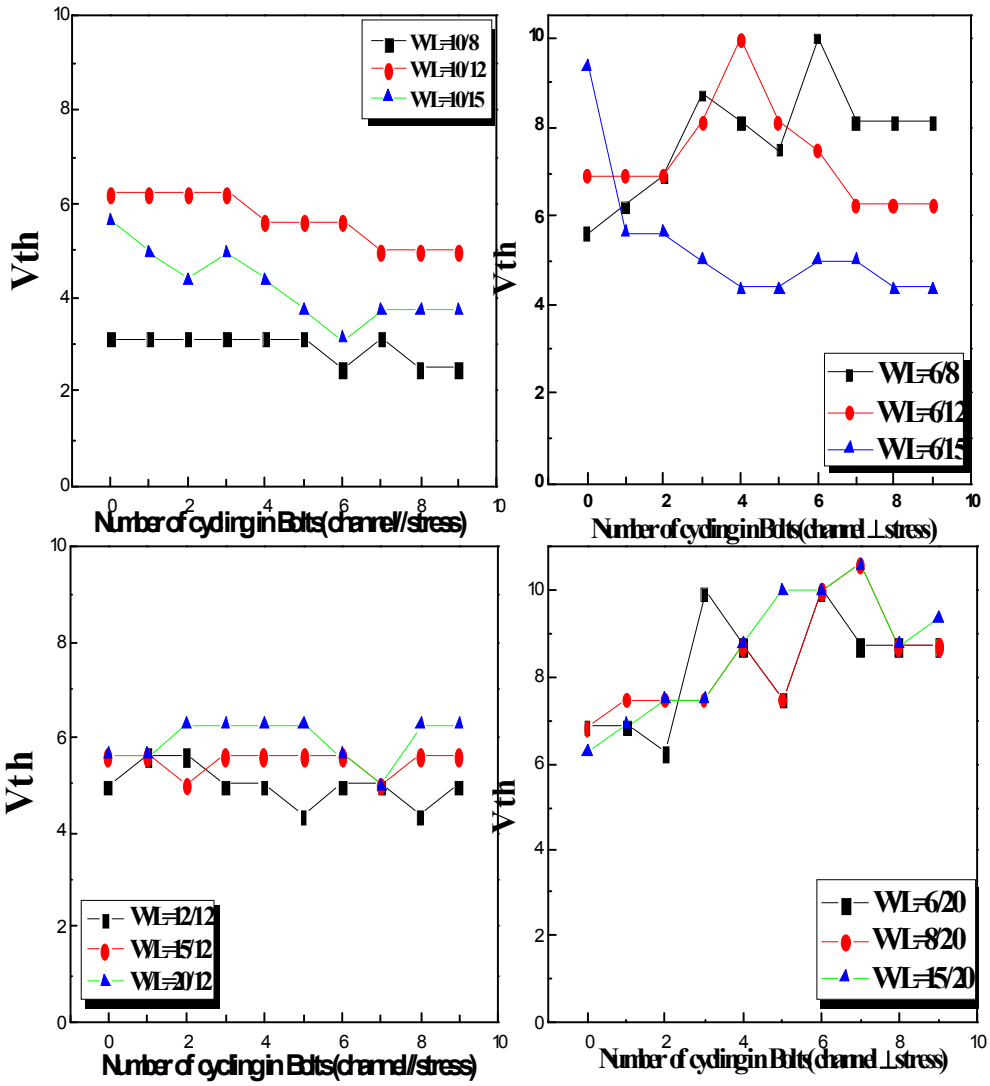

Fig.7-16. Tensile stress effects on V_{th} in N-TFT

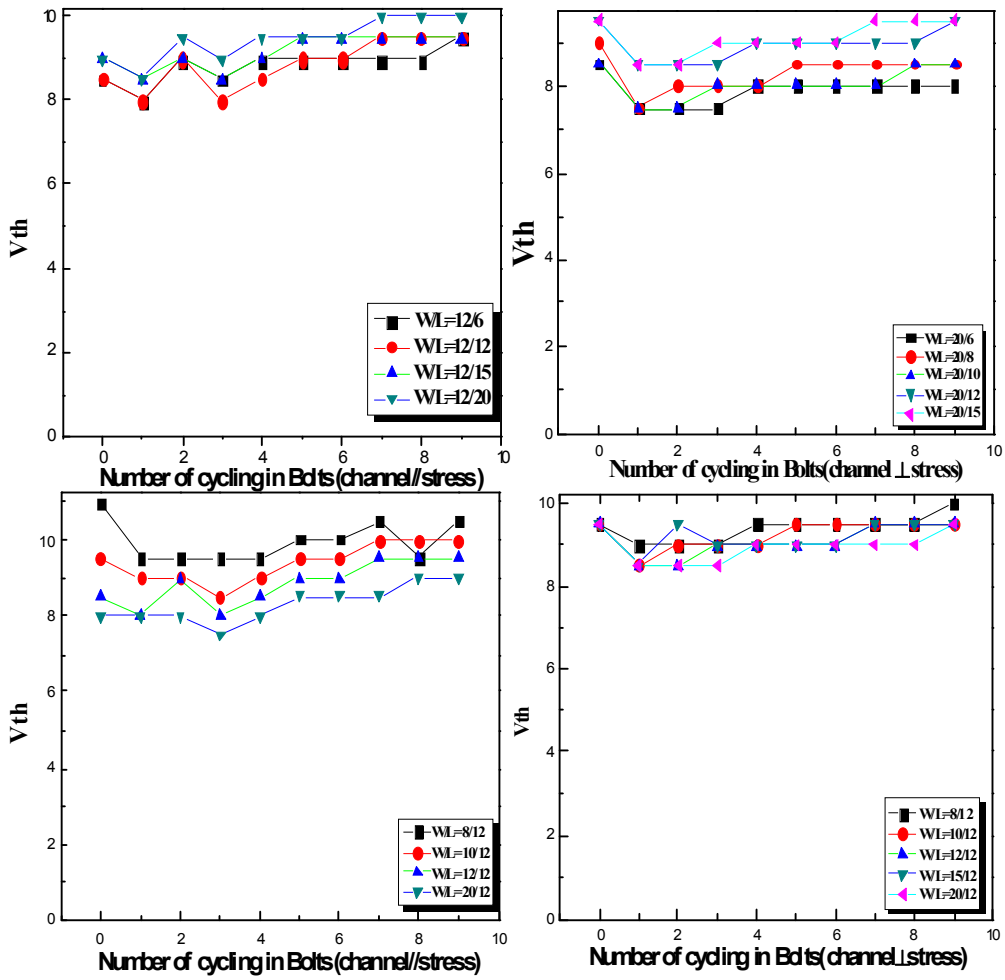

Fig.7-17. Tensile stress effects on V_{th} in P-TFT.

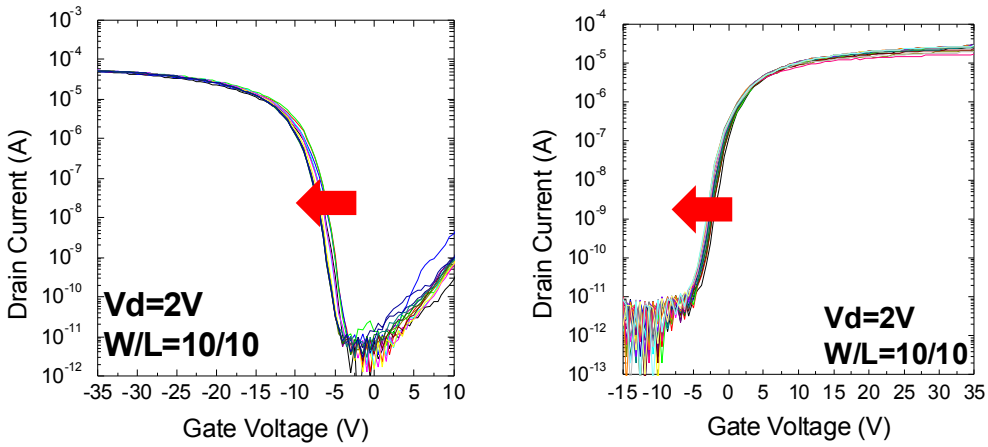

Fig.7-18. I-V curve in P channel TFT and N channel TFT

under tensile stress.

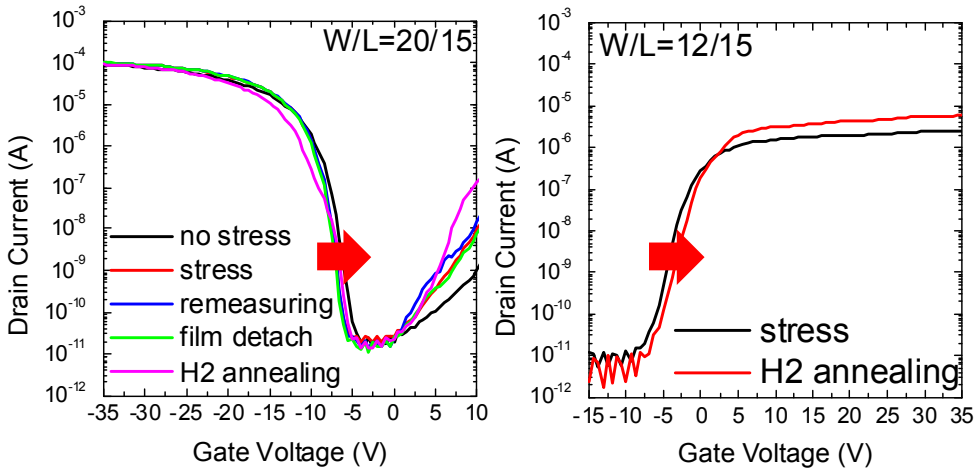

Fig.7-19. After H_2 annealing, I-V curve recovers to original status's direction

Chapter 8

Thermal stress

8.1. Introduction

Recently display market was moved from active-matrix liquid crystal display (AMLCD) to active-matrix organic light-emitting diodes (AMOLEDs) due to low driving voltage, large viewing angle, high definition, fast response time. Due to low mobility a-Si TFTs are not suitable for driving TFTs in AMOLED. The Polycrystalline silicon (Poly-Si) TFTs having high mobility are suitable for AMOLED. A-Si thin film can be crystallized by many kinds of methods, such as solid phase crystallization (SPC), direct deposition, rapid thermal annealing (RTA), liquid phase re-crystallization,

excimer laser annealing (ELA) and so on. Among the various crystallization methods, ELA method is much more preferable for fabricating low temperature poly-Si TFTs on a glass substrate. However, it still has many unsolved problems, such as uniformity and manufacturing cost. Another crystallizing method is MILC (metal induced later crystallization). The crystallizing temperature in MILC was more lowered than solid phase crystallization temperature. MILC process is low temperature process (>500 ºC) [1-4]. In this point, it is necessary

to understand thermal stress effects in MILC process. In MILC process, compaction process is necessary for preventing glass shrinkage. In our work, the characteristics of poly Si TFT in different substrate (bare glass, compacted glass, wafer substrate) were investigated.

8.2. Experiments

Different substrates (bare glass, compacted glass, wafer substrate) were used for poly Si TFT. Figure8-1 shows compaction process. A-3000 Å thick SiO2 thin film was deposited as a buffer layer by plasma enhanced chemical vapor deposition (PECVD). A-1000 Å thick a-Si thin film was deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C using SiH4 as the precursor. Active region was patterned. On top of active area of Si, Ni mask pattern was formed and Ni sputtering was done. By lift-off process, Ni remains on source and drain(S/D). After lift-off process, Ni was removed by H_2SO_4. After Ni removal process, annealing of MILC (metal induced lateral crystallization) was carried out at 550℃ for 2hours in H_2 ambient. Figure8-2 shows misalignment in different substrate. Wafer and compacted glass has no shrinkage problem. But the shrinkage was generated in bare glass. Table8-1 shows gate insulator condition. A-1000 Å thick SiNx film was deposited as a

gate insulator and 2000 Å thick MoW film was deposited as a gate electrode by PECVD and sputtering, respectively. After gate electrode definition, lightly doped drain (LDD) region was formed using additional mask. To form source and drain(S/D) region, Ion Mass Doping (IMD) was done. The dopant gases used were PH3 for n-type and B2H6 for P-type. To activate dopant, annealing was processed in H2 ambient at 550 ℃ for 2 h.

8.3. Results and Discussion

Fig8-3 shows I-V curve in different substrate. GI 1 condition was used. There is no difference in electrical performance between compaction and no compaction case. In wafer substrate, I_{on} current is high and I_{off} current is low. The subthreshold slope in poly Si TFT fabricated on wafer is high. If we assume TFT on wafer substrate has no stress, there are no effects in stress reduction of the compaction substrate. Compressive stress improved slope.

Fig8-4 shows N-type I-V curve in different substrate. In the case of N type, GI 1 condition was used. The more in the stress, the higher in the leakage currents. In this case, stress wasn't related to I_{on}, slope and V_{th}. Under light, measuring was done.

Fig8-5 shows I-V curve of wafer substrate depending on gate insulator (GI)

deposition condition. In nitride deposition condition, Silane flow reduces from 25sccm to 15sccm (GI condition 1: 25sccm, GI condition 2: 15sccm). In wafer, Vth more increases by 5volts than that in GI condition 1. In gate insulator condition3, slope is obviously improved. If the working pressure increase from 300mTorr (GI2) to 450mTorr (GI3), the quality in gate insulator is improved due to lower slope.

Fig8-6 shows I-V curve of no compacted substrate depending on GI condition. Transistors don't have switching operation in gate insulator 2 condition. Compressive stress induced crack in Nitride layer during annealing process. Also from GI (2) condition to GI (3) condition, slope was improved.Fig8-7 shows I-V curve of compacted substrate depending on GI condition. From GI (1) to GI (2), flat region was generated. So the electrical performance is improved. In compacted glass, stress is not high to crack nitride layer of gate insulator. And this stress has effects on improving electrical characteristics. In GI (3), I_{on} currents increase and I_{off} currents decrease.Fig8-8 shows I-V curve in different substrate. And GI (2) condition was used. In Fig8-7 the characteristics in wafer of GI (3) is similar to that in compaction glass of GI(3). The results in Fig8-7 were mentioned in detail before.

In GI (3), I-V curve of different substrate was compared. In compaction glass,

slope reduced and the leakage currents decrease. In bare glass, pinning point raised and slope increase. In wafer substrate, the electrical characteristics were totally improved. So Nitride quality was improved. It is desirable to compare stress effect in Poly Si TFT with better GI layer. In wafer substrate, the electrical characteristics are the best among the three cases. In wafer, there is no stress [5]. The electrical performance of compaction glass is middle value between wafer and bare glass. In bare glass, electrical performance was more improved than previous cases (GI1, GI2). In Fig 8-9, Stress wasn't related to high leakage current.

Fig8-10 shows I-V curve in N channel poly Si TFT using GI condition 2. Comparing with Fig8-4, the electrical characteristics were improved. The performance in wafer is similar to that in compaction glass. In N type TFT, Stress cause the leakage currents to increase and reduction in on currents. No effects in slope and pinning phenomenon

8.4. Summary

The electrical characteristics were compared in different substrate and different GI condition. In P-type TFT, stress has effects on slope and Ion and leakage currents. But in N type TFT, the leakage currents increase. And In both N channel

and P channel, the performance on wafer is similar to that in compaction. So It is important to do compaction process in LTPS (>500ºC)

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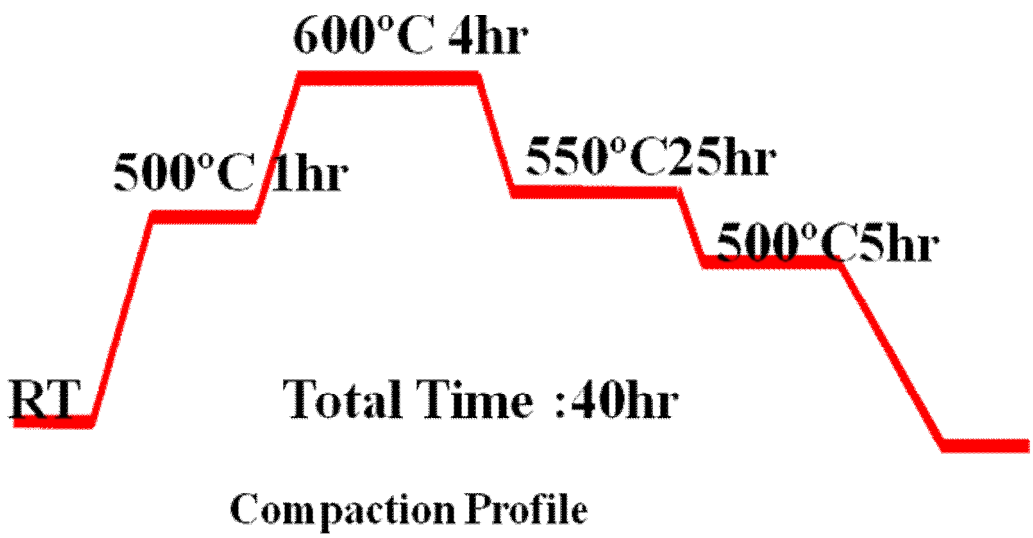
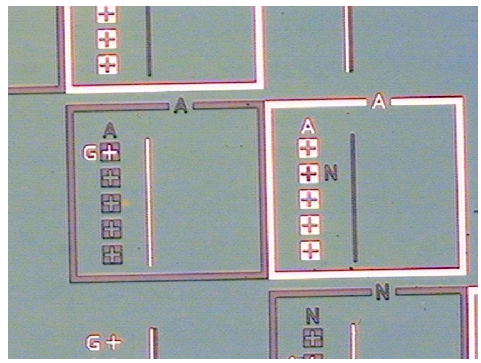


Fig.8-1. Compaction process.

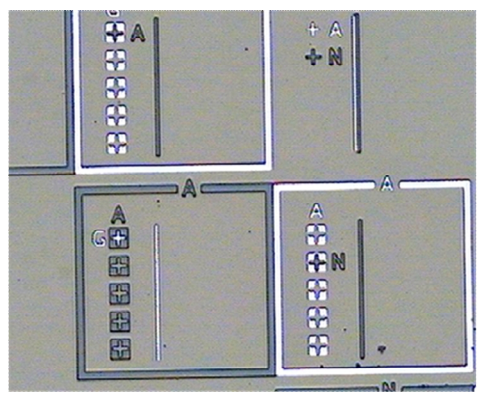
GI condition

	WP	RF	NH_3	SiH_4	Ar	Light response
1	300mTorr	20W	100sccm	25sccm	10sccm	Yes
2	300mTorr	20W	100sccm	15sccm	10sccm	No
3	450mTorr	20W	100sccm	15sccm	10sccm	No

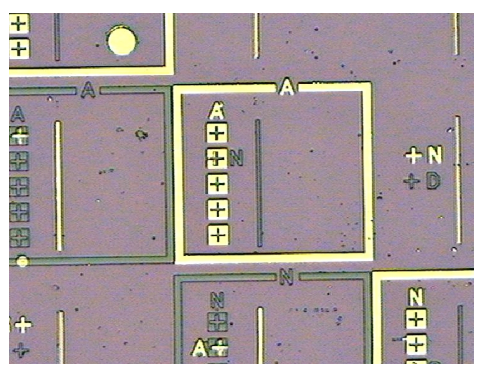
Table.8-1. Gate Insulator condition.



Wafer



Compacted glass



Bare glass

Fig.8-2. Misalignment in different substrate

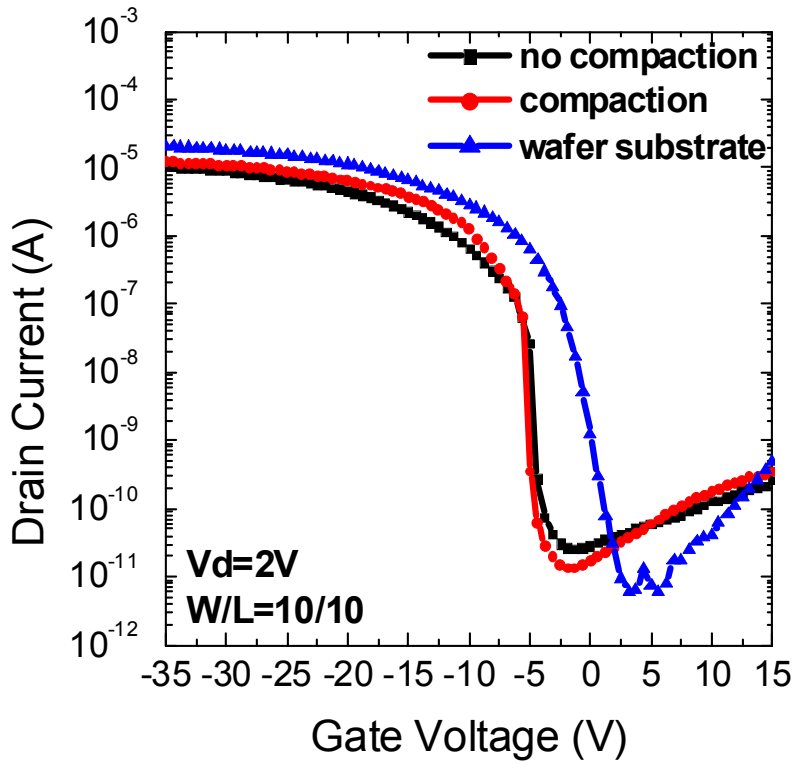


Fig.8-3. Thermal Stress effects on poly Si TFT of different substrate.

(PECVD Si)

	μ(cm^2 /VS)	V_{th} (V)	Slope(V/dec)	Ion($x10^{-5}$ A)	Ioff($x10^{-11}$ A)
Bare	**33**	**10**	**0.49**	**1.04**	**2.59**
Compaction	**50**	**6.87**	**0.4**	**1.23**	**1.34**
Wafer	**70**	**5**	**1**	**2.05**	**0.6**

Table.8-2 Detailed device parameters in poly Si TFT of different substrate.

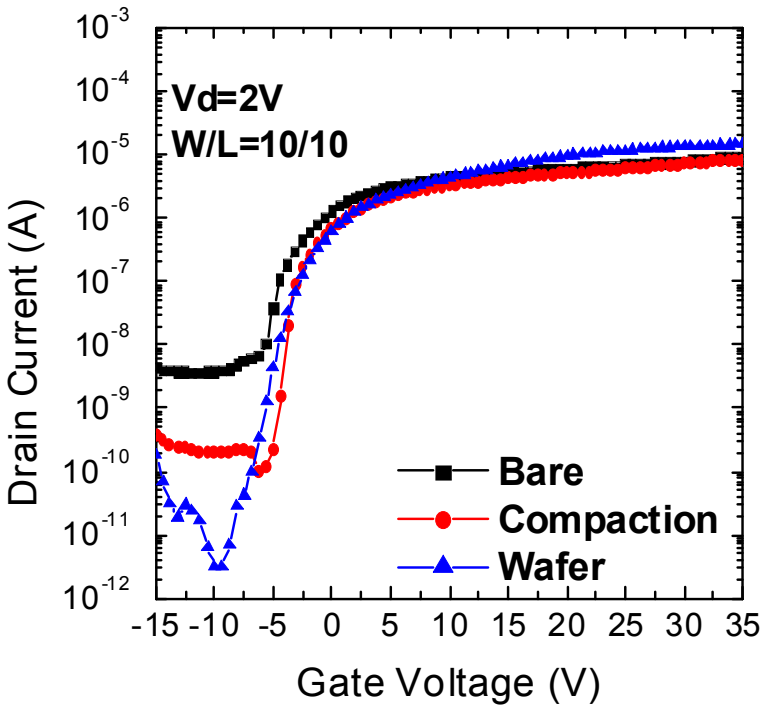


Fig.8-4. Thermal Stress effects on N channel poly Si TFT of different substrate.

(PECVD Si)

	μ(cm^2 /VS)	V_{th}(V)	Slope(V/dec)	Ion($x10^{-5}$ A)	Ioff($x10^{-11}$ A)
Bare	**26.6**	**1.25**	**1.23**	**0.97**	**382**
Compaction	**25**	**0**	**0.63**	**0.87**	**1.96**
Wafer	**38**	**1.25**	**1.1**	**1.46**	**0.3**

Table.8-3. Detailed device parameters in Poly-Si TFT with different substrate.

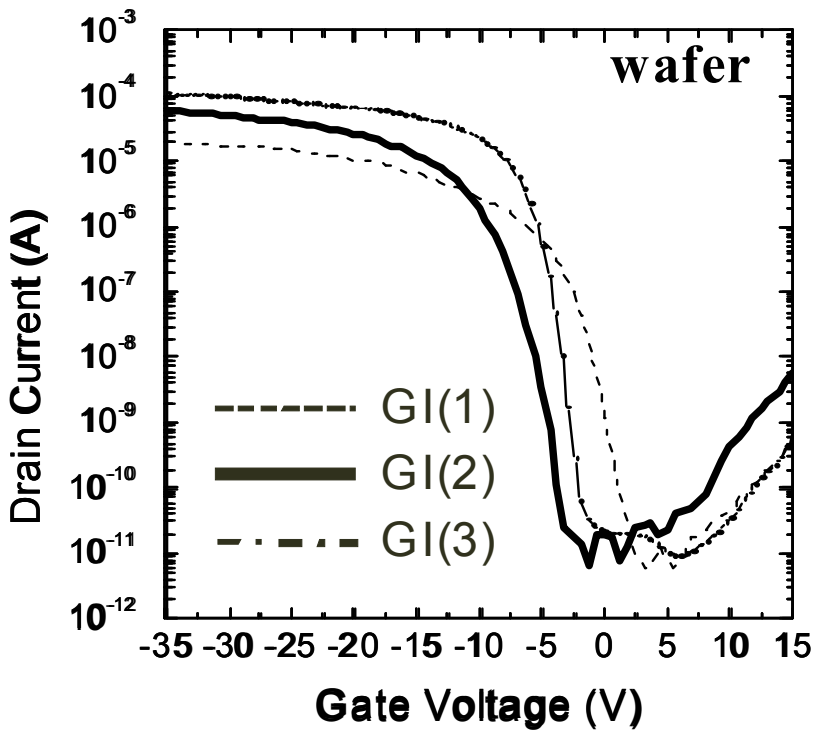


Fig.8-5. Relation between stress and nitride layer quality.

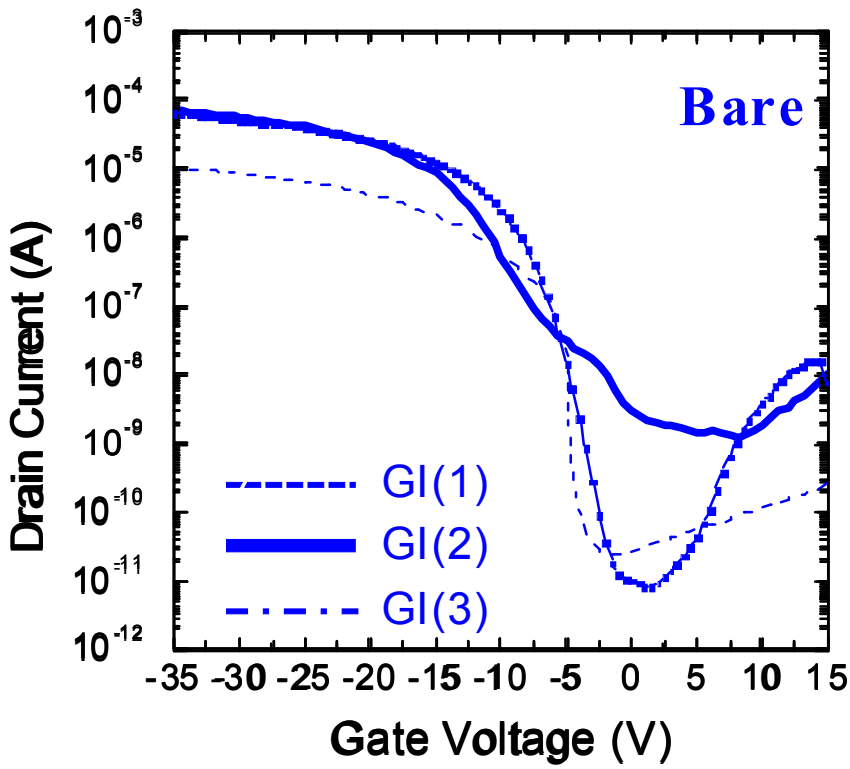


Fig.8-6. Relation between stress and nitride layer quality

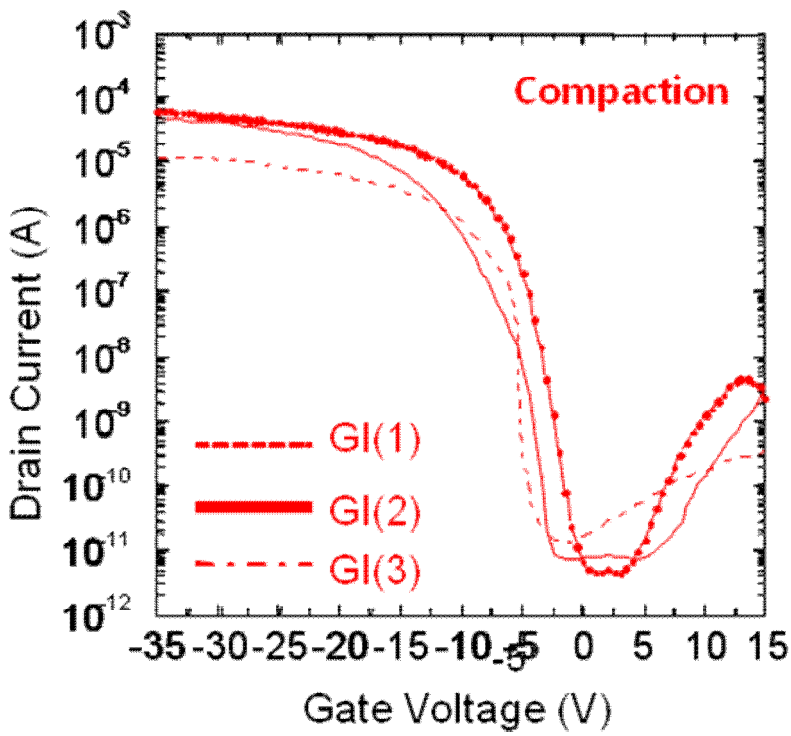


Fig.8-7. Relation between stress and nitride layer quality

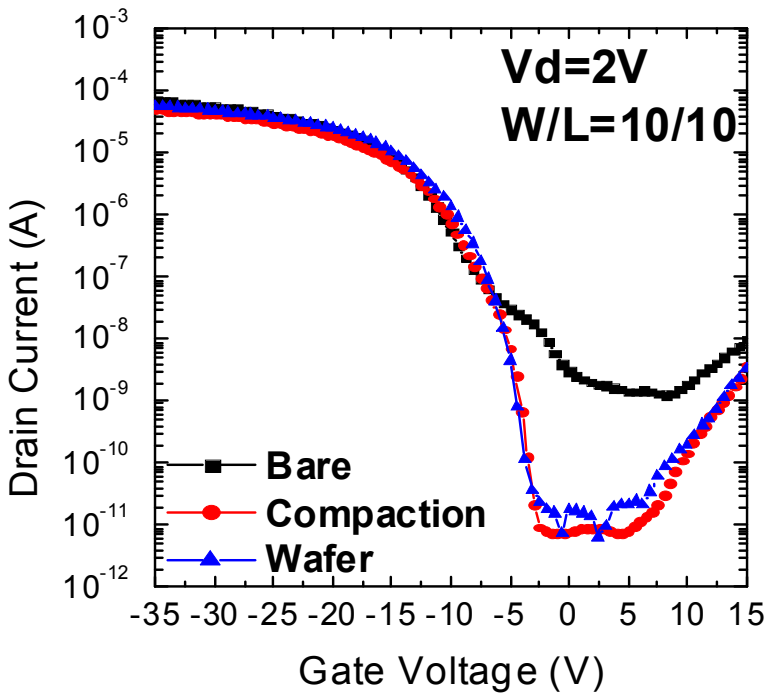


Fig.8-8. Comparison of P type TFT in different substrate

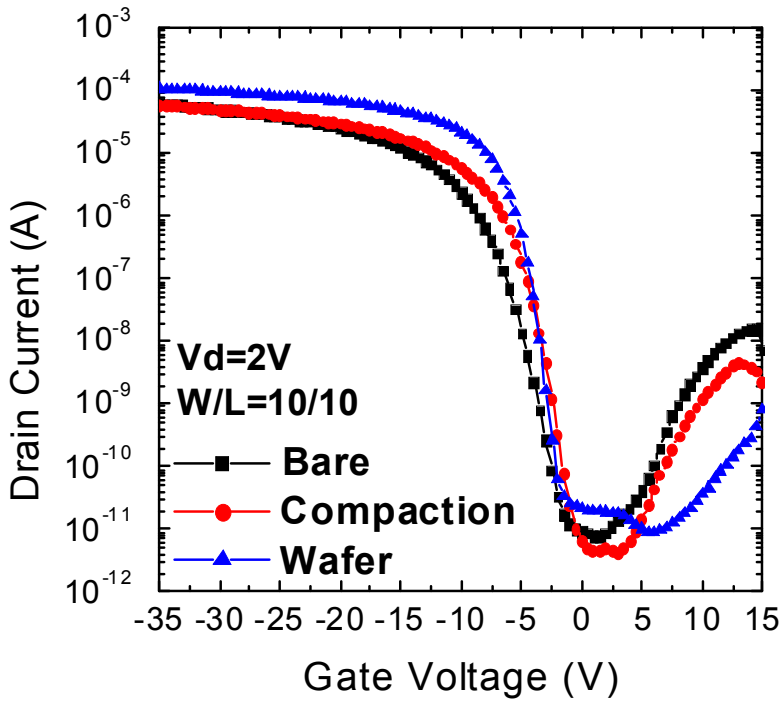


Fig.8-9.Comparison of P-type TFTs with New GI.

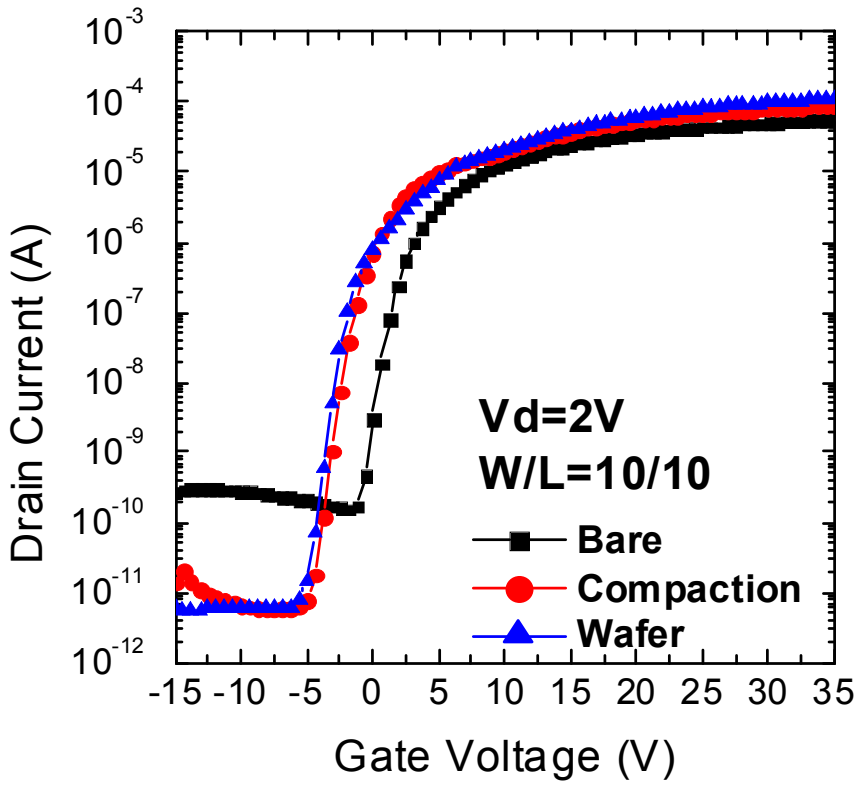


Fig.8-10.Comparison of N-type TFTs with GI(2).

	μ(cm^2 /VS)	V_{th}(V)	Slope(V/dec)	I_{on}($x10^{-5}$ A)	I_{off}($x10^{-11}$ A)
Bare	38	3.13	0.76	3.93	12
Compaction	172	0.6	0.64	6.11	0.42
Wafer	160	1.25	0.67	7.44	0.44

Table 4 Detailed device parameters in Poly-Si TFT with different substrate.

국문초록

금속 유도 측면 결정화에 의한 저온 다결정 실리콘 박막 트랜지스터의 구조 및 전기적 특성에 관한 연구

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액정 표시장치 회사들은 보통 저온 다결정 실리콘 박막 트랜지스터 기판이 후면 판으로 사용되는 능동 형 유기발광 다이오드로 전환하고 있다. 유기발광다이오드 디스플레이는 높은 휘도와 장시간의 수명을 요구하므로, 이러한 이유로 후면 판의 박막 트랜지스터는 높은 이동도와 높은 신뢰성을 필요로 한다. 일반적으로 저온 결정화 실리콘에서 박막 트랜지스터의 구조는 상부 게이트를 가지는 구조를 사용하며, 대형 유리 기판 위에 제조할 경우 어려움이 많다. 어려움 중 하나는 공정의 복잡화와 결정화를 위한 레이저 장비와 같은 제조 기기에 대한 개발이다. 실제 라인에서는 비정질 실리콘 박막 트랜지스터는 대형기판에서 제작이 유리한 하부 전극을 가지는 구조를 가진다. 그러나 유기발광 다이오드 디스플레이에서는 전기적 특성과 특히 낮은 신뢰성 때문에 적합하지 않다. 균일한 박막 트랜지스터를 얻기 위하여 여러

가지 방법들이 제한되었다. 그 중 하나는 고상 결정화인데, 제조가격이 저렴하고, 레이저결정화법에 비해 균일하게 만들 수 있다. 최근에 또한 니켈 촉매를 써서 만드는 금속유도 측면결정화법을 이용하며 높은 박막의 질을 가지는 소자를 만들 수 있다. 이러한 이유로 액정표시장치 회사의 생산라인에는 레이저를 이용하지 않은 결정화 기술이 필요하다. 액정 표시장치 회사들은 결정화 공정을 추가함으로써 유기발광다이오드 디스플레이를 제조할 수 있다. 하부전극을 가지는 소자는 한 챔버 내에서의 공정이 가능하며, 실제액정 표시장치 회사들의 실제 라인에 쓰이는 공정을 바꾸지 않고 제조 할 수 있다는 장점이 있다. 이 논문에서는 실제 제조라인에서 적용 가능한 하부전극을 가지는 다결정 박막 실리콘 트랜지스터의 공정 최적화를 연구하였다. 또한 외부에서 스트레스를 주어, 다결정 박막 실리콘의 전기적 특성도 연구되었다.

파트1 다결정 박막 실리콘트랜지스터에서의 공정최적화

파트2 다결정 박막 실리콘트랜지스터에서의 외부 스트레스가 미치는 영향

파트1에서는 공정 최적화에 관하여 논의되었다. 공정 최적화는 채널 두께, 게이트 절연막 두께, 소오스와 드레인과 게이트와의 중첩거리의 영향, 채널도핑에 관한 내용을 포함한다. 하부전극을 가지는 박막 트랜

지스터에서 채널 두께는 100Å에서900Å까지 변화를 주었으며, 400Å~600Å일 경우 전기적 특성이 다른 두께에서 보다 좋은 특성을 가졌다. 채널의 두께가 얇아지면서, 이동도 또한 낮아졌다. 게이트 절연막 두께는 1000Å이 적당하다.게이트 절연막의 두께가 증가할수록, 커패시턴스값이 작아지고, 이 때문에 온전류는 작아지고 기울기는 나빠지게 된다. 소오스와 드레인과 게이트와의 중첩에 있어서 소오스는 게이트와 중첩이되고 드레인은 떨어져있는 구조가 전기적 특성면에서 가장 바람직하다. 측면 전기장 때문에 드레인과 게이트사이의 거리가 누설전류에 큰 영향을 미친다. 그리고 수직 전기장의 영향은 채널 두께, 게이트 절연막의 두께를 바꿔가며 조사되었다. 게이트와 드레인 사이의 박막 두께는 수직적인 거리를 결정하기 때문이다. 채널 도핑은 상부전극을 가지는 다결정 박막 실리콘 트랜지스터에서 시행되었다. 다양한 채널 도핑법이 시도되었으며, 플라즈마를 이용한 화학기상증착법을 이용하여 채널 도핑 법이 가장 효과적이었다. 모스펫에서의 채널 외부에 위치한 게이트 절연막의 구조에 변화함에 따라 트랜지스터의 온 전류와 기울기가 개선되었다. 그 구조가 다결정 박막 실리콘 트랜지스터에 적용한다면 가파른 기울기를 기대할 수 있다.

파트2에서는 외부 스트레스 효과에 대한 영향을 살펴보았다. 외부효과는 기계적 스트레스와 열적 스트레스를 포함한다. 기계적 스트레스에

서는 유리기판을 잡아당김으로써 인장 스트레스를 가하였으며, 열적 스트레스에서는 기판을 달리 사용함으로써 확인하였다. 열처리 동안, 일반적인 유리기판은 줄어든다. 이때 이 스트레스는 압축 스트레스의 성격을 가진다. 이러한 점에서 외부스트레스가 다결정 박막 실리콘 트랜지스터의 전직적 특성의 미치는 영향이 조사되었다. 인장 스트레스에서는 이동도와 누설전류의 변화가 주요한 변화이다. P채널 박막트랜지스터와 N채널 박막 트랜지스터에서의 양상이 다르다. P채널에서는 인장방향에 상관없이 이동도는 증가하였으며, N 채널에서는 이동도가 수평방향의 인장스트레스에서는 증가하였고, 수직방향의 인장스트레스에서는 감소하였다. N 채널의 경우 모스펫 이론으로 설명이 가능하였다. 열적 스트레스에서는 이동도가 스트레스를 받을수록 감소하였다. 금속유도 측면 결정화 열처리와 활성화 열처리 동안 일반적인 유리는 줄어든다. 이때 게이트 절연막으로 사용된 질화막은 스트레스로 인한 균열을 가지게 된다. 일반적인 유리 위의 다결정 박막 실리콘 트랜지스터는 스위칭소자로써 동작하지 않게 된다. 이는 열적스트레스가 게이트 절연막에 균열을 생성시키게 하기 때문이다. 이러한 점에서 500° C가 넘는 저온 결정화 공정에서는 컴팩션 공정이 중요하다.

주요어 : 금속유도 측면 결정화, 다결정 실리콘,박막트랜지스터, 중첩,
오프셋, 하부전극을 가지는 박막 트랜지스터, 인장 스트레스,
압축 스트레스, 컴팩션 공정,이동도,누설전류, 기울기

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