Ph.D. DISSERTATION

Characterization of atomic layer deposited HfO_2 and TiO_2 high-k dielectrics on Si and Ge substrates

by

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Characterization of atomic layer deposited of HfO_2 and TiO_2 high-k dielectrics on Si and Ge substrates

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Abstract

The scaling of the CMOSFETs in silicon era which is using silicon dioxide has been already finished. Next generation CMOSFETs using HfO_2 high-k gate dielectric have been particularly in the mass production as high-k gate dielectric. Atomic layer deposition has many advantages in the formation of gate dielectric thin films for extremely scaled planar or three-dimensional structured devices due to self-limiting growth behavior, which confirms a low leakage current, high dielectric constant, and atomic-level precise thickness control. However, more studies are required to solve the issues such as charge trapping, insufficient reliability, and the abnormally high threshold voltage (V_{th}) due to Fermi level pinning, and fabricate Hf-based dielectric films with even higher-k values (k > 30) for further scaled MISFETs (EOT < ~0.5 nm). In addition, there is a greater challenge to apply ALD-processed HfO_2 to high-mobility channel materials such as III-V or II-V compound semiconductors for the n-type and Ge for the p-type MISFET. These challenges are known to be caused by the unstable interfaces between the HfO_2 film and the high-mobility substrates, the status of which is largely influenced by the detailed ALD conditions. Several other high-k dielectrics have been adopted for the high-mobility substrates, but HfO_2 is most favorable, can be extended to these substrates considering its mature process equipment, conditions, and contamination-control protocols in mass-

production lines.

To control the abnormally high V_{th} value of Hf-based gate dielectrics, capping a rare earth metal oxide layer or Al_2O_3 on Hf based dielectrics have received great attention. The capping layer needs to be thin and uniform to achieve the desired V_{th} control effect over a wide wafer and not to increase the CET values. Therefore, one of the most promising approaches to modulate the V_{th} is to adopt ALD capping layers, which is being tipped off as a solution due to its superior thickness controllability and uniformity, along with no plasma damage.

The effects of the relative position and thickness of ALD grown Al_2O_3, SrO, and La_2O_3 capping layers with HfO_2 gate dielectrics on flat band voltage (V_{FB}) modulation of metal-insulator-semiconductor (MIS) capacitor is reported in this study. Atomic layer deposited Al_2O_3, SrO, and La_2O_3 capping layers with HfO_2 gate dielectrics were examined. Al_2O_3 capping layers cause a V_{FB} shift into the positive voltage direction, while SrO and La_2O_3 capping layers cause a shift into the negative voltage direction. The bottom capping layer, which positions between the Si substrate and the HfO_2 dielectric was more effective in modulating the V_{FB} compared to the top capping layer. The insulating properties of the gate dielectric stacks with different capping layers were also examined. X-ray photoelectron spectroscopy analysis verified that top capping layers did not generally diffuse to the interface between the Si substrate and the HfO_2 dielectrics, which supports the result that bottom capping layers are more effective in

modulating the V_{FB}.

Variations in the growth behavior, physical and electrical properties, and microstructure of the atomic layer deposited HfO_2 gate dielectrics were examined with two types of oxygen sources: O_3 and H_2O for the given Hf-precursor of $Hf[N(CH_3)(C_2H_5)]_4$. The ALD temperature windows for the O_3 and H_2O were 160-320^oC and 160-280^oC, respectively, with the growth rate of HfO_2 using O_3 being higher than that of the films using H_2O within the ALD window. While the film density of HfO_2 using O_3 decreased, that of HfO_2 using H_2O increased with the decreasing ALD temperature. As the deposition temperature decreased, the amount of impurity in the HfO_2 film with the O_3 oxygen source increased due to the insufficient reaction, which led to the crystallization of the HfO_2 film into the tetragonal structure after the post-deposition annealing at 600^oC. The films with a lower density and a higher carbon-impurity concentration retained the portion of the tetragonal phase (~30%) to the highest annealing temperature of 1000^oC. However, the HfO_2 films grown at 200^oC with H_2O showed the best electrical performance, which could be ascribed to the highest density, low impurity concentration, and negligible involvement of the interfacial low dielectric layer.

HfO_2 films using O_3 and H_2O oxygen source at different deposition temperature applied to high-mobility substrates Ge. H_2O oxygen source could reduce the formation of sub-oxide at interface between HfO_2 and substrate. However, H_2O has weaker oxization power than O_3, impurities such as carbon is residued in deposited film which can act as defects. SiO_2,

Al_2O_3 passivation layer improved the leakage current and passivation of reaction or intermixing at interface between HfO_2 and substrate.

There was a limit to improve using HfO_2 high-k dielectric on high mobility substrate, it is essential to insert the passivation layer at interface which has low k value. Therefore TiO_2 of higher k value was adopted which have even small band gap with low barrier with Si and Ge substrates. SiO_2 and SiON passivation layer were effectively reduced the hysteresis voltage, frequency dispersion, and interface trap density. For more scaling the CET, the thickness of SiO_2 passivation layer was decreased from 2 to 0.5nm with TiO_2 high-k oxide. D_{it} values were maintained in order of 10^{11} level until 1nm of SiO_2 thickness; it is degraded in the condition of 0.5nm of SiO_2 thickness. At least 1nm of SiO_2 thickness is required for passivation the surface of Ge substrate. The EOT was scaled up to 1.4nm, D_{it} value was decreased as $1.3x10^{11}cm^{-2}eV^{-1}$.

Keywords: High-k, gate dielectric, Hafnium oxide, Titanium oxide, ALD, Atomic layer deposition, V_{FB} modulation, O_3 and H_2O oxygen source, high mobility channel, Ge

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List of Abbreviations

AES	Auger electron spectroscopy
AFM	Atomic force microscope
ALD	Atomic layer deposition
CBO	Conduction band offset
CET	Capacitance equivalent oxide thickness
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
C-V curve	Capacitance – voltage curve
DI water	Deionized water
D_{it}	Interface trap charge
DRAM	Dynamic random access memory
EOT	Equivalent oxide thickness
E_{ext}	External electric field
E_{dep}	Depolarizing field
E_{ox}	Electric field
E_g(oxide)	Bandgap of the oxide
E_g(Si)	Bandgap of the Si substrate
EWF	Effective Work Function
GAXRD	Glancing angle incidence X-ray diffraction
HCl	Hydrogen chloride
HF	Hydrofluoric acid
HRTEM	High resolution transmission electron microscopy

HP 4155	Hewlett-Packard 4155
HP 4194A	Hewlett-Packard Impedance/Gain-Phase Analyzer 4194A
I_{cp}	Charge pumping current
IL	Interfacial Layer
J_g	Leakage current density
J_g –V curves	Leakage current density – voltage curve
k value	Dielectric constant value
MOSFET	Metal oxide semiconductor field effect transistor
MOSCAP	Metal oxide semiconductor capacitor
MIS	Metal insulator semiconductor capacitor
MIM	Metal insulator metal capacitor
BTI	Bias temperature instability
P/NBS	Positive/negative bias temperature stress
PDA	Post deposition annealing
Poly-Si	Polycrstalline Silicon
PEALD	Plasma-enhanced atomic layer deposition
RMS	Root mean square
RTA	Rapid thermal annealing
SEM	Scanning electron microscope
t_{phy}	Physical thickness
TEM	Transmission electron microscopy
TEMAH	Tretrakis-Ethyl-Methyl-Amino-Hafnium
TMA	Tri-Methyl-Aluminum
VBO	Valence band offset

V_{FB}	Flat band voltage
V_g	Gate voltage
V_{th}	Threshold voltage
XPS	X-ray photoelectron spectroscopy
XRD	X-ray Diffraction
XRR	X-ray Reflectivity

1. Introduction

1.1. Introduction

New electronic device is launched with enhanced specification of high performance, low power, and small size consumption on every year. According to this scaling trend, chip makers tried to develop the technology to integrating more chips have a smaller feature size of transistor into a same or smaller space. Moore's law is no exaggeration to say that it has been guide the technology of the number of transistors on integrated circuits doubles approximately every two years (or 18 months). [1] That is, it is continuously scaled the minimum feature size of transistors. ITRS (International Technology Roadmap for Semiconductor) roadmap has been announced the technology trend of semiconductor industry every 1 or 2 years. [2] According to the contiuous scaling thickness of gate dielectric, the SiO_2 was faced with physical limit by gate leakage current due to direct tunneling of electrons. The ligthography and implant technology delayed the physical limits in terms of gate length, width, and junction depth. Therefore, high-k dielectrics which used as higher physical thickness to get identical capacitance equivalent oxide replaced SiO_2. [2-5] Various candidates of high-k gate dielectrics so many researched with respect to the ability to continuous scaling, instability by defect density, loss of carrier mobility, and gate threshold voltage (V_{th}) shift.

[5] Among various candidates, Hf-based high-k gate dielectrics have been choiced and then implemented in the 45 nm node [6]even though there are still some problems that need to be solved though, such as charge trapping, insufficient reliability, and the abnormally high threshold voltage (V_{th}) perhaps due to Fermi level pinning. Throughout the years, much research has been conducted to improve the properties of HfO_2, starting from research on the intrinsic properties of the material itself all the way to studies on the integration of thin films into semiconductor devices.

To control the abnormally high V_{th} value of Hf-based gate dielectrics, several approaches have been reported. Recently, capping a rare earth metal oxide layer on Hf based dielectrics have received great attention because it can effectively decrease the V_{th} value in n–type metal oxide semiconductor field effect transistors (nMOSFET) [7-9]. In addition capping Al_2O_3 on Hf based oxides have also been reported to reduce the V_{th} in p-type MOSFET (p-MOSFET) [10-11]. The capping layer needs to be thin and uniform to achieve the desired V_{th} control effect over a wide wafer and not to increase the capacitance equivalent oxide (CET) values. Atomic layer deposition (ALD) is particularly suitable for such purposes. However until now, reports for appropriate ALD precursors for rare earth metal oxide deposition for V_{th} modulation are rare. Therefore sputtering systems have been widely used as the major deposition technique for nMOS V_{th} modulation layers [7-9]. In addition, the mechanism for the V_{th} modulation is still rather unclear although there have been several attempts to explain the origin of it. Therefore, one of

the most promising approaches to modulate the V_{th} is to adopt ALD capping layers, which is being tipped off as a solution due to its superior thickness controllability and uniformity, along with the fact that there is no plasma damage [10, 12]. In this paper, the effects of the relative position and thickness of ALD grown Al_2O_3, SrO, and La_2O_3 capping layers with HfO_2 gate dielectrics on flat band voltage (V_{FB}) modulation of metal-insulator-semiconductor (MIS) capacitor is reported.

As continuing the requirement to high performance device, HfO_2 gate dielectric will be also suffer the limit of physical thickness. For finding a breakthrough, equivalent oxide thickness (EOT) scaling by reduce the interfacial layer, or gate dielectrics of higher dielectric constant (higher-k) have been intensively investigated. It is important not only high-k gate dielectrics but also metal gate replaced the poly-Si gate which can cause interaction with high-k dielectric, gate depletion, and boron penetration. [2,5] Metal gate is also studied for controlling the work function for suiting n/p MOSFETs, matching with high-k gate dielectrics. High-k gate dielectric metal gate stack (HKMG) is inseperable each other, and major terminology in semiconductor industry. [2, 5-6]

Moreover, to achieve further increased transistor performance, high-k gate dielectrics combined with the high mobility channel materials such as Ge and III-V semiconductors have attracted lots of attention by assumption the end of Si era. Figure 1.1 shows ITRS Roadmap of Process Integration, Devices, and Structure (PIDS) in Front end announced in 2011. [2] For gate stack, Hf based

high-k with higher-k gate dielectric on non-Si high mobility channels with ALD tool is required to research. In addition, Ge based high mobility channel for pFET and III-V based high mobility channel for nFET are also needed to research. However, defective oxide at interface was formed by oxidation of high-mobility substrate during high-k ALD process, so oxygen source of ALD process is important to improve the interface quality and structural and electrical properties of high-k dielectric gate dielectric on high-mobility substrate. Therefore, point of view of improvement and effects of O_3 and H_2O as oxygen sources and deposition temperature of high-k dielectric it self and change on high mobility substrate was focused in this study.

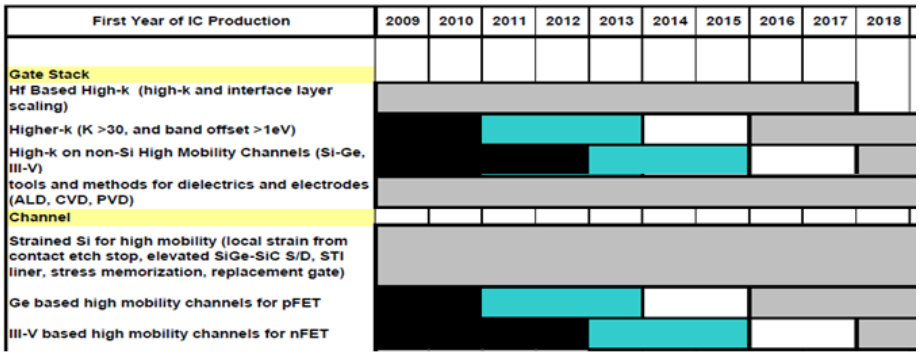

Figure 1.1 ITRS Roadmap of Process Integration, Devices, and Structure (PIDS) in Front end (2011) [2]

1.2. References

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2. Literature Review

2.1. High-k gate dielectrics

2.1.1. Introduction of high-k gate dielectrics

Silicon is called as “material of God” in semiconductor history that has so many advantages such as easy to obtain, stable interfacial/thermal oxid. Si based complementary metal oxide semiconductor field effect transistors (CMOSFETs) was successfully developed and evolved with continuos scaling by courtesy of technology for decades. SiO_2 as gate oxide have a lot of advantages that is able to thermally growing from Si substrate with procise control the thickness and uniformity, and naturally configurates a stable interface with Si substrate, has largest bandgap ~ 9eV for isolation, and has low intrinsic interface trap/defect density which can fluently apply to integration/fabrication the CMOSFETs due to high resistance and immunity to sustain high thermal budget as 1050 ^{o}C. [1-3]

As the new era of high-k metal gate (HKMG) stack is coming according to aggressive scaling down for high density integration which limits of physical thickness of gate oxide even though nitride silicon oxide layer. The gate leakage current by direct tunneling through thin SiO_2 can be reduced by replace to thicker high-k gate dielectric in capacitance equivalemt oxide

(CET). CMOSFETs are operated using capacitance, since gate capacitance controls the source-drain current (I_{on}) in figure 2.1 and equation 1.

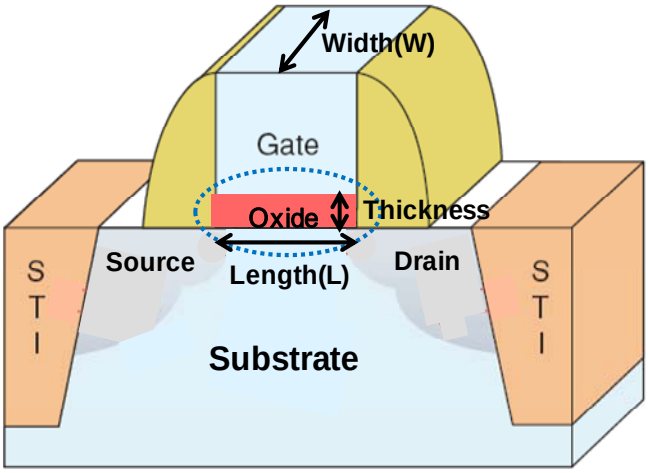

Figure 2.1. Conventional metal oxide semiconductor field effect transistor (MOSFET)

$$I_{on} = \frac{\mu_{eff} C_{ox,inv}}{2} \frac{W}{L} (V_{gs} - V_{th})^2 \qquad \text{- Equation 1}$$

I_{on} is source-drain current, μ_{eff} is the effective mobility of carrier, C_{ox} is gate capacitance, W is width and L is length of gate on transistor, and V_{gs} and V_{th} is the operating and threshold voltage of transistor, respectively. Cox could be got from equation 2, k is the dielectric constant (relative permittivity) of gate dielectric, ε_0 is permittivity of free space, A is the area

which measured the capacitance, T is physical thickness of gate dielectric. Therefore, high-k gate dielectric is able to maintain thicker T in condition of same capacitance with same area. In addition, thicker high-k dielectric can reduce the leakage current by direct tunneling. [1,4-5]

$$C_{ox,inv} = \frac{k\varepsilon_0 A}{T_{inv}} \qquad \text{- Equation 2}$$

As adoption of high-k dielectrics, electrical thickness is required for conventially conversion of thickness relative to SiO_2. So equivalent silicon dioxide thickness or 'equivalent oxide thickness' (EOT) is proposed.

$$t_{ox} = EOT = \frac{3.9}{k} T_{high-k} = \frac{3.9\varepsilon_0}{k} T_{high-k} \qquad \text{- Equation 3}$$

The dielectric constant of SiO_2 is 3.9, $T_{high\text{-}k}$ is physical thickness of high-k dielectric. Reducing this EOT value is goal of scaling down by high-k or decreasing $T_{high\text{-}k}$. In addition, capacitance equivalent thickness (CET) will be frequently mentioned in this study because it is conventionally extracted from measured capacitance and area.

$$CET = \frac{3.9\varepsilon_0 A}{C_{\max}} \qquad \text{- Equation 4}$$

A is gate area of measured capacitance, C_{max} is maximum capacitance in condition of carrier accumulation. Futhremore, CET is sum of EOT and quantum mechanical effect (0.3-0.4 nm) by carrier accumulation of semiconductor substrate.

Considering these factors, necessity of high-k dielectric is thoroughly mentioned. Among various candidates of high-k gate dielectrics are ploted in figure 2.2. The requirements are; high enough k value prepared for scaling, thermodynamically stable direct contact with channel, kinetically stable and compatible to process over 1050^{o}C, insulating property which have over band offsets over semiconductor substrate, good electrical interface with substrate, and few bulk electrically active defects. For insulating property, the band gap is important especially conduction band offset (CBO) for blocking electron carriers, but relationship between band gap and dielectric constant is trade off as shown in figure 2.2. TiO_2 and $SrTiO_3$ represnets large dielectric constant, but it has too low band gap with low CBO, tahat is candidate for dielectircs in DRAM capacitor. [6] Figure 2.3 shows the calculated conduction band and valence band offsets of various oxides on Si.

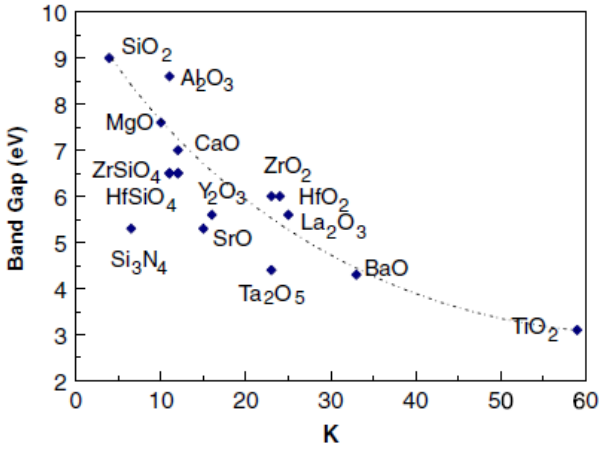

Figure 2.2 Static dielectric constant versus band gap for candidate gate dielectrics. [1,2]

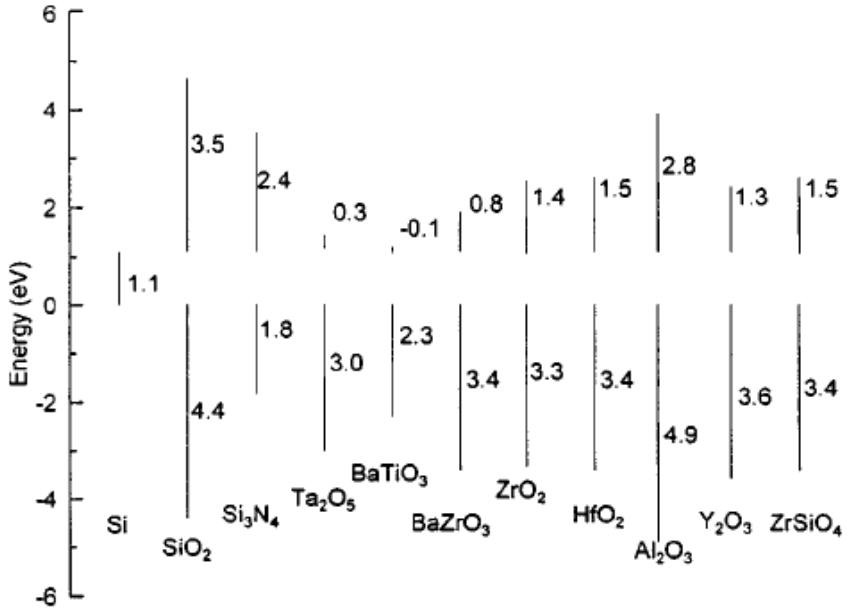

Figure 2.3 Calculated conduction band and valence band offsets of various oxides on Si. [1]

2.1.2. HfO_2 High-k thin films by ALD

HfO_2 is most promising candidate among various high-k dielectrics, the evidence that is applied in the mass production of Si-based metal insulator semiconductor field effect transistors (MISFETs), as high dielectric constant gate dielectric thin films since 2007 [4,7-8]. Atomic layer deposition (ALD) has many advantages in the formation of gate dielectric thin films for extremely scaled planar or three-dimensional structured devices due to its self-limiting growth behavior, which confirms a low leakage current, high dielectric constant, and atomic-level precise thickness control. However, more studies are required to fabricate Hf-based dielectric films with even

higher-k values (k > 30) for further scaled MISFETs that require an equivalent oxide thickness (EOT) < ~0.5 nm. Several other high-k dielectrics, such as Al_2O_3, La_2O_3, and $LaLuO_3$ [9-12], have been adopted for the high-mobility substrates, but it might be best if the use of HfO_2 can be extended to these substrates considering its mature process equipment, conditions, and contamination-control protocols in mass-production lines.

Because of these important aspects of HfO_2 in advanced semiconductor chips, ALD of the HfO_2 film is one of the most extensively studied ALD processes. While the commercialized ALD process of the HfO_2 film for high-k gate dielectric application adopted $HfCl_4$ and H_2O as the Hf-precursor and the oxygen source, respectively [13-16], alternative ALD processes that utilize metal-organic Hf-precursors and O_3 are still under intensive research [17-19]. The major driving force for the search for such an alternative ALD process is the difficulty in handling the powdery $HfCl_4$ precursor, which requires a high vaporization temperature (~200^oC) to achieve sufficient vapor pressure, and hardware problems related to the corrosive reaction by-product (HCl) of the process [20]. The ALD process of the HfO_2 film using $HfCl_4$ and H_2O could be performed well at the substrate temperatures (T_s) of 300 - 400^oC without the concern related to the thermal decomposition of the $HfCl_4$. In contrast, most metal-organic Hf-precursors suffer from such degradation at a relatively low T_s; most Hf-alkoxides and Hf-alkylamides thermally decomposed at temperatures lower than ~200-250 and 300-350^oC, respectively, the accurate

values of which are dependent on the detailed process conditions [21-23]. (Modified) cycloropentadienyl (Cp)-based Hf-precursors have shown higher thermal decomposition temperatures (of up to ~ 400^{o}C) [24], but ALD using the Cp-based Hf-precursors usually has a lower growth rate (< ~0.05 nm/cycle) than other metal-organic Hf-precursors, presumably due to the higher bulkiness of the ligand and its superior thermal stability [24-25]. Finally, N-containing Hf-precursor, $Hf[N(C_2H_5)(CH_3)]_4$; TEMAH was used to examine the possible improvement keeping the *in-situ* $Si(O)N_x$ reaction barrier layer. TEMAH is widely used recently, because it shows relatively high growth rate (0.1 nm/cycle), good reproductivity and stability with low impurity. [16]

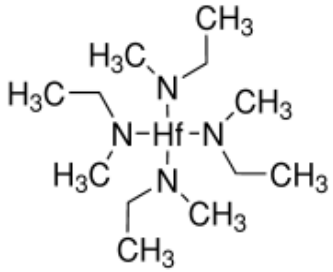

Figure 2.4 Schematic diagram of Hf precursor TEMAH

2.2. Issues and challenges of high-k

2.2.1. V_{th} modulation issue

To control the abnormally high V_{th}, various methods and materials were examined. Firstly, various rare earth metal capping on high-k dielectric by sputtering is reported, it causes large V_{th} shift, the shift amount is different according to the capping material. V_t tuning depends on rare earth (RE) type and diffusion in Si/SiO*x*/HfSiON/REO*x*/metal gated *n*FETs as follows: Sr<Er<Sc+Er<La<Sc<none. In addition this V_{th} ordering is similar with the trends in dopant electronegativity (EN) dipole charge transfer and ionic radius (r) dipole separation expected for a interfacial dipole mechanism and oxygen vacancy model in figure 2.5. [26]

One of the most popular V_{th} modulation layer is La_2O_3. La_2O_3 capping induced V_{th} shift according to the increase of La_2O_3 ALD cycle. In addition, relative position of La_2O_3 with HfO_2 also influences on V_{FB} shift in figure 2.6.

By separating the effect of the fixed charges located at each interface by thickness-dependent V_{FB} evolution, total voltage shifts (dipole) at metal/high-k and high-k/SiO_2 interfaces have been estimated. A simple model using electronegativity has been proposed to explain the V_{FB} shift. [27]

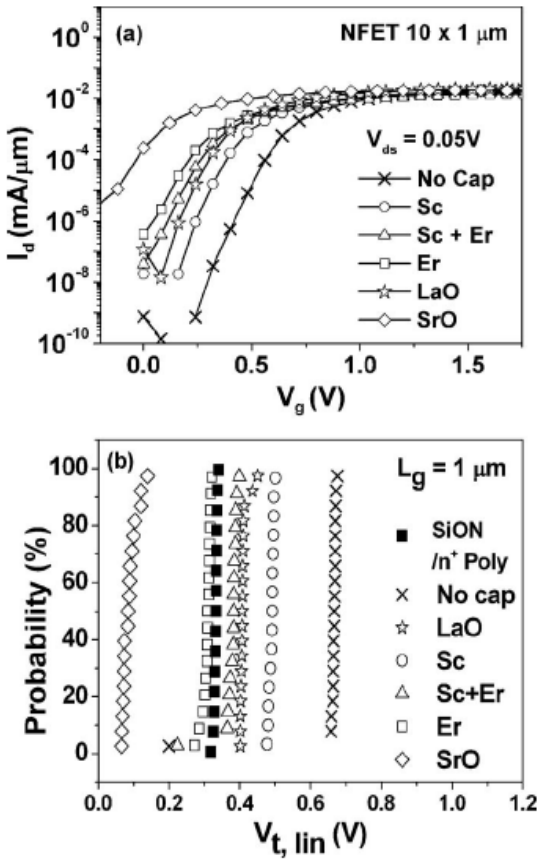

Figure 2.5 (a) *Id-Vg* characteristics at *Vds*=50 mV for *n*FET with different HfSiON dopants. (b) Dopant type significantly affects *Vt*. Maximum *n*FET *Vt* tuning of ~600 mV for SrO and minimum *Vt*, tuning of ~250 mV for Sc. Similar transfer characteristics are observed for both 1 um and 80 nm gate length. [26]

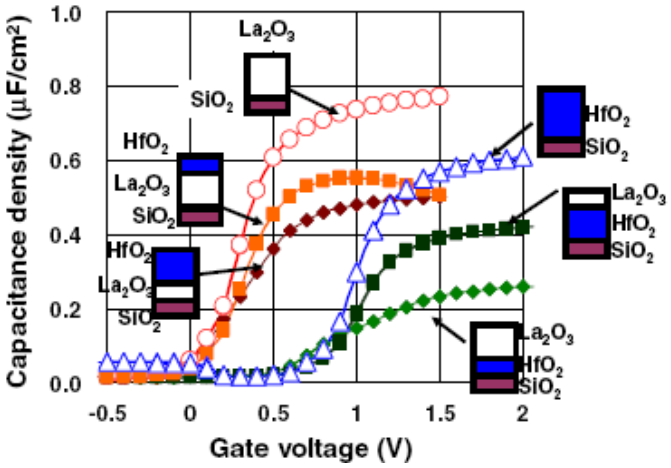

Figure 2.6 C-V characteristics of high-k stacked MOS capacitors with SiO_2 IL. V_{FB} is determined by the high-k on IL. [27]

There are some reports for figure out the origin of V_{FB} shift. Firstly, Kita and Toriumi reported that dipole is formed by the different oxygen areal density of high-k dielectric and interfacial SiO_2. This difference causes diffusion of oxygen which results dipole formation in figure 2.7. [28] In this theory, the dipole moments of various high-k oxides are calculated and address the trend of V_{FB} shift direction and amount with respect to many kinds of V_{th} modulation layers in figure 2.8. [30] Secondly, Lin and Robertson reported that charged ions and their image charges at a polar interface of an oxide next to metal induce dipole layer after cancelling neutral units in figure 2.9. [29] Finally, Kirsch et al. reported that charge transfer in the Hf-O-RE(rare earth) configuration of chemical bonding induce dipole moment by EWF shift as amount of Δ in figure 2.10. [26]

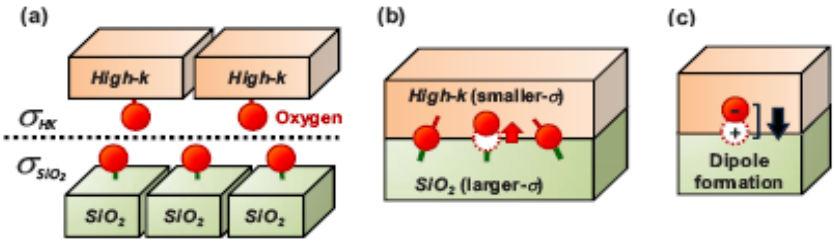

Figure 2.7 Schematics of our model to explain the dipole formation at high-*k*/SiO_2 interface based on the difference of areal density of oxygen atoms (σ) for the case that high-*k* oxide has smaller- σ than SiO_2. [28]

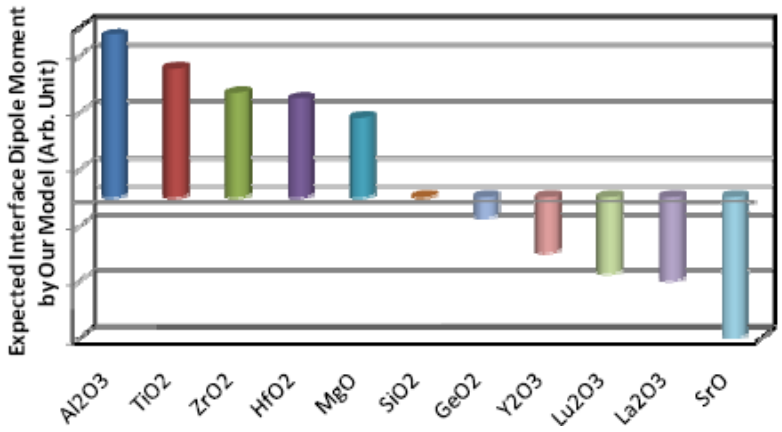

Figure 2.8 Summary of the dipole moment formed at high-k/SiO_2 interface predicted by our model, for various high-k candidates including GeO_2. The dipole direction to increase V_{FB} is represented as a positive direction [30]

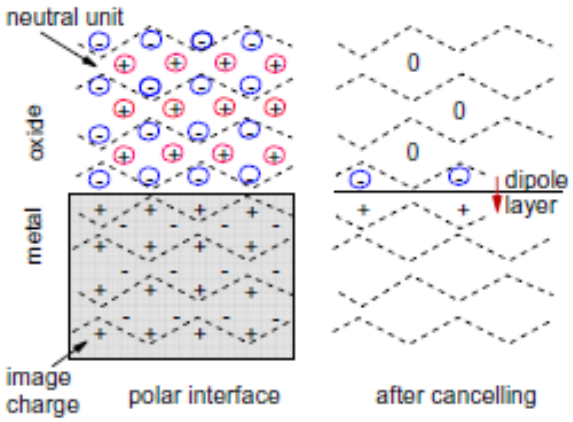

Figure 2.9 Schematics of (a) Charged ions and their image charges at a polar interface of an oxide next to metal, (b) dipole layer after cancelling neutral units. [27]

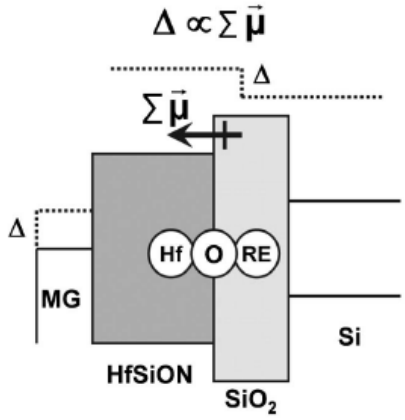

Figure 2.10 Interface dipole moment model. EWF shift (Δ) is proportional to dipole moment due to the charge transfer in the Hf-O-RE configuration. The dipole moment magnitude varies with dopant type explaining the V_{th} dependence on dopant type. [26]

2.2.2. Higher-k gate dielectrics

There are many kinds of materials which have higher dielectric constant, but it will be focused on doping or changing the crystal structure of conventially used HfO_2 films. Firstly, Jung et al. reported the effect of deposition temperature of ALD HfO_2 on Si and Ge substrates. After annealing, the HfO_2 films grown at 200◦C and 280◦C were crystallized to the tetragonal (*t*) and monoclinic (*m*) phases, respectively, which was related to the carbon contents within the films and grain boundary energy. To clarify this, the energy difference between a *t*- and a *m*- phases (ΔE_{tetra}) was calculated by first principles calculations. The higher k value of *t*-HfO_2 compared to amorphous and monoclinic HfO_2 was experimentally confirmed. Figure 2.11 shows the EOT vs. T_{phy} plots and J_g vs. EOT plots.

Higher concentration of impurities due to low O_3 concentration of ALD process can cause crystallization by tetragonal phase (higher-k) rather than monoclinic due to C-O bonds between HfO_2 domains described in figure 2.12. It was found that in the as-grown states, the oxygen stoichiometry and local atomic structure in amorphous HfO_2 domains are maintained nearly as constants even when the film is grown without external ozone supply, while some C−O bonds remain between the almost stoichiometric HfO_2 domains due to incomplete oxidation of the precursors. After a postdeposition annealing (PDA), the films crystallize with a monoclinic structure ($P2_1/c$), except for the case of the no-ozone supply in which the film possesses a tetragonal crystal structure ($P4_2/nmc$). It is

demonstrated that the carbonate bonds play a major role in stabilizing the tetragonal structure through nanoscale separation of the HfO_2 domains. Accordingly, the roles of the oxygen source and the PDA are also newly addressed as being related to the carbonate bonds. The ozone gas acts as an oxygen supplier, and more importantly, it reduces the residual carbonates to stabilize the bulk crystal structure in the thin films. The PDA not only delivers the thermal energy to induce the crystallization but also eliminates C atoms to increase the size of the HfO_2 domains leading to the densification of the films.

Lee et al. reported that increase the k values of the HfO_2 film by transforming its structure from monoclinic to tetragonal phase by mixing with ZrO_2. The HfO_2 films were alloyed with ZrO_2, which was an effective method of changing the structure from monoclinic to tetragonal. While the k values of the $Hf_{1-x}Zr_xO_2$ (HZO) film could be tuned by the Zr concentration and the PDA temperature, the increase of the PDA temperature to over 800^{o}C induced the compositional segregation of HZO, which largely increased the leakage current. A critical Zr concentration was found (between 50 and 70%), in which the k-value increase was quite abrupt but the increase in leakage was not very evident after the PDA at 700^{o}C as shown in figure 2.13.

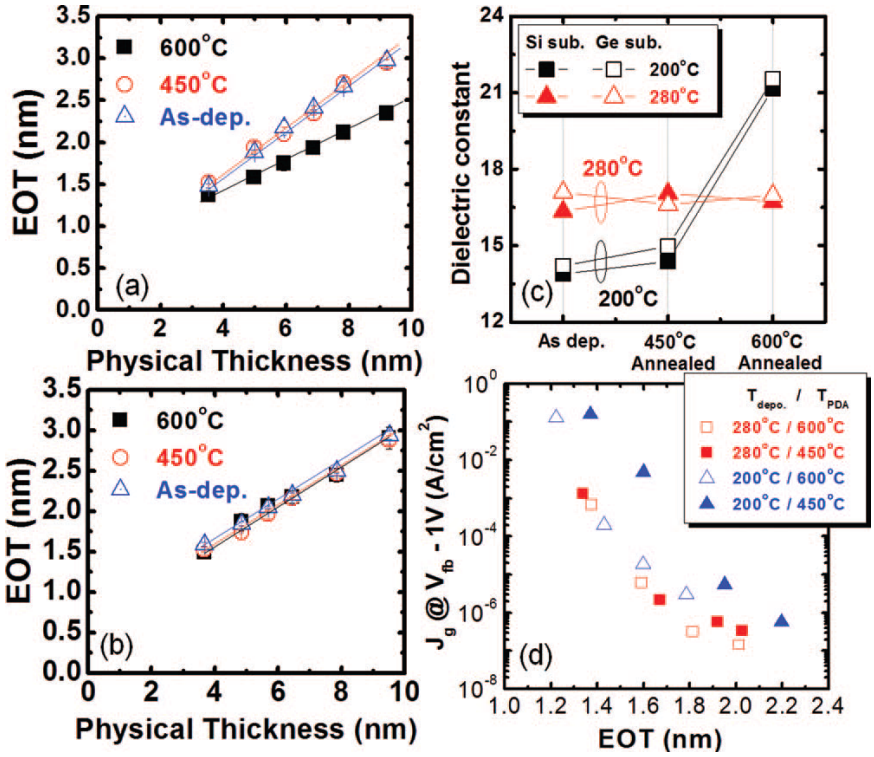

Figure 2.11 EOT vs. T_{phy} plots of (a) 200-HfO_2 and (b) 280-HfO_2 grown on Ge substrates after annealing at various temperatures. (c) The calculated k values of the HfO_2 films grown on Si and Ge substrates prepared at various deposition and PDA temperatures. (d) Variation of dielectric leakage current density (measured at a voltage of V_{FB} – 1V) as a function of EOT of the 200-HfO_2 and 280-HfO_2 samples after the PDA at 450 and 600◦C, respectively. [31]

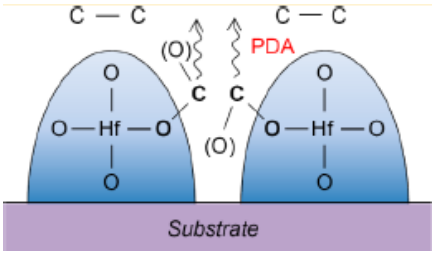

Figure 2.12 Schematic diagrams of C-O bonds between HfO_2 domains. [32]

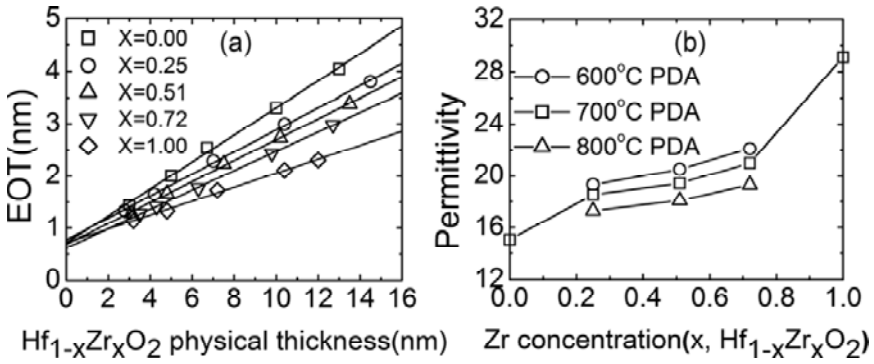

Figure 2.13 (a) Variation of CET as a function of the physical oxide thickness for different Zr concentrations and TPDA. (b) Summary of the k values for the different conditions. [33]

2.2.3. High hole mobility channel for pMOS

As the aggressive scaling of Si-based complementary metal-oxide semiconductors approaches the fundamental limit, various attempts such as modified channel materials have been investigated in attempts to improve device performance by enhancing the carrier mobility in the channel region. One possible modification of the channel region being considered at present involves replacing the conventionally used Si by alternative semiconductor materials such as Ge and III-V compound semiconductors. Among various semiconductor materials, Ge and GaAs are promising candidates for p/nFET due to about 4 times higher hole mobility/6 times higher electron mobility than value of Si, the properties of various potential channel materials at 300K in table 2.1. In advance, Ge substrate is mentioned in this section.

	Si	Ge	GaAs	InAs	InSb	InGaAs	InP
E_g [eV]	1.12	0.66	1.42	0.36	0.17	0.75	1.344
μ_e [cm^2/Vs]	1500	3900	**9200**	40000	80000	10000	5400
μ_h [cm^2/Vs]	450	**1900**	400	500	1250	250	150
Dielectric constant	11.7	16.0	13.1	14.8	17.7		

Table 2.1 The properties of various potential channel materials at 300K.

It is known that the lattice constant of Ge is close to that of GaAs is expected to facilitate integration of III-V n-MOSFETs and optical devices on Ge substrates in the future. Although Ge has the excellent properties, the lack of a stable passivation oxide and the necessity of a lower temperature process have hindered the fabrication of Ge-based devices. Ge has lower thermal stability, it starts to melt at 938^{o}C, which sets the maximum temperature that can be used in a Ge containing process. In addition, Ge is easily oxidized in various environments and form an oxide layer consisting of a mxture of mainly mono oxide (GeO) and dioxide (GeO_2) species. GeO_2 is a polymorph, and the characteristics of GeO_2 obviously depend on the oxidation state and crystallinity. GeO_2 is transformed from hexagonal phase to tetragonal phase at 1033°C by annealing. Since hexagonal or amorphous GeO_2 is a major phase at room temperature, GeO_2 is soluble in water. In contrast, GeO(s) is insoluble. The most important reaction is GeO_2 + Ge → 2GeO (s) or 2GeO (g), which indicates that GeO_2 consumes Ge at the interface. Moreover, GeO_2 on Ge not only decomposes into GeO(s) but also desorbs as gas-phase GeO(g.). Figure 2.14 shows instability of Ge on high temperature. GeO is formed over 600 ^{o}C, and GeO_2 desorption is stated over 430 ^{o}C. [34]

Next is reported that effect of H_2O and O_3-based ALD high-k dielectric films on GeO_2 passivation layer. Figure 2.15 shows the interface chemical bonding state, the sample conditions are as follows;

a: 1nm GeO_2 by 20min oxidation with O_3

b: 1nm GeO_2+2nm Al_2O_3 (O_3 ALD)

c: HF cleaned Ge+2nm Al_2O_3 (O_3 ALD)

d: 1nm GeO_2 + 2nm HfO_2 (H_2O ALD)

H_2O oxygen source effectively reduced sub-oxide bonding peaks, in addition CET values are also decreased due to less reaction of substrate when high-k film was deposited using H_2O as shown in figure 2.16. [35] Furthermore, the interface state density can be significantly reduced by annealing the Pt-gated capacitors in forming gas (H_2/N_2) at 300°C.

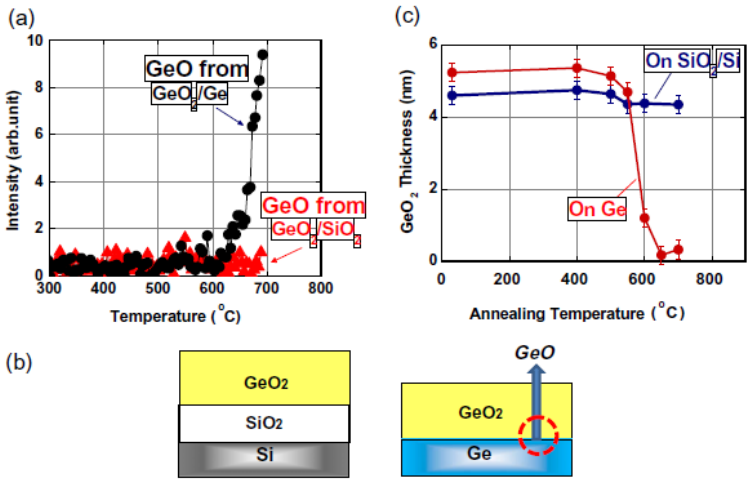

Figure 2.14 (a) GeO_2 thickness on Ge and on SiO_2/Si as a function of annealing temperature,(b) Schematic view of GeO desorption in GeO_2/Ge stack [34].

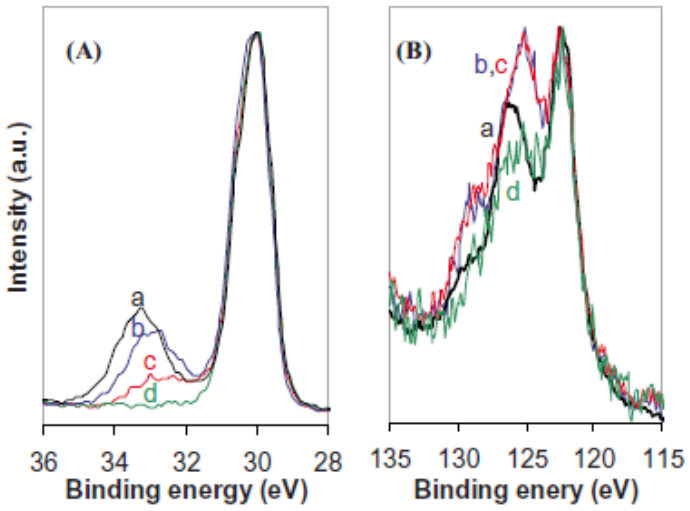

Figure 2.15 XPS Ge 3d spectra of the following samples: (a) 1 nm GeO_2 obtained by 20 min oxidation with O_3 at 300°C, (b) 1 nm GeO_2 + 2 nm Al_2O_3 (TMA/O_3 ALD), (c)HF-cleaned Ge + 2 nm Al_2O_3 (TMA/O_3 ALD), and (d) HF-cleaned Ge + 2 nm Al_2O_3 (TMA/H_2O ALD).(B) XPS Ge 3p spectra of the following samples: (a) 1 nmGeO_2 obtained by 20 min oxidation with O_3 at 300°C, (b) 1 nmGeO_2 + 2 nm HfO_2($HfCl_4$/O_3 ALD), (c)HF-cleaned Ge + 2 nm HfO_2 ($HfCl_4$/O_3 ALD) [the spectra for (b) and (c) are identical], and (d) 1 nm GeO_2 + 2 nm HfO_2 ($HfCl_4$/H_2O ALD) [35].

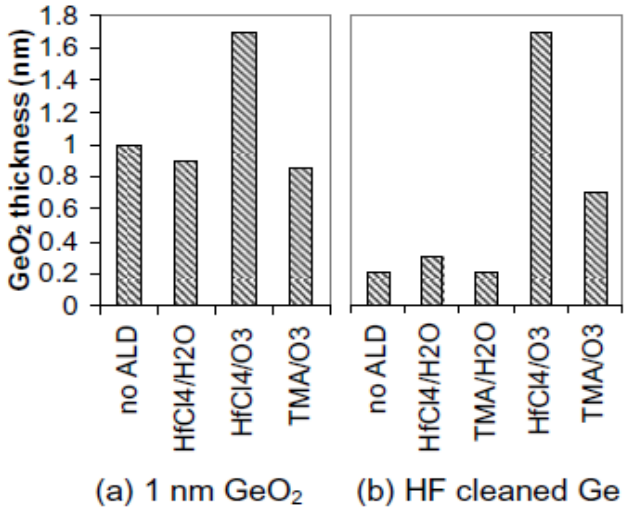

Figure 2.16 GeO_2 thickness determined by XPS after ALD of 2 nm HfO_2 or Al_2O_3 (a) on 1 nm GeO_2 (20 min oxidation with O_3 at 300°C), and (b) on HF-cleaned Ge [35].

2.2.4. High electron mobility channel for nMOS

III-V compound semiconductors also have unstable characteristics similar with Ge. Therefore, there are reports that adopted surface treatment or passivation layer similar with Ge substrate. First, self cleaning effect with passivation effect of Al_2O_3 is reported. Al_2O_3 using TMA and H_2O induce the improvement of frequency diepersion with D_{it} property and reduce the thickness of interfacial layer confimed by TEM in figure 2.17.

Next, effect of ALD deposition temperature of high-k dielectric was reported. The interface properties such as the C-V characteristics and the interface trap density (D_{it}) and the interface structure of HfO_2/InGaAs have strong dependence on the ALD temperature, while the Al_2O_3/InGaAs interfaces hardly depend on it. As a result, we have achieved the HfO_2/InGaAs interfaces with low Dit comparable to that in the Al_2O_3/InGaAs interface by lowering the ALD temperature down to 200^{o}C or less. Also, we have found that As_2O_3 and Ga_2O_3 formed at the interface during ALD increase with a decrease in the ALD temperature as shown in figure 2.18. Combined with the ALD temperature dependence of the electrical characteristics, the better C-V characteristics and the lower D_{it} obtained at the lower ALD temperature can be explained by the As_2O_3 and Ga_2O_3 passivation of the HfO_2/InGaAs interfaces, which is consistent with a reported theoretical result on the effective passivation of III-V MOS interfaces by trivalent oxides.

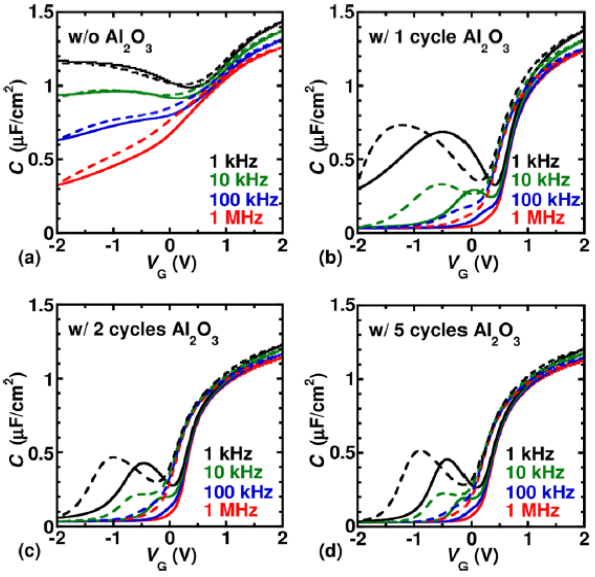

Figure 2.17 C-V characteristics of Au/HfO_2 (100 cycle: 10 nm)/InGaAs capacitors (a) without Al_2O_3 inter-layer and with (b) 1 cycle (0.1 nm), (c) 2 cycle (0.2 nm), (d) 5 cycle (0.5 nm) Al_2O_3 inter-layer, respectively. Solid and broken curves correspond to the gate voltage sweep from V_{acc} to V_{inv} and from V_{inv} to V_{acc}, respectively. [36]

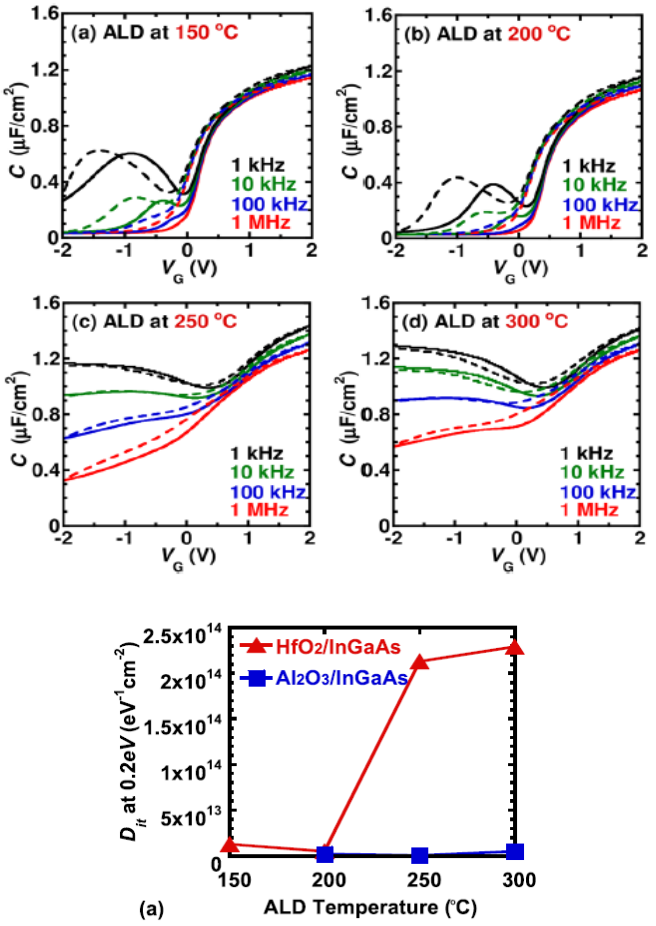

Figure 2.18 (a) GeO_2 thickness on Ge and on SiO_2/Si as a function of annealing temperature,(b) Schematic view of GeO desorption in GeO_2/Ge stack [37].

The effect of treatment on surface is reported that the decrease in interface trap density (D_{it}) in Al_2O_3/InGaAs metal oxide semiconductor (MOS) capacitors by using electron cyclotron resonance plasma nitridation of the InGaAs surfaces. The plasma nitridation process is observed to form a nitrided layer at the InGaAs surface which results with a minimum D_{it} value of $2.0x10^{11}$ cm^{-2} eV^{-1}. Plasma nitridation is more effective than sulfur passivation as shown in figure 2.19. [38] Another report about H_2 and N_2 plasma treatment is that in-situ hydrogen or nitrogen plasma surface cleaning procedures is processed by alternating cycles of nitrogen plasma and trimethylaluminum (TMA) prior to growth. This allow for highly scaled dielectrics with equivalent oxide thicknesses down to 0.6 nm and interface trap densities that are below $2.5x10^{12}$ cm^{-2} eV^{-1} near midgap. It is shown that the benefits of the nitrogen plasma surface cleaning procedure are independent of the specific dielectric as shown in figure 2.20.

Finally, the effect of H_2O and O_3-based ALD high-k dielectric films on GaAs substrate was researched. In comparison with the H_2O-based ALD process, the O_3-based process produced a large amount of elemental As and Ga–O related bonds near the HfO_2/GaAs interface due to its stronger oxidizing power as shown in figure 2.21. High interface state and border trap densities of the O_3-based sample degraded the low-field electrical stability, which was confirmed by the capacitance and leakage current measurements under various voltage-stressing conditions. However, in terms of high-field

stability, the O_3-based sample showed a much stronger resistance to stress-induced trap generation than the H_2O-based sample.

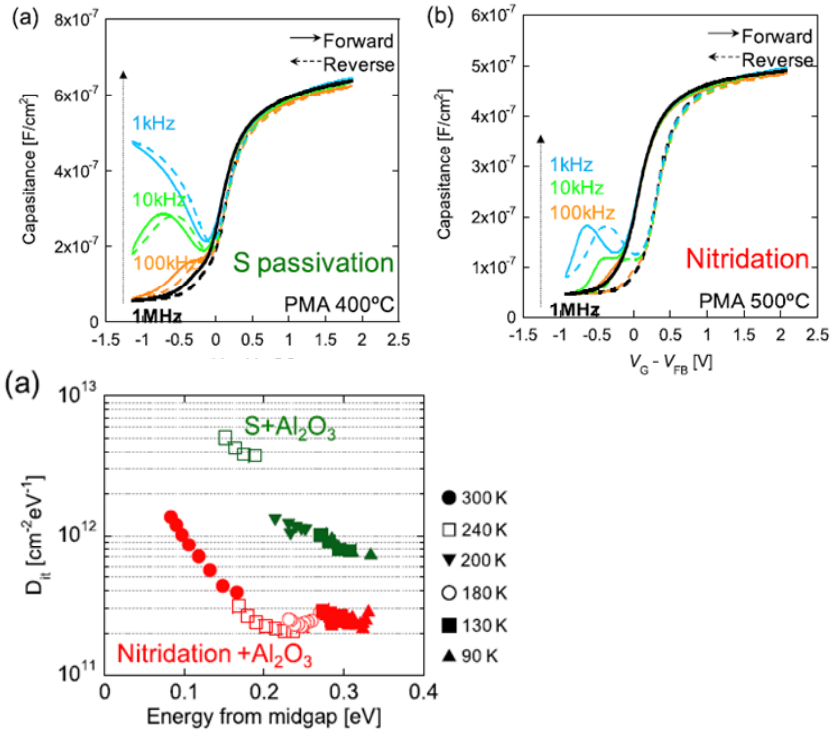

Figure 2.19 C-V characteristics at room temperature of ALD-Al_2O_3/InGaAs MOS capacitors with (a) sulfur passivation and (b) nitridation. The frequency dispersion and hysteresis are shown. [38].

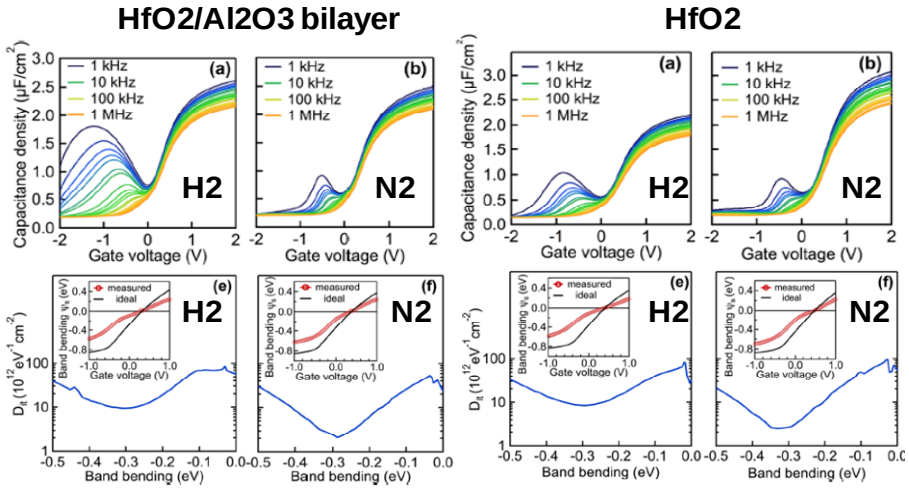

Figure 2.20 (Left) $In_{0.53}Ga_{0.47}As$ MOSCAPs with HfO_2/Al_2O_3 bilayers. (Right) $In_{0.53}Ga_{0.47}As$ MOSCAPs with HfO_2 dielectrics with CV characteristics as a function of frequency in upper layer, and the extracted band bending as a function of gate voltage in down layer [39].

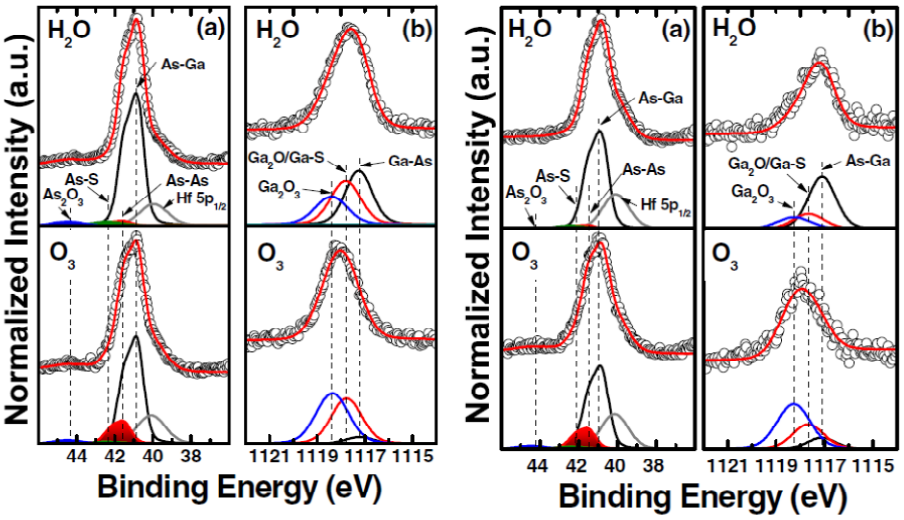

Figure 2.21 (a) GeO_2 thickness on Ge and on SiO_2/Si as a function of annealing temperature,(b) Schematic view of GeO desorption in GeO_2/Ge stack [40].

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3. Experiments and Analyses

3.1. Atomic layer deposition of high-*k* dielectrics

The dielectric films were usually grown on 2x2 cm^2 size of substrates using a thermal atomic layer deposition (ALD) reactor (CN1 Corp., Suwon, Korea). Argon (Ar, purity 99.999%) was used as a carrier and a purging gas. In most of the experiments the substrates were p-type silicon(14-22 Ohm-cm), but also Ge and GaAs substrates were also used.

Figure 3.1 shows a schematic diagram of the thermal ALD system used in these experiments. The ALD system has traveling-type chamber and four precursors (or canisters) and ozone generator. By composing process sequence, four kinds of other precursors (Hf, Si, Zr and Al) can be used independently for various dielectric films. The ozone generator can supply O_2 and N_2 gas with various ozone (O_3) concentrations from 0 to ~300 g/Nm^3.

The metal source was vaporized from external canisters according to the vapor pressure of each precursor. In the case of hafnium (Hf) and zirconium (Zr) precursors, because the vapor pressures are properly low at room temperature, these sources were heated at 60^oC and carried by Ar gas. Silicon (Si) and aluminum (Al) precursors were cooled at 5^oC due to the high vapor pressure at room temperature and the vaporized source gases were traveled into the chamber. In this work, Hf precursor was mainly used

as gate oxides when the MOS capacitor was fabricated.

In this work, the HfO_2 films were deposited directly on hydrofluoric acid (HF) cleaned Si wafers by ALD at a wafer temperature of 270-280^oC. $Hf[N(C_2H_5)(CH_3)]_4$ and $SiH[N(CH_3)_2]_3$ and ozone (typical concentration of 170 g/m^3) were used as the Hf-/Si- precursors and oxygen source, respectively, in the deposition of the HfO_2 and HfSiO gate dielectric layers. The standard precursor pulse - precursor purge – ozone pulse – ozone purge time was 3 – 20 – 3 – 10 sec in HfO_2 and 3 – 15 – 3 – 10 in SiO_2, respectively, which was confirmed as within the well saturated ALD window. Physical and chemical properties of the two precursors are summarized in Table 3.1, and process conditions are summarized in Table 3.2.

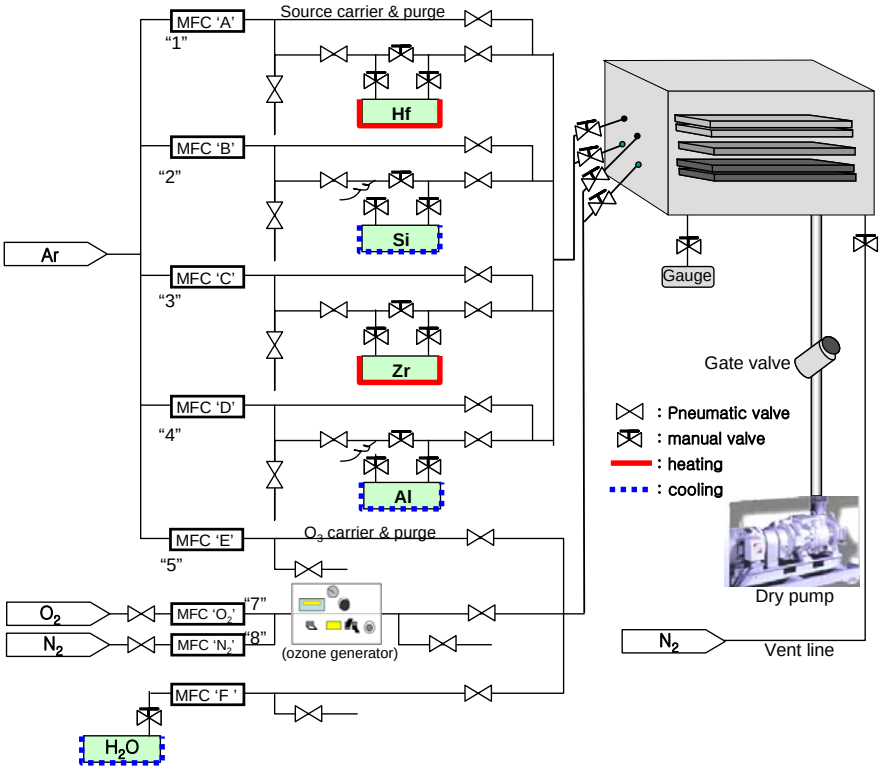


Figure 3.1 Schematic diagram of the thermal ALD system

	TEMAHf : Tetrakis(ethyl-methyl-amino) hafnium	TMA : Trimethylaluminium	Tri-DMAS :Tris[Dimethyl Amino] Silane
Chemical Formula	$Hf[N(CH_3)C_2H_5]_4$	$Al_2(CH_3)_6$	$SiH[N(CH_3)_2]_3$
Purity(%)	99.9999(6N)	99.9999(6N)	99.9999(6N)
Physical Status	Liquid at R.T.	Liquid at R.T.	Liquid at R.T.
Color	Colorless Light yellow	Colorless	Colorless
Molecular Weight (g/mol)	410.95	144.18	161.3
Boiling point(℃)	79	125	145
Density	1.324g/mol	0.752g/L	0.833g/mol

Table 3.1 Physical and chemical properties of TEMAHf, TMA, and tri-DMAS.

		HfO_2		Al_2O_3		SiO_2	
Metal precursor		$Hf[N(CH_3)C_2H_5]_4$		$Al_2(CH_3)_6$		$SiH[N(CH_3)_2]_3$	
Oxidant		O_3 or H_2O					
Growth temperature(℃)		280					
Carrier Ar flow rate(sccm)		200					
Cannister temperature(℃)		60		5		5	
Line temperature(℃)		90					
Feeding Time(s)	Precursor pulse	3		1		3	
	Precursor purge	20		10		15	
	Oxidant	O_3	H_2O	O_3	H_2O	O_3	H_2O
	Oxidant pulse	3	3	3	3	3	3
	Oxidant purge	10	20	10	20	10	20

Table 3.2 Process conditions of thermal ALD grown HfO_2, Al_2O_3, and SiO_2.

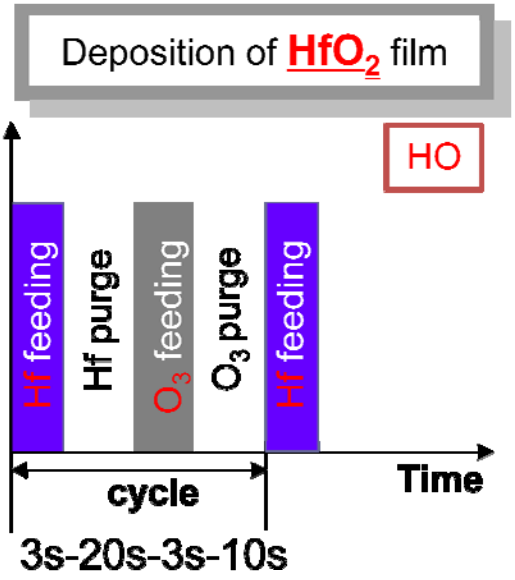


Figure 3.2 Schematic diagram of composition of the ALD cycle

3.2. Film characterization

The thickness of dielectric film on Si, Ge and GaAs were determined at center area of the 2x2 cm^2 substrate using an ellipsometer (L116D, Gaertner Corp., US) with a single light source (633 nm) and spectroscopic ellipsometry (SE; M2000, Woollam Corp., US) with wide light source (193 ~ 1690 nm). The physical thicknesses of metal films including dielectric films were confirmed by the layer density and the vertical image of the films.

The layer density of the dielectric films as well as metal films was determined by X-ray fluorescence spectroscopy (XRF; Themoscientific, ARL Quant'x).

The chemical bonding states of the films were examined by X-ray photoelectron spectroscopy (XPS). The XPS measurements were carried out using a Kratos AXIS-HSi system equipped with a Mg Kα source (1253.6eV) for the excitation of photoelectrons. The positions of all peaks were calibrated to the surface carbon C 1s peak at 284.5eV.

The atomic concentrations and depth profiles of the films were analyzed by Auger electron spectroscopy (AES). The AES measurements were carried out using a Perkin-Elmer PHI 660 system.

The crystalline structure of the films was examined by glancing angle incidence X-ray diffraction (GAXRD, PANalytical, X'pert Pro).

The microstructure and vertical image of the films was analyzed using a high-resolution transmission electron microscopy (HRTEM; Tecnai F20, field-emission, 200kV), Fast Fourier Transformation (FFT), and the electron energy loss spectroscopy (EELS ; GIF Tridiem 863).

3.3. Fabrication of MOS capacitor

Firstly, the high-*k* gate dielectrics (HfO_2 or HfSiO) with various thicknesses films were deposited directly on hydrofluoric acid (HF)-cleaned Si wafers by ALD at a wafer temperature of 270^{o}C. When thermal budget on the high-*k* dielectrics was needed, post deposition annealing (PDA) was performed at various temperatures in a N_2 ambient using a rapid thermal annealing (RTA) process for 30 sec. Various top metal electrodes, such as platinum (Pt) and titanium nitride (TiN), were sputtered on the dielectric films using a shadow mask to define the gate electrodes. Finally, forming gas annealing (FGA) was performed in the mixture gas of N_2 (95%) and H_2 (5%) at 450^{o}C for 10min.

Figure 3.3 shows the schematic diagram of a shadow mask and MOS capacitor used in this work. Various metal layers between Pt and gate oxide was in-situ inserted for investigating electrical property. Size of a dot

deposited on samples using the shadow mask was about 90,000 ~ 100,000 μm^2.

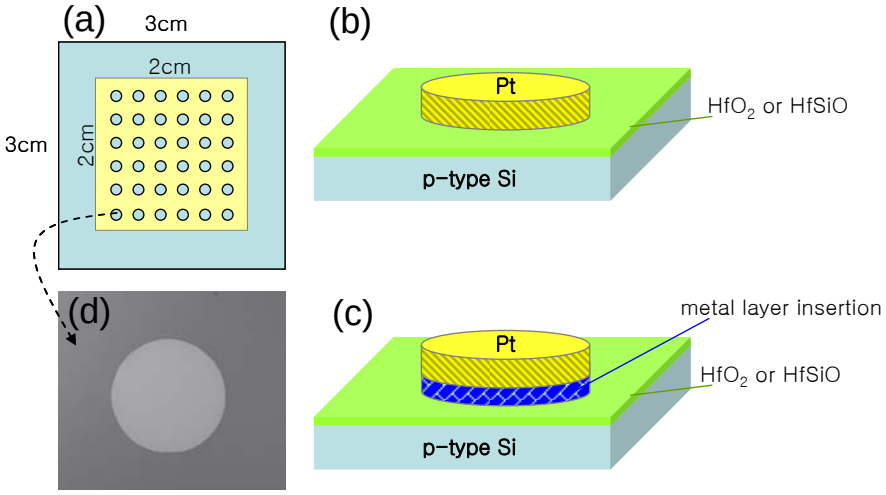


Figure 3.3 Schematic diagram of (a) a shadow mask used in this work and (b) Pt electrode on the dielectrics and (c) other metal insertion between Pt and dielectrics on Si substrate and (d) scope image of a dot.

3.4. Electrical measurements

A HP 4194A Impedance/Gain-Phase Analyzer for Capacitance-Voltage (C-V) curve and a HP 4140B pA Meter/DC Voltage Source for I-V characterization were used in the MOS capacitor devices.

Bias temperature instability (BTI) and Interface trap density (D_{it}) from the MOS capacitor are also measured by using a Hewlett-Packard (HP) 4155 semiconductor parameter analyzer and a HP 4284 LCR meter system. The measurement system and schematics of BTI and D_{it} measurement in MOS capacitor devices were illustrated in Figure 3.4 and 3.5. During the BTI measurements, a constant voltage (or field) stress was applied to the gate of MOS capacitor, while the Si substrate was grounded. The gate voltage (V_g) was swept from -1 to 1 V at 1,3,5,10,22,47,100,216,465,500sec during 500sec at 100 kHz for measuring C-V. However, the inversion condition can hardly be achieved from the usual MOSCAP device due to the lack of source and drain, so the depletion/accumulation condition must be used to evaluate the BTI characteristics. Therefore, V_{FB} values extracted from the C-V curves after gate bias stress were used instead of V_{th} values in MOSFET.

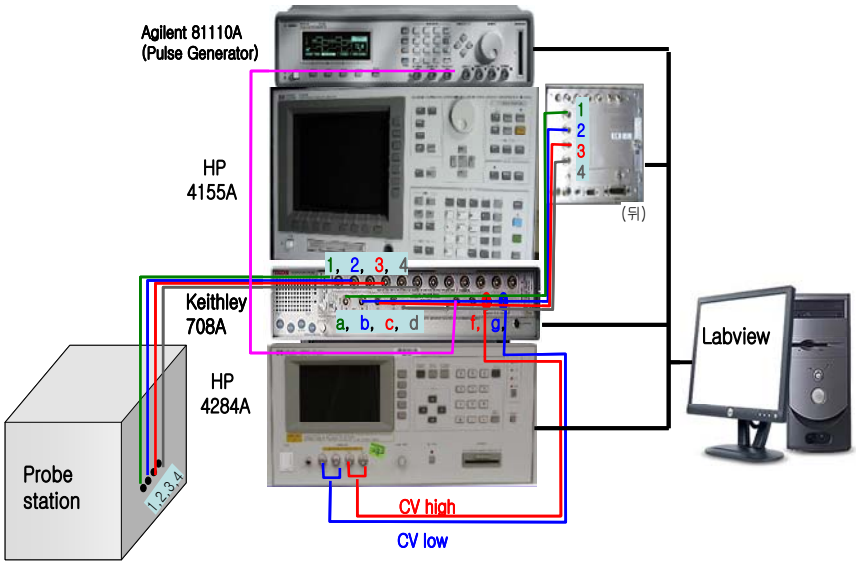


Figure 3.4 BTI and D_{it} measurement system in these experiments

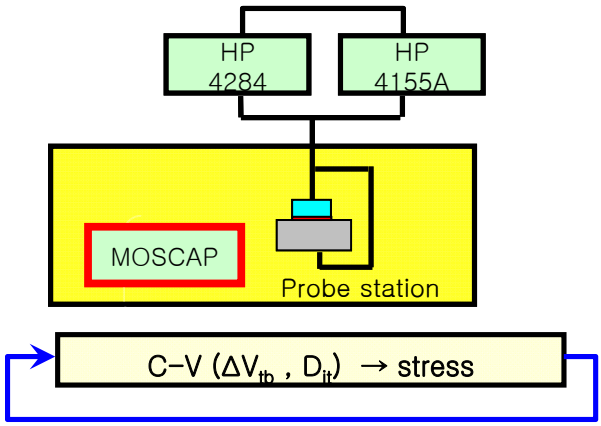


Figure 3.5 Schematic diagram of BTI and D_{it} measurement in MOS capacitor devices.

4. Results and Discussions

4.1. ALD capping layer for V_{FB} modulation

4.1.1. Introduction

HfO_2 gate dielectrics have been under the spotlight for a considerably long time now, long enough to be in use at industrial levels [1]. There are still some problems that need to be solved though, such as charge trapping, insufficient reliability, and the abnormally high threshold voltage (V_{th}) perhaps due to Fermi level pinning. Furthermore, as scaling the EOT, the new problems arises that V_{FB} value of high-k/metal gate stack transistor is not controlled and fell down regardless of the type of metal electrode in small EOT region which is called V_{FB} roll-off. Controlling the reasonable V_{th} value is key technology for stable operating the CMOSFET device. Throughout the years, much research has been conducted to improve the properties of HfO_2, starting from research on the intrinsic properties of the material itself all the way to studies on the integration of thin films into semiconductor devices.

To reduce the abnormally high V_{th} value of Hf-based gate dielectrics, several approaches have been reported.

Recently, capping a rare earth metal (oxide) layer on Hf based dielectrics have received great attention because it can effectively decrease the V_{th} value in n–type metal oxide semiconductor field effect transistors

(nMOSFET) [2-4]. In addition capping Al_2O_3 on Hf based oxides have also been reported to reduce the V_{th} in p-type MOSFET (p-MOSFET) [5-6]. Some of theses reports used the sputtering tools for rare earth metal deposition. However, this metal layer is need to be ultra thin and uniform over the whole wafer, in this respect, sputtering of this metal layer is difficult to apply in industry.

The capping layer needs to be extremely thin and uniform to achieve the desired V_{th} control effect over a wide wafer, not to increase the capacitance equivalent oxide (CET) values, and no degradation of reliability. Atomic layer deposition (ALD) is particularly suitable for such purposes. However until now, reports for appropriate ALD precursors for rare earth metal oxide deposition for V_{th} modulation and an in-depth study are still required. Therefore sputtering systems have been generally used as the major deposition technique for nMOS V_{th} modulation layers [2-4]. Because it is difficult to synthesis the precursor containing Lathanide metal, so there are only few kinds of precursors with some ligands. Moreover, the Lathanide precursors are mostly known that it is hard to handle since it has unstable property of low vapor pressure which is required to bublling at high temperature with degradation of stability, and hard to optimize the ALD condition. (This is not formally reported, but authors who met in conference said handling the Lathanide precursors is difficult in common). In addition, the mechanism for the V_{th} modulation is still rather unclear although there

have been several attempts to explain the origin of it. Therefore, one of the most promising approaches to modulate the V_{th} is to adopt ALD capping layers, which is being tipped off as a solution due to its superior thickness controllability and uniformity, along with the fact that there is no plasma damage [5, 7].

In this study, the effects of the relative position and thickness of ALD grown Al_2O_3, SrO, and La_2O_3 capping layers with HfO_2 and ZrO_2 gate dielectrics on flat band voltage (V_{FB}) modulation of metal-insulator-semiconductor (MIS) capacitor are studied.

4.1.2. Experimental

Various oxides (Al_2O_3, SrO, and La_2O_3) were deposited via ALD as the top and bottom capping layers of the HfO_2 gate dielectrics. To investigate the effect of the location of the capping layer on V_{FB} shift, the capping layers were placed at two different locations. In this paper, "Top M_xO_y" refers to the metal oxide capping layer on top of the HfO_2, and "Bottom M_xO_y" refers to the layer interposed between the HfO_2 (Fig. 1 (a)) and Si substrate. The HfO_2 and Al_2O_3 thin films were grown by ALD on a HF cleaned p-type Si substrate at 280^oC using $Hf[N(C_2H_5)(CH_3)]_4$; TEMAH(Tetrakis-ethylmethylamino hafnium) and $Al(CH_3)_3$; TMA(Trimethyl aluminum) as Hf and Al precursors, respectively. O_3 (170g/m^3) was used as the oxygen source. The ALD SrO thin films were grown using $Sr(iPr_3Cp)_2$; Bis(1,2,4-trisisopropylcyclopentadienyl) strontium with O_3 (400g/m^3) at 370 ^oC, and

the ALD La_2O_3 thin films were grown using $La[N(SiMe_3)_2]_3$; Tris[bis(trimethylsilyl)amino]lanthanum with H_2O at 310 ^oC. Pt was used as the top electrode, which was deposited by sputtering as well as defined the area through shadow mask. The forming gas annealing (FGA) was performed at 400 ^oC for 10 min. in a N_2 95% / H_2 5% atmosphere. The capacitance-voltage (C-V) curve and leakage current property of the MIS capacitors were measured using a Hewlett-Packard 4194 impedance analyzer and a Hewlett-Packard 4140B parameter analyzer, respectively. The chemical bonding status of the various high-k gate stacks was examined by X-ray photoelectron spectroscopy (XPS). The XPS measurements were carried out using a ThermoVG Sigma Probe system equipped with a monochromatic *Al- K* source (1486.7eV).

4.1.3. ALD La_2O_3 capping layer

Figure 4.1 shows the original and normalized capacitance-voltage (C-V) curves of HfO_2 dielectric films with Top and Bottom La_2O_3 capping layers. The thickness of HfO_2 film was fixed as 3 nm. The thickness of ALD La_2O_3 capping layer was increased as 1, 3, 5, 10 Å, respectively. As an increase of thickness of La_2O_3 capping layer, the accumulation capacitance was decreased due to the increase of total oxide thickeness. There was no degradation of property in C-V curve, for example, hysteresis voltage, slope of C-V curve and hump in the region of inversion. The interesting thing was that V_{FB} shift of C-V curves was represented in the case of Bottom La_2O_3

layer. In the case of Top La_2O_3 layer, the C-V curves did not shift at all. This means the reason of V_{FB} shift is mainly affected in interface between HfO_2 dielectric film and Si substrate. In addition, the amount of V_{FB} shift was increased according to the increase of thickness of Bottom La_2O_3 layer, and saturated at critical thickness of La_2O_3 layer. The direction of V_{FB} shift of C-V curves was negative which means formed the positive charge by La_2O_3 layer. The mechanism or origin of V_{FB} shift will be discussed later in detail

Figure 4.2 indicate a function of V_{FB} values extracted from C-V curves of Top and Bottom La_2O_3 layer with HfO_2 film. As shown in previous C-V curves, Top La_2O_3 caused negligible V_{FB} shift, while Bottom La_2O_3 layer represents dramatic V_{FB} shift to the negative direction, and the amount of V_{FB} shift was saturated at La_2O_3 thickness of 5 Å, and the shift amount was 0.37V.

Figure 4.3 shows leakage current density J_g at -1V vs. CET plots of Top and Bottom La_2O_3 layer with HfO_2 film. In figures, there are two lines; black one is the reference SiO_2 and the other line is reference HfO_2 line, and theses are simulated results. [9] Compared to the HfO_2, Top La_2O_3 induced the increase of CET with the decrease of J_g, while Bottom La_2O_3 caused the degradation of insulating property. Top La_2O_3 can be explained by the increase of the total oxide physical thickness, and bottom La_2O_3 case is due to the poor interfacial layer. ALD La_2O_3 was deposited as La silicate which has lower k-value than HfO_2, because La precursor formed Si-containing

silyl ligand. The reason why the data is not exactly fit linearity is that we using the shadow mask when we define the gate electrode, gate electrode which is defined shadow mask has some of the slope, So it is hard to get the exact area of MOSCAP. However, it is also performed repeatability test, always identical result was obtained.

Figure 4.4 represents XPS profiles of O 1s, Hf 4f, and La 3d peaks of Top and Bottom La_2O_3 layer with HfO_2 film. There is no difference between Top and Bottom La_2O_3 layer which means La_2O_3 layer did not affect the bonding state of HfO_2 film, and no difference whether La_2O_3 layer is located upper HfO_2 or under HfO_2 film.

In addition, it is reported that La_2O_3 are easily hydrated and reacted with the other layers. [11] So it is expected that it can cause the increase of RMS roughness. Therefore, in order to investigate the interfacial reaction, the RMS roughness of both Top and Bottom La_2O_3 with HfO_2 oxide layers (thickness was ~5 nm) was analyzed. Figure 4.5 shows AFM 3-dimensional images and root mean square (RMS) roughness of surface of Top and Bottom La_2O_3 layer with HfO_2 film. There was no difference between the two samples. The RMS roughness value is negligible reflecting that very smooth and uniform films were deposited.

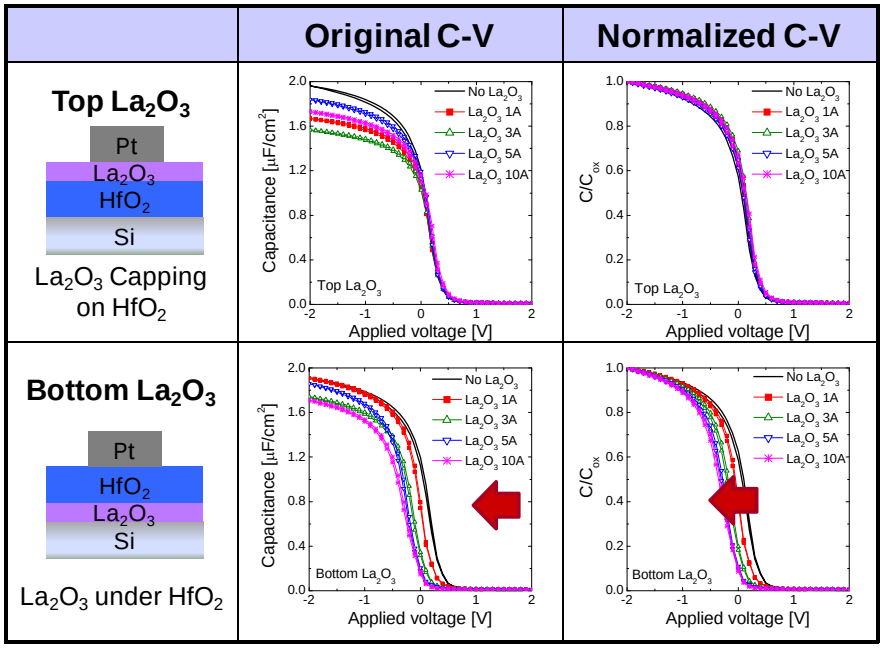


Figure 4.1 The original and Normalized C-V curves of Top and Bottom La_2O_3 capping layers with HfO_2 thin films

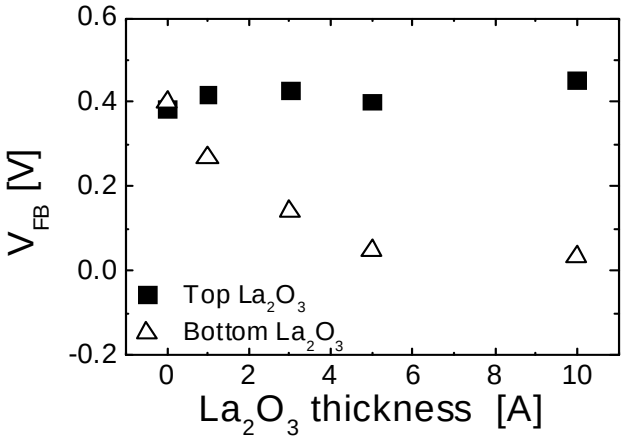


Figure 4.2 A function of Top/Bottom La_2O_3 thickness and V_{FB} values extracted from C-V curves

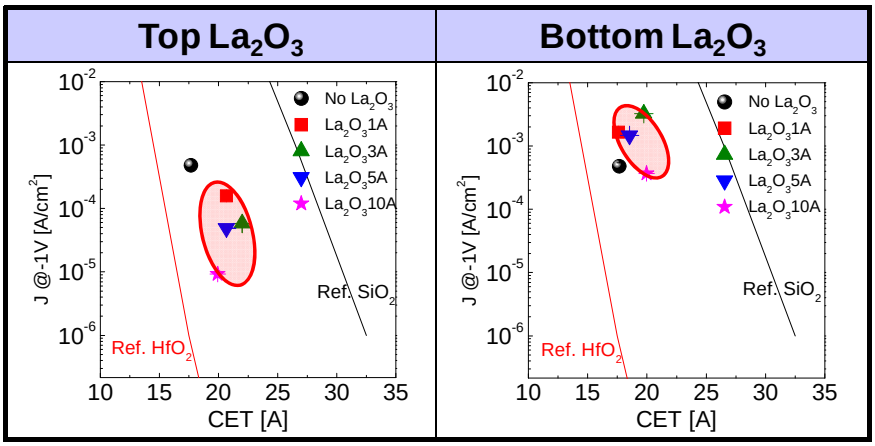


Figure 4.3 J_g. vs CET graphs of Top and Bottom La_2O_3 with HfO_2 films with the lines of universal reference of SiO_2 and HfO_2 films

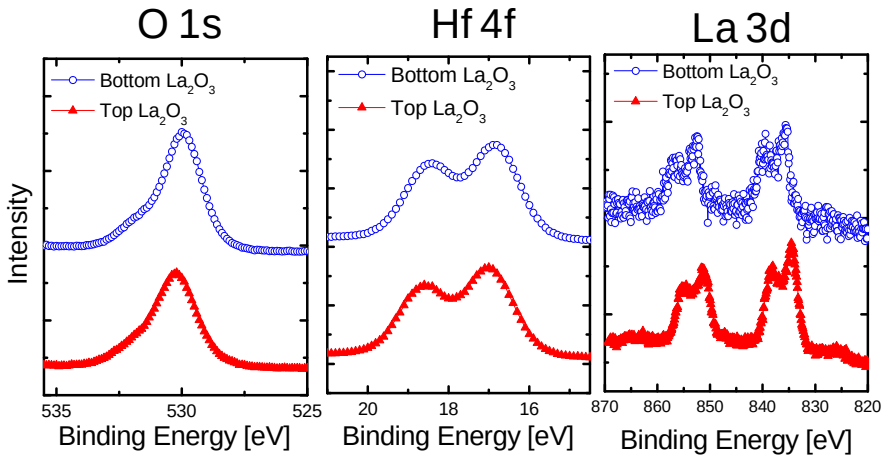
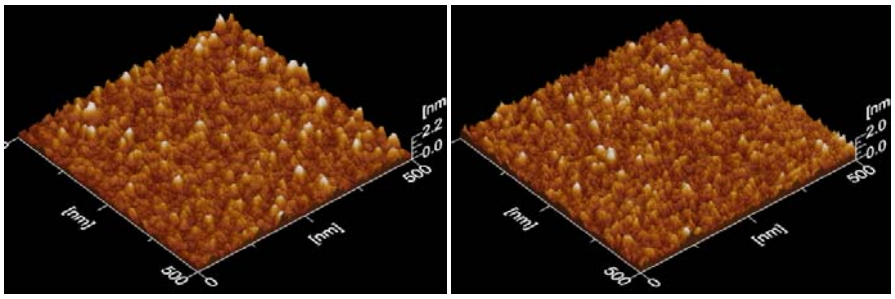


Figure 4.4 XPS profiles of O 1s, Hf 4f, and La 3d peaks of Top and Bottom La_2O_3 layer with HfO_2 film.



Top La_2O_3
RMS roughness
0.225nm

Bottom La_2O_3
RMS roughness
0.228nm

Figure 4.5 AFM 3-dimensional images and RMS roughness of surface of Top and Bottom La_2O_3 layer with HfO_2 film.

ALD La_2O_3 capping layer effect on Hf-based high-k dielectrics was also investigated. Top and Bottom La_2O_3 layer of 1, 3 nm with HfO_2, $HfZrO_x$, and ZrO_2 films, which total oxide thickness was 4 nm, and La_2O_3 films were tested. The original and normalized C-V curves of Top and Bottom La_2O_3 capping layers with HfO_2, HZO_x and ZrO_2 thin films in the figure 4.6. All three cases, Bottom La_2O_3 layer was effective to V_{FB} shift to the negative direction which is identical with V_{FB} value of La_2O_3 film itself. In addition, 1nm of Bottom La_2O_3 layer was sufficient to V_{FB} shift of saturated value. On the other hand, Top La_2O_3 layer did not affect on V_{FB} value even in thickness of 3 nm. This means the interfacial layer between high-k dielectric and Si substrate is a key of V_{FB} modulation. In addition, there was no significant difference according to the kinds of high-k dielectric, because of its characteristics are similar to HfO_2 and ZrO_2.

Figure 4.7 shows the variations of V_{FB} values and delta V_{FB} extracted from C-V curves of figure 4.6 with regard to the effect of Bottom La_2O_3 layer according to the high-k dielectrics; ZrO_2, HZO_x, and HfO_2 films. As the Zr contents increase, V_{FB} shows more negative shift due to positive fixed charges of ZrO_2 itself compared with HfO_2. [6] However, for the case of Bottom La_2O_3 layer, the difference of V_{FB} values between with and without La_2O_3 layer are decrease, as Zr contents increase. V_{FB} shift by using the La_2O_3 layer is larger in HfO_2 films compared to the $HfZrO_x$ and ZrO_2.

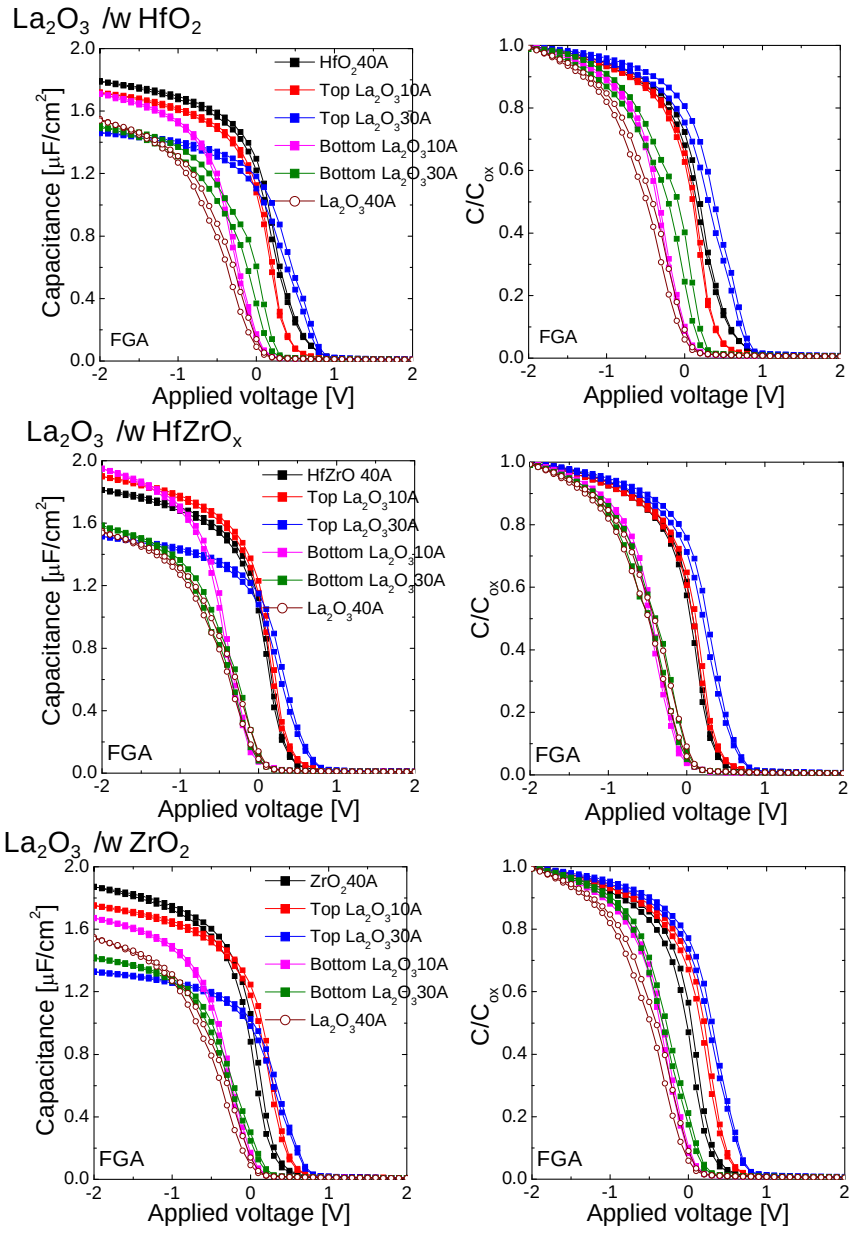


Figure 4.6 The original and normalized C-V curves of Top and Bottom La_2O_3 capping layers with HfO_2, HZO_x and ZrO_2 thin films

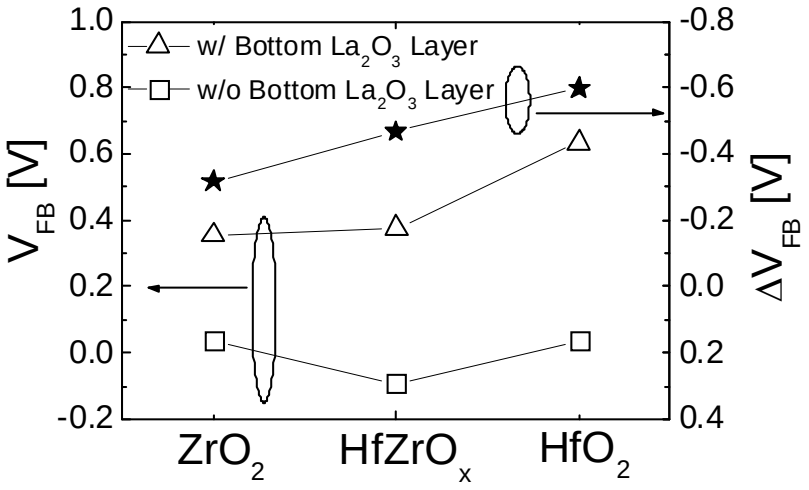


Figure 4.7 Variations of V_{FB} and delta V_{FB} the effect of Bottom La_2O_3 layer according to the high-k dielectrics; ZrO_2, HZO_x, and HfO_2 films

The effect of high temperature annealing whether to cause the diffusion of Top La_2O_3 layer, and thermal budget provided against gate fist process which contains high temperature annealing was examined. Figure 4.8 represents the original and normalized C-V curves of Top and Bottom La_2O_3 capping layers with HfO_2 thin films with respect to annealing effect in condition of 600 ^oC 30s under N_2 atmosphere. It was expected diffusion or intermixing of capping layer with HfO_2 which can cause changed properties, however the direction and amount of V_{FB} shift were still maintained. This means La_2O_3 capping layers with HfO_2 thin films could endure a thermal budget about 600 ^oC.

Figure 4.9 shows J_g. vs CET graphs of Top and Bottom La_2O_3 with HfO_2 films in accordance with annealing effect. Post deposition annealing results overall increase of CET and poor leakage characteristics as silicate formation by promotion the reaction with Si substrate. [11] Among them, Top La_2O_3 10Å represents best insulator propert both of before and after annealing. It means interface between HfO_2 and Si substrate is most stable and Top La_2O_3 layer could propect the degradation by thermal budget.

XPS depth profile of La 3d peaks of Top and Bottom La_2O_3 with HfO_2 films in terms of annealing effect(600 ^oC 30s N_2 atmosphere) in figure 4.10. The doublet of La 3d peak is observed on the surface in the case of Top La_2O_3, it is observed according to the sputtering to the substrate in the case of Bottom La_2O_3. It accounts for no diffusion of La_2O_3. Even after the

annealing, the result was same except decrease of noise. Thermal budget about 600 ^{o}C did not induce the diffusion of La_2O_3.

Figure 4.11 shows the valence band measured by XPS of 5, 10 Å thick Top and Bottom La_2O_3 with HfO_2 films and HfO_2 films, the valence band offset(VBO) which optained by point meets two tangent lines of inflection point, are listed in table 4.1. As the La_2O_3 layer thickness was increased, the VBO was decrease in both Top and Bottom case. In addition, the VBO values are lower in the case of Bottom La_2O_3. This suggest the possibility of the barrier height was lowered by La_2O_3 layer and in the case of Bottom La_2O_3, can coincide with higher leakage current.

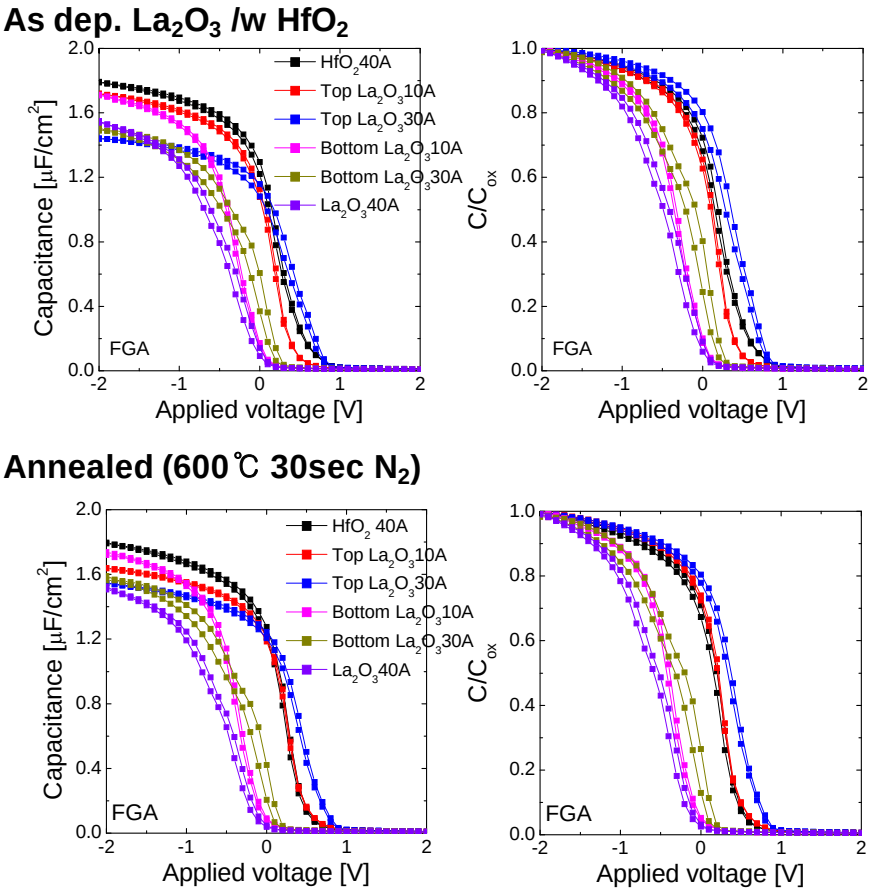


Figure 4.8 The original and Normalized C-V curves of Top and Bottom La_2O_3 capping layers with HfO_2 thin films with respect to annealing effect (600 °C 30s N_2 atmosphere)

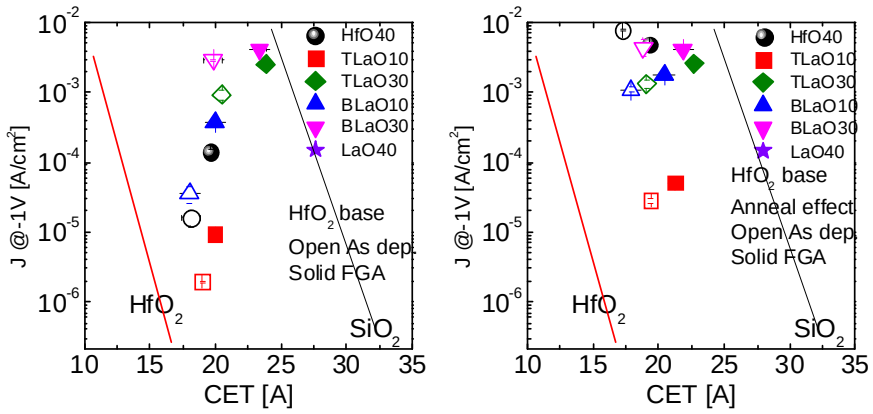


Figure 4.9 J_g. vs CET graphs of Top and Bottom La_2O_3 with HfO_2 films in accordance with annealing effect (left is before, right is after annealing)

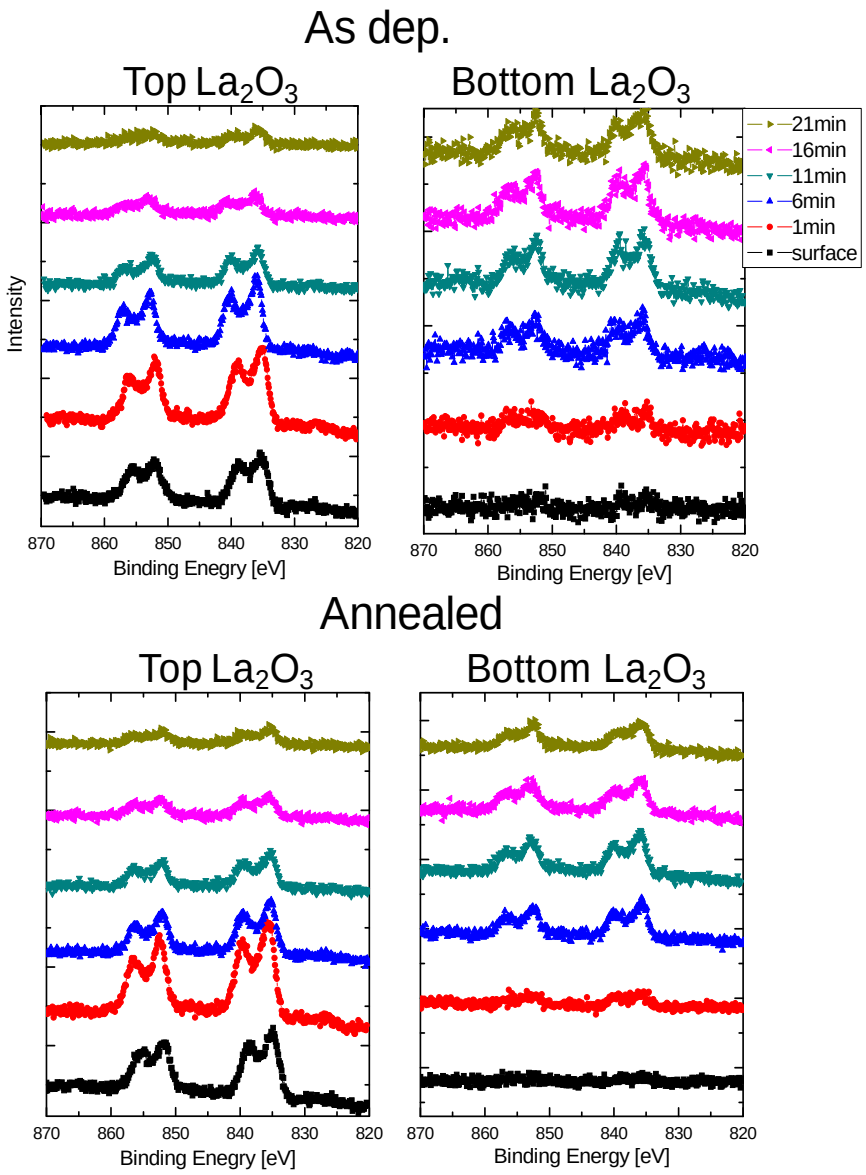


Figure 4.10 XPS depth profile of La 3d peaks of Top and Bottom La_2O_3 with HfO_2 films in terms of annealing effect.(600°C 30s N_2 atmosphere)

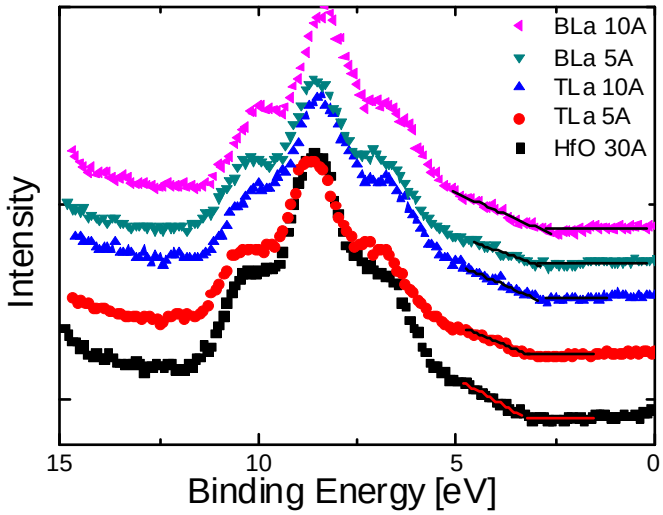


Figure 4.11 Valence band measured by XPS of Top and Bottom La_2O_3 with HfO_2 films and HfO_2 films

Sample stack	VBO [eV]
Bottom La_2O_3 10A	2.42
Bottom La_2O_3 5A	2.63
Top La_2O_3 10A	2.57
Top La_2O_3 5A	2.92
HfO_2 30A	3.01

Table 4.1 Valence band offset(VBO) measured by XPS of Top and Bottom La_2O_3 with HfO_2 films and HfO_2 films

The modified bias temperature instability(BTI) property was examined. In the laboratory, it is hard to fabricate the MOSFET, so it is studied by MOSCAP in the top of figure 4.12. It is confirmed that the BTI character is same at both MOSFET and MOSCAP(nMOS PBTI at transistor and pMOS PBTI at MOSCAP). The degradation is not occurred by positive bias stress, since there is no electron source such as n+ of transistor. Transistor can measure nMOS PBTI, but it is impossible in MOSCAP. Therefore it was measured the nMOS NBTI by hole. For confirming degradation effect by electron, it is needed to measure the pMOS PBTI. The constant voltage stress positive and negative bias stress was induced for 1, 10, and 100sec. As mentioned above, NBTI shows degradation.

Therefore, modified BTI(Constant voltage stress at 15MV/cm negative bias stress) results by delta V_{FB} from C-V curves according to the stress time of Top and Bottom La_2O_3 with HfO_2 films in figure 4.13. [12] La_2O_3 represents smallest degradation, and Top La_2O_3 has gotten worse than HfO_2. On the contrary, Bottom La_2O_3 has improved with a similar level of La_2O_3.

Figure 4.14 shows a temperature dependency of modified BTI(Constant voltage stress at 15MV/cm negative bias stress) results according to the stress time of Top and Bottom La_2O_3 with HfO_2, HfO_2 and La_2O_3 films. Temperature range was 25 degree intervals from 25 to 125. Trend is separated whether HfO_2 is located at interface or not. HfO_2 and Top La_2O_3 are improved from 25 to 50^{o}C, but degradation was started from 75^{o}C. Delay time is long from few

um to few seconds, so recovery is favorable than degradation by increase of temperature. On the other hands, the go-around phenomenon to the positive direction was started from 75°C. This phenomenon was due to avalanche effect [12].

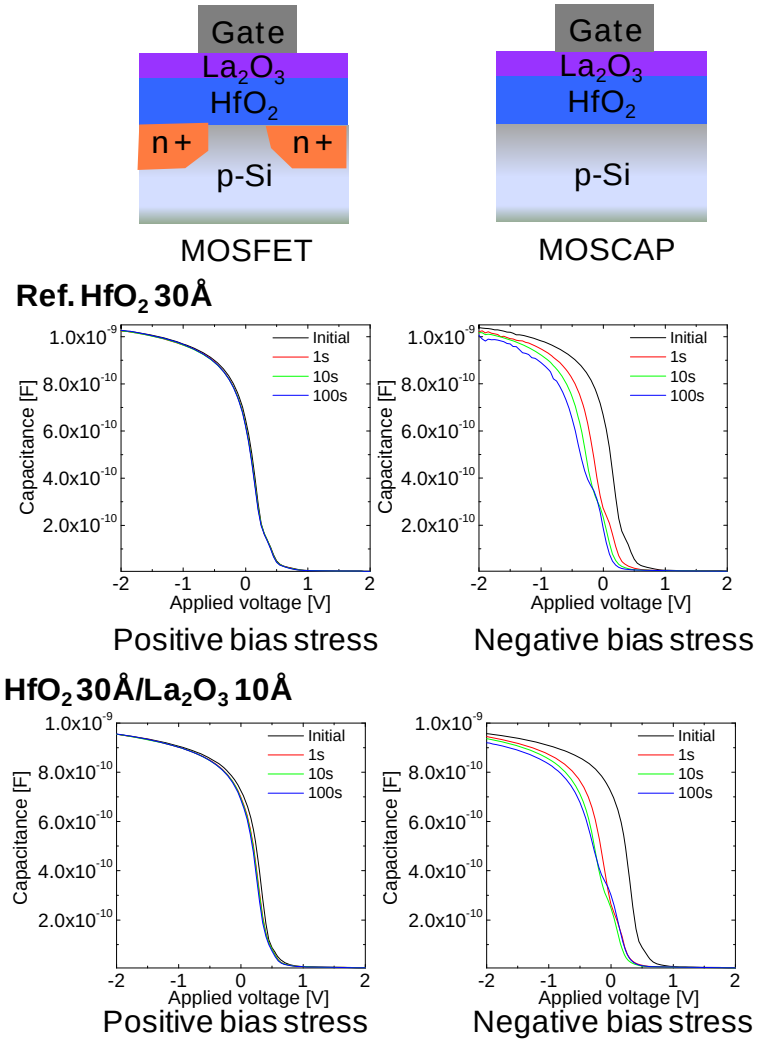


Figure 4.12 Modified BTI(CVS; Constant voltage stress) results of Top and Bottom La_2O_3 with HfO_2 films

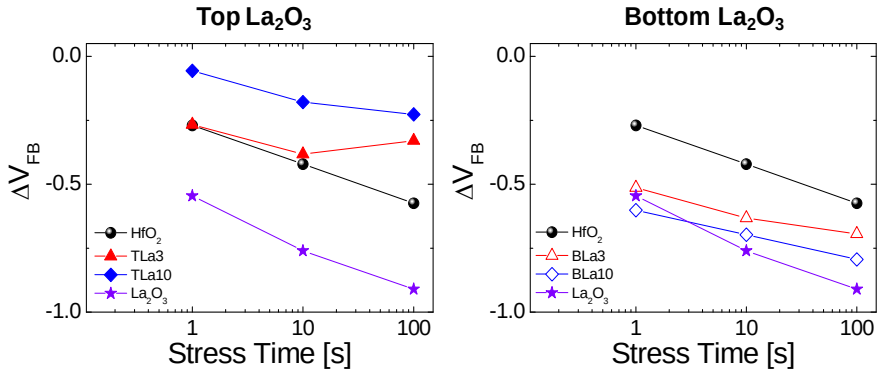


Figure 4.13 Modified BTI(Constant voltage stress at 15MV/cm negative bias stress) results according to the stress time of Top and Bottom La_2O_3 with HfO_2 films

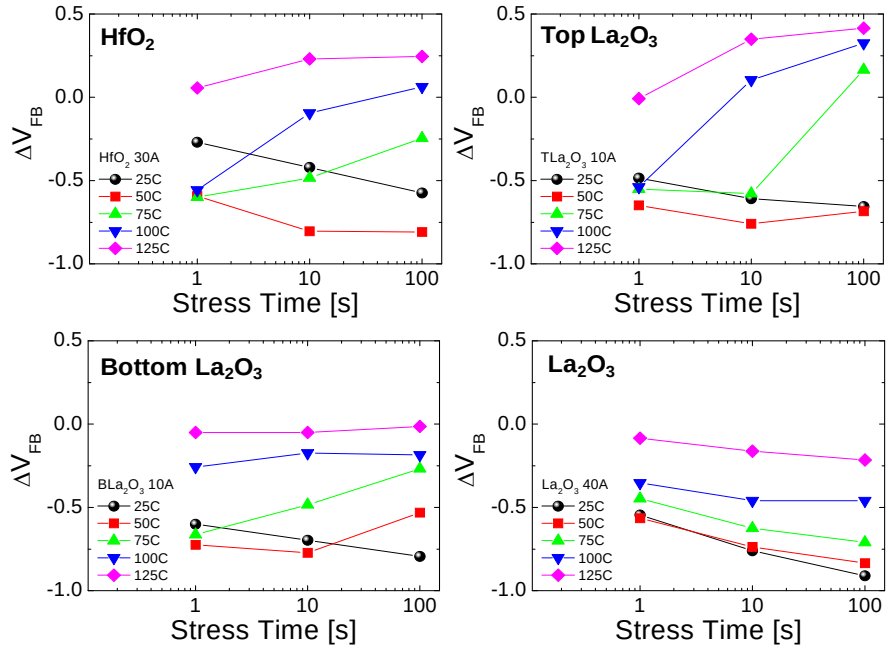


Figure 4.14 Temperature dependency of modified BTI(Constant voltage stress at 15MV/cm negative bias stress) results according to the stress time of Top and Bottom La_2O_3 with HfO_2, HfO_2 and La_2O_3 films

4.1.4. ALD Al_2O_3 capping layer

Next, ALD Al_2O_3 capping layer was adopted to Hf-based high-k dielectrics for pMOS application. Figure 4.15 shows the focused in V_{FB} region of normalized capacitance-voltage (C-V) curves of HfO_2 dielectric films with Top and Bottom Al_2O_3 capping layers. The thickness of HfO_2 film was fixed as 2.3 nm. The thickness of ALD Al_2O_3 capping layer was increased as 1, 3, 5, 10 Å, respectively. V_{FB} shift to the positive direction was observed as increasing thickness of Al_2O_3 layer both Top/Bottom Al_2O_3. The V_{FB} shift as a function of Al_2O_3 thickness, clearly show the V_{FB} shift in figure 4.16. The Bottom Al_2O_3 was more effective on V_{FB} shift than Top Al_2O_3. Bottom Al_2O_3 induced larger V_{FB} shift to the positive direction, while Top Al_2O_3 caused relatively smaller V_{FB} shift.

It is also evaluate the effect of Al_2O_3 on the insulating properties, which is shown in the figure 4.17. In terms of J_g at -1V vs. CET data, Bottom Al_2O_3 represents better insulating property than Top Al_2O_3. This can be explained by the interface state of this gate stack. It is believed that Al_2O_3 with relatively larger band gap are located in the interface between HfO_2 and Si substrate, it can reduce the leakage current due to the higher potential barrier. In addition, It is generally believed that Al_2O_3 has better interface quality than La_2O_3. [11]

Figure 4.18 shows the variations of V_{FB} and ΔV_{FB} the effect of Bottom Al_2O_3 layer according to the high-k dielectrics; ZrO_2 and HfO_2 films. V_{FB} modulation effect was identical at both HfO_2 and ZrO_2.

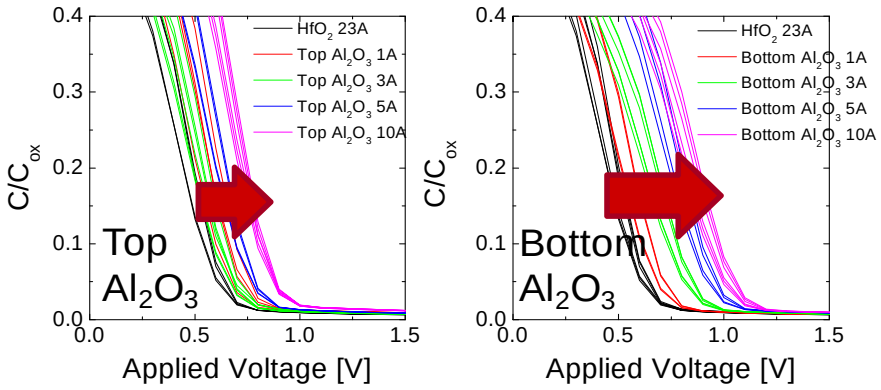


Figure 4.15 The Normalized C-V curves of Top and Bottom Al_2O_3 capping layers with HfO_2 thin films

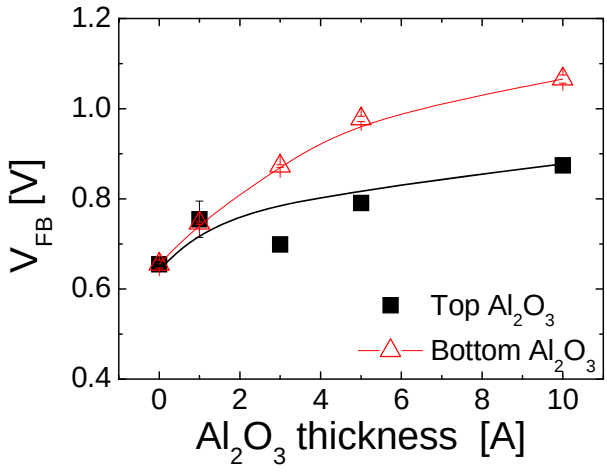


Figure 4.16 A function of Top/Bottom Al_2O_3 thickness and V_{FB} values extracted from C-V curves

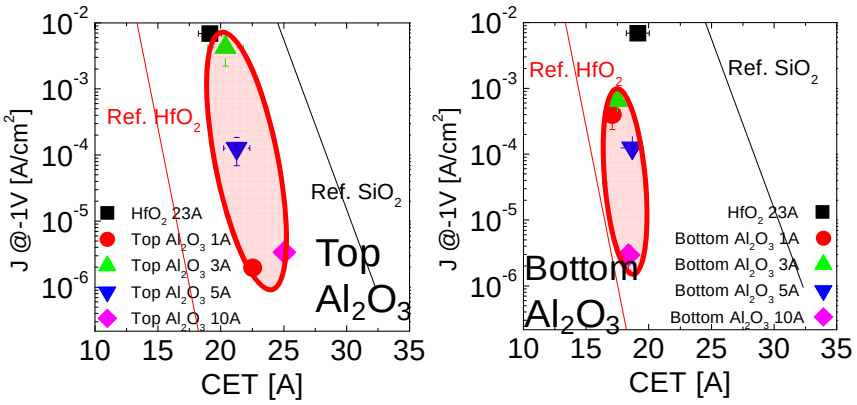


Figure 4.17 J_g. vs CET graphs of Top and Bottom Al_2O_3 with HfO_2 films.

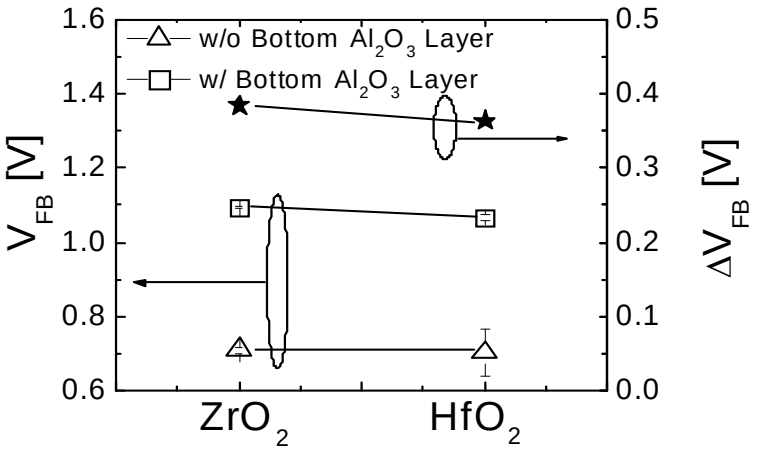


Figure 4.18 Variations of V_{FB} and delta V_{FB} the effect of Bottom Al_2O_3 layer according to the high-k dielectrics; ZrO_2 and HfO_2 films

For investigate of bonding state of ALD Al_2O_3 layer with HfO_2 films, the XPS profile of O 1s peak and valence band of Top and Bottom Al_2O_3 layer with HfO_2 films. The peaks of Top layers shows larger portion of capping materials, in the same vein as the peaks of Bottom layers shows larger portion of HfO_2. This means represents the top capping layer did not diffuse to interfacial layer, and it is consistent with electrical properties. The VBO extracted from valence band of XPS profile is listed on table 4.2. Bottom Al_2O_3 represents lower VBO than Top Al_2O_3 which is correlated with electrical property in reverse trend with the case of La_2O_3.

The effect of high temperature annealing ALD Al_2O_3 layer, and thermal budget on 800^oC was examined. Figure 4.20 represents the original and normalized C-V curves of Top and Bottom Al_2O_3 capping layers with HfO_2 thin films with respect to annealing effect in condition of 800 ^oC 30s under N_2 atmosphere. It was improved the hump of C-V curves due to very thin HfO_2 by thermal curing effect with decrease of accumulation capacitance by oxidation, in addition the direction and amount of V_{FB} shift were still maintained. This means Al_2O_3 capping layers with HfO_2 thin films could endure a thermal budget about 800 ^oC.

Figure 4.21 shows J_g. vs CET graphs of Top and Bottom Al_2O_3 with HfO_2 films in accordance with annealing effect. Post deposition annealing results overall increase of CET and poor leakage characteristics as the reaction with Si substrate. However, the degree of degradation was reduced in the case

of Al_2O_3. It suggests that Al_2O_3 is more stable and endurable on high temperature.

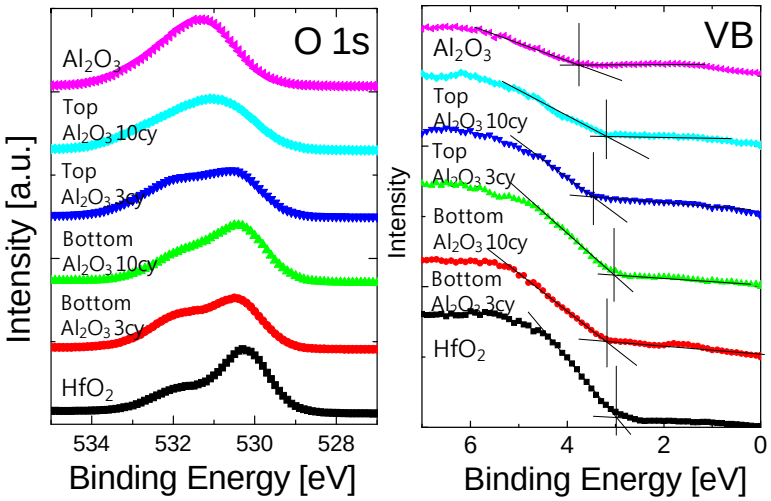


Figure 4.19 XPS profile of O 1s peak and valence band of Top and Bottom Al_2O_3 layer with HfO_2 films

Sample stack	VBO [eV]
Al_2O_3	3.76
Bottom Al_2O_3 10cy	3.19
Bottom Al_2O_3 3cy	3.45
Top Al_2O_3 10cy	3.03
Top Al_2O_3 3cy	3.18
HfO_2	2.99

Table 4.2 Valence band offset(VBO) of Top and Bottom Al_2O_3 layer with HfO_2 films

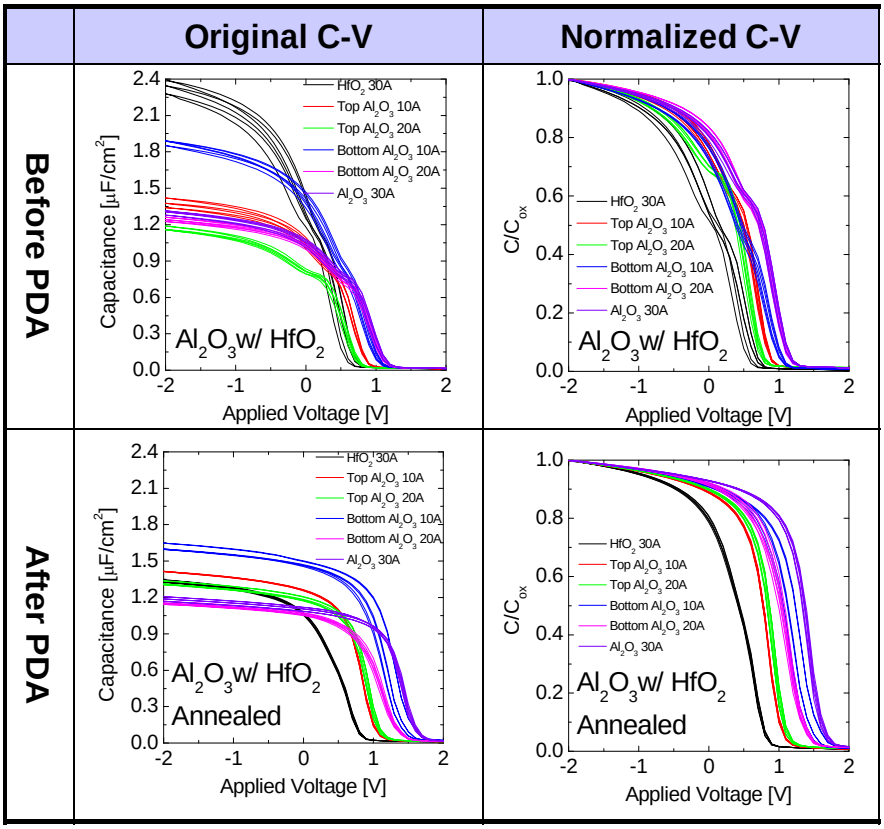


Figure 4.20 C-V curves of Top and Bottom Al_2O_3 with HfO_2, HfO_2 and Al_2O_3 films in terms of annealing effect.(800°C 30s N_2 atmosphere)

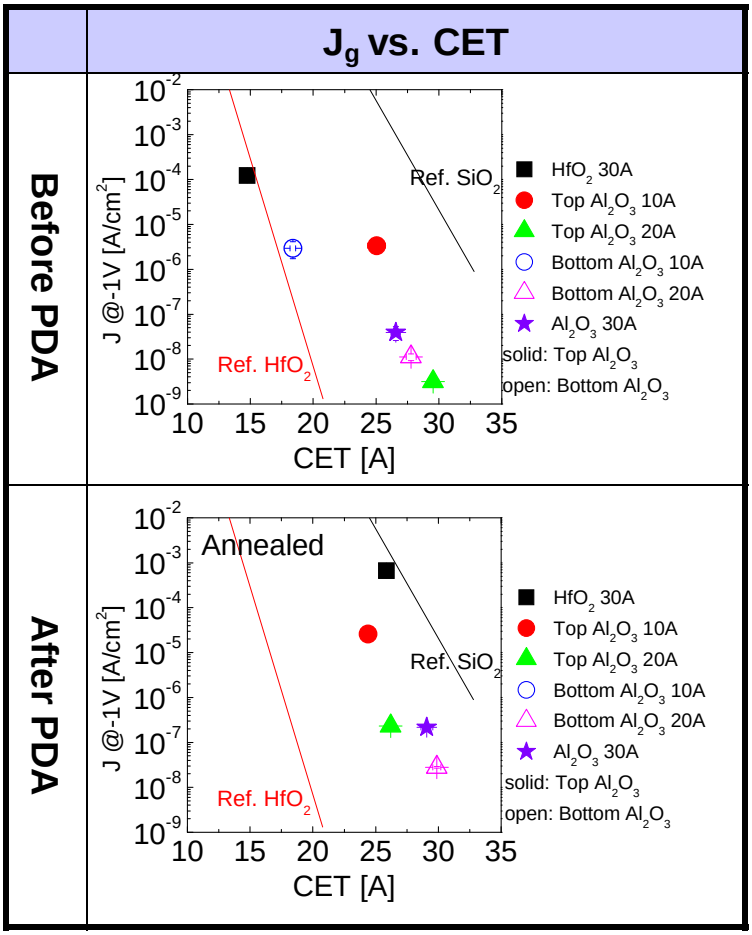


Figure 4.21 J_g vs. CET graphs of Top and Bottom Al_2O_3 with HfO_2, HfO_2 and Al_2O_3 films in terms of annealing effect.(800°C 30s N_2 atmosphere)

4.1.5. ALD SrO capping layer

Finally, ALD SrO capping layer was adopted to Hf-based high-k dielectrics for pMOS application. Figure 4.22 shows the focused in V_{FB} region of normalized capacitance-voltage (C-V) curves of HfO_2 dielectric films with Top and Bottom Al_2O_3 capping layers. The thickness of HfO_2 film was fixed as 3.2 nm. The thickness of ALD SrO capping layer was increased as 3, 6, 9 cycles(thickness is 5.5, 10, 14 Å), respectively. V_{FB} shift to the negative direction was observed as increasing thickness of SrO layer only in Bottom SrO. The V_{FB} shift as a function of SrO thickness, clearly show the V_{FB} shift in figure 4.23. The Bottom SrO was more effective on V_{FB} shift than Top SrO. Bottom SrO induced larger V_{FB} shift to the negative direction as amout of 0.94V, while Top SrO caused negligible V_{FB} shift ~0.13V. The shift amount was not saturated even at 14 Å thick of SrO. This can be explained the the intrinsic preperties of ALD SrO, easily carbonating property of unstable strontium oxide. It is observed in AES depth profile of Top and Bottom SrO with HfO_2 films in figure 4.25. Carbon contents of La_2O_3 and Al_2O_3 with HfO_2 films were negligible (data not shown). Large amount of carbon contents are represented with SrO layer. In the same manner, C 1s peak of La_2O_3 , SrO, Al_2O_3, HfO_2 films in figure 4.26 (a) represents that only SrO shows large carbonate peak at ~280 eV. Therefore, worse insulatinig property by worse interface quality of Bottom SrO was obtained in the J_g at -1V vs. CET plot in figure 4.24.

For investigate of bonding state of ALD SrO layer with HfO_2 films, the XPS profile of O 1s peak and valence band of Top and Bottom SrO layer with HfO_2 films. The peaks of Top layers shows larger portion of capping materials, in the same vein as the peaks of Bottom layers shows larger portion of HfO_2. This means represents the top capping layer did not diffuse to interfacial layer, and it is consistent with electrical properties. The VBO extracted from valence band of XPS profile is listed on table 4.3. Top SrO represents lower VBO than Bottom SrO which is correlated with electrical property in reverse trend with the case of Al_2O_3, and same trend with La_2O_3.

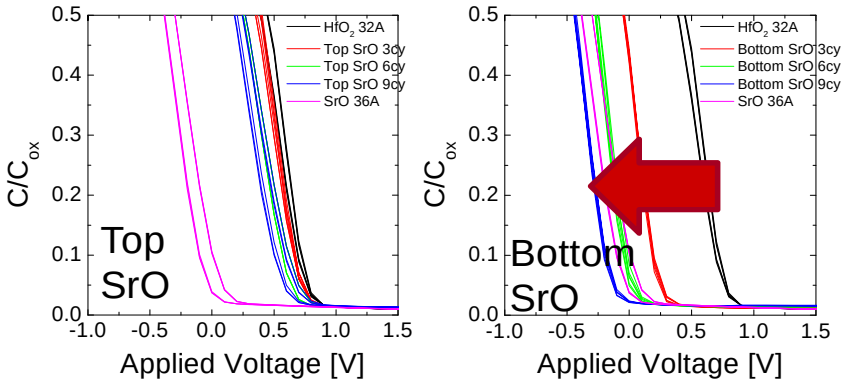


Figure 4.22 The Normalized C-V curves of Top and Bottom SrO capping layers with HfO_2 thin films

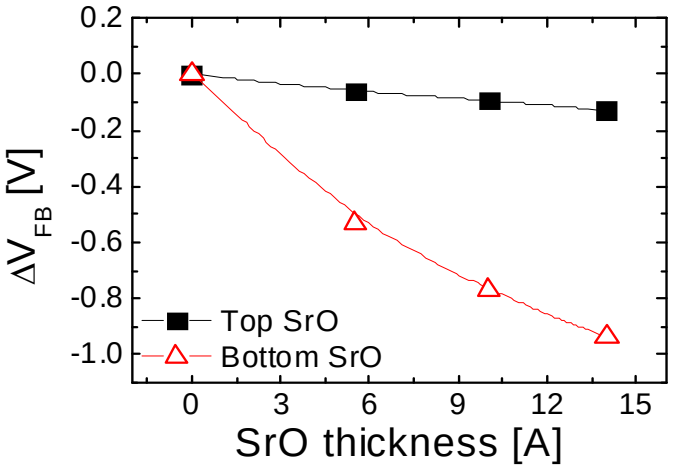


Figure 4.23 A function of Top/Bottom SrO thickness and delta V_{FB} values extracted from C-V curves

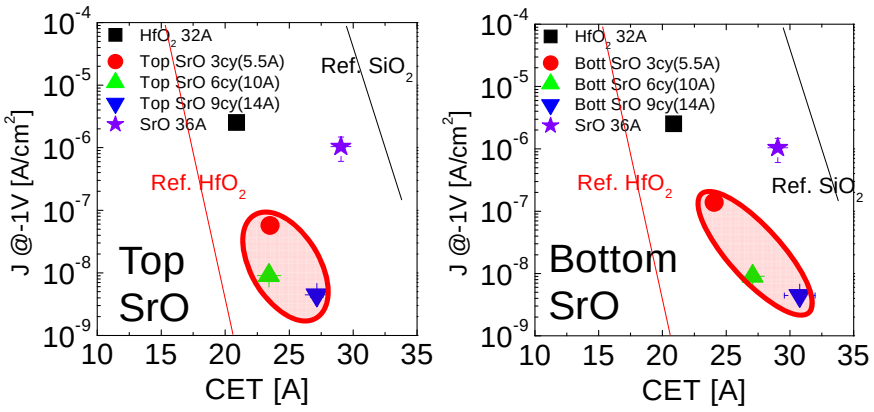


Figure 4.24 J_g. @-1V vs CET graphs of Top and Bottom SrO with HfO_2 films.

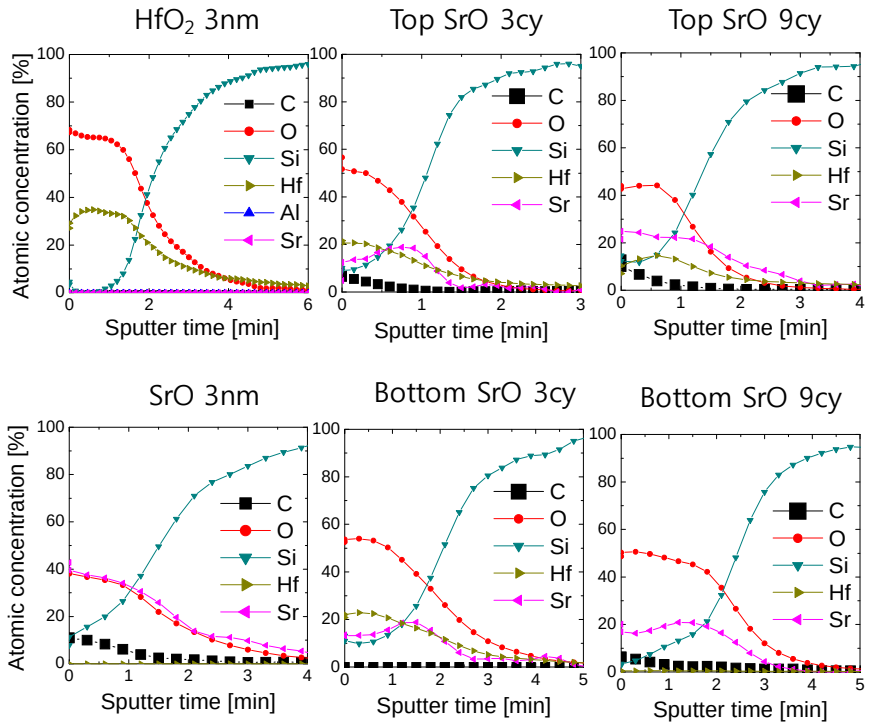


Figure 4.25 AES depth profile of Top and Bottom SrO with HfO_2 films.

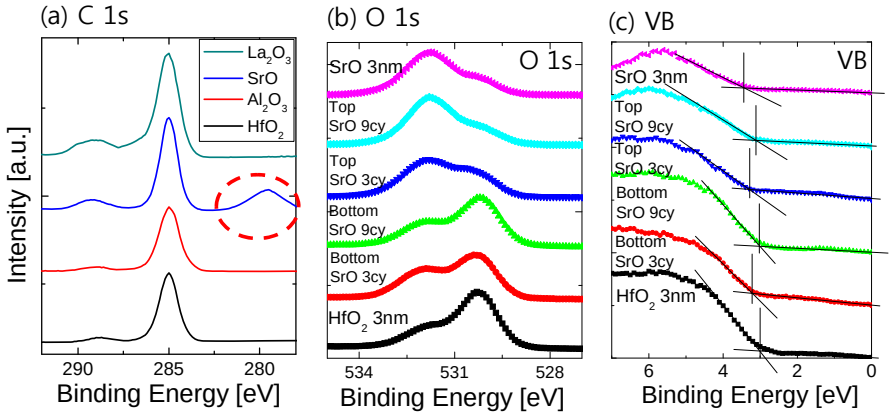


Figure 4.26 XPS profile of (a) C 1s of La_2O_3 , SrO, Al_2O_3, HfO_2 films , (b) O 1s peak and (c) valence band of Top and Bottom SrO layer with HfO_2 films

Sample stack	VBO [eV]
SrO	3.44
Bottom SrO 9cy	3.11
Bottom SrO 3cy	3.29
Top SrO 9cy	3.02
Top SrO 3cy	3.22
HfO_2	3.00

Table 4.3 Valence band offset(VBO) of Top and Bottom SrO layer with HfO_2 films

4.1.6. Comparison and discussion

Totally three kinds of ALD La_2O_3, Al_2O_3, SrO capping layer was adopted to Hf-based high-k dielectrics for n/pMOS application. The delta V_{FB} values according the the capping layer thickness are summarized in figure 4.27, and listed in table 4.4. Figures 4.27 (b)-(d) shows the V_{FB} shift according to the thickness of the capping layers at top and bottom positions. Here, the HfO_2 film thickness was 3 nm. A capping layer thickness of 0 refers to a sample with no capping layer, which is just HfO_2 sandwiched between Pt top electrode and p-Si substrate. As shown in Fig. 4.27, the capping layer thickness clearly has an influence on the V_{FB} shift. The Al_2O_3 bottom layer causes the V_{FB} to shift in the positive direction by 0.41V as shown in Fig. 4.27 (b), while the SrO, and La_2O_3 capping layer cause a shift in the negative direction by -0.94V and -0.37V as can be seen in Fig. 4.27 (c) and (d),

respectively. The V_{FB} shift value for each capping layer is listed in Table 4.4 Previous reports account the V_{FB} shift to the diffusion of the capped metal layer through the dielectrics toward the interface with the Si substrate by high temperature post deposition annealing. The metal at the interface appears to induce interface dipoles, which shifts the energy band structure of the dielectrics. This in turn causes a shift in the V_{FB} [4]. In the data presented in this study, the bottom capping layer is more effective than the top layer in V_{FB} modulation in all cases. This can be attributed to the fact that the top capping layer requires a considerable amount of mixing for an effective amount of interface dipoles to be present. This V_{FB} shift trend, in terms of both direction and amplitude, is in agreement with calculations based on interface dipole moments and valence band offsets [6, 8]. Refer to table 4.5, which is calculated dipole moment from areal density of oxygen atom(σ) at interface of each oxide [6,13], σ was calculated.

$\sigma_{HfO2}/\ \sigma_{La2O3} = 0.1440/0.1092 = 1.32$

$\sigma_{La2O3}/\ \sigma_{SiO2} = 0.1092/0.0.1247 = 0.88$

From these data, σ of La_2O_3/ HfO_2 interface is +1.32, σ of La_2O_3/ SiO_2 interface is -0.88, sum is +0.44 in the case of Bottom La_2O_3. This result is similar with V_{FB} values of Bottom La_2O_3 (-0.37V). In the same theme,

$\sigma_{Al2O3}/\ \sigma_{SiO2} = 1.37$

$\sigma_{HfO2}/\ \sigma_{Al2O3} = 0.1440/0.1705 = 0.84$

$\sigma_{Al2O3}/\ \sigma_{SiO2} = 0.1705/0.1247 = 1.37$

From these data, σ of HfO_2/ Al_2O_3 interface is +0.84, σ of Al_2O_3/ SiO_2 interface is -1.37, sum is -0.53. The calculated dipole moment from oxygen areal density and molar volume is well correlated with experimental result of V_{FB} shift (+0.41V).

In another approach, the dipole mement calculated by electro negativity and bonding length was compared during the capping materials. The calculated dipole moment values are well correlated with experimental result of V_{FB} shift.

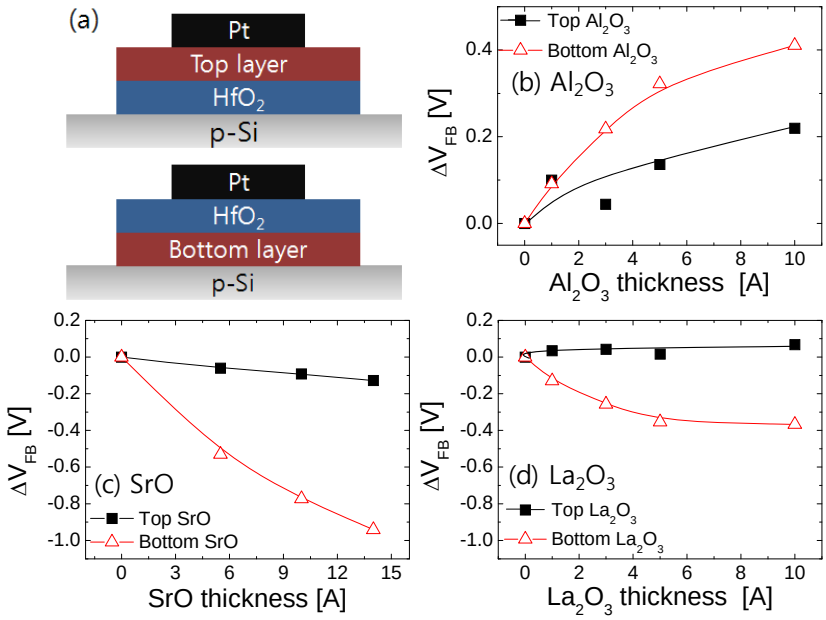


Figure 4.27 (a) Schematic diagram of sample stack, V_{FB} shift depending on thickness and relative position with HfO_2 of ALD capping layers (b) Al_2O_3, (c) SrO, and (d) La_2O_3

Capping Layer	Top Layer	Bottom Layer
Al_2O_3 (10 Å)	0.22 V	0.41 V
SrO (14 Å)	-0.13 V	-0.94 V
La_2O_3 (10 Å)	0.07 V	-0.37 V

Table 4.4 The variations of ΔV_{FB} of each capping layers with HfO_2 dielectrics.

Oxides	SiO_2	HfO_2	Al_2O_3	La_2O_3
Pauling's EN	1.90	1.3	1.61	1.1
Sanderson's EN	2.86	2.49	2.54	2.18
Density (g/cm^3)	2.2	9.6	3.99	6.51
Molar volume V_m ($Å^3$)	45.4	34.7	42.5	83.1
Unit structure	$Si_{1/2}O$	$Hf_{1/2}O$	$Al_{2/3}O$	$La_{2/3}O$
V_u($Å^3$) (# of oxygen atom/unit area)	22.7	18.3	14.2	27.7
$\sigma=V_u^{-2/3}$	0.1247	0.1440	0.1705	0.1092
σ/σ_{SiO2}	1.00	1.15	1.37	0.88

Table 4.5 Calculated dipole moment from areal density of oxygen atom(σ) at interface of each oxide [13]

Element	Electro negativity (Pauling)	△EN wrt HfO_2	Bonding length (sum of ionic radii) [Å]	Dipole moment = △EN x Bonding Length	Experimental result
HfO_2	1.3	0	2.18	0	0
Al_2O_3	1.61	0.31	1.90	0.589	0.41V
La_2O_3	1.1	-0.2	2.46	-0.492	-0.37V
SrO	0.95	-0.35	2.53	-0.886	-0.94V

Table 4.6 Calculated dipole moment from electro negativity and bonding length of each oxide [13, 14]

The CET vs. leakage current (J_g) insulator properties, considering V_{FB} shifts are shown in Figure 4.28. The two lines in the figure represent the calculated values of SiO_2 and HfO_2 (5). As can be seen in the figure, better gate insulator properties, namely, a lower J_g at a given CET is shown with bottom layers in the case of Al_2O_3, while SrO and La_2O_3 show better quality when used as top layers. This can be attributed to the fact that SrO and La_2O_3 thin films are vulnerable to moisture, and to the formation of carbonate or silicate which generates a poor interfacial layer (IL) that degrades the insulator properties. It need to be remembered that the SrO and La_2O_3 layers grown *ex-situ* while the Al_2O_3 layer was grown *in-situ* with the ALD HfO_2

layer. The fact that the band gap of Al_2O_3 is wider than SrO and La_2O_3 can also be an explanation for this behavior [8, 10].

Figure 4.29 shows the XPS results of O 1s core-level spectra of the top and bottom Al_2O_3 and SrO capped HfO_2 films. Although the peaks of both top and bottom layers shows a mixture of each capping layer and HfO_2, larger peak intensities of the capping layer are observed in top capped devices. This can be understood as a modest mixing of the top capping layer and the HfO_2, suggesting that all the top capping layer did not diffuse to the substrate-stack interface. This concurs with the aforementioned V_{FB} shift results and other previous reports. It was reported that a 1000 ^oC annealing process causes a V_{FB} shift because the capping layer diffuses to the substrate – gate dielectric interface at such high temperatures [3, 5]. The massive amount of diffusion caused by the high temperature process in these reports can be thought to be similar to the bottom capping layer case in this experiment. As a result, the V_{FB} of HfO_2 gate dielectrics can be effectively modulated by controlling the thickness and relative position of ALD grown capping layers.

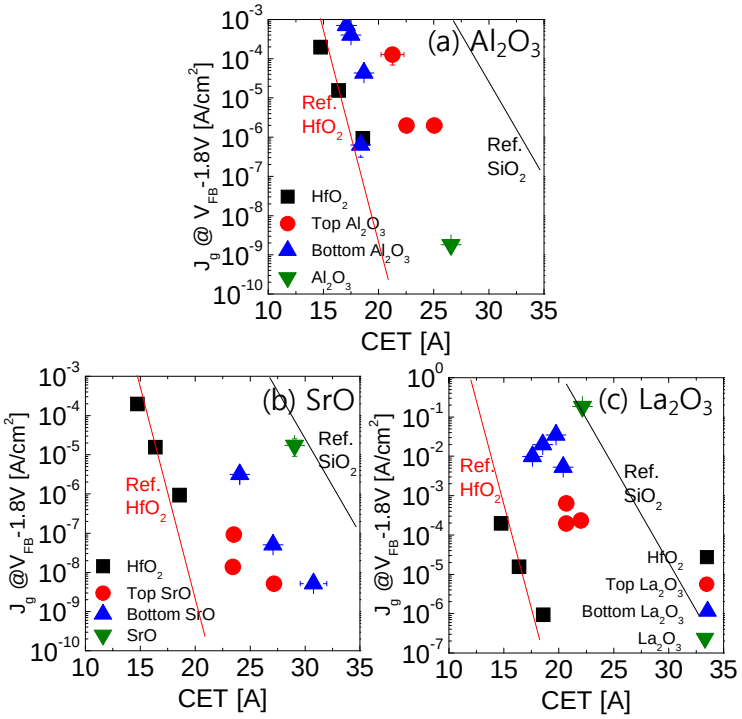


Figure 4.28 CET vs. J_g gate insulator properties considered V_{FB} (V_{FB}-1V)(a) Al_2O_3, (b) SrO, and (c) La_2O_3 capping with HfO_2.

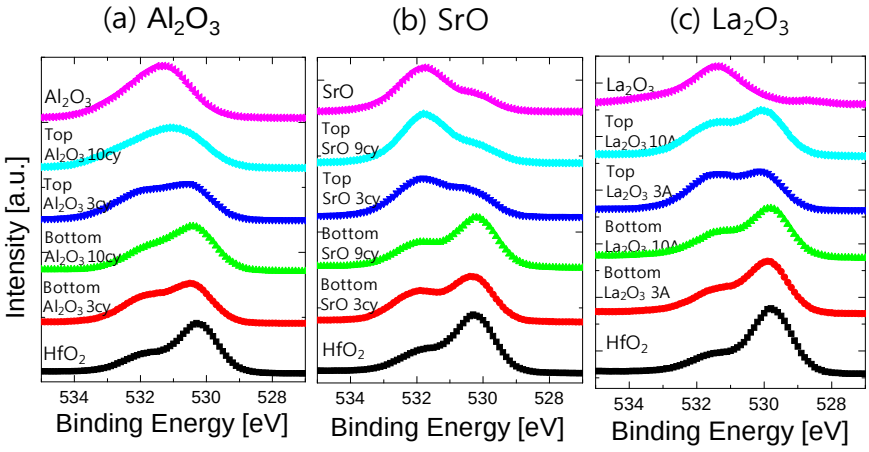


Figure 4.29 The O 1s peak which means each oxide bonding represents the top capping layer did not diffuse to interfacial layer.

4.1.7. Conclusion

The bottom layers grown by ALD are more effective than top layers in modulating the V_{FB} of HfO_2 gate dielectrics. Al_2O_3 capping layers cause a V_{FB} shift in the positive direction, while SrO and La_2O_3 capping layers cause a negative shift. The insulating properties of the gate dielectric stack rely on the formation of unstable top or bottom capping layers. XPS data implies that all the top capped layers did not diffuse to the interface, which supports that bottom capped layers are effective in modulating the V_{FB}. SrO represented most large amount of V_{FB} shift, however it contained losts of amount of carbonate due to characteristic of easily carbonated Sr. The effect of capping layer on leakage current density observed according to degree of reaction between capping layer and substrate or own band gap. However, the reaction or intermixing at interface did not affect the roughness of high-k dielectrics due to too thin thickness. The origin of V_{FB} shift could be explained by dipole theory, it is well mated with electrical property and calculated dipole moment of amount and direction of V_{FB} shift.

4.1.8. References

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4.2. Effects of O_3 and H_2O as oxygen sources in ALD of HfO_2 gate dielectrics at different deposition temperatures

4.2.1. Introduction

HfO_2 thin films have been widely used in the semiconductor industry, especially in the mass production of Si-based metal insulator semiconductor field effect transistors (MISFETs), as high dielectric constant (high-k) gate dielectric thin films since 2007 [1-3]. Atomic layer deposition (ALD) has many advantages in the formation of gate dielectric thin films for extremely scaled planar or three-dimensional structured devices due to its self-limiting growth behavior, which confirms a low leakage current, high dielectric constant, and atomic-level precise thickness control. However, more studies are required to fabricate Hf-based dielectric films with even higher-k values ($k > 30$) for further scaled MISFETs that require an equivalent oxide thickness (EOT) < ~0.5 nm. In addition, there is a greater challenge to apply ALD-processed HfO_2 to high-mobility channel materials such as III-V or II-V compound semiconductors for the n-type MISFET and Ge for the p-type MISFET [2-3]. These challenges are known to be caused by the unstable interfaces between the HfO_2 film and the high-mobility substrates [4-8], the status of which is largely influenced by the detailed ALD conditions. Several other high-k dielectrics, such as Al_2O_3, La_2O_3, and $LaLuO_3$ [9-12], have been

adopted for the high-mobility substrates, but it might be best if the use of HfO_2 can be extended to these substrates considering its mature process equipment, conditions, and contamination-control protocols in mass-production lines.

Because of these important aspects of HfO_2 in advanced semiconductor chips, ALD of the HfO_2 film is one of the most extensively studied ALD processes. While the commercialized ALD process of the HfO_2 film for high-k gate dielectric application adopted $HfCl_4$ and H_2O as the Hf-precursor and the oxygen source, respectively [13-16], alternative ALD processes that utilize metal-organic Hf-precursors and O_3 are still under intensive research [17-19]. The major driving force for the search for such an alternative ALD process is the difficulty in handling the powdery $HfCl_4$ precursor, which requires a high vaporization temperature (~200^oC) to achieve sufficient vapor pressure, and hardware problems related to the corrosive reaction by-product (HCl) of the process [20]. The ALD process of the HfO_2 film using $HfCl_4$ and H_2O could be performed well at the substrate temperatures (T_s) of 300 - 400^oC without the concern related to the thermal decomposition of the $HfCl_4$. In contrast, most metal-organic Hf-precursors suffer from such degradation at a relatively low T_s; most Hf-alkoxides and Hf-alkylamides thermally decomposed at temperatures lower than ~200-250 and 300-350^oC, respectively, the accurate values of which are dependent on the detailed process conditions [21-23]. (Modified) cycloropentadienyl (Cp)-based Hf-

precursors have shown higher thermal decomposition temperatures (of up to ~ 400°C) [24], but ALD using the Cp-based Hf-precursors usually has a lower growth rate (< ~0.05 nm/cycle) than other metal-organic Hf-precursors, presumably due to the higher bulkiness of the ligand and its superior thermal stability [24-25].

O_3 is attracting increasing interest as the oxygen source for the ALD of various oxide films due to its generally higher oxidation potential than H_2O at a normal ALD temperature range. The higher oxidation power of O_3 is particularly attractive when the ALD process temperature approaches the upper limit of the ALD temperature window, where the (partial) thermal decomposition of Hf-precursors results in C-impurity contamination in the film. H_2O can hardly remove the cracked C from the ligands, but the strong oxidation power of O_3 can remove it by forming volatile CO and CO_2 [17]. O_3 has been highly accepted in capacitor dielectric layer formation for dynamic random access memory (DRAM), such as ZrO_2 and Al_2O_3, where the as-high-as-possible ALD temperature was preferred to achieve higher crystallinity accompanied by a higher dielectric constant. However, for the MISFET application, O_3 almost always induces interfacial thin SiO_2 formation during the ALD of the HfO_2 film, which really deteriorated the overall k-value of the gate dielectric layer when the high-k HfO_2 film was within the practical thickness range (2-4 nm) [26]. Therefore, there must be an appropriate compromise between the attainable lowest EOT and the film

quality by controlling the T_s, O_3 concentration and the O_3 pulse time [27]. The lower T_s generally induces a lower interfacial layer (IL, mostly SiO_2 or Hf-silicate), but the high quality of the high-k film must be sacrificed under such condition. Recently, a technology where adoption of a chemically active metal gate, which is active enough to scavenge the oxygen from the IL without degrading the quality of HfO_2, was developed [28]. This means that the IL can be removed by the post-process after the gate formation [29-30]. Such removal of IL was inevitably accompanied by the degradation of the carrier mobility and reliability in the MISFET device, but such deterioration of the device performance could be overcompensated for by the increased capacitance effect [28,30]. Therefore, the adoption of O_3 for MISFET fabrication has a higher probability in the most recent integration flow. Another advantage of O_3 over H_2O is its faster purge-out speed, especially when the ALD temperature is lower than < ~150^oC, during which the purge-out speed of H_2O becomes very slow [17,31]. In contrast, the chemical activity of O_3 at such a low temperature drops quickly, so adoption of O_3 for low-temperature ALD is not desirable. In this regard, the maintained high chemical activity of H_2O toward the ligand-exchange reaction of ALD oxide films could be highlighted.

Another important task of the ALD of high-k films is the phase control to achieve an even higher k value, which has been less focused on the MISFET field compared with the capacitor dielectric for DRAM. The k-

value of HfO_2 is largely dependent on its crystallographic phases (amorphous and monoclinic, ~15, and tetragonal and cubic, ~30) [32-33], which must be largely determined by the detailed deposition as well as the post-deposition annealing (PDA) conditions. Although the thermodynamic stable phase of HfO_2 at the ALD temperature (160-360^{o}C in this study) and at the typical PDA temperature (T_{PDA}, up to 1000^{o}C) is monoclinic [34], there have been many reports on the formation of tetragonal- or cubic-phase HfO_2 thin films by controlling the microstructure of the films [35-39]. In this report, the higher-k HfO_2 phase is considered the tetragonal phase because it is usually difficult to clearly distinguish the tetragonal phase from the cubic phase in a thin HfO_2 film via laboratory X-ray diffraction. In addition, the k values of the two phases do not differ much and are also dependent on the crystallographic directions [40]. Therefore, the higher-k phase could be tetragonal, cubic, or even a mixture of them, but a clear distinction was not attempted for as long as the phase was distinguished from the monoclinic phase. Although there are diverse detailed methods of such transformation of HfO_2 to the higher-k phases [39,41], they basically rely on the grain size effect (a smaller grain size is preferred in the higher-k phase) because the surface (or the grain boundary) energy of the higher-k phase is lower than that of the monoclinic phase [42-44]. Therefore, varying the T_s and the types of oxygen sources could be a viable way to vary the grain size at the as-deposited state or after the PDA, and to achieve the higher-k phase.

For the III-V and Ge substrates, the different oxidation powers of H_2O and O_3 at different T_s values may provide a certain ALD process window for the HfO_2 films, where the adverse interfacial effects are minimized. Additionally, the application of the very-low-temperature ALD of high-k dielectric films to transparent and flexible electronic devices is being actively studied. Some of the authors recently reported the growth behavior and film properties of the HfO_2 film at a T_s as low as 30°C using a high O_3 concentration (350 g/m^3) as the oxygen source in ALD [31]. Therefore, in this study, various properties of ALD-HfO_2 films using tetrakis-ethylmethylamino-hafnium {$Hf[N(CH_3)(C_2H_5)]_4$, TEMAHf} as the Hf-precursor and different oxygen sources (H_2O and O_3) grown at different T_s values are examined systematically. While the mentioned previous reports focused on extending the higher end of the ALD temperature window to higher T_s values [17,21-25], this study attempted to explore the possible deposition of high-quality ALD HfO_2 films at lower T_s values, which could provide an essential clue to the achievement of promising growth and electrical behavior of HfO_2 on high-mobility substrates for futuristic MISFET or on plastic substrates for flexible-device fabrication, although this study dealt with only Si substrates. The evolution of phases according to detailed ALD and PDA conditions is also studied in detail.

4.2.2. Experimental

The HfO_2 films were deposited on deionized water(DI water)-diluted, hydrofluoric (HF) acid-cleaned p-type Si(100) wafers with 10Ωcm resistivity via ALD at substrate temperatures (T_s) of 160-360^oC, using TEMAHf as the Hf-precursor and different oxygen sources (H_2O and O_3). O_3 was generated by flowing a mixture of O_2 (1,350 sccm) and N_2 (10 sccm) into an ozone generator (Astex, AX8200). The ozone concentration was fixed at 170 g/m^3. The optimized condition of the Hf-precursor pulse-Ar purge-H_2O (or O_3) pulse-Ar purge time was 3-20-3-10 s, respectively, where an Ar purge gas flow rate of 200 standard cubic centimetres per min (sccm) was adopted. The Hf-precursor vapor was achieved by heating the Hf-precursor canister to 60^oC and transporting it into the cross-flow-type ALD reactor, which is capable of processing an 8-inch-diameter wafer, with the help of Ar carrier gas with a flow rate of 200 sccm. The deionized water with which a steel canister was filled was cooled down to 5^oC to achieve the appropriate H_2O vapor pressure.

The thickness of the HfO_2 film was measured with a single-wavelength ellipsometer (L116D, Gaertner Co.) and a spectroscopic ellipsometer (SE, ESM-300, Wollam Co.). The crystalline structure of the HfO_2 film was analyzed via glancing angle incidence X-ray diffraction (GAXRD, X'Pert PRO MPD, PANalytical Co., X-ray incidence angle 2^o). The surface morphology was examined with a scanning electron microscope (SEM, S-4700, Hitachi) and an atomic force microscope (AFM, JSPM-5200, JEOL

Co.). The root-mean-squared (RMS) roughness of the thin films was measured with the same AFM. The density and roughness of the thin films were measured via X-ray reflection (XRR, using the same equipment as in the XRD). The microstructure of the films was observed via cross-sectional high-resolution transmission electron microscopy (HRTEM, JEM 3000F, JEOL). The HRTEM sample was prepared via standard sample bonding, grinding, and ion milling. The chemical bonding states of the HfO_2 films were examined with the X-ray photoelectron spectra (XPS, Sigma Probe, ThermoVG) using a monochromatic Al Kα source (1486.6 eV) to excite the photoelectrons. The positions of all the peaks were calibrated for the C 1s peak of the adventitious carbon-carbon binding energy to be assigned at 284.5 eV. The carbon impurity concentration was confirmed via Auger electron spectroscopy (AES, Perkin-Elmer 660) in the depth profiling mode, which is performed via Ar^+ ion sputtering.

To examine the electrical property, metal-insulator-semiconductor (MIS) capacitors were fabricated with sputter-deposited Pt top electrodes through a shadow mask with 300 μm-diameter holes. Forming gas annealing was performed to passivate the dangling bonds at the interface between the oxide and the substrate under a H_2 (5%)/N_2 (95%) mixture gas atmosphere at 450^{o}C for 10 min. The capacitance-voltage (C-V) was measured using an HP 4194A impedance analyzer at the frequency of 100 kHz. The oxide leakage current (J_g) was investigated using an HP 4140B picoammeter/DC voltage

source. The Pt gate was biased while the Si substrate was grounded during the electrical measurements. The capacitance equivalent thickness (CET) was estimated from the accumulation capacitance values when the films were thick enough (> ~10 nm), and from the fitting of the C-V curves to the theory using the CVC program [45].

4.2.3. Growth behavior and film characteristics

First, the changes in the film growth rate (the thickness increase per ALD cycle) and the film density were examined as functions of T_s. Figures 4.30 (a) and (b) show the variations in the growth rate and the film density of the HfO_2 film, respectively, as functions of T_s. Here, the growth rate was estimated from the slope of the best-linear-fitted graphs of the data points that showed the film thickness as a function of the ALD cycles for each condition (data not shown). Therefore, the data presented in Figure 4.30 (a) are free from the possible influence of any interfacial layer (IL) growth. In the case of the HfO_2 with O_3, the film growth rate monotonically decreased with the increasing T_s up to ~320^{o}C, but suddenly increased at the T_s of 360^{o}C. This suggests that the ALD window could be assigned to the T_s of ~240 to 320^{o}C, where the variation in the growth rate is minimized, and the growth rate was ~0.1 nm/cycle, which is similar to that in previous reports [16-17]. The sudden increase in the growth rate at the T_s of 360^{o}C revealed that the film growth was by then governed by the thermal cracking of the Hf-precursors on the O_3-pulsed surface. The increased growth rate at T_s < ~240^{o}C could be ascribed to the decreased film density and the increased impurity concentration in the films, which will be shown later.

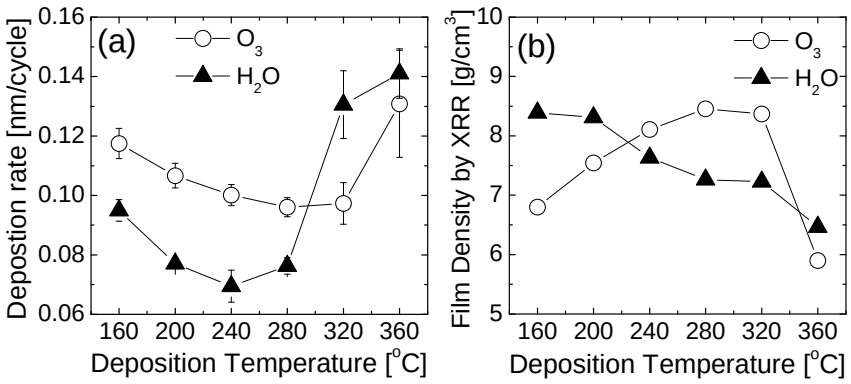

Figure 4.30 Variations in the (a) growth rate and (b) film density, measured via the XRR of the HfO_2 films with O_3 and H_2O oxygen sources as a function of T_s (160-360°C)

In the case of HfO_2 with H_2O, the film growth rate was generally lower than that with the O_3 within the ALD T_s window (< 280°C) which could be ascribed to the lower oxidizing power of H_2O than of O_3 [15]. Within the ALD temperature window, the ALD film growth rate is generally governed by the steric hindrance effect of the chemically adsorbing precursors. When the Hf-precursor was pulsed on the O- or OH^--terminated surfaces, for the O_3 and H_2O cases, respectively, a certain part of the ligands was removed by the ligand-exchange reaction. Depending on the chemical reactivity between the surface reaction sites (the O-radical or OH^--group) and the ligands of the Hf-precursor, the number of ligands left, and thus, the bulkiness of the chemisorbed species, is determined when this reaction is completed. The higher reactivity induced the lower bulkiness and the higher growth rate.

As the T_s exceeded 320°C, the growth rate increased abruptly, which again suggests that the thermal cracking of chemisorbed Hf-precursors is activated at this temperature and chemical vapor deposition (CVD)-like deposition occurs. It is interesting to note that the initiation temperature at which the CVD-like deposition reaction occurs is lower for H_2O even though its driving force toward the ALD-type deposition reaction in the lower T_s region appears to be lower than in the O_3 case. The accurate reasons for such disparate chemical activity of O_3 and H_2O toward CVD-type reaction at different T_s regions are not understood yet, but a hypothesis is given below.

Figure 4.30 (b) shows that the film density of HfO_2 was the highest

(~8.5 g/cm^3) when HfO_2 was deposited with O_3 at a T_s of 280^{o}C, but it is still substantially lower than the ideal value of bulk HfO_2 (9.68 g/cm^3). This highest value was similarly achieved at the T_s of 320^{o}C, but it decreased significantly with the decreasing T_s down to 160^{o}C. The film grown at a T_s of 360^{o}C also showed a very low density, which could be ascribed to the CVD-like growth behavior of the film at such temperature. On the other hand, the layer-by-layer growth in the ALD mode at lower T_s could induce films with a higher density despite the lower T_s. Even in the ALD mode, however, a too low T_s (< 200^{o}C) provides the surface-adsorbed atoms with insufficient thermal energy for them to migrate and form a dense film. The insufficient thermal energy also induced an incomplete ligand exchange reaction, which resulted in the high impurity (carbon-related impurities) in the film, as will be shown later, and which also contributed to the lower film density.

In contrast, the film density of HfO_2 with H_2O increased monotonically with decreasing T_s, and the highest density (~8.5 g/cm^3) was achieved at the lowest T_s of 160^{o}C. While the low density of the films grown at the T_s of 320 and 360^{o}C could be ascribed to the CVD-like growth behavior, as in the O_3 case, the decreasing density with the increasing T_s within the ALD window required different explanations from the usual temperature-dependent density of ALD films.

Figure 4.31 shows the AES depth profiling results of HfO_2 films grown

at four different deposition conditions. The condition of 280°C O_3, as shown in Figure 4.31 (a), had the lowest carbon impurity contents (< 5 atomic %), which indicates that the ALD reaction fluently occurred under this condition. The HfO_2 film also contained Si with an approximate concentration of 5 atomic %, which must be diffused from the substrate. The Hf/O ratio was constant throughout the film thickness. The film grown at the same T_s with H_2O, as shown in Figure 4.31 (b), also had a low carbon impurity concentration, and the Hf/O ratio was also constant throughout the film thickness. In addition, the Si concentration was much lower than that in Figure 4.31 (a). This suggests that the Si diffusion observed in Figure 4.31 (a) was induced by the high oxidation potential of O_3 and not by the thermal energy of 280°C. O_3 could be well decomposed into O_2 and O-radicals at this T_s, and the resulting O-radicals induced the fluent ALD-type reactions to form the stoichiometric HfO_2. The high activity of the O-radicals adsorbed on the film surface induced the outward diffusion of Si from the substrate. In the case of the 200°C O_3, as shown in Figure 4.31 (c), a significant concentration of carbon impurity was observed, which was also seen in the previous report [36]. However, the Si concentration in the HfO_2 film was negligible in this case. It can also be seen that the Hf concentration was much lower than that in the film grown at a higher temperature and was non-uniform across the film thickness, but the oxygen concentration did not significantly differ. This suggests that some of the oxygen atoms might have

combined with C (and also H, which cannot be detected by AES) and been contained in the film. This explains well the low film density in this case, as shown in Figure 4.31 (b). It appears that the decomposition of O_3 into the O_2 and O-radicals at this T_s was not high enough, so the fluent ALD-type reaction did not occur. The almost negligible Si concentration in the films also supports this hypothesis, because the small difference in the T_s (80^oC) was not expected to induce such a subtle difference in the thermal diffusion of Si into the HfO_2 film. The high carbon impurity concentration in the HfO_2 film was also reported under similar ALD conditions, except for the adoption of O_2 instead of O_3 at a T_s of 280^oC by Cho et al. [39].

In contrast, the condition of 200^oC H_2O, as shown in Figure 4.31 (d), resulted in lower carbon contents than in the film grown at 200^oC with O_3, and the overall composition profiles did not significantly differ from that of the film grown at 280^oC under the H_2O condition. These AES results suggest that the ALD behavior of the HfO_2 films with O_3 or H_2O is not simply governed by the oxidation power of the adopted oxygen source.

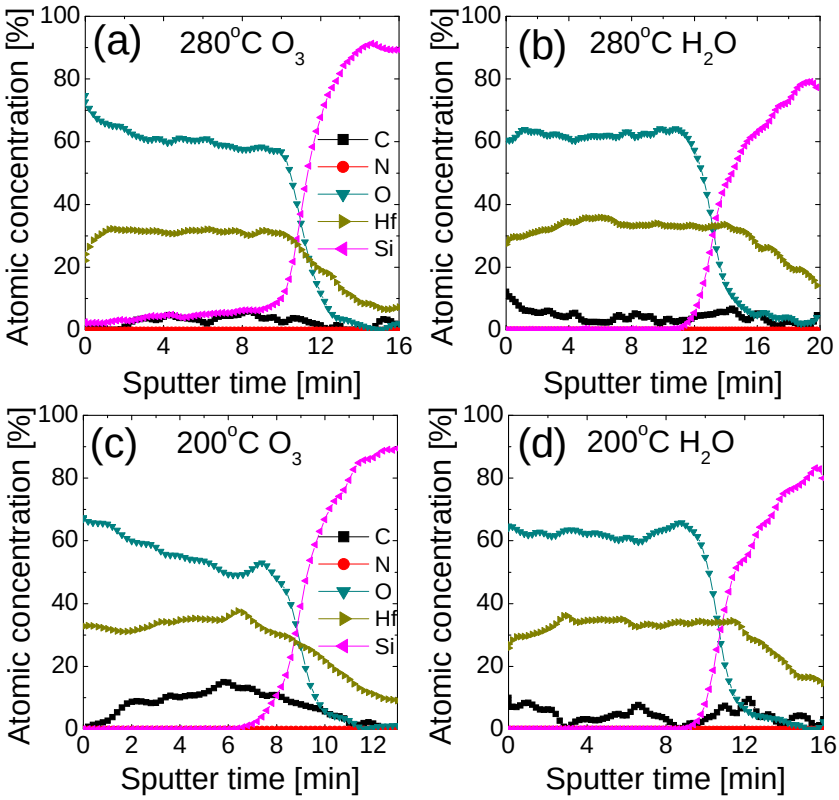

Figure 4.31 AES depth profile of the HfO_2 films under these four deposition conditions: (a) 280°C O_3, (b) 280°C H_2O, (c) 200°C O_3, and (d) 200°C H_2O

4.2.4. Growth mechanism

From these data, the deposition mechanisms of the HfO_2 film with O_3 or H_2O as the oxygen source could be as follows. The possible chemical reaction routes for the ALD of HfO_2 using TEMAHf and H_2O were carefully examined using molecular dynamic simulations based on the density functional theory [46]. In that study, it was concluded that the key ingredient that triggers the ALD reaction of the HfO_2 film to commence with the TEMAHf and H_2O was the supply of protons from the OH^- groups to the incoming TEMAHf molecules when they were pulsed on the OH^--terminated surface [28]. The donation of protons to the TEMAHf molecules and the chemical reaction with the TEMA ligands have a highly exothermic nature, which makes them occur fluently even at a very low temperature without involving the significant activation energy barrier. This is in quantitative agreement with the earlier suggestion on the two-step ALD mechanism based on the experiment results reported by Liu et al [17]. Therefore, it could be considered that the 160^oC of T_s was high enough to induce the ideal ALD reaction between the TEMAHf-precursor and H_2O, and to produce HfO_2 films with a high density and a high growth rate. However, as the T_s increases, the surface concentration of the OH^- group decreases due to re-evaporation, which would inevitably induce sparse adsorption of TEMAHf-precursor molecules in the subsequent metal-precursor pulse step. Once the TEMAHf-precursor molecules sparsely adsorb on the growing surface, further ALD steps would produce a film with a porous structure because the

subsequently impinging TEMAHf-precursor molecules must feel the steric hindrance effect when they attempt to fill in the empty surface sites that were formed in the previous ALD cycle. H_2O molecules may not feel such hindrance effect because they have much smaller molecular size. This could explain the tendency of growth and impurity concentration with respect to T_s, as shown in Figures 4.30 and 4.31, in the cases of ALD using H_2O. As the T_s exceeds 320^oC, such proton diffusion may occur at a higher extent to form multiple layers composed of partially fragmented TEMAHf molecules in the Hf-precursor pulse step. This could significantly increase the growth rate, as shown in Figure 4.30 (a), but the multiple layers could have a less dense structure, which is in accordance with the results shown in Figure 4.30 (b). This is not correlated with the normal mechanism of film growth, wherein the increase in the deposition temperature promotes migration of an adatom and results in a high film density.

In contrast, in the case of ALD with O_3, a different mechanism should be invoked, because there is hardly any OH^- group [17] on the film surface, and therefore, there would be hardly any proton donation as well. Instead, in this case, when the Hf-precursor molecules were pulsed, they chemically adsorbed on the surface by temporarily making the coordination number metal centers of the TEMAHf molecules five from the reaction between them and the surface oxygen ions [46] that were contained in the previously grown HfO_2, or the O-radicals adsorbed at the Hf sites. When the O_3 was

subsequently injected onto the O-TEMAHf-containing surface, it decomposed to the O_2 molecules and O-radicals, and the O-radicals reacted with the ethylmethylamide-ligands, which finally completed the ALD reaction. From the analysis of the reaction by-products of the TEMAH-O_3 ALD process, it was concluded that there was a low probability of replacing the ethylmethylamide-ligand with OH^- groups, but the Hf-N bond was replaced by the Hf-O bond, and the fragmented ethylmethylamide-ligands were decomposed into simpler compounds due to their combustion from their reaction with O_3 [17]. The decomposition of O_3 into the O_2 molecule and the O-radical must be thermally activated. Such reaction routes may involve a very high activation energy barrier that could thermally activate the overall reaction and lead to more effective ligand removal and a higher film density and purity at a higher T_s. O-radicals are not expected to diffuse to the chemically absorbing molecules in the precursor pulse step, as they are very different from the proton donation and diffusion in the case of ALD with H_2O, so the initiation temperature for the CVD-like behavior increased to 360^oC, as shown in Figure 4.30 (a). Such a subtle difference in the reaction mechanism of ALD using H_2O and O_3 resulted in the following very distinctive film properties. Two types of reaction mechanism of HfO_2 deposition with H_2O and O_3 is represented in schematic diagram in figure 4.32.

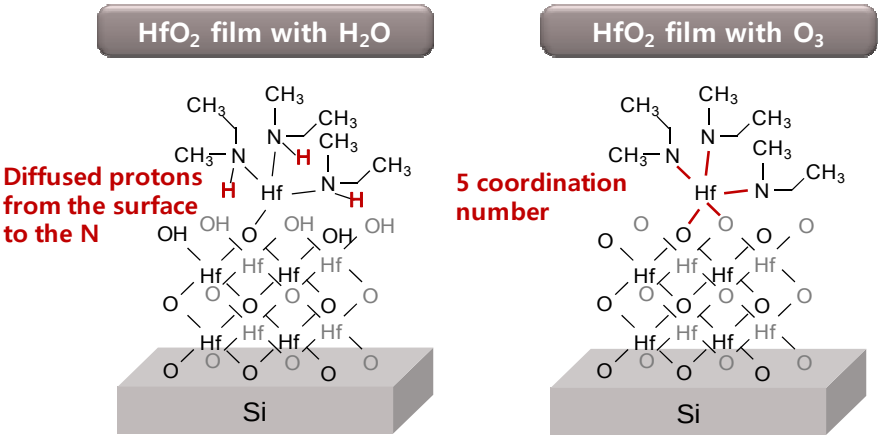

Figure 4.32 Schematic diagram of reaction mechanism of HfO_2 deposition with H_2O and O_3.

4.2.5. Crystallinity and Microstructure

The evolution of crystalline phases according to the deposition and PDA conditions was examined using GAXRD. Figure 4.33 (a) shows the GAXRD spectra of the as-deposited films with an increasing film thickness when the films were grown at a T_s of 280^{o}C using O_3. When the films were thinner than ~25 nm, they retained amorphous structure; but they started to be crystallized to the monoclinic phase as they became thicker than ~27 nm. When the films were ~47nm-thick, clear diffraction peaks that could be assigned to the monoclinic phase emerged, which suggests that the films were crystallized well to the monoclinic phase even at their as-deposited state under such ALD condition. Figure 4.33 (b) shows, from bottom to top, the GAXRD patterns of the as-deposited 45nm-thick HfO_2 films grown under these four different deposition conditions: 280^{o}C O_3; 280^{o}C H_2O; 200^{o}C O_3; and 200^{o}C H_2O. The HfO_2 films grown at the T_s of 280^{o}C crystallized to the monoclinic phase for both oxygen sources, and the HfO_2 film grown under the condition of 200^{o}C H_2O showed very weak crystallization. However, the HfO_2 film grown under the condition of 200^{o}C O_3 showed an almost complete amorphous state despite such thickness. However, the evolution of the crystalline phases upon the PDA of the as-deposited film differed significantly according to the ALD conditions, as shown in Figure 4.34.

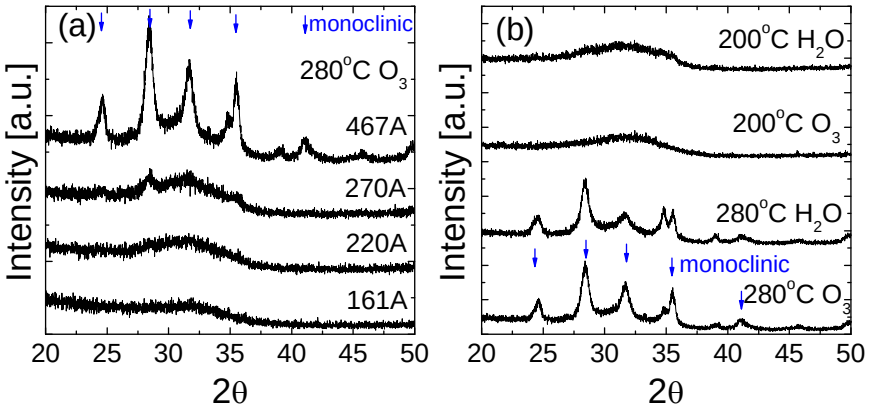

Figure 4.33 GAXRD spectra of the (a) as-deposited HfO_2 films that thickened when the films were grown at a T_s of 280°C using O_3, and (b) as-deposited 45nm-thick HfO_2 films grown under these four different deposition conditions: 280°C O_3, 280°C H_2O, 200°C O_3, and 200°C H_2O, from bottom to top.

Figures 4.34 (a)-(d) show the variations in the GAXRD patterns of the four different HfO_2 samples grown under conditions identical to those in Figure 4.31, which thicknesses were 6 nm, with the increasing PDA temperature (T_{PDA}) of 450°C to 600°C. All the as-deposited samples were amorphous. While the HfO_2 films grown under the conditions of 280°C O_3 and 200°C H_2O were crystallized to the monoclinic phase after the PDA at > 550°C, the HfO_2 films grown under the conditions of 200°C O_3 and 280°C H_2O retained their amorphous structures up to 550°C and crystallized to the mostly tetragonal phase at the T_{PDA} of 600°C. The crystallizations to the monoclinic phase of the films grown under the conditions of 280°C O_3 and 200°C H_2O were normal, as the monoclinic phase is a thermodynamically stable phase. However, the evolution of the HfO_2 phase to the tetragonal phase in the case of the two other conditions had a somewhat unexpected result. As mentioned in the Introduction section, the crystallization of HfO_2 to the tetragonal phase is mainly driven by the grain size effect, and the results shown in Figure 4.34 (c) could be understood from the viewpoint of the adverse interference effect of carbon impurity with the crystallization and grain growth of the amorphous HfO_2 on the PDA. This is in good agreement with the report of Cho et al. [39], where the ALD of HfO_2 was performed at a T_s of 280°C, with the oxygen source of molecular O_2, the oxidation potential of which was far lower than that of O_3, so that the film had a similar level of carbon impurity concentration (~10%) despite its high T_s.

However, the density and AES data shown in Figures 4.30 (b) and 4.31 (b) revealed that the HfO_2 films grown under the condition of 280°C H_2O had a low density and a low carbon impurity concentration. This clearly revealed that not only the carbon impurity but also the low density of the as-deposited film induced the crystallization to the tetragonal phase. The low density of the as-deposited film interfered adversely with the grain growth in the PDA and resulted in the tetragonal phase, which was confirmed by the AFM and TEM data that will be shown later. Such trend could be further confirmed by the harsher PDA condition and the thicker thickness.

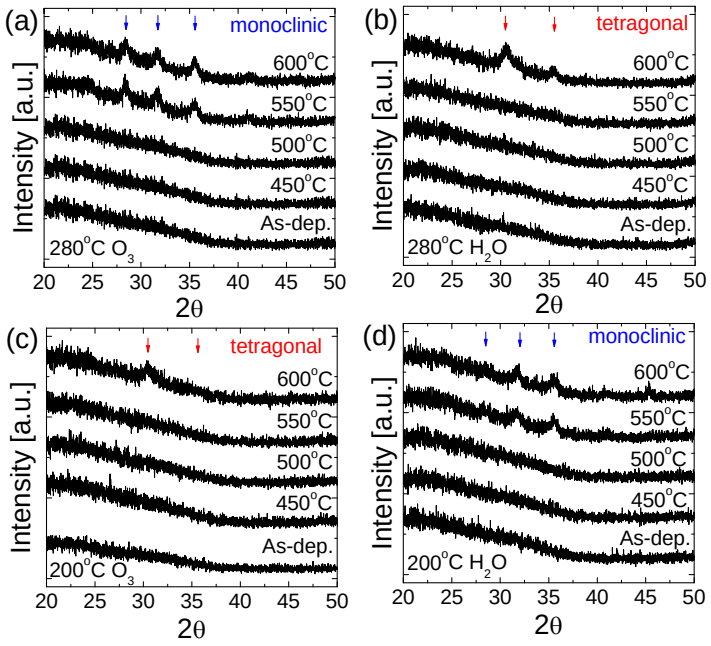

Figure 4.34 Variations in the GAXRD patterns of the four different HfO_2 samples: (a) 280°C O_3, (b) 280°C H_2O, (c) 200°C O_3, and (d) 200°C H_2O, the thickness of which was 6 nm, with the increase in the PDA temperature (T_{PDA}) from 450°C to 600°C

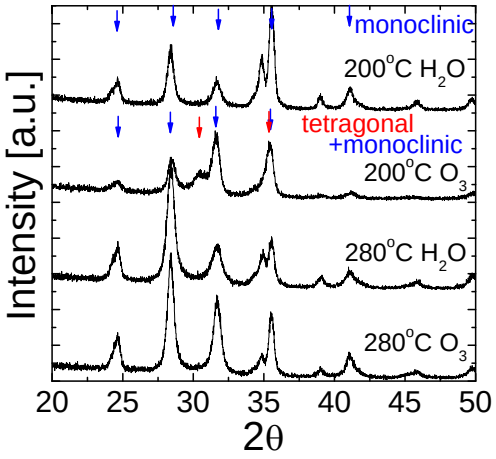

Figure 4.35 GAXRD spectra of the 45nm-thick HfO_2 films grown under the four different conditions after the PDA at 1000°C

Figure 4.35 shows the GAXRD spectra of the 45nm-thick HfO_2 films grown under the four different conditions after the PDA at 1000°C. The crystalline quality generally increased so that the diffraction peaks became clearer. The HfO_2 films that were grown under the conditions of 280°C O_3 and 200°C H_2O were further crystallized to the monoclinic phase. Interestingly, the HfO_2 film grown under the condition of 280°C H_2O, which was predominantly tetragonal after the PDA at 600°C [Figure 4.34 (b)], is now predominantly monoclinic. However, the film grown under the condition of 200°C O_3 still has a non-negligible peak intensity that corresponds to the tetragonal phase, although monoclinic phase peaks appeared after this PDA. This suggests that the carbon impurity really interfered with the grain growth and crystallization of the HfO_2 film to the monoclinic phase even at the T_{PDA} of 1000°C.

The correlation between the ALD conditions and the microstructure of the 45nm-thick film after the PDA at 1000°C was further examined via extensive HRTEM analysis. Figure 4.36 (a)-(d) show the representative HRTEM images of the 45nm-thick HfO_2 films grown under these four different deposition conditions: 280°C O_3; 280°C H_2O; 200°C O_3; and 200°C H_2O after the PDA at 1000°C. For each sample, more than 10 HRTEM images were taken, and at least 20 grain images were analyzed using the fast-Fourier transformation technique to identify their phases. The phase analysis results and the grain size distribution in this TEM study are

summarized in Figure 4.37 and Table 4.7, respectively. While the GAXRD results indicated the phase distribution qualitatively, this TEM analysis showed quantitative distributions of the monoclinic and tetragonal phases in each sample. Interestingly enough, the 200°C H_2O condition resulted in the most dominantly monoclinic phase, and the 200°C O_3 condition resulted in ~30% of the tetragonal phase even after the PDA at 1000°C. The 280°C H_2O condition also showed a high portion (~26%) of the tetragonal phase, which could be understood from its initially low density and low carbon impurity concentration. The 280°C O_3 condition, which was not expected to induce any tetragonal phase due to its high density and low carbon concentration, showed ~15% of the tetragonal phase, which could be ascribed to the presence of Si impurity [48]. The grain size distribution was consistent with the phase distribution. As expected, the 200°C O_3 condition produced the smallest average grain diameter (28.6±8.02 nm), which corresponds well to the highest portion of the tetragonal phase in this sample. The 200°C H_2O condition produced the largest grain diameter (47.7±19.3 nm), which means that this sample has the lowest driving force for the formation of the tetragonal phase. The two other conditions resulted in an intermediate grain diameter, so the intermediate phase distribution in this case could be understood well from the grain size effect.

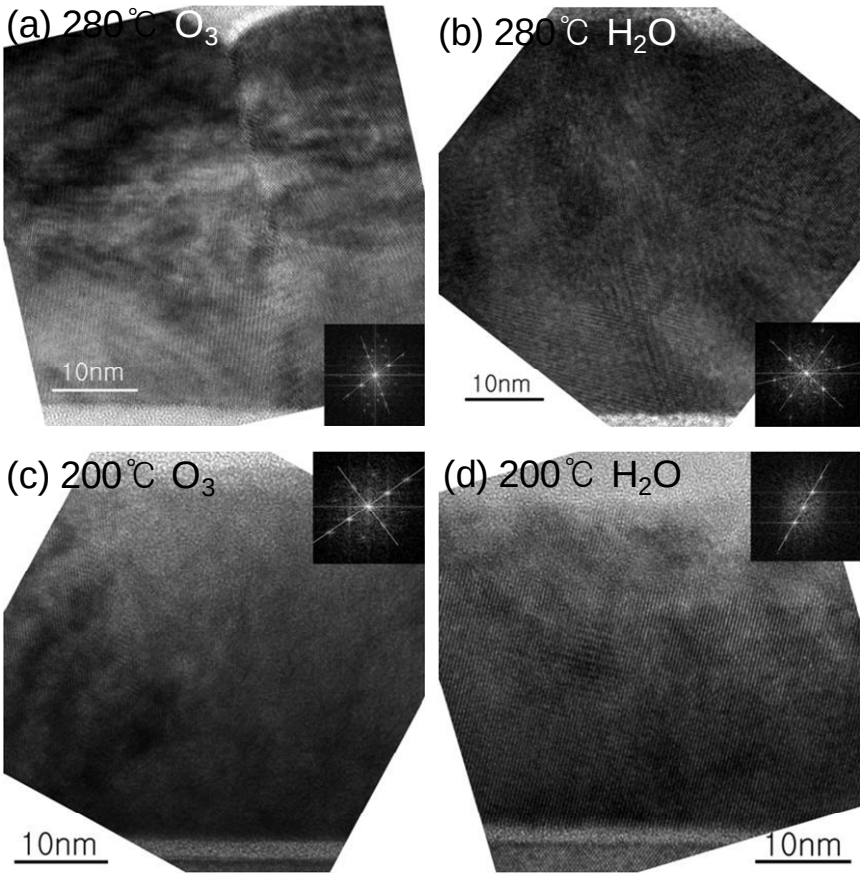

Figure 4.36 HRTEM images of the 45nm-thick HfO_2 films grown under these four different deposition conditions: (a) 280°C O_3, (b) 280°C H_2O, (c) 200°C O_3, and (d) 200°C H_2O after the PDA at 1000°C

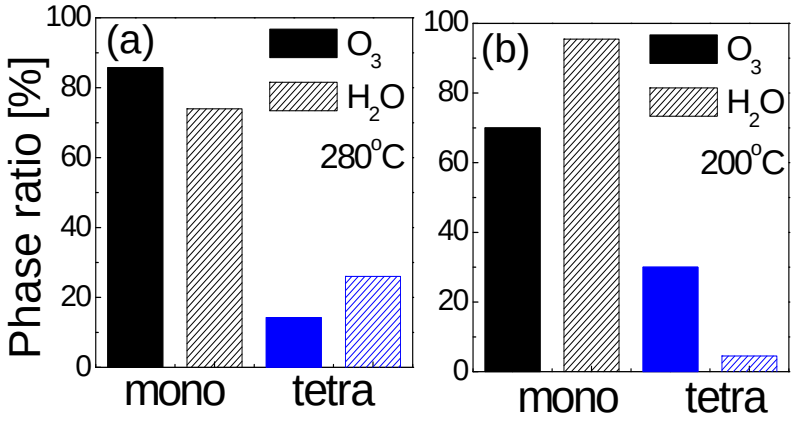

Figure 4.37 Phase ratios of the HfO_2 films using the O_3 and H_2O grown at (a) 280°C and (b) 200°C, from the TEM analysis, via the statistical analysis of the HR images

Deposition condition of HfO_2 films	**Average grain size [nm]**	**Standard deviation [nm]**
280℃ O_3	37.6	9.66
280℃ H_2O	33.4	6.94
200℃ O_3	28.6	8.02
200℃ H_2O	47.7	19.3

Table 4.7 Grain size distribution from the TEM bright field images via statistical analysis of the HR images

The crystallization behavior of the HfO_2 films grown under the four different conditions was further examined as a function of the film thickness for different T_{PDA}'s by measuring the RMS roughness of the films using AFM. Although the RMS roughness does not provide direct evidence of the detailed evolution of crystallographic phases in oxide thin films, the increase in such value could be generally ascribed to the accompaniment of the grain formation by crystallization. SEM images can supplement the AFM data. Figures 4.38 (a)-(d) show the SEM (left panel) and AFM topographic (right panel) images of the 45nm-thick films annealed at 1000^{o}C and deposited under the four different conditions. The morphological images in Figures 4.38 (a) and (b) allowed estimation of the grain sizes in the two cases, which were 39.5±0.8 nm and 31.6±0.8 nm, respectively, which coincide very well with the data shown in the first and second rows of Table 4.6 that were estimated from the TEM. However, the much smoother surface morphologies in Figure 4.38 (c) and (d) did not allow statistically meaningful grain size estimation.

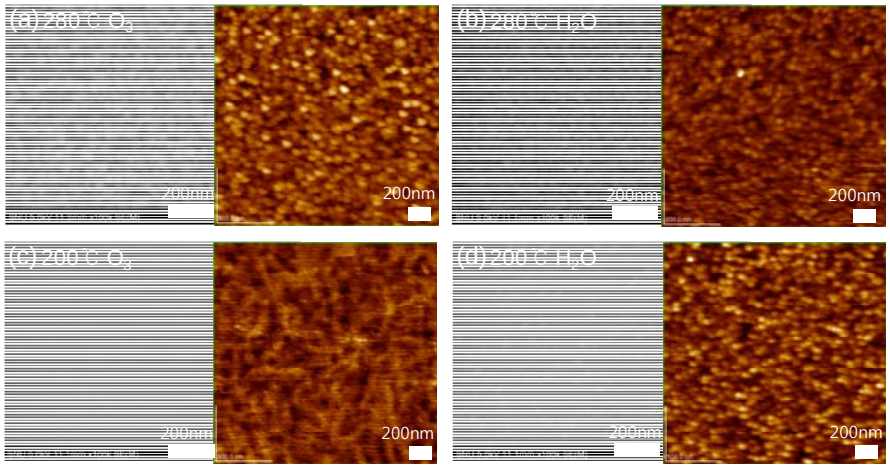

Figure 4.38 SEM (left panel) and AFM topographic (right panel) images of the 45nm-thick films annealed at 1000°C and deposited under these four different conditions: (a) 280°C O_3, (b) 280°C H_2O, (c) 200°C O_3, and (d) 200°C H_2O

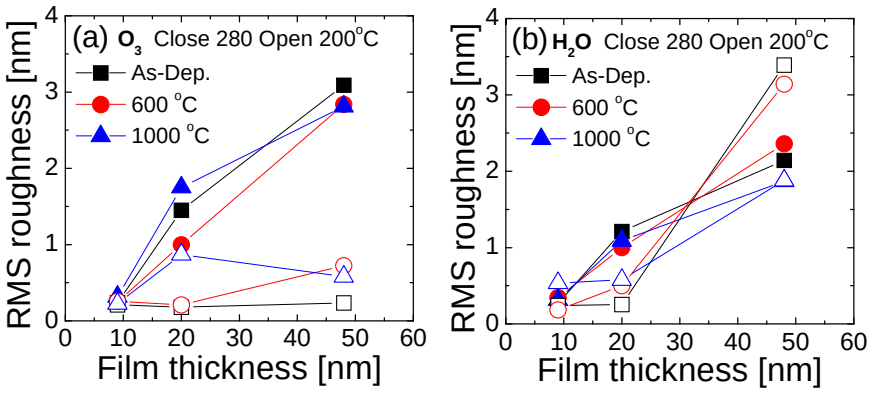

Figure 4.39 Variations in the RMS roughness, measured via AFM of the HfO_2 films deposited using (a) O_3 and (b) H_2O grown on 280°C (closed data) and 200°C (open data) at the as-deposited state, and after the PDA at 600 and 1000°C, respectively, as functions of the film thickness

Figures 4.39 (a) and (b) show the variations in the RMS roughness measured via AFM of the HfO_2 films deposited under the four different ALD conditions, at the as-deposited state, and after the PDA at 600°C and 1000°C, respectively, as a function of the film thickness. For the cases of 280°C O_3, 280°C H_2O, and 200°C H_2O, the RMS roughness generally increased with the increasing film thickness for all three process conditions, which suggests the increased crystallization with the increasing film thickness. This is coincides well with the GAXRD results shown in Figures 4.33 and 4.35. However, the HfO_2 film grown under the condition of 200°C, O3 maintained a very low RMS roughness value irrespective of the thickness in all the PDA conditions. The RMS roughness of the as-deposited film remained at a very low value (~0.2 nm) up to the thickness of 45 nm, which corroborates the complete amorphous structure of this sample. Even after the PDA at 1000°C, the increase in the RMS roughness was very low, which is a remarkable finding considering the obvious crystallization of this sample after the PDA.

4.2.6. Analysis

Next, the chemical binding states of the films grown under the four different conditions were examined via XPS, and the results are correlated with the electrical characteristics. For the XPS examination, no PDA was performed, and the samples for the electrical characterization were annealed under the forming gas condition (see the Experiment section). For the XPS, the SiO_2 film that was thermally grown on Si was also analyzed for reference. In Figures 4.40 (a) and (b), the C 1s and O 1s spectra of the four ALD HfO_2 films and the SiO_2 samples are shown. All the samples showed clear C 1s peaks, of which C-C BE was set at 284.5 eV. The SiO_2 sample showed the lowest C 1s peak intensity, and the HfO_2 samples showed generally high intensities, which suggest the higher adsorption of adventitious carbon from the atmosphere. In addition, the HfO_2 samples showed non-negligible intensities near the BE of 288.5 eV, which coincides with the hydrocarbon peak that was not observed in the SiO_2 sample. This means that the HfO_2 films contained hydrocarbon impurities that were most probably induced by the incomplete ALD reactions. Such non-ideal aspect of ALD cannot be completely eliminated even for the most favorable ALD conditions (280^{o}C O_3 and 200^{o}C H_2O). The O 1s spectra of the HfO_2 samples showed relatively broad peaks that could be deconvoluted into three components that corresponded to the oxygen ions in the HfO_2 (BE ~530 eV), Hf silicate (BE ~531.5 eV), and SiO_2 (BE ~532.5 eV), whereas that of SiO_2 was composed of only oxygen in the SiO_2. The inclusion of the Hf silicate and SiO_2

components in the HfO_2 films was due to the chemical interaction between the HfO_2 films (or the atmosphere during ALD) and the Si substrate, which could be understood more clearly from the variations in the Si 2p XPS spectra shown in Figures 4.40 (c) and (d). In the Si 2p spectra, the signal from the Si substrate (BE ~98-98.5 eV) could be clearly observed due to the thinness of the films (~6 nm). Unlike the BE of SiO_2 (~103 eV), the BEs of the oxide peaks from the HfO_2 films shifted into the lower BE direction, which suggests that the ILs were mostly Si sub-oxides or the Hf silicate. The oxide Si 2p peaks from the HfO_2 films deposited under the different ALD conditions were deconvoluted, assuming that there were Si^{4+}, Si^{3+}, Si^{2+}, and Si^{1+} components. The BE of the Si 2p spectra from the Hf silicate is similar to that of Si^{3+} and Si^{2+} [49], so they are not exclusively included in this deconvolution process. Among the four different ALD conditions, the conditions that involved O_3 resulted in the obviously intense peaks, which suggest that the Si substrate was oxidized by the strong oxidation potential of O_3 at the T_s of 280^{o}C and 200^{o}C. In contrast, the conditions that involved H_2O induced a much lower intensity of the oxide Si 2p peak, which reflects the lower oxidation potential of H_2O compared with O_3. The lower T_s also induced the lower oxide peak intensity for both oxygen sources. These observations are well-correlated with the electrical properties, as shown in Figure 4.41. Figures 4.40 (e) and (f) show the N 1s XPS peak and valence band (VB) spectra. The N1s peaks had certainly non-negligible intensities

compared to the HfO_2 samples, the intensities of which were independent of the ALD conditions. Of course, the SiO_2 film did not show any N 1s peak intensity. This revealed that a non-ideal component of ALD was involved, wherein fragments of the ligands remained and the Hf-N bonding of the Hf-precursor molecules was not completely replaced with the Hf-O bonding in the film. The VB spectra of all the HfO_2 samples are also very similar. Their comparison with the VB of Si provides information on the VB offset between the Si and HfO_2, which is commonly 1.90-1.96 eV. This value is consistent with the theoretical estimations [50-51], but previous reports of experimental results are too extensive, and, thus, were focused on a relative comparison. There are in-gap states that could be ascribed to the presence of impurities, such as C, N, and Si, and only a slight difference in the leakage current - capacitance equivalent thickness (J_g-CET) plots from the different samples for thinner films (< 6 nm), as shown in Figure 4.42, and such characteristics could be understood from the negligible difference in the VB offset and in-gap states. However, the bulk dielectric properties, represented by the k-values of the different HfO_2 layers, and the thickness of IL could be well- correlated to the XPS signals.

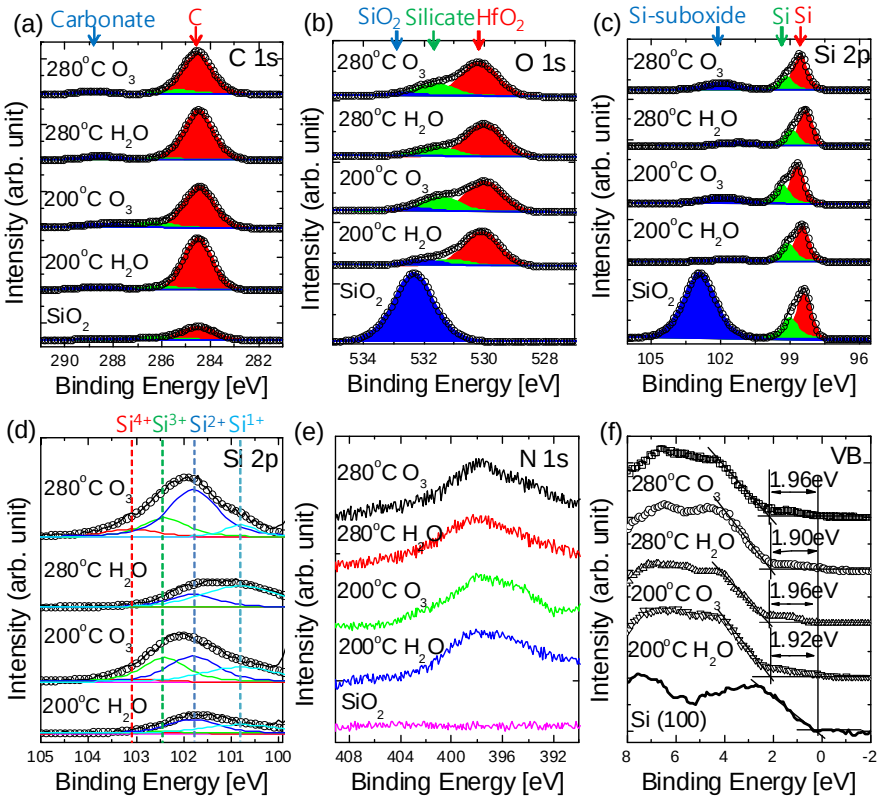

Figure 4.40 XPS spectra of the (a) C 1s, (b) O 1s, (c) Si 2p, and (d) Si 2p that were deconvoluted assuming the Si^{4+}, Si^{3+}, Si^{2+}, and Si^{1+} components, (e) the N 1s, and (f) the valence band for the four different deposition conditions of HfO_2 (280°C O_3, 280°C H_2O, 200°C O_3, and 200°C H_2O) and the thermally grown SiO_2 as references

4.2.7. Electrical properties

Figure 4.41 shows the variations in the CET as functions of the physical oxide thickness (POT) of the HfO_2 films grown under the four different ALD conditions, wherein the POT was limited to ~8 nm in (a) and increased to up to ~18nm in (b). The inverse of the slope of the best-linear-fitted graphs of the CET-POT plot indicated the k value of the HfO_2 films, which were free from the influence of any IL, and the y-axis intercept corresponded to the CET of IL, which includes any possible contribution from the interface with the metal electrode [30]. The CET-POT plots showed a change in their slope at POT ~8 nm, except for the 280^{o}C O_3 condition, so the k-values are not constant throughout the entire thickness range. The estimated k-values are summarized in Table 4.8. In the thin thickness range, all the films were mostly amorphous, so the k-values could be mostly determined by the density of the films. However, the highest k-value of ~12.7 from the 280^{o}C O_3 case was still much lower than that of other reports from the amorphous HfO_2 (~15-17 [30, 32-33, and 35-37]). The k-values of the HfO_2 films from the other conditions were even lower (~10.7), which suggests that the thin as-deposited films generally have a low density, which coincides with the density estimation shown in Figure 4.30 (b). When the films became thicker, some of them started to include crystalline grains even at the as-deposited state, which could have influenced their k-values. The k-values estimated in the POT range of ~9-18 nm were ~17, 26, 22, and 30 for the ALD conditions of 280^{o}C O_3, 280^{o}C H_2O, 200^{o}C O_3, and 200 ^{o}C H_2O,

respectively. The lowest k-value of 17 for the condition of 280°C O_3 suggests that the film maintained its amorphous structure with a slightly increased density, which could be ascribed to the self-annealing effect at the ALD temperature for growing the thicker film. The highest k- value of 30 for the condition of 200°C H_2O suggests that the film came to have tetragonal grains, although they could not be clearly identified from GAXRD perhaps due to the still too small grain size of up to 18 nm of POT. The two conditions also showed higher k-values than in the thinner film cases, which suggests that there was an increase in the crystallinity that contained the non-negligible concentration of the tetragonal phase, which could not be detected via GAXRD.

The y-axis intercept in Figure 4.41 (a) clearly shows that the conditions that involved O_3 induced a thicker IL, the CET of which was ~0.8 nm, whereas the two other conditions that involved H_2O induced an IL CET of as small as ~0.2 nm. This coincided well with the higher and lower oxide peak intensities in the Si 2p XPS spectra in the former and latter cases, respectively, which suggests the higher interfacial oxidation of Si in the former case.

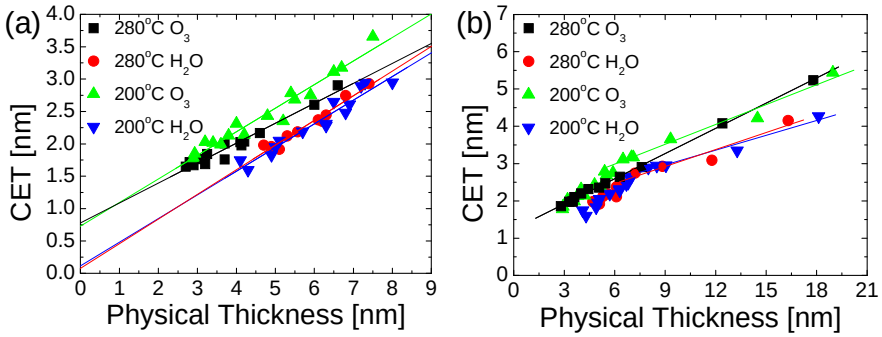

Figure 4.41 CET variations as functions of the physical oxide thickness (POT) for the HfO_2 films grown under the four different ALD conditions, wherein the POT was limited to ~8 nm in (a) and increased to up to ~18 nm in (b)

Deposition condition of HfO_2 films	**Dielectric constant in thin thickness range**	**Dielectric constant in thick thickness range**
280℃ O_3	12.7	17.3
280℃ H_2O	10.2	25.7
200℃ O_3	10.7	22.0
200℃ H_2O	10.7	29.4

Table 4.8 Dielectric constant k values of the thin (less than 8 nm) and thick thickness ranges of the HfO_2 films grown under the four ALD conditions

Figure 4.42 summarizes the J_g-CET plots of the HfO_2 films grown under the four ALD conditions. As the HfO_2 films grown under the different conditions had different flat-band voltages (V_{fb}), J_g was estimated at the gate voltage of V_{fb}-1 V. Within the smallest CET range of ~1.5-2.0 nm, the HfO_2 films grown under the condition of 200°C H_2O showed the lowest J_g level, which could be ascribed to the fluent ALD mechanism in such condition that resulted in the high density and the low impurity concentration. The J_g-CET performance was comparable to the state-of-the-art levels of the TEMAH-H_2O and TEMAH-O_3 ALD processes performed at 345°C, as reported by the IMEC group [18], even though in this study, a much lower T_s (200°C H_2O) was adopted. However, as the CET exceeded ~3 nm, the J_g level of the samples deposited under the conditions that involved H_2O became higher than that of the samples deposited under the conditions that involved O_3 by ~1-2 orders of magnitude. Such result requires further investigation for accurate understanding. Hydrogen content could be different in the various types of the films in this work, which could have quite large influence on the electrical properties. However, quantitative determination of the hydrogen content is generally difficult, so it was not attempted. Meanwhile, the hydrogen might be present in the form of hydrocarbons, so correlating the electrical properties with the carbon concentration could be an indirect indication of correlation between the property and the hydrogen content.

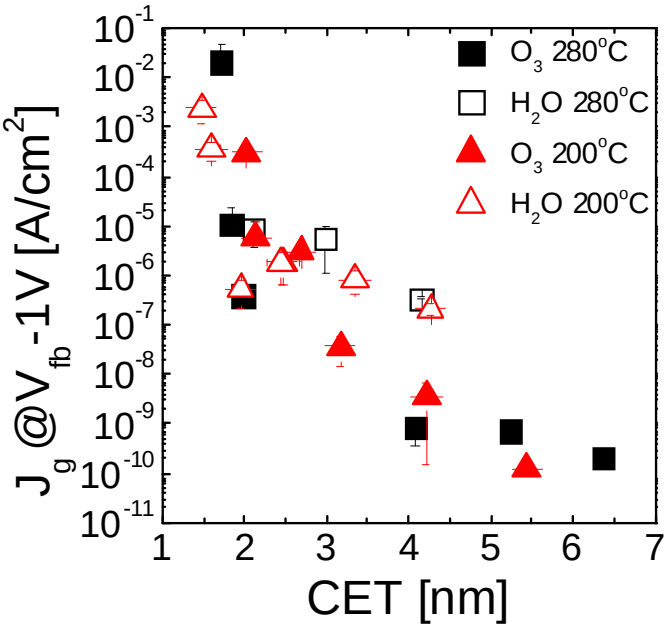

Figure 4.42 J_g-CET plots of the HfO_2 films grown under the four ALD conditions

4.2.8. Conclusions

The effects of O_3 and H_2O as oxygen sources on the ALD of HfO_2 films grown at substrate temperatures of 160-360^oC were examined in terms of their growth characteristics and structural evolution upon the thickness increase and post-deposition annealing. While the ALD process that involved H_2O was achieved well at a temperature as low as 160^oC, the ALD in which O_3 was used required substrate temperatures of 240-280^oC to induce a fluent ALD reaction. This could be ascribed to the proton-induced ligand exchange reaction in the case of the ALD with H_2O, whereas the O-radical mediated ALD reaction appeared to require supply of thermal energy to overcome its rather high activation energy. According to these different ALD mechanisms, the HfO_2 films grown at 200^oC and 280^oC for the ALD that involved H_2O and O_3, respectively, showed the highest density. The HfO_2 films with a low density or (and) a high carbon-impurity concentration crystallized to the tetragonal phase after the PDA at 600^oC, whereas the thin film with both a low density and high carbon impurity retained the highest portion of the tetragonal phase (~30%) even after the PDA at 1000^oC. While the majority phase of the crystalline materials was monoclinic phase by the increasing thickness or PDA temperature, all the HfO_2 films contained a non-negligible concentration of the tetragonal phase, which was found from the extensive and detailed HRTEM study. This could be related to the presence of the film surface with a lower energy for the phases other than the monoclinic phase. The density of the thin as-deposited films (< 8 nm) was

important in the determination of the bulk dielectric constant, and the bulk dielectric constants of the thicker films (8-18 nm) were contributed by the (partial) crystalline phase and the density. The best electrical performance was achieved in the HfO_2 film grown at 200^oC with H_2O due to the minimum-involvement of the interfacial oxide layer and the high bulk density of the film.

4.2.9. References

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4.3. ALD HfO_2, TiO_2 on high mobility substrate

4.3.1. Introduction

Beyond 10 nm nanoscale device, non-Si channel materials are favorable to required continuing the scaling of the device in not only planar structure but also 3-dimensional structure. Ge have a promising candidate why it has a highest hole mobility among semiconductor materials. In addition, GaAs is one of promising material among several III-V semiconductors is needed for high electron mobility with wide band gap.

However, there are a lot of reports about HfO_2 film deposited on high mobility substrate by ALD, the reaction of substrate is occurred during the deposition process. This result degraded structural and electrical properties. [1,2] The representative phenomenon of degradation is large hysteresis voltage of C-V curves, distorted shape of C-V curve, large frequency dispersion, and large interface trap density, since the substrate is oxidized by oxygen source, and then reacts and intermixes with high-k layer which result electrically active defects near the interface. [1,2] Ge and III-V semiconductors have unstable interface oxide what is volatile so desorbed from the surface and penetrate through high-k layer that develop trap charges with defects in high-k layer, and poor interface quality which cause interface trap density (D_{it}). [3] Therefore it is required that surface treatment or passivation layer at interfacial layer for suppressing the intermixing of high-k dielectric and substrate. In a same manner, oxygen source of ALD process

is important since O_3 make deteriorate the native oxide due to its strong oxidation power, so H_2O began to getting an attention again. There are some reports about passivation the surface, which are nitridation of surface [4-7], Si passivation layer, plasma oxidation [8-12], and thermally grown oxide [13-14], high pressure oxidation for Ge substrate [15-16], and Al_2O_3 passivation layer [17], sulfur passivation [18-23], plasma treatment of surface for III-V substrate. [24-25]

That is, defective oxide at interface was formed by oxidation of high-mobility substrate during high-k ALD process, so oxygen source of ALD process is important to improve the interface quality and structural and electrical properties of high-k dielectric gate dielectric on high-mobility substrate.

In addition, these high mobility substrates have low resistance of thermal budget. Ge is known as defective sub oxide which is volatile is formed at > 430 ^{o}C. [26] There are some reports that effect of deposition temperature on the structural and electrical properties of Al_2O_3 and ZrO_2 high-k films on a Ge substrate. Increase the deposition temperature of Al_2O_3 on Ge induces intermixing of Al_2O_3 with Ge interface oxide layer which cause the increase of surface roughness. At high deposition temperature, interfacial Ge-oxide was distinctively depleted, arise the trap levels near the interface between ZrO_2 and Ge substrate [27-28] The implementation of atomic layer deposited high-k dielectrics on high-mobility substrates has the

potential to become a mass production compatible process. However, atomic layer deposition (ALD) has only possible certain temperature range what is an ALD window. Therefore, the HfO_2 films using O_3 and H_2O oxygen source at various deposition temperature mentioned above is proper to apply on high mobility substrate.

There are some reports about several high-k dielectrics on high mobility substrate such as Al_2O_3, La_2O_3, $LaLuO_3$, $LaYO_3$, etc. [30-32] However, HfO_2 has still an advantage with respect to more conventional and popular ALD HfO_2 deposition process contained relatively easy to handle the Hf precursor than Lanthanide precursors. HfO_2 high-k dielectrics as gate dielectric have been already adopted in the semiconductor industry and particularly applied in the mass production of Si-based MOSFETs. [33-35] Atomic layer deposition (ALD) has many advantages in the formation of gate dielectric thin films for extremely scaled planar or three-dimensional structured devices such as FinFET, nanoribbon, gate all around (GAA) devices, due to its self-limiting growth behavior, which confirms a low leakage current, high dielectric constant, and atomic-level precise thickness control. Furthermore atomic layer deposited HfO_2 on lower deposition temperature has a possibility to have higher-k value by crystallization into tetragonal phase due to carbon impurity without degradation of electrical property.

However, more studies are required to fabricate Hf-based dielectric

films with even higher-k values (k > 30) for further scaled MISFETs that require an equivalent oxide thickness (EOT) < 1 nm. [34] Besides, there is a difficult but greater challenge to apply ALD-processed HfO_2 to high-mobility channel materials such as III-V or II-V compound semiconductors for the n-type MISFET and Ge for the p-type MISFET [34-35]. These challenges are known to be caused by the unstable interfaces between the HfO_2 film and the high-mobility substrates [1, 36-38], the status of which is largely influenced by the detailed ALD conditions. Several other high-k dielectrics, such as Al_2O_3, La_2O_3, and $LaLuO_3$ [30, 39-42], have been adopted for the high-mobility substrates, but it might be best if the use of HfO_2 can be extended to these substrates considering its mature process equipment, conditions, and contamination-control protocols in mass-production lines.

4.2.2. Experimental

The HfO_2 films were deposited on deionized water(DI water)-diluted, hydrofluoric (HF 1:20 solution) of hydrochlorine (HCl 25wt% solution) acid-cleaned and/or $(NH_4)_2S$ solution dipped n/p-type Ge or GaAs(100) wafers via ALD at substrate temperatures (T_s) of 160-360^oC, using TEMAHf as the Hf-precursor and different oxygen sources (H_2O and O_3). O_3 was generated by flowing a mixture of O_2 (1,350 sccm) and N_2 (10 sccm) into an ozone generator (Astex, AX8200). The ozone concentration was fixed at 170 g/m^3. The optimized condition of the Hf-precursor pulse-Ar purge-H_2O (or O_3) pulse-Ar purge time was 3-20-3-10 s, respectively, where an Ar purge gas flow rate of 200 standard cubic centimetres per min (sccm) was adopted. The Hf-precursor vapor was achieved by heating the Hf-precursor canister to 60^oC and transporting it into the cross-flow-type ALD reactor, which is capable of processing an 8-inch-diameter wafer, with the help of Ar carrier gas with a flow rate of 200 sccm. The deionized water with which a steel canister was filled was cooled down to 5^oC to achieve the appropriate H_2O vapor pressure.

The thickness of the HfO_2 film was measured with a spectroscopic ellipsometer (SE, ESM-300, Wollam Co.). The crystalline structure of the HfO_2 film was analyzed via glancing angle incidence X-ray diffraction (GAXRD, X'Pert PRO MPD, PANalytical Co., X-ray incidence angle 2^o). The surface morphology was examined with a scanning electron microscope (SEM, S-4700, Hitachi) and an atomic force microscope (AFM, JSPM-5200,

JEOL Co.). The root-mean-squared (RMS) roughness of the thin films was measured with the same AFM. The density and roughness of the thin films were measured via X-ray reflection (XRR, using the same equipment as in the XRD). The The chemical bonding states of the HfO_2 films were examined with the X-ray photoelectron spectra (XPS, Sigma Probe, ThermoVG) using a monochromatic Al Kα source (1486.6 eV) to excite the photoelectrons. The positions of all the peaks were calibrated for the C 1s peak of the adventitious carbon-carbon binding energy to be assigned at 284.5 eV. The carbon impurity concentration was confirmed via Auger electron spectroscopy (AES, Perkin-Elmer 660) in the depth profiling mode, which is performed via Ar^+ ion sputtering.

To examine the electrical property, metal-insulator-semiconductor (MIS) capacitors were fabricated with sputter-deposited Pt top electrodes through a shadow mask with 300 μm-diameter holes. Forming gas annealing was performed to passivate the dangling bonds at the interface between the oxide and the substrate under a H_2 (5%)/N_2 (95%) mixture gas atmosphere at 400^{o}C for 10 min. The capacitance-voltage (C-V) was measured using an HP 4194A impedance analyzer at the frequency of 100 kHz and Agilent LCR meter, 4284A with Keithley switching system 708A. The oxide leakage current (J_g) was investigated using an HP 4140B picoammeter/DC voltage source. The Pt gate was biased while the Si substrate was grounded during the electrical measurements. The capacitance equivalent thickness (CET)

was estimated from the accumulation capacitance values when the films were thick enough (> ~10 nm), and from the fitting of the C-V curves to the theory using the CVC program.

4.2.3. ALD HfO_2 on Ge substrate

All of high-k dielectric on Ge substrate is processed together with Si substrate at once for confirming the thickness and electrical property. HfO_2 using O_3 and H_2O oxygen source and lower deposition temperature had adopted on high-mobility substrate. In a same manner of HfO_2 using O_3 and H_2O on Ge, the impurity in the film was investigated. Figure 4.43 shows the AES depth profile of HfO_2 films using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200 ^oC. The growth behavior of growth rate and film density is already well investigated in figure 4.30.

Figure 4.43 shows the AES depth profiling results of HfO_2 films grown on Ge at four different deposition conditions. The condition of 280^oC O_3 had the lowest carbon impurity contents (< 5 atomic %), which indicates that the ALD reaction fluently occurred under this condition. The Hf/O ratio was constant throughout the film thickness. In the other cases of the films of 280^oC H_2O, 200^oC O_3, 200^oC H_2O, as shown in Figure 4.43, had a high carbon impurity concentration, and the Hf/O ratio was not constant throughout the film thickness. It was diffenent with previous result of Si substrate that 280^oC H_2O show larger carbon contents. However, it is certain that carbon content is decrease as decline of deposition temperature which means H_2O is more effective oxygen source toward the low temperature. This is well correlated with growth behavior of growth rate and film density in figure 4.30.

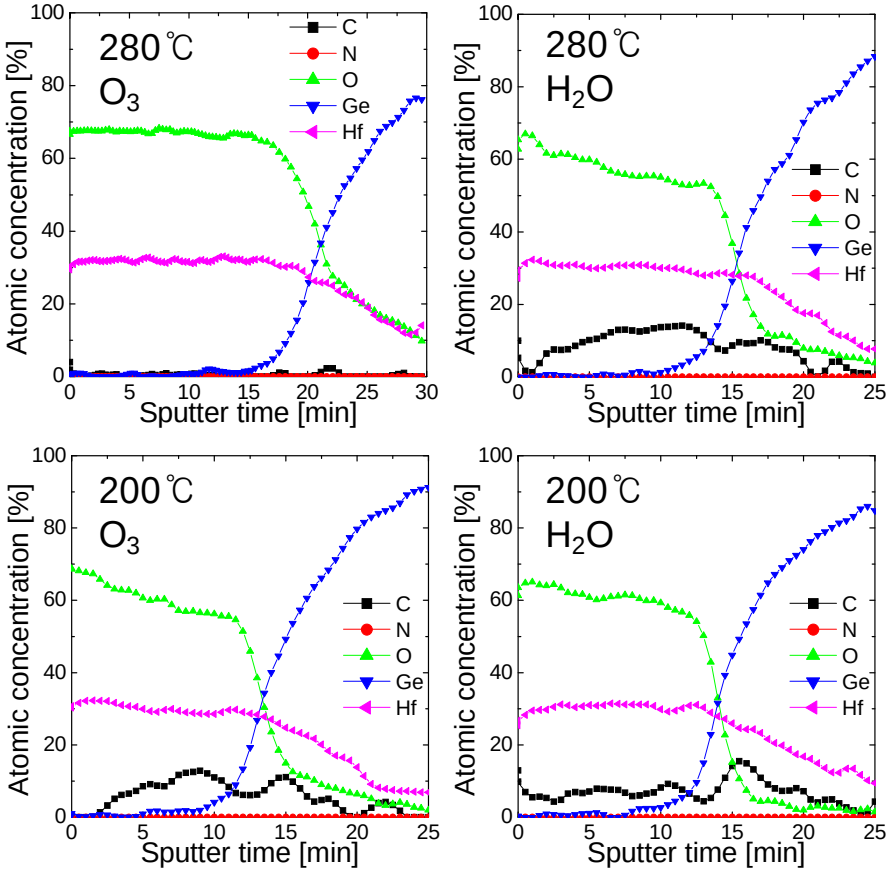

Figure 4.43 AES depth profile of HfO_2 films using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200 °C.

The electrical property was examined that figure 4.44 represent C-V curves of HfO_2 films(6.5 nm) using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200 ^oC with annealing effect on 450, 600 ^oC. HfO_2 in condition of 280^oC O_3 shows large hysteresis voltage over 1V, it is still maintained after 450, 600 ^oC PDA. The maximum capacitance was decreased as PDA that may be due to interface reaction between HfO_2 and Ge substrate and volatile suboxide of GeO is caused over 430 ^oC. [26] After 600^oC anealing, HfO_2 film crystallized to monoclinic phase with no advantage in terms of dielectric constant in case of 280^oC O_3 as shown at figure 4.33. On the other hand, 200^oC O_3 exhibit C-V curves with reduced hysteresis voltage which is identical in previous report. [17]

This is because intermixinig of HfO_2 and Ge substrate by thermal energy was reduced. In addition, there is a merit with regard to higher dielectric constant and smaller CET related to increased maximum capacitance. Figure 4.34 is shown that HfO_2 in condition of 200^oC O_3 is crystallized by tetragonal structure over 600^oC annealing. However, HfO_2 using H_2O oxygen source displayed seriously distorted C-V curves due to severe leakage current. 280^oC H_2O after 600^oC PDA represents very high capacitance even in small voltage region, this suppose 280^oC H_2O is crystallized to tetragonal phase in figure 4.34.

Figure 4.45 indicate C-V curves of HfO_2 films using O_3 and H_2O oxygen source with SiON, AlON passivation layers grown on Ge at

deposition temperature of 280^{o}C with annealing effect on 450, 600 ^{o}C. Refer to previous report [17], the SiO_xN_y 1, 2 nm, and AlO_xN_y 1 nm of passivation layer had inserted between HfO_2 and Ge substrate for passivation the intermixing or reaction. SiON layer has effectively reduced the hysteresis voltage but recuced capacitance too. In the case of HfO_2 using H_2O make better than HfO_2 without the passivation layer, but it is still distorted while not overcome the severe leakage current.

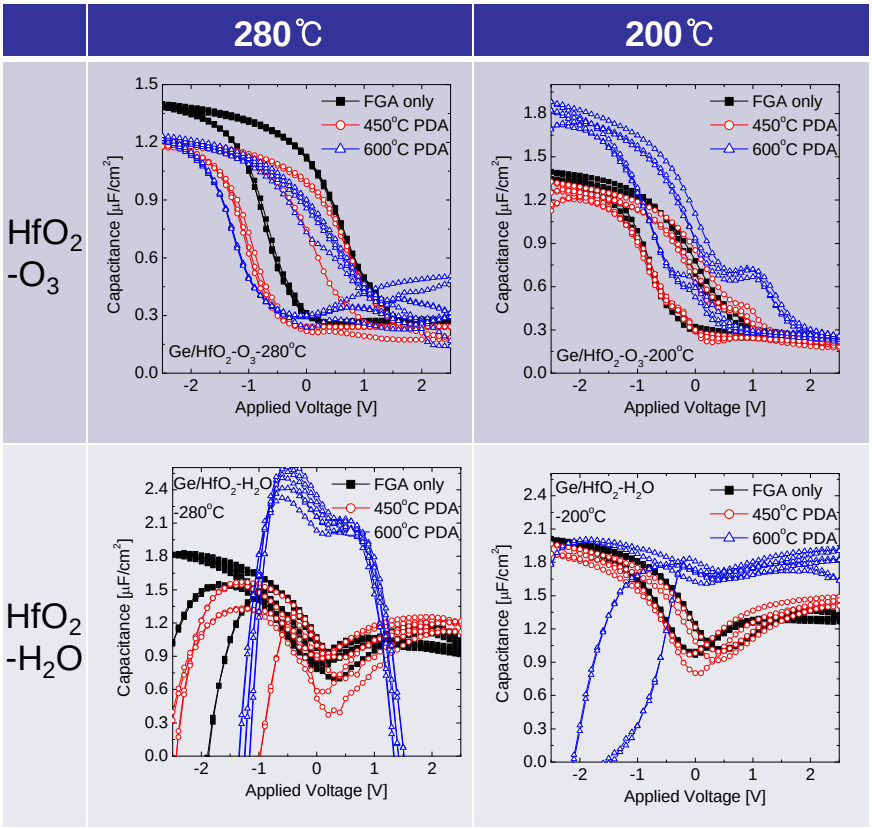

Figure 4.44 C-V curves of HfO_2 films using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200 °C with annealing effect on 450, 600 °C.

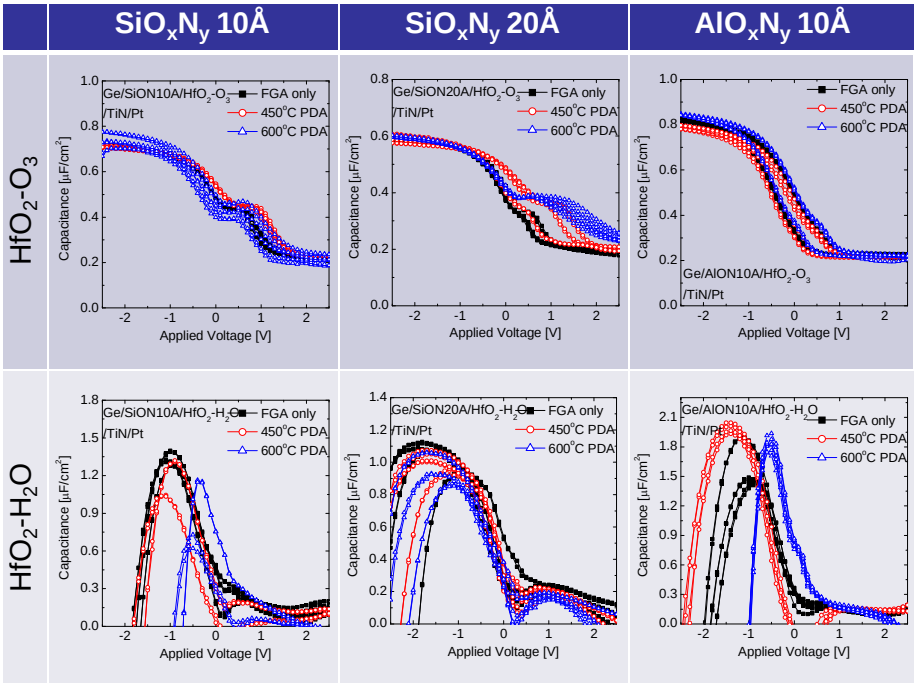

Figure 4.45 C-V curves of HfO_2 films using O_3 and H_2O oxygen source with SiON, AlON passivation layers grown on Ge at deposition temperature of 280°C with annealing effect on 450, 600 °C.

RTO(Rapid thermal oxidation) annealing effect was examined in HfO_2 using O_3 and H_2O oxygen source. RTO was processed during 1 min. by RTA(rapid thermal annealing) under O_2 atmosphere. HfO_2 films in condition of as-dep., FGA only, RTO 450 ^oC, RTO 600 ^oC were compared in figure 4.46. RTO 600 ^oC results increase of hysteresis voltage in the case of HfO_2 using O_3. HfO_2 using H_2O is previously represents distorted C-V curves by severe leakage current, and it is improved by RTO 600^oC. Figure 4.47 show improved frequency dispersion property of HfO_2 using O_3 and H_2O by RTO 600^oC. RTO 600 ^oC improved frequency dispersion why induce curing the defects in HfO_2, and remove the impurities.

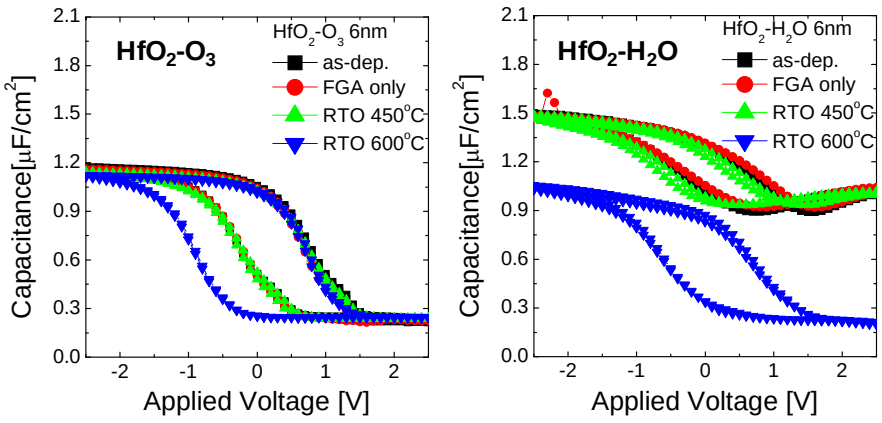

Figure 4.46 C-V curves of HfO_2 films using O_3 and H_2O oxygen source grown on Ge with RTO(rapidi thermal oxidation) effect on 450, 600 °C.

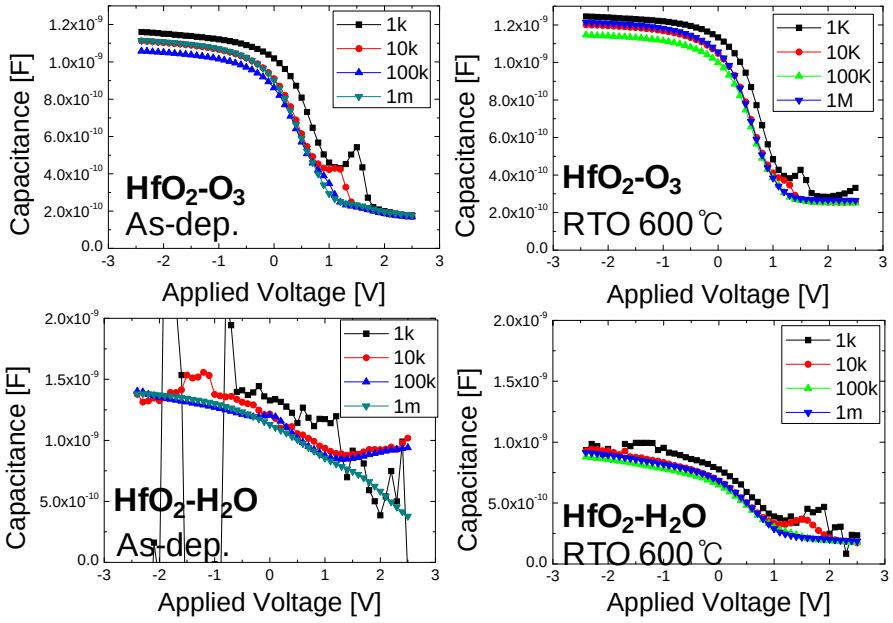

Figure 4.47 Frequeny dispersion of HfO_2 films using O_3 and H_2O oxygen source grown on Ge with RTO(rapidi thermal oxidation) effect on 600 °C.

For solve the problem of leaky HfO_2-H_2O, thickner physical thickness (5.5, 6, 6.7, 7.5 nm) of HfO_2 were examined. Process optimization of H_2O feeding and purging time in our ALD system was tried in advance. However, it is still showed distorted C-V curves in condition of 7.5nm thick HfO_2. (data not shown)

Next 14nm-thick HfO_2 was examined, C-V curves are scarcely obtained in figure 4.47. Similar with previous results, 280^oC O_3 showed huge hysteresis voltage, and it is reduced on 200^oC O_3. 200^oC H_2O showed saturated C-V curve with smaller hysteresis voltage even though there is hump, and 280^oC H_2O represented worst result which is correlated with above AES impurity data. Figure 4.49 shows frequency dispersion of HfO_2 films(14 nm) using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200^oC. 280^oC H_2O coule not be obtained normal C-V curves according to the change of frequency due to leakage current. 200^oC O_3 showed better frequency dispersion than 280^oC O_3, in a same manner with hysteresis voltage. Especially, increase of capacitance at inversion region in low frequency was represents. Accumulation capacitance was effective under 100kHz. 200^oC H_2O showed relatively decrease of capacitance at strong inversion region.

The Al_2O_3 passivation layer of 10, 15 ALD cycle was inserted between HfO_2 and Ge substrate. Figure 4.50 shows C-V curves of HfO_2 films(14 nm) using O_3 and H_2O oxygen source with Al_2O_3 passivation layer grown on Ge

at deposition temperature of 280^{o}C, 15 cy of Al_2O_3 passivation layer is effectively improved the hysteresis voltage with small decrease of capacitance. More detailed discussion will be continued with additional analysis data.

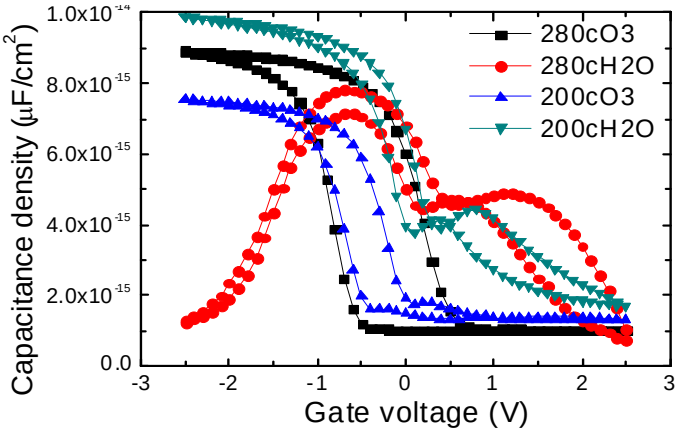

Figure 4.48 C-V curves of HfO_2 films(14 nm) using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200°C.

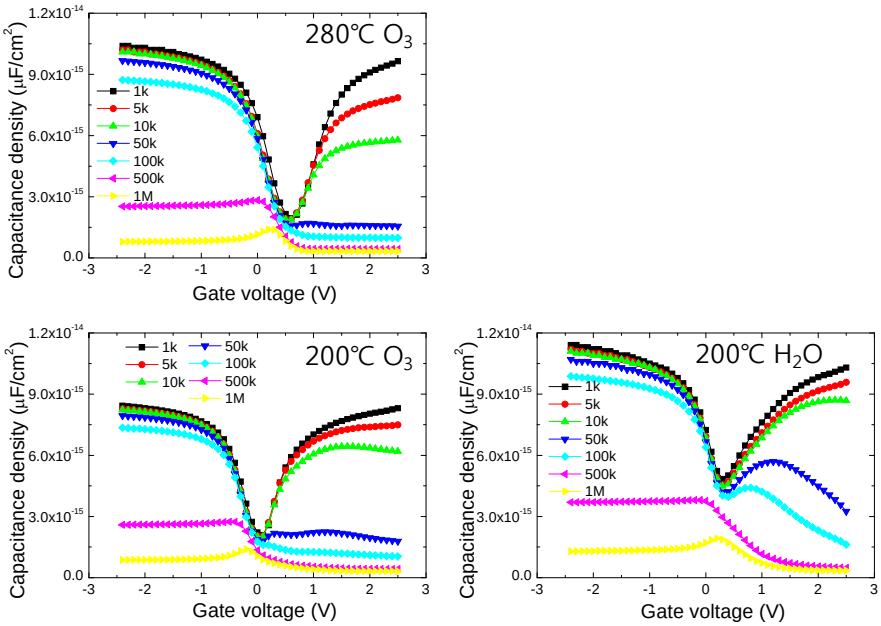

Figure 4.49 Frequency dispersion of HfO_2 films(14 nm) using O_3 and H_2O oxygen source grown on Ge at deposition temperature of 280 and 200°C.

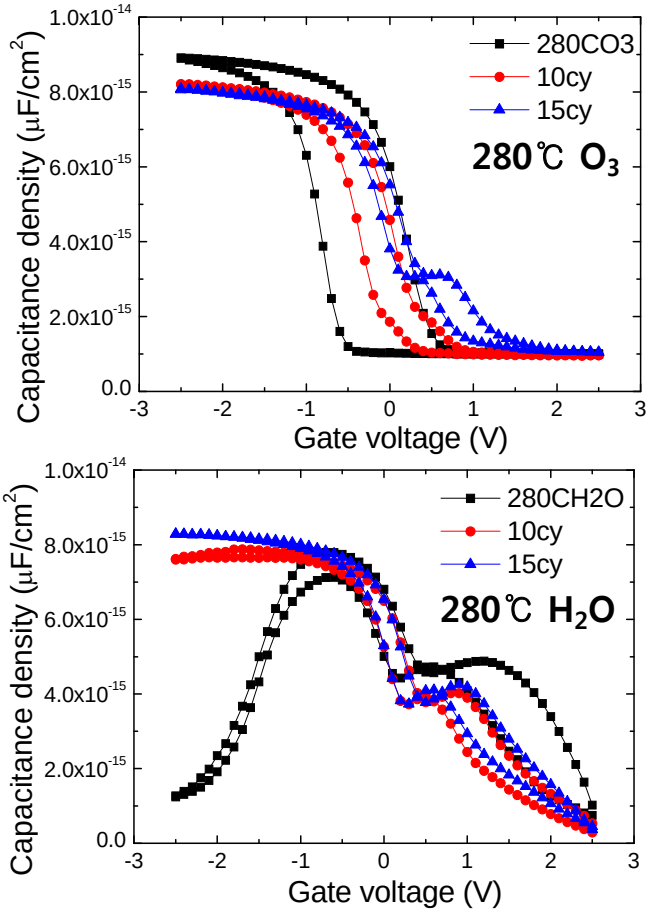

Figure 4.50 C-V curves of HfO_2 films(14 nm) using O_3 and H_2O oxygen source with Al_2O_3 passivation layer grown on Ge at deposition temperature of 280°C.

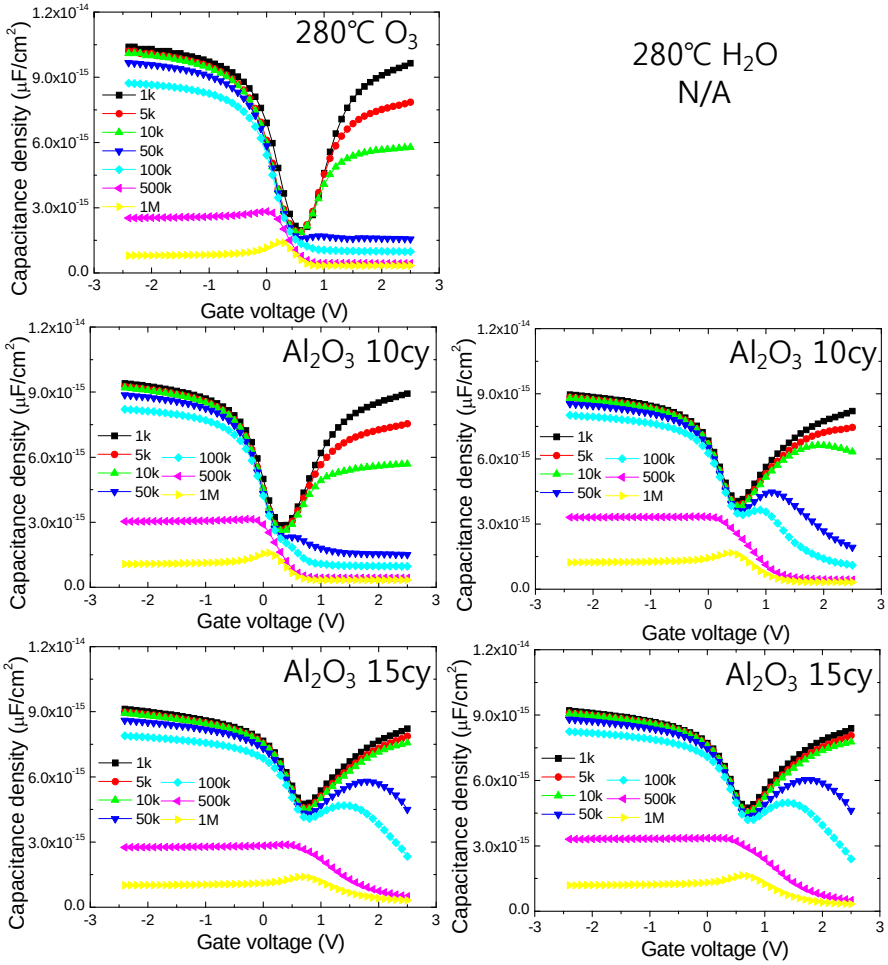

Figure 4.51 Frequency dispersion of HfO_2 films(14 nm) using O_3 and H_2O oxygen source with Al_2O_3 passivation layer grown on Ge at deposition temperature of 280°C.

4.2.4. ALD TiO_2 on Ge substrate

So far, HfO_2 represented neglibile improvement even after several treatments and insertion of passivation layer. Therefore, TiO_2 high-k dielectric which has higher-k value is compared with HfO_2, since it cause smaller CET with passivation layer due to higher-k value. TiO_2 high-k dielectrics using both O_3 and H_2O oxygen source were investigated, however TiO_2 using H_2O showed poor electrical property due to severe leakage current. TiO_2 has crystal structure after PDA of anatase phase and high leakage current due to small band gap even inserted the passivation layer. In addition, TiO_2 using O_3 was compared with HfO_2 in terms of electrical property.

Figure 4.52 shows C-V curves of the TiO_2 films with SiO_2 or Al_2O_3 passivation layer grown on Ge. The C-V curve of TiO_2 without passivation was distorted due to a high leakage current, originating from the low conduction band offset between TiO_2 and Si. By inserting passivation layers such as SiO_2 and Al_2O_3 between the Si substrate and the TiO_2 dielectric layer, a normal C-V curve was obtained. At least 20cy (24Å) of ALD Al_2O_3 was required to prevent all distortions in the C-V curve. The hysteresis voltage of C-V curves was minimized when the SiO_2 thickness was 21Å.

The crystalline structure after PDA was studied since TiO_2 is normally crystallized into anatase or rutile structure, the dielectric constant is significantly different. Dielectric constant(k) of anatase is 30-40, and rutile

structure is 90 along the a-axis with band gap of 3.2 eV, 170 along the c-axis with band gap of 3.0 eV. Rutile TiO_2 has a great advantage even for small band gap. Figure 4.53 shows XRD peaks of the TiO_2 films with SiO_2 or Al_2O_3 passivation layer grown on Ge substrate. The effect of PDA on the crystallinity of dielectric films was analyzed. The as deposited dielectric films were amorphous. After PDA (600 ^oC 30s N_2 ambient), the dielectric films with relatively thick dielectric films (>90Å) were crystallized as an anatase phase.

After optimize the thickness of passivation layer, it is adopted itself and nitrized passivation layer. C-V curves of the TiO_2 and HfO_2 films with with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Ge substrate is observed in figure 4.54. TiO_2 without passivation represented severely distorted C-V curve due its low conduction band offset (CBO) with Ge, which results high leakage current. HfO_2 without passviation shows a large hysteresis voltage due to intermixing between the HfO_2 and Ge substrate.

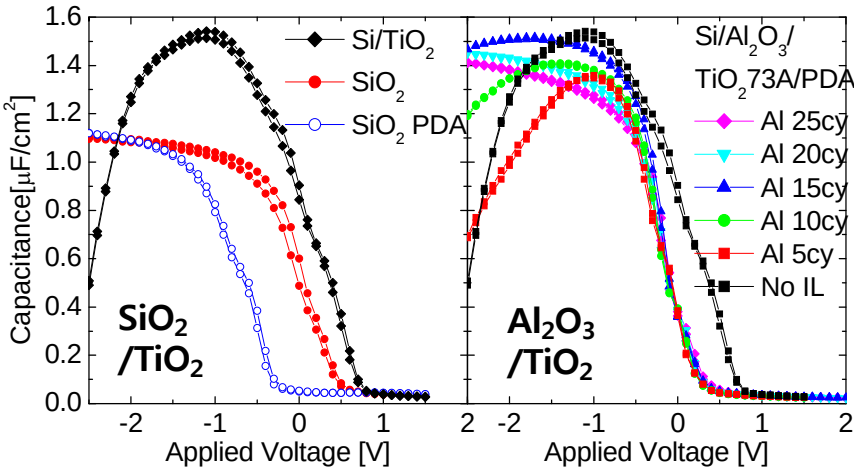

Figure 4.52 C-V curves of the TiO_2 films with SiO_2 or Al_2O_3 passivation layer grown on Ge

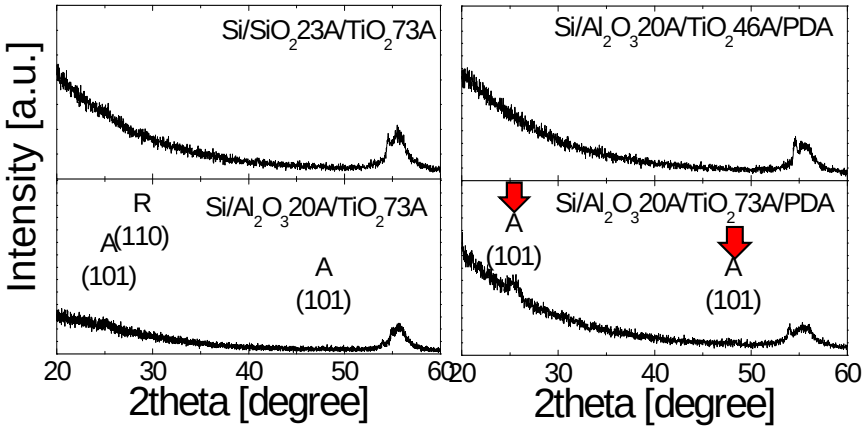

Figure 4.53 XRD peaks of the TiO_2 films with SiO_2 or Al_2O_3 passivation layer grown on Ge

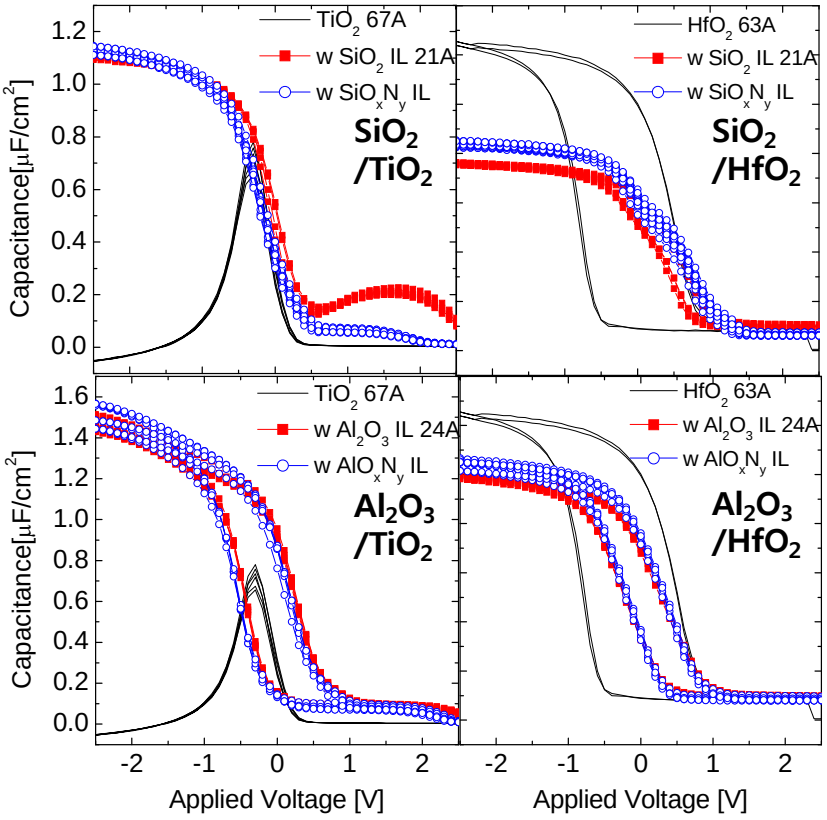

Figure 4.54 C-V curves of the TiO_2 and HfO_2 films with with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Ge

The hysteresis voltage extracted from C-V curves and CET CET values of the TiO_2 and HfO_2 films with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Si and Ge substrates are shown in figure 4.55. The SiO_2 passivation layer dramatically reduces hysteresis. Our explanation of this phenomena is that the implemented SiO_2 layer can effectively suppress the out-diffusion of gaseous GeO_x ($x<2$) , which is thought to be the cause of a poor interface and therefore large hysteresis voltage. The Al_2O_3 passivation layer had a merit compared to SiO_2 in terms of CET, although it had a larger hysteresis. It is known that stable interfaces are formed between Al_2O_3 and GeO_2. Also, Al_2O_3 has advantages in that it has a higher-k value than SiO_2 while still having a large enough bandgap, making it preferable for better insulating property.

The interface trap density is important to high-k dielectric with non-Si substrate that is mentioned above. The interface trap density (D_{it}) was measured by the conductance method. D_{it} values at the midgap of the Ge substrates were higher than the values of the Si substrates (~$3x10^{11}$ $cm^{-2}eV^{-1}$). Nitridation of the passivation layers increases the D_{it} values contrary to expectation. In the case of HfO_2 dielectrics showed higher D_{it} values than TiO_2.

Figure 4.57 represents the J_g at -1.5V vs. CET plots of the TiO_2 and HfO_2 films with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Si and Ge substrates. The TiO_2 without passivation was very leaky. Both the

SiO_2 and Al_2O_3 passivation layers reduced leakage current density. However, the Al_2O_3 passivation layer was profitable than SiO_2 in terms of CET value due to the relatively larger dielectric constant of Al_2O_3. Comparing TiO_2 and HfO_2, they have both advantages and disadvantages regarding CET and leakage current density, and the insulating properties lie on the same slope of line.

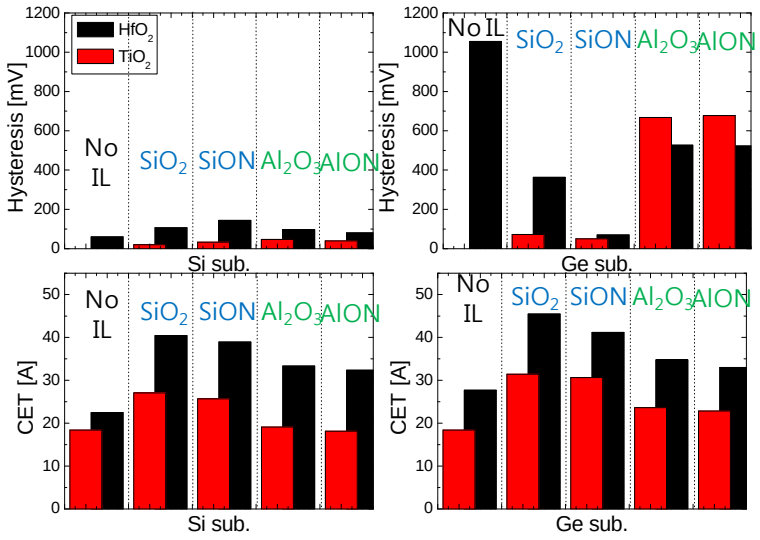

Figure 4.55 Hysteresis voltage and CET values of the TiO_2 and HfO_2 films with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Si and Ge

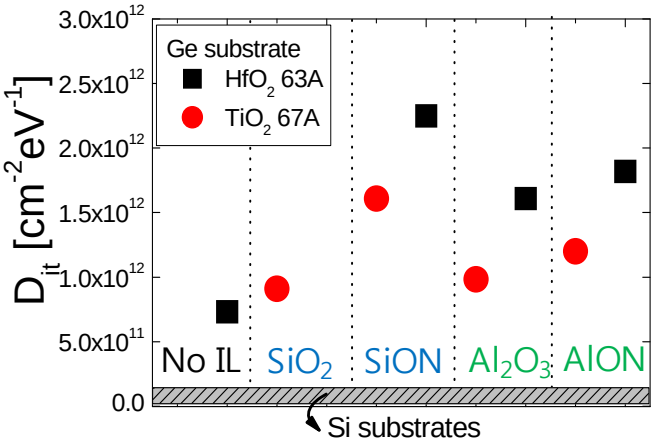

Figure 4.56 Interface trap density of the TiO_2 and HfO_2 films with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Si(the shaded area) and Ge

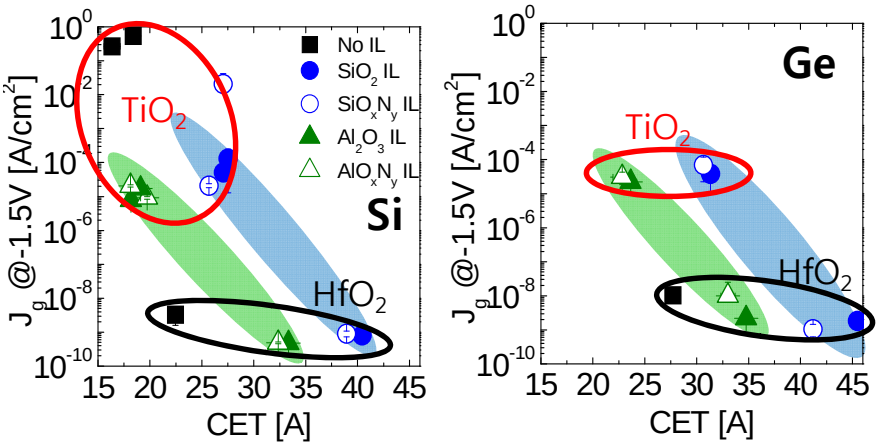

Figure 4.57 J_g at -1.5V vs. CET plots of the TiO_2 and HfO_2 films with SiO_2, SiON, Al_2O_3, and AlON passivation layer grown on Si and Ge

TiO_2 have more benefits on Ge substrate than HfO_2 which has a limit to improve. Therefore, it is focused on TiO_2 with passivaion layer on Ge substrate. In addition, Al doping in ratio of 1/60 was added to TiO_2 during deposition since Al doping is known effectively reduced leakage current. C-V curves of the TiO_2 and Al-doped TiO_2 films with with SiO_2, SiON passivation layer grown on Ge substrate is observed in figure 4.58. TiO_2 and ATO without passivaion layer showed non-reasonable C-V curves due to severe leakage current, since band gap and band offset of TiO_2 is small with almost no barrier with substrate. SiO_2, SiON passivation layer effectively made a reduction of leakage current and hysteresis voltage. Hysteresis voltage was plotted in figure 4.60; it is improved below 70 mV. The insulator property of J_g at -1 V vs. CET plots of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge is shown in figure 4.61. Three kinds of thicknesses of TiO_2 and ATO represented similar leakage current density with different CET, since passivation layer is mainly reduced leakage current. Additional CET scaling is requied, so it will be followed later in this study. Interface trap density (D_{it}) of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge according to the TiO_2 thickness is shown in figure 4.62. Passivation layer is effectively reduced Dit due to suppression of interface reaction and GeO volatilization from interface to upper high-k oxide. The best condition was $D_{it} \sim 1.3x10^{11}cm^{-2}eV^{-1}$ in stack of SiO_2 20A/TiO_2 45A.

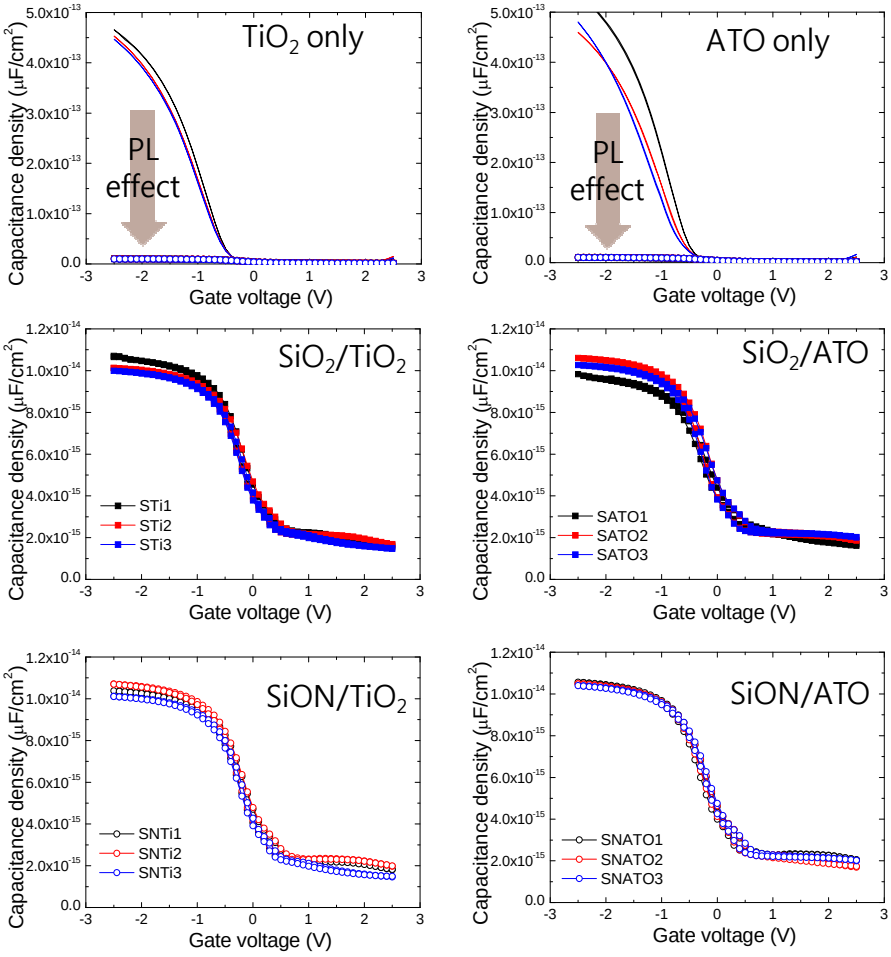

Figure 4.58 C-V curves of the TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge

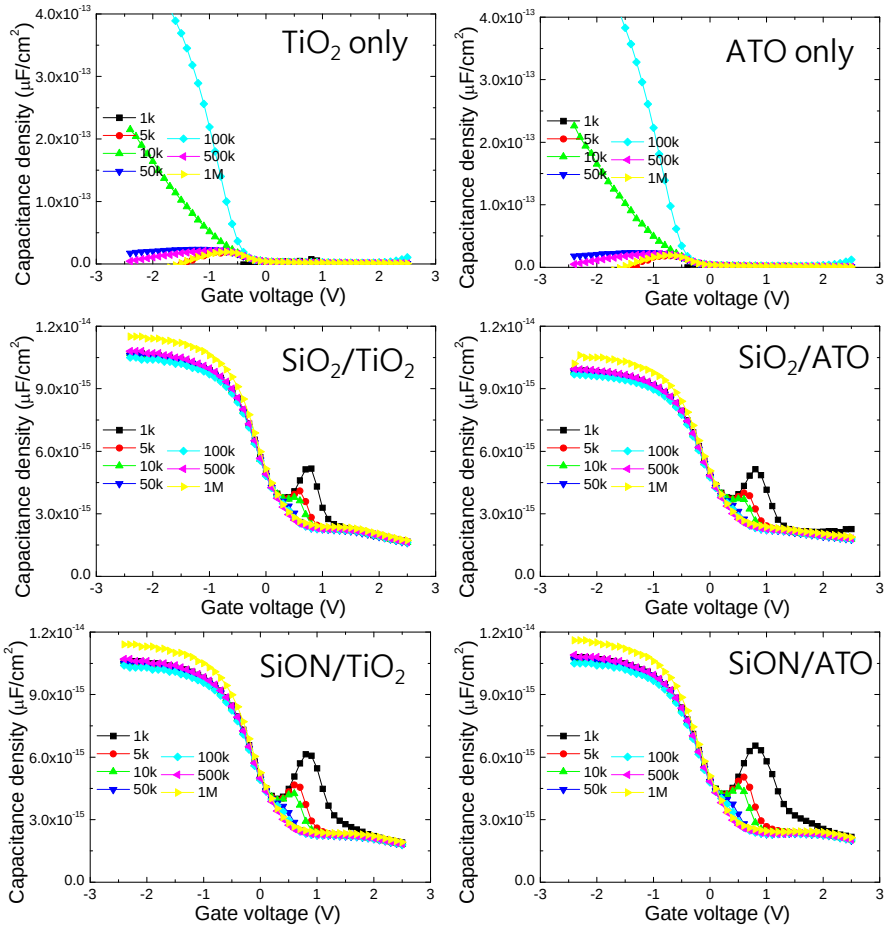

Figure 4.59 Frequency dispersion of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge

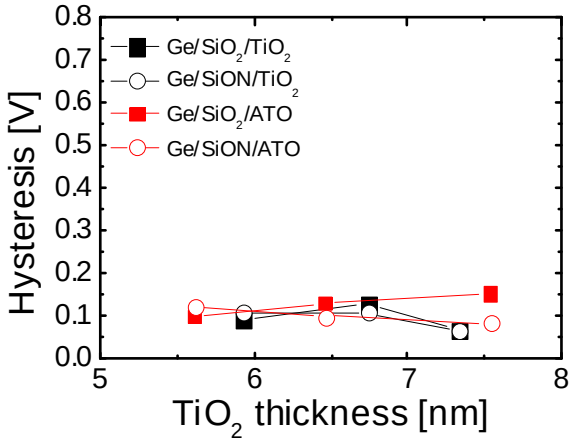

Figure 4.60 Hysteresis voltages of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge according to the TiO_2 thickness

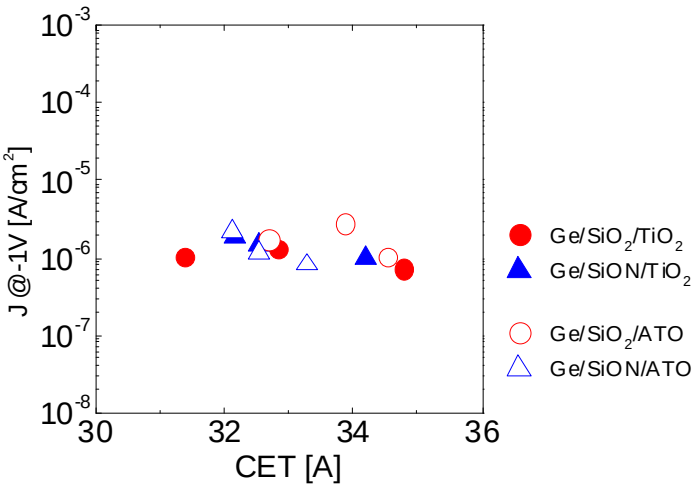

Figure 4.61 J_g at -1 V vs. CET plots of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge

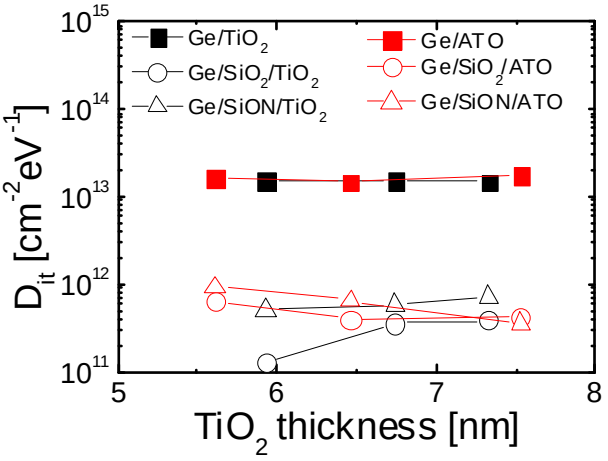

Figure 4.62 Interface trap density (D_{it}) of TiO_2 and Al-doped TiO_2 films with SiO_2, SiON passivation layer grown on Ge according to the TiO_2 thickness

For more scaling the CET, the thickness of passivation layer was reduced from 20, 15, 10, 5A. Furthermore, the thikness of TiO_2 films was also reduced as 30, 45, 75A. Interface trap density(D_{it}) of TiO_2 and Al-doped TiO_2 films with various thickness of SiO_2, SiON passivation layers grown on Ge according to the TiO_2 thickness, and D_{it} plot according to the SiO_2 thickness is shown in figure 4.63. D_{it} of Ge MOSCap with SiO_2 only was also contained in plot (~$3x10^{11}cm^{-2}eV^{-1}$). C-V curve of SiO_2 only Ge MOSCap which shows very was compared with TiO_2 in figure 4.64. D_{it} values were maintained in order of 10^{11} level until 10A of SiO_2 thickness; it is degraded in the condition of 5A of SiO_2 thickness. At least 10A of SiO_2 thickness is required for passivation the surface of Ge substrate. Dielectric constant of TiO_2 films extracted by linear plot of physical thickness and CET was plotted in figure 4.65. The CET values were extracted from TiO_2 films with SiO_2 passivation layer grown on Ge, but SiO_2 passivation layer will not affect the slope of linear fit but y-intercept. Dielectric constant of TiO_2 films was 34.4, and decreased as decline of thickness of SiO_2 passivation layer. The insulator property of J_g at -1 V vs. CET plots of TiO_2 and Al-doped TiO_2 films with with SiO_2, SiON passivation layer grown on Ge was plotted in figure 4.66. As decrease of CET, the leakage current was linearly increased. The EOT was scaled up to 14.47A in the stack of Ge/SiO_2 5A/TiO_2 30A.

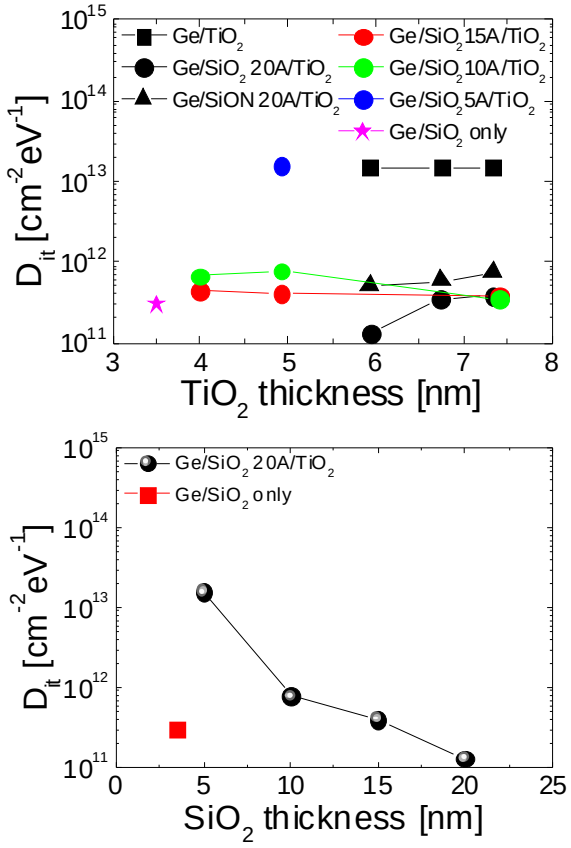

Figure 4.63 Interface trap density (D_{it}) of TiO_2 and Al-doped TiO_2 films with various thickness of SiO_2, SiON passivation layers grown on Ge according to the TiO_2 thickness, and D_{it} plot according to the SiO_2 thickness

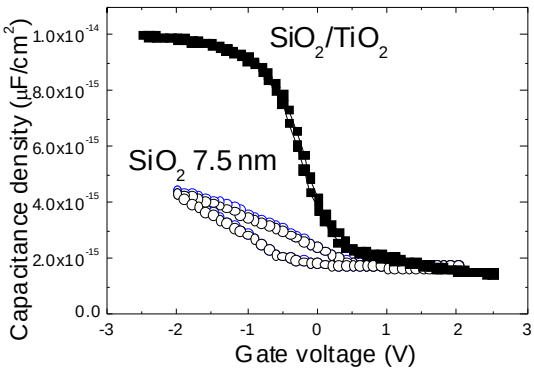

Figure 4.64 C-V curves of the SiO_2 and TiO_2 films with SiO_2 passivation layer grown on Ge

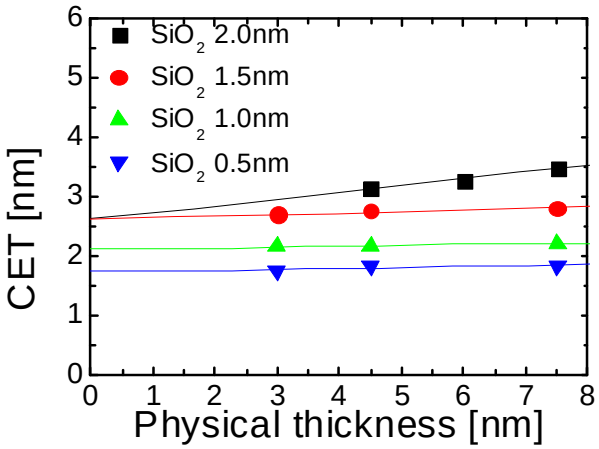

Figure 4.65 Dielectric constant of TiO_2 films extracted by linear plot of physical thickness and CET

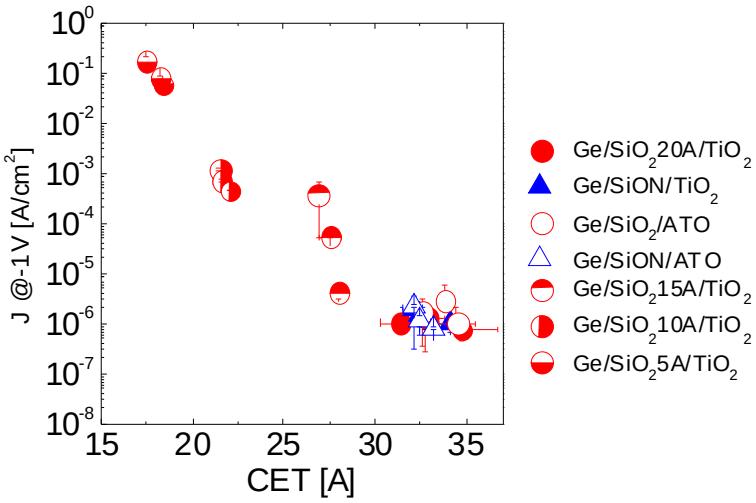

Figure 4.66 J_g at -1 V vs. CET plots of TiO_2 and Al-doped TiO_2 films with with SiO_2, SiON passivation layer grown on Ge

Next, the chemical binding states of the TiO_2, SiO_2, SiON films grown on Ge were examined via XPS, and the results are correlated with the electrical characteristics. In Figures 4.67, Ge 3d and 2p peaks are plotted. The interval of binding energy of two peaks of Ge 3d means oxidation state of Ge, BE of GeO2 is known as 3.4~3.6 eV. Peaks of SiO_2 and SiON shows intervals of 3.54, 3.60 eV which indicates formation of GeO_2 at interface. On the other hand, peak of TiO_2 shows smaller interval of 2.96 eV, it means lower oxidation state of Ge. In Ge 2p, peaks are deconvoluted by GeO_2, GeO, and bulk Ge peaks. Peaks of SiO_2 and SiON are contained more GeO_2, and TiO_2 is contained large GeO, this is same with Ge 3d peak. These analysis results means SiO_2 and SiON are effectively suppress lose the oxygen of interface to upper high-k oxide, and maintained GeO_2 relatively stable than GeO at interface. Film density by XRR was obtained as 3.6 g/cm^3 similar with 3.78 of bulk anatase TiO_2.

Table 4.9 shows Gibbs free energies in kcal/mol of the SiO_2, TiO_2, HfO_2 films under various temperatures. Gibbs free energy in larger negative value means the preferential oxidation due to reduction of total energy. Oxygen affinity is order of Hf>Ti>Si, HfO_2 is mostly tends to bring oxygen or volatile GeO from interface which results degradation of quality of high-k oxide by many defects. SiO_2 could effectively passivate the Ge surface and interface, since SiO_2 has smaller oxygen affinity than TiO_2 and HfO_2. Schematic diagram of TiO_2 films with with SiO_2 passivation layer grown on

Ge is shown in figure 4.68.

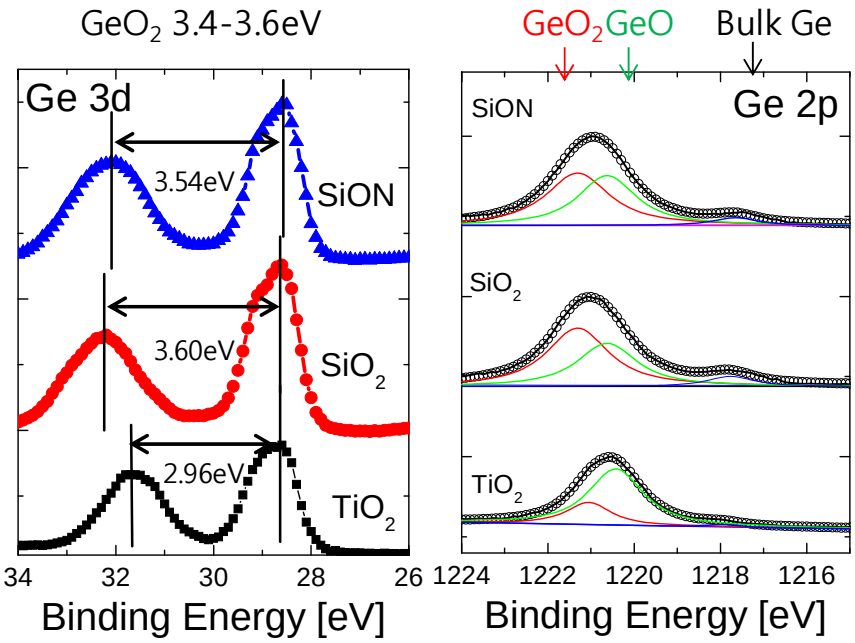

Figure 4.67 J_g at -1 V vs. CET plots of TiO_2 and Al-doped TiO_2 films with with SiO_2, SiON passivation layer grown on Ge

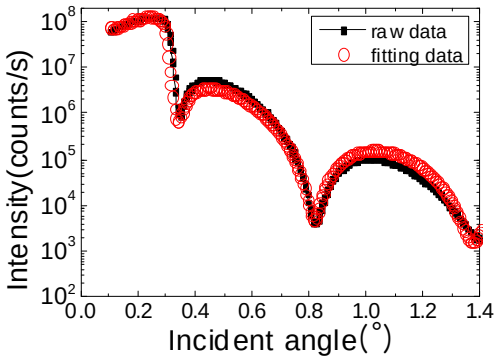

Figure 4.68 XRR analysis of TiO_2 films with SiO_2 passivation layer grown on Ge

T (K)	SiO_2	TiO_2	HfO_2
1000	−234.6	−245.7	−296.2
1100	−237.5	−248.9	−299.8
1200	−240.5	−252.3	−303.6
1300	−243.7	−255.9	−307.5

T	**SiO_2**	**GeO_2**
298	-856.3	-521.4
K	KJ/mol	KJ/mol

Table 4.9 Gibbs free energies in kcal/mol of the SiO_2, TiO_2, HfO_2, GeO_2 films under various temperatures [44,45]

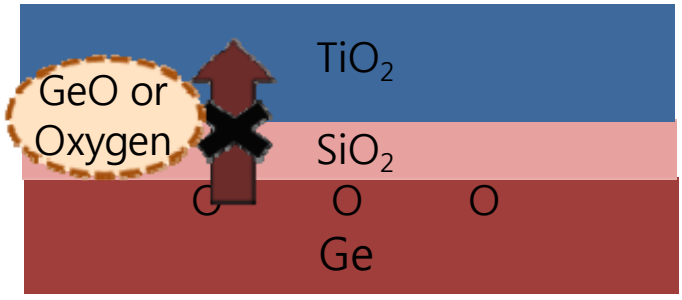

Figure 4.69 Schematic diagram of TiO_2 films with with SiO_2 passivation layer grown on Ge

4.2.5. Conclusions

The HfO_2 using O_3 and H_2O on Ge substrate has a limit to improve the electrical properties due to its strong oxygen affinity than SiO_2, GeO_2 and TiO_2 even insertion of passivation layer. In addition, it is essential to insert the passivation layer at interface which has low k value. Therefore, TiO_2 which has higher-k value is compared with HfO_2 for smaller CET is adopted with passivation layer on Ge substrate.

In conclusion, high performance gate dielectric stack composed of 0.5 – 2.0nm-thick SiO_2 passivation layer and 4.5 – 7.5nm-thick high-k TiO_2 layer were deposited on Ge substrate by ALD processes. The optimized films showed minimum EOT of ~ 1.5 nm with gate leakage current of 0.1 Acm^{-2}, when the SiO_2 thickness was 0.5 nm, while the D_{it} was as high as 2 x 10^{13} $cm^{-2}eV^{-1}$. The slight increase in the SiO_2 layer thickness to 1.0 nm drastically decreased the D_{it} to < 8 x 10^{11} $cm^{-2}eV^{-1}$, while the EOT increase was only 0.2 – 0.3 nm. This substantially decreased the leakage current by ~ two orders of magnitude. The hysteresis voltage was also maintained << 100 mV. Such a great improvement was ascribed to the low D_{it} property of the 1. 0 – 2.0nm-thick SiO_2 layer in combination with the high quality TiO_2 layer which did not bear high bulk trap density. Thicker SiO_2 layer contained high bulk defect density and interface traps as well as the low k value. Such a great performance could be fundamentally ascribed to the lower chemical activity of Ti toward the scavenge effect of GeO_2 via the SiO_2 passivation layer during the film growth process.

4.3.6. References

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5. Conclusion

HfO_2 high-k dielectric thin film was investigated to solve remained issues and improvement. To control the abnormally high V_{th}, capping layer was adopted. In addition, the effects of O_3 and H_2O as oxygen sources in ALD of HfO_2 gate dielectrics at different deposition temperatures were studied. Futhermore, the application for next generation device, it was examined on non-Si substrate such as Ge and GaAs high mobility substrates.

The bottom layers grown by ALD are more effective than top layers in modulating the V_{FB} of HfO_2 gate dielectrics. Al_2O_3 capping layers cause a V_{FB} shift in the positive direction (+0.41V), while SrO and La_2O_3 capping layers cause a negative shift as amount of -0.94, -0.37V. The insulating properties of the gate dielectric stack rely on the formation of unstable top or bottom capping layers. XPS data implies that all the top capped layers did not diffuse to the interface, which supports that bottom capped layers are effective in modulating the V_{FB}. SrO represented most large amount of V_{FB} shift, however it contained losts of amount of carbonate due to characteristic of easily carbonated Sr. The effect of capping layer on leakage current density observed according to degree of reaction between capping layer and substrate or own band gap. However, the reaction or intermixing at interface did not affect the roughness of high-k dielectrics due to too thin thickness. The origin of V_{FB} shift could be explained by dipole theory, it is well mated with electrical property of amount and direction of V_{FB} shift and calculated

dipole moment from oxygen areal density and molar volume. In addition, the calculated dipole moment from electro negativity and bonding length is also well correlated with experimental result of V_{FB} shift.

The effects of O_3 and H_2O as oxygen sources on the ALD of HfO_2 films grown at substrate temperatures of 160-360^oC were examined in terms of their growth characteristics and structural evolution upon the thickness increase and post-deposition annealing. While the ALD process that involved H_2O was achieved well at a temperature as low as 160^oC, the ALD in which O_3 was used required substrate temperatures of 240-280^oC to induce a fluent ALD reaction. This could be ascribed to the proton-induced ligand exchange reaction in the case of the ALD with H_2O, whereas the O-radical mediated ALD reaction appeared to require supply of thermal energy to overcome its rather high activation energy. According to these different ALD mechanisms, the HfO_2 films grown at 200^oC and 280^oC for the ALD that involved H_2O and O_3, respectively, showed the highest density. The HfO_2 films with a low density or (and) a high carbon-impurity concentration crystallized to the tetragonal phase after the PDA at 600^oC, whereas the thin film with both a low density and high carbon impurity retained the highest portion of the tetragonal phase (~30%) even after the PDA at 1000^oC. While the majority phase of the crystalline materials was monoclinic phase by the increasing thickness or PDA temperature, all the HfO_2 films contained a non-negligible concentration of the tetragonal phase, which was found from

the extensive and detailed HRTEM study. This could be related to the presence of the film surface with a lower energy for the phases other than the monoclinic phase. The density of the thin as-deposited films (< 8 nm) was important in the determination of the bulk dielectric constant, and the bulk dielectric constants of the thicker films (8-18 nm) were contributed by the (partial) crystalline phase and the density. The best electrical performance was achieved in the HfO_2 film grown at 200°C with H_2O due to the minimum-involvement of the interfacial oxide layer and the high bulk density of the film.

HfO_2 films using O_3 and H_2O oxygen source at different deposition temperature applied to high-mobility substrates Ge and GaAs. HfO_2 deposited on Ge using H_2O oxygen source shows distorted C-V curve due to severe leakage current. Thicker HfO_2 film ~14nm was required for normal C-V property. SiON passivation layer reduced hysteresis voltage, but hump was shown in C-V curve. AlON passivation layer remained certain hysteresis voltage, but normal C-V curve was observed even after PDA. RTO at 600°C is largely increased hysteresis voltage of HfO_2-O_3 without the decrease of maximum capacitance. HfO_2-H_2O showed distorted C-V curves, it was cured after RTO at 600°C. Sulfur passivation using H_2S gas annealing was not effective to reduce hysteresis.

There was no improvement of HfO_2 deposited on GaAs using H_2O oxygen source or low deposition temperature than that of O_3 or high

deposition temperature. 1~10 ALD cycles of Al_2O_3 inserted, hysteresis and frequency dispersion were decreased from 814 to 465mV, from 76.3 to 56.2%. Among O_3, H_2O, O_2 plasma, N_2/H_2 plasma, NH_3 annealing, some treatments induced slightly reduction of hysteresis voltage and frequency dispersion. However, the D_{it} value did not improve. The p-type GaAs represents better frequency dispersion with smaller hysteresis. It is required to improve in HfO_2/n-GaAs structure.

H_2O could reduce the formation of sub-oxide at interface between HfO_2 and substrate. However, H_2O has weaker oxization power than O_3, impurities such as carbon is residued in deposited film which can be defects. HfO_2 in condition of 200^oC O_3 reduced the hyeteresis voltage in case of Ge substrate, but it was not observed on GaAs substrate. SiO_2 passivation layer almost reduced the hysteresis voltage, but hump in C-V curve remained. Al_2O_3 passivation layer reduced to a certain hysteresis voltage and improved the leakage current due to passivation of reaction or intermixing at interface between HfO_2 and substrate.

The HfO_2 using O_3 and H_2O on Ge substrate has a limit to improve the electrical properties due to its strong oxygen affinity than SiO_2, GeO_2 and TiO_2 even insertion of passivation layer. In addition, it is essential to insert the passivation layer at interface which has low k value. Therefore, TiO_2 which has higher-k value is compared with HfO_2 for smaller CET is adopted with passivation layer on Ge substrate.

In conclusion, high performance gate dielectric stack composed of 0.5 – 2.0nm-thick SiO_2 passivation layer and 4.5 – 7.5nm-thick high-k TiO_2 layer were deposited on Ge substrate by ALD processes. The optimized films showed minimum EOT of ~ 1.5 nm with gate leakage current of 0.1 Acm^{-2}, when the SiO_2 thickness was 0.5 nm, while the D_{it} was as high as 2 x 10^{13} $cm^{-2}eV^{-1}$. The slight increase in the SiO_2 layer thickness to 1.0 nm drastically decreased the D_{it} to < 8 x 10^{11} $cm^{-2}eV^{-1}$, while the EOT increase was only 0.2 – 0.3 nm. This substantially decreased the leakage current by ~ two orders of magnitude. The hysteresis voltage was also maintained << 100 mV. Such a great improvement was ascribed to the low D_{it} property of the 1. 0 – 2.0nm-thick SiO_2 layer in combination with the high quality TiO_2 layer which did not bear high bulk trap density. Thicker SiO_2 layer contained high bulk defect density and interface traps as well as the low k value. Such a great performance could be fundamentally ascribed to the lower chemical activity of Ti toward the scavenge effect of GeO_2 via the SiO_2 passivation layer during the film growth process.

Curriculum Vitae

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I. Educations

1999. 3. - 2004. 2.	B.S.
	Chemistry
	Ajou University, Suwon, Korea
2006. 3. – 2008. 2.	M.S. Course
	Department of Materials Science and Engineering
	Seoul National University, Seoul, Korea
2008.9. – 2014.8.	Ph.D. Course
	Department of Materials Science and Engineering
	Seoul National University, Seoul, Korea

II. Research Areas

1. Atomic Layer Deposition (ALD)

- Atomic layer deposition of high-k dielectric materials
- Atomic layer deposition of multi-component materials
- Control of non-ideal growth with substrate effect
- Growth mechanism with various precursors

2. Complementary metal oxide semiconductor (CMOS) devices

- Dielectric materials (HfO_2, ZrO_2, HZO, Hf-silicate, Al_2O_3, and SiO_2) for gate oxide
- Electrode materials (Ru, TiN, Pt) for gate metal

III. Experimental Skills

1. Deposition methods

- ALD for deposition of dielectric materials (HfO_2, ZrO_2, Al_2O_3, SiO_2, TiO_2)
- ALD and CVD for growth of electrode materials (Ru, RuO_2)
- DC magnetron sputtering and e-beam evaporation of electrodes (Ru, RuO_2, Pt)

2. Annealing methods

- Rapid thermal process and conventional furnace for ambient and vacuum annealing

3. Analysis methods

- X-Ray Fluorescence Analyzer (XRF, Thermo scientific, ART Quant'X EDXRF) for analysis of composition and layer density of film
- Field Emission Scanning Electron Microscopy (FE-SEM, Hitachi, S-4800)

for characterizing thin films

- X-ray Diffractometer (PANalytical, X'Pert PRO MPD) for measurement of X-ray diffraction and X-ray reflection
- Atomic Force Microscopy (AFM, JEOL, JSPM-5200) for analysis of the topography
- Spectroscopic Ellipsometer (SE, J.A. Woollam, M-2000) for analysis of optical properties and thicknesses of thin films
- Four point probe for resistivity measurement of metals and conducting materials
- Pulse/pattern generator (Agilent, 81110A/81111A) and digital oscilloscope for pulse switching measurement of resistive switching materials
- HP4194A, 4284A for C-V and impedance measurement of capacitors
- HP4140B and HP4145B, 4155A for I-V measurement of capacitors and transistors
- Charactorizing thin films by XPS, AES, TEM, SIMS, MEIS

IV. Academic Honors

1. 2007. 2. 15. "Samsung Electronics Humantech Gold Award", Samsung Electronics
2. 2007.4.6 The 4th International Workshop on Nanoscale Semiconductor Devices "Best Poster Award", Inter-University Semiconductor Research Center, Seoul National University

List of publications

1. Refereed Journal Articles (SCI)

1.1 Domestic

1.2. International

1. Seong Keun Kim, **Sang Young Lee**, Sang Woon Lee, Gyu Weon Hwang, and Cheol Seong Hwang, “Atomic layer deposition of Ru thin films using 2,4-(dimethylpentadienyl)(ethylcyclopentadienyl)Ru by liquid injection system”, J. Electrochem. Soc., 154 (2) D95 (2007)
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8. Tae Joo Park, Jeong Hwan Kim, Jae Hyuck Jang, Joohwi Lee, Sang Woon Lee, **Sang Young Lee**, Hyung Suk Jung, and Cheol Seong Hwang, "Effects of Annealing Environment on Interfacial Reactions and Electrical Properties of Ultrathin SrTiO3 on Si", J. Electrochem. Soc. 156 (9), G129-G133 (2009)
9. Gyu-Jin Choi, Seong Keun Kim, **Sang Young Lee**, Woo Young Park, Minha Seo, Byung Joon Choi, and Cheol Seong Hwang, "Atomic Layer Deposition of TiO2 Films on Ru Buffered TiN Electrode for Capacitor Applications" Journal of The Electrochemical Society, 156 (7) G71-G77 (2009)
10. Kyung Min Kim, **Sang Young Lee**, Gyu Jin Choi, Jeong Hwan Han and Cheol Seong Hwang, "Electrically Benign Dry-Etching Method for Rutile TiO2 Thin-Film Capacitors with Ru Electrodes", Electochem. Solid-State Lett. 13(1), G1-G4 (2010)
11. Hyung-Suk Jung, Jeong Hwan Kim, Joohwi Lee, **Sang Young Lee**, Un Ki Kim, Cheol Seong Hwang, Jung-Min Park, Weon-Hong Kim, Min-Woo Song, and Nae-In Lee," Bias temperature instability characteristics of n- and p-type field effect transistors using HfO2 gate dielectrics and metal gate", J. Electrochem. Soc. 157, 3, pp. H355-H360 (2010)
12. Hyung-Suk Jung, Hyo Kyeom Kim, Jeong Hwan Kim, Seok-Jun Won, Deok-Yong Cho, Joohwi Lee, **Sang Young Lee**, Cheol Seong Hwang, Jung-Min Park, Weon-Hong Kim, Min-Woo Song, Nae-In Lee, and Sung Heo,"Electrical and Bias Temperature Instability Characteristics of n-Type Field-Effect Transistors Using HfOxNy Gate Dielectrics" J. Electrochem. Soc., Volume 157, Issue 5, pp. G121-G126 (2010)

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28. Jeong Hwan Kim, Tae Joo Park, Seong Keun Kim, Deok-Yong Cho, Hyung-Suk Jung, **Sang Young Lee**, Cheol Seong Hwang, "Chemical structures and electrical properties of atomic layer deposited HfO2 thin films grown at an extremely low temperature(≤100◦C) using O3 as an oxygen source", Appl. Surf. Sci., 292, 852-856, (2014)
29. **Sang Young Lee**, Hyo Kyeom Kim, Jong Ho Lee, Il-Hyuk Yu, Jae-Ho Lee, and Cheol Seong Hwang, "Effects of O3 and H2O as oxygen sources on the atomic layer deposition of HfO2 gate dielectrics at different deposition temperatures", J. Mater. Chem. C, 2, 2558-2568 (2014)

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2. Hyun Ju Lee, Seong Keun Kim, **Sang Young Lee**, Keun Lee, and Cheol Seong Hwang, "Influence of Al_2O_3 Hydrogen Barrier on the Ferroelectric Switching Behavior of $Pb(Zr,Ti)O_3$ Thin Film Capacitor", The 14th Korean Conference on Semiconductors, Lotte Hotel Jeju, Feb. 8-9, 2007
3. Hyun Ju Lee, Keun Lee, Gun Hwan Kim, **Sang Young Lee**, Seong Keun Kim and Cheol Seong Hwang, "Influence of Al_2O_3 Hydrogen Barrier on the Ferroelectric Switching Behavior of $Pb(Zr, Ti)O_3$ Thin Film Capacitor", poster, 제3회 강유전체 연합 심포지움, 티롤호텔 무주, Feb. 12~13, 2007
4. Jaeyeong Heo, **Sang Young Lee**, Dail Eom, Sanghyun Park, Cheol Seong Hwang, and Hyeong Joon Kim, "The enhanced nucleation behavior of atomic-layer-deposited Ru film on porous low-*k* dielectrics by UV-O_3 treatment," 2007 한국결정학회 추계학술발표회, 2007. 11. 16, 한국산업대학교 혜성관 시청각실
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3. Proceeding

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4. Project

1. 서울시 산학연 협력사업/삼성전기: “박막형 적층세라믹 축전기 (Multi-Layer Ceramic Capacitor, MLCC) 제작을 위한 원자층 증착법을 이용한 유전체 및 전극 박막 공정 및 소자 제조 기술 개발” 2006.1~2008.3
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Abstract (in Korean)

SiO_2를 이용하는 실리콘 시대의 CMOSFET 소자의 스케일링은이미 끝났다. HfO_2 고유전율 게이트 산화막을 이용한 차세대 CMOSFET은 이미 양산에 응용되기 시작했다. 극단적으로 작은 평면 혹은 삼차원 구조의 소자에서 원자층 증착 방법은 게이트 산화막을 형성하는 방법으로 많은 장점을 가지고 있는데, 자기 제어 성장 거동 때문에 낮은 누설전류와 함께 높은 유전율, 그리고 원자층 단계의 정확한 두께 제어가 가능하다. 하지만 전하 트랩, 불충분한 신뢰성, Fermi level pinning 현상에 의한 비정상적으로 높은 문턱전압 등의 해결해야될 문제점이 있어 더 많은 연구가 필요하며, 더욱 스케일된 MISFET (등가산화막두께 < ~0.5 nm)에 적용하기 위해 더욱 큰 유전율(k > 30)을 갖는 Hf를 기반으로 한 유전막을 개발하는 것이 필요하다. 게다가 원자층 증착법으로 형성한 HfO_2 박막이 n-type에 III-V 혹은 II-V 화합물 반도체, p-type에 Ge 등 고이동도 채널 물질에 적용되기 위해서는 기판과의 불안정한 계면 특성, 원자층 증착 조건에 의해 크게 영향을 받는 등 더욱 큰 문제점들이 있다. 몇몇 다른 종류의 고유전율 박막이 고이동도 기판에 적용되었지만, 여전히 HfO_2는 기존에 양산에 도입되었기 때문에 공정 설비 및 상태, 오염도 조절 등이 이미 성숙되어 적용하기 쉬운 장점이 있다.

Hf 기반의 게이트 산화막의 비정상적으로 높은 문턱전압을 조절하기 위해서 희토류 금속 산화물층이나 Al_2O_3를 적층하는 방법이 큰 관심을 받고 있다. 적층막은 얇고 균일하게 형성되어야 넓은 웨이퍼 전체에서 등가산화막 두께의 증가 없이 문턱전압을 잘 조절할 수 있다. 그래서 뛰어난 두께 제어성 및 균일성, 플라즈마 손상이 없는 원자층 증착법을 이용한 적층막이 문턱전압을 조절하기 위한 접근으로 각광받고 있다.

MIS 커패시터에서 원자층 증착법으로 성장한 Al_2O_3, SrO, 그리고

La_2O_3 적층막이 HfO_2 게이트 산화막의 플랫밴드 전압에 미치는 영향에 대해 이 논문에서 연구하였다. Al_2O_3 적층막은 양의 전압 방향으로, 반면에 SrO, La_2O_3 적층막은 음의 전압 방향으로 플랫밴드 전압을 이동시켰다. HfO_2 게이트 산화막의 아래와 Si 기판 사이에 적층막을 삽입한 경우가 플랜밴드 전압을 조절하는데 HfO_2 게이트 산화막의 위에 삽입한 경우보다 더 효과적이었다. 이러한 게이트 구조의 산화막 특성이 평가되었다. X-ray photoelectron spectroscopy 분석을 통해 고온 열처리 후에도 HfO_2 위에 있는 적층막이 계면으로 확산되지 않기 때문에 HfO_2 밑에 적층막을 삽입하는 것이 효과적임을 확인하였다.

다음으로, 이러한 HfO_2 고유전막을 고이동도 기판에 적용하기 위해서 TEMAH 전구체와 오존과 물 산소공급원이 성장거동, 물리적 전기적 특성, 미세구조에 미치는 영향을 알아보았다. 원자층 증착 온도 범위는 각각 오존은 160-320^oC, 물은 160-280^oC이며, 오존을 이용한 경우 물보다 더 높은 온도범위에서 원자층 증착 범위를 가짐을 알 수 있었다. 오존을 이용해 증착한 HfO_2는 증착온도가 감소함에 따라 박막 밀도가 감소한 반면, 물을 이용해 증착한 HfO_2는 박막 밀도가 증가하였다. 증착온도가 감소함에 따라, 오존을 이용한 박막은 불충분한 반응으로 인해 불순물의 함량이 크게 증가했으며, 이는 600도 열처리 후에 tetragonal 구조로 결정화됨을 유도하였다. 높은 탄소 불순물 함량과 낮은 박막밀도를 갖는 HfO_2 박막은 1000도의 고온 열처리 후에도 tetratonal 구조의 함량이 30% 정도로 여전히 높게 나타났다. 하지만 저온(200^oC)에서 물을 이용해 증착한 HfO_2 박막이 가장 높은 박막 밀도와 낮은 불순물 함량, 낮은 유전율을 가지는 계면을 적게 형성하여 가장 우수한 전기적 특성을 나타내었다.

오존과 물을 산소공급원으로 이용하여 여러 증착온도에서 성장한 HfO_2 박막을 Ge 고이동도 기판에 적용하였다. 물 산화제를 이용할 경우 계면과의 반응을 줄여줄 수 있을 것으로 기대하였으나,

오존보다 낮은 산화력으로 인해 박막내에 불순물이 조금 더 남을 수 있으며 그것이 결함으로 작용할 수 있다. SiO_2, Al_2O_3 패시베이션 막을 도입하면 누설전류를 줄여주며, 기판과 HfO_2 박막의 반응이나 섞임을 방지해주는 효과를 얻을 수 있다.

하지만 고이동도 기판에서 HfO_2 고유전율 박막으로 특성을 개선하는데는 한계가 있었으며, 낮은 유전율을 갖는 패시베이션 막을 계면에 반드시 사용하여야 했다. 그래서 작은 밴드갭을 갖지만 좀 더 높은 유전율을 갖는 TiO_2 고유전율 박막을 도입하였다. SiO_2, SiON 패시베이션 막이 히스테리시스 전압과 진동수 분산, 계면 트랩 밀도를 효과적으로 줄여주었다. 더 등가산화막 두께를 줄이기 위해서 SiO_2 패시베이션 막의 두께를 2nm에서 0.5nm까지 줄여보며 TiO_2 고유전율 박막에 적용했을 때, 계면 트랩 밀도가 SiO_2 패시베이션 막의 두께가 1nm일 때도 11승 정도의 값을 유지하였으며, SiO_2의 두께가 0.5nm일 때는 열화되었다. 즉 적어도 1nm 두께의 SiO_2 패시베이션 막은 Ge 기판의 표면을 패시베이션 하기 위해서 반드시 필요하였다. 등가산화막 두께 1.4 nm에서 계면 트랩 밀도를 $1.3x10^{11}cm^{-2}eV^{-1}$ 까지 줄일 수 있었다.