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공학박사 학위논문

LASER-INDUCED EPITAXIAL GROWTH FOR 3D-ICs & 3D-MEMORY DEVICES

3차원 집적회로 및 3차원 메모리 소자를 위한 LASER-INDUCED
EPITAXIAL GROWTH에 관한 연구

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손 용 훈

LASER-INDUCED EPITAXIAL GROWTH FOR 3D-ICs & 3D-MEMORY DEVICES

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Laser-induced epitaxial growth (Laser-induced Epitaxial Growth) process has been developed to obtain single crystalline silicon on insulator using a seed which is formed by selective epitaxial growth process. It was found that the lateral epitaxial growth of molten silicon occurs when the energy density of the laser beam is high enough to completely melt the deposited amorphous silicon on seeds and that on oxide films. The location and size of such single crystalline grain were precisely controlled due to the pre-patterned epitaxial seeds. Furthermore the problem caused by the edge area of the laser beam was thoroughly analyzed, and solutions to the problem were reasonably suggested. Consequently this proposed laser-induced epitaxial growth process enables the realization of location-controlled perfect single crystalline silicon layer on oxide films for monolithic three-dimensional integration.

Novel isolation technology by using LEG process has been introduced to obtain monolithically stacked active silicon without any thermal budget. With the LEG process, the epitaxial behavior is completely understood by solidification modeling. It is shown

that the characteristics of cell transistors with LEG-active silicon are the same as those with bulk-active Si, in terms of both performance and distribution using high density 512Mb DRAM devices. Thus LEG process is believed to be a promising device isolation technology for monolithic multi-stack device.

As a versatile processing method for nanoscale memory integration, laser-induced epitaxial growth is proposed for the fabrication of vertical Si channel (VSC) transistor. The fabricated VSC transistor with 80nm gate length and 130nm pillar diameter exhibited field effect mobility of $300\text{cm}^2/\text{Vs}$, which guarantees “device quality”. In addition, we have shown that this VSC transistor provides memory operations with a memory window of 700mV, and moreover, the memory window further increases by employing charge trap dielectrics in our VSC transistor. Our proposed processing method and device structure would provide a promising route for the further scaling of state-of-the-art memory technology.

KEYWORDS:

3D-IC (Integrated chip), 3D-Memory, Laser-induced epitaxial growth, Solidification, Vertical NAND

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Chapter 1

Laser Induced Epitaxial Growth for Stacked SRAMs

1.1 INTRODUCTION

Three-dimensional stacked memory has attracted much attention due to its advantages such as high-speed operation, low-power consumption and high-level integration. Many researchers have reported various novel approaches to achieve three dimensional device integration, including wafer bonding, epitaxial lateral overgrowth (ELO), zone melting recrystallization and lateral-solid phase epitaxy[1-3]. These methods are improper for low temperature processing, which is crucial for preventing the performance degradation of underlying transistors in three-dimensionally stacked devices. ELO using vapor phase epitaxy (VPE) in a chemical vapor deposition (CVD) reactor has considerable crystalline defects such as stacking faults and micro-twin due to the difference of thermal expansion coefficient between oxide and silicon layer. 3 On the other hand, Fabrication of a perfect single crystal on an oxide using continuous lasers or heated graphite strips is possible, whose quality is comparable to bonded silicon-on-oxide wafers [4]. However, this is not a proper stack technology; because the junction area of the underlying devices will be degraded by the high temperature

substrate heating during the process. Although solid phase epitaxy (SPE) can be easily acquired by using a simple furnace, Si films crystallized with long annealing times (> 6 hr) at low temperatures ($\sim 600^\circ\text{C}$) contain defects such as stacking faults and microtwins which may result in limited success of stacked devices by sub-threshold leakage, decreased on/off ratio and broaden current distribution [1].

1.2 Background of laser crystallization

In this work, we suggest a laser-induced epitaxial growth (LEG) process that utilizes a single crystalline seed grown by conventional selective epitaxial growth (SEG) process. This seed layer was formed in patterned contact holes linking the substrate silicon and the stacked layer. A raised seed could prevent the degradation of electrical properties of underlying devices. An excimer laser was then used as a light source for the epitaxial growth via recrystallization to melt the deposited amorphous silicon films both on oxide layer and seed contact within several hundred nano-seconds. In the case of conventional excimer laser crystallization, the microstructure of crystallized silicon depends on the energy density of incident laser beam and the thickness of amorphous silicon films. The melting phenomena by an excimer laser irradiation can be categorized as ‘partial melting’, ‘near-complete melting’, and ‘complete melting’ regime. In the near-complete melting regime, there are unmelted solid phase islands after the completion of melting, from which super lateral growth (SLG) can occur before impinging on adjacent grains and result in relatively large grains [6]. This LEG process is based upon a controlled SLG (c-SLG) phenomenon, in terms of the lateral growth from seed [7]. In this paper, the experimental results will be

given and the mechanism of the LEG process will be discussed based on microstructural analysis.

1.3 Results

Figure 1.1 shows a process sequence for LEG process where the underlying structure has 300 nm thick oxide layer on (100) silicon substrate with contact hole patterns by lithography process. The contact hole filling with single crystal silicon is made by the conventional SEG process, which acts as the seed for lateral epitaxy, and then followed by 50 nm amorphous silicon deposition process by a low pressure CVD reactor. And LEG process is carried out to change deposited amorphous silicon films into single crystalline silicon films using a XeCl excimer laser with the pulse duration of 23 nano-seconds and the wavelength of 308 nm.

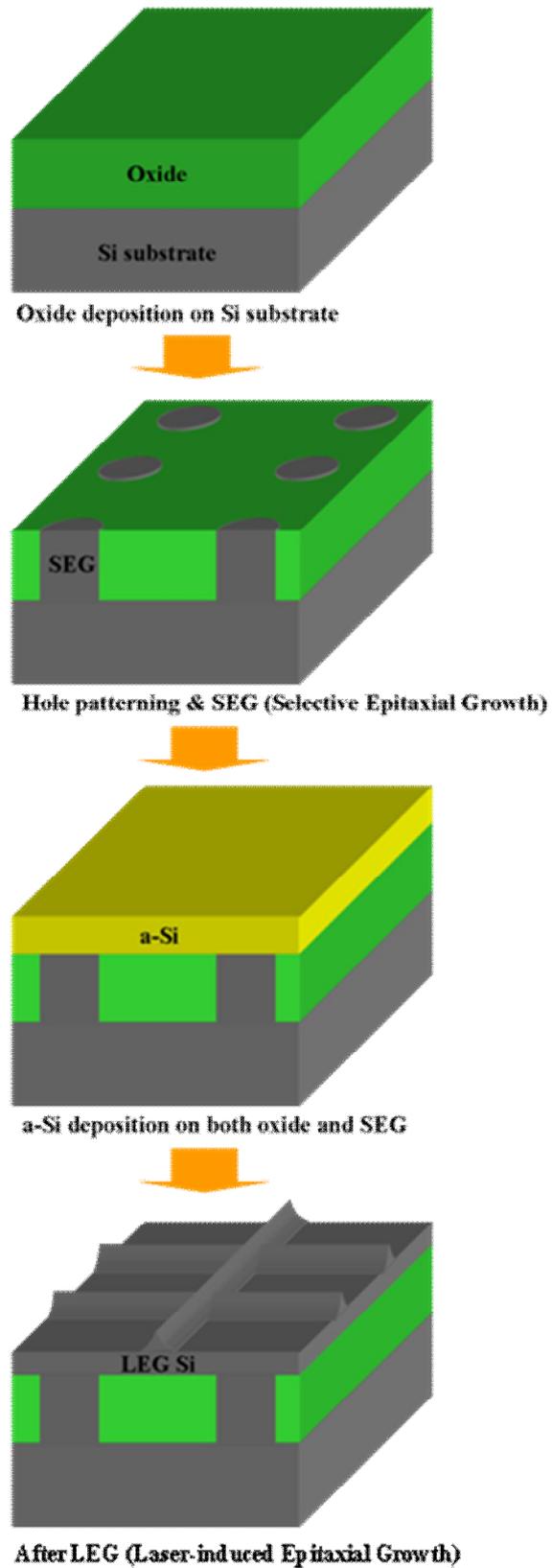


Figure 1.1. Key process sequence

As shown in Fig. 1.2, the latent heat of molten silicon may flow out through the contact hole filled with single crystal because silicon has a higher thermal conductivity than oxide. Therefore, the molten silicon is solidified from the top of the contact hole which acts as a seed for the epitaxial vertical and lateral growth, similar to the SLG phenomena.

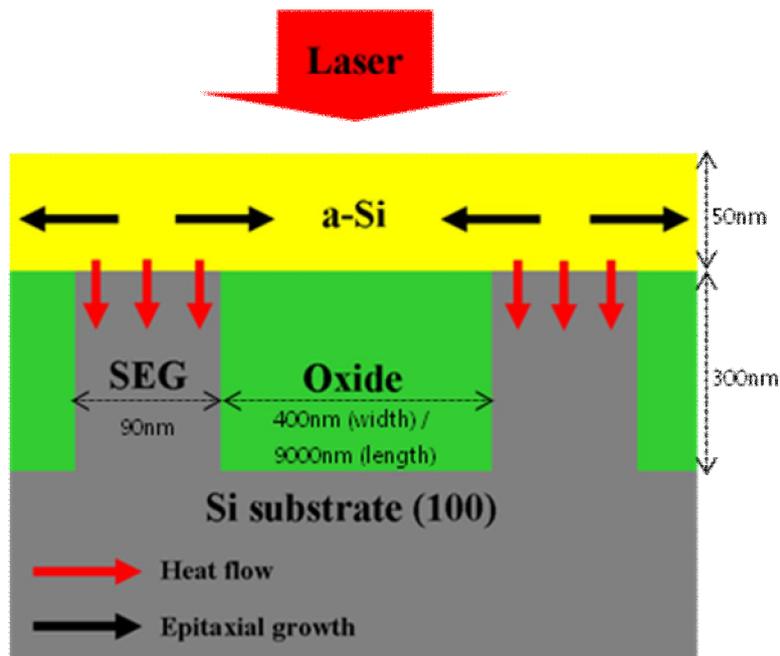


Figure 1.2. Schematic diagram of LEG process.

Figure 1.3 shows the planar transmission electron microscopy (TEM) images of the crystallized silicon films as a function of the incident laser energy density. There is a significant phase change from polycrystalline to location-controlled single crystalline phase with the increase of energy density. In the low energy density regime of 300 mJ/cm² as shown in Fig. 1.3 (a), the extremely small poly grains on SEG seed are

detected and then the laterally grown grains on the oxide are connected with such small poly grains on the SEG contact. These microstructures indicate that the energy density of incident laser beams is just above the complete melting threshold (CMT), as known in the case of non-seeded specimen, resulting in the nucleation on SEG seed and subsequently lateral grain growth from such nucleated solid. Though the energy density of 300 mJ/cm² is high enough to melt the deposited amorphous silicon films completely, amorphous silicon on SEG seed is not melted completely, leading to partial melting regime, since SEG seed plays a role as heat sink. Therefore, small poly grains corresponding to partial melting regime generate on SEG seed and subsequently the melt on oxide films is solidified from the nucleated small poly grains on the seed.

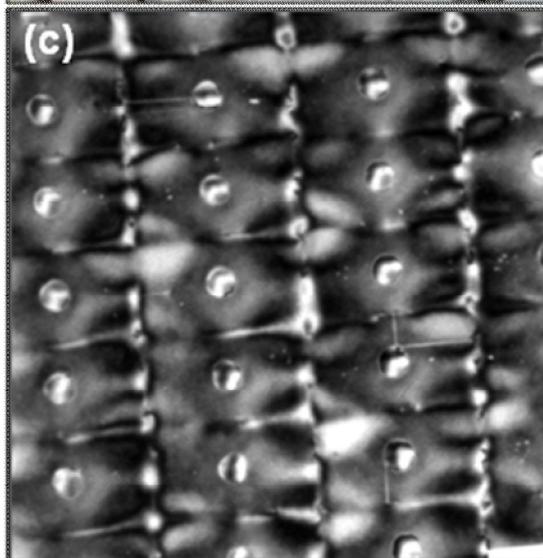
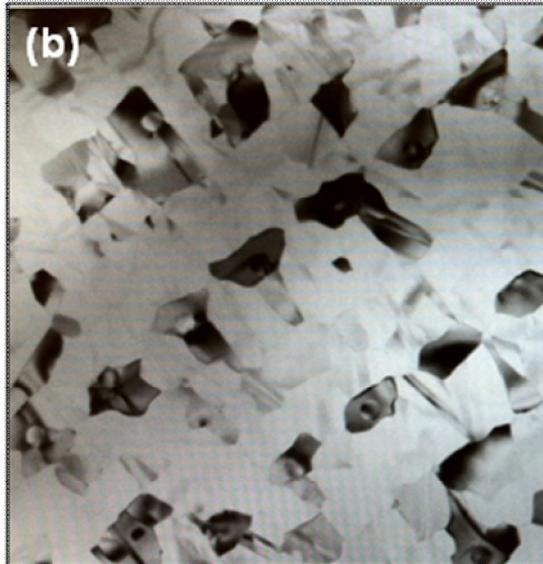
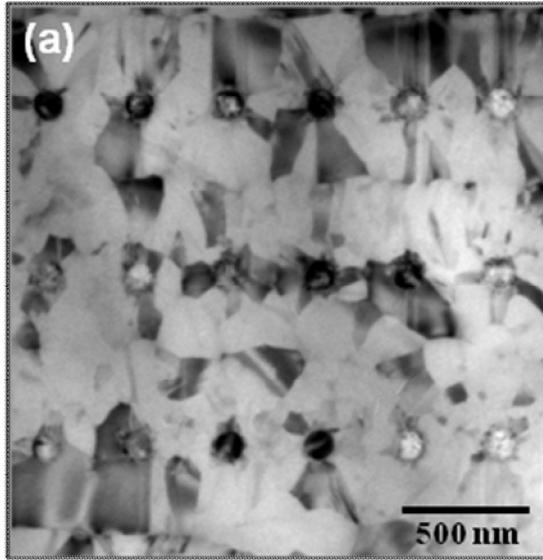


Figure 1.3. Planar transmission electron microscopy images of the crystallized silicon films as a function of the incident energy density. (a) 300 mJ/cm², (b) 370 mJ/cm², and (c) 400 mJ/cm².

In the medium energy density regime of 370 mJ/cm², 1.16 CMT, it is shown that an almost single crystal is vertically grown on SEG seed and continues the lateral epitaxial growth on the oxide, which indicates amorphous silicon on seed is completely melted by incident laser beam. However, the breakdown of perfect epitaxial growth from SEG seed occurs, and also the microstructure corresponding to defective growth is observed: the lateral epitaxy growth proceeds with the formation of twins extending into the transition of crystalline plane. Furthermore, the length of lateral growth is extremely short, comparing of that via c-SLG (a few micrometer) on the glass substrate. We speculate that it is caused by the deep undercooling of molten silicon since the silicon as a substrate, which has a higher thermal conduction than glass substrate, triggers the rapid quenching of molten silicon.⁸⁻⁹ Finally, in the optimum energy density regime of 400 mJ/cm², 1.25 CMT, the vertical and lateral epitaxy from SEG occur in all directions without any damages such as agglomeration and ablation on wafer, as shown in Fig. 1.3(c). It is noted that, in these sample configurations, the required energy density of the incident beams should be more than 1.2 times of CMT in order to acquire LEG microstructure.

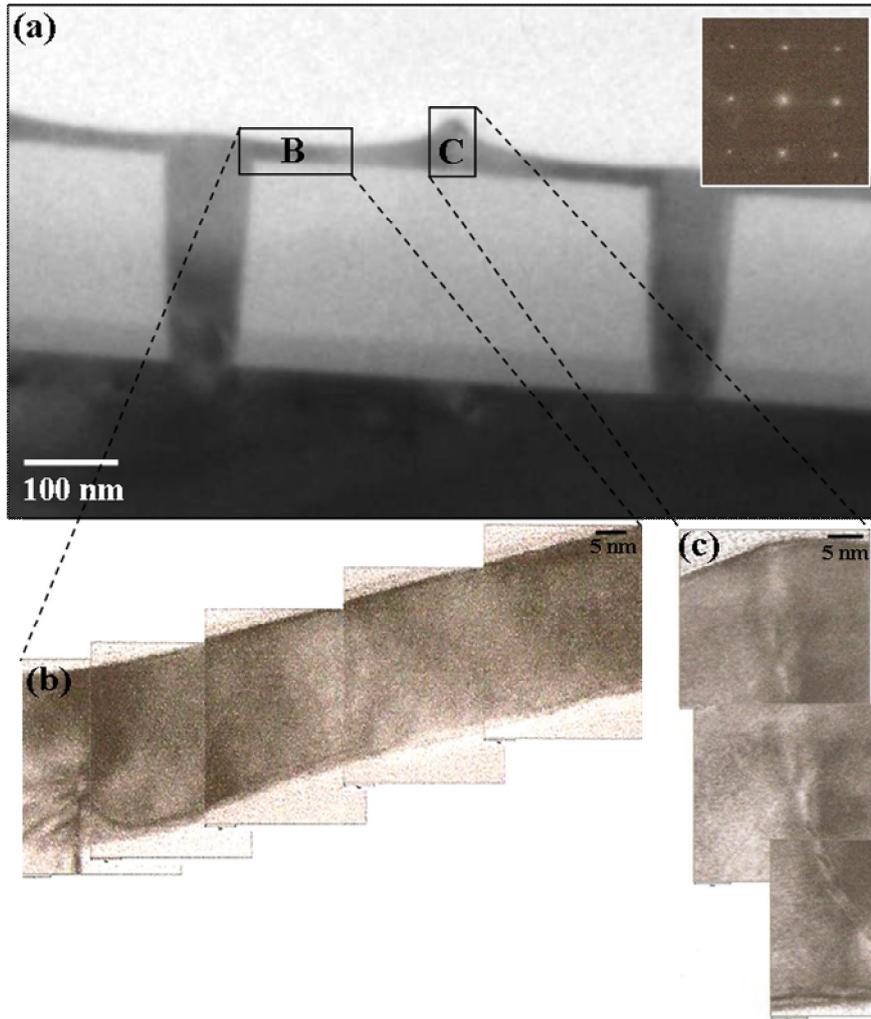


Figure 1.4. (a) Cross section TEM image of LEG Si with the energy density of 400 mJ/cm², (b) magnified view of LEG Si of region B showing perfect crystallinity of lateral epitaxy, and (c) magnified view of region C showing crystalline defect occurring at impingement with neighboring crystals.

Fig. 1.4 shows cross-section TEM image of a crystallized sample by excimer laser irradiation with the energy density of 400 mJ/cm². It reveals that single crystal silicon on oxide is formed by lateral epitaxial growth from each SEG contact. As shown in the inset of Fig. 1.4(a), the crystallographic orientation of LEG silicon films is identical to

(100) of bulk silicon. The lateral epitaxial films are found to be defect-free single crystalline and indistinguishable from the contact SEG layer [see Fig. 1.4 (b)]. There exists, however, a low-angle grain boundary at the center of crystallized silicon films between the SEG contacts, as shown in Fig. 2.4(c). This implies that lateral growth from the seed collides at midpoint with neighbor growth fronts and thereby single crystalline epitaxial growth can proceed until the impingement of the neighboring crystallites. The thickness variation of the crystallized silicon films is believed to be due to the volume change by the density difference between the liquid and solid silicon during the lateral solidification, and these protrusions can be flattened by an optimized CMP process.¹⁰ Although there are crystalline defects at the center of the stacked layer, we can easily align the channel area of transistors on perfect single crystal using conventional lithography, since the location of protrusion precisely depends on that of seed contact. To sum up, both the critical energy density of the laser beam beyond complete melting and the existence of SEG seed are found to be key factors for a perfect phase transformation.

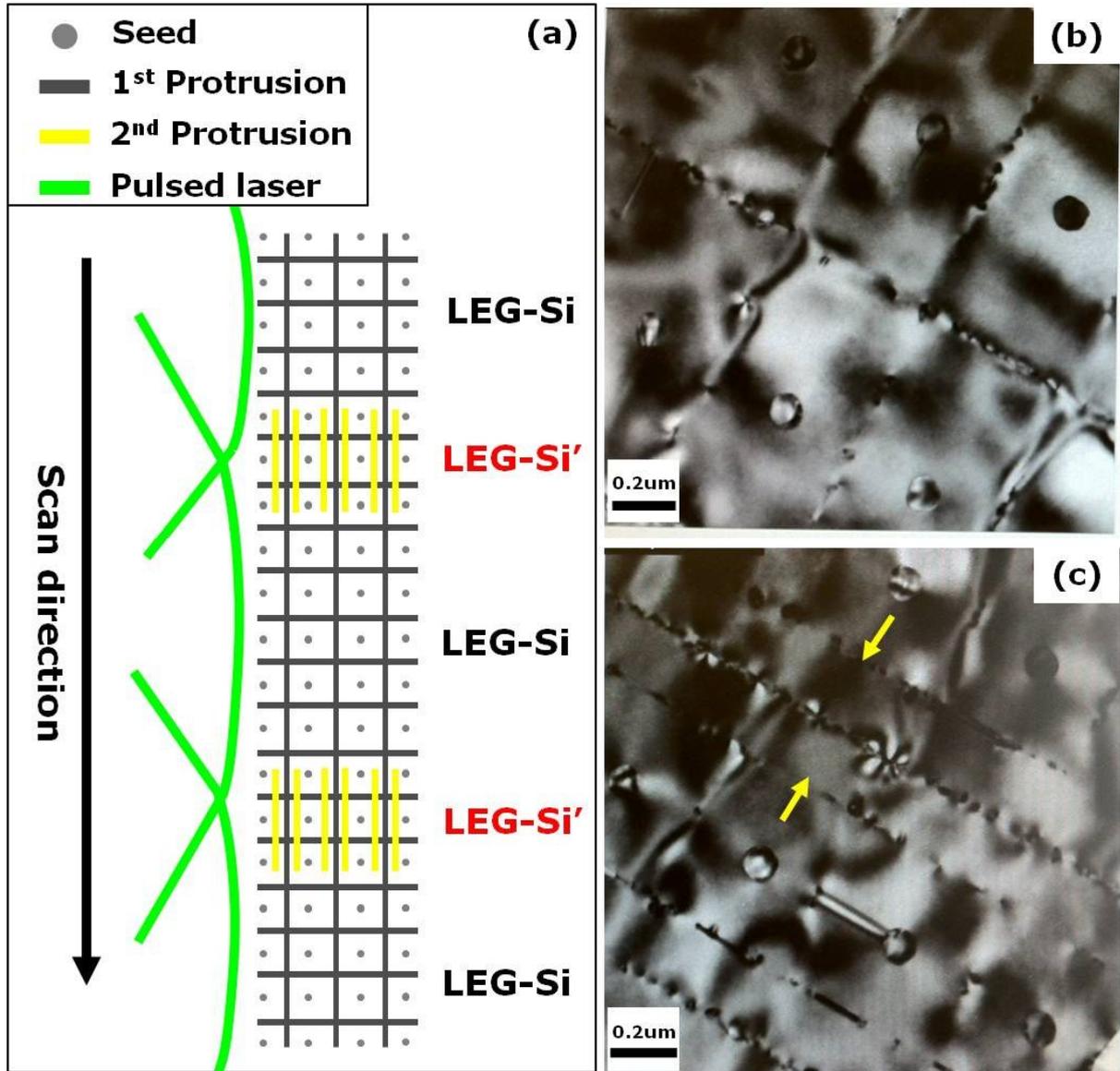


Figure 1.5. (a) Schematic diagram showing the beam scanning process with pulsed laser and periodic microstructures, planar transmission electron microscopy images of single irradiated regions (b) and beam overlapped regions (c).

However, in order to realize the microstructure of LEG-Si with the pulsed laser beam in a range of full chips, the pulsed laser beam was scanned by translating the wafer perpendicular to the length of laser beam. While scanning the laser beam, the

unexpected appearance of the periodical crystalline defect, called LEG-Si', is observed between the microstructure of LEG-Si as shown in Fig. 1.5. The microstructure of LEG-Si' is characterized by an additional protrusion which is precisely located at center of between the seed contact and the ready-made protrusion. The region of LEG-Si' always exist in the beam overlapped region, which indicates that this periodical LEG-Si' has a strong relation with overlapping of the incident laser beam. To understand these microstructures such as alternative LEG-Si and LEG-Si', the melt depth in overlapped region at second shot should be considered since there exists the variation of the film thickness just after first shot. With LEG-Si, Si atoms are transferred to make the hillock due to the density difference between liquid and solid of Si during the directional lateral solidification so that the film at the center of between neighbor seed contacts becomes to be thicker than that at the other areas as shown in Fig. 1.4 (a). When the second shot with energy density corresponding to the first shot is executed on LEG-Si films in leading edge of scanned beam, the thicker films in protrusion region leave the solid island while completely melting in other regions as shown in Fig. 1.6.

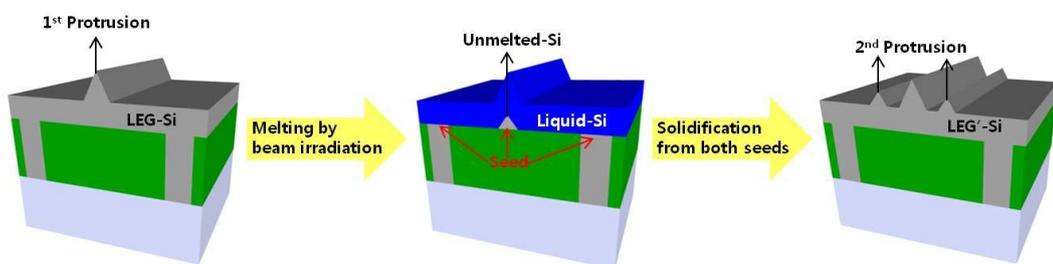


Figure 2.6. Melting and solidification scenario of LEG-Si'.

This residual solid Si serves as another seed of the lateral solidification and followed by

lateral growth until an impingement with the neighbor growth front from seed contacts, which accounts for the additional protrusions between the seed contact and the ready-made protrusion. However, as shown in Fig. 1.7, when LEG-Si in leading edge of scanned beam is encountered with 2nd pulse with beam profile lower than CMT, the films are partially melted and subsequently the epitaxial growth is induced from the unmelted bottom crystalline Si without any formations of the additional defect. Such epitaxial growth triggers LEG-Si once again. In the mean time, Poly-Si in leading edge of scanned beam is transformed to LEG-Si by second shot with beam profile over CMT because the thickness of protrusion in Poly-Si is thin enough to lead to complete melting of Poly-Si.

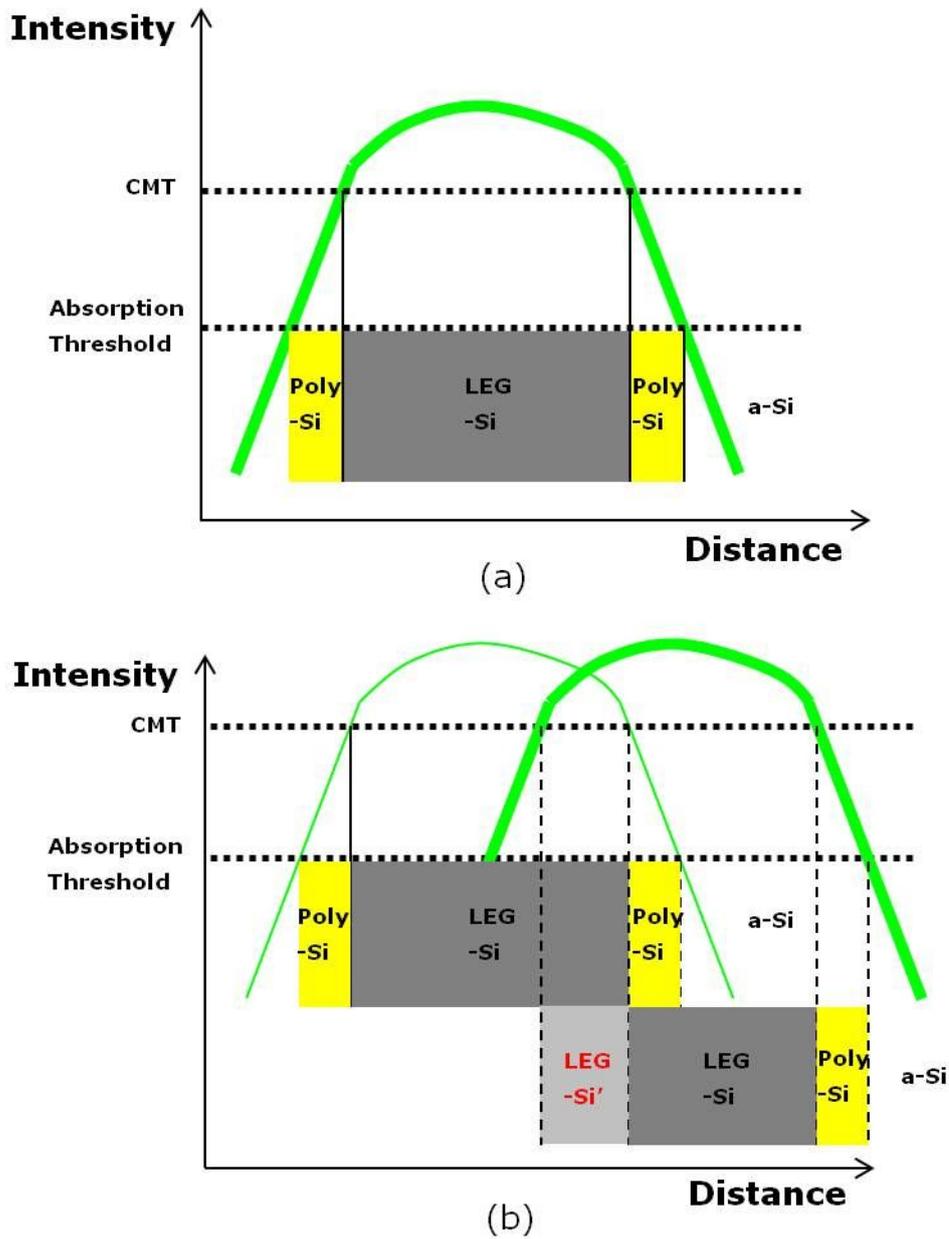


Figure 2.7. Microstructural distributions as a function of beam intensity after first shot (a) and second shot (b).

It turns out that although the single shot are capable of realizing the location controlled single crystalline over oxide layer, the scanned shot to cover the whole chip area

triggers an additional defect such as LEG-Si' which might deteriorate the performance of the stacked devices. As aforementioned, the occurrence of LEG-Si' is substantially caused by thickness of protrusions during lateral epitaxial growth. If the distance of between seed contacts is so close each other, the thickness of protrusions after first shot would become to decrease and be similar with that of the other regions, which results in complete melting of protrusions. In this case with the short distance between seeds, the scanned shot could make the location controlled single crystalline without the occurrence of LEG-Si'. However, since the location of seed contacts absolutely depends on the circuit design and architecture, the manipulations of the seed location would be not an applicable method preventing the occurrence of the additional defect. Therefore, considering the laser beam scanning with overlapping inevitably causes LEG-Si, it is necessary to introduce the chip-scaled laser system corresponding to stepper type laser beam for photolithography which can provide single shot over the entire chips on wafer.

1.4 Summary

In conclusion, we have demonstrated a LEG process which utilizes SEG process as a seed for epitaxial growth and excimer laser irradiation as a recrystallization source of amorphous silicon films. As a result, high quality and location-controlled single crystalline silicon over oxide layer can be successfully produced. The ultimate usefulness of LEG technology strongly depends on the uniformity of crystalline quality, the distribution of device characteristics and yield. Device results dealing with these concerns were successfully evaluated in transistor arrays and a product level.¹⁰ It is concluded that the LEG process is a promising candidate for obtaining single crystalline

silicon films on dielectric materials for three-dimensional system-on-chip applications.

Chapter 2

Laser Induced Epitaxial Growth for Stacked DRAMs

2.1 INTRODUCTION

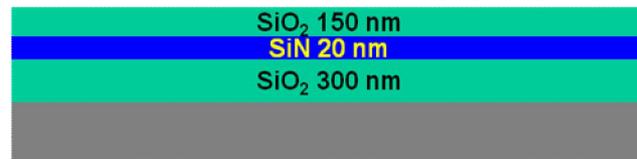
Semiconductor industry in recent years gradually turns its attention from conventional feature scaling to stack technologies, that is, three dimensional (3D) integration technologies. It has been pointed out that high performance, low cost, and small form factor would be viable in 3D integration technologies without a huge investment that has been inevitable for a new generation of lithography technology [1]. Moreover, in addition to the well-developed 3D integration based on through silicon via (TSV) technology [1], monolithic 3D integration has also been investigated as an ultimate solution for future ultra large scale integration [2-8].

The most critical aspect of monolithically stacked devices relies on high quality active formation at low temperatures below 400 oC, which is limited by the degradation of Cu interconnect induced by thermal stress [9, 10]. Accordingly, laser induced recrystallization or epitaxial growth with an appropriate seeding scheme has been suggested as a possible solution to attain high quality active formation in stack devices with low thermal budget preventing thermal stress problems of Cu interconnects [2, 11-

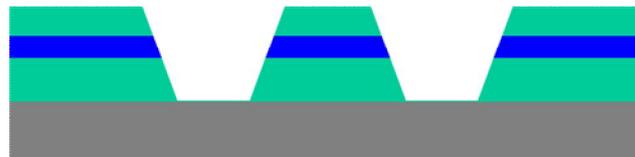
13].

Meanwhile, the thickness of active region in stack devices should be adjustable according to the device application of the corresponding stack layer. Especially, in the case of devices that require back bias applications such as dynamic random access memory (DRAM) or NAND flash, thick active regions with shallow trench isolation (STI) process would be necessary to accomplish back bias applications. In conventional STI process, high temperature processes such as sidewall oxidation and densification anneal are required to manage leakage currents of cell transistors that are critical in controlling refresh time of DRAM [14, 15] and program disturbances of NAND flash [16]. These high temperature processes are not applicable for monolithic stack devices, and thus development of low temperature isolation technology is highly required to realize monolithic stack devices employing memory layers. In this work, we present a low temperature STI process using laser-induced epitaxial growth (LEG) with silicon substrate as a seed material. This work presents a workable prototype device targeting monolithically stacked 3D device with thick active silicon layers, which can be applicable to stack DRAM, stack NAND flash, and other 3D stack integrated circuits employing memory layers. Furthermore, various device characteristics of cell transistors depending on LEG process conditions and possible advantages of this proposed technology will also be discussed.

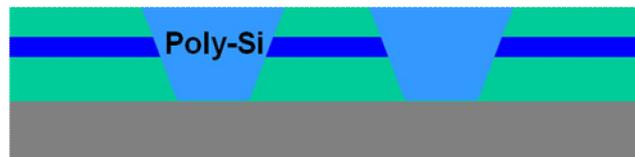
2.2 Experimental details



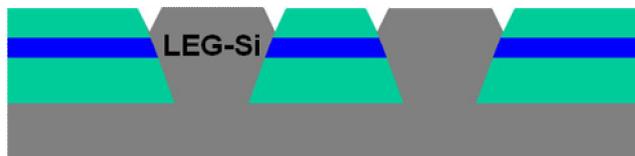
**Pre-deposition of isolation films
(SiO₂/SiN/SiO₂)**



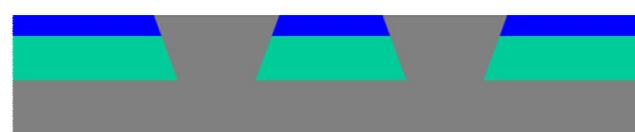
**Reverse patterning of active region
(Positive active profile)**



Si filling and node CMP



LEG; Laser-induced Epitaxial Growth



Planarization CMP (SiN Stopping)

Figure 2.1 Schematic process sequence of LEG isolation.

Fig. 2.1 shows the schematic sequence of the device isolation process using LEG. After a series of implantation steps for well formation, 300 nm thick SiO₂ film is thermally formed as an isolation layer on a p-type silicon wafer with (100) orientation and 8 inches in diameter; and 20 nm thick silicon nitride (SiN_x) film and 150 nm thick SiO₂ film are sequentially deposited by plasma enhanced chemical vapor deposition method to support the subsequent chemical-mechanical polishing (CMP) process. The reverse patterning of the active region is performed using an ArF-based photolithography, leading to a positive slope in the sidewall profile. Polycrystalline silicon film is deposited on this patterned wafer using a low-pressure chemical vapor deposition reactor at 530 °C, which is possible to be replaced with sputter deposition reactor at low temperature below 400 °C. , and then the wafer is planarized using a CMP process to remove the polycrystalline silicon on top of the oxide layer. In order to induce epitaxial growth of polycrystalline silicon in patterned area, Nd:YAG laser beam was irradiated with a wavelength of 532 nm and a pulse duration of 150 ns [8]. The energy density of irradiation laser beam was split by 800, 900, and 1000 mJ/cm² (denoted by E1, E2, and E3) to clarify the optimum condition for epitaxial growth.

Finally, a CMP process is performed until the exposure of SiN stopping layer to remove the faceted region and planarize the surface of the active area. The gate oxide was formed by thermal oxidation with the thickness of 4 nm. For electrical characterization of transistors prepared by various LEG process conditions, planar N-metal oxide semiconductor (NMOS) transistors were fabricated with the design rule of 80 nm, and other processes are followed by the front end of the line process technology of 80 nm DRAM , and more details regarding fabrication methods are reported

elsewhere [17].

2.3 Results and discussions

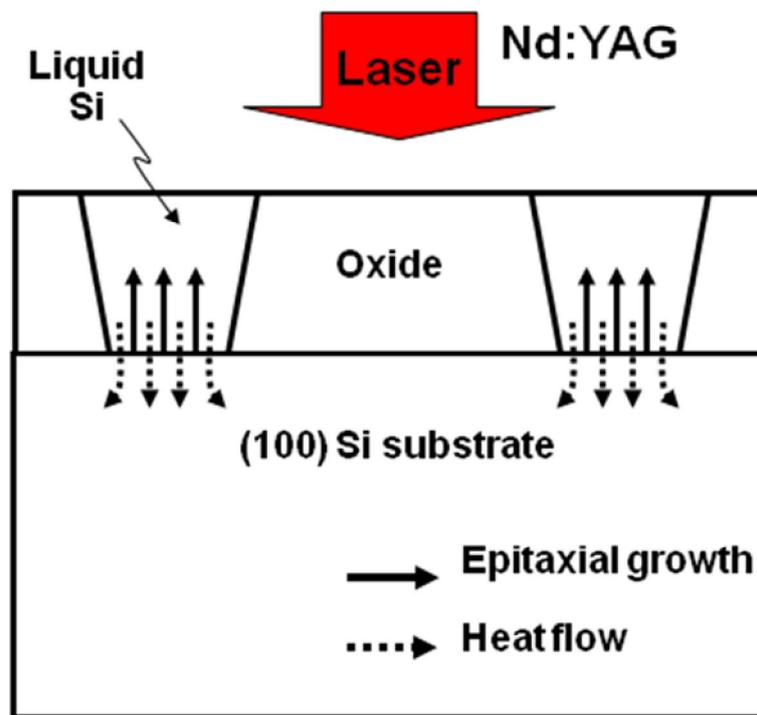


Figure 2.2 Schematic illustration of LEG process. Selective melting of Si active region and solidification from the crystalline Si seed are indicated.

Once the polycrystalline silicon in the active region is selectively melted by incident laser beams, the residual heat in the melted silicon may preferentially flow out through silicon substrate because the thermal conductivity and heat capacitance of silicon substrate are higher than those of sidewall oxide and air [8, 12] as illustrated in Fig. 2.2. In addition, incident laser beams which pass through oxide and nitride layers,

do not significantly affect silicon substrate since the absorption coefficient of single crystalline silicon is much lower than that of polycrystalline silicon. The melted silicon is rapidly solidified from the interface with silicon substrate which acts as a seed material, thereby leading to perfect single crystalline LEG silicon in the active region. As can be seen in Fig. 3.3, there are no crystalline defects in both LEG silicon and its interface with silicon substrate, as shown in the inset. Figure 3.4 shows a tilted view of active region after LEG process, where four symmetrical facet planes are uniformly formed at the top edge of LEG silicon.

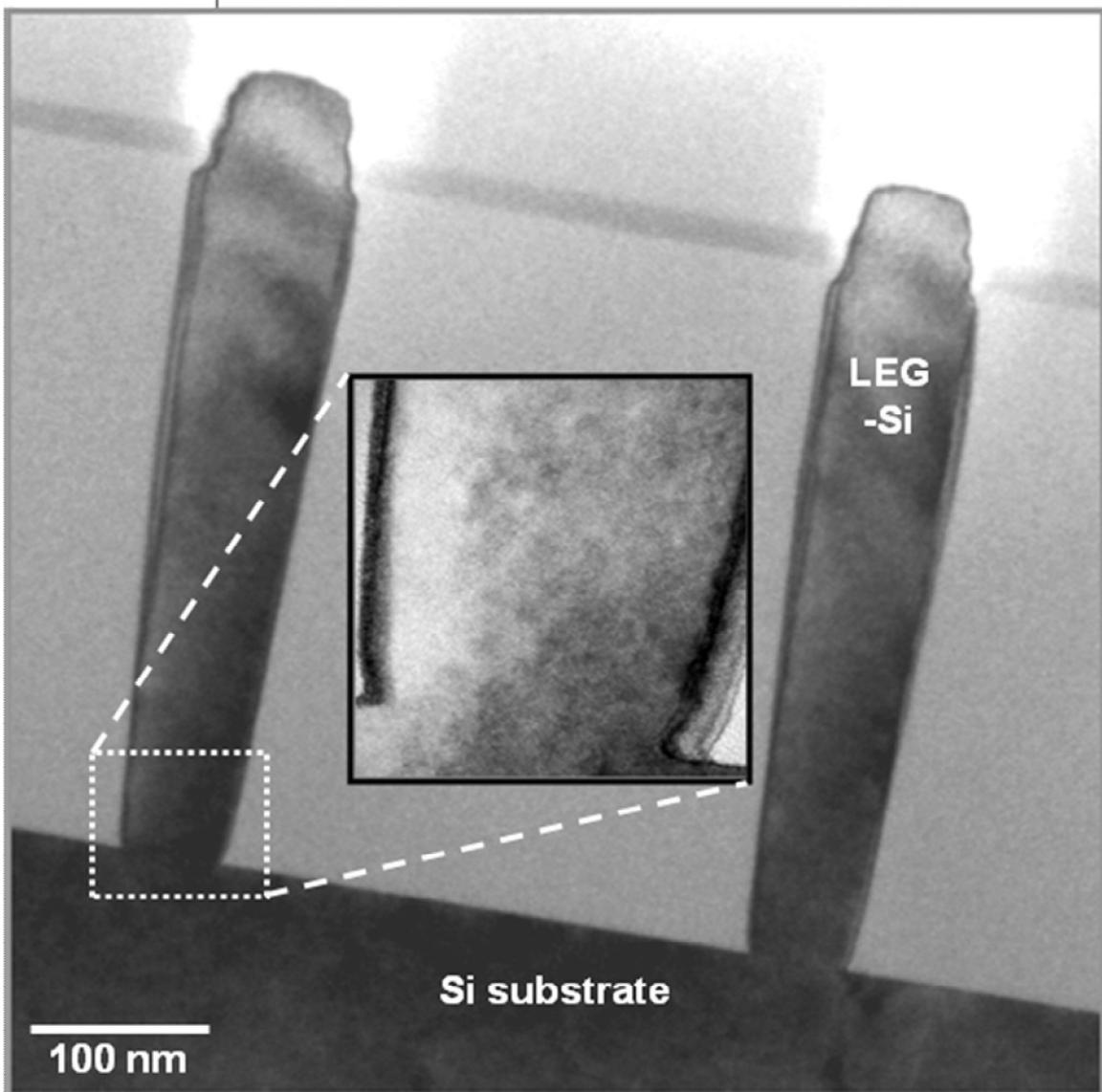


Figure 2.3 Cross section transmission electron microscopy image of LEG processed region. The inset shows the magnified image.

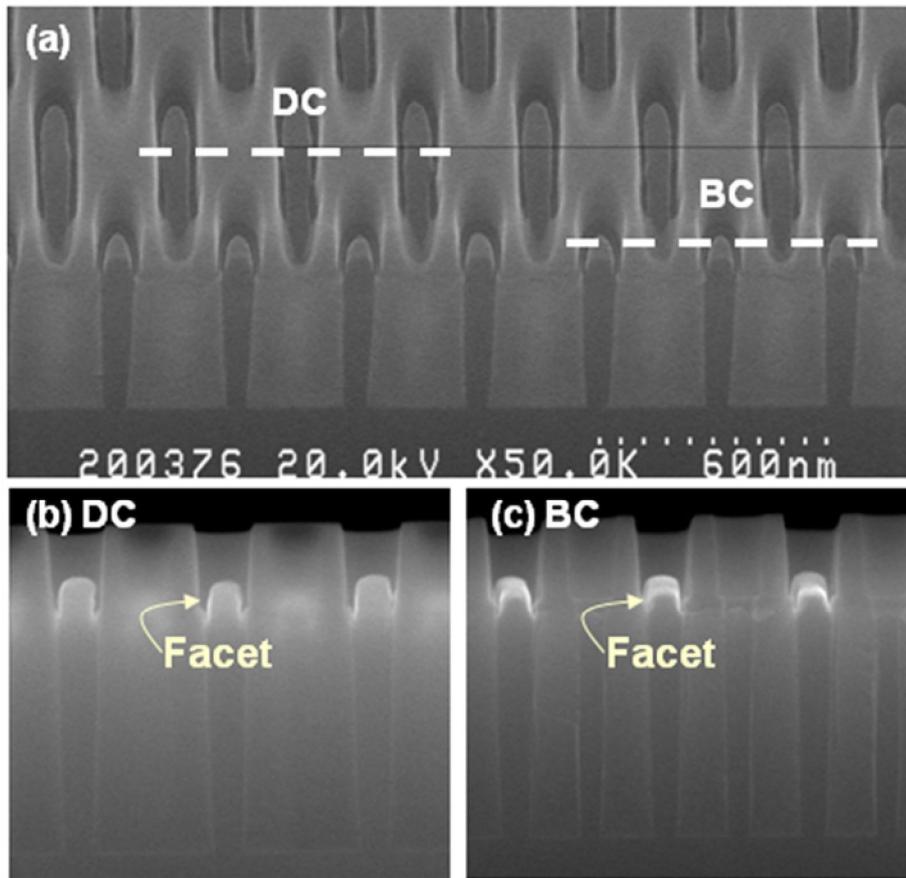


Figure 2.4 (a) Tilted scanning electron microscopy (SEM) image with a wide view. (b) Cross-section image in direct contact (DC) area. (c) Cross-section image in buried contact (BC) area.

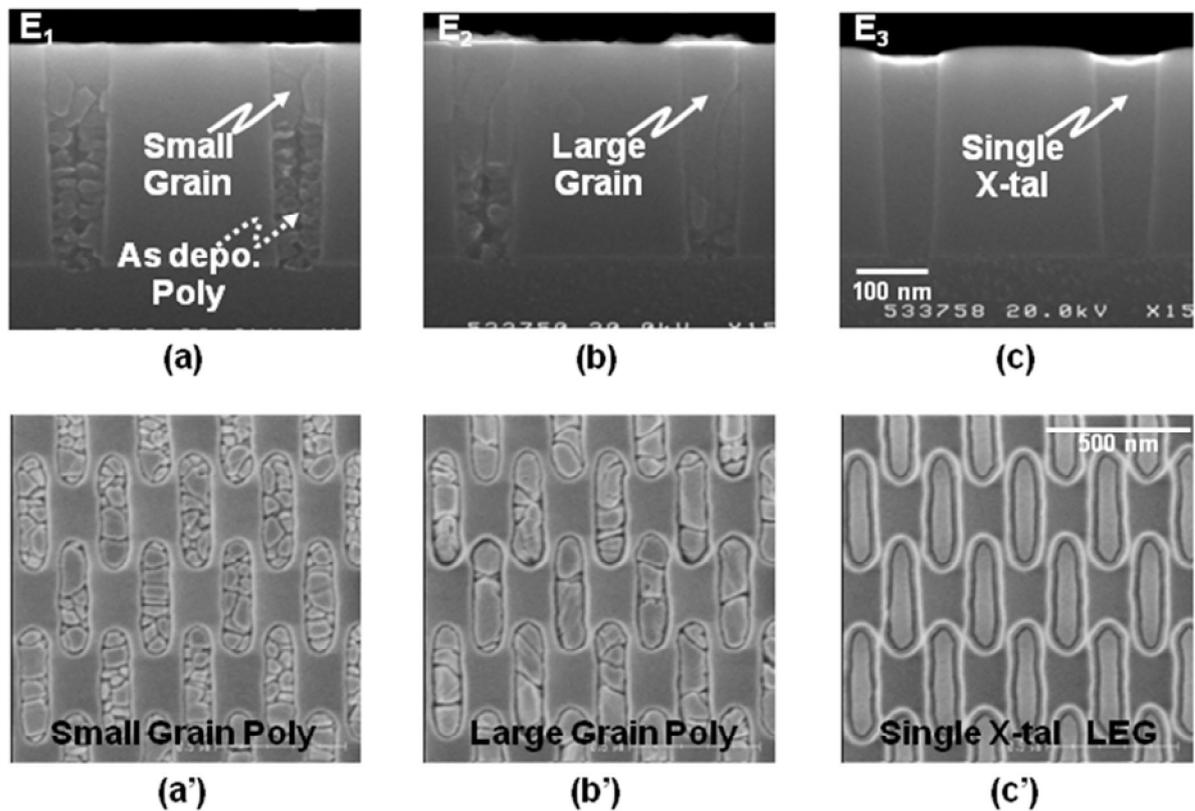
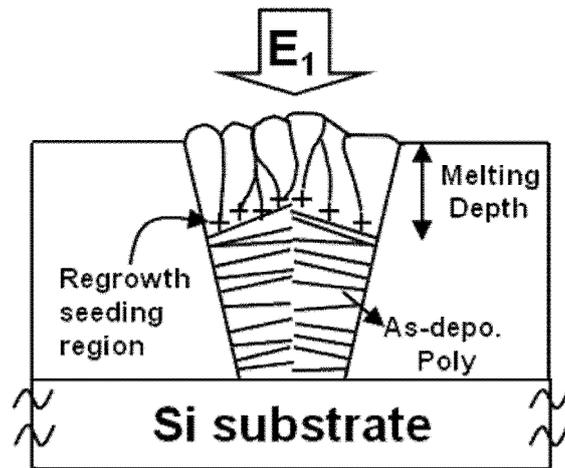


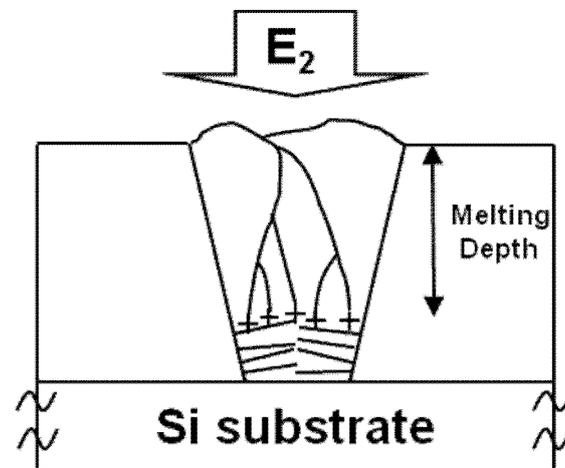
Figure 2.5 SEM images of LEG processed samples decorated by defect etchant at various energy densities. Cross-section view with (a) E_1 , (b) E_2 , and (c) E_3 . Plan-view with (a') E_1 , (b') E_2 , and (c') E_3 .

Figure 2.5 shows decorated cross-sectional SEM images ((a)~(c)) and planar SEM images ((a')~(c')) of LEG-silicon as a function of energy density of the incident laser beam. For the case of E_1 and E_2 , the microstructure of LEG silicon is composed of recrystallized polycrystalline grains at top region and deposited polycrystalline grains at bottom region. Furthermore, the grain size of recrystallized polycrystalline silicon at top region that was formed after being irradiated by the low energy density (E_1) is smaller than that of polycrystalline silicon by the medium energy density (E_2). On the other hand, for the case of E_3 , single crystalline structure was formed in the whole

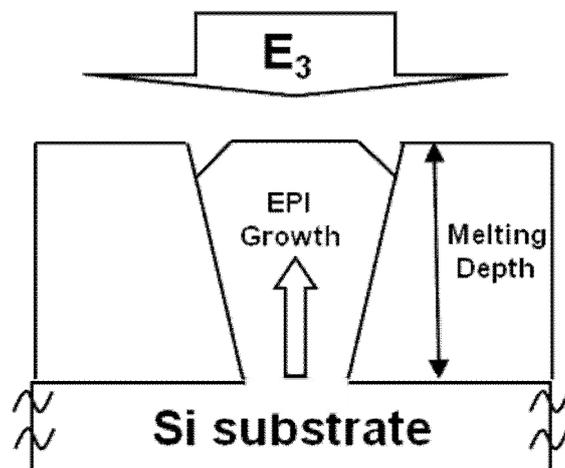
active silicon. In order to understand these different microstructures depending on the irradiation energy density, we speculate that the melting depth of silicon is proportional to the energy density of incident laser beam as illustrated in Fig. 2.6, providing that it is possible to analyze the recrystallization behavior of LEG silicon. As the melting depth of silicon becomes larger with the higher energy density, the occlusion of grains occurs, reducing the number of growing grains by the similar mechanism of grain-filter [18]. In addition, when the energy density of laser beam is high enough to completely melt the deposited polycrystalline silicon, the melted silicon becomes solidified from the melt/substrate interface in the form of liquid phase epitaxial growth, which implies that there exists a critical energy density of laser irradiation for the single crystalline silicon growth.



(a)



(b)



(c)

Figure 2.6 Schematic illustration showing energy density dependent crystallization behavior. (a) E_1 , (b) E_2 , and (c) E_3 .

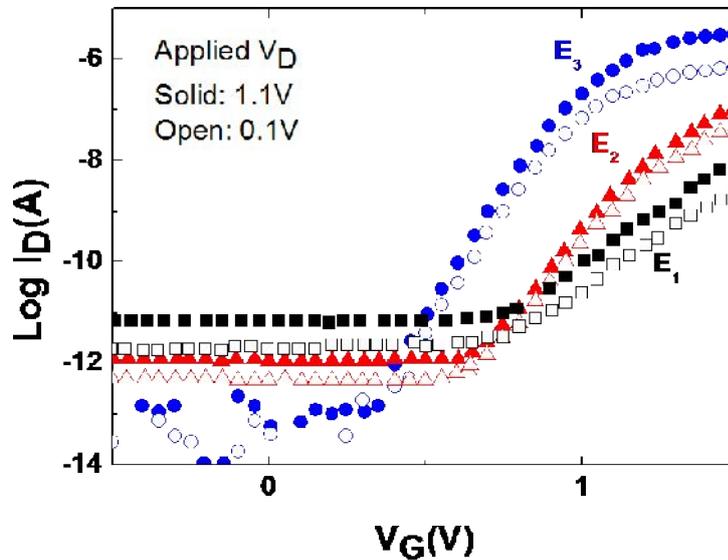


Figure 2.7 Transfer characteristics of cell transistors with different LEG process conditions. The source terminal is grounded and the body bias is -0.8 V. $W/L=80$ nm/ 80 nm. V_G is the gate voltage, and I_D is the drain current.

In order to utilize the LEG process for practical applications, it is required to clarify the transistor performance optimized by various LEG processes. Drain current versus gate voltage transfer characteristics of cell transistors prepared by various energy densities for LEG are shown in Fig. 2.7. A gradual increase of turn-on current and decrease of sub-threshold leakage currents are pronounced as the energy density increases from 800 mJ/cm 2 (E_1) to 1000 mJ/cm 2 (E_3). Inferior transistor characteristics of transistors with E_1 and E_2 are attributed to the nature of polycrystalline structure of the transistor active channel, which can be attributed to the well-established theory on polycrystalline silicon thin film transistor with reduced channel mobility and increased

subthreshold leakage [19]. On the other hand, the device with LEG silicon employing the energy density of E3 exhibits similar turn-on current and subthreshold characteristics compared to the device with bulk silicon as shown in Fig. 2.8.

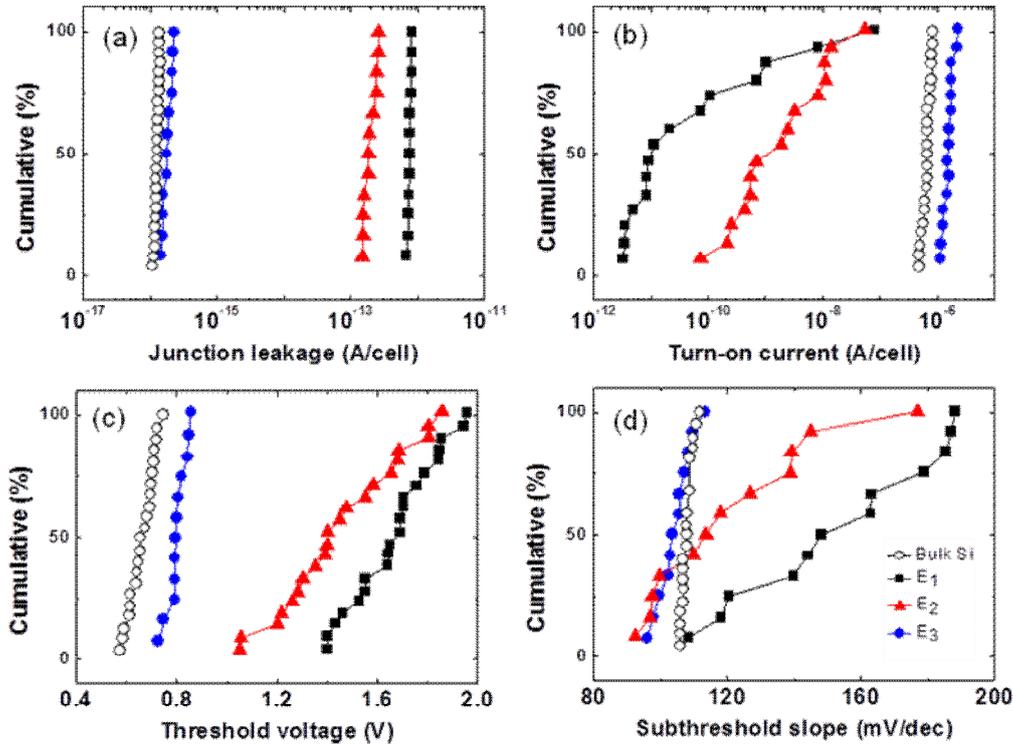


Figure 2.8 Distribution of transistor parameters for different LEG process conditions.

The measurement was performed at 12 ~ 25 devices in the same wafer. The measurement conditions are (a) $V_G=0$ V, $V_D=1.2$ V for junction leakages, (b) $V_G=1.2$ V, $V_D=1.2$ V for turn-on currents, (c) V_G at $I_D=10$ nA for threshold voltages, and (d) subthreshold slopes extracted by linear fitting from $\log I_D$ versus V_G plot. The measured junction leakage in parallel-connected 176,000 transistors ($W/L=80$ nm/ 80 nm) is divided by 176,000 again to represent the junction leakage for a single cell transistor.

Turn-on currents, threshold voltages, and subthreshold slopes were chosen from the measurement of single transistor test patterns ($W/L=80\text{ nm}/80\text{ nm}$).

Slightly larger turn-on current of the device with LEG silicon compared to the reference device shown in Fig. 2.8(b) can be explained by the decrease in the threshold voltage as shown in Fig. 2.8(c). This difference in the threshold voltage is attributed to the lower thermal budget of LEG STI process compared to the conventional one. Since high thermal budget is required for conventional STI process, boron impurities that were implanted for the well formation may have diffused out of the channel surface or into underlying silicon substrate; and thus lowering both the concentration of boron at the channel surface and the threshold voltage of conventional STI device. Therefore, considering the threshold voltage, and turn-on cell current of both devices, the transistors with LEG silicon channel can be regarded to have the similar performance with those with bulk silicon channel. Moreover, comparable distributions of junction leakages and subthreshold slopes of both devices allow us to conclude that the LEG silicon has a defect-free single crystalline nature. Larger threshold voltages, larger subthreshold slopes, larger junction leakages, smaller turn-on currents, and wider distribution of polycrystalline channel devices (i. e., for cases of E1 and E2) are attributed to the effect of grain boundary traps and the variation of grain sizes [19, 20]. The sharp distribution of junction leakage currents for the devices irradiated by the energy density of of E1 and E2 as opposed to the large distribution of other parameters is due to the fact that the extraction of junction leakage from large sized array transistors averaged the variability of individual devices.

Regarding process simplification and robustness, the proposed LEG isolation has the following advantages. First of all, the number of process steps for this LEG isolation scheme is approximately 20% smaller than that for the conventional STI process due to the elimination of sidewall oxidation, liner deposition, and densification anneal steps. In addition, after the CMP process to acquire flat surfaces of LEG silicon, SiN films reside selectively on field oxide, whereas SiN films are present on active silicon region in the case of conventional STI process. It should be noted that it may provides further advantage in terms of preventing the degradation of active silicon, which can be induced by the film stress of SiN on active silicon.

Monolithic stack technology is targeting multi-stack device on a single wafer. In this technology, several key processes in wafer-to-wafer, chip-to-chip, or chip-to-wafer 3D integration technologies such as alignment, wafer thinning, bonding, TSV formation, etc., are not necessary. In addition, potential cost reduction compared to other 3D integration technology is also expected due to the reduced wafer cost. Although low temperature active formation techniques utilizing laser induced epitaxy or single grain formation with some kind of patterned seed or microstructure have been suggested by several groups [11-13, 18], there are still copious issues for the complete design of whole integration processes at low temperatures. For example, low temperature silicon deposition, low temperature gate dielectric formation with sufficient reliability, low temperature dopant activation, low temperature isolation, etc., are key issues. Nonetheless, this work provides one part of the complete solution for the achievement of monolithic multi-stack devices, and the proposed LEG isolation would be promising, especially in the technology for 3D monolithic stack devices employing memory layers.

2.4 Summary

A simple isolation scheme using LEG process has been proposed with an established 80 nm DRAM fabrication process. It was found that the crystalline quality of LEG silicon is identical to that of bulk Si from both structural observation and electrical characterization of the cell transistors. The proposed LEG isolation is a promising ingredient in monolithic stack device technology with potential low cost and high performance, which must be an indispensable technology in stack devices with memory layers. On the basis of low temperature process capability of LEG and high quality of silicon epitaxial layer presented in this paper, the first decisive steps toward achieving high density 3D memory devices utilizing LEG process will be made in the near future.

Chapter 3

Laser Induced Epitaxial Growth for vertical silicon channel

3.1 Introduction

Recently, integration of memory cells such as flash or dynamic random access memory (DRAM) confronts serious scaling issues [1]. In case of DRAM, as an alternative technology with relaxed scaling constraints, capacitor-less one-transistor (1T) DRAM cells have been investigated by several research groups [2, 3]. Impact ionization or gate induced drain leakage generates excess majority carriers in floating body, which switches the channel conductance of metal-oxide-semiconductor field effect transistor (MOSFET) from a low conductance state to a high conductance state [2, 3]. The drain current between two states can then be sensed in the linear operation regime of MOSFET, allowing us to determine memory states. 1T DRAM can be scalable to the minimum unit cell area of $4F^2$ (F: minimum feature size) in vertical device architecture [3], which provides larger scale integration at the same technology node. Vertical integration of memory cells is also important in recent flash memory development [4], where the effective unit cell size can be reduced below $4F^2$ by three dimensional stacked integration. These indicate that the formation of high quality

vertical Si channel (VSC) is essential in nanoscale memory integration. In channel-first-gate-last scheme, VSC can be readily formed by etching Si wafers [5] via conventional semiconductor manufacturing processes, but several integration difficulties can be addressed in this scheme: e.g., forming gate electrodes with accurate vertical lengths and controlling sidewall profile or its surface roughness by dry etching [6]. In gate-first-channel-last scheme, high quality VSC can be attained without using Si wafers, which requires selective epitaxial growth techniques on pre-patterned vertical holes as VSC molds. Among selective epitaxial growth techniques [7], laser-induced epitaxial growth (LEG) has been proved to give high quality as Si wafers at low processing temperatures [8].

In this work, we have fabricated VSC transistors using the gate-first-channel-last scheme using LEG to prove that LEG is an essential element in nanoscale memory integration. In addition, 1T DRAM cell with an ultimate scalability of $4F^2$ will be demonstrated using the fabricated VSC transistor, whose promising aspect in scaling will also be discussed.

3.2 Experimental details

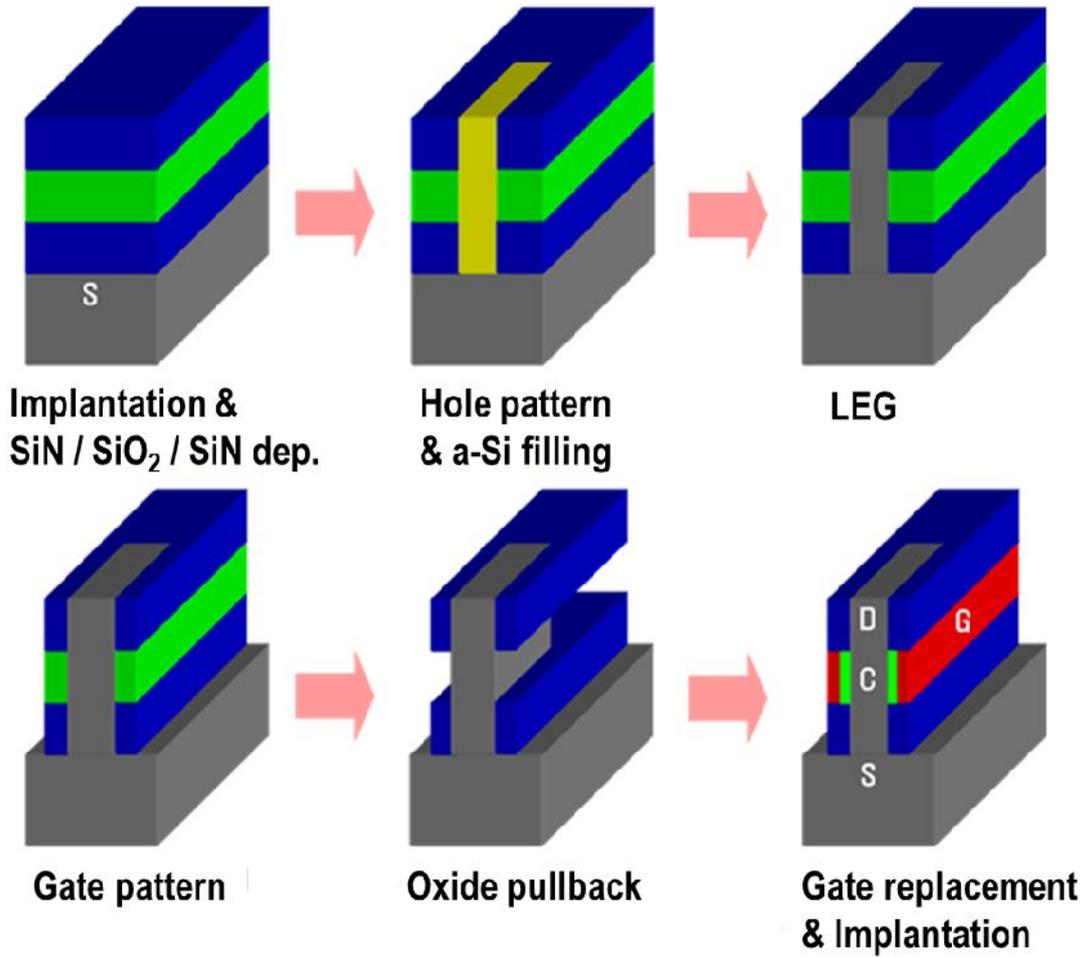


Figure 3.1 Schematic process sequence of gate replacement process.

Table 1 show the process sequence and detailed process parameters to fabricate the VSC transistors on a bulk-silicon substrate. Fig. 1 illustrates the sequence of gate replacement process, where single crystalline silicon channel is obtained by LEG process. After the conventional shallow trench isolation process, ion implantations (P+, 20keV, $8 \times 10^{12} \text{cm}^{-2}$) were performed to form bottom source and drain junctions. In addition, silicon nitride/silicon oxide/silicon nitride (SiN/SiO₂/SiN) layers were deposited by low pressure chemical vapor deposition (LPCVD); where the top and bottom SiN layers were used as the isolation layer, and the sandwiched SiO₂ was used for the dummy gate. The holes for transistor channels were patterned by ArF-based

photolithography and dry etching. Subsequently, amorphous silicon was deposited by LPCVD and then chemical-mechanical polishing process was employed to remove the amorphous silicon on top of the SiN layer. Afterward, in order to perform an epitaxial growth of amorphous silicon in the channel hole area, an Nd:YAG laser beam was irradiated with a wavelength of 532nm and a pulse duration of 150ns [9], where the energy density of irradiated laser beam was adjusted to optimize the epitaxial growth. The vertical channel region was doped by B⁺ ($3 \times 10^{13} \text{ cm}^{-2}$, 27keV) implantation to control short channel effect, and top source/drain junction was formed by ion-implanting P⁺ (10^{13} cm^{-2} , 10keV) and As⁺ (10^{15} cm^{-2} , 10keV) followed by a rapid thermal annealing at 1000°C for dopant activation. We have used two different types of gate dielectric (SiON and SiO₂/SiN/SiO₂) prior to the gate material deposition for a comparative study of 1T DRAM devices. Finally, we have used doped polycrystalline Si as the gate electrode, followed by the contact formation and metallization using a conventional silicon process technology.

Table I Details of critical process parameters in the fabrication of VSC, and their process sequence.

Parameters	Conditions	Process sequence
Pillar height	150nm	● Shallow trench isolation
Pillar	130nm	● SiN/SiO ₂ layer deposition
Gate oxide	SiON, ONO	● Channel hole etch
Channel Si	a-Si, poly-Si, c-Si	● Channel Si formation (a-Si dep. & crystallization by LEG)
Gate material	Doped Poly-Si	● Gate replacement process (oxide etchback, oxidation, poly-Si dep.)
Gate length	80nm	

- Contact formation
- Metallization

3.2 Results and discussions

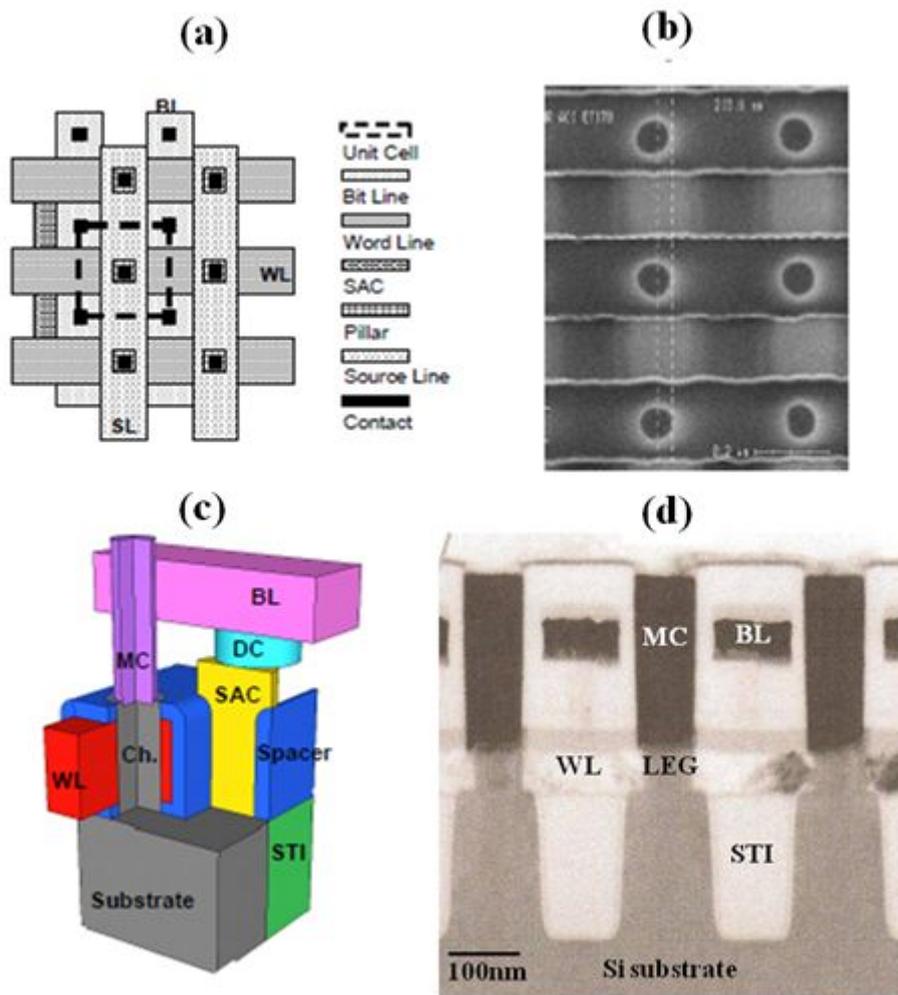


Figure 3.2 Schematic diagrams and electronic microscopy images of VSC transistors, (a) planar layout, (b) planar SEM image, (c) three dimensional illustration, and (d) cross sectional TEM image.

Figure 3.2 shows schematic diagrams and electron microscopy images of VSC transistor, where Figure 3.2 (a) displays the layout of the VSC transistor with the gate all around structure and the unit cell area of $4F^2$. The planar scanning electron microscopy (SEM) image in Figure 3.2 (b) depicts the contact hole with a diameter of 90nm. Figure 3.2 (c) illustrates three dimensional schematic representing the unit cell area of $4F^2$ with stacked word line (WL), bit line (BL), self-aligned contact (SAC) to the active Si, and direct contact (DC) to SAC shifted by $0.5F$. In Figure 3.2(d), a cross-sectional transmission electron microscopy image of the fabricated VSC transistor is shown, where single crystalline VSC is formed by LEG.

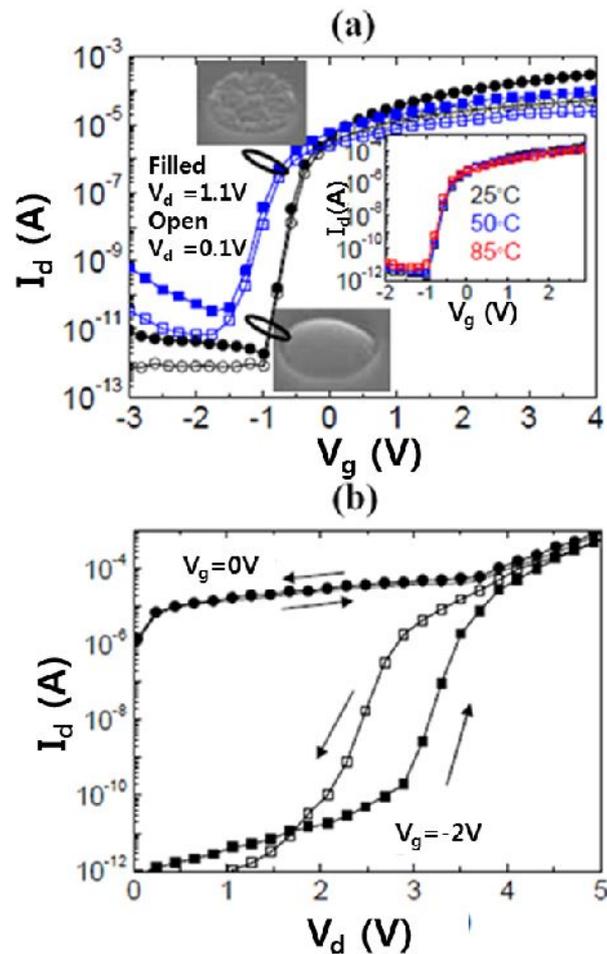


Figure 3.3 (a) Transfer curves of the VSC transistors with polycrystalline (upper curves) and single crystalline (lower curves) VSC. Inset shows the planar SEM images of surface morphologies of poly crystalline (upper image) and single crystalline LEG Si (lower image). Right inset shows temperature dependent transfer curves of VSC transistor with single crystalline Si channel. (b) The output characteristics (semi-logarithmic current versus voltage) of VSC transistor with hysteresis measurement.

The crystallinity of VSC plays a crucial role in the device performance. The polycrystalline and epitaxial single crystalline silicon channels are prepared by changing the energy density of the incident laser beam ranging from 700mJ/cm² to 1000mJ/cm² during the LEG process [9-12]. Figure 3.3(a) shows the transfer characteristics of the vertical pillar transistor with polycrystalline (900mJ/cm²) and single crystalline (1000mJ/cm²) LEG silicon. For the fabricated transistor with the single crystalline LEG silicon, the electrical characteristics can be summarized as follows: field effect mobility of 300cm²/Vs, threshold voltage of 0.2V, and sub-threshold slope of 100mV/decade. While the transistor with poly-crystalline silicon shows field effect mobility of 80cm²/Vs, threshold voltage of -0.3V and sub-threshold slope of 145mV/decade. In addition, the inset SEM images in Figure 3.3(a) indicate different surface morphologies of polycrystalline and single-crystalline Si depending on the energy density of the incident laser beam. Moreover, negligible temperature dependence in leakage currents of VSC transistor with LEG Si indicates high quality crystalline nature (inset graph of Figure 3.3(a)) [13,14].

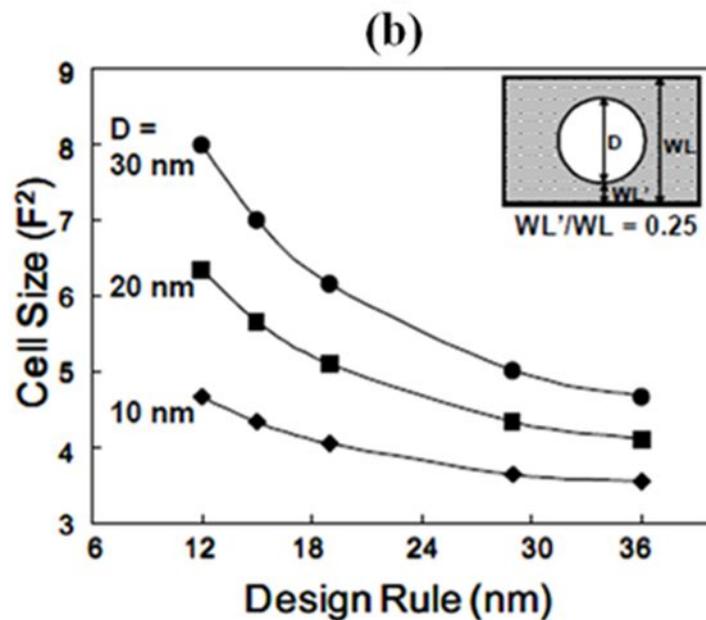
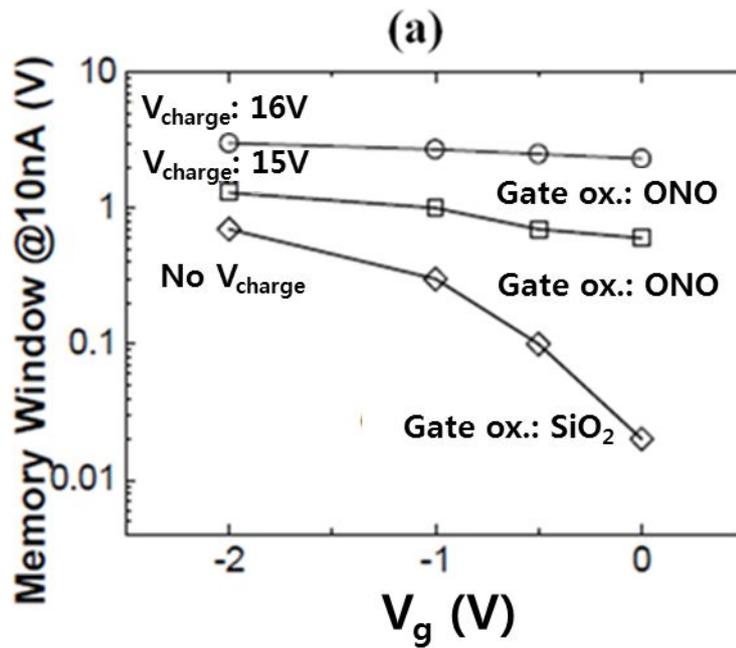


Figure 3.4 (a) Memory window versus applied gate bias at various charging conditions.

(b) Simulated cell size (the unit is the square of the minimum feature size F) of VSC transistor versus design rule, where three pillar diameters are applied.

The drain current of VSC transistor is a function of the potential of VSC, and the

potential at VSC is variable according to the charge density in VSC. That is, due to the floating body effect [2,3], the VSC transistor can be used as 1T DRAM. Drain voltage hysteresis demonstrates the floating body effect as shown in Figure 3.3(a). Considering that the measurement time of hysteresis sweep was estimated to be around 100ms, the memory window determined from this drain voltage implies the memory window for the 100ms retention time. As shown in Figure 3.3(a), the memory window is 0V at the gate bias of 0V, while memory window of 0.7V is observed with the gate bias of -2V. This implies that an additional negative gate bias is required for sensing with refresh time around 100ms in our VSC 1T DRAM. Applying a negative bias of -2V on the gate provides a deeper potential well for the storage of excess holes inside the vertical silicon channel, which increases the memory window and retention time [2,3].

Electron trapping at the gate insulator is an alternative strategy for the enhancement of the memory window instead of the negative gate bias. To prove this concept, two types of gate dielectrics, i.e., SiON and SiO₂/SiN/SiO₂ (ONO), were compared to observe the further enhancement of memory window. The former is almost trap-free dielectric, and the latter has a trap-rich SiN layer between trap-free SiO₂ layers. Prior to applying drain bias for the hysteresis measurement, charging bias (V_{charge}) was applied to trap electrons in the gate dielectrics. In an ONO gate dielectric, electrons are charged in nitride layer by tunneling through the bottom oxide, which is a well-known mechanism in charge trap flash memories [15]. The negative charges in the gate dielectric enhance the junction barrier between the channel and source/drain. As shown in Figure 3.4(a), electron trapping at ONO gate dielectric enhances memory window, and this enhancement increases with more electron trapping by increasing V_{charge} . Charge retention of ONO can be larger than 10 years [15], and thus, V_{charge} is

necessary only during the memory production. This approach based on charge trapping gives more promising options in the application VTC 1T DRAM since negative voltages are not required for device operations.

In scaling VTC 1T DRAM, the diameter of the pillar is the key parameter in determining the cell size. Figure 3.4(b) shows simulated cell size of VTC 1T DRAM versus design rule, where several pillar diameters are used and the width of WL is set twice of the design rule. It is seen that VTC 1T DRAM can provide a solution for high density DRAM with the cell area of about $4F^2$ when structure parameters are optimized, that is, smaller pillar diameter is crucial. To attain ultimate scalability in VTC 1T DRAM, development of patterning and dry etching technologies for nano-sized holes would be important; and further investigation on the performance of LEG in nano-sized pillars is also required.

3.3 Summary

In summary, we have demonstrated that LEG is a promising process method for nanoscale memory integration by demonstrating high performance VSC transistors with field effect mobility around $300\text{cm}^2/\text{Vs}$. In addition, we have demonstrated a VSC 1T DRAM by employing charge trap gate dielectric, which exhibited enhanced memory window as the amount of charge trapping increased. We believe that high quality VSC by LEG is a promising elements in future nanoscale memory integration, and in particular, VSC 1T DRAM harnessing charge trap dielectric will provide a solution for scaled DRAM below 20nm.

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