Ph.D. DISSERTATION

Interfacial Characterization of GaAs MOS Capacitors and Passivation using High Pressure Oxidation and Ti Scavenging Effect

by

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Abstract

Recently GaAs has attracted great attention as a promising channel material for sub-10nm logic metal-oxide-semiconductor field effect transistor (MOSFET) due to its high electron mobility and relative large band gap, which allows a high speed operation and low off-state current of the resulting FETs compared to their conventional silicon devices. However, many problems to limit the realization of the MOSFET have still remained unsolved in spite of enormous amount of researches accumulated over the past 3 decades. For such problems, thermal instability of GaAs native oxide can be firstly considered as one of the most crucial issues. The instability of GaAs oxides tends to induce high density of interface states, resulting in Fermi level pinning and frequency dispersion in capacitance-voltage (C-V) curve.

In this study, MOS capacitors using GaAs and various gate dielectric films were fabricated. Electrical characterizations were performed to evaluate the interface properties through C-V hysteresis, frequency dispersion, E_F movement efficiency and interface states density. Especially to evaluate the deep level interface states of GaAs, C-V and G-V measurements at elevated temperature up to 125 ℃ were tried in this study. Interfacial analysis by XPS, AES, and TEM were also performed to investigate the compositions and structures of GaAs surface.

Firstly electrical characterizations of GaAs MOS devices were examined to

evaluate the interface states. Significant frequency dispersions in depletion region at high temperature suggest that higher density of interface states exist near the mid-gap. Consistent results were also obtained in the D_{it} distribution, extracted from conductance method. It was confirmed that huge interface states more than $x10^{13}$ $cm^{-2}eV^{-1}$ was observed in the mid-gap region not band edge unlike Si showing the U-shape profiles.

To investigate the origin of the high mid-gap D_{it}, the effects of Ga oxide at GaAs interface were examined by adopting the thin Ga_2O_3 insertion layer, which was deposited by ALD on GaAs prior to gate dielectric film. For the Ga_2O_3 inserted samples, two times larger hysteresis and huge frequency dispersions in C-V curves compared to the control Al_2O_3 were observed indicating that the Ga_2O_3 acts as the defective species inducing high interface states. Different electrical results according to dielectric materials could be explained correlated with the amount of interface Ga_2O_3 which can be naturally formed during thermal process.

For the passivation of the GaAs interface, new approaches using high pressure oxidation and Ti scavenging effect were employed to suppress the Ga_2O_3 generation. For high pressure oxidation samples, hysteresis and frequency dispersion at the depletion range were substantially improved. Significant reduction of mid-gap D_{it} was also observed down to 3.4×10^{12} $cm^{-2}eV^{-1}$ at E_i + 0.25 eV and 6.2×10^{12} $cm^{-2}eV^{-1}$ at E_i - 0.2 eV in upper half and lower half band gap respectively, which was less than half level of un-passivated samples. These improvements are attributed to the composition

rearrangement converting to As excess and Ga deficient surface. This composition surface can be obtained by selective oxidation of Ga and subsequent removing of Ga_2O_3 through high pressure oxidation and HF wet etching, respectively. This surface structure can effectively block oxygen transfer to the GaAs substrate and suppress the generation of interfacial Ga_2O_3. In this case, high pressure process was also verified to be more effective to form As layer compared to atmospheric pressure process.

For Ti passivation, reductions of hysteresis and interface states by ~40% were also obtained. From the XPS analysis much less Ga_2O_3 were observed in Ti inserted sample compared to control sample. Scavenging effect due to high oxygen affinity of Ti is believed to effectively suppress the surface oxidation resulting Ga_2O_3.

In conclusion, high pressure oxidation and insertion of Ti scavenging film are the effective ways to passivate the GaAs interface for controlling the formation of Ga_2O_3 at the interface.

Keywords: GaAs, Ga oxide (Ga_2O_3), elemental As, interface state, high pressure oxidation, scavenging effect

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1. Introduction

The continuing shrinkage of semiconductor devices is required for high performance and low power consumption. From Moor's law, 30% scaling down is needed at every generation node. However, for 30 - 40nm range devices, dimension scaling will reach the ultimate limitation with only conventional semiconductor materials and technologies due to technical difficulties associated with nanoscale shrinkage. The representative issues would be short channel effect and V_{th} mismatch for smaller transistors, and large gate leakage current for thinner gate oxides. To overcome these problems, many researches for replacement of conventional SiON/Poly-Si with new high-k/metal gate have been performed [1-9] and for the first time the high-k/metal gate technologies began to be employed in semiconductor industry in 2007 [10, 11].

On the other hand, since the next generation devices beyond 20nm have the obvious limits for improving the performance in the further scaled device using only high-k/metal gate process, intensive researches for introduction of new materials and structures to solve these problems have been performed [12]. Generally three major topics are discussed for future technologies: ultimate EOT scaling, multi-gate transistor, and high mobility channel device as depicted in Fig. 1.1 [13].

For ultimate EOT scaling, introduction of higher-k dielectrics as substitute

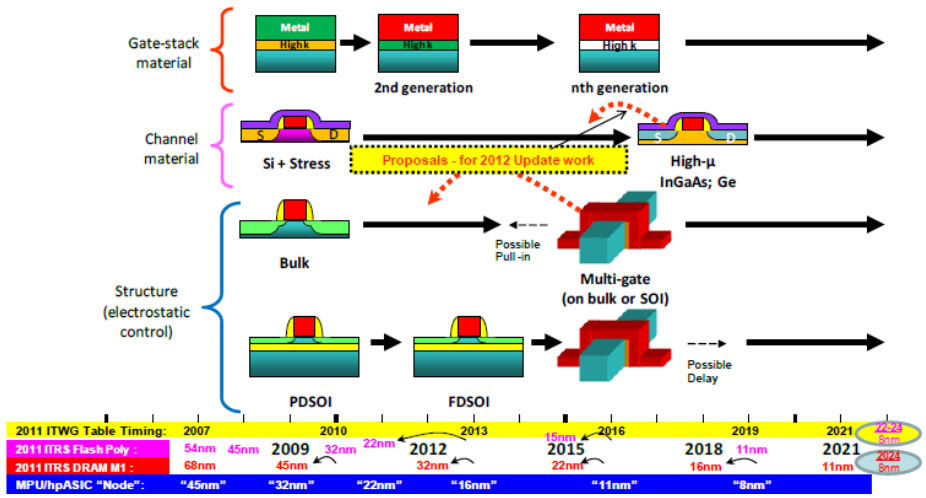


Figure 1.1. 2011 ITRS "Equivalent Scaling" Process Technologies Timing [13].

for current HfO_2 and suppression of low-k interfacial layer using scavenging effect have been primarily studied [14, 15].

For the multi-gate transistor, high speed operation is possible through the increased area of current path [16-18]. In addition, improvement of short channel effect can be obtained by better electrostatic control. Recently many device makers adopted this technology for 20nm and 10nm range logic devices.

In case of high mobility channel device, Ge and III-V compound semiconductors have been studied for long times as potential candidates for replacement of conventional Si substrate [19-25]. It has been proposed that n- and p-channels are separately formed using GaAs and Ge respectively. Some of leading semiconductor companies published the research of quantum well field effect transistor (QWFET) using InGaAs [26-28]. However, while the semiconductor road map for 20nm and 10nm range devices clearly suggest the prospective technologies like ultimate EOT scaling and multi-gate transistors, there is still no definite solutions for sub-10nm device in spite of exploring of Ge and III-V materials for next generation channel devices beyond Si.

For GaAs, a great deal of attention has been attracted as a promising channel material for sub-10nm devices due to its high electron mobility and relative large band gap, which allows a high speed operation and low off-state current of the resulting FETs compared to their conventional silicon counterparts [29-32]. However, many problems to limit the realization of the

metal-oxide-semiconductor field effect transistor (MOSFET) have still remained unsolved in spite of enormous amount of researches accumulated over the past 3 decades.

For such problems, thermal instability of GaAs native oxide can be firstly considered as a most crucial issue [33-38]. In the case of Si MOSFETs, the thermal SiO_2 film has excellent interfacial properties and thermal stability with respect to the Si substrate, which allows a low D_{it} and low subthreshold gate swing of the resulting FETs. On the other hand, the thermal oxides of GaAs tend to induce unwanted interfacial defects due to lower stabilities. It is well known that such these defects can generate the high density of interface states that can induce Fermi level pinning and hence deteriorate the frequency dispersion and hysteresis properties in capacitance-voltage (C-V) curves [30, 39-44]. Reliability issues such as V_{th} shift or dielectric breakdown originated from these interfacial defects are also concerned. In order to passivate the interfacial defects, various approaches have been proposed including epitaxial growth of Ga_2O_3(Gd_2O_3) [45-47], Ge [48] or Si [49-51] passivation layers, hydrogen passivation [50, 52], sulfur treatment [53-60], and arsenic decapping of GaAs surfaces [61]. However, unfortunately, we have no enough information about the fundamental degradation mechanisms of the GaAs interface. Therefore, understandings of defective species leading the interface degradation as well as the improvement of the interface quality are required for high performance GaAs channel devices.

Secondly, it can be pointed out that selection of appropriate high-k oxides

for GaAs MOSFET are not decided yet. Various high-k oxides for GaAs devices have been examined whereas Hf based oxides were fixed for Si devices [62-65]. Until now, several positive results have been reported including $Ga_2O_3(Gd_2O_3)$ grown by molecular beam epitaxy (MBE), which is not compatible with mass production. Therefore it becomes key issue to decide suitable high-k oxides having superior electrical characteristics as well as high productivity.

Thirdly, the difficulties of mass-production can also be regarded as critical obstacle in adopting new technologies. There are no practical methods for epitaxial growth of Ge or III-V semiconductors on 300mm Si substrate except MBE showing very low productivity. Many buffer layers to reduce the stress induced by difference of lattice constants can make the process complex and expensive.

This study is primarily focused on the first and second topics which were mentioned above: thermal instabilities of GaAs enabled to induce the interface states and selection of appropriate high-k dielectrics which can mitigate these interfacial defects. Defects species at the interface and its degradation mechanisms are also discussed. Furthermore, new passivation methods using high pressure oxidation (HPO) and insertion of Ti scavenging layer to suppress the interfacial defects will be presented in detail. For HPO, the passivation effect will be explained through the evolution of surface composition of GaAs analyzed by x-ray photoelectron spectroscopy (XPS) and auger electron spectroscopy (AES). For Ti scavenging passivation,

suppression of defect species will be addressed in terms of strong oxygen affinity of Ti.

This dissertation is organized with 5 chapters. In Chapter 2, thermal stabilities of the native oxides of GaAs and electrical characterization of the MOS devices in literature are described. Various passivation processes of GaAs surface are also given with recently published paper. Chapter 3 shows experiments and analysis methods employed in our study. Fabrication of MOS capacitors using various dielectrics and surface treatments are illustrated in detail. Different methodologies of electrical characterization of GaAs samples compared to Si are introduced based on C-V and G-V measurements. Chapter 4 provides the degradation mechanism and the passivation processes to improve the interface qualities. To evaluate the mechanism, the effects of Ga_2O_3 at the GaAs interface on electrical properties are discussed. Electrical properties depending on high-k gate dielectrics are explained relating to Ga_2O_3. Two passivation methods using high pressure oxidation and Ti scavenging effect are presented. In HPO part, different oxidation conditions are also examined and compared with HPO condition to investigate the effect of pressure and temperature during thermal oxidation. Finally, Chapter 5 summarizes the conclusions of this study.

2. Literature Review

2.1. Oxide formation of GaAs

2.1.1. Stable oxidation states on GaAs

It is well known that As_2O_3, As_2O_5, Ga_2O_3, Ga_2O, and $GaAsO_4$ can be generated by the oxidation of GaAs [33-35, 66-69]. Gibbs free energies of the relevant bulk native oxides of InGaAs are shown in Table 2.1 [39, 42, 67, 69, 70]. In terms of the relative stabilities of Ga-oxides and As-oxides, these Gibbs free energies can provide the useful guideline that the lower free energy indicate the more stable oxide. From the comparison of the $Metal_2O_3$, it is clearly shown that the As-oxides are the most unstable while the Ga-oxides are the most stable. This holds true for other oxidation states like $Metal_2O$. From these trends, the progression of native oxides on the substrate can be easily expected when the high temperature processes are given. Therefore less stable oxides like As_2O_3 can be easily removed or converted to the more stable oxides, in particular Ga_2O_3. Because of the stability of this particular oxidation state, this stable oxide can remain during typical chemical processing or relatively low temperature thermal desorption.

As shown in Fig. 2.1, native oxides composed mainly of As 5+, As 3+, Ga 3+, and Ga 1+ oxidation states and a small amount of elemental As can be

Table 2.1. List of stable InGaAs-oxides and their bulk oxide Gibbs free energies. Also shown are XPS core-level binding energies of the stable oxides [39, 42, 67, 69, 70].

Oxide	Gibbs free energy, ΔG (kcal/mol)	XPS core-level binding energy (eV)	
Ga_2O	−75.3	1117.3 (2*p*3/2)	19.6 (3*d*)
Ga_2O_3	−238.6	1117.9 (2*p*3/2)	20.2 (3*d*)
$GaAsO_4$	−212.8	1118.8 (2*p*3/2)	21.1 (3*d*)
In_2O_3	−198.6	444.7 (3*d*)	
$InAsO_4$	−209.4	445.3 (3*d*)	
As_2O_3	−137.7	1325.4 (2*p*3/2)	43.7 (3*d*)
As_2O_5	−187	1326.7 (2*p*3/2)	45.0 (3*d*)

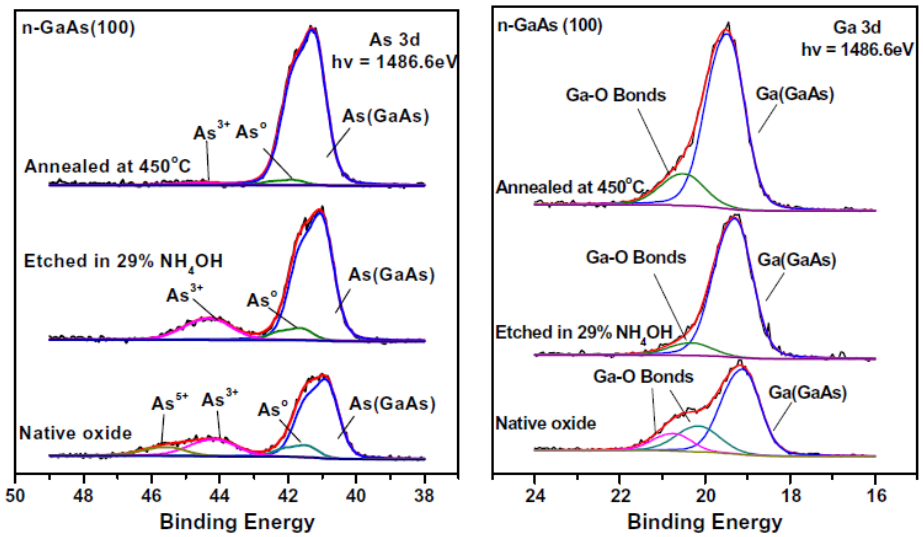


Figure 2.1. XPS core-level spectra showing the oxidation states of GaAs native oxide [68, 69].

created at the low growth temperature [68, 69]. However if the oxides are formed at higher temperature or annealed under an increased thermal budget, the composition of the oxide can change dramatically. As-oxides become less pronounced due to less stability as the temperature increases and eventually sublimate from the oxide layer or oxidize the GaAs resulting in the formation of stable oxides like Ga_2O_3 [39]. As-oxide can be further reduced by a post-etch, in situ anneal in vacuum up to 450 ℃. From the XPS analysis of the O1s for the annealed surface, it is found that the O intensity for the etched surface and the annealed surface is comparable, suggesting that no significant oxygen loss occur. Therefore it implies that the bond conversion from As–O bonding to Ga–O bonding arises under such annealing treatments. For temperatures above 500 ℃, As-oxide is below the detection limit while the oxide becomes almost completely Ga_2O_3. According to Eq. (2.1) [67],

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \qquad (2.1)$$

elemental As should also appear for these higher temperature process which is reported in most of the literatures[68, 69]. As expected in the reaction (2.1), this elemental As is primarily located at the interface. Some of elemental As may diffuse through the oxide layer to form $GaAsO_4$ or As-oxide which is highly unstable and easily evaporate during annealing [71].

2.1.2. Ga-suboxides

Because the As-oxides are very unstable and easily decomposed to elemental As under chemical and thermal process, the role of Ga-oxides are important in terms of the interface characteristics [30, 42, 68, 69, 72]. From the analysis mentioned above, substantial Ga-oxides obviously form on the surface. As shown in Fig. 2.2 (a), reference binding energy and linewidth for Ga 2p spectra of Ga-As bond can be given through in situ XPS analysis of a thermally decapped InGaAs surface without chemical contamination. It was confirmed that oxidized species or spurious carbon were not detected from the inspection of related spectra [68]. These results can be also obtained from the hydrogen cleaned GaAs samples as well. Subsequent Ga_2O beam exposure on the decapped InGaAs results in different feature of Ga 2p spectra, which is asymmetric and measurably broader, compared to the initial decapped surface [73-75]. At this time As-O and spurious C were not detected.

From the comparison of the Ga 2p spectra between initial decapped surface and Ga_2O exposed surface, it was confirmed that the minimum two additional spectral features were created. The feature at 0.55eV higher binding energy than the bulk peak is therefore due to the Ga 1+ oxidation state, originating from Ga_2O on the surface. In addition, small amount of Ga-Ga bonding originating from the powder source used in this experiment may bring on the slightly detectable feature at ~1116.1 eV. Similar results are obtained for GaAs as well.

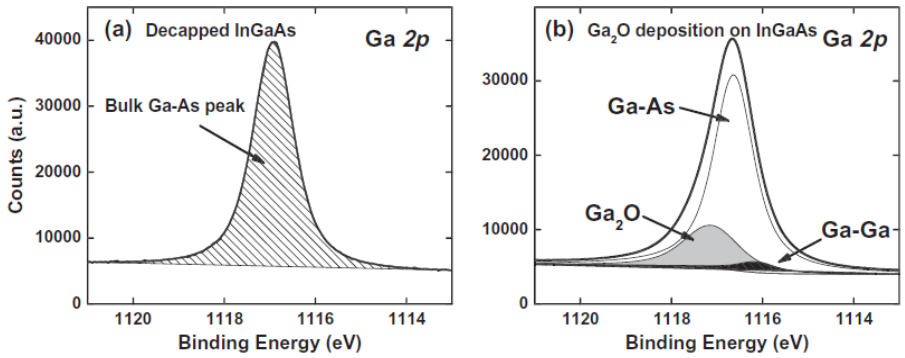


Figure 2.2. (a) Ga 2p XPS spectrum for an As capped $In_{0.53}Ga_{0.47}As$ substrate following thermal desorption of the As cap. (b) Ga 2p XPS spectrum of an $In_{0.53}Ga_{0.47}As$ substrate following decapping and Ga_2O deposition [68, 69].

As described above, higher oxidation states of Ga can be shown for $In_xGa_{(1-x)}As$ surfaces as well. It is generally known that Ga–O bonds are located at the 1–2 eV higher binding energies than the bulk Ga–As peak. After wet cleaning of native oxide using NH_4OH, a large shoulder on the high binding energy side of the bulk peak appears extending above 1 eV from the bulk peak, indicating the existence of another oxidation state of Ga. These spectra can be convoluted by two oxidation states of Ga, the Ga 1+ oxidation state (Ga_2O) and the Ga 3+ oxidation state (Ga_2O_3) as seen in Fig. 2.3 [42, 68, 69, 76]. Since binding energies of the bulk Ga-As peak and Ga 1+ peak were already determined from the experiments of thermally decapped and Ga_2O exposed surfaces, the peak position of Ga 3+ can be derived from the deconvolution of the full spectra of Ga 2p resulting in the binding energy located at 1.2 eV above the bulk peak. For the samples with substantially thick oxides, a higher binding energy state near 1.6 eV above the bulk peak may also appear. Several states including $GaAsO_4$, $Ga(AsO_3)_3$ as well as $Ga(OH)_3$ [67] are possible for this thick sample. These sates are easily removed under chemical treatment. However through the careful analysis of Ga 2p spectra Ga-suboxides (Ga 1+: Ga_2O) are conformed to remain stable on all substrate that have had any exposure to oxygen, hydroxyls, etc. despite of its relatively high (less stable) Gibbs free energy. For example, the HF treated GaAs surface has also Ga 1+ as well as Ga 3+ as shown in Fig. 2.3. The reason for the generation of Ga 1+ cannot be explained by the thermodynamic data of bulk oxides. Since the almost of suboxides are found at the substrate interface [42], the effect from

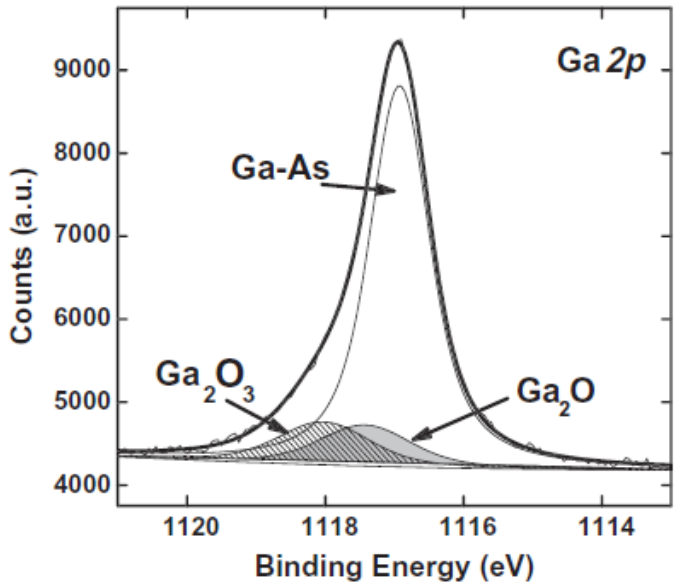


Figure 2.3 XPS core-level spectrum showing the two interfacial oxidation states of Ga. The suboxide is present for any surface exposed to oxygen or hydroxyls [42, 68, 69].

other elements near the interface rather than intrinsic bulk effects are thought to be more dominant. Such suboxides have been characterized by various analysis methods including scanning tunneling microscopy (STM) [73], high-resolution transmission electron microscopy [75], high resolution electron energy loss spectroscopy [77] or XPS [78]. Evaluation of the interfacial effects depending on Ga oxidation states can be regarded as a crucial work to solve the instability of MOS devices.

2.2. Oxide deposition on GaAs by ALD

2.2.1. Precursors and oxidizers for ALD

Various process conditions for ALD oxide deposition including deposition temperature, delivery system, and ALD process cycle are determined by the precursor characteristics such as vapor pressure, decomposition behavior, sticking coefficient and reaction chemistry. If the oxide deposition are subjected under the temperatures less than 400 ℃ and 300 ℃ for GaAs [79] and InAs [80] respectively, desorption of elemental As from the substrate surface would not occur. Thermal instability of III-V substrates could not be caused by ALD process itself.

Two kinds of metal precursors for ALD oxide: metalorganic and inorganic precursors are primarily selected. Halide precursors as the most common inorganic precursors have widely been used in semiconductor industry. Especially $HfCl_4$ is representative Hf halide compound for ALD and CVD HfO_2. Although the halide precursors have highly reactivity and thermal stability even up to 750 ℃, they have the disadvantages such as low vapor pressure or particle generation due to solid phase. ALD HfO_2 films deposited using $HfCl_4$ and water below 300–350 ℃ were known to have high residual impurities such as chlorine and hydrogen [81]. Tri-methyl-aluminum (TMA) as a alkyl precursor, is ideal metalorganic precursors for ALD Al_2O_3

containing direct bonding between the metal ion and carbon. In contrast, alkoxides and amides include oxygen and nitrogen bonding between the metal and alkyl groups, respectively. In general, alkyl precursors are highly volatile and very reactive with water through hydrolysis. On the other hand, they often have the relatively low decompose temperature. For example, decompositions occur at the temperatures higher than 275 ℃ for both TMA and Tetrakis(ethylmethylamido)hafnium (TEMA-Hf) [82, 83]. Thermal stability can be enhanced by the chelation of C (b-diketonates), O (cyclopentadienyls) and N (amidinates) with alkyls to a metal compared to single bond precursors. However they often have low volatility due to their bulky ligands leading low vapor pressure at the deposition temperature.

H_2O is most widely used as a oxygen source resulting in a OH-terminated surface in metal oxide ALD. However long purge time are required due to its high sticking coefficient on the surface. For O_3 as an alternative oxidant, unreacted or physisorbed O_3 is easily removed out of the chamber during purge period leading the enhanced throughput of ALD process. For ALD HfO_2, O_3 was also reported to improve the electrical properties with Tetrakis(dimethylamino)hafnium (TDMA-Hf) on Si and decrease the C contamination in the films [84]. However, there still remain unavoidable risks such as surface oxidation of III-V substrates due to its strong oxidation power which can cause undesirable electrical results. Table 2.2 summarizes representative examples for ALD precursors and oxidants [85].

Table 2.2. ALD precursors and oxidizers studies on $In_xGa_{(1-x)}As$ surfaces [69, 85] .

Dielectric/substrate	Precursor	Vapor pressure [200]			Oxidizer/nitridizer	T_{dep} (°C)	T_{max} (°C)
		20 °C	100 °C	200 °C			
Al_2O_3/*n*-GaAs	$Al(CH_3)_3$ [TMA]	8.6	315	–	H_2O	300	600 O_2
Al_2O_3/*n*-InGaAs	$Al(CH_3)_3$ [TMA]	8.6	315	–	H_2O	300	550 O_2
Al_2O_3/*p*-GaAs	Al(CH3)3 [TMA]	8.6	315	–	$(CH_3)_2CHOH$	400	–
AlN/*n*-, *p*-InGaAs	$Al(N(CH_3)_2)_3$ [TDMA-Al]				NH_3	250	550 N_2
HfO2/*p*-InGaAs	$HfCl_4$	10^{-6}	0.006	5.1	H_2O	320	500 O_2, N_2
HfO_2/*n*-InGaAs	$Hf[NCH_3C_2H_5)_4$ [TEMA-Hf]	0.005	1.7	155	H_2O	200	–
HfO_2/*n*-, *p*-GaAs	$Hf(N(CH_3)_2)_4$ [TDMA-Hf]	0.06	15	1074	H_2O	200	500 N_2
Hf-aluminate/*n*-, *p*-GaAs	$Al(CH_3)_3$	8.6	315	–	H_2O	300	600 N_2
	$HfCl_4$	10^{-6}	0.006	5.1			
La-aluminate/*n*-InGaAs	$Al(CH_3)_3$	8.6	315	–	H_2O	200	–
	$La(^iPrNCHN^iPr)_3$ [($^iPr_2$-fmd)3-La]	0.008	0.06	0.256			

2.2.2. ALD Al_2O_3 and HfO_2 on GaAs

Ye and coworkers firstly reported depletion mode MOSFET using ALD dielectrics directly on GaAs (100) with 8–16 nm thick Al_2O_3 [86, 87]. During the MOSFET process, GaAs substrate met with vacuum break to transfer into the ALD chamber for Al_2O_3 deposition after MBE GaAs growth. GaAs surface exposed to the atmospheric ambient made inevitably thin native oxide layer consisting of Ga- and As-oxides. It should be noted that the native oxide and elemental As on the GaAs surface can be removed during the ALD process using TMA and H_2O remaining a only 0.6 nm Ga oxide interfacial layer. Interface state densities D_{it} ~10^{12}/cm^2 eV were extracted for this gate stack [88].

Frank and coworkers reported a subsequent more detailed study using HfO_2 as well as Al_2O_3 deposition by ALD [62]. It was found that the interfacial layer formed on GaAs surface was significantly affected by the ALD process. Vacuum pre-annealing at 300 ℃ prior to ALD deposition resulted in a only small decrease of the native oxide suggesting that oxide removal on the substrate hardly occur through this annealing, consistent with prior reports. About 2.5 nm thick oxides on GaAs substrate was generally detected for the GaAs surface. Through the comparison of ALD oxides, ~1 nm thick native oxide was observed for Al_2O_3 using TMA/H_2O while a thicker native oxide of ~2-2.5 nm was detected for the HfO_2 using $HfCl_4$/H_2O on either the native oxide or an HF-last surface. Authors suggested that the significantly reduced

interfacial layer from the Al_2O_3 deposition can be attributed to formation of volatile products in the oxides or conversion of the native oxides to Al_2O_3 during the ALD process. The difference in accordance with ALD precursors can be explained by the reactivity of $Al(CH_3)_3$ compared to $HfCl_4$ based upon formation enthalpies.

This self-cleaning effect on interfacial oxide has been also observed by others [62, 89-91]. Dalapati and coworkers studied MOS capacitors using Al_2O_3 (TMA/water), HfO2 ($HfCl_4$/water) and nanolaminating layers by ALD on HCl + $(NH_4)_2S$ treated GaAs (100) surfaces [62]. Frequency dispersion behaviors of capacitance–voltage (C–V) curves were examined with n-GaAs and p-GaAs at room temperature. Since the capacitance of interface state are directly associated with the frequency, measured total capacitance is also dependent on the frequency. The maximum capacitances shown at the accumulation region of C-V curves generally decrease with an increase of the measurement frequency. Recently such behavior has also been reported by others as well utilizing PVD [49] and ALD [39, 92] dielectrics, and the utilization of Si (or Ge) interfacial passivation layers noted above, and/or post-deposition annealing, improves the dispersion problems on GaAs [93].

Dalapati et al. also investigated the chemical nature of the interface using Al_2O_3, HfO_2, and Al_2O_3/HfO_2 nanolaminates [62]. XPS studies revealed that the interfacial oxides consist of Ga- and As-oxides and C-V characteristics can be affected by these interfacial oxides. In addition, they regarded the difference of interfacial oxidation between n- and p-GaAs as dopant-

dependent oxidation process [94, 95] which can result in different C-V behaviors. However, it was reported in recent studies that chemically identical oxide on both n- and p-GaAs was formed and the difference in C-V behaviors was attributed to the capture time constants for electrons and holes rather than any dopant-dependent effects [41].

Results of XPS analysis on GaAs surface can be significantly dependent on the surface passivation process or analysis environment such as in situ or ex situ analysis. As shown in Fig. 2.4, in situ analysis performed on the surface oxides before and after formation of 1 nm thin ALD films indicates that almost of the interfacial oxides can be removed below the detection limit of XPS due to ALD self-cleaning effect depending on the oxidation states and ALD precursors [96]. Especially the surface oxide with higher oxidation states which is weakly bonded are completely removed by wet cleaning such as NH_4OH prior to ALD deposition. In contrast, previous literature also indicates that surface oxide species remain after ALD [62, 97, 98].

The XPS results [30, 69, 96] shown in Fig. 2.4 reveal a reaction mechanism, whereby Al from the TMA preferentially reacts with the As3+ and Ga3+ oxidation states, resulting in bond conversion to Al-oxide. In contrast, the reaction between the 3+ oxidation state and Hf from the TEMA-Hf precursor is less efficient, but the 5+ state is still effective indicating a more complex process. In either case, the weakly bonded oxides may decrease during the ALD process, while the stronger Ga–O bonding, including potential Ga sub-oxide species, can remain at the interface. Therefore it is likely that a

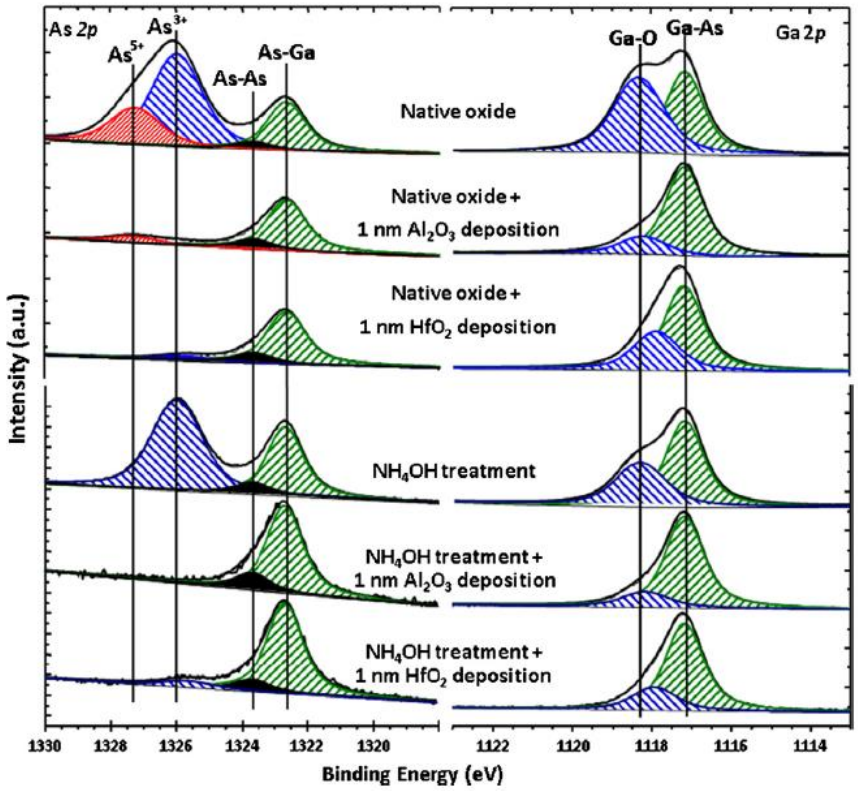


Figure 2.4. XPS of the interfacial reactions after atomic layer deposition of Al_2O_3 and HfO_2. The reactions with the surface oxides exhibit precursor specific and oxidation state-specific behavior [30, 69, 96].

significant portion of interfacial oxidation can be controlled by precursor-mediated reactions, and detrimental electrical results can be induced by the defects from uncontrolled oxidation such as Fermi level pinning and C–V frequency dispersion [99, 100].

Shift of the Ga–O peak in the Ga 2p spectra toward lower binding energy was observed upon ALD film growth in Fig. 2.4. Such chemical shifts can be explained by the M–O–Ga bonding (where M = Al or Hf), the presence of Ga sub-oxides species (such as O–Ga–O; Ga 1+) in addition to Ga 3+ (Ga_2O_3), as well as band bending effects [41, 101].

2.3. Electrical behaviors of III–V MOS devices

2.3.1. Frequency dispersion in C–V measurements

2.3.1.1. Nicollian and Brews model

In III-V semiconductors, maximum capacitances in C-V curves generally vary in accordance with measurement frequency as shown in Fig. 2.5 [69]. This anomalous behavior which is referred to as frequency dispersion is known to be observed in numerous III-V semiconductors [102-104]. In case of GaAs, the dispersion characteristic is more prominent in n-type GaAs compared to p-type GaAs MOS capacitors. For $In_xGa_{1-x}As$, the effect is intimately dependent on the Indium concentration showing the strong dispersions for low Indium contents and weak dispersions or even no dispersions for x = 0.53 and above.

In general, frequency dispersion can be induced by the high series resistance or high density of interface states. For series resistance, contact resistance, substrate bulk resistance and measurement cable resistance are the possible causes for frequency dispersion [105]. However, because the typical value of series resistance obtained by dielectric breakdown method is approximately 20 Ω, strong dispersion behavior measured in GaAs MOS capacitors cannot be explained by only this series resistance. According to

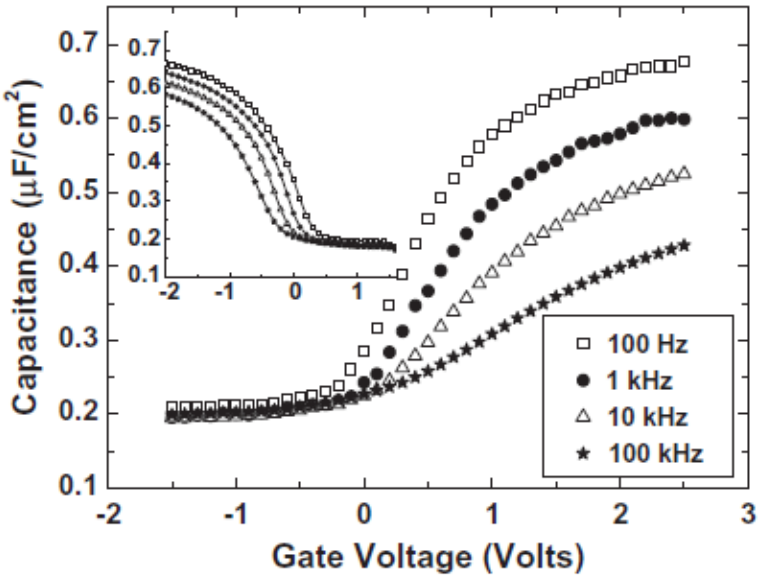


Figure 2.5. Commonly observed frequency dispersion in accumulation for TaN/Al_2O_3 stack on both n- and p-type (inset) GaAs MOS capacitor structures [69].

previous numerous researches, it was reported that this frequency dispersion is primarily attributed to a high density of interface states on III-V semiconductors [29, 102, 104, 106-108]. In Fig. 2.6, n-GaAs C–V characteristics were modeled including classical interface state capacitance corresponding to an extremely high interface state density of 1 x 10^{13} $cm^{-2}eV^{-1}$ uniformly distributed in band gap [109]. Simulation of C–V characteristics was performed using a classical model of the total semiconductor charge. Using the surface potential from this solution, the capacitance associated with interface states (C_{it}), averaged over band bending, and for a p-type substrate, was calculated numerically as a function of frequency [110].

$$C_{it} = \frac{qD_{it}(2\pi\sigma_s^2)^{-1/2}}{2\omega\tau_p}\int_{-\infty}^{\infty}\exp\left(\frac{-\upsilon^2}{2\sigma_s^2}\right)\exp(-\upsilon)\tan^{-1}\left(2\omega\tau_p\exp(\upsilon)\right)d\upsilon \quad (2.2)$$

$$\tau_p = \frac{1}{\bar{v}\sigma_p p_s} \quad (2.3)$$

where σ_s^2 is the variance of band bending in units of kT/q, ω is the measurement frequency in radians, τ_p is the characteristic capture time constant for holes, υ is band bending, $\bar{v}$ is the thermal velocity of the carriers (typically 10^7 cm/s in silicon at room temperature), σ_p is the capture cross-section for holes, and p_s is the density of free holes at the substrate surface. The total capacitance (C_{tot}) for the MOS capacitor at a given gate voltage (V_g) is then obtained using

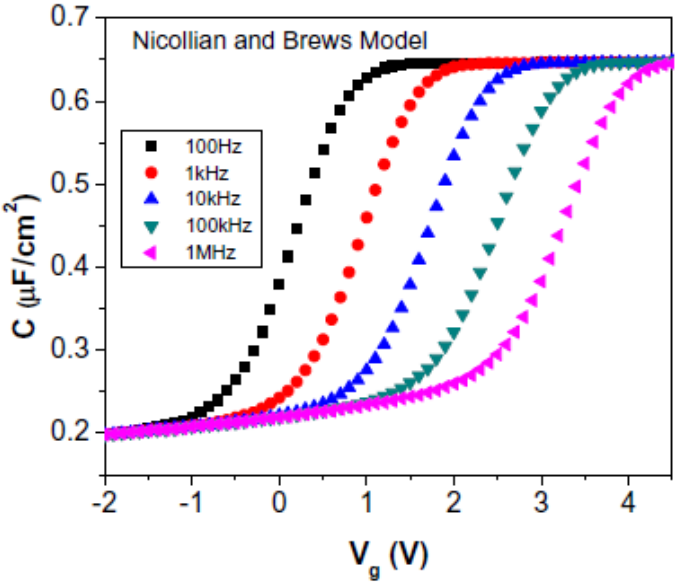


Figure 2.6. Modeled GaAs C-V characteristics including classical interface states capacitance [39].

$$C_{tot} = \left[(C_{it} + C_{sub})^{-1} + C_{ox}^{-1}\right]^{-1}. \quad (2.4)$$

The calculated results indicate a frequency-dependent kink in the depletion region of the C-V curve, which is similar to that of silicon but quite different with that of GaAs. In accumulation, since the free electron density (n_s) at the semiconductor surface is enough large indicating small trapping time constant according to above Eq. (2.3), all of the interface states can respond to the measurement frequencies and C_{it} is approximately equal to qD_{it}. Approaching toward strong depletion, n_s exponentially decrease resulting in very large τ_n. Therefore, interface trap cannot respond with measurement frequencies and C_{it} approaches zero. In the gate bias range between strong accumulation and strong depletion, only limited interface traps respond to the frequencies. In this case, the value of C_{it} is between qD_{it} and zero. The classical interface state capacitance cannot reproduce the measured behavior of many compound semiconductors [111].

2.3.1.2. Hasegawa and Sawada model

The frequency dispersion behaviors observed in III-V semiconductors well coincide with a model developed by Hasegawa and Sawada[103, 104, 107]. According to the classical theory of interface state capacitance, only defects on the interface not in the bulk dielectric can respond to the AC signal during the C-V measurement. However, Deep Level Transient Spectroscopy (DLTS) measurements of interface states performed by Hasegawa and Sawada indicated that the measured trapping time constants did not consistent with the value predicted from the classical assumption. From the trapping time constants extracted by DLTS, it was suggested that an interfacial region located at 0.33 eV lower level than conduction band minimum of GaAs is associated with a thin disordered interfacial layer at the interface and the related disorder-induced gap states (DIGS) where the defects are distributed in both energy and space. Hasegawa and Sawada found that assumption that the distribution of trap into the dielectric is subject to exponential decay satisfying the below equation can explain the dispersion observed in III-V semiconductor.

$$N_T(x) = N_{TO} \exp(-\alpha x) \tag{2.5}$$

where $N_T(x)$ is the trap density as a function of position and α is the decay constant. Assuming tunneling into these defects [112], the following

relationship was obtained for the interface state capacitance:

$$C_{it} = \frac{q^2 N_{TO}}{2\kappa_0}(\omega\tau_0)^{(\frac{\alpha}{2\kappa_0})} \int_0^{1/\omega\tau_0} z^{(\frac{\alpha}{2\kappa_0})} \tan^{-1}(z^{-1})dz \qquad (2.6)$$

assuming, $\tau(x) = \tau_0 \exp(2\kappa_0 x)$ where κ_0 is the quantum–mechanical decay constant of electron wave function, and τ_0 is the time constant of the trap located at the interface. In Fig. 2.7, total capacitance considering interface state capacitance simulated by means of Hasegawa and Sawada model are given with both n-type and p-type GaAs MOS capacitor, indicating good agreement with the real C-V behavior depending on frequency as shown in the Fig.2.5 [113]. The difference of the dispersions between n-type and p-type GaAs is primarily originated from the difference in trapping time constants for n-type vs. p-type and the energy distribution of interface states [41].

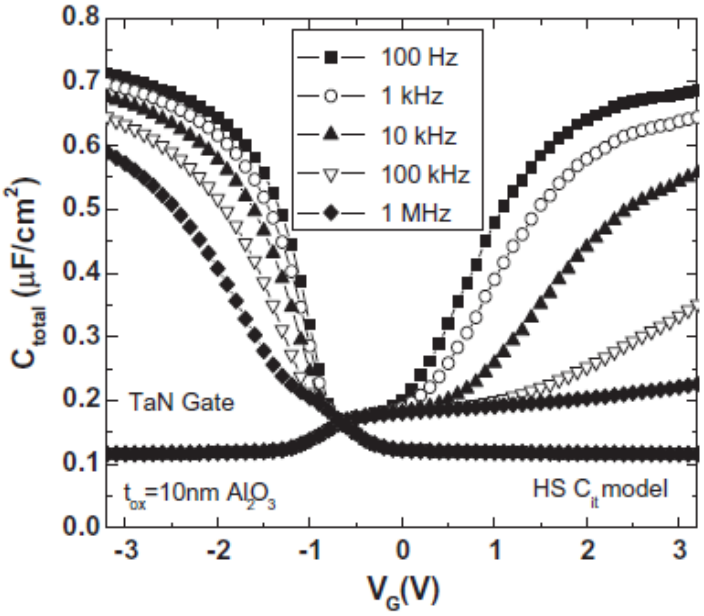


Figure 2.7. Simulated C-V characteristics of MOS capacitors on both n-type and p-type GaAs using the Hasegawa-Sawada C_{it} model [113].

2.3.2. Hysteresis in C–V measurements

Fig. 2.8 shows band diagram of a typical MOS structure [114], where a certain gate voltage (V_g) is applied between the metal and the semiconductor, leading the band bending of semiconductor characterized as surface potential. Distribution of interface state at the semiconductor–oxide interface is also described in the band diagram. When small AC signal with frequency f and amplitude of several tens of mV superposed on DC bias is applied on gate metal electrode to measure the capacitance as a function of gate voltage, energy bands of the semiconductor move up and down having the same period with AC signal, leading repetitive variation of surface potential. This variation can make the interface states located near the Fermi level filled and emptied. Only if the interface traps placed around the Fermi level have a characteristic response time that is of the order of the measurement frequency f, they can interact with the measurement AC signal and play a role as interface states capacitance. As described in the previous chapter, this capacitance can finally affect the total capacitance of the MOS capacitor depending on measurement frequency.

The characteristic time τ_e which it takes for trapped charge to emit from the trapped level E_t in a semiconductor interface can be calculated from standard Fermi–Dirac statistics and is given by [114, 115]

$$\tau_e = \tau_t \exp(\Delta E/kT) \tag{2.7}$$

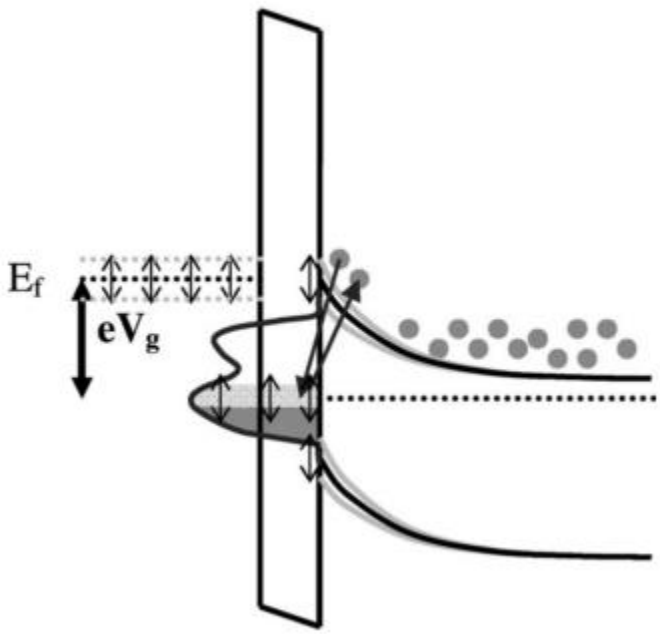


Figure 2.8. Band diagram of an n-type MOS structure with a bias voltage V_g applied between metal and semiconductor [114].

where ΔE is the energy difference between the majority carrier band-edge energy and the trapping state energy E_t, k is the Boltzmann constant, T is the semiconductor temperature, and τ_t is the charge carrier trapping time constant, given by

$$\tau_t^{-1} = \sigma v_t N \tag{2.8}$$

here σ is the capture cross section of the trapping state, v_t is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. (Equation (2.3) is a p-type form of equation (2.9).) From this characteristic emission time τ_e, the characteristic response frequency of the corresponding trapping state can be extracted using the equation of $f_e = 1/2\pi\tau_e$. This equation reveals that the characteristic emission frequency correlates exponentially with the depth of trapping level in the band gap. As the distance of the trap level from the band edge increases, emission of trapped charge occurs very slowly due to exponential term.

During sweeping the gate bias voltage, Fermi level moves through the band gap. When the characteristic response frequency at a certain position of Fermi level in the band gap become equal to the measurement frequency, this trap lied at the specific Fermi level can react with the outer signal and the capacitance and resistance can be measured by the C-V equipment. From this measurement, information on interface state density as a function of trap level in the band gap can be derived. In Fig. 2.9, the characteristic emission

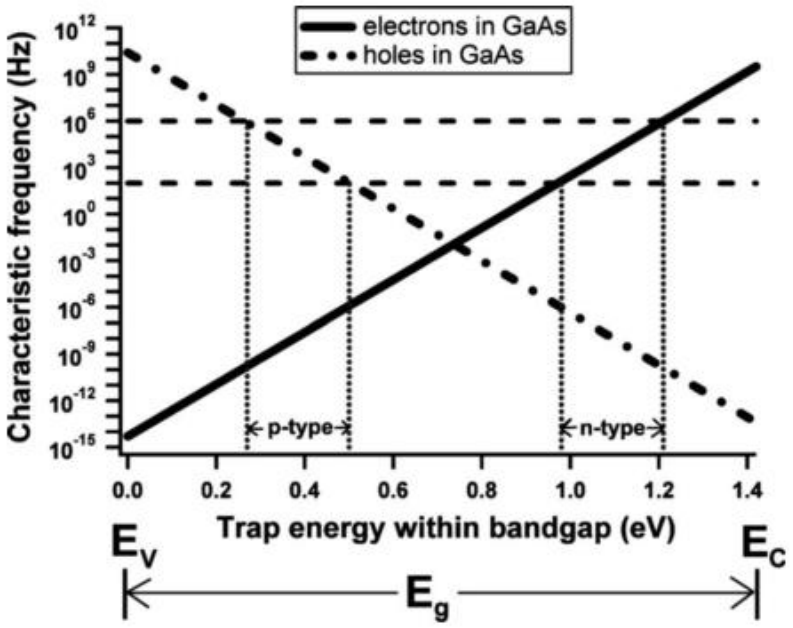


Figure 2.9. Characteristics emission frequencies of trapped charge in GaAs at room temperature [114, 115].

frequency of traps in GaAs as a function of the position of the trap in the band gap is shown. It is noted that only small portions of the band gap can be accessed using typical range of measurement frequency of 100 Hz to 1 MHz, because of the large band gap of GaAs. The mid-gap interface states cannot be probed by usual measurement conditions, neither on p-type nor on n-type MOS capacitors. These mid-gap traps have extremely small characteristic frequencies on the order of 10^{-3} s^{-1} corresponding to characteristic times of the order of 1000 s [59, 114, 115]. Once a charge carrier is trapped in such a mid-gap trap it takes long time extending several tens of minutes to hours to emit from the deep trap. Since these extremely slow traps cannot be accessed using usual measurement frequency of 100 Hz to 1 MHz, trap density at these positions in the band gap are completely veiled. They might just eventually induce the C-V hysteresis which can occur when the trapped charge carriers stay for long time and emit very slowly from such deep interface trap.

2.3.3. Temperature dependence of trap response

There are two solutions to measure the slow mid-gap states. One is extremely low frequency method such as quasi-static C-V which is slow enough to access the deep trap [116]. Another solution is high temperature method which enables the trapped charges at the deep states to be emitted as fast as they can respond with even usual measurement frequency as expected from the exponential term of equation (2.7) [114, 115]. At elevated temperature, even deep level states have reasonable value of characteristic emission time which is measurable using conventional equipment [114, 115, 117]. Fig. 2.10 shows the characteristic emission frequencies as a function of trap energy in the band gap of GaAs at a substrate temperature of 150 ℃, assuming a typical capture cross section of 10^{-14} cm^2. The characteristic emission frequencies at 150 ℃ become 4 orders of magnitude larger than at room temperature, which can measure the mid-gap states using frequencies of the order of 100 Hz. Therefore application of conductance method at room temperature as well as at elevated temperatures up to 150 ℃ enables extraction of interface states distribution over most GaAs band gap.

Fig. 2.11 shows capacitance (C_m) and conductance ($G_p/A\omega q$) as a function of gate bias and frequency respectively for the GaAs/Al_2O_3 samples [114]. To extract the interface states over wide range of band gap, 25 and 150 ℃ measurements were performed on both n- and p-type MOS capacitors. Every one of the four measurements probes a different energy region in the GaAs

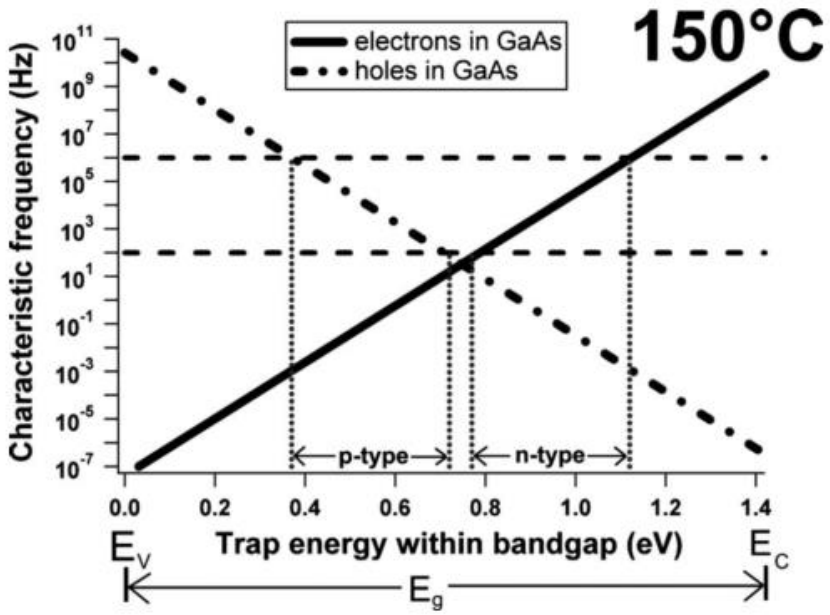


Figure 2.10. Characteristic emission frequencies of trapped charge carriers in GaAs at 150℃. The emission time for electrons (solid line) and holes (dashed-dotted line) is shown [114, 115].

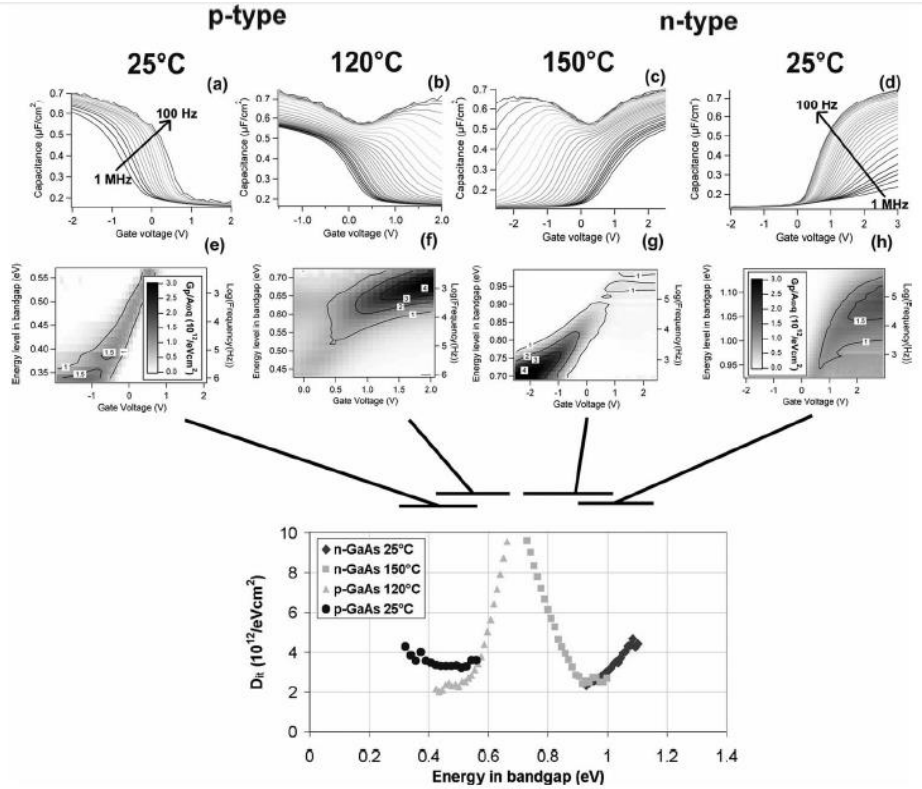


Figure 2.11. Capacitance- and conductance- voltage measurements on 200um diameter GaAs/Al_2O_3 MOS capacitors at 25℃ and 150℃ for n-type GaAs and at 25℃ and 120℃ for p-type GaAs [114].

band gap. Densities of interface states measured at room temperature show about ~10^{12} $cm^{-2}eV^{-1}$ on both n- and p-type GaAs corresponding to upper and lower half band gap respectively. However high-temperature measurements up to 150 ℃ show a very rapid increase of density of interface states toward the mid-gap from the each band edges, leading the interface states more than 10^{13} $cm^{-2}eV^{-1}$. These huge interface states can affect the Fermi level movement [118-120]. Especially passing of Fermi level through this mid-gap point is effectively suppressed. Since the existence of these high densities of interface states can even induce the Fermi level pinning, we faced the serious problem that surface potential cannot be easily modulated by a gate bias for GaAs MOS devices.

2.3.4. Conductance method for D_{it} extraction

The conductance method, proposed by Nicollian and Goetzberger [121], has the advantages of high sensitivity and relative simplicity to extract the interface states compared to other methods. Especially conductance method has been widely employed for III-V semiconductors with only MOS structure. In conductance method, D_{it} can be determined from the measured capacitance and conductance of the structure under testing [43, 110, 121-123]. Total MOS structure including the interface states can be depicted as the feature like Fig. 2.12 (c), showing the contributions from the oxide capacitance (C_{ox}), the capacitance of the depletion region (C_d), the capacitances ($C_{it,i}$), and resistances ($R_{it,i}$) of the interface states of time constant $R_{it,i}C_{it,i}$, as well as the series resistance (R_s). Simplified equivalent circuit of this MOS structure is shown in Fig. 2.12 (b). Therefore parallel capacitance (C_p) and conductance (G_p) in this circuit contain information related with interface states through C_{it} and R_{it}. Fig. 2.12 (a) shows final equivalent circuit of MOS capacitor assumed at the measurement equipment described using capacitance C_m and conductance G_m.

From the measured capacitance C_m and conductance G_m, one can extract the density of the interface states. Firstly, using equivalent relation of total impedances between two circuits shown in the Fig. 2.12 (a) and (b), conversion from measured value of G_m and C_m to G_p can be derived as the following equation [110],

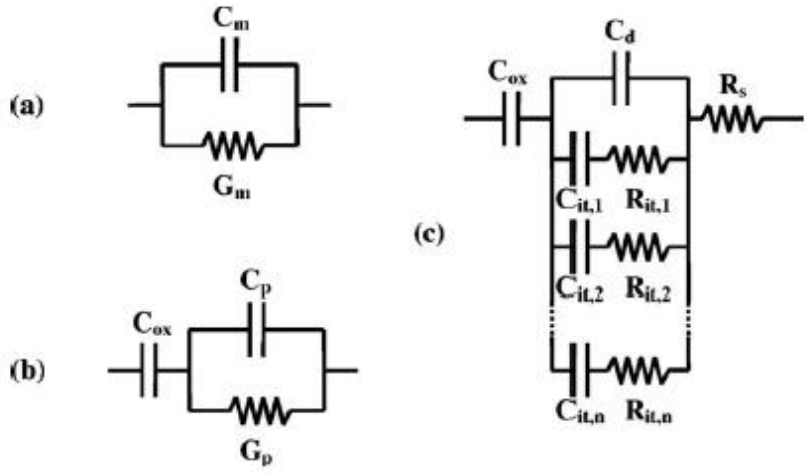


Figure 2.12. (a) Equivalent circuit of the capacitance (Cm) and parrallel conductance (G_m) measured by the experimental equipment. (b) Equivalent circuit showing the oxide capacitance (C_{ox}) and the substrate capacitance (C_p) and parallel substrate conductance (G_p), (c) Equivalent circuit of the total MOS structure, showing the oxide capacitance , the depletion capacitance (C_d), the series resistance (R_s), and the interface state capacitance ($C_{it,i}$) and the resistance ($R_{it,i}$) [114].

$$G_p = \frac{G_m}{(G_m/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2} \tag{2.9}$$

Second step is the extraction of D_{it} from G_p which is correlated with C_{it} and R_{it} as shown in the Fig. 2.12 (b) and (c). Using the equivalent relation, we can obtain the D_{it} which is linearly proportional to the peak value of a conductance G_p/ω as a function of measured frequency f as following equation [110].

$$D_{it}(V_g) \approx 2.5 \frac{(G_p)_{max}}{A\omega q} \tag{2.10}$$

Here A is the area of the MOS capacitor under testing, $\omega = 2\pi f$, and q is the charge of the majority charge carrier. Maximum value of G_p/ω occurs when the measured frequency is equal to the characteristic emission frequency of the interface states located at a certain energy level in the band gap, which is determine by a given gate bias. As sweeping the gate bias, we can determine energy distribution of D_{it} showing the interface states as a function of the trap energy level.

2.4. Surface passivation of III-V semiconductors

2.4.1. $Ga_2O_3(Gd_2O_3)$ gate dielectric

Hong and coworkers reported $Ga_2O_3(Gd_2O_3)$ (GGO) grown by MBE on GaAs [45]. In this work, capability of the $Ga_2O_3(Gd_2O_3)$ deposition processes to provide improved interface qualities between oxide and GaAs was demonstrated. Ex situ process which includes thermal desorption of native oxides of GaAs and subsequent $Ga_2O_3(Gd_2O_3)$ deposition on GaAs showed low surface recombination velocity S of 9000 cm/s corresponding to D_{it} of 10^{10} $cm^{-2}eV^{-1}$ indicating excellent interfacial characteristics.

Systemaic study in terms of the composition of Gd was carried out by Kwo et al [46]. Dependence of dielectric properties of $(Ga_2O_3)_{1-x}(Gd_2O_3)_x$ on the Gd (x) content exhibits best passivation effect when x exceeds 14%. Low leakage current and low density of interface states could be obtained in films with $x \geq 14\%$.

Shiu et al. investigated 1 nm thin passivation layer of $Ga_2O_3(Gd_2O_3)$ on $In_{0.2}Ga_{0.8}As$ [47]. Dielectric films comprising Al_2O_3/GGO revealed atomically sharp smooth interface even after high temperature annealing up to 850 ℃. Weak frequency dispersion and low density of interface states in the low 10^{11} $cm^{-2}eV^{-1}$ could be attained as shown in Fig. 2.13.

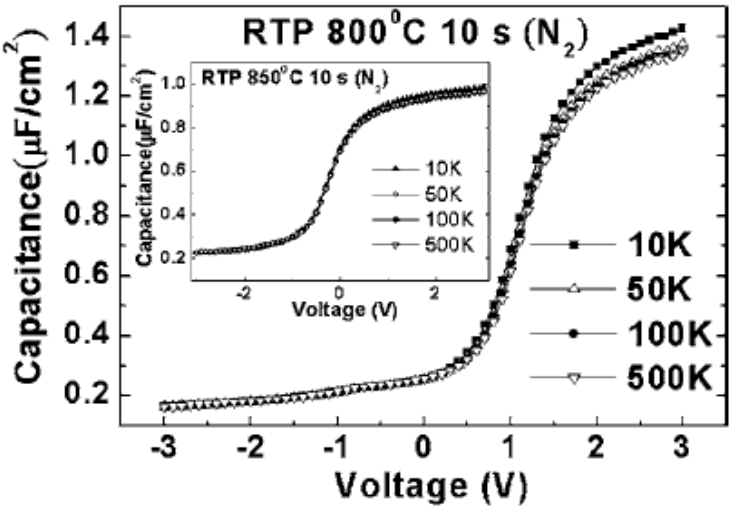


Figure 2.13. C-V characteristics for an Al_2O_3(3nm)/GGO(4.5nm)/ $In_{0.2}Ga_{0.8}As$/GaAs MOS diode RTA to 800℃ with the Au gate deposited afterwards [47].

2.4.2. Si interface passivation layer

Koveshnikov and coworkers reported the electrical properties of MOS capacitors including in situ passivated with ultrathin amorphous Si (a-Si) layer and with ex situ deposited HfO_2 gate oxide and TaN metal gate on molecular beam epitaxial GaAs [49]. In situ encapsulation of GaAs surface with an amorphous Si resulted in low stretch-out and frequency dispersion in C-V curves, indicating good interfacial properties. In addition, low leakage current densities of <1.0 mA/cm^2 with equivalent oxide thickness of 2.1 nm was also obtained. As shown in Fig. 2.14, minimum thickness of the Si interface passivation layer of 1.5 nm is required to avoid the Fermi level pinning. From transmission electron microscopy analysis, it was revealed that the Si layer was oxidized up to 1.4 nm during ex situ processing while the interface between the GaAs and a-Si remained atomically sharp without any interfacial reaction.

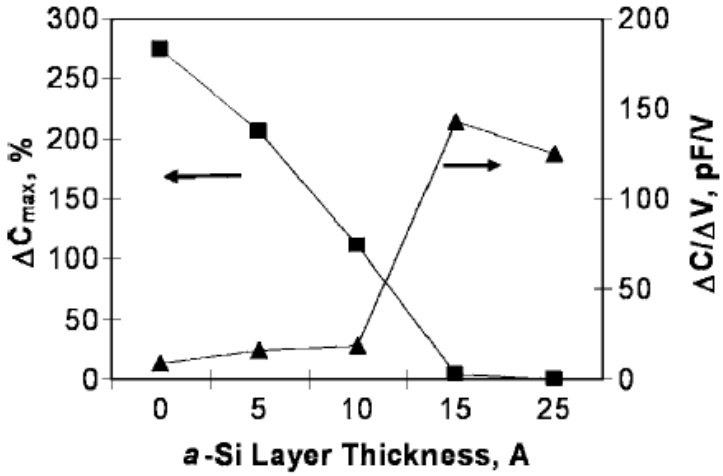


Figure 2.14. Dependence of C-V stretch-out and frequency dispersion on the Si interface passivation layer thickness. The ΔC_{max} value is normalized to the accumulation capacitance at 1 MHz. The C-V slope is measured at $C(V_{fb})$ and $C(V_{fb} + 0.3\ V)$ [49].

2.4.3. Sulfur passivation

First sulfur passivation was performed by Sandroff and coworkers using $Na_2S \cdot 9H_2O$ [53]. They reported that significant current gain with a factor of sixty in GaAs/AlGaAs heterostructure bipolar junction transistor could be achieved by spin coating thin films of $Na_2S \cdot 9H_2O$. That passivation mechanism was explained by two step process, comprising removal of native oxide or elemental arsenic and strong sulfur bonding to exposed surface resulting in stable sulfur compound such as GaS and As_2S_3.

Carpenter et al. reported the effect of $(NH_4)_2S$ treatment on surface passivation in GaAs schottky contact [54]. While not-treated sample showed Fermi level pinning leading same schottky barrier regardless of metal work function, $(NH_4)_2S$ surface treatment resulted in a reduced Fermi level pinning and hence the barrier height could be modulated by the metal work function.

O'Connor presented the effectiveness of $(NH_4)_2S$ concentrations in the passivation of n-type and p-type $In_{0.53}Ga_{0.47}As$ MOS capacitors as shown in Fig. 2.15 [60, 124]. Samples were immersed in aqueous $(NH_4)_2S$ solutions of concentrations 22%, 10%, 5%, or 1% for 20 min at 295 K. Lowest frequency dispersion was obtained in 10% conditions (Fig.2. 15 (b)). Extraction of interface state density were also performed for the optimum 10% $(NH_4)_2S$ passivated $In_{0.53}Ga_{0.47}As$ devices, showing D_{it} of ~2.5 x 10^{12} cm^{-2} with the peak density positioned in the middle of the $In_{0.53}Ga_{0.47}As$ band gap at approximately 0.37 eV (±0.03 eV) from the valence band edge.

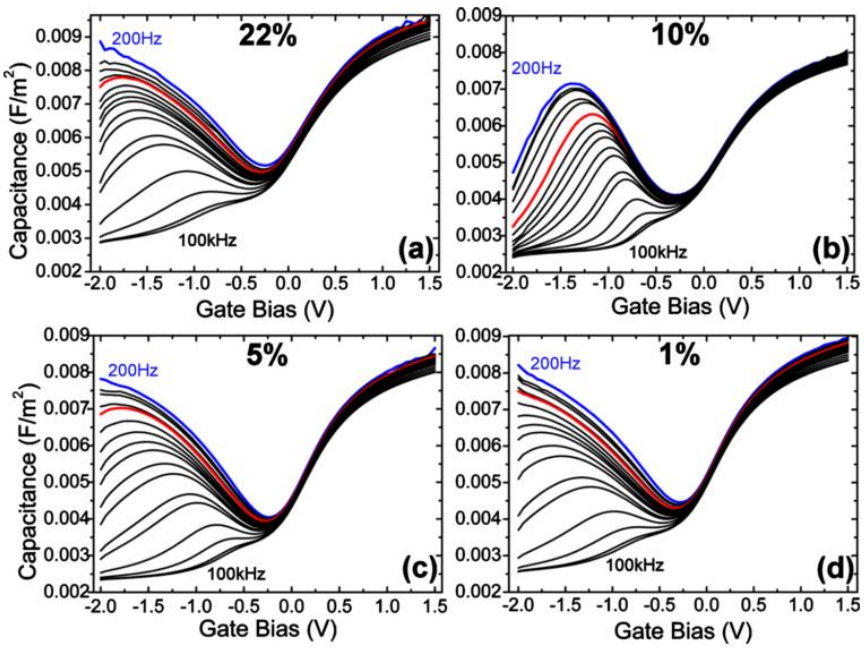


Figure 2.15. Room temperature C-V frequency variation (200 Hz to 100 kHz) of (a) 22%, (b) 10%, (c) 5%, and (d) 1%, $(NH_4)_2S$ treated, Au/Ni/~8nm Al_2O_3/n-$In_{0.53}GaAs_{0.47}$/InP devices [60].

2.4.4. Hydrogen annealing

Kim et al. presented charge trapping defects in Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors and their passivation by hydrogen annealing [125]. In this study, it was found that the trapping in Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ at accumulation occur at not interface traps but border traps in the Al_2O_3 layer near interface, judged from experimental observation such as temperature independent capacitance. The reason is because tunneling of charges into border traps is affected by only frequency while the trapping and detrapping of interface states is dependent on temperature. Hydrogen annealing at 400 ℃ shows suppression of frequency dispersion in accumulation and reduction of C-V stretch-out through depletion as shown in Fig. 2.16. Therefore these results indicate that the hydrogen annealing effectively passivates these border traps in the oxides and some, but not all, Al_2O_3/InGaAs interface states corresponding to depletion region.

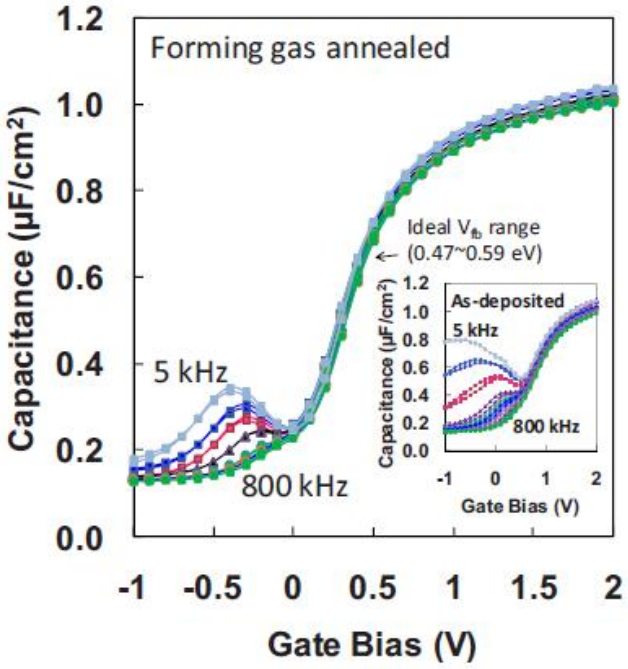


Figure 2.16. The C-V characteristics of forming gas annealed $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$, measured at room temperature. The inset shows C-V characteristics of the as-grown $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ measured at room temperature [125].

3. Experiments and Analysis

3.1. Experimental procedures for sample preparations

3.1.1. Fabrication of MOS capacitors with different dielectric materials

2 inch n- and p-type GaAs wafers doped with Si concentration of 7.1 x 10^{17} cm^{-3} and Zn concentration of 6.7 x 10^{17} cm^{-3}were used for fabrication of GaAs MOS capacitors, respectively. After the dicing of GaAs wafers into ~1cm length, pre-cleaning prior to gate oxide deposition were performed by dipping diluted HF solution of 1.75% concentration. Each piece of GaAs sample is transferred to the deposition chamber within few minutes to prevent the formation of natural oxide on GaAs.

For fabrication of MOS capacitors, 7nm thick Al_2O_3, HfO_2, La_2O_3, and SiO_2 films were deposited on cleaned GaAs at 310 ℃ using a traveling-wave type thermal ALD chamber as depicted in Fig. 3.1. Trimethylaluminium ($Al(CH_3)_3$, TMA), tris(dimethylamino)silane ($SiH[N(CH_3)_2]_3$, TDMAS), Tris[bis (trimethylsilyl)amino]lanthanum ($La[N(Si(CH_3)_3)_2]_3$), and tetrakis (ethylmethylamino)hafnium ($Hf[N(C_2H_5)(CH_3)]_4$, TEMAHf) were used as the metal precursors for Al, Si, La, and Hf respectively. Bubbling system for Al, Hf, and Si and liquid delivery system for La were employed. O_3 of 110 g/Nm^3

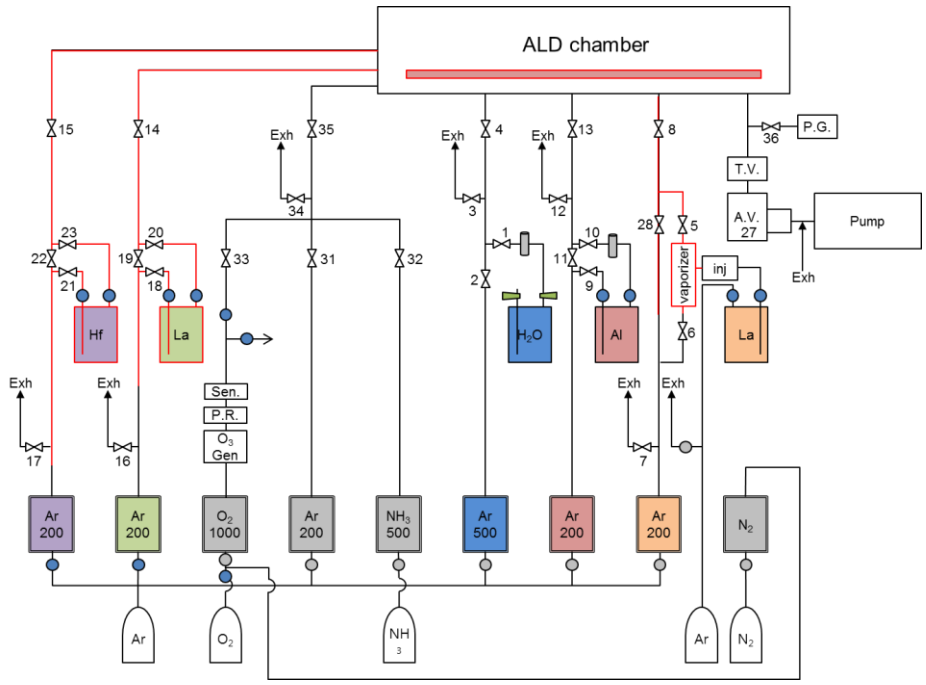


Figure 3.1. Schematic configuration of thermal ALD equipment employed in these experiments. Red line indicates heating zone.

was used as a oxidant for each oxide. Detailed conditions for ALD depositions are listed in Table 3.1. The thicknesses of oxides were measured by a spectroscopic ellipsometry. Post deposition annealing was carried out at 550 ℃ in N_2 ambient during 30 seconds.

Platinum film, as the metal electrode of the MOS capacitor, was deposited by electron beam evaporation through shadow mask with area of 6.6 x 10^4 μm^2 placed on each sample to form patterned gate electrode. Indium paste was used as the backside body contact. Process flow employed in chapter 4.1.2 and 4.2.1 is schematically illustrated in Fig. 3.2.

For the evaluation of double stacked dielectric layer which will be discussed in chapter 4.2.2, MOS capacitors with the structures of Pt/HfO_2(5nm)/SiO_2(2nm)/GaAs and Pt/SiO_2(5nm)/HfO_2(2nm)/GaAs were prepared. For both capacitors, total dielectric thickness including HfO_2 and SiO_2 were 7nm, which were identical with single gate oxide mentioned above. All other process conditions for fabrication of MOS capacitor are also same with the previous single gate oxide MOS capacitors. Fig. 3.3 shows the process flow for the MOS capacitors in detail.

In case of the evaluation of Ga_2O_3 insertion in chapter 4.2.3, 3nm thick Ga_2O_3 and 4nm thick Al_2O_3 were sequentially grown on the HF cleaned GaAs substrate by ALD using trimethylGallium (TMG) and trimethylAluminum (TMA), respectively. For a control sample, MOS capacitor using only the 7nm thick Al_2O_3 gate dielectric was also prepared. Total thickness of Al_2O_3 on Ga_2O_3 is same with single Al_2O_3 layer. of 7nm. Following processes

Table 3.1. Deposition conditions of thermal ALD in detail.

Substrate	GaAs (N-, P-type)			
Deposition	Al_2O_3	SiO_2	La_2O_3	HfO_2
Precursors	TMA	TDMAS	$La[N(SiMe_3)_2]_3$	TEMAHf
Source temp	RT	RT	160°C	85°C
Source supply	Bubbling	Bubbling	LDS	Bubbling
Oxidant	Ozone, H_2O			
Substrate temp	310°C			
Wall temp	125°C			
Carrier Ar flow	200sccm			
Purge Ar flow	200sccm			

Process flow in chapter 4.1.2 and 4.2.1

Substrate: N-, P- GaAs (Si 7.1x10^{17}/cm^3, Zn 6.7x10^{17}/cm^3)

- **HF cleaning (10s x 5)**
- **ALD oxide deposition (310°C, 7nm)**
  : Al_2O_3 (TMA); SiO_2 (TDMAS); La_2O_3 ($La(N(SiMe_3)_2)_3$); HfO_2 (TEMAH)
- **Post deposition annealing**
  : 700°C, N_2 ambient
- **Pt evaporation** (through shadow mask 66000um2)
- **In backside contact**
- **Analysis**
  : Electrical : C-V hysteresis, frequency dispersion, D_{it}
  : Chemical : XPS, AES (w/o Pt, In)

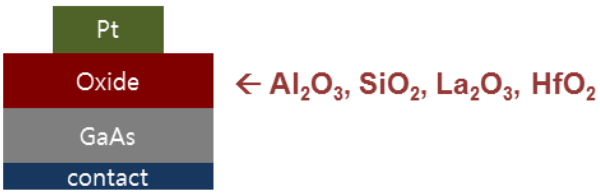
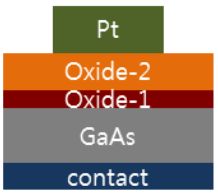


Figure 3.2. Process flow for GaAs MOS capacitors using Al_2O_3, SiO_2, La_2O_3 and HfO_2.

Process flow in chapter 4.2.2

Substrate: N-type GaAs (Si doped $7.1 \times 10^{17}/cm^3$, 2 inch)

- **HF cleaning (10s x 5)**
- **ALD oxide deposition (310°C, 2, 5nm)**
  : HfO_2 (5nm) on SiO_2 (2nm)
  SiO_2 (5nm) on HfO_2 (2nm)
- **Post deposition annealing**
  : 700°C, N_2 ambient
- **Pt evaporation**
- **In backside contact**
- **Analysis**
  : Electrical : C-V hysteresis, frequency dispersion



← **HfO_2 on SiO_2, SiO_2 on HfO_2**

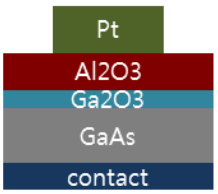
Figure 3.3. Process flow for GaAs MOS capacitors with double stacked layers: HfO_2 on SiO_2 and SiO_2 on HfO_2.

including PDA, Pt electrode formation, and In backside contact were performed in the same way. In Fig. 3.4, the full process of the MOS capacitors is also shown.

Process flow in chapter 4.2.3

Substrate: N-type GaAs (Si doped 7.1x10^{17}/cm^3, 2 inch)

- **HF cleaning (10s x 5)**
- **ALD oxide deposition (310°C, 7nm)**
  : Ga_2O_3(TMG), Al_2O_3 (TMA)
  → Al_2O_3 (4nm) on Ga_2O_3 (3nm) vs Al_2O_3 (7nm)
- **Post deposition annealing**
  : 700°C, N_2 ambient
- **Pt evaporation**
- **In backside contact**
- **Analysis**
  : Electrical : C-V hysteresis, frequency dispersion, D_{it}
  : Chemical : XPS, AES (w/o Pt, In)



← **Ga_2O_3 insertion at GaAs interface**

Figure 3.4. Process flow for GaAs MOS capacitors with and without Ga_2O_3 interfacial layer.

3.1.2. Fabrication of MOS capacitors using HPO passivated GaAs

Si doped n-type and Zn doped p-type GaAs wafers with a same concentration as mentioned above were used as substrates for the fabrication of GaAs MOS capacitors. The GaAs samples were cleaned sequentially with acetone, methanol and isopropyl alcohol, followed by diluted HF etching to remove the native oxide. Before depositing the gate dielectric film, the GaAs substrate was oxidized thermally under high pressure oxygen ambient of 10 atm for 30 min at 400 °C. Fig. 3.5 shows the equipment for high pressure annealing. Thermally-grown 20-nm-thick gallium oxide was removed completely by 10:1 diluted HF etching, which is referred to as HPO. For the control GaAs sample high pressure oxidation and subsequent HF etching steps were skipped. The GaAs substrates were transferred to the vacuum chamber for ALD within a few minutes after HF etching.

To examine the oxidation effects depending on the pressure and the temperature, two different conditions were employed firstly: 1 atm and 400 ℃ named as APO (refer to atmospheric pressure oxidation) and 1atm and 600 ℃ named as HTO (refer to high temperature oxidation). Next various oxidation conditions changing the temperature and time between APO and HTO were also evaluated. Sufficient HF etchings to remove the grown gallium oxides were subsequently performed.

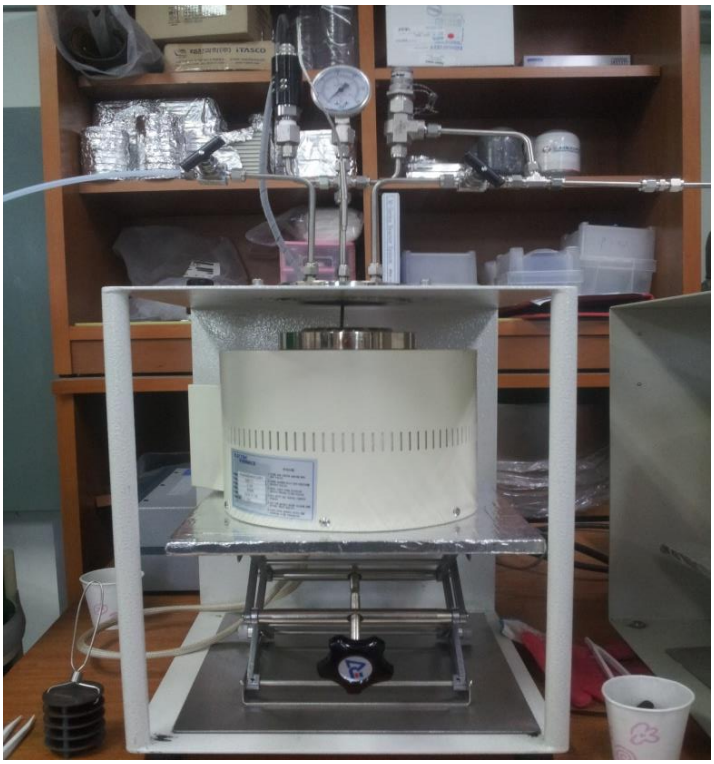


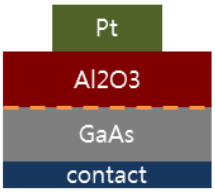
Figure 3.5. High pressure oxidation equipment employed in this study.

Al_2O_3 films, as a gate dielectric, were deposited by ALD using trimethylaluminum (TMA) and H_2O as the aluminum and oxygen sources, respectively. The 6 nm and 2 nm-thick Al_2O_3 films were prepared for electrical characterization of MOS capacitors and XPS analysis, respectively. Post deposition annealing (PDA) was performed at 550°C in N_2 ambient. A platinum (Pt) film and indium (In) were used as the metal electrode and body contact, respectively. Full process flows are summarized in Fig. 3.6.

Process flow in chapter 4.3

Substrate: N-, P- GaAs (Si $7.1 \times 10^{17}/cm^3$, Zn $6.7 \times 10^{17}/cm^3$)

- **Pre-clean : DHF cleaning (10s x 5)**
- **Thermal oxidation**
  - HPO : 10atm, 400°C, 30m
  - APO : 1atm, 400°C, 30m, HTO : 1atm, 600°C, 30m
- **Wet etching : DHF**
- **ALD oxide deposition (310°C, 7nm)**
  : Al_2O_3 (TMA)
- **Post deposition annealing**
  : 550°C, N_2 ambient
- **Pt evaporation**
- **In backside contact**
- **Analysis**
  : Electrical : C-V hysteresis, frequency dispersion, D_{it}
  : Chemical : XPS, AES (w/o Pt, In), TEM



← Surface passivation by HPO

Figure 3.6. Process flow for GaAs MOS capacitors with HPO passivation.

3.1.3. Fabrication of MOS capacitors using Ti scavenging effect

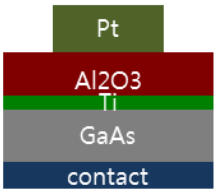
To evaluate Ti scavenging effect, insertion of thin Ti film at the gate oxide-GaAs interface in MOS capacitors was tried. For this, metallic Ti films with 1nm thickness were firstly deposited by e-beam evaporation under ultrahigh vacuum of ~10^{-6} torr on HF cleaned GaAs. And then 6nm Al_2O_3 as gate dielectric oxide was subsequently grown on Ti films by ALD. To suppress the natural oxidation of Ti film, the samples were transferred to ALD vacuum chamber after Ti deposition as soon as possible.

PDA at 550 ℃ under N_2 ambient was carried out. Pt electrode was formed by e-beam evaporation through the patterned shadow mask. Finally Pt/Al_2O_3/Ti/GaAs structure MOS capacitor was fabricated. For comparison, the control sample with Pt/Al_2O_3/GaAs structure which skipped the Ti deposition was also provided. Fig. 3.7 shows the full process flows for the Ti inserted MOS capacitor.

Process flow in chapter 4.4

Substrate: N-type GaAs (Si doped $7.1 \times 10^{17}/cm^3$, 2 inch)

- **Pre-clean : DHF cleaning (10s x 5)**
- **Ti deposition (1nm)**
  - e-beam evaporation
- **ALD oxide deposition (310°C, 6nm)**
  : Al_2O_3 (TMA)
- **Post deposition annealing**
  : 550°C, N_2 ambient
- **Pt evaporation**
- **In backside contact**
- **Analysis**
  : Electrical : C-V hysteresis, frequency dispersion, D_{it}
  : Chemical : XPS, AES (w/o Pt, In)



← Ti deposition by e-beam evaporation

Figure 3.7. Process flow for GaAs MOS capacitors with Ti scavenging effect.

3.2. Electrical and chemical characterization

3.2.1. Electrical evaluation using C-V and G-V measurements

For C-V and G-V measurements, Pt gate electrode and In backside contact in GaAs MOS capacitors were connected with LCR meter (HP4284 Impedance analyzer) and measured under dark environment. Temperature of wafer stage was controlled from 25 ℃ to 125 ℃ through Temptronic Thermochuck Controller (TP03000A2).

C-V hysteresis were characterized by capacitance variation during V_g sweep ranging from -2 V to +4 V and back to -2 V for n-type MOS capacitors. The amounst of hysteresis are defined by the change of flat band voltage (ΔV_{fb}) between forward and reverse sweep.

C-V frequency dispersions were evaluated using 9 (7) frequencies varying logarithmically from 100 Hz (1 kHz) to 1 MHz with 2 frequencies per decade. Variation of capacitances depending on measurement frequencies at accumulation and depletion region were regarded as criteria of the dispersions.

The interface states density (D_{it}) in GaAs band gap were extracted by conductance method which can calculate the D_{it} from C-V and G-V values with the frequency range of 100 Hz to 1 MHz. The D_{it} distributions as a function of trap energy were obatained from the peak substrate conductance (G_p/ω) and corresponding frequency (f). The distribution of D_{it} in the upper

and lower half band gap were separately achieved from the n-type and p-type MOS capacitors, respectively. In addition, wide range D_{it} distribution over band gap could be given by the measurement at 25 ℃ and 125 ℃.

Since large band gap materials such as GaAs have extreme long emission time constant extending the order of several minutes, C-V and G-V measurements at elevated temperature up to 125 °C are enabled to characterize the deep level states near mid-gap.

3.2.2. Chemical and structure analysis of GaAs interface

For the analysis of XPS and AES, 2nm and 10nm thick oxides were deposited on the HF cleaned GaAs wafers, respectively. Deposition parameters for ALD oxides except the thickness are determined in the same manner with the corresponding MOS capacitors. In contrast, gate electrode and backside contact were not provided.

Surface chemical bonding state of the samples were characterized by x-ray photoelectron spectroscopy (XPS) with monochromatic Al K-α source ($h\nu$=1486.7 eV). XPS spectra for Ga 3d and As 3d were primarily focused to discuss the electrical results

Composition depth profiles of the oxides and bulk GaAs were also analyzed by Auger Electron Spectroscopy (AES). To evaluate the interfacial structure in HPO passivation experiments, Transmission Electron Microscopy (TEM) analysis were performed.

4. Results and Discussions

4.1. Evaluation of interface states of GaAs

4.1.1. High temperature measurement for mid-gap analysis

It has been found that high interface state densities more than 10^{13} $cm^{-2}eV^{-1}$ near mid-gap region are generated in oxide/GaAs interface from many reports [50, 114, 126]. Since GaAs has a large band gap of 1.42eV, deep level traps near mid-gap result in extreme long emission time constant extending the order of several minutes, and hence they cannot respond instantaneously to external AC signal with usual frequency range of 100 Hz to 1 MHz in LCR meter at room temperature [59, 114, 115]. To evaluate the deep level interface states of GaAs, C-V measurements at elevated temperature up to 125 ℃ were tried in this study. High temperature C-V can easily measure the deep level trap using only appropriate low frequency starting from 100 Hz available in HP4284 without any additional equipment. However extreme low frequency methods such as quasi-static C-V have some restrictions to setup the measurement systems and prepare the test device with very low leakage current.

Fig. 4.1 shows the characteristic frequency versus trap energy indicating the temperature dependence of measureable trap location under typical range of

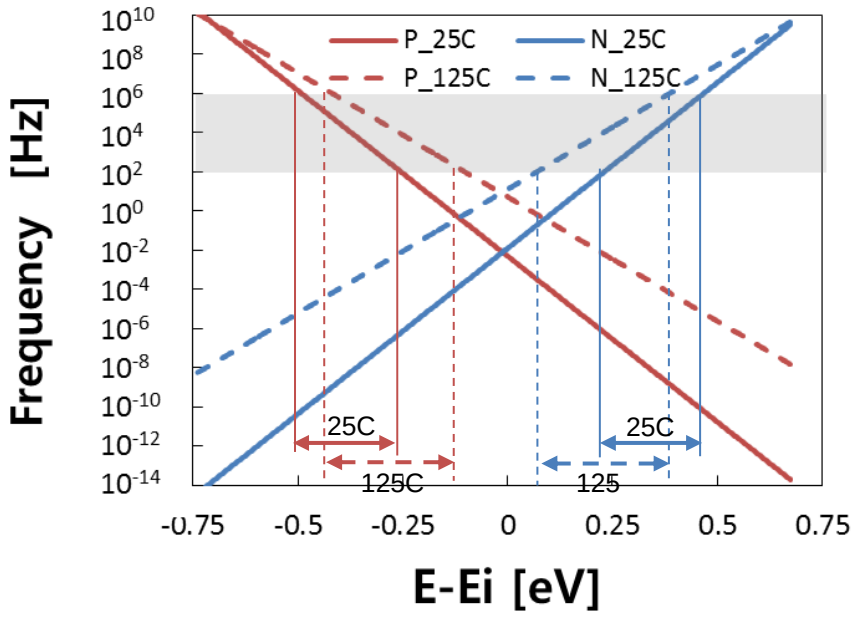


Figure 4.1. Characteristic frequency versus trap energy showing the temperature dependence of measureable trap location under usual frequency range shaded by gray.

C-V frequency shaded by gray. From this relation, it can be seen that almost of GaAs mid-gap region can be probed when measured at 125 ℃ while band edge region can be measured at 25 ℃. More than 55% of band gap can be covered through four different measurement conditions using n-type and p-type MOS capacitors for each measurement temperature.

4.1.2. Electrical characterization of GaAs MOS capacitors

Fig. 4.2 shows temperature dependent C-V frequency dispersions of n-GaAs MOS capacitors measured between 25 ℃ and 125 ℃ in intervals of 25 ℃. At each temperature, C-V curves were measured with 2 frequencies per decade varying logarithmically from 100 Hz to 1 MHz. Variation of accumulation capacitance between 100 Hz and 1 MHz did not nearly change according to measurement temperature. It indicates that the interface states at conduction band edge corresponding to accumulation voltage can be equally respond regardless of the measurement temperature. However in depletion regions, frequency dispersion of capacitance dramatically changed as the temperature increased and depletion capacitance of low frequency eventually reached the maximum capacitance at 125 ℃. These inversion-like shapes are not due to minority carrier because true inversion cannot be generated in large band gap materials like GaAs. Only possible explanation can be obtained by interface states in GaAs. Therefore these results suggest that higher density of interface states exist approaching toward the mid-gap.

Similarly, p-GaAs MOS capacitors provide same behaviors with various temperatures as seen in Fig. 4.3. In addition, the dispersions in depletion regions were observed even at room temperature and became significantly larger than that of n-GaAs MOS capacitor at 125. (Severe dispersions in p-GaAs arise even under higher frequencies than 100 Hz at 125 ℃.) However the dispersions of accumulations were relatively lower than n-GaAs. It means

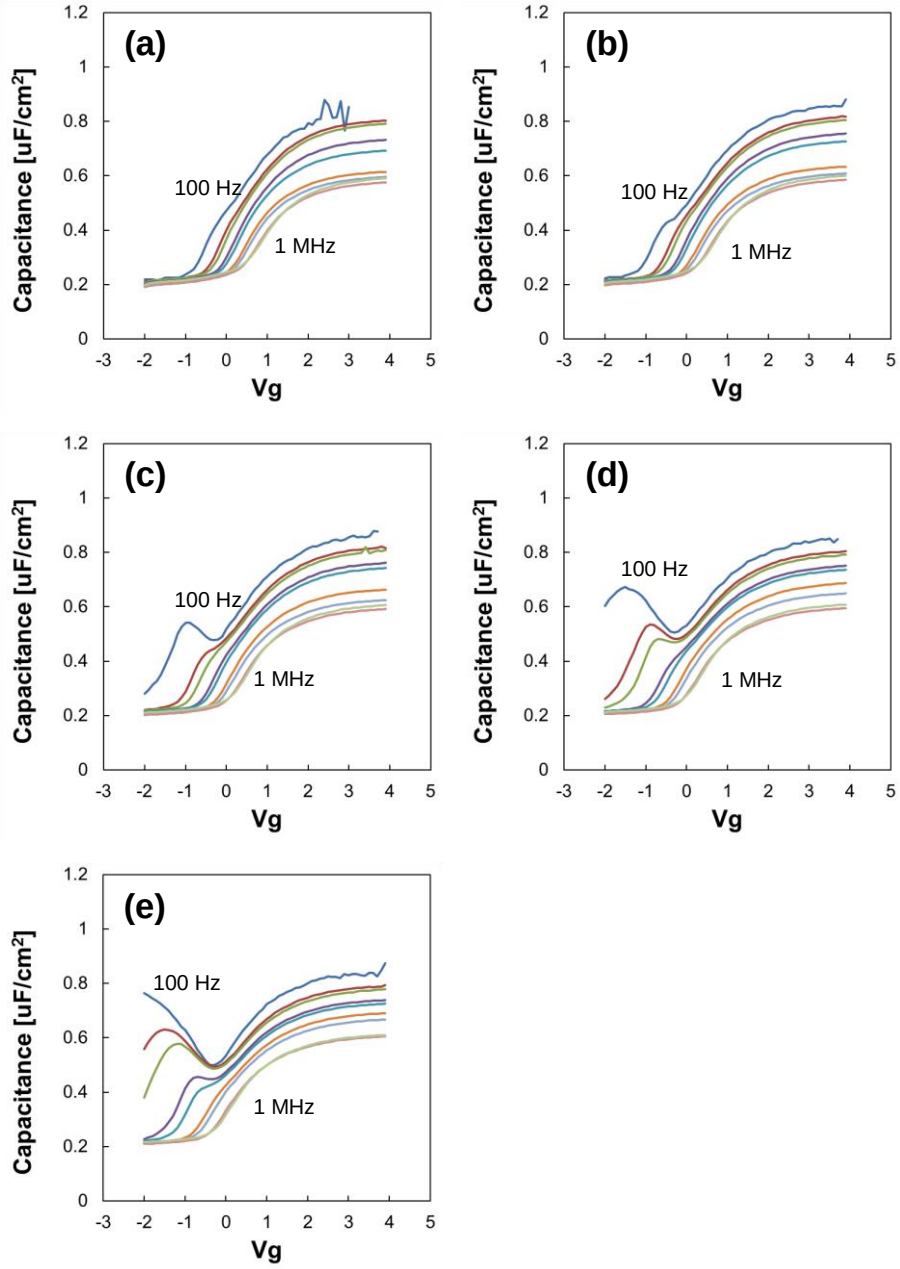


Figure 4.2. C-V frequency dispersions measured at (a) 25 ℃, (b) 50 ℃, (c) 75 ℃, (d) 100 ℃, and (e) 125 ℃ for La_2O_3/n-GaAs MOS capacitors.

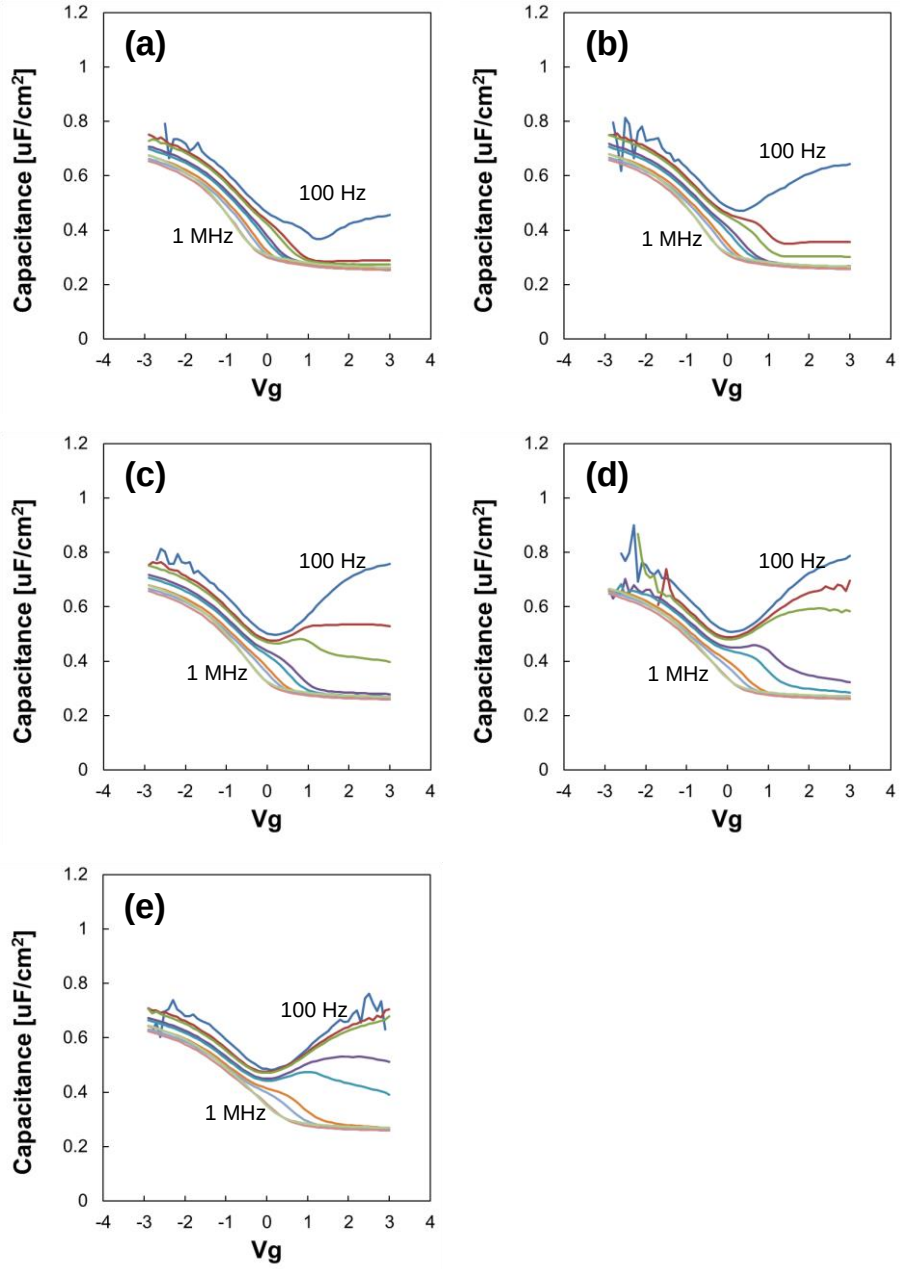


Figure 4.3. C-V frequency dispersions measured at (a) 25 ℃, (b) 50 ℃, (c) 75 ℃, (d) 100 ℃, and (e) 125 ℃ for La_2O_3/p-GaAs MOS capacitors.

that interface states similarly increase approaching toward the mid-gap and especially rapid increase are observed in lower half band gap than upper half band gap judged from the significant dispersions of C_{dep} at high temperature. On the contrary, the states in valence band edge are expected to be smaller than those in conduction band edge from the dispersions of C_{acc}. Asymmetry distribution of D_{it} was also confirmed by conductance method discussed in the end of this chapter.

Generally, large hysteresis in C-V curve can be induced from high densities of deep level states because the trapped charges can stay at the interface states for long time before detrapping from the states due to long emission time constant [59, 114, 115]. To find root cause inducing the hysteresis in GaAs MOS capacitors, C-V hysteresis as a function of measurement temperature were examined as shown in Fig. 4.4. At room temperature huge hysteresis more than 1 V appears and the amount of hysteresis decreased monotonically with increasing temperature and eventually dropped down to 0.43 V at 125 ℃. It is easy to understand that large hysteresis at low temperature such as room temperature can be primarily induced by slow emission process as mentioned above. However, when increasing measurement temperature, even deep level states apart from band edge can begin immediate response to measurement AC signal, resulting in reduced hysteresis. From these results, large hysteresis found in GaAs MOS capacitors at room temperature can be believed to primarily originate from deep level states near mid-gap. This assumption can be also supported by the fact that oxide bulk trap known as another factor

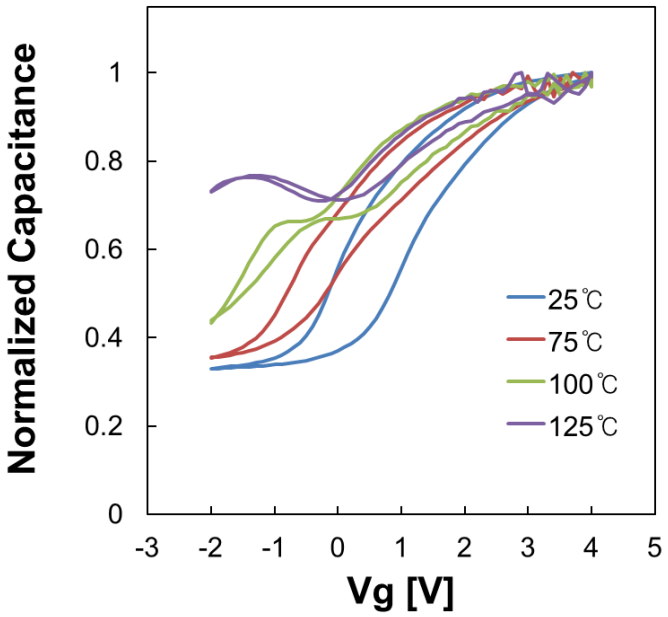


Figure 4.4. C-V hysteresis behaviors dependent on measurement temperatures.

inducing the hysteresis results in higher hysteresis as increasing temperature. The effect of oxide bulk trap on hysteresis will be discussed later in detail through comparison between different gate dielectric structures.

Fermi level movement efficiency can be provided as another criterion for evaluation of interface states [40, 119, 120, 127]. This value can be defined by the ratio of measured and theoretical values of surface potential (Ψ_s) variation rate as below equation.

$$E_F \text{ movement efficiency} = \frac{\text{measured } \Psi_s\text{-}V_g \text{ slope}}{\text{theoretical } \Psi_s\text{-}V_g \text{ slope}} \times 100 \qquad (4.1)$$

Theoretical surface potential can be obtained by solving the below two equations. In this case, the effects of interface states are supposed to be ignored as illustrated in Fig. 4.5 (a).

$$V_g = V_{fb} - \frac{Q_s}{C_{ox}} + \Psi_s \qquad (4.2)$$

$$Q_s = \pm \sqrt{2\varepsilon kTN_d}\left[\frac{n_i^2}{N_d^2}\left\{\exp\left(-\frac{q\Psi_s}{kT}\right)+\frac{q\Psi_s}{kT}-1\right\}+\exp\left(\frac{q\Psi_s}{kT}\right)-\frac{q\Psi_s}{kT}-1\right]^{0.5} \qquad (4.3)$$

On the other hand, measured surface potential are experimentally determined by the following equation known as Berglund integral.

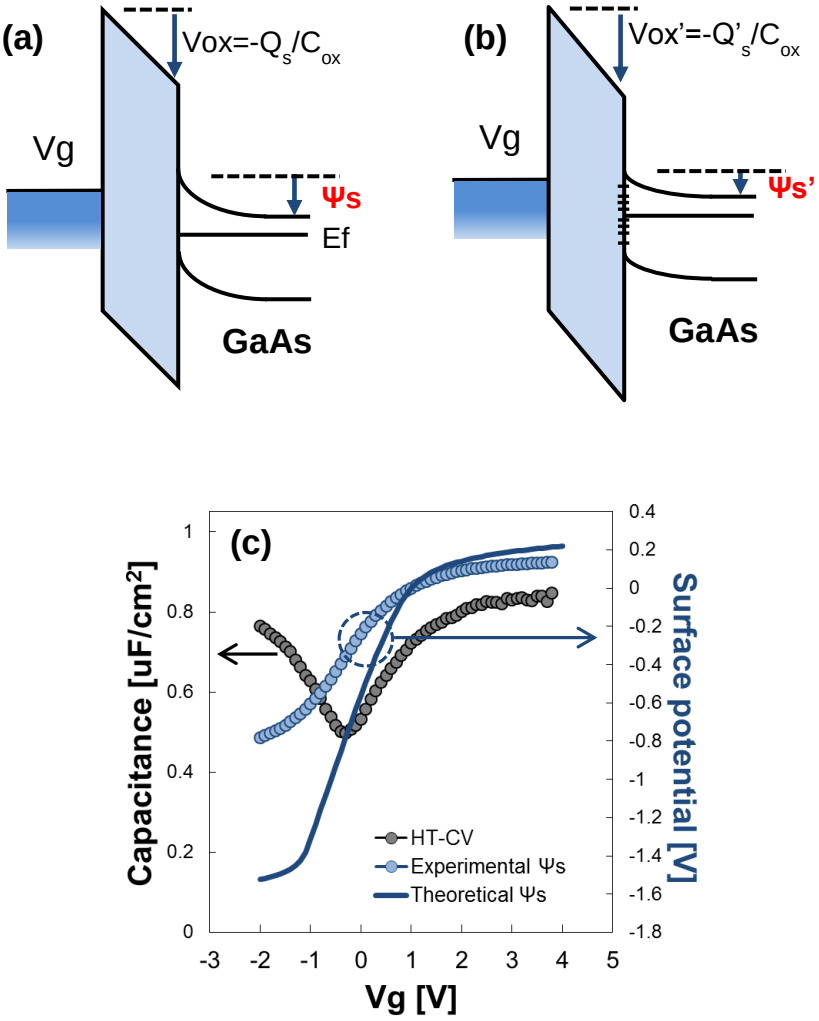


Figure 4.5. Band structures of MOS capacitors of (a) ideal case (D_{it}=0) and (b) real case (D_{it}≠0). Comparison of experimental and theoretical surface potentials (Ψ_s) of La_2O_3/GaAs MOS capacitors in (c). Experimental Ψ_s can be derived from HT-CV.

$$\Psi_s(V) = \int_{V_{fb}}^{V} \left[1 - \frac{C_{LF}(V)}{C_{ox}}\right] dV \qquad (4.4)$$

Of course, measured surface potential can be given under real situation that interface states are not zero as seen in Fig 4.5 (b). Because substrate capacitance (C_s + C_{it}) increase due to existence of C_{it} from the equation of (2.4), band bending (Ψ_s) of this real case is always smaller than that of ideal case. Therefore as the E_F movement efficiency is close to 1, it means that the effects of interface states decrease like ideal case (D_{it}=0). As the efficiency goes down, Fermi level is difficult to be modulated by gate bias due to high interface states. If the efficiency decreases down to zero, Fermi level cannot move and eventually Fermi level become perfectly pinned.

In this (4.4) equation, capacitance as a function of gate voltage ($C_{LF}(V)$) was experimentally determined from high temperature C-V (HT-CV) instead of quasi-static C-V (QS-CV). Fig. 4.5 (c) shows surface potential given by HT-CV measured at 100 Hz and 125 ℃. For comparison, theoretical surface potential is also given together. The efficiency is about 48% for GaAs MOS capacitor and this value is relatively lower than InGaAs with 63% efficiency reported in some literature [120]. It implies that the GaAs MOS capacitors generally suffer from the high interface states.

Direct evaluation of interface states were performed using conductance method. N- and p-type MOS capacitors were used to extract D_{it} in upper half and lower half band gap, respectively. The values of G_p/ω were calculated

from the measured capacitance (C_m) and conductance (G_m) and plotted as a function of measurement frequency. D_{it} and its energy location can be found from the peak value of G_p/ω and corresponding frequency. As sweeping of the gate voltage, distribution of D_{it} with a function of trap energy can be obtained. To access deep level states near mid-gap, the measurements were also conducted at 125 ℃. Fig. 4.6 shows energy distribution of D_{it} in La_2O_3/GaAs MOSCAPs. It is found that the wide range of energy level can be covered through alternating measurement temperature. As the energy level approaching toward mid-gap, high D_{it} more than 10^{13} $cm^{-2}eV^{-1}$ were observed in both upper and lower half band gap. D_{it} located ±0.27 eV away from the E_i in the upper half and lower half band gap were 1.2 x 10^{13} $cm^{-2}eV^{-1}$ and 3.4 x 10^{13} $cm^{-2}eV^{-1}$, respectively indicating that higher D_{it} exist lower half band gap side of mid-gap and these results are consistent with frequency dispersions of n- and p-type MOSCAPs. This anomalous distribution of D_{it} in GaAs is quite different with Si showing the U-shape profiles. Therefore it is very important to understand the origin which induce the huge D_{it} near mid-gap and then find the passivation methods to improve the interface qualities.

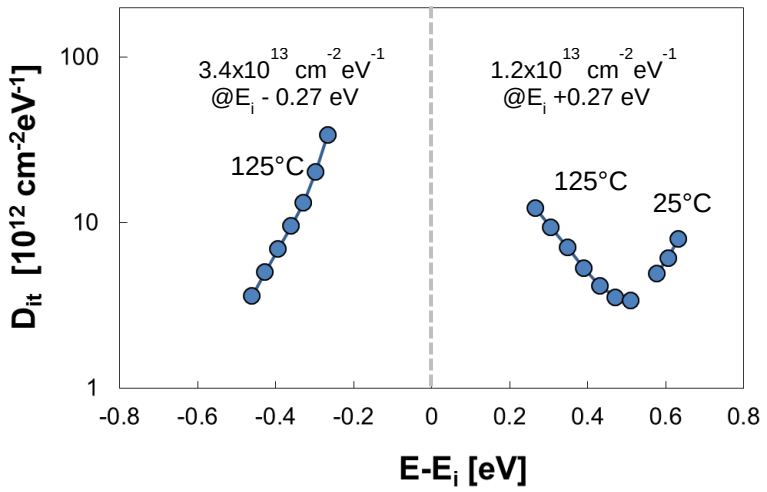


Figure 4.6. D_{it} distribution as a function of trap energy for La_2O_3/GaAs MOS capacitor.

4.2. Effects of interfacial oxides on GaAs

4.2.1. Electrical characterization with different dielectric films

Comparison of electrical properties of GaAs MOS capacitors with different gate dielectric films were performed using C-V hysteresis, frequency dispersion, and interface states density. In Fig. 4.7, C-V hysteresis of n-type GaAs MOS capacitors employed Al_2O_3, SiO_2, La_2O_3, and HfO_2 are shown. All hysteresis show clockwise loop indicating that electron carrier are injected from n-type substrate. However, the degrees of hysteresis vary widely depending on the dielectric materials. Al_2O_3 reveals the best hysteresis result showing the smallest hysteresis of ~0.62 V. For SiO_2, relatively low hysteresis of 0.72 V is also observed. On the other hand, La_2O_3 and HfO_2 show huge hysteresis of 1.1V and 1.5 V, respectively.

Generally C-V hysteresis is due to trapping and detrapping during forward and then reverse voltage sweep. These trapping and detrapping can arise at the oxide bulk trap as well as oxide-semiconductor interface trap with long emission time constant. Because mid-gap states have extremely long emission time constant of the order of 10^3 second in GaAs as already mentioned previously, the trapped charges at mid-gap states can stay for a while and detrap when the voltage sweep direction changes, eventually producing considerable C-V hysteresis. Trapping and emission through oxide bulk trap

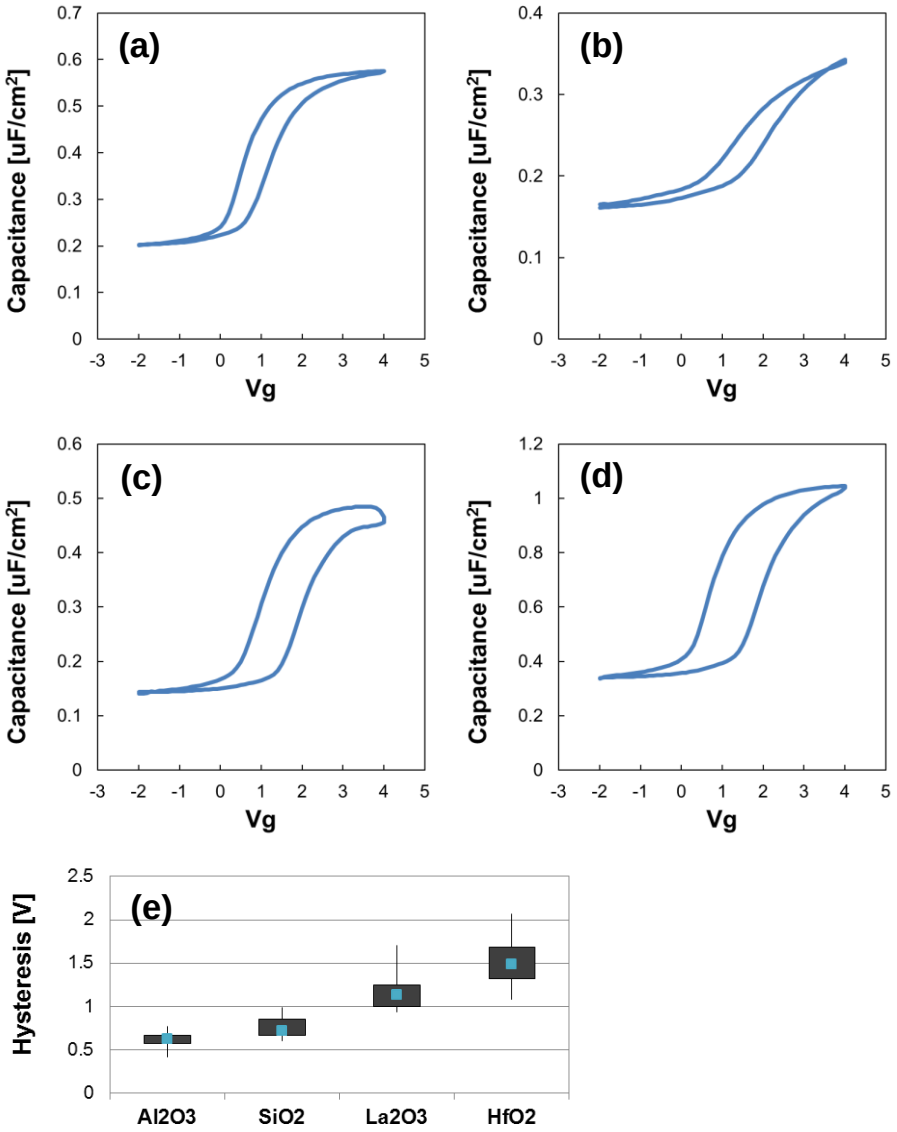


Figure 4.7. C-V hysteresis for (a) Al_2O_3, (b) SiO_2, (c) La_2O_3, and (d) HfO_2 Distributions of hysteresis voltages are shown in (e).

also give rise to the hysteresis. Therefore it needs to find the primary causes which induce the hysteresis of GaAs MOS capacitors between the effect of bulk and interface trap. We will discuss this subject using double stacked oxide layer in the following chapter.

Next we evaluated the frequency dispersion behaviors using the same dielectric oxides as shown in Fig. 4.8. C-V curves were measured from 1 kHz to 1 MHz. Since the frequency dispersion is affected by density of interface state, the distributions of D_{it} can be predicted through the dispersion behaviors depending on dielectric materials. At room temperature, deep trap near mid-gap are very slow and therefore cannot respond with normal measurement frequency. Therefore frequency dispersions in depletion range corresponding to mid-gap region do not appear for all dielectric oxides. The dispersions are only observed in accumulation voltage probing band edge region and there are not significant differences among dielectric materials except HfO_2. It can be suggested that the interface states near band edge of Al_2O_3, SiO_2, and La_2O_3 are similar while that of HfO_2 is significantly large. In contrast, as the measurement temperature goes up, the dispersions in depletion region were observed. This is because the trapping and detrapping of electron charge become fast with an increase of temperature and even deep trap near mid-gap can respond with the measurement frequency at 125 ℃. The dispersions in depletion as well as accumulation range can be seen in Fig. 4.9 measured at 125 ℃. Especially the amounts of dispersion at depletion range are significantly different depending on oxide materials. Smaller dispersions are

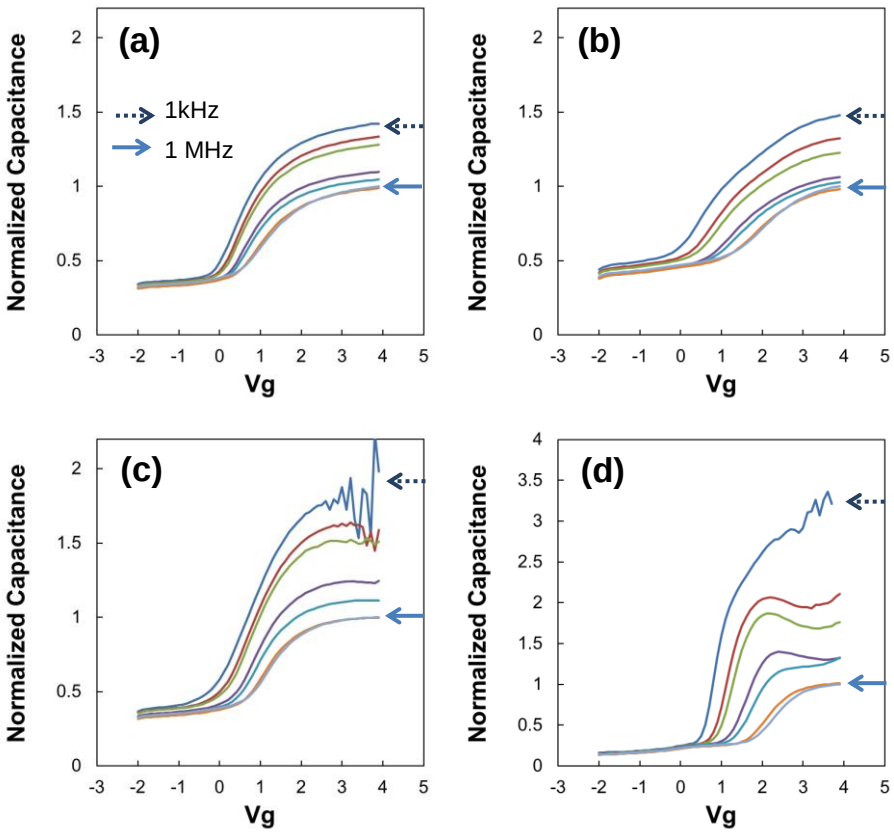


Figure 4.8. C-V frequency dispersions measured at 25 ℃ for (a) Al_2O_3, (b) SiO_2, (c) La_2O_3, and (d) HfO_2.

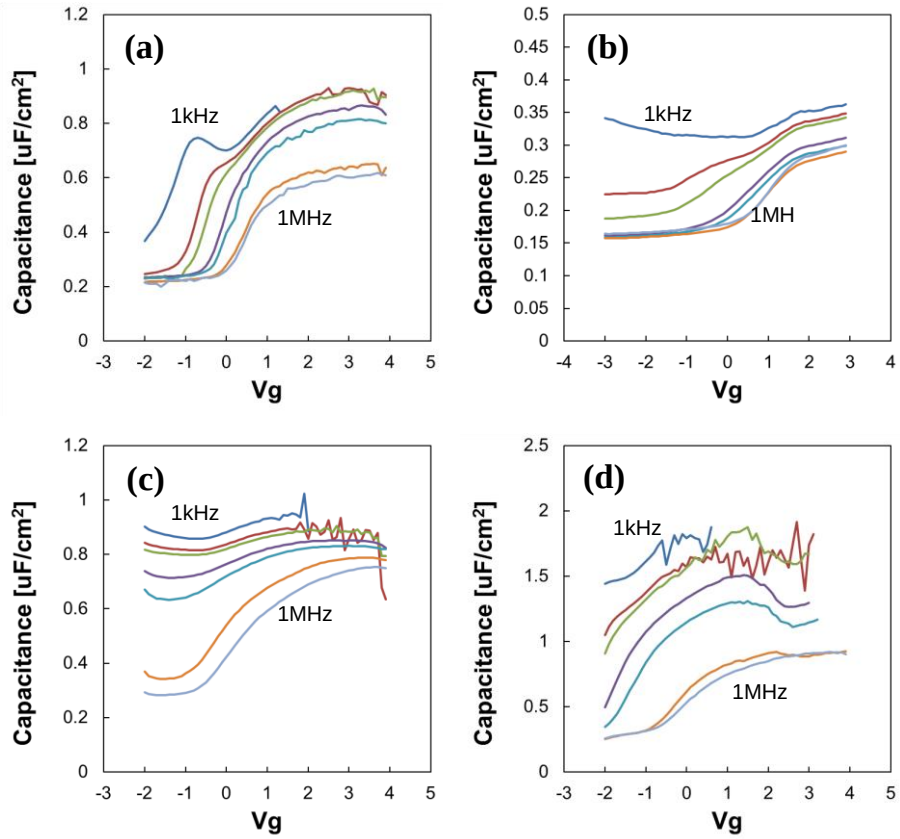


Figure 4.9. C-V frequency dispersions measured at 125 ℃ for (a) Al_2O_3, (b) SiO_2, (c) La_2O_3, and (d) HfO_2.

shown in the order of Al_2O_3, SiO_2, La_2O_3, and HfO_2, which are consistent with hysteresis results.

Thirdly we evaluated the density of interface states as a function of trap energy. Extractions of D_{it} for each dielectric material were performed by conductance method. The values of D_{it} and the trap energy were obtained from substrate conductance peak (G_p/ω) and the corresponding frequency as explained previously. Fig. 4.10 shows D_{it} distributions of four different dielectrics. D_{it} distributions in upper half band gap were measured using n-type GaAs MOS capacitors. It is shown that the D_{it} increases by about 1 order of magnitude as the trap energy approach toward mid-gap region for all samples. It is generally known that GaAs has the peak D_{it} value at mid-gap region as already discussed in the previous part. The extents of the D_{it} near mid-gap are different depending on the gate dielectric materials while there is little difference near conduction band edge as shown in Fig. 4.10. Al_2O_3 has the lowest D_{it} of 7.3×10^{12} $eV^{-1}cm^{-2}$ at $E_i + 0.25$ eV among four different dielectrics. SiO_2 and La_2O_3 are the next in this order. For HfO_2, the largest D_{it} value of 8.8×10^{13} $eV^{-1}cm^{-2}$ is observed at the same energy level. Considering all the electrical results, it can be concluded that C-V hysteresis and frequency dispersion are dependent on dielectric film and determined by the D_{it} near mid-gap region of each dielectric film.

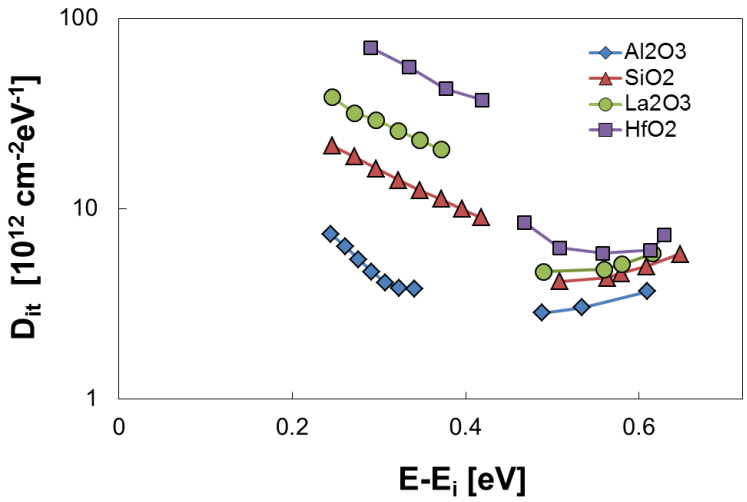


Figure 4.10. D_{it} distributions as a function of trap energy for Al_2O_3, SiO_2, La_2O_3, and HfO_2.

4.2.2. Effects of interface and bulk of dielectric films

In order to separate the effects of interface and bulk of dielectric on the electrical results, we evaluated the MOS capacitors having double stacked dielectric layers where two different oxides were located in lower interface and upper bulk region, respectively. MOS capacitors with the structure of Pt/HfO_2(5nm)/SiO_2(2nm)/GaAs were prepared. For comparison, MOS capacitors with opposite stacking sequence in gate dielectrics, Pt/SiO_2(5nm)/HfO_2(2nm)/GaAs, were also employed. Although two MOS capacitors include same oxide materials, amount of hysteresis and frequency dispersion are quite different due to different stacking sequence as shown in Fig 4.11 and Fig 4.12, respectively. It is expected that the location of the oxides as well as oxide material itself is important to decide the electrical characteristics.

MOS capacitor using HfO_2(5nm)/SiO_2(2nm) structure shows better hysteresis result of 0.73 V than single HfO_2 of 1.5 V as shown in Fig. 4.11 and Fig. 4.7. This hysteresis of HfO_2(5nm)/SiO_2(2nm) is even similar to that of single SiO_2(7nm) of 0.72 V. In Fig. 4.12, frequency dispersion of HfO_2(5nm)/SiO_2(2nm) is close to that of SiO_2 rather than HfO_2. By insertion of thin SiO_2 interfacial layer, bulk HfO_2 effect, which tends to induce detrimental hysteresis and frequency dispersion, seems to almost disappear. In contrast, for the MOS capacitor using SiO_2(5nm)/HfO_2(2nm) structure, significantly large hysteresis of 1.3 V were measured which was comparable

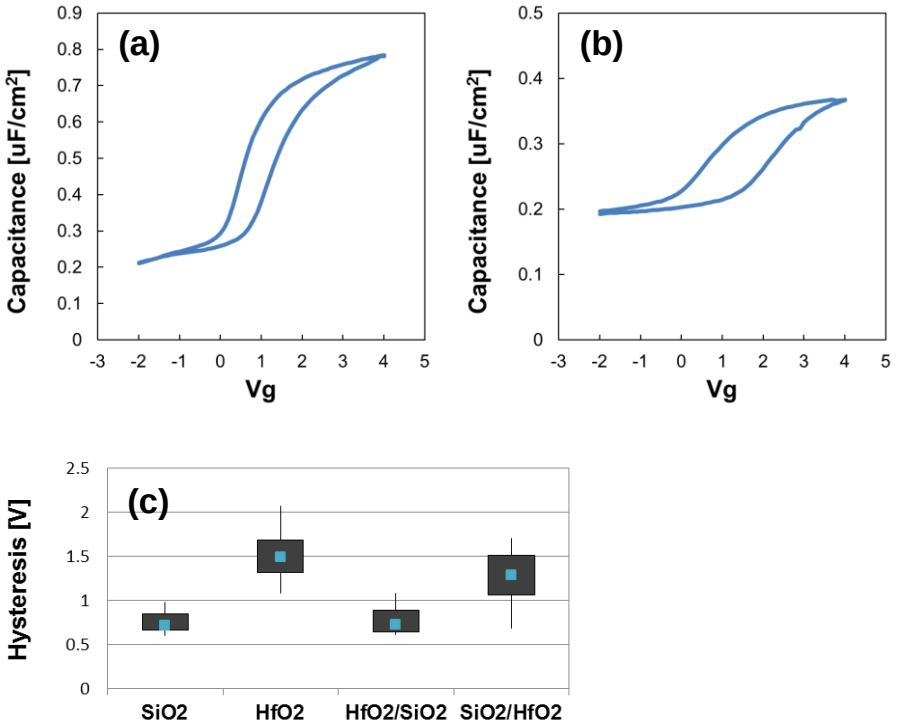


Figure 4.11. C-V hysteresis for (a) HfO_2 on SiO_2 and (b) SiO_2 on HfO_2. Distributions of hysteresis voltages are shown in (c).

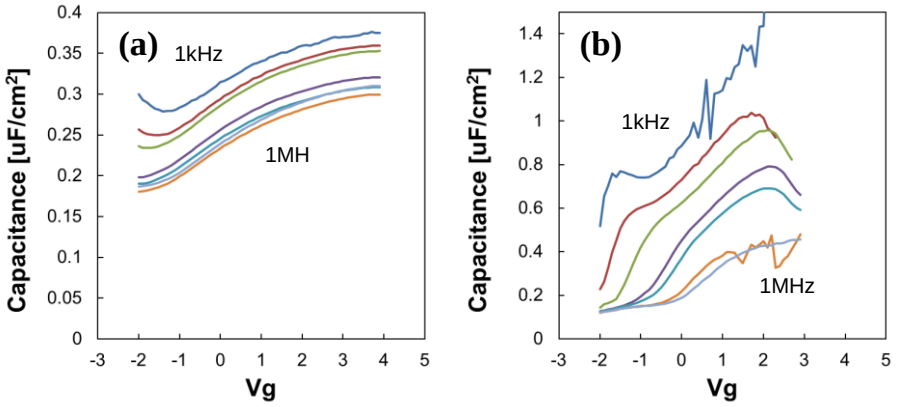


Figure 4.12. C-V frequency dispersions measured at 125 ℃ for (a) HfO_2 on SiO_2 and (b) SiO_2 on HfO_2.

with HfO_2 but much worse than SiO_2. Similar behavior in frequency dispersions are also shown in Fig. 4.12. Therefore it can be concluded that electrical characteristics such as hysteresis and frequency dispersion are determined by thin interfacial layer rather than thick bulk layer. These results also support the fact that the hysteresis is primarily induced from interface state near mid-gap.

4.2.3. Effects of insertion of Ga_2O_3 film at GaAs interface

In this part, to evaluate the effect of Ga oxide at GaAs interface, thin Ga_2O_3 was intentionally inserted between GaAs substrate and Al_2O_3 gate dielectric. The 3nm thick Ga_2O_3 and 4nm thick Al_2O_3 were sequentially deposited on cleaned GaAs substrate by ALD using tri-methyl-Gallium (TMG) and tri-methyl-Aluminum (TMA), respectively. For a control sample, MOS capacitor using only the 7nm thick Al_2O_3 gate dielectric was also prepared. Electrical characterization using C-V and G-V measurements at elevated temperatures up to 125 ℃ were given to analyze the deep level interface trap of GaAs.

From the X-ray Photoelectron Spectroscopy (XPS) analysis, Ga_2O_3 phase which is located near 20.3 eV, is confirmed to be mainly produced on GaAs in the Ga oxide deposition sample compared to Al_2O_3 deposition sample as shown in Fig. 4.13. In contrast, there is little difference between two samples in the region of As 3d spectra.

As can be seen in the Fig. 4.14, for the MOS capacitor using Al_2O_3/Ga_2O_3, slightly larger dispersion is observed in accumulation region at 25 ℃. (See the C-V curves measured at 1 MHz in both samples.) However huge dispersion in depletion region at 125 ℃ appears compared with the MOS capacitor using single Al_2O_3 as seen in Fig. 4.15. In addition, the Al_2O_3/Ga_2O_3 sample also shows two times larger hysteresis of C-V curves compared with the control Al_2O_3 sample as shown in Fig. 4.16. In the measurements of Fermi level movement efficiencies as a criterion of Fermi level pinning, the

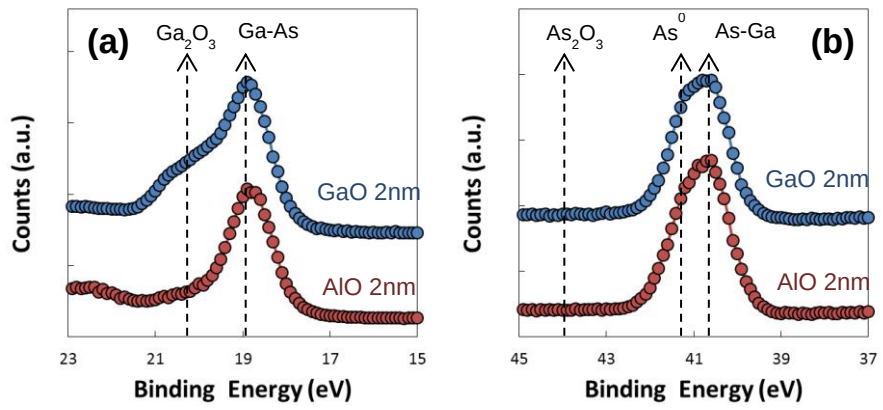


Figure 4.13. XPS spectra of (a) Ga 3d and (b) As 3d for 2nm thin Al_2O_3 and Ga_2O_3 samples.

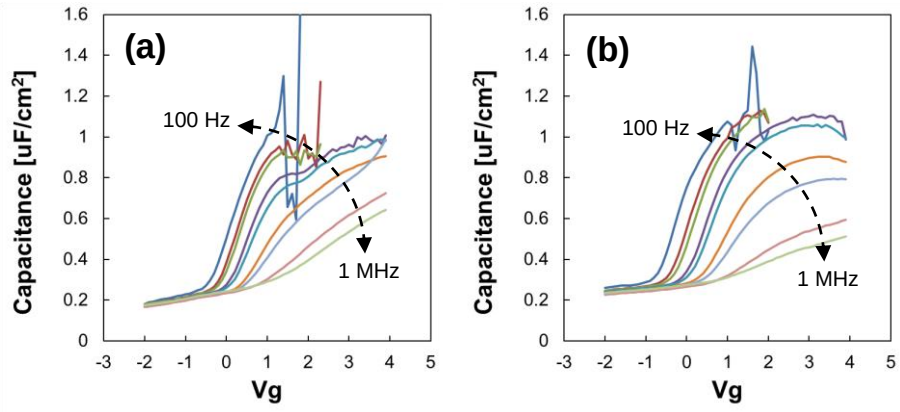


Figure 4.14. C-V frequency dispersions measured at 25 ℃ for (a) Al_2O_3 and (b) Al_2O_3 on Ga_2O_3.

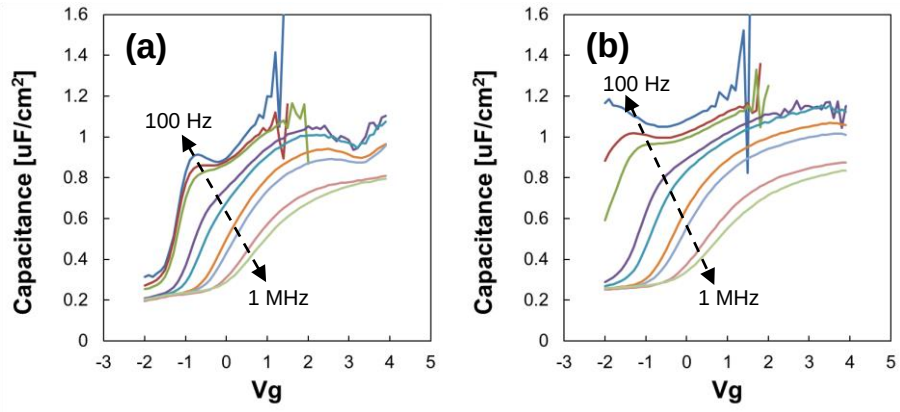


Figure 4.15. C-V frequency dispersions measured at 125 ℃ for (a) Al_2O_3 and (b) Al_2O_3 on Ga_2O_3.

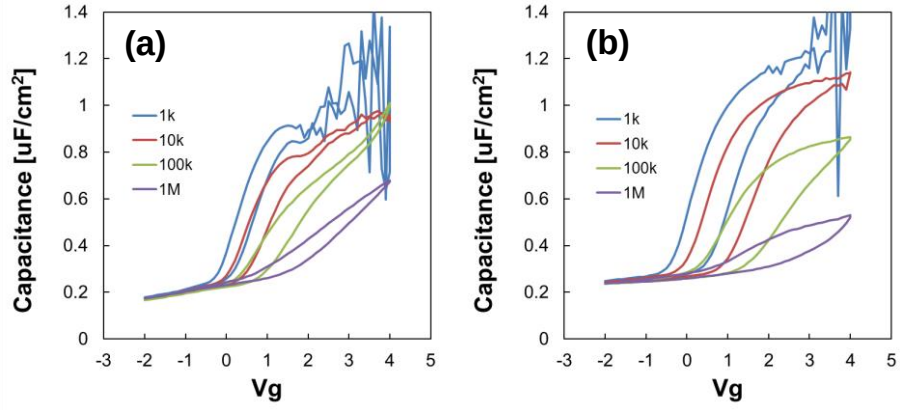
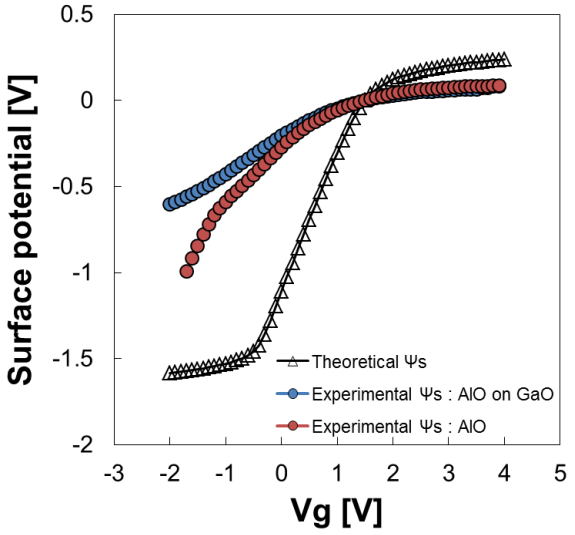


Figure 4.16. C-V hysteresis measured at the frequency of 1 kHz, 10 kHz, 100 kHz, and 1 MHz for (a) Al_2O_3 and (b) Al_2O_3 on Ga_2O_3.

Al_2O_3/Ga_2O_3 sample shows about 25 % efficiency which is significantly lower than the Al_2O_3 sample of ~44 % as shown in Fig. 4.17. These results indicate that higher interface states in deep level near mid-gap can arise due to Ga_2O_3. Consistent results were also obtained in the D_{it} measurements, extracted from the Al_2O_3/Ga_2O_3 and Al_2O_3 samples, which showed 1.8 x 10^{13} $cm^{-2}eV^{-1}$ and 9.1 x 10^{12} $cm^{-2}eV^{-1}$, respectively, at the same energy level of E_i + 0.27 eV as shown in Fig. 4.18. Considering all the analysis, it can be concluded that Ga_2O_3 plays a role as a interfacial defect to generate the D_{it}. Therefore, suppression of Ga_2O_3 generation is essential for improvement of interface characteristics.



	Al_2O_3	Al_2O_3 on Ga_2O_3
E_F movement efficiency	43.6%	24.8%

Figure 4.17. Surface potential variations as a function of gate voltage and E_F movement efficiencies as a criterion of Fermi level pinning for Al_2O_3 and Al_2O_3 on Ga_2O_3.

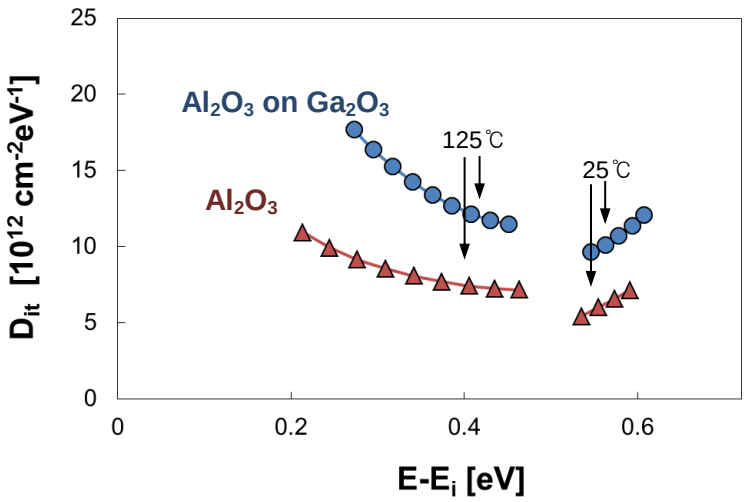


Figure 4.18. D_{it} distribution profiles as a function of trap energy measured at 25 ℃ and 125 ℃ for Al_2O_3 and Al_2O_3 on Ga_2O_3.

4.2.4. Formation of Ga_2O_3 depending on dielectric films

To find the reason for different interfacial properties depending on dielectric materials, we evaluated the amount of interfacial Ga_2O_3 with four different dielectrics by XPS. Although Ga_2O_3 are completely removed by wet etching from starting GaAs substrate, interfacial Ga_2O_3 are supposed to be naturally regrown by oxidation of GaAs during gate oxide deposition or post deposition annealing (PDA). All conditions including deposition temperature, oxidant for Al_2O_3, PDA temperature, etc are same except only metal precursors for gate dielectric films. Fig. 4.19 shows the Ga 2p XPS spectra with four different dielectrics. Ga_2O_3 peak intensities are shown to be varied depending on dielectric materials. Al_2O_3 exhibits the lowest Ga_2O_3 peak and SiO_2, La_2O_3, and HfO_2 show lower Ga_2O_3 peak in this order. These results are consistent with the electrical properties such as hysteresis, frequency dispersion, and interface state density suggesting that relative detrimental properties depending on dielectric materials can be explained by the Ga_2O_3 formation at interface.

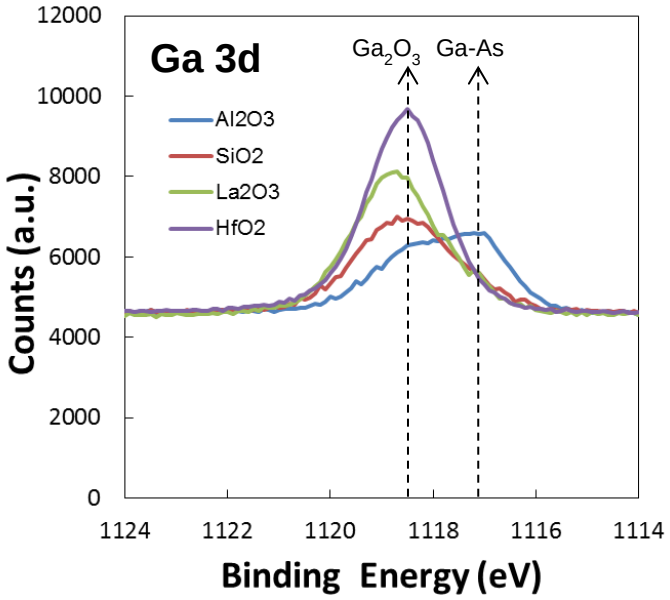


Figure 4.19. XPS spectra of Ga2p for (a) Al_2O_3, (b) SiO_2, and (c) La_2O_3 , and (d) HfO_2.

4.3. Passivation of GaAs using high pressure oxidation (HPO)

4.3.1. Effects of HPO passivation on electrical characteristics

In this chapter surface passivation using HPO performed at 10atm at 400 °C for 0.5 hour and following HF etching were evaluated. Because this HPO and subsequent HF etching were performed prior to gate dielectric deposition, it can be expected to give little difference in gate oxide structure. Fig. 4.20 shows the C-V characteristics of the control and HPO MOS capacitors at a room temperature. An identical V_g sweep ranging from -2 V to +4 V and back to -2V was applied because both devices have similar accumulation capacitance and comparable capacitance equivalent thickness (CET). The control device suffered from a huge clockwise hysteresis of >1.3V and stretchout of the capacitance under the depletion region, suggesting that substantial charge carriers are likely to be trapped at the interfacial trap sites and/or partially injected into the bulk region of ALD-derived Al_2O_3 dielectric film during the on-state operation V_g stressing duration. In particular, the hysteresis of C-V for the control device can be attributed to the existence of slow trap states with an extremely long emission time of ~several minutes as discussed early. In contrast, the HPO capacitor exhibited considerably reduced hysteresis (ΔV_{FB} = ~0.5 V) without accompanying stretchout phenomena,

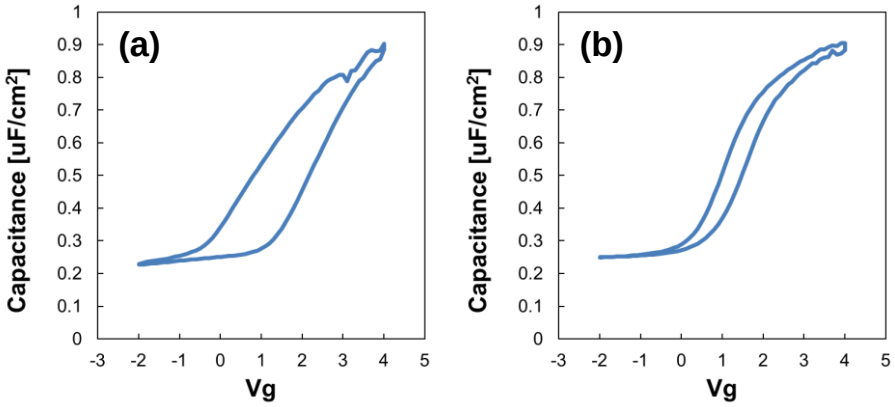


Figure 4.20. C-V hysteresis for (a) control sample and (b) HPO passivated sample.

suggesting that the D_{it} values of the MOS capacitor can be reduced substantially by introducing a HPO treatment and subsequent HF etching.

Fig. 4.21 shows the frequency dispersion characteristics of the control and HPO capacitors, respectively. The C-V curves with AC signal frequencies ranging from 100 Hz to 1 MHz were measured at 125 °C because the inactive deep level defect states at room temperature can respond to the external AC signal by increasing the measuring temperature. The HPO device showed less frequency dispersion and stretchout at a negative V_g while the control device induced the severe dispersion showing large C-V hump up to 5 kHz. This confirmed that the superior interfacial quality induced by the GaAs semiconductor and Al_2O_3 dielectric film can be achieved by a HPO treatment and subsequent HF etching.

Fig. 4.22 shows surface potential variation as a function of gate voltage and E_F movement efficiencies for each sample. From these results, surface potential can be easily modulated by gate bias in HPO sample compared to control sample. As a consequence, the efficiency of HPO sample is 16% larger than that of control sample indicating much smaller D_{it}.

Fig. 4.23 gives a quantitative comparison of the D_{it} distribution for both devices. The D_{it} values in upper and lower half band gap were extracted from the n-type and p-type $Pt/Al_2O_3/GaAs$ devices, respectively. To obtain the mid-gap D_{it}, conductance measurements were carried out at 125 °C. The overall D_{it} distributions of the HPO capacitors were improved compared to the control

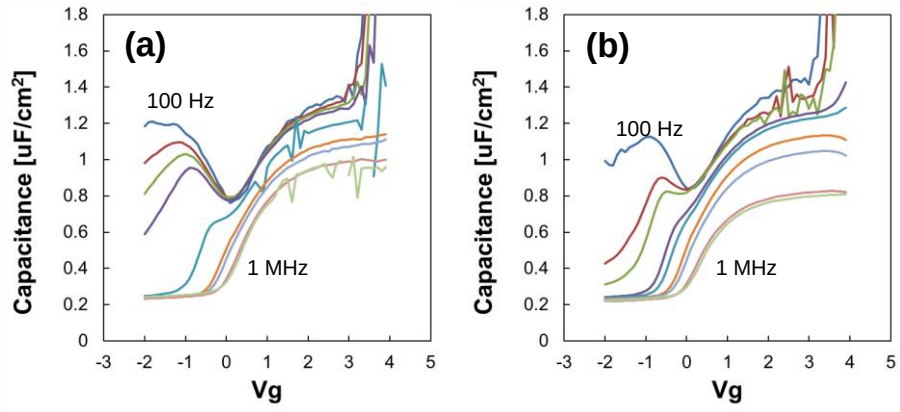
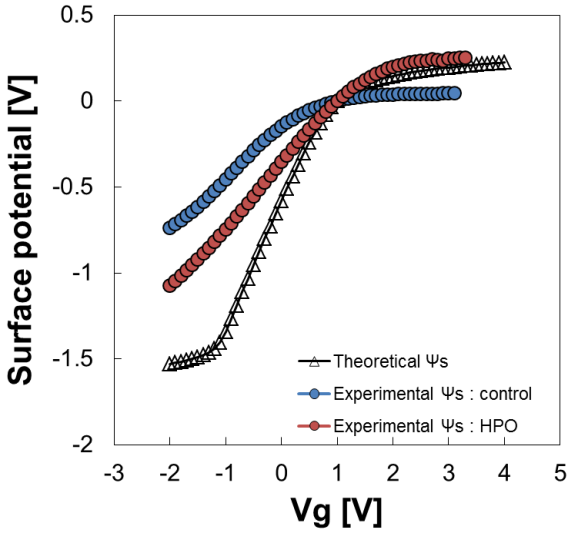


Figure 4.21. C-V frequency dispersions measured at 125° for (a) control sample and (b) HPO passivated sample.



	Control	HPO
E_F movement efficiency	37.7%	53.7%

Figure 4.22. Surface potential variations as a function of gate voltage and E_F movement efficiencies for control sample and HPO passivated sample.

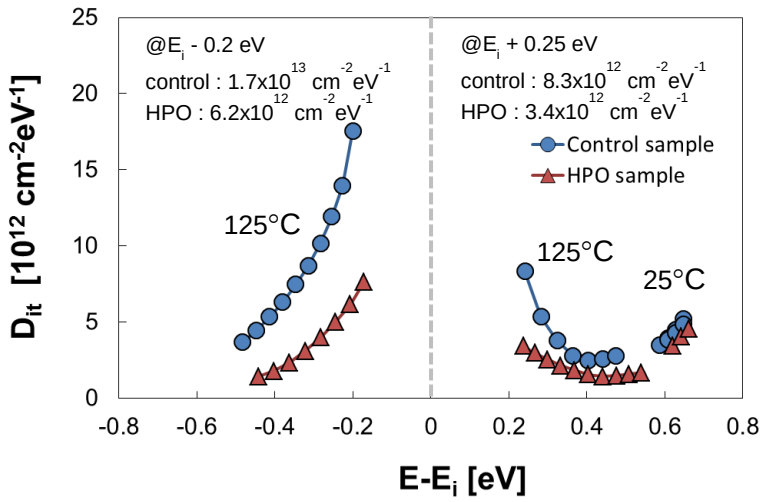


Figure 4.23. D_{it} distributions in the GaAs band gap of the control and HPO MOS capacitors. They were extracted from the conductance method at 25 ℃ and 125 ℃ using n-type and p-type GaAs MOS capacitors.

capacitors. Therefore, the D_{it} values at $E_i - 0.4$ eV and $E_i + 0.4$ eV for the HPO device were reduced from 5.3×10^{12} and 2.5×10^{12} (control device) to 1.8×10^{12} and 1.6×10^{12} $cm^{-2}eV^{-1}$, respectively. Interestingly, the trap states near the mid-gap were eliminated more effectively than those near the valence and conduction band edge. For example, the D_{it} values at $E_i - 0.2$ eV and $E_i + 0.25$ eV for the HPO device were 6.2×10^{12} and 3.4×10^{12} $cm^{-2}eV^{-1}$, respectively, whereas the corresponding values for the control device were 17.5×10^{12} and 8.3×10^{12}. This suggests that the HPO treatment and HF etching process can passivate the mid-gap states of the resulting MOS capacitor in a more effective manner.

It is noted that the improvement in the frequency dispersion property for the HPO capacitor seems to be rather weak (in Fig. 4.21) whereas the D_{it} values near mid-gap for the HPO device were reduced significantly compared to those for the control capacitor. This observation can be explained by the serial capacitance modeling of the MOS capacitor device. The overall capacitance of these MOS capacitors can be given by $C_{tot} = [C_{ox}^{-1} + (C_{sub}^{-1} + C_{it}^{-1})]^{-1}$ as described in the equation (2.4) on where C_{ox}, C_{sub} and C_{it} are the dielectric, substrate and interfacial trap-related capacitance, respectively. Generally, the smaller capacitance component affects the larger variation of C_{tot} value in the serial capacitor connection. The rather high D_{it} distribution ($> 10^{12}$ $eV^{-1}cm^{-2}$) for both devices rendered the comparable or even larger C_{it} than C_{ox}, which weakened the effect of D_{it} on the frequency dispersion characteristics in Fig.

4.21. Therefore, the further reduction of D_{it} distribution by optimizing the device fabrication process is expected to allow the better frequency dispersion property of the resulting capacitor.

4.3.2. Interfacial analysis of HPO passivated surface

To obtain insight into HPO-induced trap passivation, the chemical state of the pristine and thermally oxidized GaAs surfaces were characterized by XPS. Fig. 4.24 shows the evolution of the Ga 3d and As 3d XPS spectra for the HPO treated and HF-etched GaAs substrate. As an internal reference, the XPS spectra for the only HF-etched GaAs surface without a HPO treatment are also shown (referred to as 1st HF etching). The Ga 3d and As 3d XPS spectra for the only HF-etched GaAs consisted of Ga-As lattice bonding, which reflects the bulk chemical state of the GaAs crystal. The weak signal from Ga-O bonding can be attributed to the existence of a native oxide layer that presumably formed at the time interval between HF etching and loading in the ex-situ XPS chamber. In contrast, the lattice Ga-As bonding-related peaks disappeared almost completely for the HPO treated sample, as shown in Fig. 4.24. Instead, most Ga atoms converted to the ionic bonding to the oxygen anion, indicating the formation of a thermal Ga_2O_3 film during the HPO treatment. Selective oxidation with Ga can be understandable considering the thermodynamic instability of As_2O_3 under the given oxidation conditions. The following two reactions can be used to describe this selective oxidation process during HPO treatment based on thermodynamic predictions.

$$3O_2 + 2GaAs \rightarrow Ga_2O_3 + As_2O_3 \quad (4.5)$$

$$As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As \quad (4.6)$$

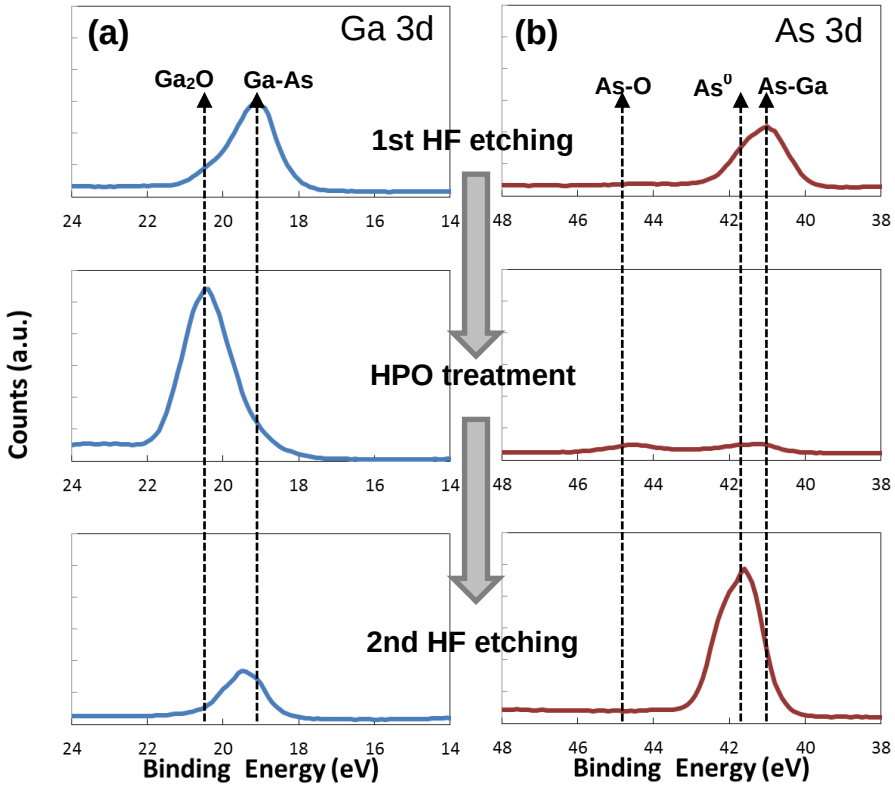


Figure 4.24. (a) Ga 3d and (b) As 3d XPS spectra showing the chemical evolution of a GaAs substrate after the HPO treatment and subsequent HF etching process.

According to Le Chatelier's principle, the equilibrium of the reaction (4.5) shift toward right direction to form oxides at even relatively low temperature of 400 °C when the pressure is increased in the thermal oxidization furnace. The As oxide that formed during the HPO treatment would evaporate because of its high volatility or react chemically with GaAs, leading to the formation of more stable Ga_2O_3 at ~ 400 °C as given in reaction (4.6).

In the HF etched sample after the HPO treatment (referred to as 2nd HF etching in Fig. 4.24), the Ga-O lattice-related peaks disappeared while strong As-As peak grew substantially. This suggests that the surface Ga_2O_3 was removed almost completely, leaving behind a large amount of elemental As on the GaAs surface. Therefore, the top surface of the GaAs substrate would have As excess and Ga deficient non-stoichiometry. This can be confirmed by the AES depth profile. Fig. 4.25(b) and 4.25(c) show the atomic depth profile of Ga, As, O, and C for the HPO-treated and HF-etched GaAs samples, respectively. It was confirmed that the elemental As which cannot be detected by XPS due to thick Ga_2O_3 existed at the bottom interface by AES depth analysis. The As content remaining in the Ga_2O_3 layer that formed during the HPO treatment was not eliminated by subsequent HF etching, which strongly accumulated at the surface of GaAs, as shown in Fig. 4.25 (c). The As excess and Ga deficient surface would slow the kinetics of Ga_2O_3 formation during the subsequent ALD process of the Al_2O_3 dielectric film. In addition, the excess As layer on the GaAs surface would prevent oxygen species from

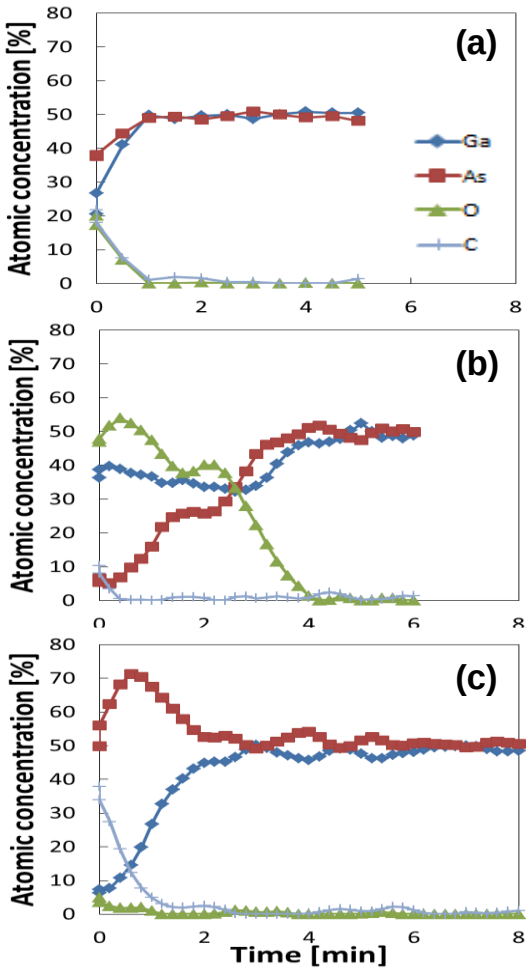


Figure 4.25. AES depth profiles after the (a) 1st HF etching, (b) HPO and (c) subsequent 2nd HF etching of GaAs substrate.

diffusing toward the GaAs substrate, leading to the suppression of Ga_2O_3 formation. This can be confirmed by an examination of the XPS spectra of a 2-nm-thick Al_2O_3 film grown on passivated GaAs substrates. Fig. 4.26 shows the Ga 3d and As 3d XPS spectra of the Al_2O_3/GaAs substrates post annealed at 550 °C depositing a 2-nm-thick Al_2O_3 by ALD. For the control sample, a considerable amount of Ga_2O_3 was formed, suggesting that the self-cleaning effect of the TMA precursor during the ALD process is limited. In contrast, no undesirable Ga-O lattice peak was observed for the Al_2O_3 film on the HPO sample, as shown in Fig. 4.26 (a). On the other hand, the neutral As species formed by the HPO treatment are likely to either sublime due to its high volatility during Al_2O_3 deposition process or be oxidized to As_2O_3 and As_2O_5 as detected in Fig. 4.26 (b), which can be also inferred from the identical As peak with the control sample near 40~41 eV. The slight existence of As_2O_3 or As_2O_5 related peaks for the HPO treated Al_2O_3/GaAs sample suggests that the conversion from As_2O_3 to As is suppressed strongly due to the low concentration of surface Ga, aforementioned in the reaction (4.6). This corroborates a previous explanation based on HPO-induced non-stoichiometry. Therefore, the superior interfacial quality of the HPO-treated MOS capacitor compared to the control capacitor can be attributed to the surface modification of GaAs with an As excess and Ga deficiency caused by the formation of a selective Ga_2O_3 layer and subsequent etching. In the literature, the As and Ga rich surface reconstructions are reported to be closely related to the amount of Ga_2O_3 and other interfacial oxide species, which affects the electrical

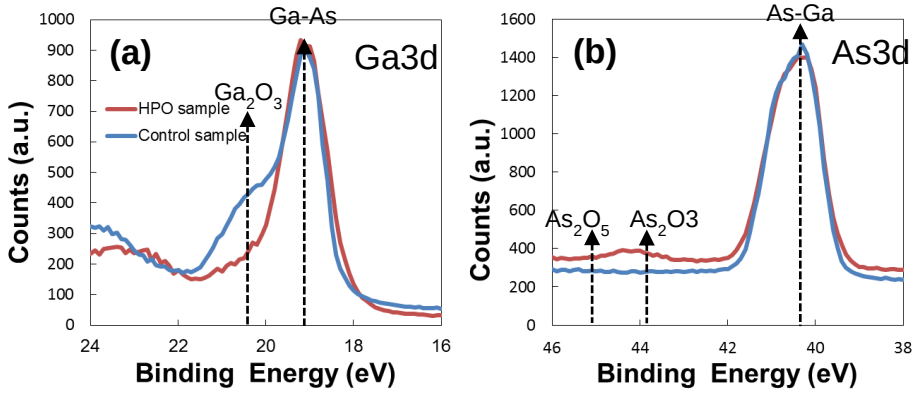


Figure 4.26. (a) Ga 3d and (b) As 3d XPS spectra showing the Ga-oxide (Ga3+) and As-oxide (As3+) on the GaAs surface after Al_2O_3 deposition and subsequent annealing at 550 ℃ among the HPO and control sample.

properties of the MOS capacitors [128]. In this study, the effect of HPO treatment is analogous to (2 x 4) reconstruction in terms of As rich surface. However, since the thick As layer to suppress the Ga_2O_3 are produced by HPO process, better electrical properties can be expected than As-rich (2 x 4) reconstruction.

In Fig. 4.27 shows the TEM images of HPO passivated and control samples. Final structure of HPO passivated sample is found to be same with control sample except the interfacial layer of Ga_2O_3, as above mentioned from the XPS analysis. While the dark interfacial layer supposed to be Ga_2O_3 is shown between Al_2O_3 and GaAs substrate in the control sample, no interfacial layer is observed in HPO sample suggesting consistent results with XPS analysis.

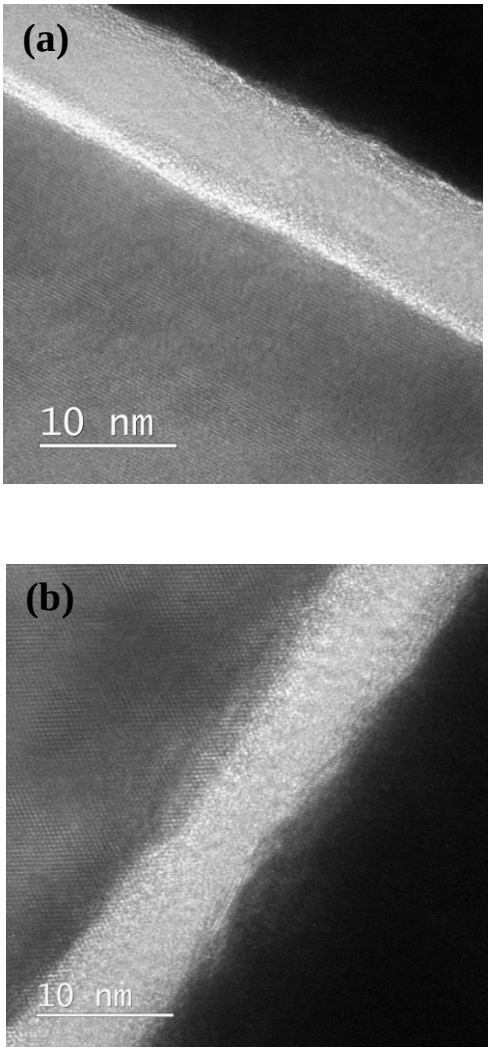


Figure 4.27. TEM images showing Pt/Al_2O_3/GaAs MOS structure for (a) control sample and (b) HPO passivated sample.

4.3.3. Effects of oxidation temperature and pressure

In this study, we also examined whether conventional thermal oxidation under oxygen ambient of 1 atm and subsequent HF etching would result in similar improvement in terms of the D_{it} distribution in the resulting GaAs MOS capacitor. Thermal oxidations of the GaAs substrate were performed under 1 atm for 0.5 hour at 400 °C and 600 °C referred to as APO (atmospheric pressure oxidation) and HTO (high temperature oxidation) respectively.

Firstly C-V hysteresis were evaluated and compared as shown in Fig. 4.28. APO sample shows comparable hysteresis with control sample of around 1V indicating that any passivation effect cannot be obtained by APO. Moreover it was found that HTO gives much more degraded hysteresis of 1.25V and stretchout of C-V curve than APO as well as HPO. Interfacial defects are expected to increase by HTO process.

Energy distributions of D_{it} were also evaluated. Four different samples were compared in terms of mid-gap D_{it} measured at 125 °C as shown in Fig. 4.29. Consistent results with C-V hysteresis were found showing the high D_{it} in the order of HTO, APO or control, and HPO. Only HPO exhibited the significant improvement of interface properties leading reduction of D_{it} less than half of the non-passivated interface as already discussed in the previous chapter. However APO revealed little improvement showing negligible

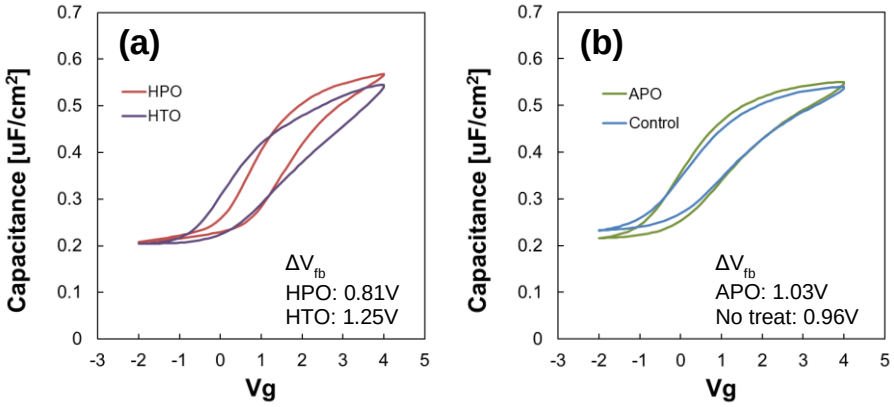


Figure 4.28. C-V hysteresis of (a) HPO and HTO, and (b) APO and control sample.

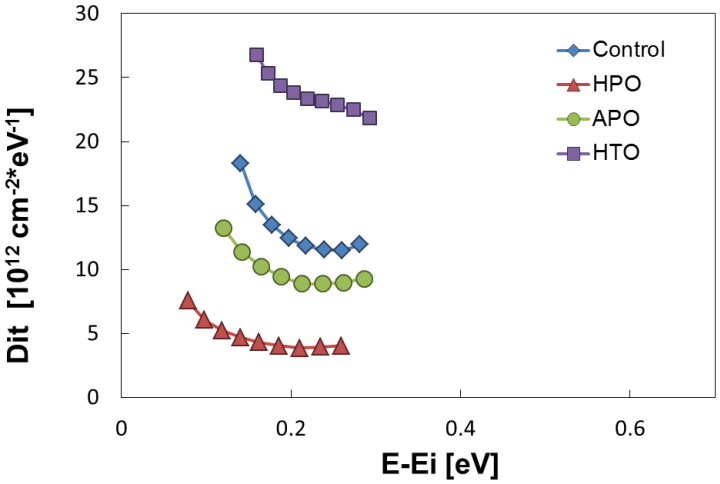


Figure 4.29. Dependence of D_{it} distributions on thermal passivation: HPO, APO, HTO and control sample.

passivation effect compared to control sample. Especially in the case of HTO, huge D_{it} more than 2.5 x 10^{13} $cm^{-2}eV^{-1}$ was given near mid-gap suggesting that consequentially this is not appropriate passivation method.

These electrical results can be explained by AES and XPS analysis. As observed in Fig. 4.30, the evolutions of surface structure produced by each oxidation method were confirmed from AES depth profile. APO samples revealed much smaller Ga_2O_3 thickness than HPO just after oxidation. [Fig. 4.30 (a)] As a result, arsenic layer obtained by following HF etching was also very thin. [Fig. 4.30 (b)] It is reasonable to conclude that this arsenic layer is too insufficient to block the surface oxidation of GaAs. On the other hand, for HTO sample, a comparable Ga_2O_3 film formed on the GaAs substrate after oxidation at 600 °C and 1atm. [Fig. 4.30 (c)] However unusually substantial Ga-oxide was still remained after sufficient HF etching exposing the Ga-oxide instead of As layer on the GaAs surface. [Fig. 4.30 (d)]

Fig. 4.31 (a) and 4.31 (b) show the Ga 3d and As 3d XPS spectra of the Al_2O_3(2nm)/GaAs substrate, respectively. For APO sample, Ga_2O_3 peak is comparable with control sample. These results agree with the prediction that thin arsenic layer produced by APO cannot block the oxidation of GaAs surface. However, for HTO sample, the significant Ga_2O_3 peak is observed indicating that an adverse Ga_2O_3 layer exists between the Al_2O_3 and GaAs substrates, which is thicker than that of the control sample. This anomalous behavior can be explained by the formation of a Ga suboxide (Ga_2O) as well as Ga_2O_3 during the high temperature oxidation process. It is known that

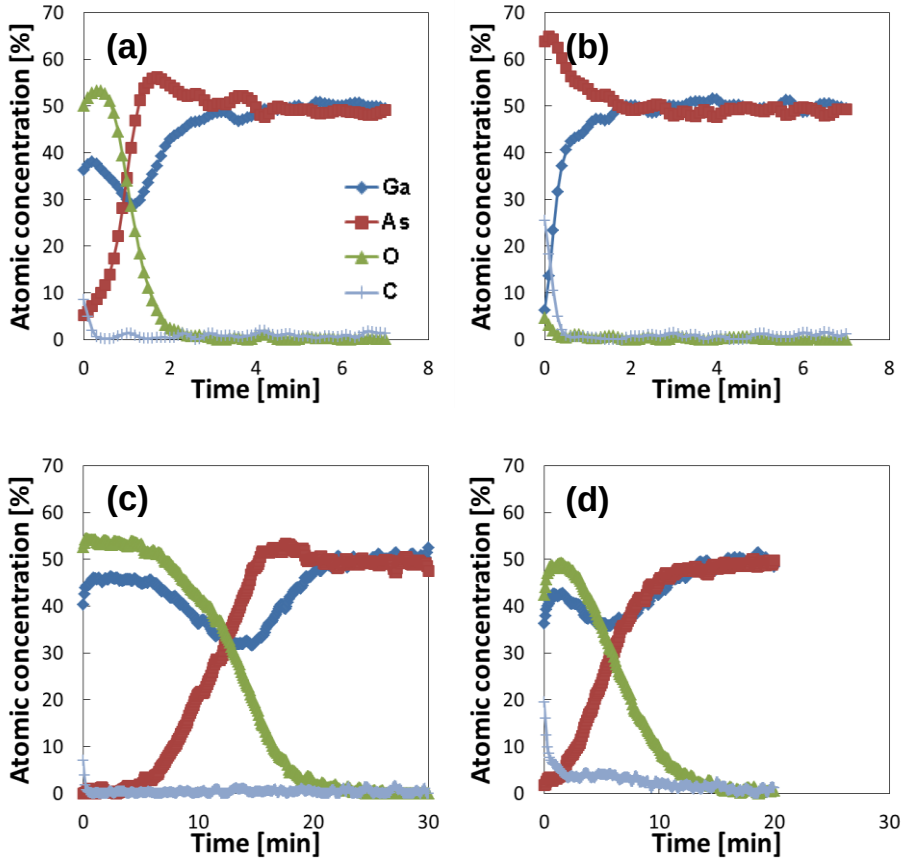


Figure 4.30. AES depth profiles after thermal oxidation and HF wet etching for APO and HTO sample : (a) after APO, (b) after HF etching of APO sample, (c) after HTO, and (d) ater HF etching of HTO sample.

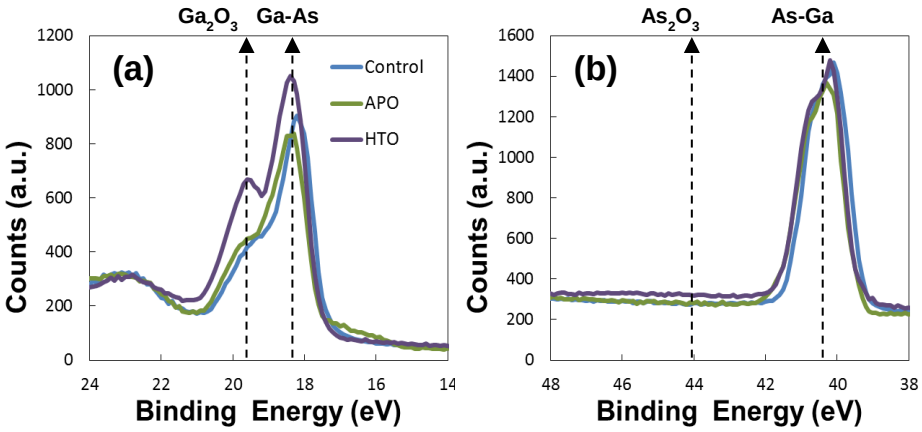


Figure 4.31. (a) Ga 3d and (b) As 3d XPS spectra for APO, HTO and control sample.

Ga_2O_3 can be decomposed to Ga_2O at temperatures higher than 500 °C [62, 129]. The considerable Ga_2O phase of the HTO sample still persisted after subsequent HF etching, which was confirmed by the Ga 3d XPS spectra (not shown). Undissolved Ga-oxide shown in AES profile can be identified as Ga_2O from this result. Hence, a thicker Ga_2O_3 layer for the Al_2O_3/HTO GaAs substrate would be a reflection of the considerable Ga_2O content remaining on the GaAs surface because the remaining Ga_2O is likely to reconvert to Ga_2O_3, even at low temperatures (~200 °C), due to the low thermal stability. Gate oxide deposition or post deposition annealing can provide the sufficient heat to produce the Ga_2O_3 from Ga_2O at the interface. Therefore it can be thought that APO and HTO would not be an effective treatment for passivating the GaAs surface states.

To investigate the passivation effect of APO to have same oxide thickness with HPO, various oxidation conditions changing annealing temperature and time at 1 atm were conducted as envisioned in Fig. 4.32. Thermal oxidation were examined from 400 °C to 550 °C spaced at 50 °C intervals with annealing time of 0.5, 1, 2, and 4 hour. Among these conditions, four samples of 400 °C – 4 hour, 450 °C – 2 hour, 500 °C – 1 hour, and 550 °C – 0.5 hour were selected and analyzed the depth profiles using AES as shown in Fig. 4.33.

Low temperature sample oxidized at 400 °C for 4 hour was almost similar to previous APO sample treated at 400 °C for 0.5 hour in terms of final

Thickness (nm)

Temp \ Time	0.5 h	1 h	2 h	4 h
400°C	3.1	3.4	4.1	5.1
450°C	8.5	11.3	13.9	
500°C	17.7	19.4		
550°C	20.9			

Figure 4.32. Detailed split conditions for thermal oxidation changing temperature and process time. Numbers in table indicate the oxide thickness in nm grown by thermal oxidation. Four samples in red shaded cell were selected to evaluate the electrical properties.

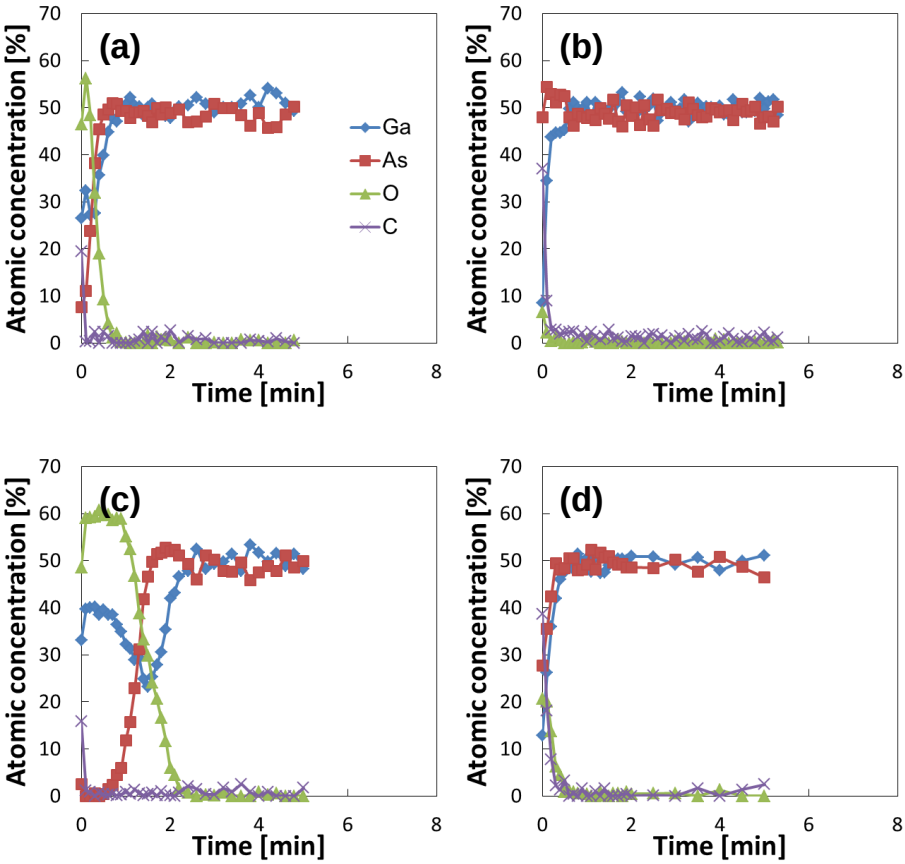


Figure 4.33. AES depth profiles after thermal oxidation in (a), (c), (e), and (g) and subsequent HF etching in (b), (d), (f), and (h): (a), (b) 400℃-4hour, (c), (d) 450℃-2hour, (e), (f) 500℃-1hour, and (g), (h) 550℃-0.5hour.

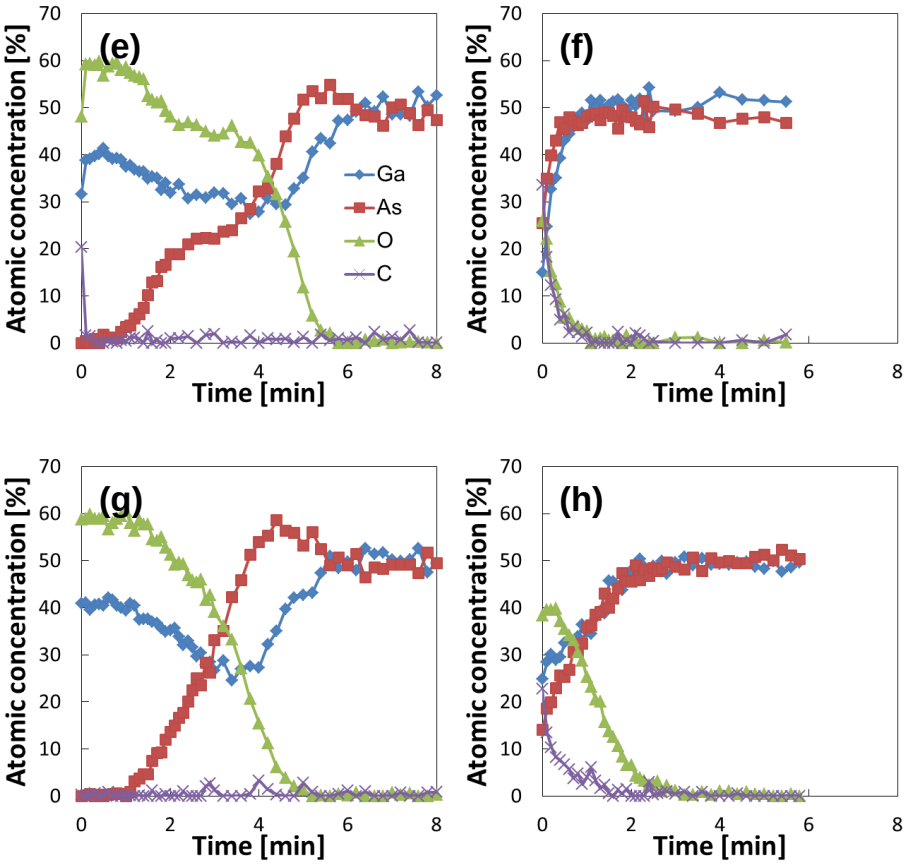


Figure 4.33. Continued.

composition profile after thermal oxidation and HF wet etching as shown in Fig. 4.33 (a) and (b). Because 5nm thick oxide is still insufficient to produce As blocking layer to suppress the oxygen transfer, it is difficult to prevent from the formation of Ga_2O_3 at the interface like APO sample.

High temperature sample oxidized at 550 °C for 0.5 hour shows same structure with HTO sample taken at 600 °C for 0.5 hour leaving the undissolved thick Ga_2O layer on GaAs as shown in Fig. 4.33 (h). This result indicates that the formation of Ga_2O can be initiated at 550 °C or less.

In the case of middle temperatures using 450 and 500 °C, substantial As layers on GaAs surface were expected to be obtained after oxidation and followed HF etching like HPO process because comparable Ga_2O_3 with HPO were formed by these oxidations. However there were little As layers left on the GaAs surfaces as seen in Fig 4.32 (d) and (f). It is well known that the elemental As produced by reaction (4.6) easily diffuse out through the oxide layer and finally escape from the sample due to its high volatility. This process can be accelerated under relatively higher temperature oxidation of 450 °C and 500 °C than HPO treated 400 °C. In addition, evaporation easily occur under relatively low pressure like 1 atm. On the other hand, gas phase is thermodynamically unstable under high pressure of 10 atm, as predicted by Le Chatelier's principle. Therefore high pressure condition in HPO can effectively suppress the As sublimation leading the thick As layer remained at the interface. However low pressure such as 1 atm in the oxidation of 450 °C

and 500 °C cannot prevent from the As evaporation.

From the XPS analysis, there are little differences of Ga_2O_3 amount generated after gate oxide formation among 400 °C, 450 °C, 500 °C and control sample as shown in Fig. 4.34. For these annealed samples, As layer were insufficiently obtained or disappeared through sublimation at the interface during oxidation as mentioned above. Therefore there is a limit to suppress the formation of Ga_2O_3 during gate oxide formation like control sample. The 550 °C sample shows higher peak of Ga_2O_3 than control sample like HTO. Similarly it can be explained by interfacial thick Ga_2O layers formed during the oxidation which tend to transit to Ga_2O_3 due to subsequent following thermal process like gate oxide formation or PDA.

Electrical results are also consistent with AES and XPS analysis as shown in Fig. 4.35. C-V behaviors of 400 °C, 450 °C, and 500 °C oxidized samples are comparable to the previous APO and control sample indicating that there are no passivation effects. For 550 °C sample, the dispersion property significantly deteriorates as shown in Fig. 4.35 (d).

In conclusion, it is proved that only high pressure oxidation can provide the effective interfacial passivation through the formation of substantial As-rich and Ga-deficient layer on GaAs leading the suppression of Ga_2O_3 at the interface.

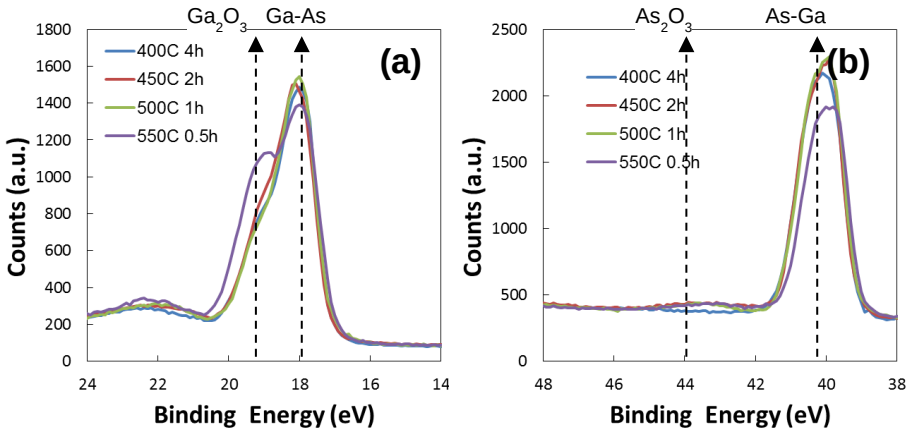


Figure 4.34. (a) Ga 3d and (b) As 3d XPS spectra for four different annealed samples: 400℃-4hour, 450℃-2hour, 500℃-1hour, and 550℃-0.5hour.

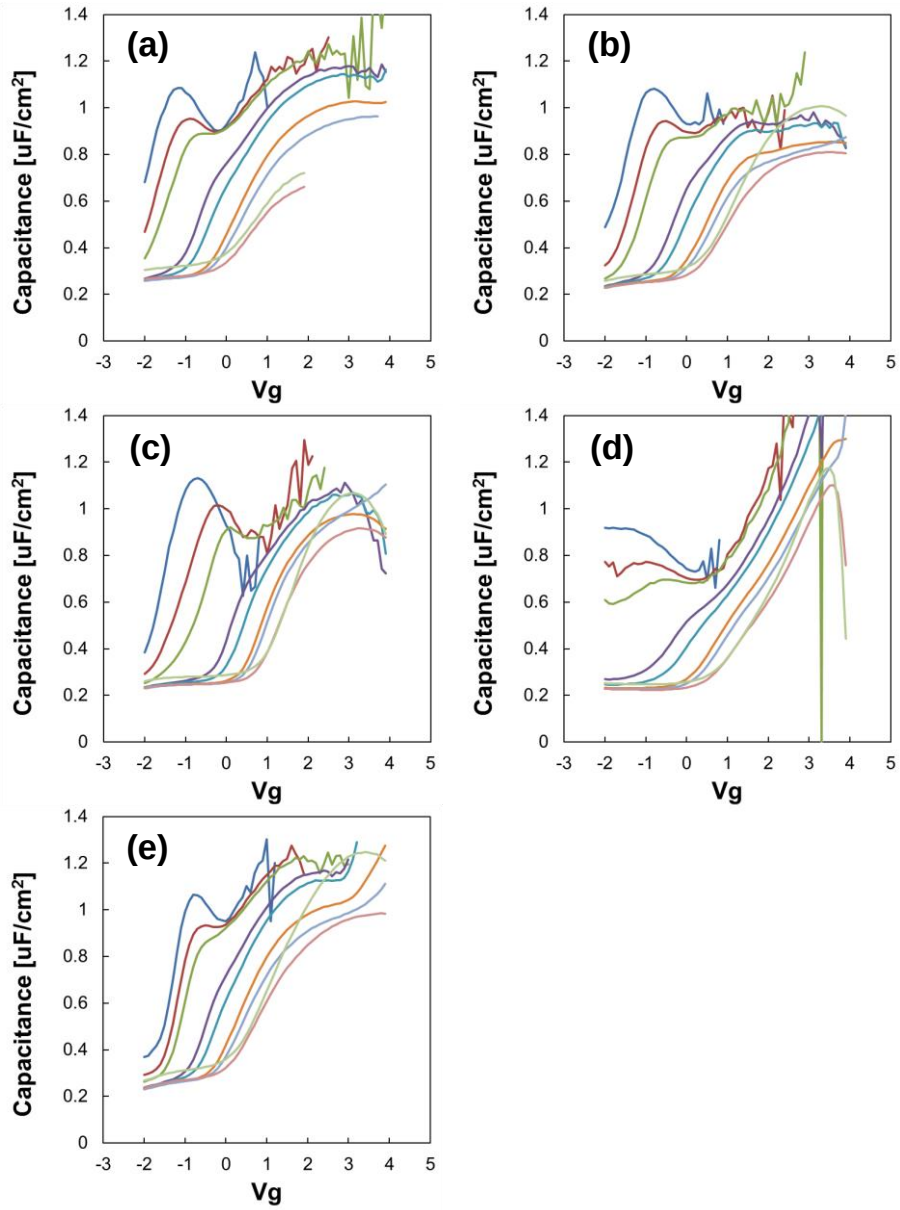


Figure 4.35. C-V frequency dispersions measured at 125° for (a) 400℃-4hour, (b) 450℃-2hour, (c) 500℃-1hour, (d) 550℃-0.5hour, and (e) control sample.

4.4. Passivation of GaAs using Ti scavenging effect

4.4.1. Effects of insertion of Ti film on electrical characteristics

In order to examine Ti scavenging effect, thin Ti film inserted MOS capacitors at the Al_2O_3-GaAs interface ($Pt/Al_2O_3/Ti(O_2)/GaAs$) were fabricated and compared to control samples ($Pt/Al_2O_3/GaAs$) in terms of C-V and G-V measurements. For the Ti inserted capacitors, metal Ti films were prepared by e-beam evaporation under ultrahigh vacuum of 10^{-6} torr order. Nevertheless, metal Ti films are expected to be fully oxidized during subsequent thermal process such as Al_2O_3 deposition or post deposition annealing of 550 ℃ or even air exposure due to its strong oxygen affinity [15]. The normal features of C-V curves for Ti inserted samples tell us that metal Ti converted to TiO_2 performing a role of a gate dielectric layer. In next part, XPS analysis for Ti 2p will be given to verify the Ti chemical status.

Fig. 4.36 shows the frequency dispersion behaviors at room temperature for Al_2O_3 and $Al_2O_3/Ti(O_2)$ as MOS gate dielectric films. Better frequency dispersion properties were obtained for $Al_2O_3/Ti(O_2)$ compared to Al_2O_3. Especially at 125 ℃ the improvement of the frequency dispersions clearly appeared in Fig. 4.37. Since the electrical characteristics are primarily dependent on interfacial dielectric materials as mentioned in the previously, it can be easily expected that these results are due to the different interfacial

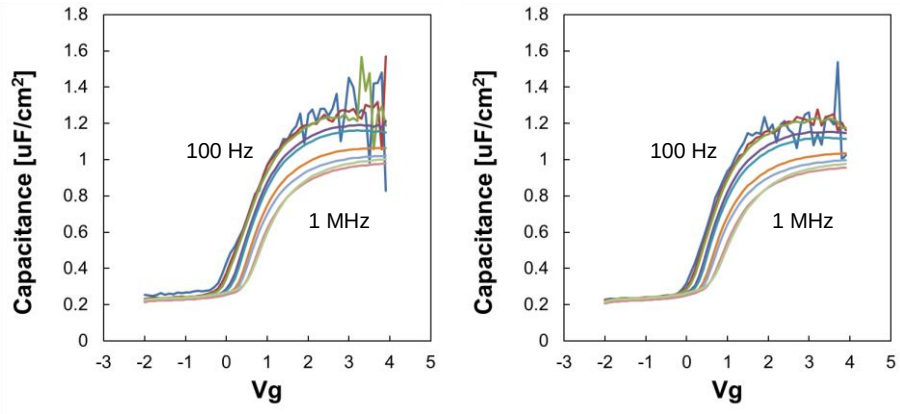


Figure 4.36. C-V frequency dispersions measured at 25° for (a) control sample and (b) Ti inserted sample.

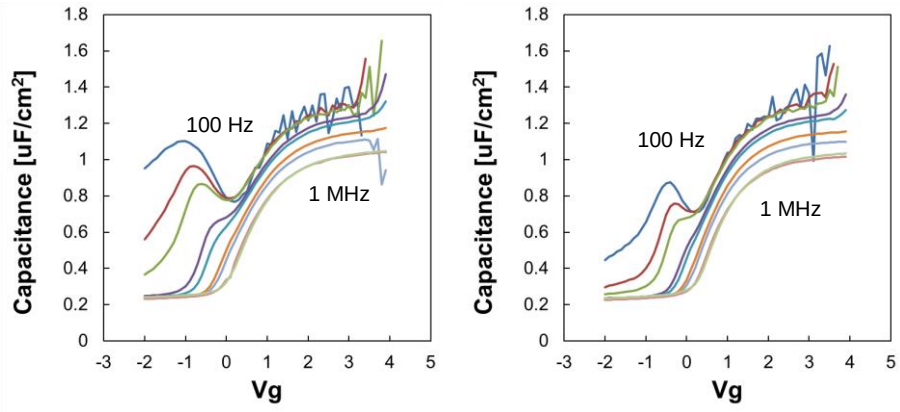


Figure 4.37. C-V frequency dispersions measured at 125° for (a) control sample and (b) Ti inserted sample.

oxides: Al_2O_3 and TiO_2.

Because the dispersions are closely correlated by the interface states, the amounts of D_{it} are also expected to show same trend with the dispersion results. In Fig. 4.38, D_{it} distributions as a function of energy level were extracted by conductance methods. For the Ti inserted sample, overall D_{it} in the upper half band gap decreases down to 6.6×10^{12} $cm^{-2}eV^{-1}$ at E_i + 2.3 eV while the control sample exhibits 2.4×10^{13} $cm^{-2}eV^{-1}$ at the same energy. Especially significant improvements near mid-gap region measured at 125℃ are obtained as already predicted from the frequency dispersion results.

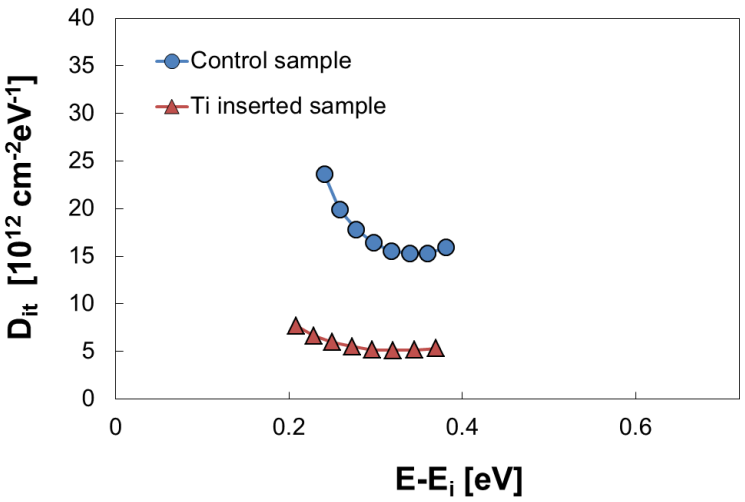


Figure 4.38. D_{it} distribution profiles with trap energy measured at 125 ℃ for control sample and Ti inserted sample.

4.4.2. Interfacial analysis of Ti passivated surface

In order to evaluate the effects of Ti insertion at GaAs interface, the analysis of chemical bonding state were carried out using XPS. Four different structure samples of Ti(2nm)/GaAs, Al_2O_3(1nm)/Ti(1nm)/GaAs, Ti(1nm)/Al_2O_3(1nm)/GaAs and Al_2O_3(2nm)/GaAs were prepared using e-beam evaporation and ALD for Ti and Al_2O_3 respectively. Post deposition annealings were applied to all samples under N_2 ambient at 550 ℃.

Fig. 4.39 (a) shows the Ti 2p spectra for three samples except Al_2O_3(2nm)/ GaAs. The peaks for Ti metallic bonding near 454 eV are not shown while strong TiO_2 related peaks are found at 459 eV. Therefore all Ti films are confirmed to be oxidized regardless of the location of the Ti films. Especially from XPS data in Ti(2nm)/GaAs sample, Ti oxidation seems to occur by only air exposure without Al_2O_3 deposition. Fig. 4.39 (b) shows Ga 3d spectra for all samples. For Ti(1nm)/Al_2O_3(1nm)/GaAs and Al_2O_3(2nm)/ GaAs samples, Ga_2O_3 peaks clearly appear at ~1eV above the Ga-As bulk peaks. However, for Ti(2nm)/GaAs and Al_2O_3(1nm)/ Ti(1nm)/GaAs samples where Ti films were directly deposited on GaAs in common, Ga_2O_3 peaks are found to be significantly suppressed. If the Ti film is included in MOS capacitors but not in immediate contact with GaAs such as Ti(1nm)/Al_2O_3(1nm)/GaAs, formation of substantial Ga_2O_3 at GaAs interface cannot be avoided.

Since the Ti has higher oxygen affinity than Ga, oxygen bonded with Ti cannot break the bonding and migrate to substrate to form Ga_2O_3. In addition,

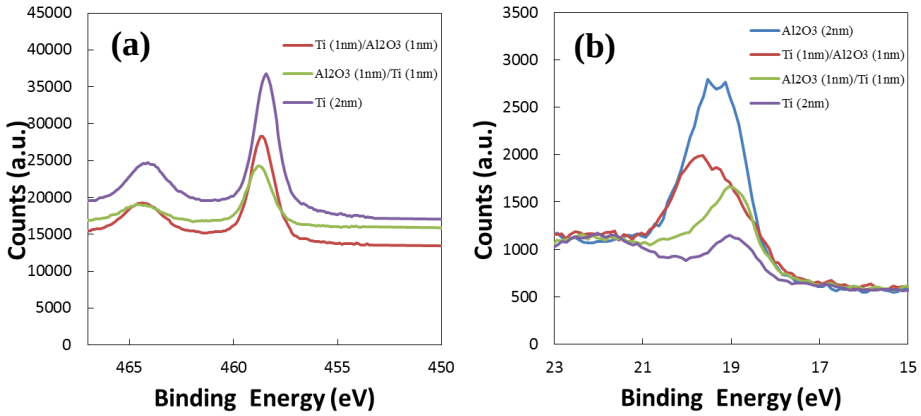


Figure 4.39. XPS spectra showing (a) Ti 2p for Ti(1nm)/Al_2O_3(1nm), Al_2O_3(1nm)/Ti(1nm), and Ti(2nm) and (b) Ga 3d for Al_2O_3(2nm), Ti(1nm)/Al_2O_3(1nm), Al_2O_3(1nm)/Ti(1nm), and Ti(2nm).

oxidized Ti (TiO_2) can effectively block the oxygen transfer from upper Al_2O_3 film to GaAs substrate. It can be also thought that low oxidation states in Ti oxides even tend to absorb the oxygen from the interfacial Ga_2O_3 leading to reduction of Ga_2O_3. These facts can support the improved electrical properties for Ti inserted sample.

Of course, this effect is expected to be achieved by insertion of another species having the high oxygen affinity to suppress the Ga_2O_3 formation.

5. Conclusions

Electrical characterizations of GaAs MOS devices were examined to evaluate the interface states. Significant frequency dispersions in depletion region at high temperature suggest that higher density of interface states exist near the mid-gap. Large hysteresis were generally observed in GaAs due to deep level states such as mid-gap with long emission time constant of the order of 10^3 second. Consistent results were also obtained in the D_{it} distribution, extracted from conductance method. It was confirmed that huge interface states more than $x10^{13}$ $cm^{-2}eV^{-1}$ was observed in the mid-gap region not band edge unlike Si showing the U-shape profiles.

In order to investigate the interfacial degradation mechanisms in GaAs, the effects of Ga oxide were evaluated by insertion of Ga_2O_3 at Al_2O_3–GaAs interface. For the MOSCAPs using Al_2O_3/Ga_2O_3, huge C-V frequency dispersions in depletion region at 125 ℃ appeared compared to the MOSCAPs using single Al_2O_3 while slightly larger dispersions were observed in accumulation region at 25 ℃. In addition, the Al_2O_3/Ga_2O_3 samples also showed two times larger hysteresis of C-V curves compared to the control Al_2O_3 sample. In the measurements of Fermi level movement efficiency as a criterion of Fermi level pinning, the Al_2O_3/Ga_2O_3 sample showed 25% efficiency which is significantly lower than the Al_2O_3 sample of 44%. Consistent results were also obtained in the D_{it} measurements, which showed

1.8 x 10^{13} $cm^{-2}eV^{-1}$ and 9.1 x 10^{12} $cm^{-2}eV^{-1}$ for Al_2O_3/Ga_2O_3 and Al_2O_3 samples, respectively, at the same energy level of E_i + 0.27 eV. These results indicate that higher interface states in deep level near mid-gap can arise from Ga_2O_3 at the interface. It can be also supported by the fact that different electrical results according to dielectric materials could be correlated with the amount of interface Ga_2O_3 which can be naturally formed during thermal process. Therefore, suppression of Ga_2O_3 formation is essential for improvement of interface characteristics.

For the passivation of GaAs interface, high-pressure oxidation (HPO) treatment on GaAs substrate was carried out at 10 atm in O_2 ambient followed by HF oxide removal. Frequency dispersion at the depletion range at 125 ℃ was significantly improved. C-V hysteresis was also improved by 45%. Significant reduction of mid-gap D_{it} was observed down to 3.4 x 10^{12} $cm^{-2}eV^{-1}$ at E_i + 0.25 eV, which was less than half level of un-passivated samples. From the XPS and AES analysis, HPO and subsequent HF etching can induce selective Ga oxidation and removal of Ga_2O_3 leading As excess and Ga deficient surface which can effectively suppress the Ga_2O_3 formation. Therefore it can be concluded that improvement of interfacial characteristics of the HPO-passivated samples is ascribed to reduction of defective Ga_2O_3 at the interface. In addition, from the experiments using various oxidation conditions changing pressure and temperature, high pressure and low temperature process such as HPO is verified to be more effective way to passivate the interface.

As another passivation approach, insertion of Ti film between gate oxide and GaAs substrate was tried. Ti is expected to tend to strongly absorb the oxygen atoms and block the oxygen transfer due to its high oxygen affinity. For Ti inserted samples, reduction of hysteresis and interface states by ~40% were also obtained. These results can be explained by the amounts of Ga_2O_3 at the interface. From the XPS analysis of Ga 3d, it was confirmed that less Ga_2O_3 was detected and this reduction of Ga_2O_3 was attributed to Ti scavenging effect.

In conclusion, high pressure oxidation and insertion of Ti scavenging film are proved as effective ways to passivate the GaAs interface for controlling the formation of Ga_2O_3 at the interface.

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1. Journals (SCI)

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2. Proceeding

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3. Conference

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4. Patent

-발명 명칭: 고압 산소 열처리를 이용한 III-V 화합물 반도체의 MOS 소자 제조 방법

한국 출원: 반도체 장치 및 그 제조방법 (P20140154660)

미국 출원: Semiconductor device and method of fabricating the same (in progress)

국문초록

GaAs는 높은 전자 이동도와 상대적으로 큰 밴드 갭을 가지고 있어서 기존 Si 소자 대비 고속 동작과 저전력 소모라는 많은 장점을 가지고 있고, 이로 인해 최근에는 10nm 이하 로직 MOSFET 소자의 채널 물질로 많은 주목을 받아 왔다. 그러나 지난 30여년간의 오랜 연구에도 불구하고 GaAs MOSFET 소자를 구현하기 위해서는 해결해야 할 많은 문제들이 산적해 있는 상황이다. 그 중에서 GaAs 산화막의 열적 불안정성이 가장 중요한 이슈로 평가될 수 있다. 이러한 열적 불안정성은 높은 계면 준위를 유발하게 되는데, 이는 결국 페르미 준위 고정과 C-V 주파수 분산 특성의 열화로 나타나게 된다.

본 연구에서는 GaAs와 다양한 게이트 유전막을 이용하여 MOS 캐피시터를 제작하였으며 이를 통해, C-V 곡선의 이력 현상, 주파수 분산 특성, 페르미 준위 이동 효율, 계면 준위 밀도와 같은 전기적 특성 평가를 실시하였다. 특히 깊은 준위의 계면 준위 밀도를 측정하기 위해 125 ° C까지 증가된 온도에서 C-V 및 G-V 측정을 실시 하였다. 또한, GaAs 계면에서 나타나는 조성 및 구조에 대한 논의를 위해 XPS, AES, TEM과 같은 표면 분석이 진행 되었다.

먼저 GaAs MOS 소자의 계면 특성 분석을 위한 전기적 평가를 진행하였다. 125 ° C의 고온에서는 C-V 공핍 영역에서 주파수 분산 특성의 열화가 발견되었으며 이는 미드갭(midgap) 영역에서 높은 계면 준위 밀도가 존재함을 보여주는 것으로 해석될 수 있다. 이와 같은 결과는 컨덕턴스 방식을 통해 추출한 계면 준위 분포와도 일치하였다. 미드갭에 해당하는 에너지 대역에서 10^{13} $cm^{-2}eV^{-1}$

이상의 매우 높은 계면 준위 밀도가 측정되었으며 밴드갭의 양쪽 가장자리로 갈수록 감소하는 형태를 보이는데 이는 U 형태의 프로파일을 보이는 Si과는 전혀 다른 거동이라고 할 수 있다.

미드갭 영역에서 높은 계면 준위가 발생하는 원인을 규명하기 위해서 계면에서 Ga 산화막이 주는 영향에 대해 평가하였다. 게이트 절연막 형성 전에 얇은 Ga_2O_3 박막을 인위적으로 삽입한 형태의 시편을 제작하여 분석한 결과 그렇지 않은 시편에 비해 2배 이상의 C-V 이력 현상이 나타나고 고온에서는 높은 주파수 분산 특성이 관찰되었다. 이와 같은 결과로 미루어, Ga_2O_3는 미드갭 영역에서 계면 준위를 유발하는 결함으로 작용한다는 사실을 확인하였다. 다양한 high-k 유전막을 사용하여 제작한 GaAs MOS 캐패시터에서 서로 다른 정도의 계면 준위가 나타나는 현상이 각 high-k 박막마다 계면에서 생성되는 Ga_2O_3 자연 산화막의 양과 관련 있다는 사실이 이러한 결과를 뒷받침할 수 있다.

다음으로 GaAs 계면의 패시베이션(passivation)을 위해 고압 산소 열처리와 Ti 스캐빈징(scavenging) 삽입층을 이용한 공정을 도입함으로써 Ga_2O_3 생성을 억제하고자 하였다. 고압 산소 열처리 적용시 미드갭 근처의 계면 준위가 $3.4 \times 10^{12}\ cm^{-2}eV^{-1}$ at $E_i + 0.25$ eV와 $6.2 \times 10^{12}\ cm^{-2}eV^{-1}$ at $E_i - 0.2$ eV 수준으로, 이는 패시베이션을 처리하지 않은 시편에 비해 약 1/2 정도로 감소된 결과임을 확인하였다. 이러한 개선은 고압 산소 열처리를 통해 GaAs 기판 상부의 조성이 As > Ga으로 변화된 사실로 설명할 수 있다. 고압 산소 열처리를 실시할 경우 GaAs 표면에서는 Ga_2O_3와 원소상태의 As 층이 두껍게 형성되는데, 이후 불산 에칭 공정을 통해 Ga_2O_3 박막을 선택적으로 제거하면 표면에는 As 층이 남게 되면서 처음과는 다른 조성의

표면을 얻게 된다. 이 경우, 기판으로 산소의 이동을 차단하기 때문에 후속 공정을 통해 생성될 수 있는 Ga_2O_3 계면층이 효과적으로 억제될 수 있다. 이 때, 높은 압력에서 산화하는 경우 낮은 압력에 비해 더 많은 As 층을 표면에 형성할 수 있기 때문에 계면 패시베이션을 더 효과적으로 수행할 수 있음도 확인하였다.

Ti 삽입층 이용한 패시베이션의 경우는 C-V 이력 특성과 계면 준위가 약 40% 감소하는 결과를 얻을 수 있었다. XPS 분석을 통해 Ti 스캐빈징 삽입층을 적용한 시편에서 Ga_2O_3의 생성이 감소된 사실이 확인 되었다. 이와 같은 결과로 미루어 Ti의 높은 산소 친화도에 기인한 스캐빈징 효과가 Ga_2O_3 생성을 억제하는 것으로 판단된다.

따라서 고압 산소 열처리와 Ti 스캐빈징 삽입층을 적용한 계면 처리는 Ga_2O_3 계면층의 생성을 억제하면서 GaAs 표면을 효과적으로 패시베이션할 수 있는 공정임을 결론지을 수 있다.

주요어: 갈륨비소, 갈륨 산화막, 비소 원소, 계면 준위,
고압 산소 열처리, 스캐빈징 효과

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