Ph. D. DISSERTATION

Interface Sulfur Passivation for Advanced MOSFETs with High Mobility Channel Materials

by

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Abstracts

Approaching with speed limit for nano-electronic device built on Si substrates, III-V compound semiconductor/Ge with a high mobility are gaining great interests to replace the Si substrate. However, the growth of interfacial layer (IL) between the gate insulator and III-V compound semiconductor/Ge substrate, which deteriorates the interfacial property, is still a critical problem.

Passivating the interface of gate insulator (GI)/III-V and Ge substrates using sulfur (S) has been known to effectively suppress the interfacial layer growth and to improve the electrical properties of interface. Among the various methods for sulfur passivation, $(NH_4)_2S$ solution treatment was commonly adopted because of simplicity of the process for laboratory experiments. However, the S passivation using $(NH_4)_2S$ solution may not be appropriate for industrial mass-production since it is a wet chemical approach which can cause non-uniform S distribution on the substrate, difficulty in controlling S concentration, and surface residues of contaminants. Pre-deposition annealing of the substrate under H_2S atmosphere is believed to be an appropriate method for replacing the S passivation using $(NH_4)_2S$ solution wet process.

In this work, the feasibility to replace the wet-process using $(NH_4)_2S$ solution with the dry-process by annealing under H_2S atmosphere was examined for the interface S passivation in metal-insulator-semiconductor capacitor (MISCAP) devices fabricated on Ge substrate. Atomic-layer-deposited (ALD) HfO_2 film was grown on Ge substrate after surface S passivation. The H_2S annealing provided uniform distribution over Ge surface and solid S passivation with the strong resistance against oxidation during ALD process.

The electrical thickness of the gate insulator by S passivation decreased and interface state density near the valence band edge suppressed, as the annealing temperature increases, because thermal energy during the annealing resulted in stronger S bonding and Ge surface reconstruction. Moreover, the hysteresis was lower for the device with H_2S annealing at 400 °C.

Surface Sulfur(S) passivation on InP substrate was performed using a dry process - rapid thermal annealing under H_2S atmosphere for III-V compound-semiconductor-based devices. In order to minimize thermal degradation of the InP compound semiconductor surface, rapid thermal annealing (RTA) was a good process under the H_2S environment. The electrical properties of metal-oxide-semiconductor capacitor fabricated with atomic-layer-deposited HfO_2 film as a gate insulator were examined, and were compared with the similar devices with S passivation using a wet process-$(NH_4)_2S$ solution treatment. The H_2S annealing provided solid S passivation with the strong resistance against oxidation compared with the $(NH_4)_2S$ solution treatment, although S profiles at the interface of HfO_2/InP were similar. The decrease in electrical thickness of the gate insulator by S passivation was similar for both methods. However, the H_2S annealing was more effective to suppress interface state density near the valence band edge, because thermal energy during the annealing resulted in stronger S bonding and InP surface reconstruction. Moreover, the flatband voltage shift by constant voltage stress was lower for the device with H_2S annealing.

Atomic-layer-deposited Al_2O_3 films were grown on ultrathin-body $In_{0.53}Ga_{0.47}As$ substrates for III-V compound-semiconductor-based devices. Interface sulfur (S) passivation was performed with wet processing using ammonium sulfide ($(NH_4)_2S$) solution, and dry processing using post-deposition annealing (PDA) under a H_2S atmosphere. The PDA under

the H_2S atmosphere resulted in a lower S concentration at the interface and a thicker interfacial layer than the case with $(NH_4)_2S$ wet-treatment. The electrical properties of the device, including the interface property estimated through frequency dispersion in capacitance, were better for $(NH_4)_2S$ wet-treatment than the PDA under a H_2S atmosphere. They might be improved, however, by optimizing the process conditions of PDA. The PDA under a H_2S atmosphere following $(NH_4)_2S$ wet-treatment resulted in an increased S concentration at the interface, which improved the electrical properties of the devices.

Keywords: ALD, High-k, High mobility channel, MOSFETs, Interface passivation

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List of Abbreviations

CMOSFETs Complementray Metal-Oxide-Semiconductor Field Effect Transistors

MIS Metal-Insulator-Semiconductor

ALD Atomic Layer Deposition

PDA Post Deposition Annealing

RTA Rapid Thermal Annealing

CET Capacitance Equivalent Thickness

C-V Capacitance-Voltage

V_{FB} Flatband Voltage

XPS X-ray Photoelectron Spectroscopy

HRTEM High Resolution Transmission Electron Microscopy

HRSTEM High Resolution Scanning Transmission Electron Microscopy

EDS Energy-dispersive X-ray Spectroscopy

ToF-SIMS Time of Flight-Secondary Ion Mass Spectroscopy

AFM Atomic Force Microscopy

D_{it} Interface state density

Chapter 1. Introduction

1.1 Power crisis in multi-core CPU era

During the past four decades, the integration density of logic circuits have been increased exponetially ("Moore's law"), powered by exponential reductions in MOSFET device size. Despite theses changes, silicon oxide, usually grown by simple exposure to oxygen gas or water vapor at elevated temperatures, until recently remained the gate insulator of choice. Its success has been based on the worderful properties of the silicon/silicon dioxide interface. This interface has only about $10^{12}/cm^2$ electrically active defects. And after a simple passivating hydrogen exposure, $10^{10}/cm^2$ defects remain - only one defect for every 100,000 interface atoms!

Reducing of the MOSFET gate length has required simultaneous scaling of other geometrical and electronic device parameters, such as gate insulator thickness, threshold and supply voltages, and body doping ("Dennard's scaling theory"). Over the last decade, the transistor architecture has undergone significant changes with the introduction of strained silicon at 90nm node [7] and HfO_2 gate dielectric (replacing SiO_2) with a metal gate (replacing poly-silicon) at the 45nm node [8]. Strain in the Si MOSFET channel results in higher carrier mobility, thus significantly boosting its ON state performance while HfO_2 with a higher dielectric constant(~ 25 compared to 3.9 for SiO_2) and gate dielectirc thickness has allowed stronger gate coupling with the channel and an exponetially reduced gate tunneling leakage. The use of metal gate electrode has increased the channel mobile charge concentration by eliminating the poly-silicon depletion, thereby resulting in higher drive current.

However, sustaining this historical complementray MOS (CMOS) scaling trend has become increasingly challenging. Voltage scaling slowed down dramatically as supply voltages approached 0.8V, due to contraints on the threshold voltage needed to limit source-to-drain leakage in the transistor "off"state. In addition, SiO_2 or silicon oxynitride(SiON) gate

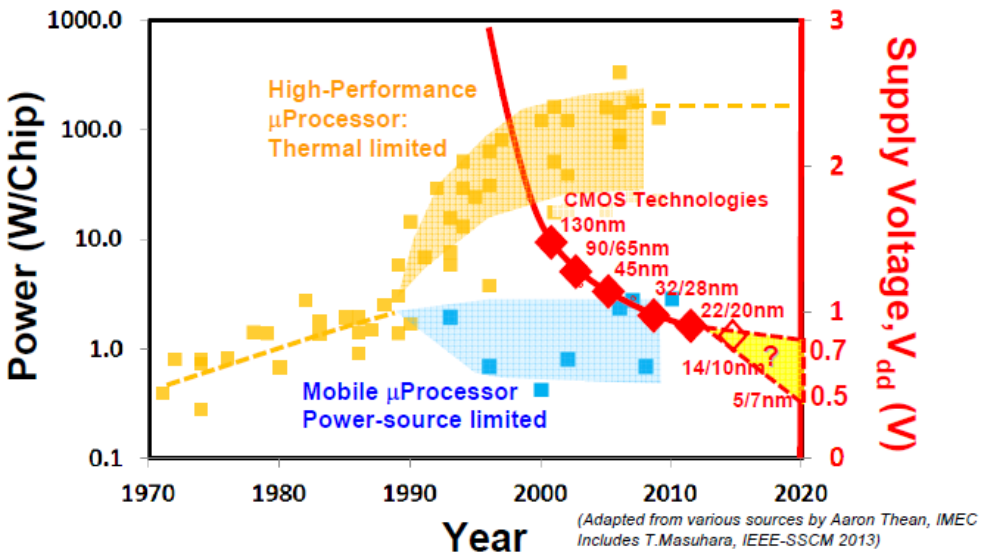


Figure 1.1 Power density and suppy voltage trends of microprocessors are plotted along with scaling (from industry data).

dielectric scaling has all but stopped at thicknesses close to 10A, as the gate leakage currents due to quantum mechanical tunneling through this "insulator" have reached values of >100A/cm^2 in transistors aimed at high performance applications, e.g., in servors. This causes computer chips to generate heat with power densities of 100W/cm^2 or more, making chip cooling technologically challenging and costly. Scaling of the gate oxide in low-power circuits, e.g., for cell phones, has reached its limit already near 20A, to ensure substantially lower gate leakage

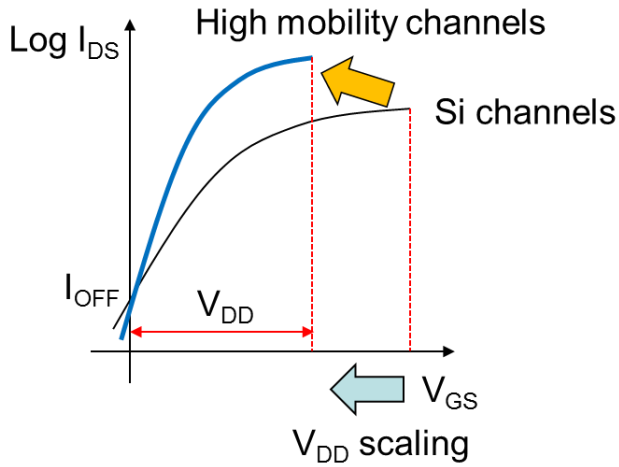


Figure 1.2 Schematic diagram of log I_{DS}(current) – V_{DD}(supply voltage) of MOSFETs.

Table 1.1 Physical properties of common group IV and III-V semiconductors.

Material / Property	IV – IV		III - V					
	Si	Ge	InP	GaAs	$In_{0.5}Ga_{0.5}As$	GaSb	InAs	InSb
Elec. mobility (cm^2 / V·sec)	1 400	3 900	5400	8 500	12 000	3000	40 000	77 000
Electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0.98	m_t: 0.082 m_l: 1.6	0.082	0.067	0.041	0.041	0.023	0.014
Hole mobility (cm^2 / V·sec)	450	1 900	200	400	450	1000	500	850
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.33 m_{LH}: 0.043	m_{HH}: 0.6 m_{LH}: 0.089	m_{HH}: 0.51 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.052	m_{HH}: 0.4 m_{LH}: 0.05	m_{HH}: 0.41 m_{LH}: 0.026	m_{HH}: 0.43 m_{LH}: 0.015
Bandgap (eV)	1.11	0.67	1.34	1.42	0.74	0.72	0.36	0.17
Lattice parameter (A)	5.431	5.658	5.868	5.653	5.868	6.095	6.058	6.479

and thereby sufficient battery life.(Fig. 1.1)

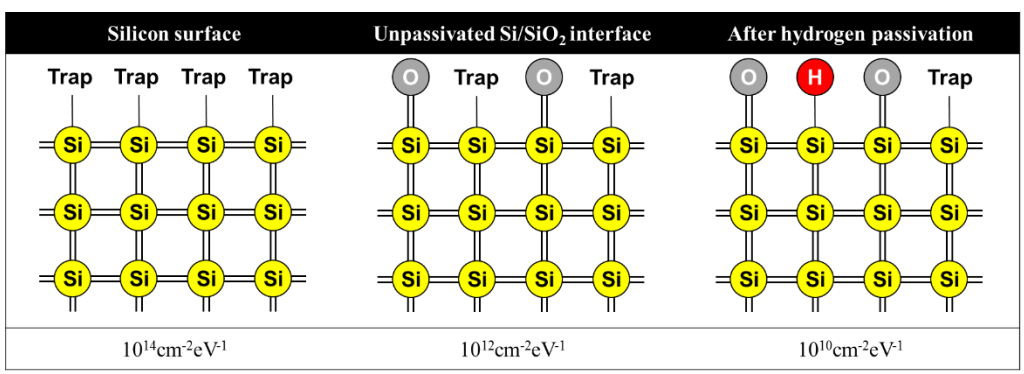
For the 14nm node and beyond a host of new devices/materials are being investigated, trying to address this most critical bottleneck to transistor scaling i.e. power dissipation, both static and dynamic. Some of the alternatives being actively pursued for future technology nodes are th Tri/Multi-Gate device architectures [10], alternate channel materials with multi-gate FETs (III-V and strained Ge quantum wells and FETs)[11], super-steep sub-threshold slope transistors(sub-60mV/dec) [12][13][14][15], carbon-nanotube/graphene based FETs[16] and spin FETs[17]. Among them multi-gate FETs using alternativec channel materials with a high mobility like III-V compound semiconductors and Ge are the most promising.(Fig.1.2 and Table 1.1)

1.2 Passivation in SiO_2/Si

The silicon atom possesses four valence electrons and therefore requires four bonds to fully saturate the valence shell. In the crystalline structure each silicon atom establishes bonds to its four neighboring atoms, leaving no unsaturated bond behind. At the surface of the silicon crystal atoms are missing and traps are formed as shown in Figure 1.3. The density of these interface states, D_{it} , in this regime is approximately D_{it}~10^{14} $cm^{-2}eV^{-1}$. After oxidation most interface states are saturated with oxygen atoms (Table 1.2). The density is then approximately D_{it}~$10^{12}cm^{-2}eV^{-1}$ [18].

This number is already a major improvement of the interface quality. But in an MOS transistor with a gate length of 100nm and a gate width of 1um this density still translates to 1000 dangling bonds. With such a high number of interface defects a transistor would still not operate properly. Therefore, it is mandatory to increase the quality of the Si/SiO_2 interface in MOS device technology as much as possible. Each electrically active interface state leads to degradation of important transistor parameters such as the threshold voltage, the on-current, or the surface carrier mobility. To further improve the interface, the number of dangling valence bonds is further reduced by annealing the interface in forming gas with hydrogen atoms, as shown in Figure1.3. The dangling silicon bonds are passivated by forming Si-H bonds. With this treatment the amount of electrically active interface states can be reduced to around Dit~10^{10} $cm^{-2}eV^{-1}$.

Table 1.2 The interface passivation in silicon



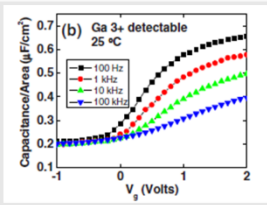
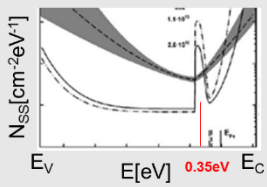
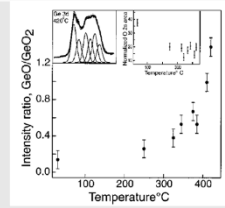
1.3 sulfur passivation at the interface of high-k/high mobility channels

Unlike silicon, native oxide of III-V semiconductors and Ge shows poor passivation properties.(Table. 1.3) During the thermal annealing process above 400 °C, GeO_2 reacts with substrate Ge through the Ge + GeO_2 → 2GeO reaction[37]. Since the GeO has volatile

property, it decomposes to Ge ion and oxygen vacancy. Subsequently, Ge ions and oxygen vacancies are diffuse out through the GeO_2 and dielectric layer. During these processes, large amount of interface defect can be formed. The high density of interface trap causes many problems to MOS device, such as large surface leakage current, carrier mobility degradation, threshold voltage increases. Like Ge, III-V semiconductors (InP , InGaAs, and so on) have poor native oxide for passivating their surface, as well.[37-40](Table 1.3)

Passivating the interface between the gate insulator (GI) and the III-V compound substrates using sulfur (S) has been known to be effective for improving the interfacial

Table 1.3 Issues on the interface passivation in III-V semiconductors and Ge with a high mobility.

	InGaAs	InP	Ge
Stable oxides	Ga_2O, **Ga_2O_3**,$GaAsO_4$,In_2O_3, In_2AsO_4, As_2O_3, As_2O_5	$InPO_4$, In_2O_3,P_2O_5, **P_2O_3(volatile)**	GeO_2, **GeO (volatile)**
Property in GI/Semiconductors	• High D_{it}, Due to As-As, In-In, and Ga-Ga dimers and **Ga_2O_3 (Ga^{3+} state)**	• Native oxide: InOx/$InPO_4$(3nm)/InP • **gap state @ 0.35eV** below CBM(due to P vacancy)	• **Thermal instability** - interface decomposition (Ge + GeO_2 → 2GeO↑@400℃) • Thick GeO_2 → High CET
			
	APL,94, Hinkle et al.(2009)	App. Surf. Sci.,254, Tomkiewicz et al.(2008)	APL,76, Prabhakaran et al.(2000)

properties in metal-insulator-semiconductor (MIS) devices based on III-V compound semiconductor substrates. The S at the interface between the GI and III-Vs plays an important role: that of passivating the surface-dangling bonds so as to reduce the electrical defects at the interface, and suppressing undesirable interfacial-layer (IL) growth. [19-25] One of the commonly adopted methods of incorporating S onto the interface is wet-treating the III-V substrates in a $(NH_4)_2S$ solution.[26-28] S passivation using $(NH_4)_2S$ solution, however, is not appropriate for industrial mass production because S bonding on the substrate surface is

unstable in the atmosphere, and the S is likely to be sensitively released from the surface depending on the process variables, such as the temperature, air exposure time, and pressure.(Table 1.4 and Fig. 1.3) Therefore, various methods for S incorporation into the interface need to be studied.[29, 30] Among them, the post-deposition annealing (PDA) of the GI films grown either under a H_2S atmosphere or with S powder in the annealing chamber [31, 32] can be a feasible candidate for replacing wet processing using a $(NH_4)_2S$ solution with simple dry processing. S could be accumulated at the interface after PDA due to the stress at the interface between the dielectric film and the substrate, which is similar to the case of the nitrogen accumulated at the interface between the SiO_2 GI and the Si substrate after PDA under NH_3, N_2O, etc.[33-36]

1.4 Scopes and organiztions

This dissertation is organized in the following chapters involving the sulfur passivation at the interface of high-k/semiconductors like Ge, InP, and InGaAs.

Chapter 2 presents the investigation about interface sulfur passivation at the interface of HfO_2/Ge using the H_2S RTA as a pre-annealing and $(NH_4)_2S$ solution pre-treatment, respectively. We report the interface reaction between ALD HfO_2 films and S-passivated Ge channel materials during ALD and the electrical characteristics of TiN/HfO_2/S-passivated Ge

Table 1.4 The physical properties of $(NH_4)_2S$ solution and H_2S gas, and process conditions for sulfur passivation.

	$(NH_4)_2S$ solution	RTA under $H_2S(5\%)/ N_2(95\%)$
appearance	Liquid (pH 11.5~7)	Gas
Process time	10 min ~ 4 hr	<1 min
DI Rinse	O	X
Thermal budget	X	O
etching	O	X

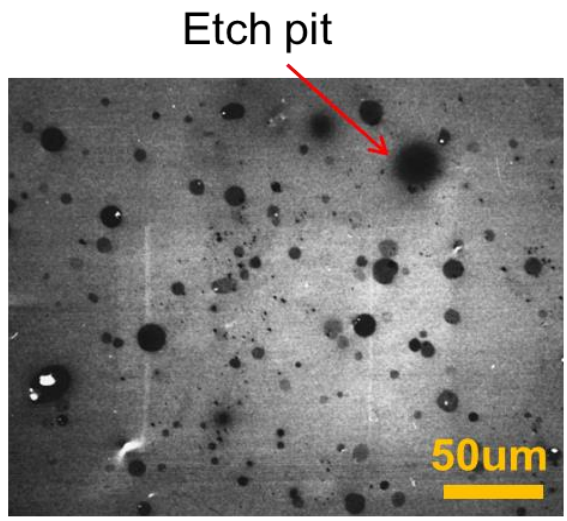


Figure 1.3 SEM images of $(NH_4)_2S$ treated GaAs(100) surfaces.[41]

MIS capacitors.

Chapter 3 covers the investigation about the adoption of H_2S RTA as pretreatment on InP substrates using the same oxide of HfO_2 as a gate insulator. We studied the electrical characteristics of TiN/HfO_2/S-passivated InP MIS capacitors. We focus the interface reaction between ALD HfO_2 films and S-passivated InP channel materials during ALD. Based on the comprehesnsion of the interfacial reactions at HfO_2/S-passivated InP, the interfacial reactions were controlled by various surface treatment conditions.

Chapter 4 presents the study on sulfur interface passivation for Al_2O_3/InGaAs using H_2S RTA post deposition annealing, which affects crucially the electrical properties of films. The suppression of interfacial layer thickness and interaction at the interface were investigated.

Finally, Chapter 5 summarized the results of Chapter 2, 3, and 4.

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Chapter 2 Interface Sulfur Passivation Using H_2S Pre-deposition Annealing for Atomic-layer-deposited HfO_2 Films on a Ge

2.1. Introduction

Because of the physical limitation, there have been many researches about substitutes of sub-14nm high performance MOS device's silicon substrate. Germanium is one of the promising candidates for these substitutes, because of its high carrier mobility and narrow band gap[1]. In common with silicon, germanium is the single element semiconductor. So It has been expected that the application of Ge substrate for conventional Si-Based MOSFET fabrication process should be easy. However, because of the high interface trap density (Dit) at the interface between substrate and dielectric layer, most of the early Ge-MOS devices show much poorer electrical properties than expected[2][3]. Recently, there are many reports that the high interface trap density of Ge-MOS devices is caused by thermodynamically unstable native oxide of Ge[4][5][24]. Unlike silicon, native oxide of Ge shows poor passivation properties. During the thermal annealing process above 400 ^oC, GeO_2 reacts with substrate Ge through the $Ge + GeO_2 \rightarrow 2GeO$ reaction[6]. Since the GeO has volatile property, it decomposes to Ge ion and oxygen vacancy. Subsequently, Ge ions and oxygen vacancies are diffuse out through the GeO_2 and dielectric layer. During these processes, large amount of interface defect can be formed. The high density of interface trap causes many problems to MOS device, such as large surface leakage current, carrier mobility degradation, threshold voltage increases[7]. There have been many reports about the interface passivation methods of Ge-MOS device to prevent performance degradation by the high interface trap density, such as surface nitridation[8][9][10], high quality GeO_2 layer

forming[11][12], Al_2O_3 passivation layer[13][14], SiO_2 capping layer[15], rare earth oxide layer[15][16] and sulfur passivation[17][18][20][21][22].

However, in most of current passivation methods, few nanometers of passivation layer which has relatively low dielectric constant than high-k dielectric layer, is necessary for the effective electric passivation[8][10][13][15][16][19]. As the result, performance degradation from high CET value is expected for the next generation sub-14nm Ge-MOS devices. In contrast, S-passivation method has advantages for next generation fabrication process. First, it is possible that forming effective passivation layer without increase of CET, because S-passivation layer shows good passivation properties despite with a few mono-layer of Ge-S bonding[20][21][22]. Additionally, S-passivation process is not that complicated, compared with other method. So It is easy to apply S-passivation process for the conventional mass-production process[17][18][20][21][22]. S-passivation layer can be formed with sulfur powder[18], ammonium sulfide($(NH_4)_2S$) solution[17][21][22] and hydrogen sulfide(H_2S) gas[18][20], respectively. In the case of using S powder, S-paaivated layer with Ge(100)-(1×1) surface reconstruction can be easily obtained by annealing process with sulfur powder. However, S-passivated surface with sulfur powder shows poor electrical passivation properties, because atomic configuration of (1×1) surface reconstruction lead to forming defect states in energy band gap of Ge[18]. In contrast, S-passivated surface with $(NH_4)_2S$ solution shows good electrical passivation properties. Furthermore, as the surface passivation process is carried out with temperature of less than 100 °C, passivation process is relatively simple and cheap. However, as the wet-based process, the use of $(NH_4)_2S$ solution for surface passivation has several problems such as surface contamination during process and non-uniform properties over the wafer due to the reoxidation of surface in air after

passivation process. Thus, In respect of conventional mass-production process, the application of $(NH_4)_2S$ solution for the surface S-passivation would be difficult[17][20]. In contrast, as the dry process, S-passivation process with H_2S gas is much familiar with conventional mass-production process. S-passivated surface can be obtained by annealing under 400 °C of H_2S atmosphere. During the annealing in H_2S atmosphere, (S-H)-(S-H) inter-Ge dimer bridge is formed, and as the result, the surface of Ge is reconstructed in Ge(100)-(2×1). In this case, Ge(100)-(2×1) surface reconstruction shows good electrical passivation properties without any energy state in energy band gap of Ge[18][20]. In addition, dry processed S-passivation layer acts as a physical passivation layer which prevents the oxidation of Ge surface during dielectric layer deposition process or subsequent annealing process. [22]

In this paper, we report the dramatic improvement of electrical properties of TiN/HfO_2/Ge MIS capacitor which is effectively S-passivated before dielectric layer deposition with H_2S gas and rapid thermal process, that familiar with conventional mass-production process. In addition, the interfacial properties of S-passivated HfO_2/Ge interface are discussed by XPS, TOF-SIMS analysis.

2.2 Experimental details

The surface of n-type Ge (100) substrate was cyclic-etched using a diluted HF solution (1%) and deionized water. To achieve surface S passivation, pre-deposition annealing was performed at 250 ~ 400 °C for 30 s under H_2S atmosphere (5% H_2S/95% N_2) using a rapid thermal annealing (RTA) process with the working pressure of 500 torr. Atomic-layer-deposited HfO_2 films were grown to the thickness of ~ 7 nm at 280 °C on the

S-passivated Ge substrate in a 4-inch travelling-wave type ALD reactor (CN-1 Co., Atomic Classic) using Tetrakis(ethylmethylamino)hafnium (TEMAHf, $Hf[(C_2H_5)(CH_3)]_4$) and O_3 with the concentration of 200 g/Nm^3 as the metal organic precursor and oxygen source, respectively. High purity N_2 (99.999%) was used as carrier gas. The pulse times of TEMAHf and O_3 were 2.5 and 1.5 s respectively, and the purging time between two chemical pulses was 15 s.

For the fabrication of MIS devices, 100 nm-thick TiN top electrode was deposited through the shadow mask using dc magnetron sputtering, which was followed by forming gas (5% H_2/95% Ar) annealing at 350 ^oC for 30 min. In-Ga eutectic alloy was used for backside Ohmic contact. The capacitance-voltage (C-V) characteristic of the MIS devices was examined using an Agilent E4980A precision LCR meter. The equivalent oxide thickness (EOT) of the film was calculated from the accumulation capacitances measured at 1 MHz considering quantum mechanical effect. The microstructures of the films and interfaces were observed through high-resolution transmission electron microscopy (HRTEM) and scanning electron microscopy (STEM) equipped with a field emission gun (FEI Co., Ltd.). The film morphology was observed via atomic force microscopy (AFM, Veeco Dimension V). The depth profiles of the elements in the films were traced via dynamic SIMS (ION-TOF IV GmbH) equipped with 25 kV Bi ion gun operated with the target current of 1 pA. The film was sputtered by Cs ion gun with the energy of 1 keV (target current of 10 nA). The interface chemical binding status of the film was examined via XPS, using Mg Kα as the X-ray source (XPS-ESCALAB 220i). In XPS analysis, ~ 3 nm-thick HfO_2/Ge was used to obtain the sufficient intensity of the signal from the interface.

2.3. Results and Discussion

Figure 2.1 shows the HRTEM and STEM images of S passivated Ge substrates using H_2S annealing at 400 ºC. The continuous sulfur layer on Ge substrates was confirmed, and the thickness was ~2nm. Moreover, it was revealed that the surface S passivation using H_2S annealing hardly degraded the substrate surface, while $(NH_4)_2S$ solution treatment deteriorated the surface as shown in SEM images of Fig. 2.3 and in HRTEM images of Fig.2.2. The surface roughness of Ge substrate increased from 0.14nm to 1.8nm after $(NH_4)_2S$ solution treatment, but it was 0.11nm even after H_2S annealing at 250 and 400 ºC (Fig. 2.4).

The interfacial Ge-S bonding was confirmed from XPS results. Figures 2.5(a)-(e) shows S 2*p*,O 1s, Ge 2*p* and Ge 3*d* core level XPS spectra of the Ge substrates without sulfur passivation and treated by $(NH_4)_2S$ solution and by H_2S annealing at 250 and 400 ℃, respectively. In Fig. 2.5(a), the peak corresponding to the Ge-S at the binding energy (BE) of ~162 eV was observed for all the S-passivated cases. However, it should be noted that the S passivation using $(NH_4)_2S$ solution leaves S-O bonding at the interface, which corresponds to the peak at the BE of ~169 eV. This suggests that S atoms in GeSx at the surface formed by $(NH_4)_2S$ solution become to be combined with oxygen when the sample was exposed to air,

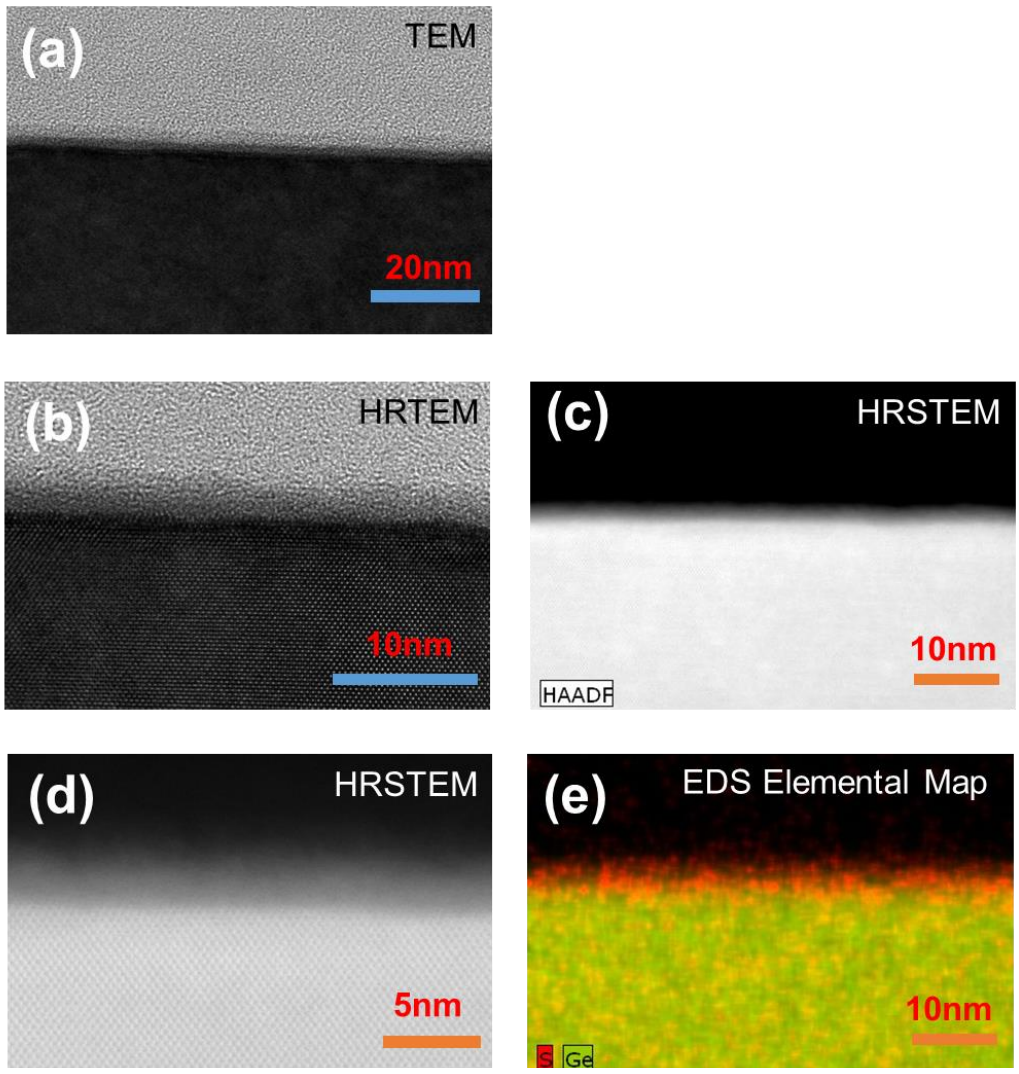

Figure 2.1 [(a)-(e)] Cross-sectional HRTEM and STEM images for Ge substrates with surface S passivation using H_2S annealing at 400 °C.

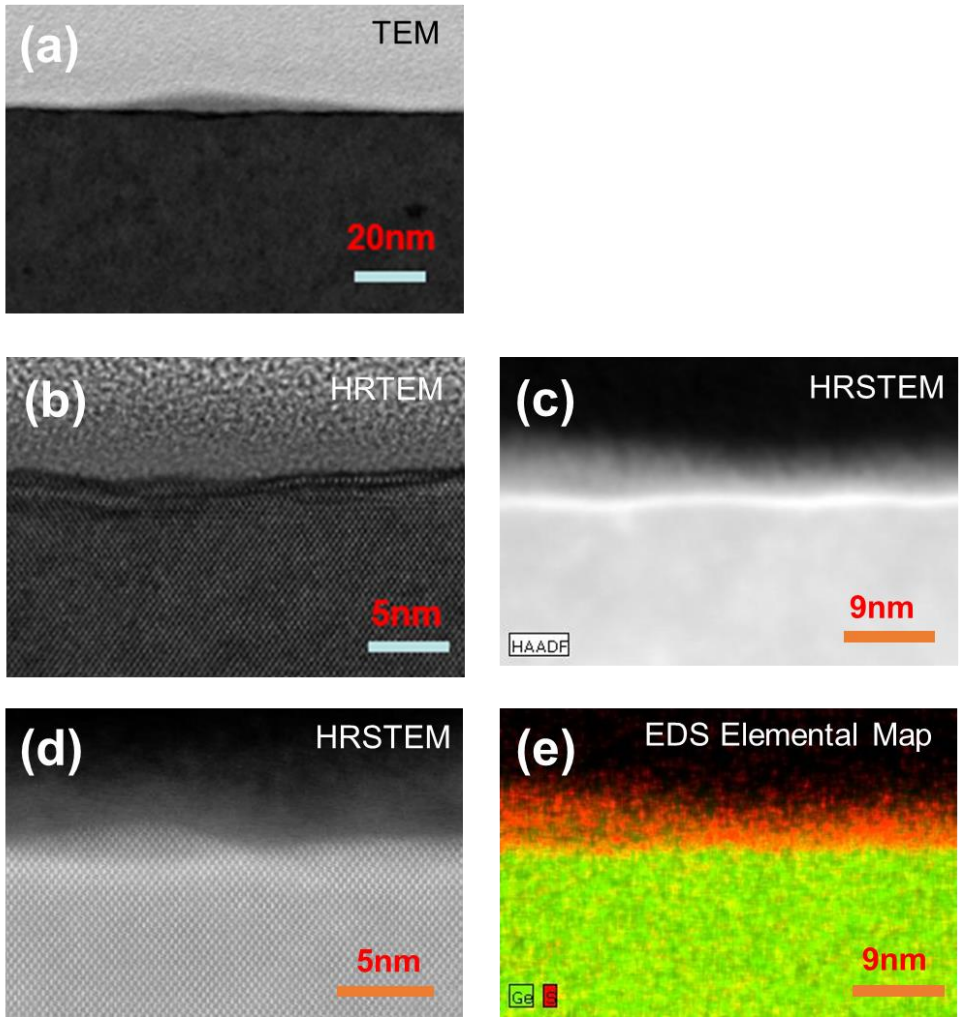

Figure 2.2 [(a)-(e)] Cross-sectional HRTEM and STEM images for Ge substrates with surface S passivation using $(NH_4)_2S$ solution.

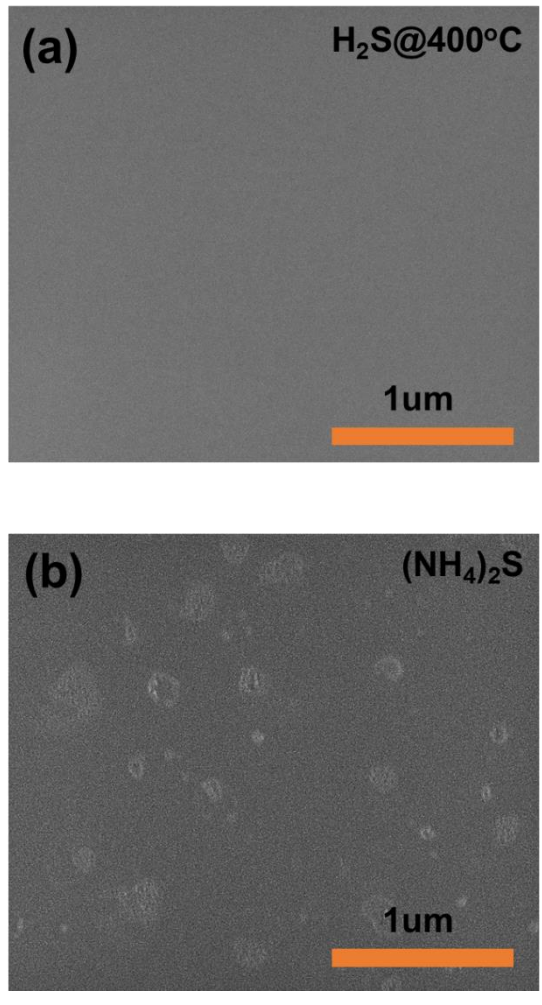

Figure 2.3 [(a), and (b)] SEM images for Ge substrates with surface S passivation using H_2S RTA at 400°C and $(NH_4)_2S$ solution, respectively.

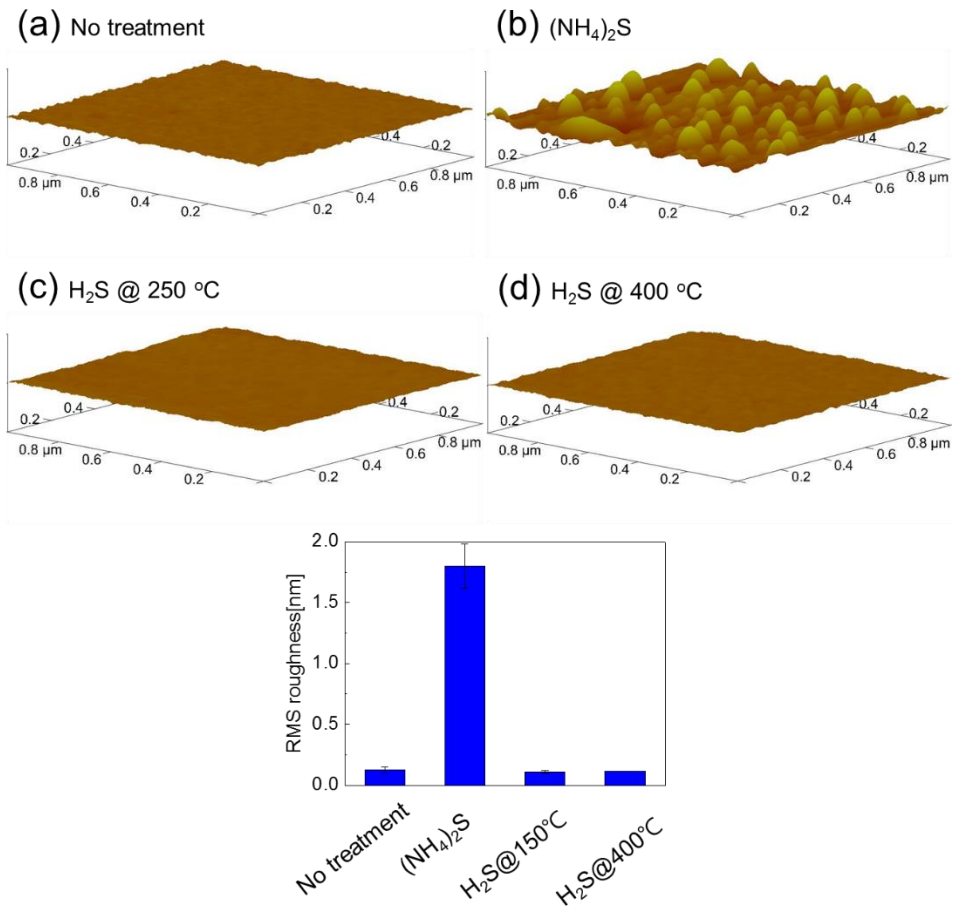

Fig.ure 2.4 AFM images of HfO_2/Ge (a) without and with surface S passivation using H_2S annealing at (b) 250, (c) 300 and (d) 400 °C.

while H_2S annealing results in the more solid Ge-S bonding at the surface, making such S-O bonding improbable. This is confirmed by O 1*s* core level XPS spectra in Fig. 2.5(b), where the peak intensity for the case with $(NH_4)_2S$ solution is higher than that for the case with H_2S annealing. The difference of the chemical binding states of various Ge substrates was shown in Ge 2*p* and 3*d* core level XPS spectra of Figs. 2.5(c),(d) and (e), respectively. It should be noted that Ge-oxide was suppressed by the S-passivation.

The formation of S passivation layer was observed through TOF-SIMS analysis as shown in Fig. 2.6(a)~(c), where is the depth profile of S, Ge and HfO_2 in ALD HfO_2(~7 nm) on Ge substrates without and with S passivation using $(NH_4)_2S$ solution and H_2S annealing at 250 ~ 400 ^oC, respectively. S signal peak was clearly observed at the interface of HfO_2/S-passivated Ge. This confirmed that the S passivation layer was successfully formed at the interface by S passivation using RTA in H_2S atmosphere and $(NH_4)_2S$ solution, which was hardly decomposed during subsequent ALD process, which is comfirmed by EDS map images of HfO_2/S-passivated Ge as shown in Fig. 2-7(a) and (b), as well. The red colored area indicated sulfur at the interface of HfO_2/Ge substrates.

It should be noted that the Ge signal intensity was lower near the interface for the case with S passivation using RTA in H_2S atmosphere as indicated by an arrow(in fig 2.8(a)), which means that the S passivation suppressed the diffusion of Ge into the film or interfacial layer growth during ALD. [20][24] This is also supported by XPS Ge 3*d* core level spectra for HfO_2(~ 3 nm)/Ge with and without the S passivation at 250, 300 and 400 ^oC as shown in Fig. 2.8(b), where the intensity of the peak corresponding to GeO_x was lower for HfO_2/Ge with S

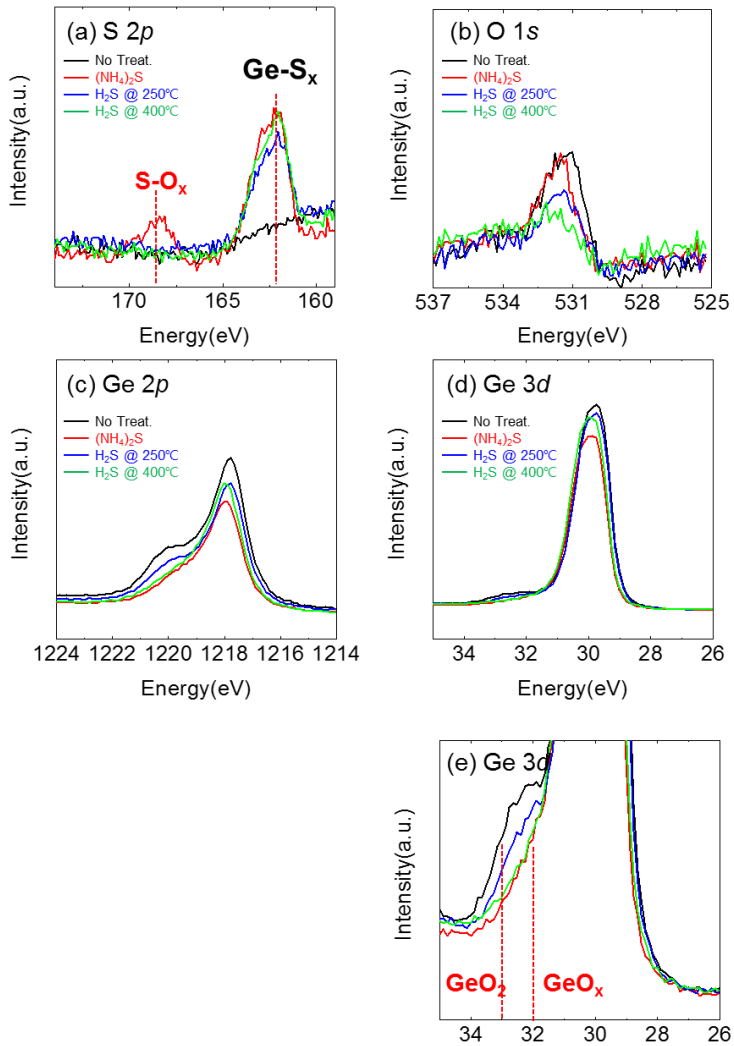

Figure 2.5(a) S 2*p*, (b) O 1*s*, (c) Ge 2*p* and (d), (e) Ge 3*d* core level XPS spectra for Ge substrates with surface S passivation using $(NH_4)_2S$ solution and H_2S annealing at 250 and 400 ℃, respectively.

passivation. The temperature dependency of GeO_x peak was hardly observed because the amount of Ge-S bonding is similar in the annealing temperatures range.[25]

Figure 2.9 shows HRTEM images for HfO_2/Ge without and with S passivation at 400 °C. The thickness of HfO_2 upper layer is similar, ~ 8 nm, but that of interfacial layer (IL) is thinner for HfO_2/Ge with S passivation, which is clearly observed in the magnified images of Fig. 2.9(c) and (d). This is attributed to the suppressed Ge diffusion into the film, which is consistent with the SIMS result.

The EOT values for the HfO_2 films on Ge without and with S passivation at 250, 300 and 400 °C were compared using MIS devices as shown in Fig. 2.10(a). The S passivation effectively reduced CET, which decreased with increasing passivation temperature due to the suppressed IL growth. The CET gain of ~0.4 nm was achieved with the S passivation at 400 °C. Figure 2.10(b) shows the normalized C-V curves for various devices. Considering the slope of curves, the D_{it} decreased with increasing temperature for the S passivation, which indicated the electrical defect passivation effect of S at the interface. The interface state density for various devices was also examined by the frequency dispersion in capacitance. Figure 6 shows the typical C-V curves measured at the frequency ranging from 10k to 1MHz for MIS devices with HfO_2 films on Ge without and with S passivation at 250, 300 and 400 °C. There are two possible causes for the frequency dispersion in capacitance at the depletion region. First, it can be attributed to true inversion by the minority carrier response in Ge, [27] which depends on the minority carrier response time (τ_R), intrinsic property of semiconductor. The τ_R ($\propto \tau_T/n_i$) is determined by minority carrier lifetime (τ_T) and intrinsic carrier concentration (n_i). Since the

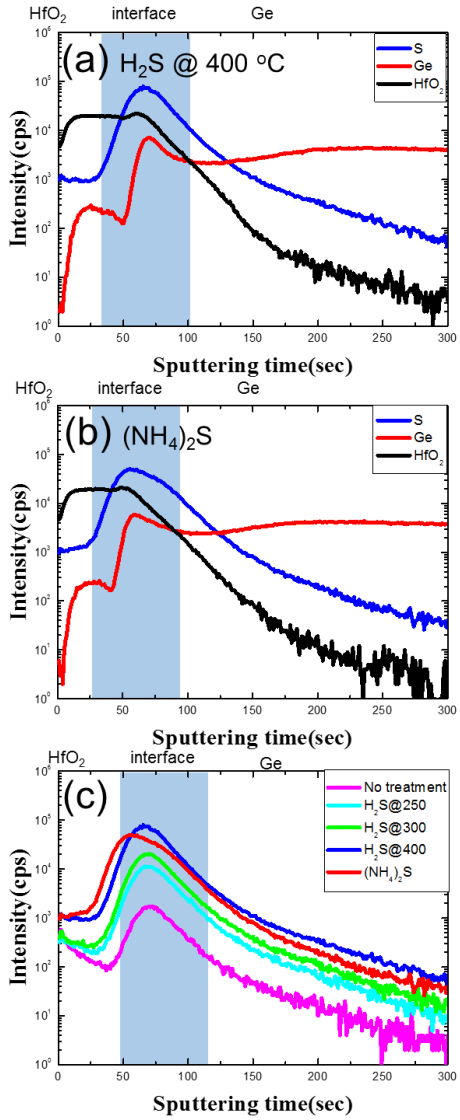

Figure 2.6 (a) – (c) TOF-SIMS depth profile of S, Ge and HfO_2 in HfO_2/Ge without and with S passivation using $(NH_4)_2S$ and H_2S annealing at 250-400 °C

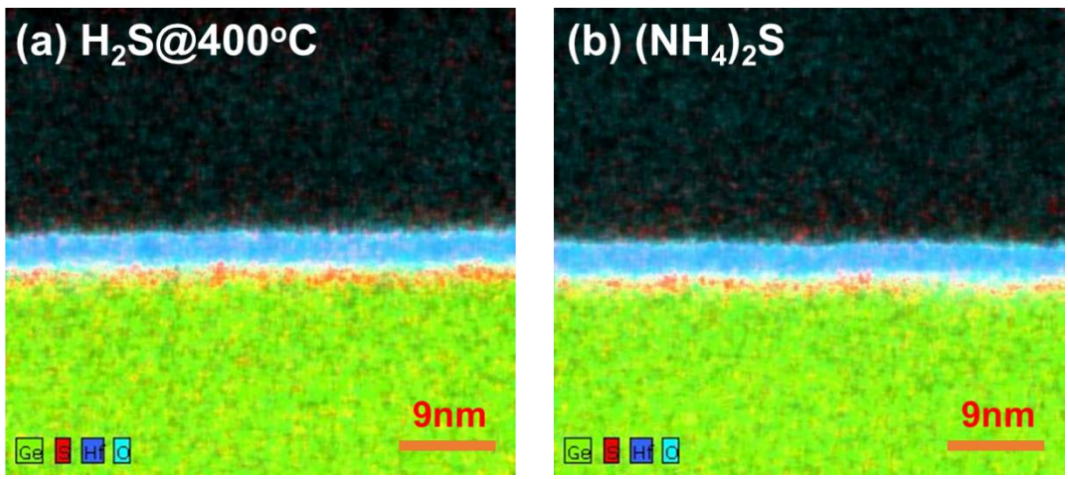

Figure 2.7(a), (b) Cross-sectional EDS map images for Ge substrates with surface S passivation using H_2S RTA at 400°C and $(NH_4)_2S$ solution.

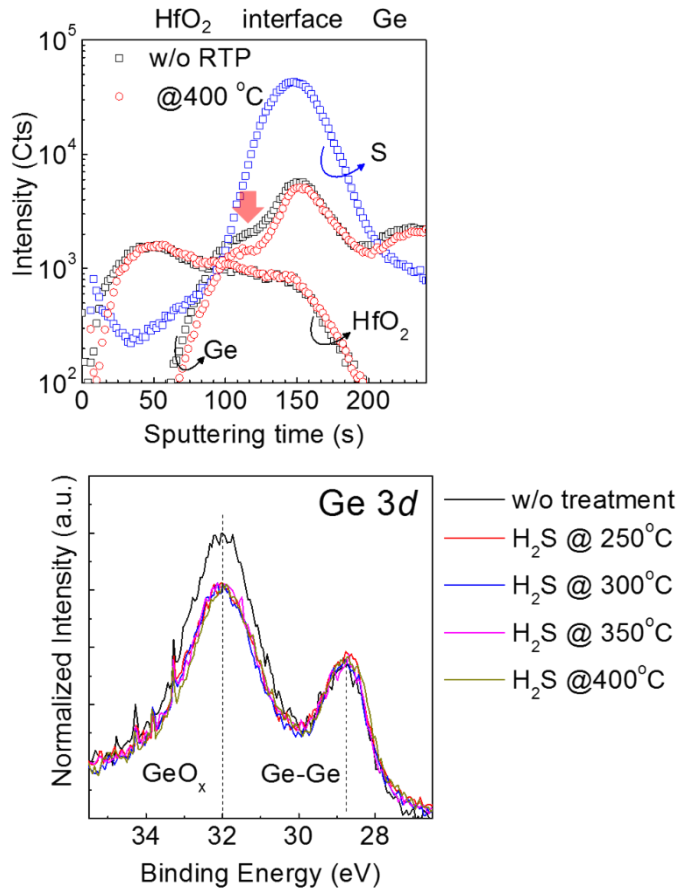

Figure 2.8(a) TOF-SIMS depth profile of S, Ge and HfO_2 in HfO_2/Ge without and with S passivation using H_2S annealing at 400 °C, (b) Ge 3*d* core-level XP spectra of the various HfO_2 films on the Ge substrate.

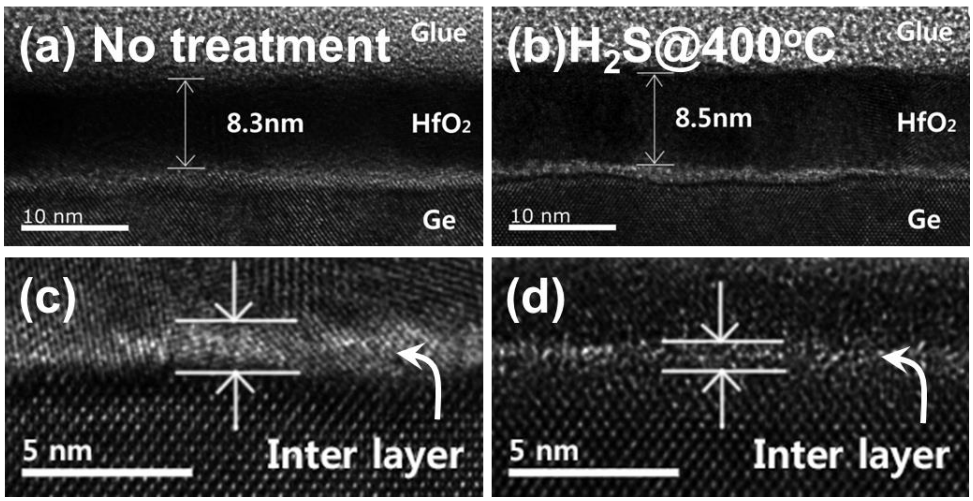

Figure 2.9[(a)-(d)] Cross-sectional HRTEM images for HfO_2 films without and with surface S passivation using H_2S annealing at 400 °C.

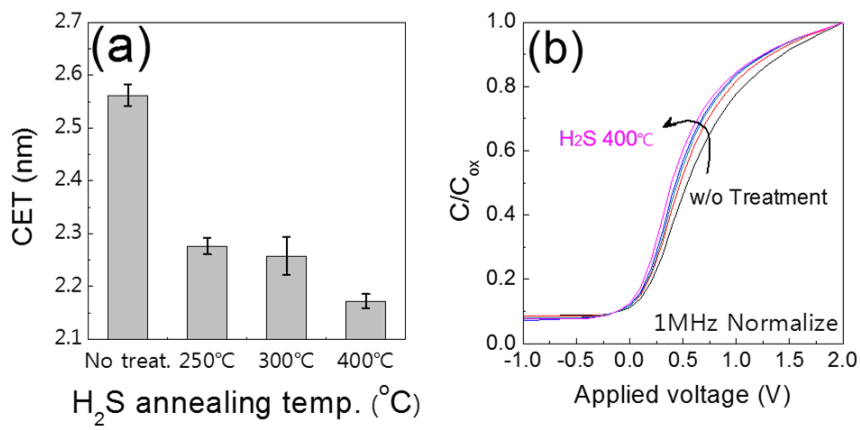

Figure 2.10 (a) CET, and (b) typical C-V curves at the 1 MHz for MIS capacitors (TiN/HfO_2/Ge) without and with surface S passivation using H_2S annealing at 250, 300 and 400 °C.

n_i in Ge is about three orders of magnitude shorter and τ_T is similar compared to Si, the frequency where the true inversion occurs in case of Ge would be higher than the case of Si. However, the true inversion in Ge would occur at the lower frequency (< 1 kHz) than that used in fig. 2.11, where the plateau in capacitance should be observed in inversion (depletion) region. [7][27] Therefore, the frequency dispersion in capacitance in C-V curves of fig. 2.11 is attributed to the high D_{it}.[7]

From the previous studies, there are many reports that Ge-based MIS devices have a large number of interface traps from the volatile decomposition reaction of thermodynamically unstable GeO. The volatilization process of GeO is proceeded in two steps. At first, GeO decomposed to oxygen vacancy and Ge ion at the GeO_x/Ge interface. After that, oxygen vacancy and Ge ion are diffused out to the GeO_2 surface through the GeO_2 layer. If such a reaction is occurred at HfO_2/Ge interface, decomposed products of GeO are diffused into HfO_2 layer and react with Hf or oxygen in HfO_2 layer. In this process, if the Ge-Hf bonding is formed, it generates the energy states in band gap of Ge. These energy states have high enough level of interface trap density which can induce the weak fermi level pinning [5][6][7]. MIS devices with the high interface trap density are very sensitive with the frequency of AC signal or change of temperature while C-V curve measurement. As a result, measured C-V curve shows high inversion capacitance, typical hump at the weak inversion region and stretch-out shape than ideal C-V curve.

The frequency dispersion in capacitance at accumulation region was similar despite of S passivation, but that at depletion region was significantly reduced by S passivation. The

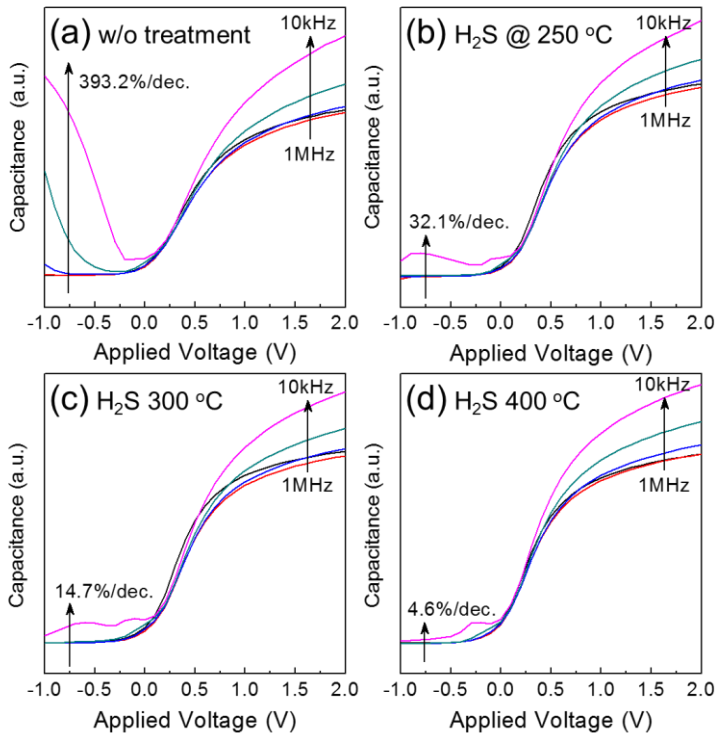

Figure 2.11 Typical C-V curves at the frequency ranging from 10 k to 1 MHz for MIS capacitors ($TiN/HfO_2/Ge$) (a) without and with surface S passivation using H_2S annealing at (b) 250 ,(c) 300 and (d) 400 °C,respectively.

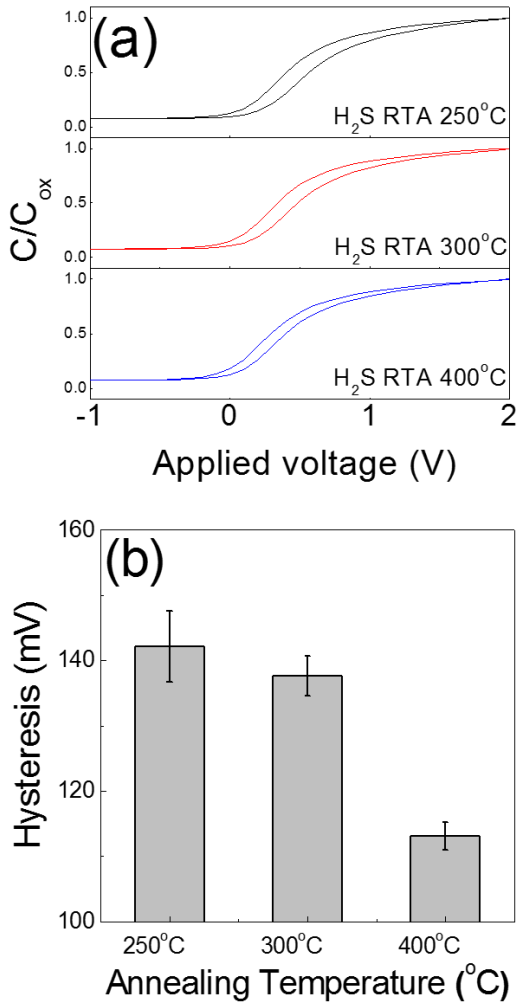

Figure 2. 12(a) The normalized C-V curves at the 1MHz with surface S passivation using H_2S annealing at 250 ,300, and 400 °C , and hysteresis were summarized in (b).

frequency dispersion in capacitance at the accumulation (positive bias) and depletion (negative bias) region reflects the interface defect state density (D_{it}) near the conduction and valence band edge, respectively. Therefore, it can be concluded that the S passivation effectively reduced the D_{it} near valence band edge of Ge, which is consistent with the first principle calculation result.[18]

Figure 2.12(a) shows the normalized C-V curves at the 1 MHz and the hysteresis in the various devices were summarized in Fig. 2.12(b). The hysteresis was reduced to 113mV for the H_2S annealing at 400 °C, while the S passivation using H_2S annealing at 250 °C reduced the hysteresis 142, and 138mV at 300 °C. Considering that the charge trapping characteristic is crucially affected by interface property, this result confirmed the improved S passivation performance of H_2S annealing.

2.4. Summary and Conclusions

In this chapter, we investigated about the S-passivation of the Ge(100) surface through the rapid thermal annealing(RTA) under H_2S atmosphere before ALD of HfO_2 layer. The resulting HfO_2/Ge stack's interfacial properties were examined by XPS and TOF-SIMS analysis. Followed by deposition of TiN, the electrical properties of TiN/HfO_2/Ge MIS capacitor were analyzed by C-V curve measurement. Resulting S-passivation layer shows dramatic improvement of electrical properties in C-V curve measurement. In addition, we can set the optimum RTA process condition by comparison of C-V curve characteristics from various RTA process temperatures. Furthermore, from the TOF-SIMS and XPS result, we can confirm the good physical passivation characteristic of S-passivation layer which can effectively prevents oxidation of Ge substrate during dielectric layer deposition or subsequent

heat treatment process. From this result, we can more easily apply Ge substrate to the conventional MOSFET fabrication process with dry S-passivation process.

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Chapter 3 Improved interface properties of atomic-layer-deposited HfO_2 film on InP using interface sulfur passivation with H_2S pre-deposition

3.1. Introduction

Approaching with speed limit for nano-electronic device built on Si substrates, III-V compound semiconductor is gaining great interests to replace the Si substrate. Many researchers have demonstrated the adoption of III-V compound semiconductors for the fabrication of advanced semiconductor devices.[1-3] However, the growth of interfacial layer (IL) between the gate insulator and III-V compound semiconductor substrate, which deteriorates the interfacial property, is still a critical problem.

Passivating the interface of gate insulator (GI)/III-V substrates using sulfur (S) has been known to effectively suppress the interfacial layer growth and to improve the electrical properties of interface.[4-8] Among the various methods for sulfur passivation, $(NH_4)_2S$ solution treatment was commonly adopted because of simplicity of the process for laboratory experiments. However, the S passivation using $(NH_4)_2S$ solution may not be appropriate for industrial mass-production since it is a wet chemical approach which can cause non-uniform S distribution on the substrate, difficulty in controlling S concentration, and surface residues of contaminants. Pre-deposition annealing of the substrate under H_2S atmosphere is believed to be an appropriate method for replacing the S passivation using $(NH_4)_2S$ solution wet process. The authors have previously reported that the interfacial S passivation for GI/III-V substrate using post-deposition annealing under H_2S atmosphere resulted in a similar S distribution at interface as that of the wet-process, and, thus, improved electrical properties.[9]

In this work, the feasibility to replace the wet-process using $(NH_4)_2S$ solution with the dry-process by annealing under H_2S atmosphere was examined for the interface S passivation in metal-insulator-semiconductor capacitor (MISCAP) devices fabricated on InP substrate. In order to minimize thermal degradation of the InP compound semiconductor surface, rapid thermal annealing (RTA) was adopted under the H_2S environment. Atomic-layer-deposited (ALD) HfO_2 film was grown on InP substrate after surface S passivation. The interfaces were examined in the respect of S distribution at the interface and IL growth behavior and their correlation with the electrical properties were also studied. The chemical composition and binding status at the interface were traced by secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS), respectively. The electrical properties were examined using MISCAP with a TiN top electrode.

3.2. Experimental details

The surfaces of n-type InP substrates were cleaned using a diluted HF solution with deionized water (10%), which were selectively wet-treated with $(NH_4)_2S$ solution for 10 min at room temperature or annealed at 150 and 350 ℃ for 30 s in H_2S (5% H_2S/95% N_2) ambient using RTA to achieve chemical S passivation. ALD HfO_2 films were grown on the substrate at a temperature of 280 ℃ in a 4-inch travelling-wave-type ALD reactor (CN-1 Co., Atomic Classic) using Tetrakis(ethylmethylamino)hafnium (TEMAHf, $Hf[(C_2H_5)(CH_3)]_4$) and O_3 with the concentration of 200 g/Nm3 as the metal precursor and oxygen source, respectively. High purity nitrogen gas (99.999%) was used as carrier and purging gas. TEMAHf precursor and O_3 pulse were introduced into the reactor for 2.5 and 1.5s, respectively. The purging time between two chemical pulses was 15 s.

A sputtered TiN top electrodes were deposited through a shadow mask to fabricate MISCAP devices, which was followed by foaming gas (5% H_2/95% Ar) annealing at 300 ℃ for 30 min. In-Ga eutectic alloy was used for back side Ohmic contact. Capacitance-voltage (C-V) and constant voltage stress (CVS) characteristic were examined using an Aglient 4980a precision LCR meter. The capacitance equivalent oxide thickness (CET) of the films was calculated from the accumulation capacitances measured at 1 MHz. The chemical binding status of the film was examined via high-resolution XPS, using Mg K as the X-ray source (VG Multilab ESCA 2000) with the analysis angle of 45°. The depth profiles of the elements in the films were traced using dynamic SIMS (ION-TOF IV GmbH) equipped with 25 kV Bi ion gun operated with the target current of 1 pA. The film was sputtered by Cs ion gun with the energy of 500 eV (target current of 30 nA). The film morphology was observed via atomic force microscopy (AFM, Veeco Dimension V). The microstructures of the films and interfaces were observed through high-resolution transmission electron microscopy (HRTEM) equipped with a field-emission gun (FEI Co., Ltd.).

3.3. Results and Discussion

Figure 3.1(a) shows the TOF-SIMS depth profile of S in HfO_2/InP structure with the pre-treatments using $(NH_4)_2S$ solution and H_2S annealing at 350 ℃. The shaded area indicates the vicinity of the HfO_2/InP interface. The S distribution near the interface is similar for both the cases. Even though the S signal intensity (concentration) is slightly lower in the case with pre-treatment by H_2S annealing compared with the case with $(NH_4)_2S$, this hardly means the lower efficiency of S incorporation by H_2S annealing because the S concentration at the interface can be controlled with the annealing temperature.

The diffusion/reaction behaviors of substrate elements during HfO_2 ALD were traced and compared to those for the case without pre-treatment as shown in Fig. 3.1(b). The difference in the signal intensity for InO is noticeable, which is indicated by a blue arrow in Fig. 3.1(b). The oxidation of In is believed to be induced during the ALD of HfO_2 using highly oxidizing O_3 as the reaction gas. It can be understood that both of the pre-treatments using $(NH_4)_2S$ solution and H_2S annealing suppressed the InO diffusion into the film during ALD of HfO_2. It is expected that the S preferentially reacts with In to form In-Sat the interface during S passivation process, which suppressed the In diffusion and formation of InO.[10, 11] The interfacial In-S bonding was confirmed from XPS results. Figures 3.2(a)-(d) shows S 2*p*,O 1s, In 3*d* and P 2*p* core level XPS spectra of the InP substrates treated by $(NH_4)_2S$ solution and by H_2S annealing at 150 and 350 ℃, respectively. In Fig. 3.2(a), the peak corresponding to the In-S at the binding energy (BE) of ~162 eV was observed for all the cases. However, it should be noted that the S passivation using $(NH_4)_2S$ solution leaves S-O bonding at the interface, which corresponds to the peak at the BE of ~169 eV. This suggests that S atoms in InSx at the surface formed by $(NH_4)_2S$ solution become to be combined with oxygen when the sample was exposed to air, while H_2S annealing results in the more solid In-S bonding at the surface, making such S-O bonding improbable. This is confirmed by O 1*s* core level XPS spectra in Fig. 3.2(b), where the peak intensity for the case with $(NH_4)_2S$ solution is higher than that for the case with H_2S annealing. The difference in the chemical binding states of substrate elements was indistinguishable as shown in In 3*d* and P 2*p* core level XPS spectra of Figs. 3.2(c) and (d), respectively. The independency of chemical state of In and P on S-treatment conditions was retained even after ALD of HfO_2 film as shown in Figs.3.2(e) and (f). Here, the thickness of HfO_2 film was controlled to ~3 nm for observing

the chemical binding state of the interface between the film and substrate. The interfacial reaction during ALD resulted in the shoulder peak in In 3*d* spectra at the BE of ~444.3 eV, and the In phosphate peak in P 2*p* core level at the BE of ~ 134 eV. However, any difference in the chemical binding state of substrate elements was hardly observed. Considering SIMS result, the effect of surface S passivation on the interfacial reaction (In-O bonding formation) was below the XPS detection limit. This was confirmed by the HRTEM results shown in Figs. 3.3 (a) – (d), which corresponds to the sample with no treatment, $(NH_4)_2S$ solution treatment, H_2S annealing at 150 and 350 ℃, respectively. In all the cross-sectional HRTEM images, the film thicknesses are similar as ~ 7 nm.

However, there is subtle difference in the CET values from these samples as shown in Fig. 3.3(e). The CETs for HfO_2 films with surface S passivation using $(NH_4)_2S$ solution and H_2S annealing are lower than that for HfO_2 films without S passivation despite the film thicknesses are similar. This could be attributed to the InO diffusion into the HfO_2 film, as observed in SIMS result, which lowers the permittivity of the film. There is no difference in

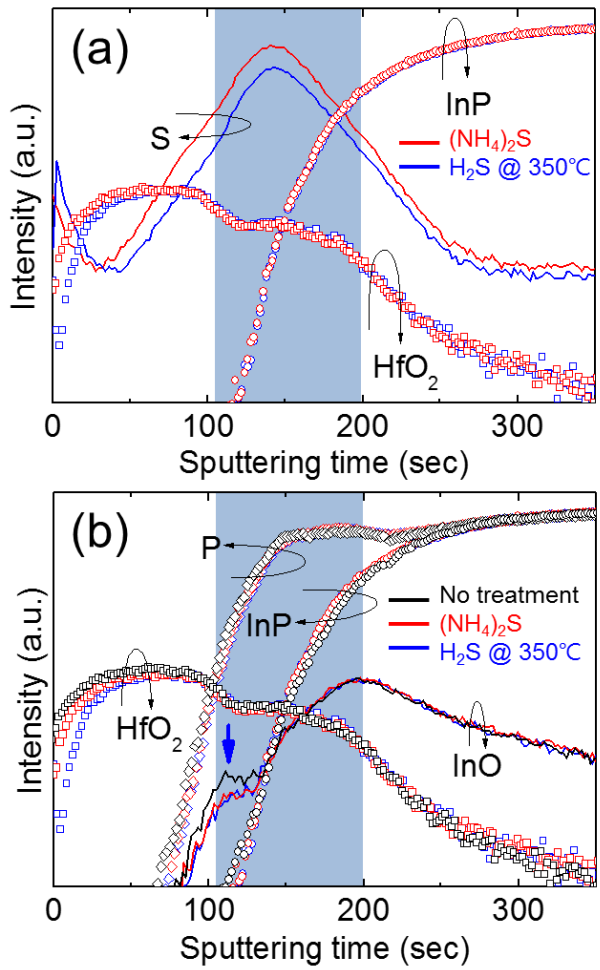

Figure 3.1. (a) TOF-SIMS depth profile of S, and (b) substrate elemental compound and HfO_2 in HfO_2/InP with S passivation using $(NH_4)_2S$ solution and H_2S annealing at 350 ℃.

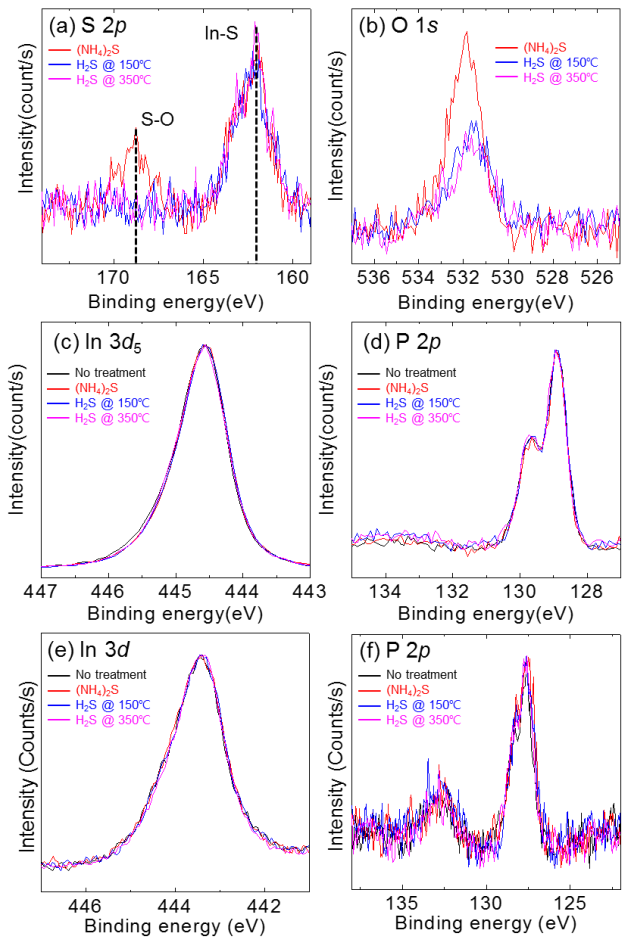

Figure 3.2. (a) S 2*p*, (b) O 1*s*, (c) In 3*d*5 and (d) P 2*p* core level XPS spectra for InP substrates with surface S passivation using $(NH_4)_2S$ solution and H_2S annealing at 150 and 350 ℃, (e) In 3*d* and (f) P 2*p* core level XPS spectra for HfO_2 on InP substrates with the surface S passivations.

CET between the samples with S passivation using $(NH_4)_2S$ solution and H_2S annealing.

The status of the interface states at the interface between the film and InP substrate was observed using frequency dispersion in capacitance from C-V curves measured at frequencies ranging from 10 kHz to 1 MHz as shown in Figs. 3.4(a)-(d).[12-14] It has been known that the true inversion in the C-V curve obtained from III-V compound semiconductor based MISCAP devices could be observed through few Hz frequency range.[15-17] Therefore, in Figs. 3.4(a)-(d), the frequency dispersion in capacitance (increase in capacitance with decreasing frequency) at the accumulation (positive bias) and depletion (negative bias) region reflects the interface defect state density (Dit) near the conduction and valence band edge, respectively, which are summarized in Fig. 3.4(e). The S passivation slightly reduced the frequency dispersion in capacitance at the accumulation region irrespective of the passivation methods. However, it should be noted that the S passivation using H_2S annealing at 350 ℃ largely decreased the frequency dispersion in capacitance at the depletion region from ~ 15.9 to ~ 7.9 %/dec., which is considerably superior to the cases with the S passivation using $(NH_4)_2S$ solution (~12.4%) and H_2S annealing at 150 ℃ (~13.5%). This is consistent with the previous result that S at the interface between the film and III-V substrate effectively decreased the Dit near the valence band edge.[18] The possible reasons for such improvement are discussed below. It is reported that thermal energy supplied during H_2S annealing induced the surface reconstruction from InP (100)-(1×1) to InP(100)-(2×1) which enhances the passivation performance through stronger In-S bonding formation.[19-21] Moreover, it was revealed that the surface S passivation using

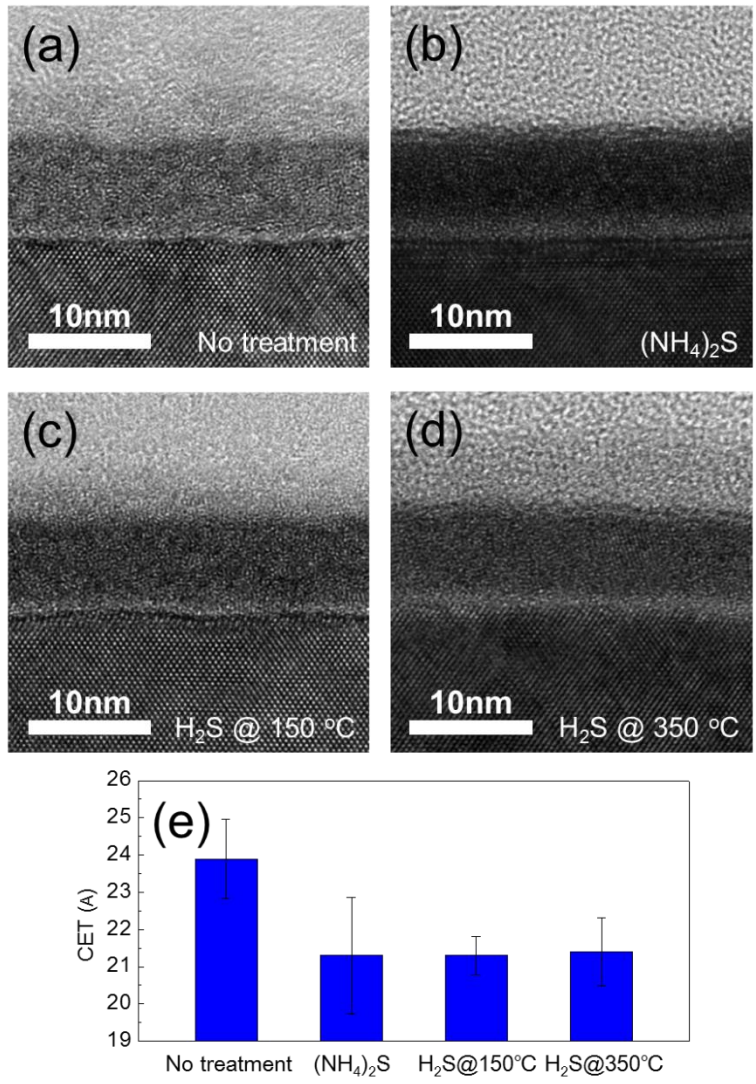

Figure 3.3. [(a)-(d)]Cross-sectional HRTEM images, and (e) the CETs for HfO_2 films with surface S passivation using $(NH_4)_2S$ solution and H_2S annealing at 150 and 350 ℃.

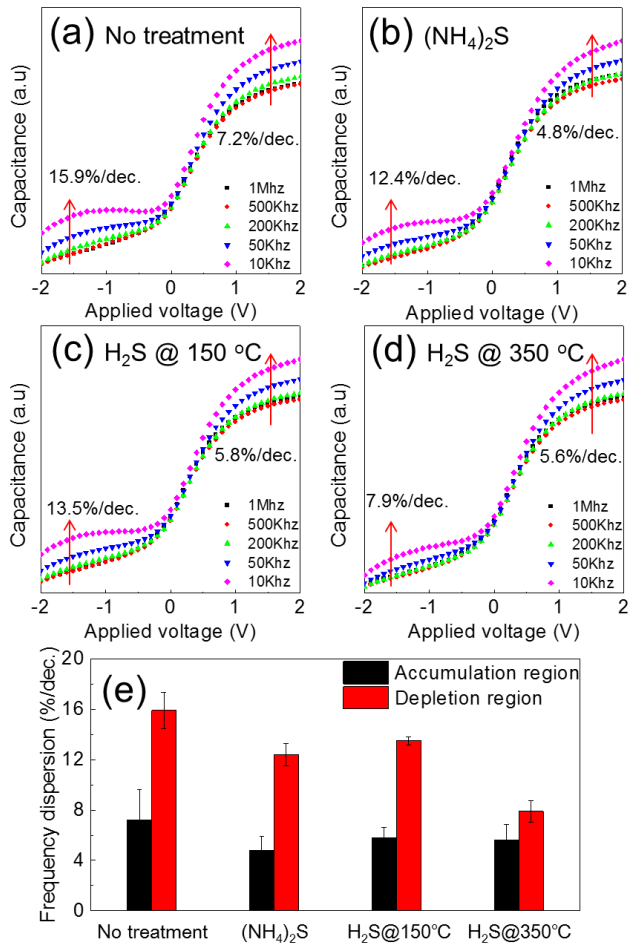

Figure 3.4. Typical C-V curves at the frequency ranging from 10 k to 1 MHz for MIS capacitors ($TiN/HfO_2/InP$) (a) without and with surface S passivation using (b) $(NH_4)_2S$ solution, and (c) H_2S annealing at 150 and (d) 350 ℃. The frequency dispersion in capacitance at the accumulation and depletion regions is summarized in (e).

H_2S annealing hardly degraded the substrate surface, while $(NH_4)_2S$ solution treatment deteriorated the surface as shown in AFM results of Fig. 3.5. The surface roughness of InP substrate (without HfO_2 film) increased from ~ 0.70 to ~ 0.95nm after $(NH_4)_2S$ solution treatment, while it was ~ 0.52 and ~ 0.47nm after H_2S annealing at 150 and 350 ℃, respectively.

The C-V curves were obtained after constant voltage stress (CVS) at 2 V for 0 to 316 s to evaluate the charge trapping characteristic at the interface between film and substrate as shown in Fig. 3.6.[22-26] The changes in flat band voltage (ΔV_{FB}) in the various devices were summarized in Fig. 3.6(e). While the S passivation using $(NH_4)_2S$ solution barely reduced ΔV_{FB} (~ 0.1 V), that using H_2S annealing reduced ΔVFB to ~ 0.08 and ~ 0.06 V for the annealing temperature of 150 and 350 ℃, respectively. Considering that the charge trapping characteristic is crucially affected by interface property, this result confirmed the improved S passivation performance of H_2S annealing compared to that of $(NH_4)_2S$ solution treatment.

3.4. Summary and Conclusions

In summary, we examined the interface sulfur passivation effect in atomic-layer-deposited HfO_2 films on InP substrate using RTA in H_2S atmosphere in order to replace the wet-based surface passivation process with $(NH_4)_2S$ solution which is inappropriate for mass-production. The treatment with $(NH_4)_2S$ solution induced slightly higher S concentration and distribution at the interface of HfO_2/InP compared with the RTA under H_2S atmosphere. While the surface oxidation of S layer on substrate occurred for the case with $(NH_4)_2S$ solution treatment, H_2S annealing resulted in only In-S boding on the substrate. The thermal

energy supplied during H_2S annealing is expected to facilitate the surface reconstruction of InP surface and solid In-S bonding formation. As a result, interface state density near the valence band and flatband voltage shift after CVS were lower for the S passivation with H_2S annealing compared with that with $(NH_4)_2S$ solution.

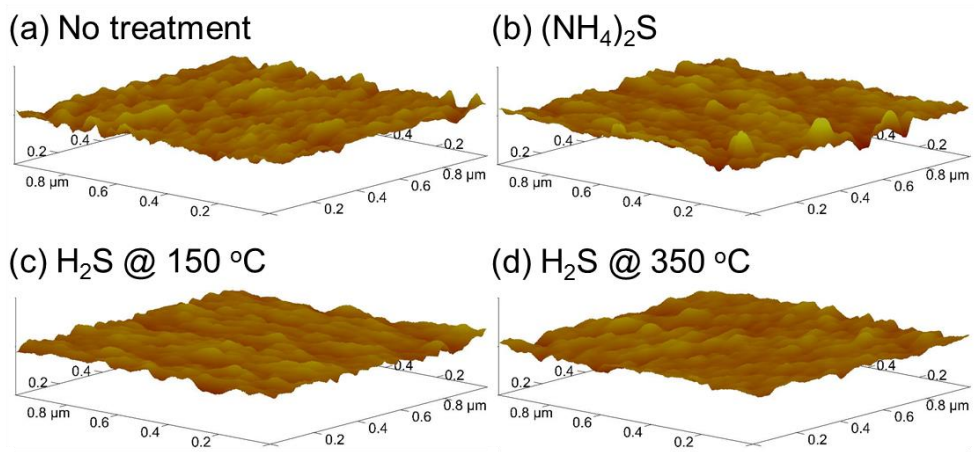

Figure 3.5. AFM images of HfO_2/InP (a) without and with surface S passivation using (b) $(NH_4)_2S$ solution, and (c) H_2S annealing at 150 and (d) 350 ℃.

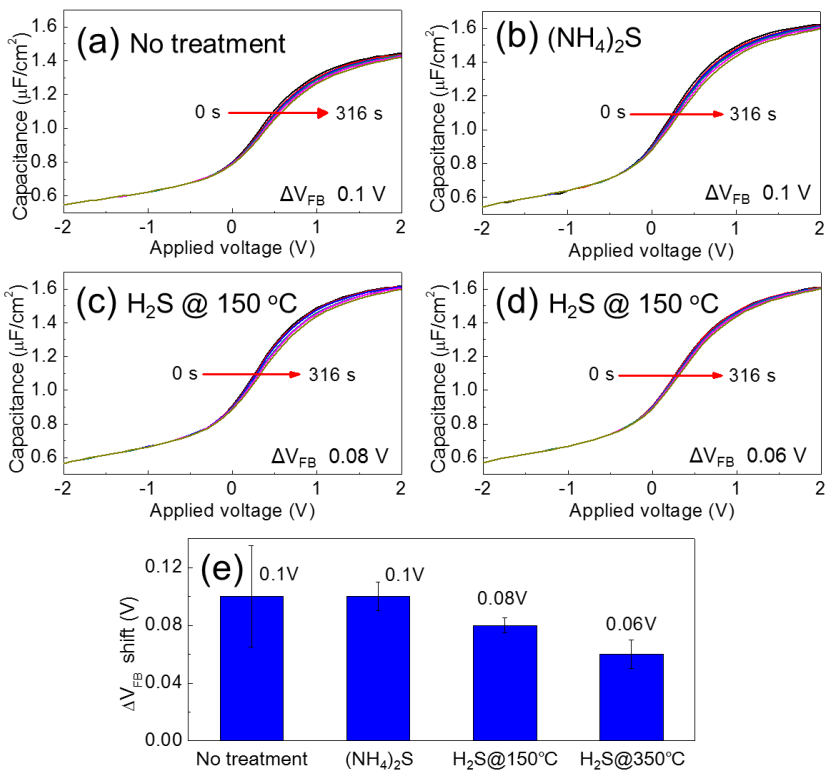

Figure 3.6. C-V curves after CVS at 2 V for 0 to 316 s. (a) without and with surface S passivation using (b) $(NH_4)_2S$ solution, and (c) H_2S annealing at 150 and (d) 350 ℃. The flatband voltage shifts were summarized in (e).

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Chapter 4. Interface Sulfur Passivation Using H_2S Post Deposition Annealing for Atomic-layer-deposited Al_2O_3 Films on an Ultrathin-Body $In_{0.53}Ga_{0.47}As$-on-Insulator

4.1. Introduction

Passivating the interface between the gate insulator (GI) and the III-V compound substrates using sulfur (S) has been known to be effective for improving the interfacial properties in metal-insulator-semiconductor (MIS) devices based on III-V compound semiconductor substrates. The S at the interface between the GI and III-Vs plays an important role: that of passivating the surface-dangling bonds so as to reduce the electrical defects at the interface, and suppressing undesirable interfacial-layer (IL) growth. [1-7] One of the commonly adopted methods of incorporating S onto the interface is wet-treating the III-V substrates in a $(NH_4)_2S$ solution.[8-10] S passivation using $(NH_4)_2S$ solution, however, is not appropriate for industrial mass production because S bonding on the substrate surface is unstable in the atmosphere, and the S is likely to be sensitively released from the surface depending on the process variables, such as the temperature, air exposure time, and pressure. Therefore, various methods for S incorporation into the interface need to be studied.[11, 12] Among them, the post-deposition annealing (PDA) of the GI films grown either under a H_2S atmosphere or with S powder in the annealing chamber [13, 14] can be a feasible candidate for replacing wet processing using a $(NH_4)_2S$ solution with simple dry processing. S could be accumulated at the interface after PDA due to the stress at the interface between the dielectric film and the substrate, which is similar to the case of the nitrogen accumulated at

the interface between the SiO_2 GI and the Si substrate after PDA under NH_3, N_2O, etc.[15-18]

In this study, the feasibility of replacing wet processing for the interface S passivation in III-V compound-semiconductor-based devices with dry processing using PDA under a H_2S atmosphere was examined. Al_2O_3 films were grown using the atomic-layer-deposition (ALD) technique on ultrathin-body $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2/Si$ substrates. The interface properties of the various samples were systematically observed from the viewpoints of (i) the S distribution at the interface and (ii) the IL growth behavior. The chemical composition and bonding status at the interface were traced through secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS), respectively. MIS capacitors were fabricated, and their electrical properties were examined. Furthermore, the properties of the devices with PDA under a N_2 atmosphere were compared with those with PDA under a H_2S atmosphere.

4.2. Experimental details

Ultrathin-body $In_{0.53}Ga_{0.47}As$ layers (~130 nm) on Al_2O_3 (~8 nm)/SiO_2(~100 nm)/Si substrates were prepared using a wafer bonding technique,[19, 20] whose cross-section transmission electron microscopy (TEM) image is shown in Fig. 4.1(a). The surfaces of the substrates were cleaned for 30 s using a diluted HF solution with deionized water (10 %) and were selectively wet-treated with $(NH_4)_2S$ solution (22 vol%) for 10 min at room temperature (to achieve chemical S passivation). ALD Al_2O_3 films were grown on the as-prepared wafer-bonded ultrathin-body $In_{0.53}Ga_{0.47}As/Al_2O_3/SiO_2/Si$ substrate in a 4-inch traveling-wave-type ALD reactor (CN-1 Co., Atomic Classic) using $Al(CH_4)_3$ and H_2O as the metal precursor

and oxygen source, respectively, at a substrate temperature of 280 ℃. Pure N_2 (99.999%) was used as carrier gas. The feeding times of $Al(CH_4)_3$ and H_2O were 1.5 sec. The purging times after $Al(CH_4)_3$ and H_2O pulses were 15 and 30 s, respectively.

PDA of the grown films was performed using a rapid thermal annealing process at 500 ℃ for 30 s, under a pure N_2 or 5%H_2S/95%N_2 atmosphere with the working pressure of ~100 torr. The schematic diagram of the fabricated MIS devices is shown in Fig. 4.1(b). A sputtered TiN gate electrode was deposited through a shadow mask, which was followed by forming gas (95% N_2/5% H_2) annealing at 300℃ for 30 min. In-Ga eutectic alloy was used for back Ohmic contact after the etch-out of the Al_2O_3 GI film using the HF solution. The capacitance-voltage (C-V) and hysteresis characteristics were examined using an Agilent E4980A precision LCR meter. The equivalent oxide thickness (EOT) of the films was calculated from the accumulation capacitances measured at 1 MHz, considering the quantum mechanical effects. The interface chemical binding status of the film was examined via XPS, using Mg *Kα* as the X-ray source (VG Multilab ESCA 2000) with the analysis angle of 45°. The depth profiles of the elements in the films were traced via dynamic SIMS (ION-TOF IV GmbH) equipped with 25 kV Bi ion gun operated with the target current of 1 pA. The film was sputtered by Cs ion gun with the energy of 500 eV (target current of 30 nA). The microstructures of the films and interfaces were observed through high-resolution transmission electron microscopy (HRTEM) equipped with a field emission gun (FEI Co., Ltd.).

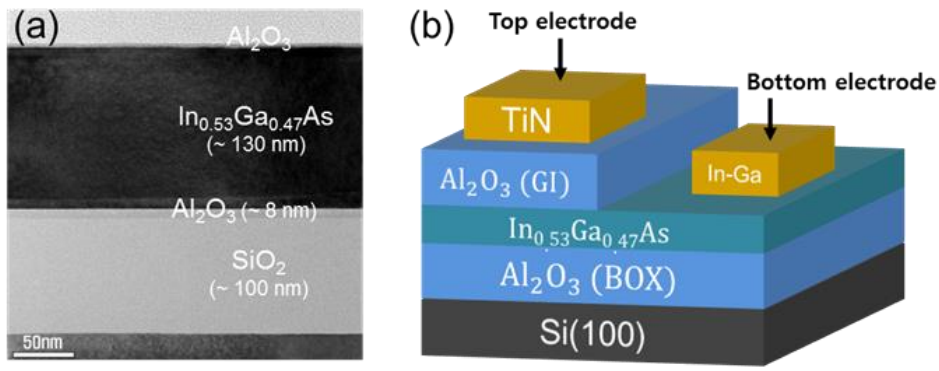

Figure 4.1 (a) TEM image of the prepared ultrathin-body $In_{0.53}Ga_{0.47}As$ on $Al_2O_3/SiO_2/Si$ substrates with Al_2O_3 gate oxide. (b) Schematic structure of the MIS capacitor with a TiN top electrode.

4.3. Results and Discussion

First, the S distribution at the interface in the various cases was traced using the SIMS depth profile. Fig. 4.2(a) shows the SIMS depth profiles for S, Al, and As in the ALD Al_2O_3 films (~3 nm) on an ultrathin-body $In_{0.53}Ga_{0.47}As$ substrate with interface S passivation using $(NH_4)_2S$ solution, and PDA under a H_2S atmosphere with no $(NH_4)_2S$ wet treatment. The Al and As signals were included to identify the position of the interface, which seem to be practically identical for both samples in Fig. 4.2(a). S was accumulated at the interface by the $(NH_4)_2S$ wet treatment as well as PDA under a H_2S atmosphere while the S concentration (which cannot be quantitatively determined via SIMS due to the lack of appropriate reference) of the former case was certainly higher than that of the latter case. The accumulation of S at the interface is known to be due to the stress present at the interface between the film and the substrate.[15, 16] The S at the film surface for all the samples was due to the surface adsorption of the H_2S gas in the reactor.

Meanwhile, the influence of PDA under H_2S on the chemical structure of the film was compared with that of PDA under a N_2 atmosphere, as shown in Fig. 4.2(b). All the substrates were chemically treated with $(NH_4)_2S$ solution prior to the ALD process. ALD Al_2O_3 films were grown on the substrates, which was followed by PDA under N_2 and H_2S atmospheres. The peak level of the S concentration at the interface was similar for all the films. While the PDA under a N_2 atmosphere hardly affected the S distribution in the film, the PDA under a H_2S atmosphere resulted in the tailing of the S concentration into the substrate, as indicated by the blue arrow. This suggests that the PDA under a H_2S atmosphere

induced more S bonding with the surface of the ultrathin-body $In_{0.53}Ga_{0.47}As$ compared to the case with only $(NH_4)_2S$ wet-treatment.

The IL growth behavior in the various study cases was observed via XPS and HRTEM. Fig. 4.3 shows the (a) In 3*d*, (b) Ga 3*s*, and (c) As 3*d* core-level XPS spectra for the different samples, where the thickness of the Al_2O_3 GI film was maintained at ~3 nm for observing the chemical-bonding status of the interface between the film and substrate. All the peak intensities were normalized using the maximum intensity. As shown in Fig. 4.3(a), the peak centered at the binding energy (BE) of ~443.7 eV coincided with the In in the $In_{0.53}Ga_{0.47}As$ while the increased intensity at the higher BE (~445 eV) may correspond to those of the oxidized In atoms (InO_x). In all the films with $(NH_4)_2S$ wet treatment, interfacial InO_x formation seemed to be quite suppressed compared to the films without $(NH_4)_2S$ wet treatment, which was hardly affected by the following PDA under N_2 and H_2S atmospheres. The PDA under a H_2S atmosphere without $(NH_4)_2S$ wet treatment also suppressed interfacial InO_x formation, but its effect was quite limited. A similar phenomenon was observed in the Ga 3s and As 3d spectra in Fig. 4.3(b) and (c), where the formation of GaO_x and AsO_x at the interface indicated by blue shaded region [21-23] were effectively suppressed by $(NH_4)_2S$ wet treatment irrespective of the PDA conditions, but the PDA under a H_2S atmosphere instead of $(NH_4)_2S$ wet treatment was less effective than the $(NH_4)_2S$ wet-treatment. These results also suggest that once IL grows during ALD, it is hardly removed by PDA under a H_2S atmosphere because the IL thickness slightly increased due to absence of interface S passivation at the beginning of PDA. The broad peak at ~46 eV in As 3*d* spectra for the case with $(NH_4)_2S$ wet treatment and PDA under H_2S is due to the background

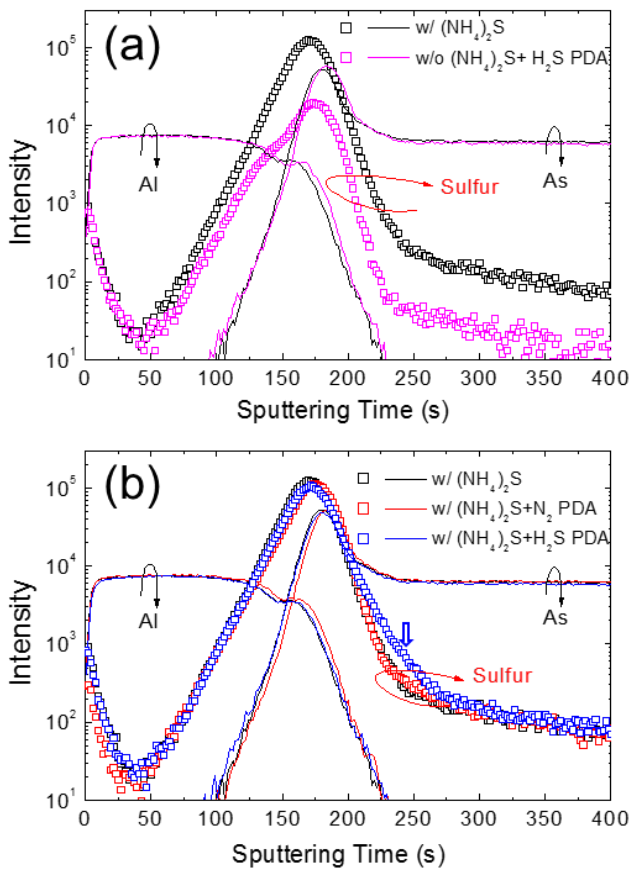

Figure 4.2 SIMS depth profiles for S, Al, and As in the ALD Al_2O_3 films (~3 nm) on the ultrathin-body $In_{0.53}Ga_{0.47}As$ substrate (a) with interface S passivation using $(NH_4)_2S$ solution, and PDA under a H_2S atmosphere without $(NH_4)_2S$ wet treatment, and (b) with $(NH_4)_2S$ wet treatment after the PDAs under N_2 and H_2S atmospheres.

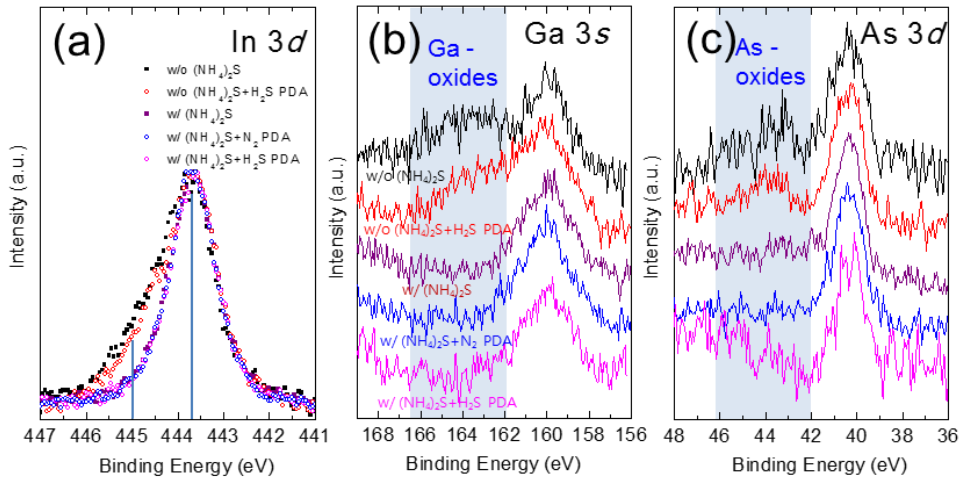

Figure 4.3 (a) In 3*d*, (b) Ga 3*s*, and (c) As 3*d* core-level XP spectra of the various Al_2O_3 films on the ultrathin-body $In_{0.53}Ga_{0.47}As$ substrate.

signal, which can be, thus, neglected here.

Fig. 4.4 shows the HRTEM images for the various samples on the ultrathin-body $In_{0.53}Ga_{0.47}As$ substrate. The calculated film thickness was averaged across the entire layer using more than 15 HRTEM images taken from different regions of the film. HRTEM could not discern the IL from the Al_2O_3 GI layer due to the fact that both layers were of an amorphous nature and possibly had very thin IL. Nevertheless, the total GI film thickness was certainly lower for the cases with $(NH_4)_2S$ wet-treatment [see Fig. 4.4(b), (c), and (d)] while the other GI films without $(NH_4)_2S$ wet-treatment showed thicker total thicknesses, which means that the IL was induced during the ALD. These HRTEM results corroborate the XPS data shown in Fig. 3. For the cases with $(NH_4)_2S$ wet treatment, the PDA under N_2 and H_2S atmospheres decreased the film thickness due to the densification of the film [Fig. 4.4(c) and (d)]. Considering that the film thickness decreased slightly after PDA under a H_2S atmosphere for the case without $(NH_4)_2S$ wet-treatment [Fig. 4.4(a) and (e)], the PDA under a H_2S atmosphere hardly suppressed IL growth due to absence of interface S passivation at the beginning of PDA, which is consistent with the XPS result.

The electrical properties of the films were examined using MIS capacitors. Fig. 4.5 shows the typical C-V curves for various Al_2O_3 films on the ultrathin-body $In_{0.53}Ga_{0.47}As$ substrate. As can be seen in Fig. 4.5(a), $(NH_4)_2S$ wet treatment resulted in a higher accumulation capacitance compared to the case without $(NH_4)_2S$ wet treatment due to the suppressed IL growth, but the hysteresis increased much, which can be attributed to the abrupt interface (too thin IL)

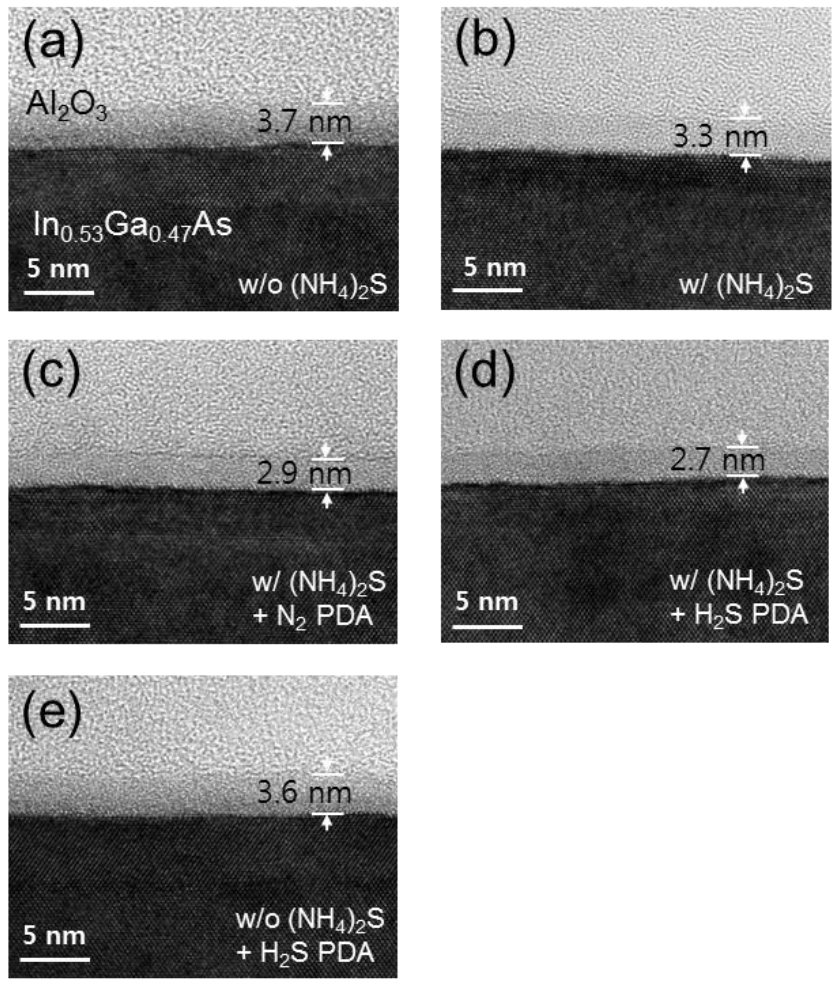

Figure 4.4 Cross sectional HRTEM images of the various Al_2O_3 films on the ultrathin-body $In_{0.53}Ga_{0.47}As$ substrates.

facilitating the charge trapping to the border traps near the interface. [24] On the other hand, the film without $(NH_4)_2S$ wet treatment, and PDA under H_2S showed no increase in hysteresis, but the capacitance slightly decreased due to the increased IL thickness. As shown in Fig. 5(b), with $(NH_4)_2S$ wet treatment, the PDA under H_2S resulted in a higher capacitance compared to the PDA under N_2 due to the lower film (IL) thickness [see Fig. 4.4]. The hysteresis slightly decreased after the PDAs, which might cure the border traps near the interface. The accumulation capacitance values of the various samples corroborate the XPS and HRTEM results. The deviation in depletion capacitance for each sample is expected to originate from the local non-uniformity of doping concentration of the substrate.

The frequency dispersion in the C-V curves for the III-V-based devices reflects the interface state density (D_{it}) of the film.[25-27] The frequency dispersion was therefore measured at the frequencies ranging from 50 kHz to 1 MHz, as shown in Fig. 4.6. The frequency dispersion in the accumulation capacitance for the device without $(NH_4)_2S$ wet treatment and PDA [Fig. 4.6(a)] was ~6.7%/dec. With $(NH_4)_2S$ wet treatment, it decreased to ~3.8%/dec, but the PDA under H_2S without $(NH_4)_2S$ wet treatment resulted in the value of ~6.0%/dec [Fig. 4.6(e)]. This is attributed to the lower S concentration at the interface (see Fig. 4.2). The devices with $(NH_4)_2S$ wet treatment after PDA under N_2 and H_2S atmospheres showed improved frequency dispersion in the capacitances of ~3.2 and ~2.2 %/dec, respectively [Fig. 4.6(c) and (d)]. PDA is generally known to reduce D_{it}.[28-31] Especially, the increased S concentration at the interface after PDA under a H_2S atmosphere further decreased D_{it}.

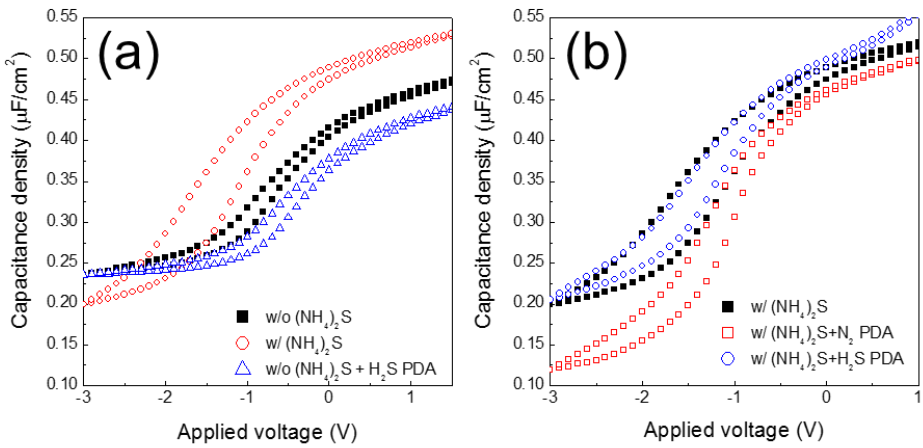

Figure 4.5 Typical C-V curves for the MIS capacitors (a) with and without $(NH_4)_2S$ wet treatment, and PDA under a H_2S atmosphere without $(NH_4)_2S$ wet treatment, and (b) with $(NH_4)_2S$ wet treatment after the PDAs under N_2 and H_2S atmospheres.

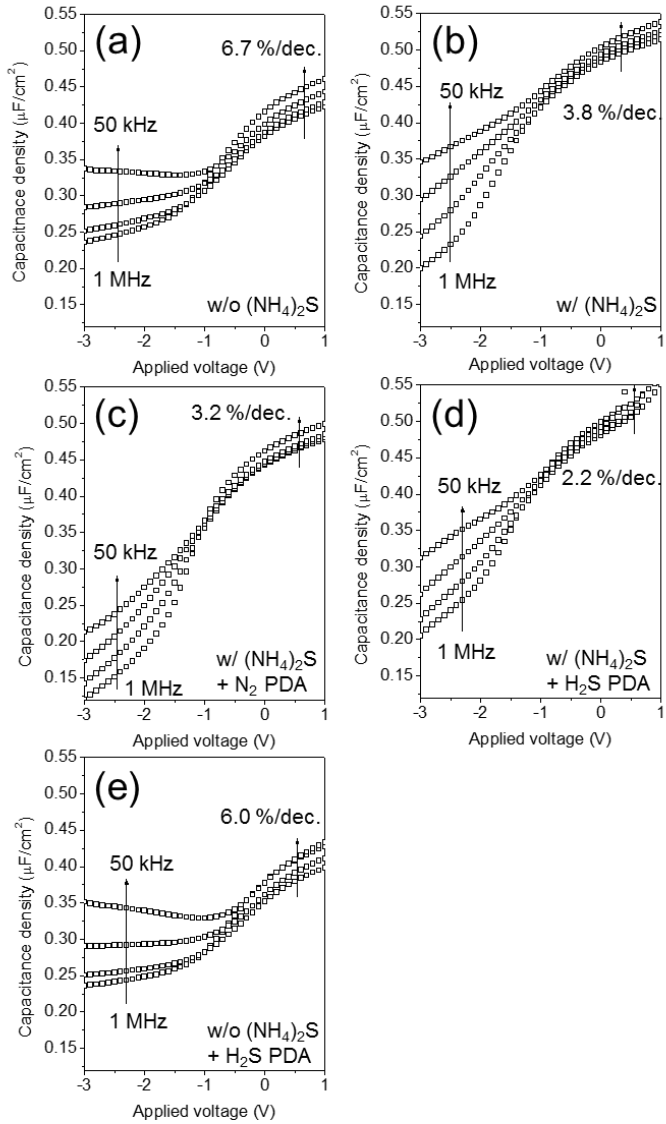

Figure 4.6 Typical C-V curves at the frequency ranging from 50 kHz to 1 MHz for the MIS capacitors with various Al_2O_3 films.

4.4. Summary and Conclusions

In summary, ALD Al_2O_3 films were grown on ultrathin-body $In_{0.53}Ga_{0.47}As$ compound semiconductor substrates. PDA under a H_2S atmosphere for the interface S passivation was performed to replace wet-based S passivation using $(NH_4)_2S$ solution. Similar S profiles with the case with $(NH_4)_2S$ wet treatment were obtained, albeit with a lower concentration. IL growth was hardly suppressed by PDA under a H_2S atmosphere, however, without $(NH_4)_2S$ wet treatment, because the IL grown during ALD was hardly curtailed by PDA. The PDA under a H_2S atmosphere induced a higher-frequency dispersion in the accumulation capacitance due to the lower S concentration at the interface, but a smaller hysteresis due to the presence of IL in this case compared to $(NH_4)_2S$ wet treatment. The PDA under a H_2S atmosphere with $(NH_4)_2S$ wet treatment further increased the S concentration at the interface, resulting in improved electrical properties.

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Chapter 5. Conclusions

In Chapter 2, the feasibility of replacing wet processing for the interface S passivation in Ge-based devices with dry processing using pre-anneanling under a H_2S atmosphere was examined. HfO_2 thin films were grown on Ge substrates, which were no treatment (control sample), dipping in $(NH_4)_2S$ solution for 10 minutes, and rapid thermal annealing under a H_2S ambient at various temperatures. Rapid thermal annealing under a H_2S atmosphere at below 400℃ was performed for the interface sulfur passivation process before the deposition of gate insulator. Sulfur was accumlated at the interface of HfO_2/Ge and interfacial layer like GeO_x was suppressed during ALD, rusulting in improved electrical properties. In the case of H_2S RTA, CET decreased because of suppresing interfacial layer, and the frequency dispersion improved in the depletion region, suggesting the decrease of interface state density in the valence band edge.

In chapter 3, HfO_2 films were grown using the atomic-layer-deposition (ALD) technique on InP substrates (n-type), which were no treatment (control sample), dipping in $(NH_4)_2S$ solution for 10 minutes, and rapid thermal annealing under a H_2S ambient at various temperatures, as well. The interface properties of the various samples were systematically observed from the viewpoints of (i) the S distribution at the interface and (ii) the IL growth behavior.

It should be noted that various sulfur treated samples have similar sulfur profile according to the SIMS analysis, and sulfur is mainly reacted with indium, which results in surface passivation. In order to investigate the improvement of interface quality, MIS capacitors were fabricated, and their electrical properties were examined. The frequency

dispersion was investigated, capacitance-voltage measurement were conducted after induced constant voltage in accumlation, and CET was calculated from C-V curves. Interface property (the decrease of Dit) of all the sulfur passivated MIS capacitor improved. Especially, in the case of H_2S RTA, the temperature increases, thermal energy is induced to reconstruction of InP surface and sulfur is rigidly bonded at InP surface. Thus, the characteristics of defect and charge trapping at surface improve, compared to $(NH_4)_2S$ pretreatment.

In chapter 4, ALD Al_2O_3 films were grown on ultrathin-body $In_{0.53}Ga_{0.47}As$ compound semiconductor substrates. PDA under a H_2S atmosphere for the interface S passivation was performed to replace wet-based S passivation using $(NH_4)_2S$ solution. Similar S profiles with the case with $(NH_4)_2S$ wet treatment were obtained, albeit with a lower concentration. IL growth was hardly suppressed by PDA under a H_2S atmosphere, however, without $(NH_4)_2S$ wet treatment, because the IL grown during ALD was hardly curtailed by PDA. The PDA under a H_2S atmosphere induced a higher-frequency dispersion in the accumulation capacitance due to the lower S concentration at the interface, but a smaller hysteresis due to the presence of IL in this case compared to $(NH_4)_2S$ wet treatment. The PDA under a H_2S atmosphere with $(NH_4)_2S$ wet treatment further increased the S concentration at the interface, resulting in improved electrical properties.

List of related publications (SCI Journal)

1. T. Seok, **Y.J. Cho**, H. Jin, D. H. Kim, D. W. Kim, S. K. Kim, C. S. Hwang, and T. J. Park, "Interface sulfur passivation using H_2S pre-deposition annealing for atomic-layer-deposited HfO_2 film on Ge substrate",in preparation.

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Abstract (in Korean)

Si 기반 소자 기술이 한계에 이름에 따라 전하 이동도가 큰 3-5 족 화합물 반도체/Ge 이 차세대 CMOSFET 의 channel 재료로 주목받고 있다. 하지만, 게이트 절연체와 channel 재료 계면에서 발생하는 저유전율을 가진 층간 물질 성장의 억제 및 계면에서의 전기적 특성이 개선 되어야 한다.

ALD 기술은 차세대 CMOS 공정에 있어 필수적인 기술이지만, 게이트 절연체 성막 공정 중 주입되는 산화제에 의해 층간 물질이 성장하며, 이때 황(sulfur)을 이용한 passivation 방법이 생성되는 층간 물질 성장 억제 및 게이트 절연체와 channel 재료의 계면 dangling bond 제거를 통한 D_{it} 저감에 있어 효과적이다.

특히, 3-5 족 화합물 반도체와 Ge 에 대한 황(sulfur)의 passivation 효과는 표면의 dangling bond 와 황(sulfur)이 결합하여 band gap 내의 interface state denisity 를 감소시켜 주는 것과 이후 고유전율 게이트 절연체 성막 공정 중 층간 물질 생성을 억제 시켜 낮은 CET 를 얻게 하는 것이다. 일반적으로 황(sulfur) passivation 공정은 $(NH_4)_2S$ 용액을 이용하는 습식 공정으로 진행되어왔다. 강염기성 용액의 특성으로 반도체 표면이 식각이 되기도 하고, 심한 경우 표면 거칠기를 증가시키기도 한다. 특히, 공정 후 대기 노출시 표면의 불균일한 산화로 인한 passivation 공정 재현성 문제가 있고, 습식 공정은 양산 공정에 적합하지 않기 때문에 본 연구에서는 H_2S 분위기 열처리의 기존 습식 공정 대체 가능성을 보고자 하였다.

Ge 기판에 황(sulfur) passivation 공정을 H_2S 분위기 열처리 공정과 $(NH_4)_2S$ 습식 공정을 전처리 공정으로 적용 비교하였다. 전처리 공정 후

기판의 표면 상태를 확인한 결과 H2S 열처리 공정의 표면 특성이 습식 공정을 진행 한 것에 비해 우수함을 확인하였다. 황(sulfur) 전처리 공정 후 ALD 공정을 이용하여 HfO_2 성막하였고, 습식 공정과 400°C H_2S 열처리 공정 모두 HfO_2/Ge 계면에 황(sulfur)가 동일한 수준으로 존재하는 것을 확인하였다. MIS capacitor 를 제작하여 계면의 전기적 특성을 평가하였고, 층간 물질 억제에 따른 CET 감소와 capacitance dispersion 감소, 계면에서의 Dit 감소로 인한 전기적 특성이 개선된 것을 확인하였다.

3-5 족 반도체는 열적 안정성이 떨어져 5 족 원소가 주로 휘발하는 현상이 있기 때문에 본 연구에서 사용된 rapid thermal annealing process 가 효과적이다. InP 에 적용하였으며, Ge 에서와 같이 습식 공정과 350°C H_2S 열처리 공정을 비교하였다. Ge 에서와 동일하게 습식 공정에 비해 InP 표면이 평활한 것을 확인하였고, ALD 공정을 이용하여 HfO_2를 성막 후 HfO_2와 InP 계면에 유사한 형태의 황(sulfur)가 존재하는 것을 확인하였다. 다만 Ge 과 달리 황(sulfur)의 량이 상대적으로 적었는데, 이는 5 족 원소 휘발로 인한 문제를 제거하고자 공정 온도를 350°C 로 낮은 것에 기인된 것으로 판단된다. 계면의 전기적 특성을 평가하기위해 MIS capacitor 를 제작하였고, 습식 공정과 H_2S 열처리 공정 모두 층간 물질 생성 억제에 따른 CET 의 감소와 capacitance dispersion 의 감소로 계면의 Dit 감소를 확인할 수 있었다. 그리고, CVS 연구를 통해 H_2S RTA 공정을 진행하는 경우 계면에서 전화 포획이 줄어들어 계면 passivation 에 습식 공정에 비해 더 효과가 있었다.

Direct wafer bonding 법으로 만들어진 InGaAs/Al_2O_3/Si wafer 상에 ALD 공정을 이용하여 Al_2O_3를 성막하였다. Al_2O_3 성막전 황(sulfur) 전처리 공정과 Al_2O_3 성막후 H_2S RTA 를 후열처리 공정의 황(sulfur) passivation

효과를 비교하였다. H_2S RTA 를 후열처리 공정으로 진행한 경우 gate 절연층과 기판사이에 존재하는 황(sulfur)의 양이 작았고, 층간 절연층의 감소에 있어 효과적이지 않았다. CET 감소 및 계면에서의 전기적 특성 개선 또한 제한적이었다. 그러나, 황(sulfur) 전처리 공정과 H_2S 후열처리 공정을 병행하여 진행한 경우 전처리 공정 대비 계면에서의 전기적 특성이 개선이 우수함을 확인할 수 있었다.

Keywords: ALD, High-k, High mobility channel, MOSFETs, Interface passivation

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