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Ph.D. DISSERTATION

**Fabrication and characterization of 3D stacked
crossbar array employing a rectifying RRAM
device**

by

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August 2016

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

COLLEGE OF ENGINEERING

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**Fabrication and characterization of 3D stacked
crossbar array employing a rectifying RRAM
device**

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A thesis submitted to the Graduate Faculty of Seoul National
University in partial fulfillment of the requirements for the
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Department of Materials Science and Engineering

August 2016

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Abstract

Resistive switching random access memory (RRAM) is becoming a strong contender as the replacement of NAND flash memory. When it is implemented in crossbar array (CBA) configuration, which does not require the employment of transistor as its selector, it becomes very cost-competitive especially in vertically integrated form. However, the highly parallel memory cell architecture of CBA gives such a serious interference problem among the cells, originated from the undesirable sneak currents flow through the unselected cells. Such a sneak current has been the main challenge that hampers the realization of RRAM to a high density storage (class) memory. Therefore, aside from enhancing the performance of a RRAM device itself, active researches on enhancing the selector performance have been reported in recent years. Nevertheless, the design criteria for such selectors have relied on the reading margin evaluation based on the preceding studies on the sneak currents analysis during read operation.

As the first part of this study, it is revealed that the sneak current issue needs to be considered more seriously even during writing margin evaluation, which have been relatively overlooked compared with the reading margin evaluation. Being further improved from the preceding sneak currents analysis, sneak current effects are even more thoroughly examined combined with the effect of resistances of memory cells and interconnection wires, and operation parameter of the device. As a result, it is shown that further intensified voltage division

effect of interconnect wires occurs due to the involvement of sneak currents through the neighboring cells. Moreover, it is also verified that the voltage applied to the unselected cells during the write operation may critically disturb those cells, incurring additional writing margin problem. The study is proposing an analytical model dealing with such sneak currents involved in the writing margin issue, provided with validation of the model through a HSPICE circuit simulation. Furthermore, the analysis is applied to a few typical resistive switching systems accompanying rectifying characteristic, mainly based on the aim of mitigating such sneak currents problem in a high density CBA.

Complimentary resistive switching (CRS) is one of the most promising system, wherein resistive switching occurs between two different high resistance states. Based on this system, every unselected cell in a crossbar array except for a selected cell features high resistance irrespective of their status, therefore, sneak currents through the unselected cells can be effectively suppressed. Transition metal oxides (TMO) have been known to be the promising resistive switching materials owing to their naturally inherent high non-stoichiometry. Resistive switching in these materials have been attributed to the migration of ionic defects according to electric field. Making use of the ionic resistive switching at conducting filaments ruptured region of a single layered TMO, an effective way of achieving a CRS just by applying a series of electrical stimulus is suggested. Combined analysis upon the time-transient current during the voltage pulsing and the resistance status obtained in the voltage sweep mode confirms and gives the detailed physical reasoning and kinetic behaviors for the

desired phenomenon in the system. It is also proven that, through a series of comparison with the samples of different materials and stacks, such property basically requires the finite amount of defects, which can be readily achieved especially in the transition metal oxides involving phase transition into the metallic phase (Magnéli), such as TiO_2 and WO_3 .

However, in order for an integration of 3 dimensional-(3D-) RRAM, higher selectivity than that of the CRS was required. Therefore, a diode selector was adopted to introduce an excellent rectifying property to a resistive switching memory, resulting in a stacked structure of one-diode one-resistance switching memory (1D1R). TiO_2 as the main functioning oxide for both the diode and the memory comprising 1D1R is fabricated at room temperature (RT), optimized for stacking of the multiple planar crosspoint structures being free from the thermal disruption issues over the repetitive stacking procedures. The RT fabricated diode showed a rectification ratio improved as much as 10^3 from the preceding diode devices for ReRAM selector applications. As the rectifying property is enhanced with the decreasing electrode area, the maximum rectifying ratio of 8.4×10^8 (at a reading voltage of 2V) even in the low resistance state (LRS) of the resistive switching memory, is obtained alongside a reliable on/off window of 10^{3-4} based on a filamentary unipolar resistive switching (URS) in $2 \times 2 \mu\text{m}^2$ crosspoint 1D1R device. Random access memory operation of erasing, programming, and reading a selected cell being uninterrupted by sneak currents from neighboring cells was demonstrated in a double-layered 3D 4×4 crossbar array. Furthermore, a 2bit-memory operation with little

overlaps among three LRS states and one HRS was performed, further shrinking the cell size down to F^2 , where F is the minimum feature size.

Keywords: resistive switching memory, crossbar array, sneak currents, writing margin, selector requirements, complimentary resistive switching, 1diode-1resistive switching memory (1D1R), 3D RRAM

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List of Abbreviations

| | |
|-------|--|
| AES | Auger Electron Spectroscopy |
| AFM | Atomic Force Microscope |
| ALD | Atomic Layer Deposition |
| BE | Bottom Electrode |
| BRS | Bipolar Resistive Switching |
| CRS | Complimentary Resistive Switching |
| EDS | Energy Dispersive Spectroscopy |
| GAXRD | Grazing Angle incidence X-ray Diffraction |
| HRS | High Resistance State |
| HRTEM | High Resolution Transmission Electron Microscope |
| I-V | Current-Voltage |
| LL | Lower Layer |
| LRS | Low Resistance State |
| NAND | Negative AND |
| RRAM | Resistive switching Random Access Memory |
| SEM | Scanning Electron Microscope |
| TE | Top Electrode |
| TEM | Transmission Electron Microscope |
| UL | Upper Layer |
| URS | Unipolar Resistive Switching |
| WM | Writing Margin |
| XRD | X-Ray Diffraction |
| XRF | X-ray fluorescence |
| 1D1R | 1diode-1resistive switching memory |
| 3D | 3-dimensional |

1. Introduction

1.1. Resistive switching Random Access Memory

Since resistance switching random access memory (RRAM) was highlighted in the early 2000s when IBM Zürich group reported a feasible resistance switching (RS) properties in a Cr-doped SrZrO₃ film,¹ RRAM has become a strong contender for non-volatile storage memory with circuit geometry of crossbar structure. The RRAM is relying on a memory operation between the low resistance state (LRS) and the high resistance state (HRS) triggered by electrical stimulus such as voltage or current application to the RS materials. Therefore, it can be applied to a simple two-terminal crossbar structure just by placing a RS material in between two metal electrodes, each playing as a word-line and a bit-line. The exclusion of the transistor within the geometry allowed its minimum cell size of $4F^2$, where F is the minimum feature size, whereas other conventional memories such as dynamic random access memory (DRAM) or NAND flash have larger cell area of $5F^2 - 8F^2$.^{3,4} A few more preferable aspects of RRAM over the NAND flash as the non-volatile storage memory is organized in Table 1.1.

Therefore, extensive researches on finding the RS materials as well as the studies on their underlying mechanisms have been conducted over recent decades. As a result, it was found that the RS is found in a variety of materials such as transition oxide materials, chalcogenides, and even polymers. Typical mechanisms that are responsible for these RS materials are: phase change

mechanism, thermochemical mechanism, valance change mechanism, electrochemical metallization mechanism, and electrostatic, or electronic mechanisms.² The RRAM operation occurs either in the manner of unipolar or bipolar resistive switching (URS or BRS). The former corresponds to the resistive switching whose set (HRS to LRS) and reset (LRS to HRS) occurs irrespective of the polarity of the applied voltage, whereas the latter corresponds to the case where set and reset occurs in the opposite polarity of the applied voltage.

TiO₂ is a material that has been studied extensively for its potential in non-charge-based resistance switching (RS) memory applications. The unipolar resistive switching (URS) phenomena in such materials, where set operations in which switching from a high resistance state (HRS) to a low resistance state (LRS) occurs, while reset operations involving switching from LRS to HRS occur under the same bias polarity, has been studied through various analytical and experimental methods. URS is mainly attributed to the formation and rupture of local conduction paths known as conducting filaments (CFs) inside the dielectric thin film.⁵ In contrast, bipolar resistive switching (BRS), where set and reset switching occurs in the opposite bias polarity, has been elucidated to occur by the localized drift of oxygen vacancies along the direction of an electric field, making the Schottky barrier modulated at the active interface, while the opposite interface remains (quasi-) Ohmic.⁶

| | |
|---|--|
| <p>Scaling limitation of NAND flash</p> | <ul style="list-style-type: none"> • Charge based operation: Reliability issue below <10nm due to the lack of the number of electrons involved in the operation. • Low electron mobility: high resistivity of Silicon channel. Heavily doped Si : $\sim 1 \times 10^{-1} \Omega \cdot m$ • 3bit operation: overlaps among the states. • Vertical integration: imperfect etching as the number of stacks increases. |
| <p>High scalability of crossbar RRAM</p> | <ul style="list-style-type: none"> • Non-charge based operation, switching mechanism relying on localized conducting region of \simnm diameter. • High electron mobility of metal wires: $10^{-7} \sim 10^{-8} \Omega \cdot m$ • $4F^2$ minimum cell size (F: feature size) (Smaller than NAND of $5F^2$) • Simple fabrication, Low cost, Low power |

Table 1.1 High scalability of crossbar RRAM compared to the NAND flash

1.2. Overcoming sneak currents issue in crossbar array

Despite the advantages of RRAM based on the crossbar architecture and such an extensive studies on the RS materials, due to the highly parallel architecture, realization of a high-density crossbar array (CBA) RRAM has long been hampered by the involvement of the sneak currents. The sneak currents problem becomes most troublesome when reading a selected cell of high resistance state (HRS). As the main principle of a RRAM device lies on its resistance change and reading the resistance difference of the selected cell, current through the unselected RRAM cells in low resistance state (LRS) can generate sneak currents interrupting the accurate reading of the selected cell. According to the previous studies on the sneak currents problem during reading in a CBA RRAM, the issue becomes more serious with increasing array size.⁴⁻⁹

Integrating two-terminal selectors such as diodes or threshold-switches is considered to be the salient method to alleviate the sneak current problem. Figure 1.2a presents one of the most straightforward voltage schemes in RRAM CBA which is called floating-scheme or V_{dd} -scheme. In this voltage scheme, all the unselected word- and bit-lines are floated while voltage with the magnitude of V_{dd} is applied only to the selected word-line, and the current flows out to the bit-line, the end of which is connected to a sense amplifier (SA). SA is assumed to be grounded (GND). Therefore, each sneak current path is comprised of two forward biased half-selected cells, with resistance of R_1 and R_3 , each being connected to the selected word- and bit-line, respectively, and a

reverse biased cell with resistance of R_2 placed in between the two forward biased cells.⁴ The consequent total parallel resistance caused by the entire sneak current components (R_{sneak}) is expressed in Figure 1.2b. Therefore, a diode selector can impede the sneak currents by limiting current flow through the reverse biased cell R_2 , while a threshold switch can perform similar function using its much low current at low voltage region through the forward biased cells of R_1 and R_3 . Such selector employed CBA RRAMs,¹⁰⁻¹² or self-selective RRAM devices,¹³⁻¹⁵ wherein the selector is embedded in the memory cell, have extensively been demonstrated in recent years. In addition, complimentary resistive switching is another type of RRAM device exploiting two rectifying characteristics of the opposite polarity as the main resistance states, which can approximately be considered as a back-to back switching diode.¹⁶⁻¹⁵

On the other hand, another attempt to mitigate such problem is to tune the bias voltage application scheme. As shown in Figure 1.1, various kinds of voltage scheme, such as applying $V_{\text{dd}}/2$ (or $V_{\text{dd}}/3$)⁸ or V_{dd} ^{5,9} to the unselected word- and bit- lines, have been suggested to entirely (or partly) exclude the currents flowing through the reverse biased cells or forward biased cells, respectively. However, these schemes induce additional current sources to the unselected word- and bit-lines, which drastically increases power consumption.

As such, a novel read-out scheme based on two-port sensing scheme has been proposed recently, mainly to increase the CBA density based on the most power efficient floating scheme. In this scheme, a word-line having the replicas of the RRAM cells is introduced as an extra sensing port in addition to the main

sensing port connected at the end of a bit-line in the floating scheme. The additional port is mainly used in estimating the amount of sneak currents within the CBA, which is denoted as I_{COMP} in the right figure of Figure 1.3a. Then the overall sensing current flowing through a selected cell is obtained in the form of I_{SENSE} , wherein the I_{COMP} is cancelled out from the main sensing port (I_{MAIN}) with adoption of an multiplication factor, for example $M-2$ in the figure. The consequent increased reading margin of the proposed two-port scheme, compared to that of the one-port scheme in Figure 1.3b, is presented in Figure 1.3c. Further accurate sensing method for each different array size and RRAM specification is proposed in detail in ref. [18], based on the optimization fo the pre- I_{COMP} multiplication factor.

Many diodes system have been proposed to impose the rectification property to RS memory. Metal oxide based diodes are preferred to their poly silicon counterparts as they can be fabricated at low temperature and high electron mobility through the metal wires. As the oxide heterostructure based pn diodes suffered small current density that limits the operation current when scaled down,^{20,21} the MIM structure based schottky diodes were extensively studied for its relatively high current density and high rectification property.²²⁻²⁵ The highest rectification ratio ever reported until recently, for the diode is 10^{10} based on MIM structure has been reported. However, it was not integrated into a 1D1R, implying that finding an appropriate memory component whose operation current level matches up with that of the diode not degrading the rectifying property when integrated into a 1D1R is not easily achieved.

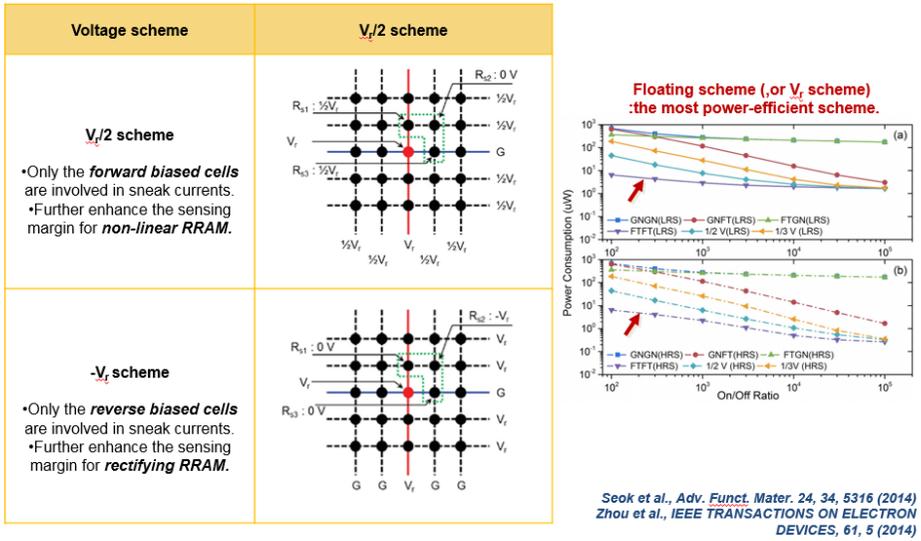


Figure 1.1 Typical voltage schemes for RRAM CBA and power consumed in each voltage scheme.

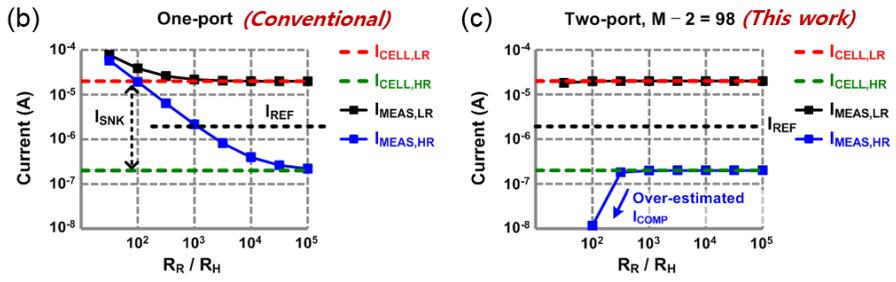
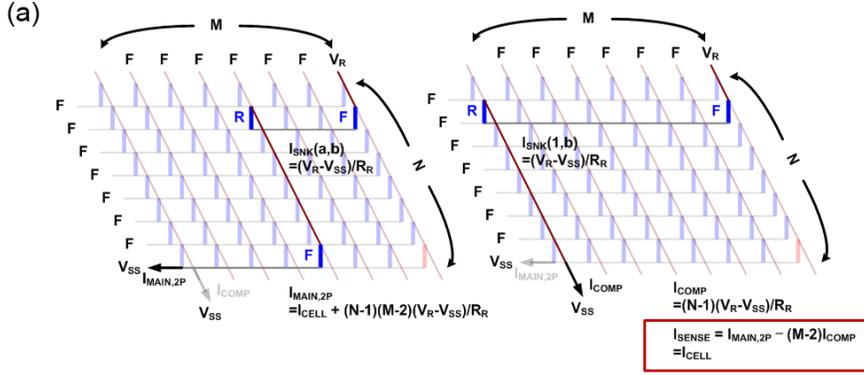


Figure 1.3 (a) main measurement current ($I_{\text{MAIN,2P}}$) path/value and compensation current (I_{COMP}) path/value of the proposed two-port current-mode sensing. Sensing currents of a 10-kbit (100 x 100) array with $R_H/R_L = 100$ based on (b) conventional one-port floating scheme and (c) the proposed two-port scheme.

1.3. Vertical integration of crossbar array

To compete with the NAND Flash, which boasts extremely high memory density up to two hundreds Gb mainly with the help of the vertical structure, vertical integration of RRAM is inevitable. There are mainly two structures of 3D crossbar RRAM. One is the stacked type by stacking multiple planar CBA planes, and the other is the vertical type utilizing the side wall structure of the current vertical NAND flash, whose schematic is presented in Figure 1.4a and Figure 1.4b, respectively. Metal wire, resistive switching memory, and selector are denoted as M, R, and S, respectively in the figures. Each structure corresponds to the concept of the word plane type and the crossline type crossbar array, respectively, presented in Seok. et al..⁴

Recent announcement on the 3D crosspoint memory of the joint product by Intel and Micron corresponds to the former structure, while the latter was reported in ref. [14]. In the stacked type 3D RRAM, a selector can be easily employed by placing a middle electrode between the RS memory and the selector. Therefore, separate engineering is available in both the RS memory layer and selector layer. However, lithography is required for every CBA layer, and the thermal margin of each layer should be considered. On the other hand, for a vertical type 3D RRAM, etching of the metal wires and insulator layers is required for forming the side wall structure, and the conformal deposition technique for the resistive switching memory layer and the selector layer is demanded. As the middle electrode joining the memory and selector layers

cannot be adopted in this structure, however, the development of a high performance self-selective RRAM device is necessary.

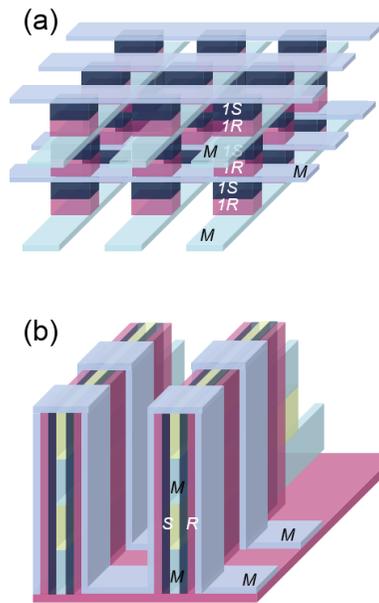


Figure 1.4 3D crossbar structure of (a) stacked type (b) vertical type

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2. Writing margin evaluation incorporating the sneak currents analysis in crossbar RRAM

2.1. Introduction

Until recently, the design criteria for selectors or for self-selective RRAM devices have mostly relied on reading margin evaluation.¹⁻⁴ As the writing margin has been considered most likely influenced by the series resistance of word and bit lines through the voltage division effect,⁶ the parallel resistance component by the sneak currents has relatively been overlooked. In a unipolar resistive switching (URS) device, reset operation (RS from LRS to HRS) occurs in the same bias polarity with set operation (RS from HRS to LRS), but with a smaller magnitude ($V_{\text{reset}} < V_{\text{set}}$). Therefore, during the resetting of a cell placed far from the voltage source and the ground in a CBA, a severe disturbance may occur to the selected cell if V_{reset} increases to as high as V_{set} due to the additional voltage taken by the interconnected wire resistances.⁵ The resistances of word and bit lines composed of metal have been neglected when they are thick and wide enough. For the nm-scale planar CBA devices (i.e., 10 nm of F and the same height dimension with a 1,000x1,000 integration density in one memory block), however, the maximum wire resistance can be as high as 40 k Ω when the resistivity of metal is taken as 10 $\mu\Omega\text{cm}$. Considering that the optimum sensing current range for the general sense amplifier is of the order of $\sim 10 \mu\text{A}$ and that the expected V_{dd} is of the order of $\sim 1 \text{ V}$, the resistance of the memory cell must be of the order of $\sim 100 \text{ k}\Omega$, meaning that the wire resistance is not ignorable. In this regard, a bipolar resistive switching (BRS) device, where set

and reset occur at the other bias polarity, would be preferred to a URS device. This study, however, further reveals an even more complex situation associated with the presence of the non-negligible effect of sneak currents on the writing margin, which can be briefly addressed as follows. The aforementioned three unselected cells comprising a sneak current are also placed under the voltage application almost close to or slightly less than the source voltage applied to the selected word line. Therefore, not only the selected cell itself but also the unselected cells can be disturbed during the operation. Moreover, as one of the three cells is always reverse-biased, the resistance state even of a BRS device may suffer a disturbance from the unwanted voltage application. Besides, the sneak currents along the selected word and bit lines can even increase the writing voltage, further narrowing down the writing voltage margin. Considering that such adverse effect of sneak currents becomes even more serious with increasing array size, the problem has to be dealt with in detail especially for the high-density CBA RRAM (>1 Mb). In this work, the writing voltage margin is calculated while taking into account the sneak currents within a CBA, wherein the critical parameters are rectification ratio r_d for a diode selector, array size (N^2) and ratio of the wire resistances of the word and bit lines between the neighboring cells (unit wire), and the cell resistance during the write operation (r_c). In general, r_d is $\gg 1$ and r_c is $\ll 1$.

Such effect of sneak currents on the writing margin has also been examined by Lu et al.⁷ The study, however, relied on the numerical simulation method, which relatively lacks an insightful description of the circuits and the mechanisms behind it. In addition, the study covered only the $V_{dd}/2$ scheme,

arriving at the somewhat trivial conclusion that it is nonlinearity that matters after all both for the diode and threshold switch selectors. In this work, an analytical model providing an in-depth description of the effect of sneak currents on the writing voltage margin is given, of which results are compared with the HSPICE simulation results, mainly based on the V_{dd} scheme. The V_{dd} scheme is the most appealing voltage scheme for the least power consumption irrespective of the type of selector adopted in RRAM CBA.^{1,3} Furthermore, based on the experiment results from the stacked 1-diode/1-resistive switching memory (1D1R) device showing a highly promising memory performance at a single cell level, a detailed method of determining the related parameters is shown in this work to suggest a plausible design strategy for enhancing the writing margin of a device.

2.2. Simulation

To confirm the disturbance in the reverse-biased cells, a situation where most of the voltage applied on a sneak current path is dropped to the reverse-biased cell was postulated. Therefore, the rectifying RRAM device in Figure 2.1 was adopted as the model RRAM device in the HSPICE simulation. All the cells were designated as being in LRS to investigate the writing (reset) margin issue for the worst case. The resistances of the device at the forward and reverse biases during the write operation were denoted as R_{cell} and $r_d R_{\text{cell}}$, respectively, while the unit wire resistance was denoted as $r_c R_{\text{cell}}$. Here, the unit wire means the word or bit line component between the neighboring cells. Then the source voltage (V_s) required to successfully deliver the writing voltage (V_w) to the selected cell was monitored while varying r_d and r_c with a fixed R_{cell} of 50 k Ω . The voltage applied to a reverse-biased cell (V_r) was simultaneously monitored. Netlists of 10x10, 20x20, 40x40, and 100x100 RRAM arrays were generated using Cadence. To simulate a higher-density CBA with an array size above 100x100, a simulation model that enables the expansion of the array size was used based on the following assumption: an array size increased N^2 -fold is equivalent to an R_{wire} increased N -fold or to an r_d decreased N^2 -fold. As long as the number of segmentations is sufficient, the assumption is correct. This approach is similar to the pi- and T-segment models, which have been widely used by IC designers to estimate the RC time delay of a long wire.

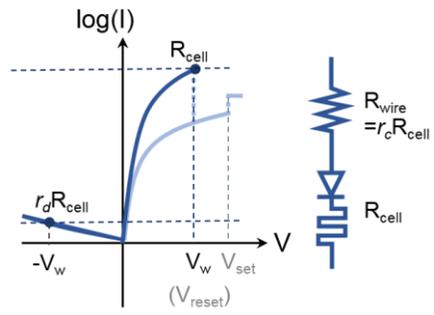


Figure 2.1 Model RRAM device used in the simulation.

2.3. Results and Discussions

The aforementioned disturbance to the reverse-biased cells in the sneak current paths was evidenced by the simulation results shown in Figure 2.2. The simulation was carried out for the worst case of a floating scheme, as described in Figure 2.2a, where the selected cell (yellow bar) is placed at the farthest corner from the voltage source and the ground, and all the selected and unselected cells in the array are in LRS. Under this circumstance, the adverse effects of both the wire resistances of the selected word and bit lines and the sneak currents are maximized. In addition, the simulation was conducted for the CBA with rectifying RRAM devices, mainly to verify the writing margin issue of the reverse-biased cells. The rectification ratio r_d of a diode was more conveniently conceived as the ratio of the resistance at the reverse bias to the resistance at the forward bias of the RRAM device for this simulation. Then the voltage drop on each (reverse-biased) unselected cell among cells 1, 2, and 3 indicated in Figure 2.2a was monitored using an HSPICE simulator while applying a source voltage of V_s on the selected word line, which is required to deliver V_w to the selected cell for a successful write operation. As a result, as shown in Figure 2.2b, the increasing r_d at a fixed crossbar array size of 1 Mb, or $N \times N=10^6$, led to the generally increased reverse bias voltage application to the unselected cell. As a sneak path is composed of two forward-biased cells and a reverse-biased cell in addition to the parasitic wire resistances, the increased r_d of the device results in a relatively negligible voltage drop on the forward-biased cells and the wire resistances, but the most part of the voltage drops on the reverse-biased cell. Provided with a sufficiently high r_d (larger than

10^5), a voltage almost as high as the source voltage (V_s) is applied to the reverse-biased cells. Therefore, even the BRS cells, in which set occurs in the reverse bias, are likely to be disturbed during the reset operation of the selected cell (and vice versa). On the other hand, the magnitude of the voltage applied to the reverse-biased cells varies according to the position of the cells. This is because despite the same number of unit wires, $2N$, contribute to a sneak current path of every reverse-biased cell, the segments of the *selected* word and bit lines and of the *unselected* word and bit lines involved in the path vary according to the position. This variation could be understood quantitatively from the following consideration. The overall resistance of an arbitrary sneak path consists of word and bit line resistances in addition to the three cell resistances mentioned above. Depending on the location of the reverse-biased R_2 within an array, however, the involved word and bit lines are composed of selected or unselected unit segments of the wires. For example, in Figure 2.2a, the word and bit lines along the sneak path involving cell 1 are almost completely composed of *unselected* segments of the unit wires whereas the path involving cell 3 is almost completely composed of *selected* unit segments. As the high current through the selected cell (i_{select}) flows through the *selected* word and bit lines whereas only the small sneak current (i_{sneak}) flows through the *unselected* word and bit lines, the voltage drop along the *selected* word and bit lines is much higher than that along the *unselected* ones. This means that a reverse-biased cell along a sneak current path with a higher portion of the *selected* word and bit lines suffers a relatively lower disturbing voltage applied to the cell because a higher portion of V_s is dropped over the involved *selected* word and

bit line components. The consequent voltages on the reverse-biased cells (V_r), cells 1, 2, and 3, which represent the three typical cases for the sneak paths, are expressed as follows:

$$V_{r,cell1} = -\{V_s - 2R_{wire}i_{select} - 2(N - 1)R_{wire}i_{sneak}\} \quad (1)$$

$$V_{r,cell2} = -\{V_s - NR_{wire}i_{select} - NR_{wire}i_{sneak}\} \quad (2)$$

$$V_{r,cell3} = -\{V_s - 2(N - 1)R_{wire}i_{select} - 2R_{wire}i_{sneak}\} \quad (3)$$

$$i_{select} \gg i_{sneak} \quad (4)$$

$$\therefore |V_{r,cell1}| > |V_{r,cell2}| > |V_{r,cell3}| \quad (5)$$

Consequently, cells 1 and 3 are the most and least disturbed cells, respectively, during the reset operation of the selected cell. In a device with V_{set} at the opposite polarity of V_{reset} , in a BRS memory, the most disturbed cell is likely to suffer a set process unless its $|V_{set}|$ at the reverse bias is sufficiently higher than $|V_{r,cell1}|$. In this sense, the writing voltage margin is defined as $|V_{set}| - |V_{r,cell1}|$. On the other hand, as shown in Figure 2.2c, the increasing array size results in a decrease in the voltage application on the reverse-biased cells because the increased number of unit wires involved in a sneak current path induces a more pronounced voltage drop along the wires. For the array size above 10^7 , even the magnitude of $V_{r,cell1}$ becomes significantly less than V_s , which is among the merits (or is perhaps the only merit) of the involvement of wire resistances in CBA RRAM.

Based on the results shown in Figure 2.2b and Figure 2.2c, the magnitude of the reverse disturbing voltage on the most disturbed cell ($V_{r,cell1}$ in Figure 2.2a) can be considered the same as the source voltage (V_s) when a sufficient rectifying property is provided in the RRAM device. Then the writing voltage

margin becomes $|V_{\text{set}}| - V_s$. The V_s can be derived based on an analytical model addressing the series resistance effect of the wires on the selected cell. Combined with i_{select} and i_{sneak} , the wire resistances of the selected word and bit lines induce a substantial voltage loss to the selected cell. While i_{select} can be conceived as a constant value of V_w/R_{cell} irrespective of the size of CBA, the effect of i_{sneak} on the voltage loss to the cell becomes detrimental with increasing array size. Therefore, such voltage drop along the selected word and bit lines needs to be expressed in terms of r_d , N , and r_c . To attain this goal, it is noted that all the sneak currents that originated from the selected word line converges to the selected bit line through each half-selected cell as shown in Figure 2.3. As a result, the amount of current flowing along a unit wire element of the selected word and bit lines increases the farther the wire element is placed from the selected cell, due to the loss and gain of sneak currents along the selected word and bit lines, respectively. Then a tricky situation arises as a substantial voltage drop occurs on the selected word and bit lines; each sneak current path is placed under a different voltage application according to the position of its half-selected cells. This was also confirmed from the HSPICE simulation results in Figure 2.2b and Figure 2.2c. The consequent numerous different sneak current values make the situation extremely complicated for analytical interpretation. Nevertheless, thanks to the highly suppressed i_{sneak} flowing through the reverse-biased cells, wherein the value is barely affected by the applied voltage, it is reasonable to assume that all the voltages applied to each sneak path are identical. Therefore, all the reverse-biased cells are conceived to have the same amount of current flow. Here, the voltage applied to every

reverse-biased cell is approximated to be $-V_s$, which is the upper limit of the possible voltage application across a reverse-biased cell. The effect of such an approximation on the deviation between the analytical and simulation results will be elucidated later in Figure 2.4. In addition, despite the fact that this approximation can hold only with a sufficiently high r_d , the non-negligible effect of such very limited sneak currents on the voltage drop of the selected word and bit lines will be confirmed by the HSPICE simulation results in Figure 2.4. Based on this approximation, the amount of every i_{sneak} that escapes from/merges with the selected word/bit line can be approximated to be the same irrespective of its escaping/merging position on the selected word/bit line. Each sneak current collected at a half-selected cell along the selected bit line consists of the currents flowing through the $(N-1)$ reverse-biased cells (see Figure 2.3b). Consequently, the analytical solution for the sneak current flowing through a single half-selected cell on the selected word or bit line, which is represented by the blue arrow in Figure 2.3a and Figure 2.3b, respectively, is given as

$$i_{\text{sneak}} \approx (N - 1) \frac{V_s}{r_d R_{\text{cell}}}. \quad (6)$$

While the collected sneak current at an arbitrary cell on the selected bit line can be understood from the explanation above, it can be understood that the same amount of current flows out from each cell on the selected word line. According to Kirchhoff's rule, i_{wN} and i_{bN} , denoting the currents flowing along the N -th unit wire of the selected word and bit lines from the selected cells, are obtained in the form of an arithmetic sum of i_{sneak} in addition to i_{select} as equation (7) below. Identical values were obtained for the same N value.

$$i_{wN} = i_{bN} \approx \frac{V_w}{R_{\text{cell}}} + (N-1)^2 \frac{V_s}{r_d R_{\text{cell}}} \quad (7)$$

The above equation can be alternatively understood from the equivalent circuit, with which the CBA can be considered a parallel resistor circuit composed of R_{cell} and R_{sneak} , where $R_{\text{sneak}} = r_d R_{\text{cell}} / (N-1)^2$ according to Figure 1.2b. From the above-derived currents flowing at the unit wires of the selected word and bit lines, the following voltage drop on the selected word and bit lines, designated by ΔV_{WL} and ΔV_{BL} , were obtained:

$$\Delta V_{\text{WL}} = R_{\text{wireWL}}(i_{w1} + i_{w2} + i_{w3} + \dots + i_{wN}), \quad (8)$$

$$\Delta V_{\text{BL}} = R_{\text{wireBL}}(i_{b1} + i_{b2} + i_{b3} + \dots + i_{bN}), \quad (9)$$

where R_{wireWL} and R_{wireBL} denote the unit wire resistances of the word and bit lines. By substituting (7), (8), and (9) into equation (10) below, V_s can be obtained as an explicit function of V_w , as in equation (12).

$$V_s - \Delta V_{\text{WL}} - \Delta V_{\text{BL}} = V_w, \quad (10)$$

$$\therefore V_s = \frac{\left[1 + \frac{N(R_{\text{wireBL}} + R_{\text{wireWL}})}{R_{\text{cell}}} \right]}{\left[1 - \frac{(N-1)N(2N-1)}{6r_d} \frac{(R_{\text{wireBL}} + R_{\text{wireWL}})}{R_{\text{cell}}} \right]} V_w \quad (11)$$

with $R_{\text{wireBL}} = R_{\text{wireWL}} = R_{\text{wire}}$, and $N \gg 1$

$$\therefore V_s = \left(\frac{1 + 2N \frac{R_{\text{wire}}}{R_{\text{cell}}}}{1 - \frac{2}{3} N^3 \frac{R_{\text{wire}}}{r_d R_{\text{cell}}}} \right) V_w = \left(\frac{1 + 2Nr_c}{1 - \frac{2}{3} N^3 \frac{r_c}{r_d}} \right) V_w \quad (12)$$

The V_s derived from the proposed model includes the effect of i_{sneak} , expressed as a function of r_d and the array size (N^2), in addition to the conventional considerations on R_{wire} with respect to R_{cell} (r_c). Irrespective of the N , r_d , and r_c values, the pre- V_w coefficient is larger than the unity, meaning that a voltage must be added to compensate for the voltage drop along the selected word and

bit lines. Therefore, the (simultaneously) reverse-biased cells along the sneak paths, placed under the $-V_s$ voltage application, suffers a reverse voltage larger than V_w when writing the selected cell with the voltage of V_w . Therefore, in this sense, a 1D1R or self-(diode-embedded)-rectifying RRAM property should have a reverse operation voltage larger than the operation voltage at the forward bias so as not to be disturbed when writing a selected cell. The usefulness of equation (12) can be most evidently noted from the fact that it is a general equation for any necessary source voltage for both set and reset, and the same holds for both BRS and URS. It must also be noted that r_c varies depending on whether it is set or reset; it is large and small for reset and set because the memory cell resistance is small (before reset) and large (before set), respectively. As the pre- V_w coefficient increases with increasing r_c , and a higher pre- V_w coefficient is unfavorable for the circuit operation, it can be understood that reset is most likely problematic in the general BRS and URS. There could be other cases, however, where set is even more problematic, as will be shown in Figure 2.5b.

In Figure 2.4, the validity of the analytical solution for V_s from the proposed model is confirmed by comparing the calculated V_s/V_w values with those from the HSPICE simulation, with respect to different r_d , r_c , and N^2 values. In Figure 2.4a, Figure 2.4b, and Figure 2.4c, it is obvious that the V_s/V_w values from the proposed analytical model coincide well with those from the simulation, except for when a too large r_c , a too small r_d , or a too large N was applied. Such deviation is mainly attributed to the approximation made in the above model: the V_r for every reverse-biased cell was approximated to be $-V_s$. As $-V_s$

corresponds to the upper limit of the possible voltage application to the reverse-biased cells, the amount of sneak currents in the system may be overestimated by adopting the approximation. This is the case when V_r becomes remarkably smaller due to the increasing voltage partaken by the wire elements, which is ascribed to low diode performance (small r_d), large wire resistance (large r_c), and large array size (large N^2). The actually reduced effect of i_{sneak} on the voltage drop on the selected word and bit lines in turn gives a V_s smaller than the value estimated from the analytical solution (Figure 2.4a-c). It is particularly noteworthy that V_s is obviously affected by the performance of the diode selector (r_d) for a large-array-size region above 1 Mb (Figure 2.4b and Figure 2.4c), which strongly supports the importance of taking into account the effect of sneak currents even in the writing margin evaluation of a high-density CBA. Therefore, ensuring a high r_d is critical for both stable reading and writing.

Next, more detailed discussions are made considering the disparate shapes of the switching current-voltage (I-V) curves of the RRAM cells. In fact, there are numerous reports on the detailed switching I-V curves, but they can be duly classified into three cases, as shown in Figure 2.5, for the purpose of assessing the writing margin according to the model of the present work. In Figure 2.5a, the reset and set operation of the bipolar RRAM occurs at the forward and reverse biases, respectively (BRS rectifying-set), whereas in Figure 2.5b the reset and set occur at opposite bias polarities (BRS rectifying-reset). The type of switching I-V curve in Figure 2.5a is more unfavorable in terms of the writing margin because the reset occurs in the forward-bias region, and as such, the highest i_{select} occurs, making r_c the largest. In this case, the writing margin

can be represented by $|V_{\text{set}}| - V_{\text{S}}$. If the writing margin is not sufficient (i.e., $|V_{\text{set}}|$ is not sufficiently large), the unselected cell (reverse-biased cell) could be unintentionally set. In contrast, in Figure 2.5b, the set occurs in the forward-bias direction, and as such, the memory cell resistance could be higher, making the r_c smaller. In this case, the writing voltage margin is therefore $|V_{\text{reset}}| - V_{\text{S}}$, with V_{reset} denoting the reset voltage of the device at the reverse bias. If the $|V_{\text{reset}}|$ is not sufficiently large, unintentional resetting of the unselected cell could occur. On the other hand, the URS-rectifying RRAM shown in Figure 2.5c has both set and reset voltages at the forward bias. As has been discussed in previous reports,^{4,6} the resetting of a selected cell may fail when the V_{S} for reset increases to as high as the V_{set} of the cell due to the series resistance effects of the selected word and bit lines. In this case, the writing voltage margin is thus $V_{\text{set}} - V_{\text{S}}$. The simultaneous voltage application to the reverse-biased unselected cells may cause a breakdown if the breakdown strength of the diode is not sufficiently high. Therefore, with V_{b} being the breakdown voltage of the cell, the writing voltage margin in this case is determined by the smaller value between $|V_{\text{b}}| - V_{\text{S}}$ and $V_{\text{set}} - V_{\text{S}}$.

As a consequence, a small writing voltage margin of a RRAM device becomes another critical constraint for integrating it into a high-density CBA. Recently, Hsu et al.⁹ and Yoon et al.⁸ reported promising rectifying RRAM devices with multi-level resistance states. Each type of RRAM corresponds to the cases shown in Figure 2.5a and Figure 2.5b, respectively. As shown in Table 2.1, however, their writing voltages at the forward bias are larger than their counterparts at the reverse bias. As a voltage larger than the writing voltage of

the selected cell is supposed to apply at the reverse bias of the most disturbed cell, it means that there are actually no writing voltage margins for these cases. For refs. [9]/[8], when the most disturbed cell in a sneak path is in HRS/LRS, it will be easily set/reset during the reset/set operation of a selected cell. Therefore, for V_{dd} scheme application, their operation voltages need to be adjusted, taking advantage of their multi-level resistive switching characteristics; otherwise, only the $V_{dd}/2$ scheme will be applicable. In that case, the device characteristics should be re-examined based on nonlinearity rather than on the rectification ratio.

Instead, the rectifying URS RRAM presented by the authors in this work will be used as an example for appropriate writing margin evaluation. Based on the related parameters organized in Figure 2.5d, the detailed evaluation method will be shown below. As the writing voltage margin (WM) is defined as the difference between V_s and V_{set} , V_{reset} or even V_b , it can be expressed by equations (9) and (10), where c is a constant that represents the ratio between V_w and V_{set} , V_{reset} or V_b .

$$\therefore WM = \left(c - \frac{1 + 2Nr_c}{1 - \frac{2}{3}N^3 \frac{r_c}{r_d}} \right) V_w \quad (13)$$

$$\therefore WM(\% \text{voltage}) = \left(c - \frac{1 + 2Nr_c}{1 - \frac{2}{3}N^3 \frac{r_c}{r_d}} \right) \times 100 \quad (14)$$

The higher c is, the smaller the disturbance in the unselected cell, but if it is too high, the operation voltage of the RRAM increases too much. As such, c must be carefully chosen to achieve a subtle balance between disturbance-free

operation and low-voltage (thus, low-power) operation. In this work, the appropriate c region was arbitrarily taken to be between 1.2 and 4, but the precise value should be determined based on the specific RRAM material. In Figure 2.6a and Figure 2.6b, the writing margins obviously decrease as the array size increases, where a higher value of r_d and a lower value of r_c are beneficial to keep the WM at a higher array size. An arbitrary value of $c=2$ was adopted for these calculations. Figure 2.7 includes the results from the cases of $c=1.2$ and 1.4. Based on these results, the allowable array size, below which a certain WM is guaranteed, can be evaluated. The CBA size (N^2) allowing for a 10% WM of a rectifying RRAM cell with different r_d and r_c values is estimated in Figure 2.6c and Figure 2.6d, respectively. High r_d , low r_c , and high c values are required to increase the CBA size while maintaining a certain WM. From the results, it is worth noting that increasing the selector performance (increasing r_d) has merit only when a sufficiently high c value is provided.

As the possible array size allowing for a certain WM is determined by r_d and r_c , the consequent power consumed in each array size can be calculated. The array power is equivalent to the power consumed at the voltage source, which is conveniently derived by multiplying V_s by the total current flow through the selected word line (i_{wN} in Figure 2.3b).

$$P = V_s \times i_{wN} = V_s \left[\frac{V_w}{R_{\text{cell}}} + (N' - 1)^2 \frac{V_s}{r_d R_{\text{cell}}} \right] \quad (15)$$

$$\text{with } R_{\text{wireBL}} = R_{\text{wireWL}} = R_{\text{wire}}, N' \gg 1,$$

$$\therefore P = \left(\frac{1 + 2N'r_c}{1 - \frac{2}{3}N'^3 \frac{r_c}{r_d}} \right) \left[1 + \frac{N'^2}{r_d} \left(\frac{1 + 2N'r_c}{1 - \frac{2}{3}N'^3 \frac{r_c}{r_d}} \right) \right] \frac{V_w^2}{R_{\text{cell}}} \quad (16)$$

where N' stands for the number of word and bit lines that guarantee a 10% WM. The power consumed in the entire array is proportional to the power consumed by a single cell ($\frac{V_w^2}{R_{\text{cell}}}$). That is, when a cell is placed in a crossbar array, additional power consumption is introduced by the parasitic series and parallel resistances from the wires and neighboring cells, respectively. The power consumed in the array size (N^2) allowing for a 10% WM is calculated with respect to r_d and r_c , as shown in Figure 2.8a and Figure 2.8b. With a fixed c value, each array size is determined to share the same V_s value: $V_s=1.1, 1.3, 1.9,$ and $3.9 V_w$ for $c=1.2, 1.4, 2,$ and $4,$ respectively. As the term $\frac{1+2Nr_c}{1-\frac{2}{3}N'^3\frac{r_c}{r_d}}$ in equation (12) stands for V_s/V_w , which is fixed for a given c value, only the changes in the N^2/r_d term according to r_d and r_c contribute to the results in Figure 2.8a and Figure 2.8b, respectively.

The proposed analytical model can be further applied to a CBA with RRAM employing a threshold switch selector. In this case, the amount of sneak currents within the CBA is considered differently from the case of the RRAM with a diode selector because of the different I-V characteristics of the threshold switch compared to those of diode.

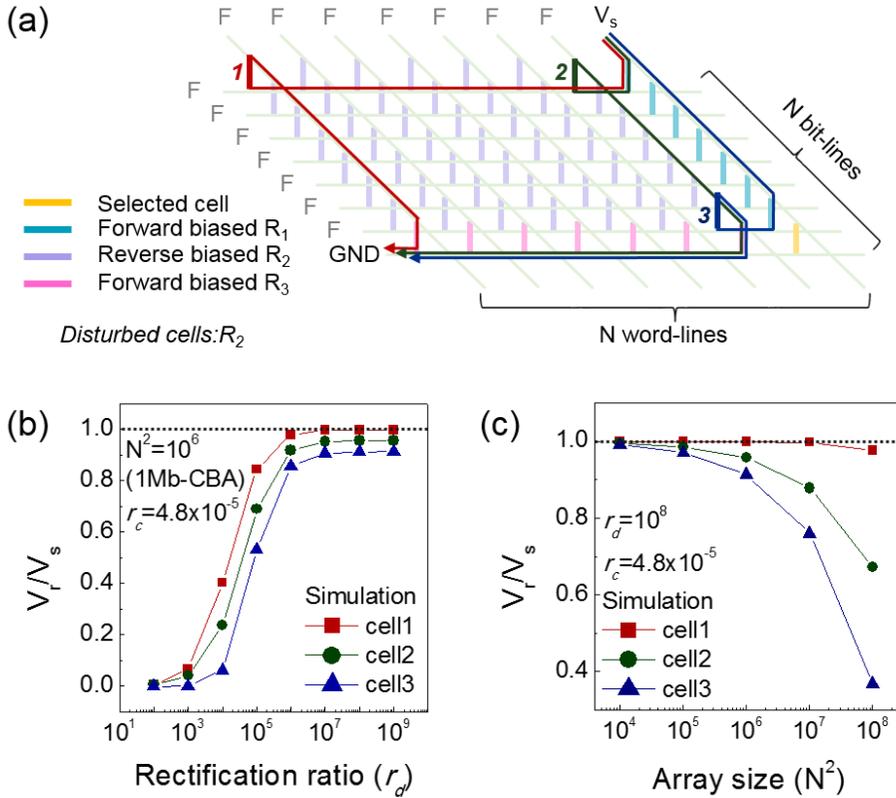
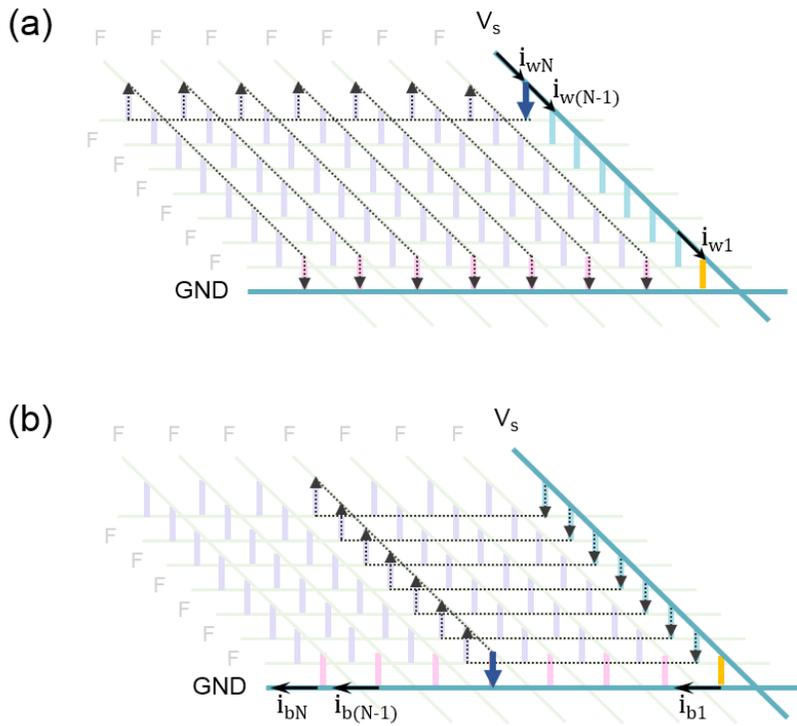


Figure 2.2 (a) Disturbed cells lying on the sneak current paths in the RRAM CBA employing a diode selector. Simulated results on the actual voltage application on the disturbed cells (V_r) according to their positions, with respect to (b) the rectification ratio of the RRAM cells with a fixed array size of 10^6 (1 Mb) and (c) the array size with a fixed rectification ratio of 10^8 .



➡ Sneak current through a single half-selected cell on the selected word-, or bit line.

Figure 2.3 Effect of the sneak currents (i_{sneak}) on the voltage drop of the selected (a) word line and (b) bit line.

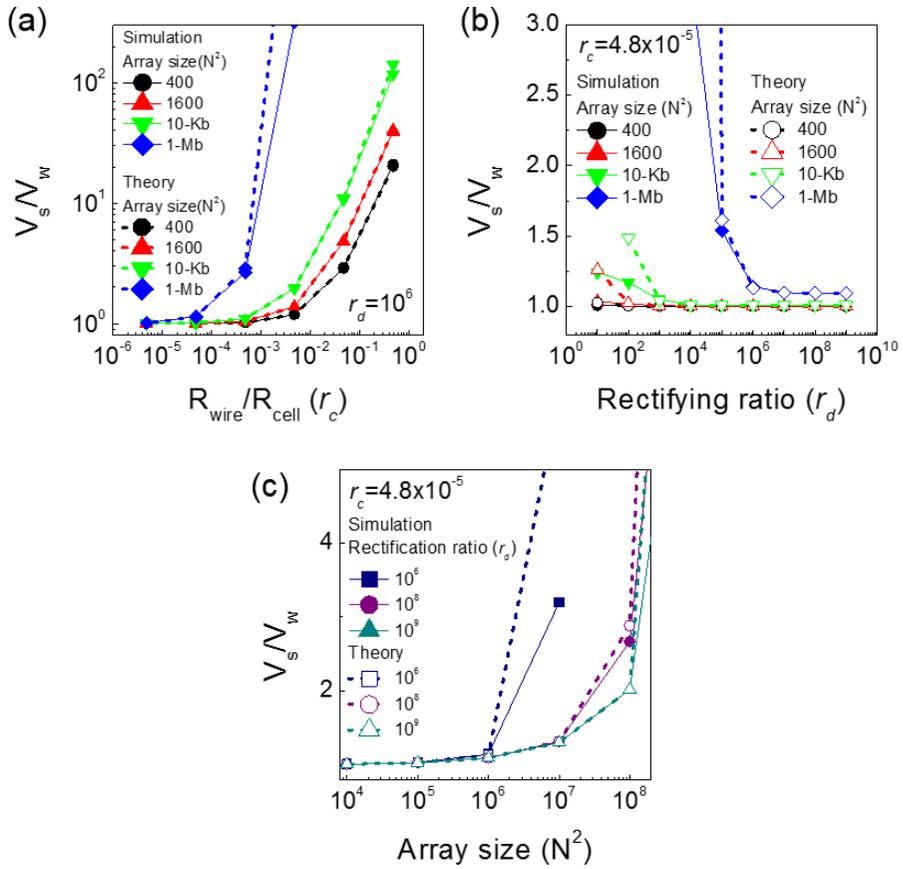


Figure 2.4 Comparison of the theoretical value of V_s/V_w of the proposed model and the V_s/V_w from the HSPICE simulation according to (a) r_d , (b) r_c , and (c) N^2 .

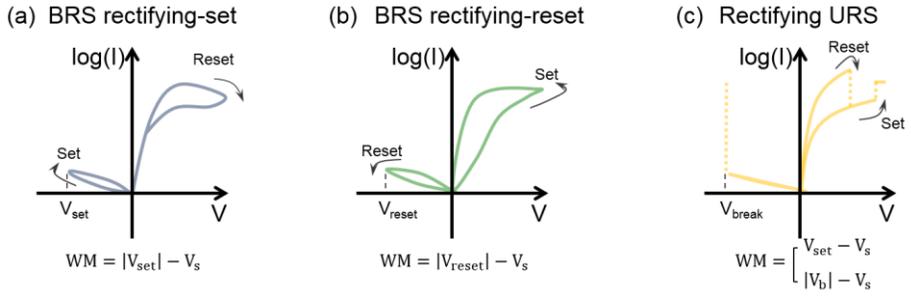


Figure 2.5 Typical I-V curves of rectifying RRAM devices employing or embedding a diode selector.

| Type of rectifying crossbar RRAM | BRS rectifying-set | BRS rectifying-reset | Rectifying URS |
|---|--------------------|-----------------------------------|--|
| Rectification ratio(r_d) | 10 (at $\pm 6V$) | 6.50×10^5 (at $\pm 4V$) | 8.9×10^8 (at $\pm 2V$) |
| R_{cell} | 7.5×10^7 | 4.14×10^6 | 1.62×10^3 |
| V_w | 6V (V_{reset}) | 8V (V_{set}) | 2.5V (V_{reset}) |
| Operation voltage concerned in the writing margin | $V_{set} = -5V$ | $V_{reset} = -4V$ | $V_{set} = 5V$ $V_{breakdown} < -15V$ |
| V_{dd} -scheme | Not appropriate | Not appropriate | Appropriate |

Table 2.1 Parameters related to the writing margin evaluation for each type of RRAM device presented in Figure 2.5.

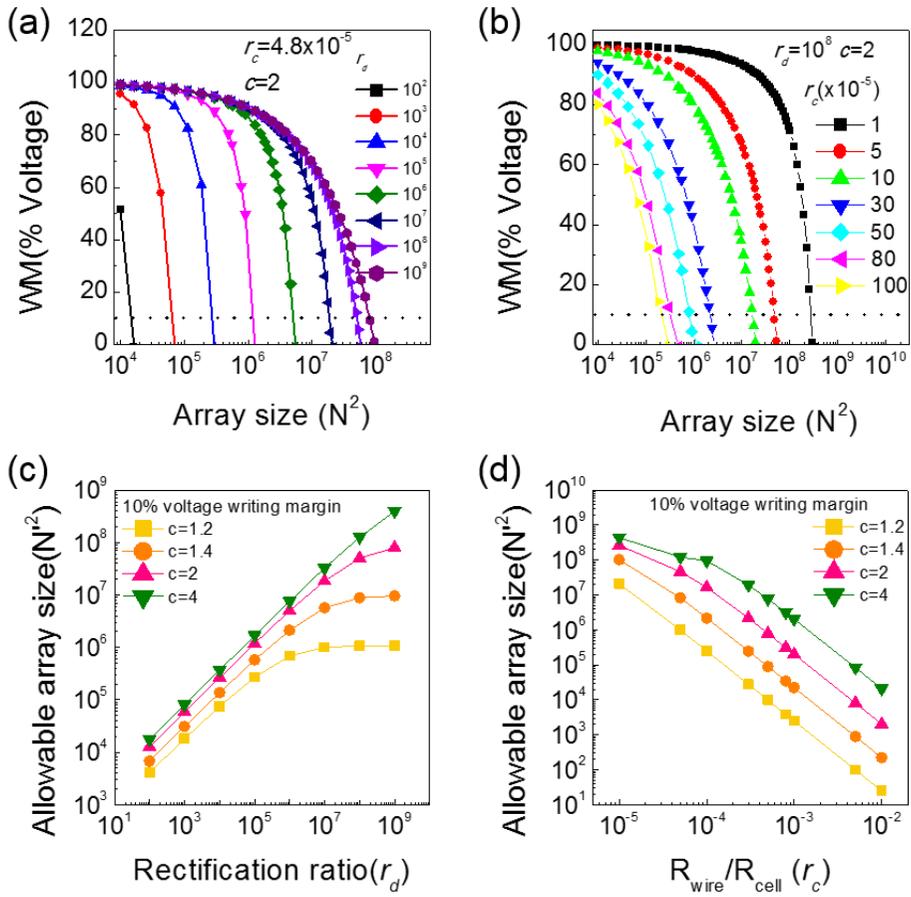


Figure 2.6 Percent writing margin with a dashed line representing the 10% margin with respect to (a) r_d and (b) r_c . Array size allowing for a 10% writing margin according to (c) r_d and (d) r_c .

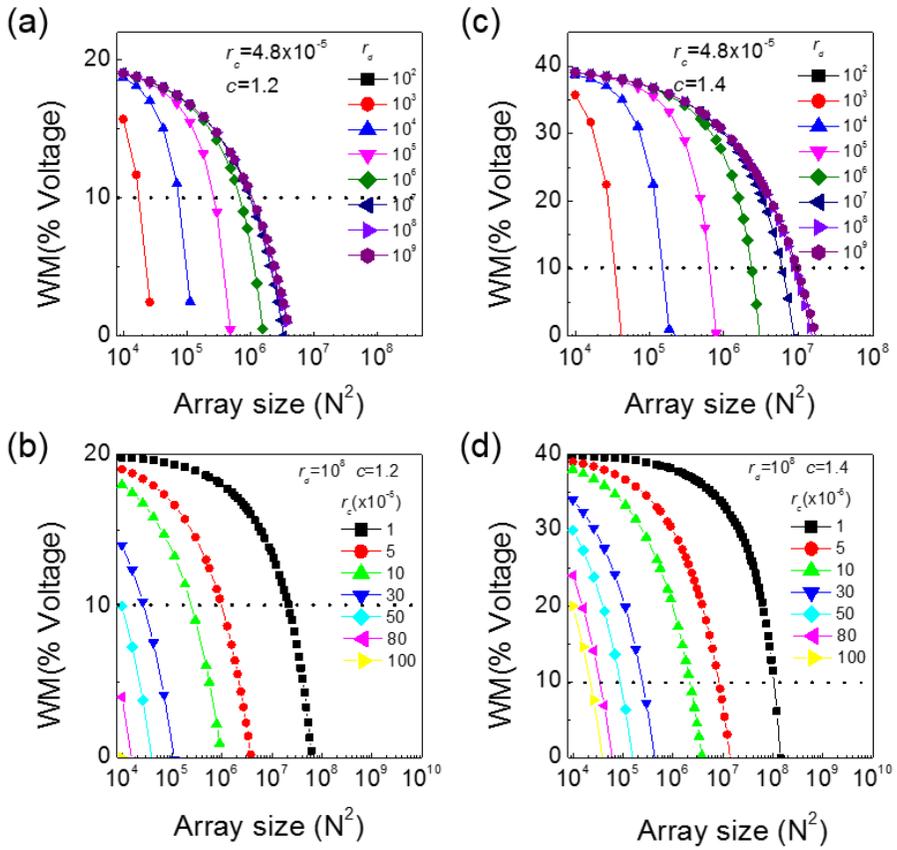


Figure 2.7 Percent writing margin with a dashed line representing a 10% margin with respect to (a), (c) r_d with a fixed $r_c = 4.8 \times 10^{-5}$; (b), (d) r_c with a fixed $r_d = 10^8$. $c = 1.2$ and $c = 1.4$ were adopted for (a), (b) and (c), (d), respectively.

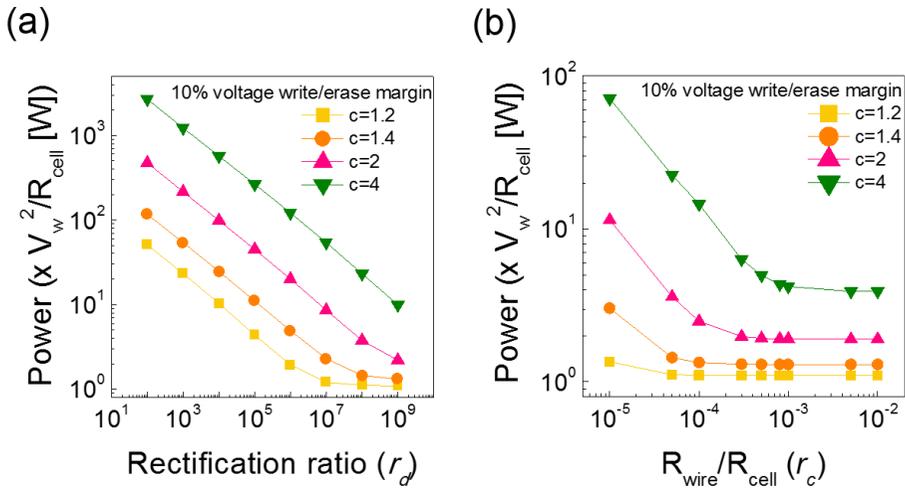


Figure 2.8 Power consumption according to (a) r_d and (b) r_c . At each point, the power consumption was derived from different array sizes, which have been determined as N^7 to guarantee a 10% writing margin according to the r_d and r_c values shown in Figure 2.6b and d.

2.4. Summary

Due to the extremely parallel geometry of the passive CBA RRAM, the disturbance problem during memory reading has been highlighted, and the studies on the adoption of appropriate selectors and bias schemes have been extensive. The possible influences of sneak paths and wire resistances on the writing voltage margin in the same structure, however, have been relatively overlooked despite their importance. This work set up an analytical model to evaluate the voltage drop across the selected metal wires (word and bit lines) and the maximum (worst-case) reverse voltage that is simultaneously applied to the unselected cells. Due to the generally higher current along the selected path compared with the current along the sneak path, the maximum reverse voltage applied to the unselected cell is always higher than the writing voltage of the selected cell. This problem becomes even more serious when the voltage drop across the selected wires becomes excessive either due to the high resistivity or small cross-section of the wires, which increases the source voltage required to successfully write the selected cell. To setup an analytical model for the writing voltage margin, which is defined as the difference between the maximum reverse voltage across the unselected cell and the operation voltage at the reverse bias, evaluation was performed and the results were compared with the HSPICE simulation results, confirming the validity of the model.

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3. Complimentary resistive switching in single layered transition metal oxides

3.1. Various ionic bipolar resistive switching modes via URS reset in Pt/TiO₂/Pt device

3.1.1. Introduction

As has been mentioned in the introductory part, TiO₂ is a material that has been studied extensively for its potential in non-charge-based resistance switching (RS) memory applications¹⁻⁹ One of the most intriguing aspect of this material is that both URS and BRS can be achieved from the same sample by adjusting the current-voltage (I-V) sweep scheme.¹⁰⁻¹⁵ For example, transitions between URS and BRS in a given TiO₂ sample are commonly observed, suggesting that the two mechanisms are not independent. While performing the set switching process on a URS-reset sample, the set power applied to the sample can vary depending on the resistance/conductance of the URS reset sample, and the I-V operation sequences. The dissipated power during the electroforming can change the resistive switching modes between URS and BRS, or even the type of BRS.^{11,12} Kim et al. have revealed that BRS in TiO₂ can be understood from the bias-polarity-dependent carrier trapping and de-trapping processes, which are called electronic-BRS, assuming an asymmetric potential barrier and a high density of traps within the localized region where the CFs are ruptured.^{13,14}

In this study, the BRS model will be further developed based on the drift of oxygen vacancies within the locally ruptured CF region, which shows forward

and reverse rectification properties. This could be understood as a type of ionic bipolar resistive switching due to the oxygen ion drift according to bias polarity from an effective microscopic structure of Pt/TiO_{2-x}/TiO₂/Ti₄O₇/Pt, and the corresponding band structure at the ruptured CF region. The BRS model basically assumes a mixed electronic-ionic conduction system, which occurs in a localized area of the URS-reset CF region, while other parts of the sample do not contribute to the RS.¹⁵

However, despite applying an identical I-V sweep sequence, quite different BRS behaviors were achieved, and even URS set was sometimes observed with such a low I_{CC} level. Depending on the configuration and chemical composition of the pre-existing filament, the Joule heating energy consumed during the URS reset process, the amount of oxygen vacancies and their distribution within the filament ruptured region would vary, which would bring about the diversity in the subsequent resistive switching behaviors. It is supposed that the highly asymmetric oxygen vacancy configuration generated during the URS reset encourages the subsequent BRS set, while the highly insulating and symmetric oxygen vacancy (and accompanying potential) configuration with few oxygen vacancies are more likely to lead to the subsequent URS set. In this work, a large number of switching experiments involving sequences of electroforming – URS reset – BRS set/reset were performed, and the diversity of BRS was classified. The possible origins of such diverse BRS behaviors were pursued by tracking back the URS properties of each BRS event.

3.1.2. Experimental section

Pt/TiO₂/Pt sample was fabricated by depositing a 60-nm-thick TiO₂ film on a 100-nm-thick Pt/SiO₂/Si substrate by plasma-enhanced atomic layer deposition at 250°C, using Ti-tetraisopropoxide and plasma-activated O₂ as the Ti-precursor and the oxygen source, respectively. Structural and chemical characterizations using X-ray diffraction and X-ray photoelectron spectroscopy showed that the as-grown TiO₂ film has a polycrystalline anatase structure with an O:Ti ratio of ~2.1. The grain shape was columnar, and no specific preferred crystallographic orientation was observed.⁸ 70-nm-thick Pt top electrodes with diameters of 100 μm were then deposited using an e-beam evaporator through a metal shadow mask. A commercial semiconductor parameter analyzer (HP4145B) and a micro-probe setup were used for all the voltage ramping DC I-V sweeps. During the electrical measurements, the top electrode was biased, whereas the bottom electrode was grounded.

3.1.3. Results and Discussion

The electrical bias sequence used to initiate BRS in a Pt/TiO₂/Pt sample and the accompanying I-V curves are presented in Figure 3.1. The sample was first electroformed by applying positive bias with a current compliance (I_{CC}) of 20 mA (arrow#1 in Figure 3.1) to prevent hard breakdown of the TiO₂ thin film. Then, the sample was URS reset (arrow#2 in Figure 3.1), by applying the same positive bias resulting in a HRS. In this case, the reset current (the maximum current immediately prior to the abrupt current drop at ~0.9V) was as high as ~32mA. At this stage, local regions of the sample that used to contain the Magnéli CF in the URS LRS get to have an effective configuration of Pt/TiO₂/TiO_{2-x}/Ti₄O₇/Pt. From the HRS of URS, it is possible to return back the sample to the LRS of URS by applying either the positive or negative voltage with the same high I_{CC} of 20mA (data not shown). In contrast, the sample can be switched into the LRS of BRS by applying a negative bias with a reduced I_{CC} of -1 ~ -3mA as shown by the arrow#3 in Figure 3.1 (in this case, I_{CC} = -2 mA). The current jumps abruptly at ~ -1.6 V, which corresponds to the BRS set operation. When the BRS set was attempted with the positive bias and an identical I_{CC} of 1-3 mA, however, there was no such current jump but just continuous increase in the current up to the I_{CC} level. Therefore, it was concluded that the BRS set after the URS reset was possible only with the opposite bias polarity to that of the electroforming or URS set. Due to the much smaller I_{CC} values used during the RRS set, current values of the LRS of BRS is much smaller than that of the LRS of URS as represented by arrows #4 and 5. This suggests that the ruptured CF during the previous URS reset process

was not completely recovered by the BRS set operation. Then, the LRS of BRS can be switched to the HRS of BRS by applying a positive bias as represented by arrows #5 and 6 in Figure 3.1a. In the I-V curve indicated by arrow #5, the current started to decrease at ~ 0.8 V showing that the BRS reset occurs. The I-V curve indicated by arrow #6 shows that the sample is in the BRS reset state. It was noted that the sample can be switched into the LRS of URS at this stage if the I_{CC} was increased again to 20 mA, and the voltage in the positive region was increased until the high I_{CC} was attained as shown by the I-V curve indicated by arrow #6 in Figure 3.1a. Therefore, this must be avoided for the purpose of BRS. The electrical stressing sequence in this experiment is, therefore, as follows; electroforming in positive bias region – URS reset in positive bias region – BRS set in negative bias region – BRS reset in positive bias region.

It should be noted that, as in Figure 3.1a, the HRS is clearly distinguished from the pristine insulating state, meaning that the resistance of the HRS is much lower than that of the pristine state, by 2-3 orders of magnitude. This is because once a Magnéli filament is generated through the electroforming, the filament is only partially ruptured during the URS reset, as previously proven by Kim et al., and Kwon et al.^{3,8} The filament ruptured region is the most resistive part in the sample, and since it will mainly govern the conduction in the URS HRS, the URS reset sample shows much lower resistance compared to the pristine state.¹⁵ The sample regions without involving the CF formation and rupture are assumed to be remained inactive during the whole BRS process. In fact, these regions could have higher defect density compared to the pristine state but their

resistance must be much higher than the regions involving the (ruptured) CF region. Therefore, such assumption must be valid. Since the following electrical bias will mostly be applied on the ruptured Magnéli filament region, the sequent BRS mechanism dealt with in this study will be mainly described, along with the oxygen vacancy configuration and density confined to the region. It should be noted that during the following BRS, it is only the oxygen vacancy configuration in this region that is affected by the electrical bias, and the remaining portion of the Magnéli filament merely plays a role as a (metallic) electrode, since there happens to be far less power dissipation during the BRS operation compared to the amounts required for either the rejuvenation or rupture of the filament.

Figure 3.1b-d show the I-V curves for three typical BRS behaviors after positive electroforming with an I_{CC} of 20 mA, followed by positive URS reset in a Pt/TiO₂/Pt sample. These BRS I-V curves were selected as the representative ones from more than a hundred I-V sweep curves. In previous work, it was found that ionic BRS samples that were electroformed and URS reset with positive bias shared a common microscopic structures of the Pt(top electrode)/TiO₂/TiO_{2-x}/Ti₄O₇(bottom electrode).¹⁵ The subsequent BRS set only occurred when the top Pt electrode was negatively biased as mentioned above. However, the BRS set process sometimes brings about somewhat disparate resistance states other than the normal BRS-LRS.¹⁵ Typical examples are shown in Figure 3.1. As can be seen in Figure 3.1b, for the normal BRS case, the BRS is operated by negative set and positive reset, and its reset current, which is defined by the current when the LRS resistance is about to increase with

negative differential resistance (NDR), almost exactly coincides with the I_{CC} assigned during the previous BRS set step in the negative bias. A somewhat modified version of the normal BRS, so-called “overshoot” BRS, is shown in Figure 3.1c. The LRS resistance is lower than that of the normal BRS, with notably higher reset current than I_{CC} . In several other cases, however, the negative voltage bias leads to a transition from one HRS (URS reset state) to another HRS despite an apparent current jump that appears just like those of the “normal” and “overshoot” BRS set in the negative bias region. This type of BRS is called an “inversion” mode, and examples are shown in Figure 3.1d. In this case, the first current jump during the voltage sweep in the negative bias region (arrow#1) does not bring about the LRS of BRS but another HRS. As indicated by arrow#3 in Figure 3.1d, the I-V curve shows another current jump in the positive bias region suggesting that the sample still remained in HRS in the positive bias region despite the current jump formerly seen in the negative bias region. Such additional HRS usually shows an asymmetric I-V curve, where the current is higher in the negative voltage region when compared with the positive voltage region. Such an asymmetric I-V curve apparently is an inverted version of the HRS of BRS I-V curve (,or the HRS of URS) before the first current jump in the negative bias region. In addition to the abovementioned I-V behavior of the BRS “inversion” mode, following observations suggest that such phenomena is mainly resulted from the inverted configuration of oxygen vacancy distribution of that of the BRS “normal” mode within the CF-ruptured region. A multi-level resistance of the LRS of BRS has been reported.¹⁵ In this RS system, depending on the I_{CC} values during the BRS set, which is also the

case here as shown in the inset I-V curves of Figure 3.1b. The I_{CC} is varied from -2 to -5 mA during the “normal” BRS set in the negative bias region, and the LRS resistance decreased accordingly which is accompanied with the increased reset current during the subsequent BRS reset in the positive bias region. The “inversion” mode of BRS set is as well followed with a similar multi-level resistance of the LRS when the I_{CC} values of the subsequent current jump (actually set current) in the positive bias region is varied from 2 to 5 mA as shown in the inset of Figure 3.1d. The LRS resistance decreases with the increasing I_{CC} and the reset current increases in the negative bias region during the following BRS reset step. This implies that the oxygen vacancy configuration at the CF-ruptured region has been inverted during the first negative voltage stressing and consequently the BRS in the other direction is followed.

As has been mentioned above, each BRS behavior seemed to originate from a certain oxygen vacancy configuration, which should be defined during the pre-BRS treatment, that is, electroforming followed by URS reset. Therefore, parameters identifying the situation of the sample ahead of the BRS were examined, such as the resistance of the electroformed filament, the current and voltage needed for URS reset, and the URS reset power. The possible correlations of these parameters with the type of subsequent BRS modes were considered. As can be seen in Figure 3.2, the results showed a fairly clear tendency for all three types of samples. For sufficient statistical significance, 45 RS cells were taken from one sample packet, and the aforementioned electroforming – URS reset – BRS set/reset sequence was performed for each

RS cell. Furthermore, the same analysis was implemented for three sample packets meaning that 135 RS cells in total were tested. Despite all the samples having been electroformed with a common I_{CC} of 20 mA, the resistance of the electroformed sample ($R_{LRS,URS}$ in the figure) increased in the order of “inversion”, “overshoot”, and “normal” BRS, as in Figure 3.2a. It must be noted that such classification was made after the BRS measurements were executed, and the $R_{LRS,URS}$ of each case was traced back. Such difference in the filament resistance results in the tendency required in the voltage and current for rupturing the filaments (URS reset), as shown in Figure 3.2b and c, which is even more clearly identified in the plot of the power consumed, obtained by multiplying the reset voltage and reset current terms, as in Figure 3.2d. The data shown in Figure 3.2a - d demonstrate that there are higher likelihoods of “inversion” and “overshoot” BRS over “normal” BRS, as a stronger filament is generated through electroforming, which is eventually accompanied with the higher consumption of URS reset power. Yet another statistical analysis on the BRS switching parameters according to the BRS mode was carried out. The values of voltage and current immediately prior to the BRS set (current jump) for each mode were estimated, and their distributions are shown in Figure 3.2e. Their products, which are the power dissipated during the BRS set process, are plotted in the inset figure. In fact, the first BRS set (current jump) for the inversion case is not an actual set but transition to another BRS reset state, but called here as BRS set for the sake of convenience. The average power dissipation during BRS set clearly increased in the order of normal, overshoot, inversion mode. Assuming that the dissipated power is equivalent to the Joule

heat generated during the set process, and since the time required for resistive switching barely varies between the samples within 100 ns for almost every case (data not shown), the power estimated in Figure 3.2e gives a direct estimation of how much Joule heat has been involved in the BRS set process.

From the data given in Figure 3.2, it can be concluded that the origin of the disparate BRS behaviors can be traced back to the electroforming step. As the CF is more strongly formed for a certain statistical reason, more power is consumed during the URS reset step, which is then accompanied by higher Joule heating during the subsequent BRS set step. This, in turn, gives an ‘overshoot’ or an ‘inversion’ type of set rather than a ‘normal’ set. Such a dependency of the BRS set power upon the URS reset power and the variation in the following BRS behavior can be comprehended in light of the electric-field-induced ionic BRS mechanism associated with the oxygen vacancy configuration in the filament ruptured region, as discussed in detail below.

It has been known through previous studies that during a URS reset process, the part of a conically shaped Magnéli filament that experiences disruption is the weakest part with the highest resistance.³ Then, once a certain part in a filament is ruptured, the rest of it stays almost intact, just as a metal electrode, since the system virtually lacks the power to further rupture the rest of the filament because the current flow is rapidly abated from that moment. Depending on the power consumed over a very short time interval during the reset process, the oxygen vacancy configuration at the ruptured filament region where the subsequent BRS set process takes place would vary.

BRS is considered to mostly be caused by electric-field-induced oxygen

vacancy migration, which is assisted by the Joule heating effect, while the URS is more likely to be controlled in a thermo-chemical way. Therefore, the electric field and Joule heating by the current flow are regarded to be the two critical parameters that control the emergence of the three BRS modes.

For samples in which the electroformed filament undergoes a complete URS reset due to the high reset power dissipated, a larger portion of the Magnéli filament is mostly re-oxidized back to insulating TiO_2 , which brings about high resistance in the ruptured filament region. Considering that it will be the rupture region where the electric field will mostly be applied during the subsequent BRS operation, a sample with high URS reset power will likely have a low value of effective electric field across the ruptured filament region. This is because a sample in which the filament has been severely oxidized would have a longer region of the recovered TiO_2 , as depicted in the right-hand panel of Figure 3.3a, making the sample present under a relatively small effective electric field, since the electric field is inversely proportional to the length of the ruptured filament region. Accordingly, a higher voltage for the subsequent BRS set would be demanded, considering that a certain threshold voltage value exists for migrating oxygen vacancies (Figure 3.3b).

However, it is remarkable that not only the BRS set voltage but the current is also highly dependent upon the BRS mode shown in Figure 3.2e. This provides an important clue for understanding the distinctive variation in the BRS set according to its type. The samples with relatively longer ruptured filament region would have high leakage current value in addition to the high threshold voltage during the BRS set due to the following reasons. Since the URS HRS

or BRS HRS samples mainly have band structure with a (high) Schottky barrier at the top electrode interface (Pt/TiO₂), the leakage current during the BRS set under the negative bias must be mostly dependent on the Schottky barrier height and electric field (E_i). An applied field would invoke lowering of the barrier height by the image force effect at the Pt/TiO₂ interface. When the insulating region has sufficiently high space charge density, E_i is not simply given as V_a/d_i , where V_a and d_i are the applied voltage and thickness of the filament ruptured region, respectively, but the field enhancement by the space charge must be considered. Shin et al. reported a quantitative estimation of the electric field enhancement at the cathode interface depending on the space charge density and film thickness in the Pt/(Ba,Sr)TiO₃/Pt system.¹⁶ Although the system configuration is different from that of the present study, the same analysis can be adopted, because the field enhancement at the cathodic interface can be straightforwardly calculated by Poisson's equation, which only relies upon the space charge density and dielectric constant.¹⁶ When the space charge density is high enough ($> 10^{19}\text{cm}^{-3}$), thicker film results in higher E_i due to the increased total amount of charge.

The ionic BRS presented in this paper originates from the migration of oxygen vacancies which are present within the CF-ruptured region. The presence of oxygen vacancies are due to incomplete re-oxidation of Magnéli filament during the URS reset step, and they work as electron traps resulting in a high space charge density under the electric field application. When the density of oxygen vacancy is very high ($> \sim 10^{20}\text{cm}^{-3}$), the Schottky barrier height at the Pt/(reoxidized) TiO₂ interface decreases to a low enough value to make the

junction quasi-Ohmic. Under this circumstance, the electron transport was controlled by the space-charge-limited conduction mechanism when the sample was in URS reset state, and the electronic-BRS mechanism was observed.¹²⁻¹⁴ The interfacial Schottky barrier height could be increased to a certain value that would make the electron transfer to be controlled by the Schottky emission mechanism when the density of oxygen vacancy decreases to a value $< \sim 10^{20} \text{ cm}^{-3}$ by a slightly enhanced oxidation of the CF during the URS reset.¹⁵ This must coincide with the ionic-BRS mechanism dealt with in this paper. However, it is still reasonable to assume that the URS-reset region has a quite high density of oxygen vacancies, perhaps as high as $\sim 10^{19} \text{ cm}^{-3}$, as the occurrence of BRS in this material relies upon the presence of high density of oxygen vacancies and their drift according to the electric field. An almost the same electric field would be present at the cathode interface of the ruptured filament region irrespective of its length, which is a result of the increased applied voltage over the increased rupture region length, when the space charge density is low ($\ll 10^{19} \text{ cm}^{-3}$). However, the actual electric field at the cathode interface must be higher due to the higher amount of space charge for the case with longer ruptured filament, when the space charge density is high ($\sim 10^{19} \text{ cm}^{-3}$). Such a higher electric field at the cathode interface can induce a higher electronic current, which will increase the local temperature by the Joule heating effect. Therefore, the vacancy migration across the ruptured filament region would be enhanced by the heating effect, even if the average field over the bulk part of the filament rupture region is invariant, and more obvious change in the BRS state occurs. It has to be noted that the average field over the entire CF-ruptured

region is determined solely by V_a and d_i . Therefore, the BRS set with an even identical average field can result in the more effective motion of oxygen vacancies when the filament rupture region is longer for the high enough oxygen vacancy concentration to induce the field-enhancement effect at the cathode interface.¹⁶ As a consequence, the power dissipation during the BRS set increases in the order of normal, overshoot, and inversion modes. In the following, the possible correlation between the I-V curve shape and degree of vacancy migration is discussed.

In a normal mode, LRS after the BRS set shows an almost symmetrical I-V curve with respect to the voltage bias, which is ascribed to the formation of conducting paths consisting of oxygen vacancies.¹⁵ In this case, the excessive vacancy migration assisted by Joule heating was minimized, so the BRS reset current value is comparable to the I_{CC} value involved in the set process. Again, the role of Joule heating can be disregarded in this case, and even if there is any Joule heating effect, they have almost identical influence on both the set and reset processes, so that the BRS I-V curves are most symmetrical. This may come from the shortest filament rupture region, and correspond to the favorable BRS condition, which is represented by the schematic figures shown in the left-hand panels of Figure 3.3a and b.

However, as the set current increases due to the longer filament rupture region, as mentioned above, the mostly field-driven migration of oxygen vacancies would be interrupted during the BRS set, because the excess Joule heat further accelerates the migration of oxygen vacancies. More Joule heat generated allows the vacancies to migrate further, even under a given magnitude of

electric field, making the recovered conduction channel much stronger. Therefore, under this circumstance, a lower LRS resistance as well as higher reset current would result, corresponding to the overshoot case. This is schematically shown in the middle panels of Figure 3.3a and b.

If the filament ruptured region was too long and excessive Joule heating was generated during the BRS set, too many oxygen vacancies drift to the TE interface, as schematically shown in the right-hand panels of Figure 3.3a and b, and the actual configuration of the switching region changes from the Pt/TiO₂/TiO_{2-x}/Ti₄O₇ into Pt/TiO_{2-x}/TiO₂/Ti₄O₇. For the latter case, the Pt/TiO_{2-x} interface may form a (quasi-) Ohmic contact, while the TiO₂/Ti₄O₇ interface forms a Schottky-type contact, even though its barrier height could be lower than that of Pt/TiO₂. The Schottky barrier heights for Pt/TiO₂ and TiO₂/Ti₄O₇ have been calculated to be ~0.6eV and ~0.1eV in a previous report using the modified Richardson equation, invoking the image force effect.¹⁵ Therefore, the I-V curve shape must be inverted in this case, which coincides well with the “inversion” mode of BRS. In fact, such an alternating configuration of the switching region shares common aspects with switching diodes and the electronically re-configurable memristive nanodevices.^{17,18} The present work provides an important clue to the reason for the presence of such switching systems, which is excessive migration of defects from one interface to the opposite one, mostly probably due to the excessive Joule heating in addition to the electric field effect.

Exploiting the fact that each distinct type of BRS set process of the samples is determined by their own URS reset status, a multi-mode BRS can be achieved

in a single sample by electrically adjusting its HRS status. Figure 3.4 demonstrates the transfer between the “normal”, “overshoot”, and “inversion” modes from one sample, even with a given I_{CC} of 2 mA during the BRS set in the negative voltage region. Another important parameter for this experiment was $V_{\text{reset,URS}}$, which is the reset voltage during the URS reset process. First, a sample showing “normal” mode immediately after the URS reset was selected. The BRS I-V curves are shown in Figure 3.4a, where $I_{\text{reset}} \sim I_{CC}$, and the switching sequence was indicated by 1set and 2reset in the figure. When the maximum applied voltage after the 2reset did not pass over $V_{\text{reset,URS}}$, the same BRS cycles can be induced (data not shown). However, once the voltage is further swept over the value of $V_{\text{reset,URS}}$ during the BRS reset in the positive voltage region, as indicated by the number “3” in 4a, the resistance of the sample keeps increasing, and the subsequent BRS set in negative voltage occurs at a lower (higher absolute) negative voltage, as shown by the 4set curve in Figure 3.4b. During the subsequent reset in the positive voltage region, a distinct “overshoot” is observed, as indicated by the 5reset curve.

This can be understood from the discussions given above. During the “3” voltage stressing in Figure 3.4a, the length of the ruptured CF region may increase, and the excessive Joule heating could be present during the subsequent 4set step. When the maximum reset voltage was limited to ca. 1.5 V, which is designated as $V_{\text{reset,overshoot}}$ in Figure 3.4b, the subsequent BRS showed overshoot I-V curves repeatedly (data not shown). However, if the voltage was further swept over $V_{\text{reset,overshoot}}$, as shown by the number “6” in Figure 3.4b, the subsequent set occurs at an even lower (higher absolute)

negative voltage, as shown by the 7set curve in Figure 3.4c, and the following I-V curve in the positive voltage region shows another set (8set). It is also notable that the resistance of the set state after the 7set is much higher than in the other cases. This suggests that the sample has transferred to the “inversion” state during the positive reset stressing represented by the “6” step in Figure 3.4b.

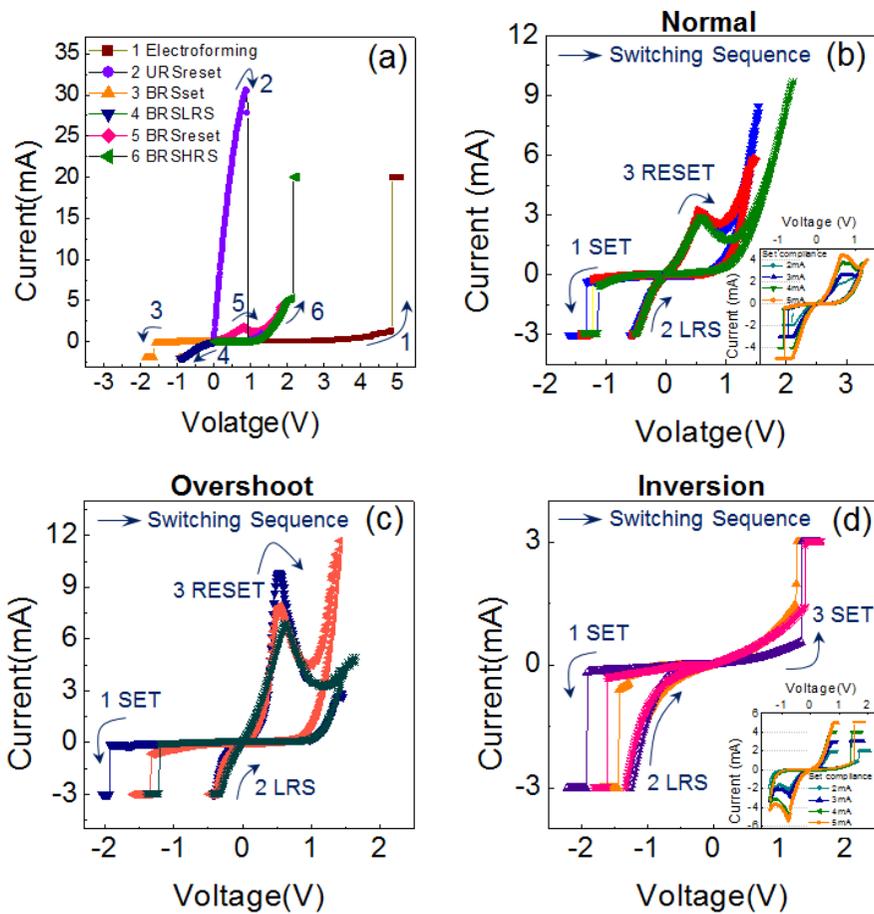


Figure 3.1 (a) A voltage stressing sequence to initiate the ionic BRS in a Pt/TiO₂/Pt sample. (b)-(d) Modes of bipolar resistive switching beginning from the URS reset state in the Pt/TiO₂/Pt sample. I-V curves of (b) *normal* (c) *overshoot* (d) *inversion* mode of bipolar resistive switching.

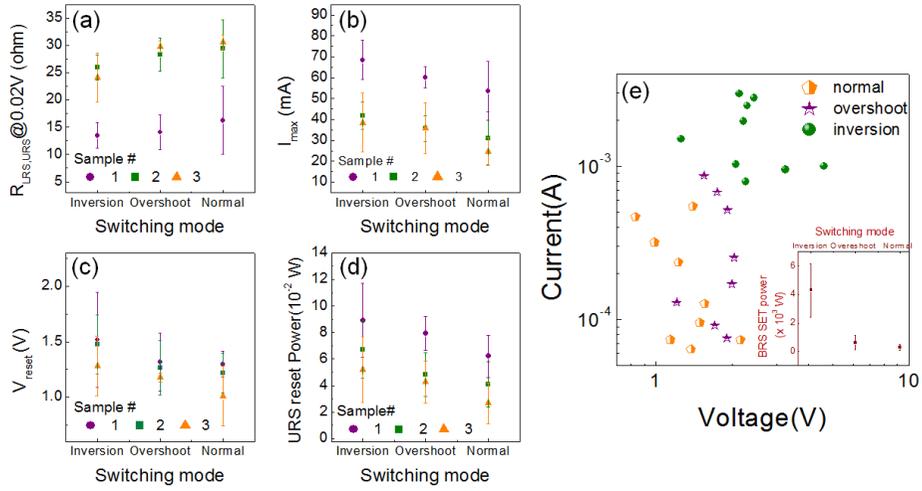


Figure 3.2 (a)-(d) BRS set type dependency upon URS reset parameters; (a) URS R_{LRS} (b) URS reset current (c) URS reset voltage (d) URS reset power. (e) Voltage vs. Current dispersion at the verge of set current jump for each resistive switching mode. Inset figure in (e) shows the comparison in the average power driven during set process of resistive switching modes.

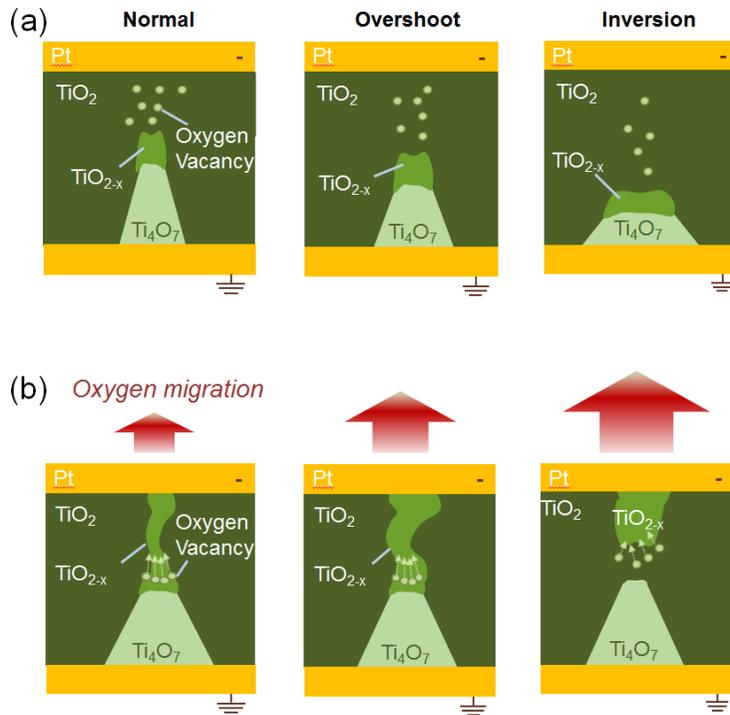


Figure 3.3 (a) Schematics of URS reset state which corresponds to BRS HRS for each BRS mode, (b) Schematics for each set type according to the amount of joule heat and the resultant oxygen migration during the set process.

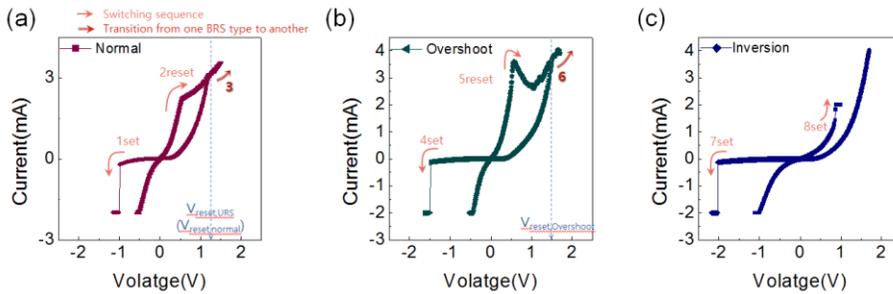


Figure 3.4 Multi-mode BRS set in a single sample. (a), (b) and (c) show the I-V curves according to the voltage stressing sequence from first set (1set) to eighth set (8set) demonstrating the transition from the normal mode to inversion mode.

3.1.4. Summary

Different ionic bipolar resistive switching modes represented as “normal”, “overshoot”, and “inversion” modes are found in a Pt/TiO₂/Pt RS sample, which had been subjected to electroforming and URS reset. Authors suggest a model ascribing the disparate BRS set behaviors to the different amount of Joule heat association in the set process, which is mainly caused by the different length of filament ruptured region from the URS reset behavior. In fact, a direct observation on the microscopic procedures involving oxygen vacancies is barely accessible. The authors cope with the difficulty by thoroughly examining the macroscopic parameters concerned both in the URS reset and each BRS I-V behaviors. And the asserted model is further strengthened by the statistical analysis upon the 135 cells in total. By tracing back the URS states of each mode in BRS, it was found that the emergence of such disparate BRS modes is closely related to the degree of re-oxidation of the Magnéli filament, which may be represented by the length of the filament ruptured region in the Pt/TiO₂/TiO_{2-x}/Ti₄O₇ structure. In the “normal” BRS mode, which in this model is usually associated with the shortest filament ruptured region during the previous URS reset, the I_{CC} and I_{reset} are comparable, meaning that the switching is mostly driven by the average electric field over the filament ruptured region. In this model, as the length of the ruptured filament region increases, the electric field enhancement induced by high space charge density at the cathode interface (Pt/TiO₂) enhances the carrier injection, which is accompanied by increased Joule heating. This additional effect accelerates the oxygen vacancy migration toward the Pt/TiO₂, even under the nominally identical average electric field

across the ruptured filament region, and a much higher I_{reset} was required ($I_{\text{CC}} \ll I_{\text{reset}}$). In the extreme case of a very long ruptured filament region, the Joule-heating-assisted vacancy migration becomes too severe, making the structure of the switching region reversed from Pt/TiO₂/TiO_{2-x}/Ti₄O₇ to Pt/TiO_{2-x}/TiO₂/Ti₄O₇, so that the I-V curve is also inverted with respect to the bias polarity. In fact, the very long filament ruptured region for the inversion case can be alternatively interpreted as having similar length to the other cases but of higher vacancy density, which can induce similar enhancement in the carrier injection and accompanying Joule heating. When the vacancy density becomes even higher, the sample would show the electronic-BRS invoked by Kim et al.¹²⁻¹⁴ In contrast, the RS mode may return back to the URS mode if the vacancy density within the CF-ruptured region is very low. Therefore, the emergence of URS, disparate types of BRS, including the normal, overshoot, inversion-type ionic RS, and electronic RS could be ascribed to the different oxygen vacancy density in the CF-ruptured region immediately after the URS reset. According to such understanding, an arbitrary transition between the three modes was possible, even in a given sample by varying the maximum applied reset voltage. This understanding could contribute to the development of resistive switching random access memory by elucidating the origin of the variation of switching characteristics.

3.1.5. Bibliography

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3.2. Time-transient analysis of complimentary resistive switching in single layered transition metal oxides

3.2.1. Introduction

It has been verified in the previous section 3.1 that the TiO_2 is one of the most promising resistive switching materials, in that it shows a multiple modes of resistive switching covering from the filamentary URS to the ionic BRS of various types. When a $\text{Pt/TiO}_2/\text{Pt}$ resistive switching (RS) sample is in the URS reset state, the electrical states of the Magnéli CF ruptured region could undergo various bipolar resistive switching (BRS) phenomena, wherein set switching and reset switching occur in the opposite bias polarity, depending on the history of the bias voltage application (polarity) and the height of the bias voltage. The BRS behavior varied from the electronic switching type,^{1,2} where the bias-polarity-dependent electron trapping and detrapping due to the asymmetric potential barrier could explain such behavior well, to the ionic switching type, where the shift in the oxygen vacancies between the Pt/TiO_2 interface and the $\text{TiO}_2/\text{Magnéli}$ phase is responsible for the switching-diode-like RS behaviour.^{3,4} All these interesting RS behaviours could be ascribed to the migration of a limited amount of oxygen vacancies within the local region of the Magnéli-CF ruptured region.

Complementary resistive switching (CRS) is an intriguing RS element that contains the switching and selection devices in one structure, and, thus, is desirable for the cross-bar array (CBA).⁵⁻⁷ In the original suggestion of CRS by Linn et al., two anti-serial electrochemical metallization cells comprised one memory element, wherein either of the two anti-serial cells is always in the

HRS, thereby suppressing the sneak current in the CBA, while the CRS cell can be written and read by the application to it of an appropriate voltage pulse. Recently, Balatti et al. reported that a similar CRS operation can be achieved even from a single RS layer of HfO₂ (Pt/HfO₂/Pt structure) by noting that the directionality of the conical conducting path in the HfO₂ can be adjusted upward or downward using the appropriately controlled voltage pulses.⁷ In this case, one of the key prerequisites was to limit the available density of the oxygen vacancies within the CF region; otherwise, the always-off state of the HfO₂ CRS cannot be attained. This triggered an idea that the similar CRS-type operation might be possible in the URS-reset TiO₂ RS memory cell. Furthermore, even more careful control of the voltage application may provide direct evidence of the transition from one resistance state to another via the intermediate state, which may pave the way to a multi-level CRS or even to an analogue type operation. Therefore, this study provides further insights on the URS-reset TiO₂ RS system, based on the time-transient behavior of each resistive switching mode and the evaluation of the properties depending on the atomically controlled shape of the conducting filaments.

3.2.2. Experimental

In addition to an identical Pt/TiO₂/Pt sample used in the experiment presented in the previous section 3.1, Pt/TiO₂/TiO_{2-x}/Pt and Pt/WO₃/Pt samples were also fabricated as the comparison samples. Pt/TiO₂/TiO_{2-x}/Pt was fabricated by depositing a 15nm-thick TiO₂ via the identical PEALD on a 100nm-thick Ti film grown via DC magnetron sputtering on Pt/SiO₂/Si. During the ALD of the TiO₂, the Ti underlayer was oxidized to TiO_{2-x}, which works as the unlimited source or sink of the oxygen vacancies during the ionic BRS. A WO₃ film was deposited via reactive RF-magnetron sputtering using a W-target under a 30% O₂/70% Ar ambient with a working pressure of 15 mtorr at room temperature (50W RF power was applied to the 3-inch-diameter target), and was subsequently annealed in an O₂ ambient at 400°C for 30 min. to obtain the desired RS phenomenon. The substrate placed under the WO₃ film was also Pt/SiO₂/Si. Circular Pt top electrodes (TE) with a diameter of 300 μm were commonly fabricated using an electron beam evaporation method through a metal shadow mask. No post-annealing was performed after the TE fabrication. The electrical test was performed in either the pulse-type voltage application [with the HP 81110A pulse generator (PG) as the voltage-programmed current source and the Tektronix 684C oscilloscope (OSC) as the current monitor] or the voltage sweep mode using a semiconductor parameter analyser (HP 4145B). The electrical test sequences for the RS performance evaluation are described in the following Results section. All the bias voltage during the voltage ramping in DC sweep mode was applied to the TE while the BE was grounded.

3.2.3. Results and Discussion

As described in the previous section 3.1, the ionic BRS begins from the URS-reset status of the Pt/TiO₂/Pt memory. First, the sample was electroformed using a compliance current (I_{comp}) of 20 mA, and then URS-reset in the voltage sweep mode. Subsequent application of an appropriate electric field can drive the oxygen ions in the Magnéli CF-ruptured region of the sample that induced the occurrence of the ionic BRS. To accomplish the ionic BRS and to avoid rejuvenation of the Magnéli phase CF during the BRS set process, the I_{CC} should be settled at much smaller values than that of the URS (typically < 10 mA in this study). The detailed physical interpretation of the ionic BRS has been reported in the previous section 3.1, based on the drift of the oxygen vacancies within the local CF-ruptured region, where the effective microscopic structure of Pt/TiO₂/TiO_{2-x}/Ti₄O₇/Pt is achieved.^{9,10} In this configuration, the remaining Magnéli CF near the cathode interface hardly contributes to the oxygen vacancy concentration but stays intact as an electrode due to the stability of its vacancy-ordered structure. The TiO₂ regions without the Magnéli CFs are assumed not to contribute to the diverse RS behavior.

First, the CRS-type operation of the Pt/TiO₂/Pt sample was confirmed using the voltage sweep operation. After the URS reset with the positive voltage being applied to the TE, the sample showed a low current during the current-voltage (I-V) sweep in the negative bias direction, which corresponds to “+HRS”, of which the memory cell structure could be schematically represented by the inset in Figure 3.5a. When the voltage reaches ~ -1 V, the current suddenly jumps, and the sample goes to the LRS. Since the study mainly deals with the field driven vacancy migration based system, the term “LRS” used in this study will

always stand for the LRS of BRS otherwise specified. At this stage, the charged oxygen vacancies (V_O), which were accumulated at the TiO_{2-x}/Ti_4O_7 immediately after the URS reset, are attracted to the top interface (Pt/ TiO_2) and form a relatively well-conducting current path. It must be noted that this conducting path is much weaker than the Magnéli CF, as can be understood from the much smaller maximum current (~ -6 mA). This weakly connected conduction path is termed a ‘conducting channel (CC)’ to differentiate it from the Magnéli CF in this study. As the voltage further decreases to -2 V, the current level decreases and shows a negative differential resistance effect (NDR) due to the further migration of V_O toward the Pt/ TiO_2 interface (right figure in the inset in Figure 3.5a) that switches the memory cell back to a HRS yet with the opposite I-V behavior to the +HRS, which is termed “-HRS”. When the bias voltage was further decreased to ~ -2.5 V, the sample undergoes URS set (data not shown) by a rejuvenation of the Magnéli CF so this was not attempted. When the bias voltage was increased in the positive direction, the sample switched back to the LRS at ~ 0.6 V through the formation of the CC again induced by the migration of V_O to the middle portion of the Magnéli CF-ruptured region. A further increase in the voltage induces further movement of the V_O toward the TiO_{2-x}/Ti_4O_7 interface, which is accompanied by another NDR in the positive bias region. Therefore, the sample stayed in the HRS when the bias voltage was small (usually lower than half of read pulse voltage), and the ON- and OFF-switching could be induced in both bias polarities, which corresponds to the CRS-type operation. When a pulse bias voltage, of which the absolute value is in between the current jump voltage and the maximum

voltage in either bias polarities, is applied, the sample would show transient current peak or not depending on the configuration of V_o accumulation. Therefore, the CRS type operation could be achieved from this type of memory cell. This type of operation is possible because a given amount of V_o 's drift along with the bias voltages. If V_o 's are further introduced or removed, which is very likely in the URS mode, such type of operation is impossible. This further supports the idea that the remaining Magnéli CF stays intact during the BRS, while only working as the actual BE. Such a transition from +HRS to –HRS via LRS (or vice versa) is more accurately examined using the following pulse-switching-type setup.

Next, the responses of the Pt/TiO₂/Pt sample in the URS-reset state to the different voltage pulses were examined by monitoring the real-time current flow through the sample using the setup shown in the inset of Figure 3.5b. For these measurements, another Pt/TiO₂/Pt cell different from the one used in Figure 3.5a with the identical sample fabrication history was chosen, and was again electroformed and URS reset. The operation voltages in BRS mode of this cell were slightly different from those of the one presented in Figure 3.5a. Even for memory devices sharing the same fabrication history with a fair uniformity being guaranteed (atomic layer deposition method was used to grow the TiO₂ film in this work), the series operation of electroforming and the subsequent URS reset can lead to different oxygen (vacancy) distribution due to the statistical nature of filament formation and rupture processes. Therefore, a direct comparison between the switching voltages in Figure 3.5a and b can hardly have any significance. In addition, the pulse voltages in Fig. 1b are the

programmed voltage to the PG which differ from the voltage actually applied to the sample. Then, the resistance state of the memory after the switching was evaluated in the voltage sweep mode, as shown in Figure 3.5c. The resistance status of the memory is returned to the +HRS during the latter measurement in the voltage sweep mode. Therefore, repetitive pulsing and sweeping were performed in one memory cell.

In Figure 3.5b, the voltage across the oscilloscope (V_{OSC}) immediately after the application of the pulse is presented with respect to the height of each of the targeted pulses (V_p) that were varied from -0.5 V to -1.9 V. The inset in Figure 3.5b highlights how the PG and the OSC at the monitoring node are connected. The PG, which is a voltage-programmed current source, flows a specified current so as to make the voltage across the equivalent resistance of 25Ω , which is supposed to be composed of the internal resistance of the PG ($R_{PG} = 50 \Omega$) and that of the OSC ($R_{OSC} = 50 \Omega$) which are connected parallel to each other, finally meet the intended value. From the estimation of the peak current values when the parasitic capacitance (C_{memory}) is being charged, at which the circuit resistance is assumed to be composed of R_{OSC} and the possible serial term (R_i) to the resistance of the memory (R_{memory}) it was found that an R_i of $\sim 25 \Omega$ is always present, irrespective of V_p . The R_i could be constituted by the contact resistance, the BE and TE sheet resistance, and the series resistance from the circuit wire. Therefore, the actual voltage applied to the memory cell could be even higher than the programmed voltage (See Figure 3.5d).

The set process occurs always alongside the C_{memory} charging and discharging effect of the memory. The charging of C_{memory} is featured as the peak V_{OSC}

immediately after the pulse application, and the set switching is represented by the increase in V_{OSC} after the decay of the charging peak. There could be charge contribution from the parasitic capacitance of the measurement setup, but this was proven to be less than 10 % to that of the memory cell.¹⁸ When V_p was as small as -0.5 V (the black square symbols in Figure 3.5b) there was no increase in V_{OSC} after the C_{memory} charging was completed at time ~ 120 ns, which suggests that the BRS set switching did not occur. When V_p was terminated at time = 300 ns, there was a peak in the V_{OSC} with the sign opposite to that of the charging peak, which corresponds to the discharging of C_{memory} . This means that R_{memory} remained high during the V_p of the -0.5V application, which is confirmed by the very low current during the subsequent I-V sweep, as shown by Figure 3.5c (the black square symbols). The wiggles after the primary charging and discharging peaks are due to the circuit noise. When V_p was decreased to -0.9 V, V_{OSC} began to show an increase at time ~ 120 ns (the red circle symbols in Figure 3.5b), which suggests that the sample started to set in the BRS mode, as confirmed by the subsequent I-V sweep in Figure 3.5c (the red circle symbols). As V_p further decreased, the time to show the BRS set further decreased (~ 100 ns at -1.3 V) and the saturation V_{OSC} level increased, which means R_{memory} decreased. This trend was again confirmed in Figure 3.5c, where the I-V curves showed an increasing current with the decreasing V_p down to -1.3 V (the bottom triangle symbols). When V_p was -1.5 or -1.7 V, the time for the increase in V_{OSC} due to the BRS set could not be accurately estimated because it was merged with the tail region of the decaying C_{memory} charging peak. This means the BRS set time for these two voltages is certainly shorter than \sim

100 ns. The higher saturation level of V_{OSC} after the charging peak seems to suggest that the R_{memory} was further decreased due to the even lower V_p level. However, this was not the case, as shown by the subsequent I-V curves in Figure 3.5c (the left and right triangle symbols). The I-V curves show that the R_{memory} actually increased with the further decrease in V_p to -1.5 and -1.7 V in the voltage region $< \sim 0.6$ V and $< \sim 0.7$ V, respectively, at which a current jump occurs and the subsequent NDR effect is observed at higher voltages. Therefore, the higher V_{OSC} (so the higher current) in Figure 3.5b for a V_p of -1.5 V and -1.7 V is due to the higher absolute voltage and non-linearity of R_{memory} with respect to the voltage, not the further-decreased R_{memory} . Down to a V_p of -1.7 V, an almost identical discharging current peak was observed when V_p was terminated, which suggests that a certain amount of charge remained in C_{memory} even though the BRS set already occurred. This is due to the insufficiently low R_{memory} of the BRS set state, which implies that the Magnéli CF was not rejuvenated. However, when a V_p of -1.9 V was adopted, a clear and large increase in V_{OSC} was observed at ~ 100 ns, and almost no discharging current was observed at the termination of V_p . The subsequent I-V curve, shown in Figure 3.5c (the black diamond symbols), revealed that the sample is now in the Ohmic conduction state. This means the Magnéli CF is rejuvenated under this pulse condition. Therefore, this condition is no longer adopted. The peculiar variation of R_{memory} with respect to V_p will be discussed in detail later.

As mentioned, the BRS set time from the pulse switching data shown in Figure 3.5b is difficult to estimate accurately due to the overlap of the charging peak and the current responses through the R_{memory} reduction. Therefore, the

following method was used to accurately estimate the BRS set switching time. It was considered that there is a certain threshold voltage (V_{th}) for the BRS set to occur, as can be understood from Figure 3.5b and Figure 3.5c. However, the estimation of V_{th} from those figures is not straightforward due to the involvement of various circuit elements. Therefore, the following calculation was performed to estimate the voltage applied to the memory as a function of time [$V_{memory}(t)$], and the results are summarized in Figure 3.5d for the various V_p values shown in Figures 1b and c. From the parallel configuration of R_{PG} and the other R and C components as in the inset of Figure 3.5b, the following equation can be derived.

$$V_{memory}(t) + V_{osc}(t) + V_i(t) = V_{PG} \quad (1)$$

From the current conservation and 50Ω of R_{OSC} and R_{PG} , equation (2) can be achieved.

$$\frac{V_{osc}(t)}{50} + \frac{V_p(t)}{50} = I_{pulse} \quad (2)$$

The current that flows along the path that contains the memory is composed of a capacitive charging and DC leakage current through R_{memory} . Thus, the following equation is formulated.

$$\frac{V_{osc}(t)}{50} - \frac{V_i(t)}{25} = C \frac{\partial V_{memory}(t)}{\partial t} + \frac{V_{memory}(t)}{R} \quad (R = R_{memory} = R_{HRS}) \quad (3)$$

By solving equations (1), (2) and (3), V_{memory} and V_{OSC} before the onset of the resistive switching are calculated as follows.

$$V_{\text{memory}} = \frac{2V_p R}{125+R} - \frac{2V_p R}{125+R} \exp\left(-\frac{125+R}{125RC}t\right) \quad (4)$$

$$V_{\text{osc}} = \frac{4}{5}V_p - \frac{2V_p R}{125+R} + \frac{2V_p R}{125+R} \exp\left(-\frac{125+R}{125RC}t\right) \quad (5)$$

Equation (5) indicates that the V_{OSC} is 4/5 of V_p at $t = 0$, which is indeed the case, as can be understood from the peak V_{OSC} values in Figure 3.5b. Thus, the validity of the preceding analysis is verified.

Figure 3.5d shows an estimated variation in $V_{\text{memory}}(t)$ when R_{memory} was assumed to be constant during the entire time range for the different values of V_p . Here, R_{memory} was assumed to be identical to R_{HRS} [3,300 Ω from the I-V of +HRS (data not shown)] of the memory cell. C can also be estimated from the fitting of V_{OSC} according to equation (5) when $V_p = -0.5$ V (inset in Figure 3.5d) because no RS occurred during the pulse application of this value. The fitting results indicated that $C_{\text{memory}} \sim 500$ pF, which agrees well with the direct measurement of the capacitance of the memory cell using the low-frequency impedance bridge (HP 4284A).⁸ Therefore, by inserting the R_{memory} and C_{memory} values of the +HRS in equation (4), $V_{\text{memory}}(t)$ could be estimated at the different values of V_p , as shown in Figure 3.5d. It can be noted that V_{memory} could be much lower than the programmed V_p due to the much higher value of R_{memory} than R_{PG} and R_{OSC} . It must be further noted that the actual V_{memory} could not be so low because the memory switches to the on-state of the BRS once V_{memory} reaches V_{th} . V_{th} for such BRS set could be identified from the data shown in Figure 3.5d. When V_p was set to -0.5 V, V_{memory} approached ~ -0.9 V, which cannot induce the BRS set, as can be understood from Figure 3.5b and c. Therefore, V_{th} must be slightly lower than this value. The I-V sweep of the

memory cell in +HRS showed that V_{th} was -1.05 V (data not shown), which is consistent with the results shown in Figure 3.5d. The slight difference in the switching voltage compared with that in Figure 3.5a (-0.95 V) is due to the slight variation in the switching parameters of the different test cells. Then the time to reach this V_{th} (indicated by the dashed line in Figure 3.5d) could be estimated from the other curves of V_{memory} in Figure 3.5d, and the values are $t_{-0.9} = 52$ ns, $t_{-1.1} = 41$ ns, $t_{-1.3} = 32$ ns, $t_{-1.5} = 27$ ns and $t_{-1.7} = 23$ ns. These values are generally much smaller than the time at the onset of the V_{OSC} increase for different V_p values. Although the difference between the two time values at a given V_p could not be accurately estimated, there is generally a time difference of ~ 70 -100 ns, which may correspond to the onset time for the BRS set in this memory cell. This also suggests that the voltage charging behavior shown in Figure 3.5d is no longer valid once the resistance of the memory begins to change, when disparate voltage behavior may appear, which is mainly composed of the combination of the resistive switching and the partial discharge of C_{memory} . Therefore, it is difficult to extract the portion that takes part solely in the resistive switching from V_{OSC} , which is the main obstacle to an in-depth analysis of the real-time growth of the filament during the BRS in TiO_2 . During the BRS set, the switching occurs in the middle of the charging of C_{memory} , which obscures V_{OSC} through the simultaneous contributions of the charging and the leakage current that accompany the BRS, whereas the unipolar resistive switching appears to occur after C_{memory} is fully charged (the black diamond symbols in Figure 3.5b), which makes the quantitative analysis feasible.⁹

Nevertheless, since V_{memory} only decreases once the memory reaches V_{th} , which triggers the ion migration, the electric field is considered to become much less effective for the BRS set to proceed. Therefore, what matters in the BRS set in determining the ultimate status of the ion distribution and the accompanying R_{memory} is assumed to be the power consumption during the switching (P_{memory}). Indeed, it has been reported in the previous section that the P_{memory} , or the Joule heat generation, plays a significant role in the determination of the directionality and conductance of CC during the BRS set.⁴ Although it is difficult to exactly interpret the real-time evolution of CC during each step of the resistive switching due to the aforementioned reasons, this study mainly examines the evolution of conduction states according to the P_{memory} during the V_p application. The tendency for the P_{memory} amount to contribute to the whole switching process according to the set pulse height would likely coincide with the relative P_{memory} evaluated at the moment of completion of the resistive switching, which can be easily obtained from the V_{OSC} data as follows.

The calculation must be performed for a moment when apparently both the resistive switching and the charging are complete. Therefore, no such charging effect of C_{memory} is considered within the circuit. Under these circumstances, equations (1) and (2) are valid, but equation (3), which gives an account of C_{memory} , should be replaced with equation (6).

$$\frac{V_{\text{memory}}(t)}{R(t)} = \frac{V_{\text{osc}}(t)}{50} = \frac{V_i(t)}{25} \quad (6)$$

By solving equations (1), (2) and (6), V_{memory} and R_{memory} , and the resulting

P_{memory} at the end of the resistive switching ($t = t_f$), are derived in the explicit form of $V_{\text{osc}}(t_f)$.

$$V_{\text{memory}}(t_f) = 2V_P - \frac{5}{2} V_{\text{osc}}(t_f), \quad R(t_f) = 100 \frac{V_P}{V_{\text{osc}}} - 25 \quad (7)$$

$$\therefore P_{\text{memory}}(t_f) = \frac{(2V_P - \frac{5}{2} V_{\text{osc}}(t_f))^2}{100 \frac{V_P}{V_{\text{osc}}} - 25} \quad (8)$$

Therefore, P_{memory} according to V_p is calculated, and the results are tabulated in Table 3.1.

| V_P (V) | -0.5 | -0.9 | -1.1 | -1.3 | -1.5 | -1.7 |
|-----------------------------|------|------|------|------|------|------|
| P_{memory} (mW) | 0.3 | 6.5 | 9.4 | 12.4 | 15.3 | 22.5 |

Table 3.1 Consumed power during the pulse-type BRS with different V_p values.

It can be understood that the decrease in V_p from -0.5 V to -0.9 V is accompanied by a drastic increase in power consumption due to the onset of the BRS set between the two V_p values.

Figure 3.6 provides detailed information on the conduction properties of switching states according to P_{memory} . Figure 3.6a shows the variation in R_{memory} , as estimated from the slope of the I-V curves at $V = 0$ V after the BRS set with each V_p , as a function of P_{memory} . When the memory remained in +HRS, which was originally induced by electroforming and the URS reset, with the positive bias being applied to TE, most of the oxygen vacancies resided at the bottom interface and caused a quasi-Ohmic interface of $\text{TiO}_{2-x}/\text{Ti}_4\text{O}_7$ while having a Schottky barrier at the top Pt/ TiO_2 interface. An insulating TiO_2 region

intervenes between the two interfaces, making R_{HRS} high ($\sim 3,300\Omega$). When P_{memory} was 0.3 mW ($V_p = -0.5$ V), the BRS set was not induced, and R_{memory} remained at the high value of the initial R_{HRS} . As P_{memory} increased to 6.5 mW ($V_p = -0.9$ V), R_{memory} largely decreased to $\sim 150\Omega$, since the BRS set occurred, and further decreased to $\sim 100\Omega$ (R_{LRS}) when P_{memory} was 12.4 mW ($V_p = -1.3$ V). However, a further increase in P_{memory} up to 22.5 mW ($V_p = -1.7$ V) increased R_{memory} again to up to $\sim 300\Omega$, which is contradicts the results at the lower P_{memory} region. These results indicate that different states of CC are induced by P_{memory} . The states are schematically shown in Figure 3.6b. The status of the memory cell at +HRS and after applying a P_{memory} of 0.3 mW can be represented by the leftmost panel in Figure 3.6b. As the set threshold voltage gave rise to the rupture of the barrier by migrating the oxygen vacancies from the bottom interface to the top, it eventually resulted in quasi-Ohmic conduction for both voltage biases. However, at this stage, the rejuvenated CC may still have a trapezoidal shape with wider dimensions at the bottom interface. Then the increase in P_{memory} will lead to the further migration of the oxygen vacancies to the TE interface, which would make the CC more cylindrical in shape (middle panel of Figure 3.6b). This may correspond to the minimum R_{memory} (R_{LRS}). The vacancy migration was further enhanced when the P_{memory} kept increasing, and the shape of the CC has become that of an inverted trapezoid. Finally, most oxygen vacancies reside at the Pt TE interface at a very high P_{memory} (rightmost panel in Figure 3.6b). This corresponds to the -HRS that is accompanied by the increase in R_{memory} in Figure 3.6a, and the current jump at a certain positive bias voltage (~ 0.58 V for a V_p of -1.5 V, and ~ 0.66 V for a

V_p of -1.7 V) in Figure 3.5c. In -HRS, the top and bottom interface is of quasi-Ohmic and Schottky barrier, respectively. It must be noted that such a systematic variation in the V_O distribution and accompanying CC shape according to the V_p could be induced because a certain and limited amount of V_{OS} are available during the entire BRS cycles. This is compared with the unlimited V_O source case of Pt/TiO₂/TiO_{2-x}/Pt, which will be discussed later.

It has been generally understood in other BRS systems that the voltage, from which NDR happens (V_{NDR}) is inversely proportional to R_{LRS} because the effective voltage across the memory decreases for lower R_{LRS} value and therefore higher nominal voltage is required for the reset process to occur.²⁰⁻²² However, in Figure 3.6c, V_{NDR} as well as the current at V_{NDR} (I_{NDR}) monotonously increases despite the inconsistent variation in R_{LRS} .

Moreover, there is a critical difference in the retention performance of the BRS set state depending on the hypothesized shape of rejuvenated CC as shown in Figure 3.6d. In this case, another memory cell was taken and electroformed/URS reset just as the previous memory cell. Then, the memory cell was BRS set under the pulse switching mode using the V_p s of -0.6, -0.9 and -1.2 V, respectively, which induced the R_{memory} of ~ 700, ~ 600, and ~ 1,100 Ω , respectively, at 0 V during the subsequent I-V sweep. The different V_p and resultant R_{memory} values compared with the other case is due to the cell-to-cell variation. It can be understood that the rejuvenated CC with a V_p of -0.9 V would have a more cylindrical shape, as in the middle panel in Figure 3.6b, and a normal and inverted trapezoidal shape with the V_p of -0.6 V and -1.2 V, respectively. The excellent retention data of the cell with the V_p of -0.9 V

revealed that the rejuvenated CC shape is such a critical determinant of a state's reliability in the BRS mode. For this retention test, a bias voltage of 0.2 V was applied to TE, which can induce the sluggish drift of oxygen vacancies from TE to Magnéli CF BE direction. When the V_p was -0.6 V, so that the CC has normal trapezoidal shape, the retention test bias voltage would slowly move some of the V_{OS} near TE toward BE because that is the region where higher electric field would be applied than others. Then the weaker part of the CC near TE becomes even weaker, which induces the decrease in current as represented by the red circle symbol in Figure 3.6d. Under the same reason, however, the retention test of the cell with the inverted trapezoidal CC shape ($V_p = -1.2$ V) under the identical test condition would strengthen the weaker part near BE interface making the CC more symmetric, so that the current increases with the increasing retention test time (blue triangle symbol in Figure 3.6d).

The distinctive properties of the system shown in Figure 3.6a, Figure 3.6c and Figure 3.6d can be comprehended within the context of the evolution in the shape of conducting channel shown in Figure 3.5b. Since the electrical property of LRS would follow a bulk-limited conduction basically due to the quasi-Ohmic nature of both top and bottom interfaces, the microscopic shape of rejuvenated CC determines R_{memory} . Basically, the CC is postulated to be a resistor comprised of oxygen vacancies, whose total amount hardly changes during the resistive switching, implying that the volume of the CC resistor is considered to be constant. Therefore, its asymmetry as well as orientation contributes to the R_{memory} as is given in the formula of the inset in Figure 3.6a. They are mainly determined by the distribution of the oxygen vacancies, which

is highly dependent on the dissipated power during the BRS set. In this sense, each regime of the decreasing or increasing R_{memory} in Figure 3.6a corresponds to the decrease or increase of asymmetry in the CC, respectively. As depicted in the schematics in Figure 3.6b, with the increase of P_{memory} , the CC shape evolves in a way that its asymmetry decreases and again increases via the point where the CC is almost symmetric so that the R_{memory} becomes the minimum. As for Figure 3.6c, because it is the amount of oxygen vacancies at the TE interface that governs the V_{NDR} and I_{NDR} , they monotonously increase with the increasing P_{memory} while inconsistent change in the R_{memory} values was observed according to P_{memory} . As schematically shown in Figure 3.6b, the amount of V_{OS} near TE monotonically increases with increasing P_{memory} , so do the V_{NDR} and I_{NDR} .

Next, the reverse process of what was shown in Figure 3.5 and Figure 3.6 was attempted using the V_p values with positive polarity beginning from -HRS. To do this, another memory cell was taken, positively electroformed and subsequently URS reset in the same bias to have the +HRS. Then, just as in Figure 3.5a, it was further driven to the -HRS by applying the negative voltage up to -1.3 V. The abrupt current jump during the transition from +HRS to -HRS occurred at $\sim -0.9\text{V}$. After these bias applications, the microscopic state of the cell can be represented by the schematic of the rightmost panel in Figure 3.6b, wherein almost all the V_{OS} reside at the TE interface region. Subsequently, migration of some V_{OS} toward the BE interface through the minimum R_{memory} state, which corresponds to the almost cylindrically rejuvenated CC, is performed by applying the positive V_p of 0.6 V, 0.8 V, 1.0 V, 1.4 V and 1.6 V

for 300 ns, respectively, as shown in Figure 3.7a. Figure 3.7b and Figure 3.7c show that when V_p was 0.6 V, the BRS set did not occur because it could not induce the V_{memory} to reach the V_{th} of this specific cell. Between the V_p values of 0.8 and 1 V, R_{memory} was minimized, and then it increased again to a large value at a V_p of 1.4 V, which means the sample was returned to +HRS after this V_p application. The sample is eventually URS set with the application of a very high V_p of 1.6 V. This is exactly the reverse process of what are shown in Figure 3.5 and Figure 3.6, and suggests that the delicate and reversible control of CC, composed of V_{Os} within the Magnéli CF-ruptured region in the TiO_2 memory, is possible via the V_p application. Again, this is due to the limited amount of migrating oxygen vacancies in the CC region. The same could not be acquired from the system that contains unlimited sources of V_{O} , as shown below.

Such delicate control of the shape of the CC was attempted in a $\text{Pt/TiO}_2/\text{TiO}_{2-x}/\text{Pt}$ system whose bipolar resistive switching has mainly been ascribed to the same physical reasoning of oxygen ion migration as that of the URS reset $\text{Pt/TiO}_2/\text{Pt}$, yet with a much richer oxygen vacancy layer (TiO_{2-x}), as reported elsewhere.⁹ This sample shows a typical BRS-type I-V curve where set and reset occurs in negative and positive bias voltage regions, respectively (data not shown). After the BRS reset in the positive bias region during the I-V sweep, an attempt was made to set the sample in the pulse switching mode by applying 300ns-long pulses with different V_{p} s, from -1.2 V to -3.0 V (identical pulse switching setup, as shown in Figure 3.5 and Figure 3.6. As shown in Figure 3.8a, the sample shows increasing charging and leakage current with the decreasing V_p (the increase in the absolute V_p value), whereas the discharging

peaks are constant almost irrespective of V_p , suggesting that there is no major change in the microstructure of the sample even with the lowest V_p of -3.0V. The -1.2V V_p did not induce any significant change in the R_{memory} , whereas the V_p values less than -1.2 V induced a progressive decrease in R_{memory} , as shown in Figure 3.8b and c. However, there was only a monotonous decrease in R_{memory} in the BRS mode, but no such transition either to the -HRS or URS was seen according to the decrease in V_p . The occurrence of the BRS set under the negative bias that was applied to TE suggests that the set is induced by the migration of V_{OS} from the TiO_{2-x} layer, which is actually an unlimited source of V_{O} , to the Pt TE interface by forming CC. The decreasing V_p merely promotes further migration of V_{OS} , making the CC ever stronger, but no inversion of the CC shape as there is no limitation for the supply of V_{OS} from TiO_{2-x} . This strongly suggests that the transition of the resistance state from +HRS to -HRS via LRS during the BRS mode (or vice versa) with increasing or decreasing V_p could originate only from a system where a finite amount of defects or oxygen vacancies in this kind of transition metal oxide exists. It seems to stem from the fact that the gradual variation of the asymmetry and the orientation of the conducting channel can only be caused by the defect in the distribution change when the volume of conducting channels is constant and small enough for the distribution change driven by the electric field to significantly affect its resistance.

Such consideration of the inducement of the transition of +HRS \rightarrow LRS \rightarrow -HRS (or vice versa) by the change in the distribution of a given density of V_{OS} according to the BRS set pulse was further confirmed in the experiments with

another kind of transition metal oxide, WO_3 , which also contains the Magnéli phases in its phase diagram.²³⁻²⁵ Initially, the electroforming followed by the URS reset was performed with a Pt/ WO_3 /Pt device with a positively biased Pt TE. Thus, part of the Magnéli filament retained near the Pt BE served as the actual BE during the subsequent BRS experiments. The subsequent BRS showed a stable operation yet with a smaller on/off ratio than that of the TiO_2 . The pulse switching results with the V_p values from -0.5 V, the absolute voltage of which is too low to induce the BRS set, to -1.8 V, at which the URS set occurred, are shown in Figure 3.9a-c. Although the absolute switching parameter values were different from those of the TiO_2 memory, the trends were fully identical with those of TiO_2 in Figure 3.5b and c, and Figure 3.6a. The sample was initially +HRS and switched to -HRS at the V_p of -1.6 V through the point of the lowest R_{memory} ($V_p = -1.2$ V), and eventually, to the URS set state at $V_p = -1.6$ V. Even though the data sets in Figure 3.7-Figure 3.9 are presented with V_p as the variable, it is quite obvious that the dissipated power during the memory switching was the governing factor.

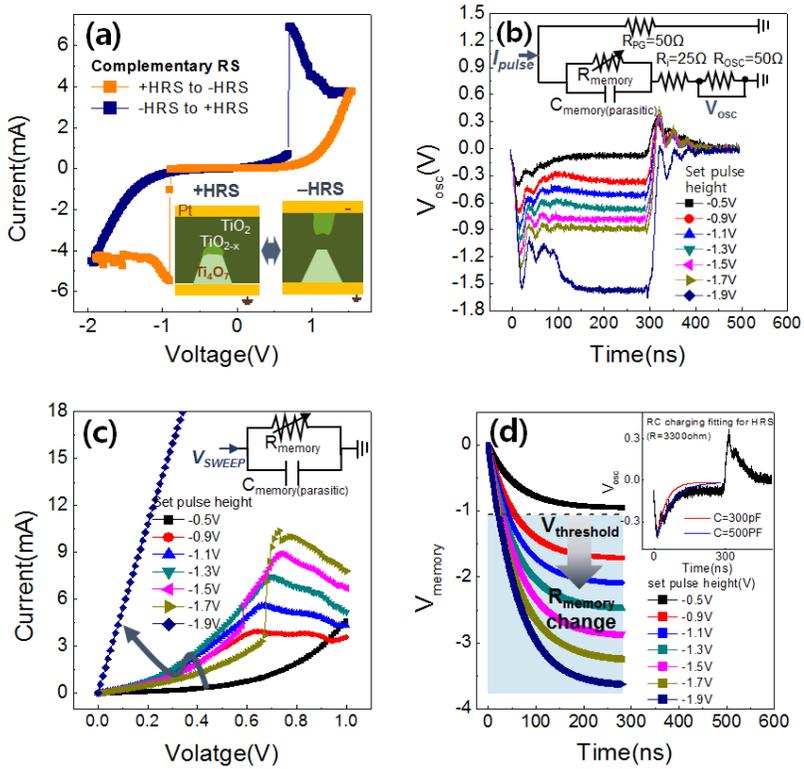


Figure 3.5 (a) I-V curve of the complementary resistive switching in URS reset Pt/TiO₂/Pt (b) V_{osc} during the resistive switching by current pulse of different heights. Inset is the corresponding circuit for the current pulsing to the +HRS of URS reset Pt/TiO₂/Pt. (c) I-V curve of memory measured in the voltage sweep mode after resistive switching by the current pulses of (b). Inset is the circuit during the voltage sweep mode. (d) Calculated V_{memory} during the parasitic capacitance charging during the current pulsing of (b). The corresponding time needed to reach the threshold voltage (the grey dashed line) for the set process, which is presented in Table 3.1.

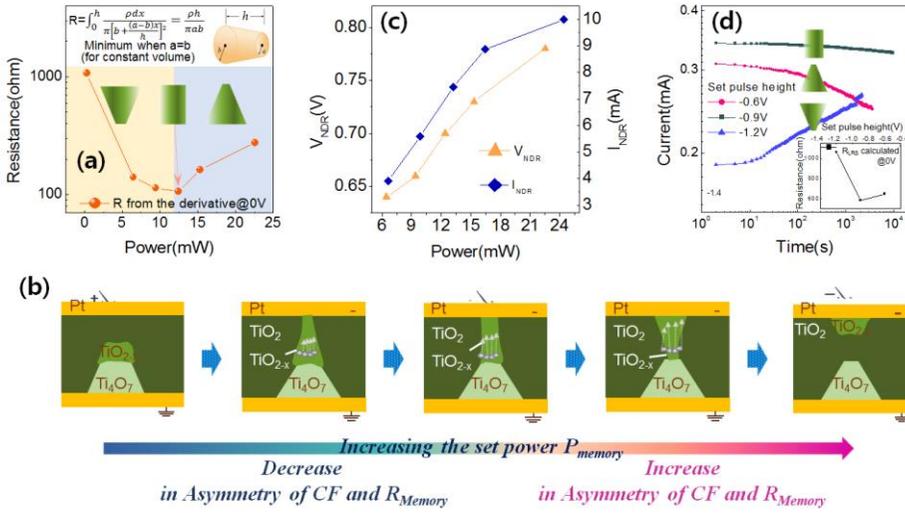


Figure 3.6 (a) Resistance of memory (R_{memory}) change (b) Schematics of the conducting channel shape (c) The maximum current and voltage (I_{NDR} and V_{NDR}) after resistive switching, according to the increase in power (P_{memory}) consumed during the preceding resistive switching. (d) Retention characteristic and R_{memory} (inset) according to the height of current pulse.

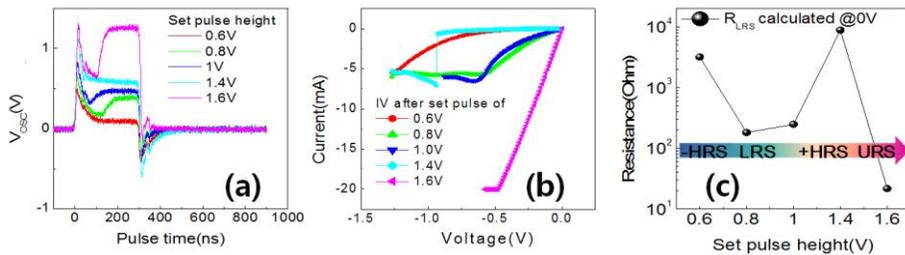


Figure 3.7 (a) V_{osc} during the resistive switching by current pulse of different heights from -HRS of URS reset Pt/ TiO_2 /Pt. (b) I-V curve of memory measured in the voltage sweep mode after resistive switching by the current pulses of (a). (c) Resistance of memory (R_{memory}) change according to the height of current pulse during the preceding resistive switching.

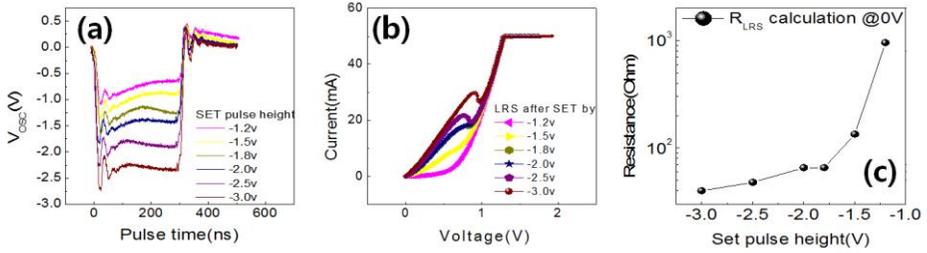


Figure 3.8 (a) V_{osc} during the resistive switching by current pulse of different heights in Pt/TiO₂/TiO_{2-x}/Pt. (b) I-V curve of memory measured in the voltage sweep mode after resistive switching by the current pulses of (a). (c) Resistance of memory (R_{memory}) change according to the height of current pulse during the preceding resistive switching.

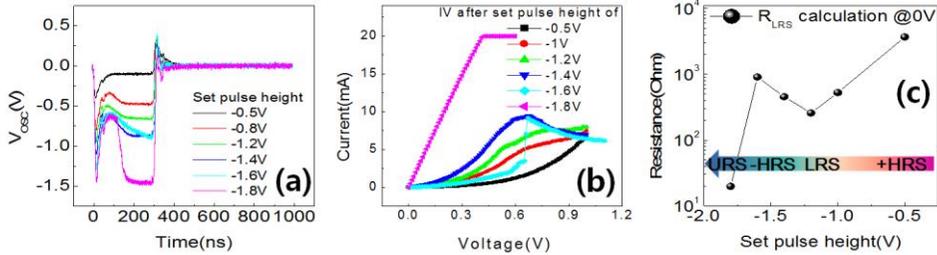


Figure 3.9 (a) V_{osc} during the resistive switching by current pulse of different heights from +HRS of URS reset Pt/WO₃/Pt. (b) I-V curve of memory measured in the voltage sweep mode after resistive switching by the current pulses of (a). (c) Resistance of memory (R_{memory}) change according to the height of current pulse during the preceding resistive switching.

3.2.4. Summary

In conclusion, the reversible transition between two different HRSs in the BRS via the LRS was accomplished by applying different pulse voltages. To carefully control the defect distribution that induced the different shapes of the conduction channel in the evident conducting filament-ruptured region, as well as the accompanying resistance change of the memory, there must be a finite amount of oxygen vacancies involving in the BRS. Transition metal oxides, particularly those involves the phase transition to the metallic phase (Magnéli), such as TiO_2 and WO_3 , can effectively meet such a condition through the partial re-oxidation of the Magnéli CF via the electroforming, followed by the URS reset operation scheme. The combined analysis of the time-transient current during the voltage pulsing and the resistance status obtained in the subsequent voltage sweep mode confirmed the validity of the switching model and gave a detailed physical reason for the desired phenomenon in the system. The power consumption during the ion migration-based resistive switching is the key determinant of the conduction states, which is highly consistent with the previous result shown in section 3.1.⁴ Unlike the original form of the CRS suggested by Linn et al., where only two different HRS are involved, such an analogue type of CRS operation presented in this study can be regarded highly promising for its potential use in the multi-bit CRS operation.

3.2.5. Bibliography

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4. Double-layers stacked 3D crossbar RRAM employing a diode selector with extremely high rectification ratio

4.1. Introduction

Resistance switching random access memory (ReRAM) is a highly appealing contender for a versatile replacement of NAND flash or storage class memory filling in the performance gap between dynamic random access memory (DRAM) and hard-disc (or NAND flash) in computers.¹ Recent announcement on the production of three-dimensional cross-point (3D X-point) memory jointly developed by Intel and Micron appears to be a great step-forward in this area, although the materials and process details are yet to be uncovered (ReRAM or phase change RAM). The eye-catching aspects of the 3D X-point memory are the adopted crossbar architecture that uses a two-terminal device instead of a transistor as the cell-selector combined with the double-layer stacked structure, which results in an extremely small cell size of $2F^2$, where F is the minimum feature size. The crosspoint, or crossbar array (CBA) is a passive array architecture, which has been used in the first random access memory of magnetic core memory about fifty years ago. Ever since the development of metal-insulator-semiconductor field effect transistor (MISFET), the cell selection function for a matrix-type memory has been taken by the MISFET, as in DRAM, thanks to its supreme performance as a switch. With the extreme scaling of the memory cell, however, down to $F < 20$ nm, MISFET may not be an optimum solution as the cell selector because of its inherently

larger cell size ($8F^2$) than the diode or threshold switch ($4F^2$) in addition to the performance degradation according to downscaling. Recent development of a ultrahigh density NAND flash memory of 256GB, based on its vertical integrated structure and 3-bit operation, is an excellent demonstration of the strategy with which can further increase the integration density without shrinking the memory cell size.²

In this regard, the evolution of ReRAM into the third dimension, i. e. layer stacking or vertical integration of memory cells, is a natural consequence from the engineering efforts for achieving ultra-high density memory. Some of the authors have reported the details for various aspects of integrating the ReRAM in the 3D structures, and it was found that the layer stacking and vertical integrations have their own pros and cons.^{3, 4} Nevertheless, layer stacking of CBA is a highly feasible and immediate approach given the circumstances that vertical integration requires complicated process techniques, such as deep hole (or trench) etching and conformal deposition of all the functional layers onto a very high aspect ratio structures, in addition to even tougher selector requirements than those for the planar CBA.³ This can be feasibly understood from the double-layers stacked planar memory architecture of the aforementioned 3D X-point memory. In passive array, the sneak current is a significant problem, which is mainly due to the parallel configuration of memory cells to given bit- and word-lines (BL and WL). If the performance of selector, which prevents the sneak current during reading and suppresses leakage current during writing, is not high enough, number of memory cells sharing one BL or WL must be limited, and larger numbers of periphery circuit

elements, such as sense amplifier, become necessary. Therefore, high performance of selector is as important as that of memory element. Although a few very recent studies have demonstrated vertically integrated 3D ReRAMs up to four layers at the maximum,^{5,6} their selector performance are still yet to be enhanced further actually to take advantage of such vertical integrated structure, which is only meaningful when provided with enough memory density per a layer. Therefore, in fact, the planar CBA provided with high selector performance should be preceded to the demonstration of the vertically integrated structure. In this sense, the stacked crossbar structure is still an appealing structure in that it has the relatively mitigated sneak currents issue compared to its vertical counterparts. Besides, it allows easier engineering of selector performance as it has a room for the shared middle electrode, which serially connects a memory element to a selector element being placed in between the two.

Nonetheless, the reason for the delayed immediate adoption of the stacked architecture in 3D ReRAM devices may lie upon not only the demanding procedures requiring lithography processes for every electrode layer but also the thermal budget problem that is even more detrimental in repetitive stacking procedures particularly involving the two terminal selectors such as diodes and threshold switches where inherently high potential gradient reside in the device. Therefore, the only viable method to solve such problem is to adopt a fabrication method that does not impose the severe thermal budget to the underlying layers. In this work, according to this idea, a reactive sputtering method was developed at room temperature to make the appropriate TiO₂ layers

for both memory and diode layers, which could provide a Schottky diode with a performance of more than 1,000 times higher rectification ratio value compared with the preceding case adopting ALD TiO₂ films.⁷⁻⁹ Because of the planar structure based stacking integration, low step coverage of sputtering process was not a serious concern. Based on this fabrication method, a double layered ReRAM in the CBA form was fabricated and an extremely high rectification ratio ($I_{\text{forward}}/I_{\text{reverse}}$ measured at $\pm 2\text{V}$) of $\sim 10^8$ was confirmed from both the upper and lower layers, although the array size was only $4 \times 4 \times 2$. The ratio is the highest among those reported to date according to the authors' best knowledge from the recent publications on RRAM device with rectifying property.^{5-7, 10-18} Moreover, the cell size of the double layers stacked CBA can shrink down to F^2 , with the help of 2-bit operation. As the minimum feature size F , achievable in the lab scale lithography technique is $2\mu\text{m}$, the device scalability according to device area was confirmed, which will help to pave the way to the realization of the ultra-high density ReRAM in CBA architecture.

4.2. Experimental

Figure 4.1 shows a schematic supporting for the overall fabrication processes for the double layer stacked 1D1R crossbar integration. Two layers of 1D1R with diode-over-memory structure are fabricated alternately stacking the electrode and oxide layers. The total of five UV photo-lithography techniques followed by photoresist lift-off was involved for patterning every electrode layer to generate the crossbar junctions, while the total of six oxide layers including the adhesion layer was inserted in between the electrode layers. A reactive ion beam etching (RIBE) with SF_6 gas ambient was conducted at the end to reveal the bottom electrodes of each 1D1R layer buried under the TiO_2 film. Initially, a 10nm- Ta_2O_5 was deposited by PEALD (plasma enhanced atomic layer deposition) method using a tbtDET precursor with O_2 oxidant at a substrate temperature of 200°C , to mitigate the poor adhesion of Pt on SiO_2 substrate obtained by a thermal oxidation from the Si substrate. TiO_2 oxide as the main functional oxides for both the memory and the diode layers was fabricated by a lab-made sputter with RF power of 150W within the 15mtorr reactive working pressure in O_2/Ar ratio of 20 percent gas ambient at room temperature using a TiO target. A constant deposition rate according to the sputtering time is confirmed from the layer density of Ti obtained by an X-ray fluorescence analysis (XRF) as shown in Figure 4.2a. All of the metal electrodes were deposited by electron gun evaporation method.

The electrical characteristics of all the devices was obtained by DC voltage sweep on the device using a semiconductor parameter analyser (HP 4155). An incremental step pulse programming method was used for the endurance test.

All the bias voltage was applied to the TE while the BE was grounded. The structural and chemical analysis provided with Auger Electron Spectroscopy (AES), Scanning Electron Microscope (SEM), Atomic Force Microscopy (AFM), High Resolution- and Scanning- Transmission Electron Microscope (HRTEM, STEM), Energy Dispersive Spectrometer (EDS) and XRD results are included.

4.3. Results and Discussion

Figure 4.3a presents a cross-sectional HRTEM image of a planar crossbar 1D1R device, of which the materials stack consists of Au(70nm)/Pt(20nm)/TiO₂(60nm)/Ti(70nm)/Pt(20nm)/Ni(20nm)/Pt(20nm)/TiO₂/Pt(20nm)/Ta₂O₅(10nm)/SiO₂(100nm)/Si. While the Pt/TiO₂/Ti/Pt node comprises a diode, the Pt/TiO₂/Pt node comprises a RS memory component. The two components are serially connected with the middle electrode of Pt/Ni/Pt, where the Ni layer was inserted as an oxygen diffusion barrier layer⁷ to prevent the oxygen diffusing into the diode layer from the memory layer during electroforming and the subsequent repetitive set operations in the RS memory layer.^{19,20} (inset schematic of Figure 4.3a) On the other hand, the Au layer is added onto the top electrode to alleviate the voltage partake issue by the electrode line resistance in CBA. A typical 1D1R operation is investigated in a 4x4μm² crossbar device of a planar 2x2 CBA shown in Figure 4.3b, whose top, middle, and bottom electrode (TE, ME, BE) is defined as in Figure 4.3c of a SEM image. In Figure 4.3d, a reliable operation accompanied by an outstanding rectifying property is maintained even in the low resistance state (LRS). With a current compliance (I_{cc}) of 300μA during the initial electroforming process, the resistance state of the pristine device is turned to LRS, followed by a reset process accompanied by an abrupt current decrease to high resistance state (HRS). The relatively higher current level of HRS compared to that of the pristine state implies that only a part of the conducting filament generated during the preceding set process is ruptured during the reset process. Typically, resistive switching in a single Pt/TiO₂/Pt memory device

shows a unipolar resistive switching (URS) with the set and reset occurring regardless of the bias polarity, however in the 1D1R device, resistive switching occurs only at the forward (positive) bias because any attempt of resistive switching in the reverse (negative) bias is not available as the highly rectifying property of the diode hampers an effective voltage drop on the memory layer at the reverse bias.

Such a typical URS in Pt/TiO₂/Pt is widely known to occur by the thermally-assisted soft-breakdown of the oxide layer generating a local conducting filament within the layer, which has been verified as the oxygen deficient Magnéli phase (Ti₃O₅ or Ti₄O₇).²¹ In Figure 4.3d, the relatively high current level of HRS compared to that of the pristine state alongside the smaller set voltage (~4-5 V) than the electroforming voltage (~6V) implies that only a part of the filament is ruptured and recovered during the subsequent reset and set processes, respectively. As a sneak current path in CBA is comprised of a series connection of two forward biased cells and one reverse biased cell,³ the remarkably suppressed reverse current in the LRS of this 1D1R device can effectively prevent the sneak currents in CBA. In this state, despite the highly conducting filament is residing at the memory layer, high Schottky potential barrier at the top Pt/TiO₂ interface of the diode governs the overall conduction. When the voltage is increased high enough to be applied even to the memory layer, the conduction is somewhat affected by the filament, evidenced by the slightly increased current near -2V after electroforming. Even at the forward bias, most of the voltage is applied to the diode layer, therefore, the memory operation is achieved only at a relatively larger voltage range above ~1V. Until

this voltage, conduction is governed by the forward bias conduction through the TiO₂/Ti bottom interface of the diode layer, giving identical I-V characteristics for both the HRS and LRS. Rectification ratio and memory window for the first three resistive switching operation cycles are evaluated with respect to voltage values, as provided in the inset of Figure 4.3d. Above the reading voltage of 1.5V, highly rectifying characteristics with the ratio of $\sim 10^8$ is shown with an obvious memory window of over 10^3 between LRS and HRS.

In order for a successful 1D1R operation, it was important to adjust the thickness of the TiO₂ for the memory layer (1R). The XRD diffraction peak results according to the thickness of the RT sputtered TiO₂ on SiO₂ substrate is shown in Figure 4.4a. As the thickness of the TiO₂ increases, the initial amorphous TiO₂ is grown into the Anatase phase and further to the Rutile phase with an expense of the Anatase phase. It may be the initial amorphous layer formation that promotes the growth of Anatase, which is normally stable in higher temperature above the deposition condition (RT), and further to Rutile, which is stable at even higher temperature. Such a thickness dependent growth of the RT sputtered TiO₂ leads to an interesting thickness dependent leakage behavior. In Figure 4.4b, strangely, a thicker TiO₂ of 40nm gives even higher leakage current followed by a smaller breakdown voltage than those of thinner 20nm-TiO₂. Aside from the fact that normally a material in its amorphous form is more insulating than its crystalline form,²² the Rutile TiO₂ has a smaller bandgap ($\sim 3.2\text{eV}$) than that of the Anatase TiO₂ ($\sim 3.4\text{eV}$).²³ Therefore, the 40nm-TiO₂/Pt containing larger portion of the Rutile phase may comprise a

smaller potential barrier at the interface, hence giving fluent leakage characteristics with small break down voltage despite its thicker thickness compared to that of the 20nm-TiO₂ with the partially crystallized Anatase phase. This can be further applied to the memory TiO₂ thickness dependent 1D1R property. While the successful 1D1R operation was performed in Figure 4.3d, where 20nm-TiO₂ was inserted as the memory layer, a 1D1R adopting a 40nm-TiO₂ for its memory layer did not show a stable memory operation, as shown in Figure 4.4d. The 1D1R with thicker 40nm-TiO₂ RS memory layer showed rather higher leakage level followed by smaller electroforming voltage (~4V). Such a smaller electroforming voltage led to an insufficient filament formation in the memory layer resulting in a more resistive LRS state compared to the case of Figure 4.3d, which eventually led to a reset failure. A too weak filament generation during the set process leads to a reset failure as it lacks the sufficient Joule heat generation to partially re-oxidize the oxygen deficient (Magnéli) filament back to the insulating TiO₂.

HRTEM analysis is carried out to further support the underlying mechanisms for the above described 1D1R I-V characteristics. Being consistent with the thickness dependent phase property of the TiO₂ described in Figure 4.4, HRTEM images of Figure 4.4a-b reveal that the TiO₂ comprising the diode and memory layer show disparate crystalline structures. In the memory layer, the 20nm-TiO₂ was partially crystallized into the Anatase phase, represented by the FFT (Fast Fourier Transform) analysis in the blue squared region of Figure 4.4a, along with some remaining amorphous regions. On the other hand, the thicker 60nm-TiO₂ of diode layer, represented by the yellow square in Figure 4.4b,

exhibits highly poly crystalline structure, most of which have been evolved into the Rutile phase according to an extensive FFT analysis. In Figure 4.4b, the bottom Ti electrode is confirmed intact as a poly crystalline Ti metal even after the TiO₂ deposition despite the high oxygen affinity of Ti. The FFT of Ti layer, represented by the green square in Figure 4.4b, provides a diffraction information of Ti (100). The small oxygen content in the Ti layer compared to those of TiO₂ in diode and memory layer is also proven by the AES analysis for a single diode (Figure 4.5c) and the EDS analysis for a 1D1R (Figure 4.5d). These results are different from those of the previously reported Schottky diode where the TiO₂ was deposited by PEALD method with O₃ oxidant and tetra-iso (TTIP) precursor at 250°C. In those works, deposition of the TiO₂ at such high temperature lead to a substantial oxidation of Ti bottom layer toward TiO_{2-x}, comprising a quasi-Ohmic and blocking contacts for TiO_{2-x}/Pt and Pt/TiO₂ junctions.^{8,9} In principle, the Forward/Reverse ratio of the Pt/TiO₂/Ti Schottky diode could be as high as 10¹² ($\sim \exp(0.7\text{eV}/kT$, where 0.7 eV is the approximate barrier height difference between the two junctions, and k and T are Boltzmann constant and temperature, respectively) at room temperature, which is more than sufficient value for ultra-high density crossbar array application. However, the experimentally achieved rectification ratio in the high temperature fabricated diode was limited to $\sim 10^6$,^{8,9} mainly ascribed to the severe leakage current through the weak spots generated in Pt/TiO₂ top interface. The weak spots were generated by the unwanted local reduction of TiO₂ at the Pt/TiO₂ junction where the reduction was initiated by the reaction of TiO₂ with Ti at the opposite interface. Owing to the RT fabrication method, on the other hand, little

leakage paths are introduced within the device, and therefore, the diode conduction at the reverse and forward bias is governed by the Schottky barriers at the top Pt/TiO₂ and bottom TiO₂/Ti interface. As a result, a much better rectifying property of the RT diodes compared to that of the PEALD fabricated diode is achieved. Nevertheless, it is still smaller rectification ratio than the value achievable in principle (10^{12}) because it is actually inevitable to completely get rid of the oxygen residing in the Ti layer. Even a slight oxidation of Ti will increase the actual work function of Ti, consequently giving a relatively increased TiO₂/Ti barrier height than in principle. Such an amount of oxygen inherently incorporated in the Ti layer may be reduced by optimally increasing the deposition rate of Ti, as demonstrated in a previous study by Kim et al.⁹

The slightly oxidized TiO_x amorphous at the uppermost region of Ti, confirmed in Figure 4.5b as well as in Figure 4.3a may be another reason for the degraded rectifying performance value than the theoretical value. On the other hand, the thin amorphous layer may rather positively affect to the downscaling of the diode. 1x32 CBA diodes with different feature size from 16μm² to 100μm², are fabricated to investigate the electrode area and wire line resistance dependent diode I-V characteristics. The stack of the fabricated diode was

Au(30nm)/Pt(20nm)/TiO₂(60nm)/Pt(20nm)/Ni(20nm)/Pt(20nm)/Ta₂O₅(10nm)/SiO₂(100nm), with a notably thinner Au than that of the 1D1R device shown above in Figure 4.3a (Au(70nm)). In order to exclude the effect of line resistance on the device characteristics, the device that is closest to the bottom

electrode contact pad (1st cell of the Figure 4.2b) was measured. Based on their raw I-V curves in Figure 4.6a, the inset of the figure shows the rectification ratio (Forward/Reverse current ratio, F/R ratio) evaluated according to the reading voltage from 0.5V to 2V. Forward and reverse current densities measured at the reading voltage of ± 2 V are organized in Figure 4.6b according to electrode area. The increasing current density with the decreasing electrode area at the forward bias implies that the conduction at forward bias is governed by a local injection through the bottom TiO₂/Ti interface. This is ascribed to the inhomogeneous conductive area over the interface caused by the TiO_x amorphous layer as was proven in Figure 4.5b. In contrast, the reverse current density showed a constant density over all electrode area range, implying for a homogeneous interfacial conduction through the Schottky barrier at Pt/TiO₂ top interface. The RT sputtering method for TiO₂ mainly led to the homogeneous interfacial conduction at Pt/TiO₂, in contrary to the local conduction even at the reverse bias of the PEALD fabricated TiO₂ case by Kim et al.⁸ In the study, the local conduction was verified to be ascribed to the partial reduction of TiO₂. As only the forward bias conduction is attributed to the local conduction, the rectifying property improves with the decreasing feature size of the device as in the inset of Figure 4.6b.

On the other hand, Figure 4.6b shows an effect of line resistance on the diode characteristics. While the reverse current density showed little difference depending on the distance of the cell from the bottom contact pad, the forward current density of the 31st cell from the bottom contact pad (see Figure 4.4b) was remarkably degraded compared to that of the 1st cell. Figure 4.4c shows

that the significant degradation in the forward current density arises as the device is placed farther from the bottom electrode pad, or, as the wire line resistance increases. This is because the diode resistance at the forward bias is smaller than that of the reverse bias, the forward current is more apt to be affected by the line resistance due to the relatively increased voltage drop on the wire, if the same absolute reading voltage value is applied for both biases.

Figure 4.5c presents typical I-V curves for the electroforming and the subsequent first LRS state of 1D1R devices with different electrode area. In addition to the crossbar 1D1R with feature size of $4\mu\text{m}^2$ through $100\mu\text{m}^2$, dot-shaped electrodes with the area of $452\mu\text{m}^2$ through $2290\mu\text{m}^2$ were used for an extensive area dependency test. Current density and rectifying property of only the crossbar devices were evaluated according to electrode area, as they showed different operation voltage range and hence were not directly comparable to the devices of dot-shaped electrodes, mainly due to the inherent line resistance effect in the crossbar devices. As in the inset of Figure 4.6d, the increasing rectifying property of the diodes is also maintained in the 1D1R devices. As the allowable memory density is highly dependent on the rectifying property of the RRAM devices in a CBA, even higher memory density can be achieved with this 1D1R device as the node size scales down. Distinguished from the single diode case, however, not only the forward current but also at the reverse current in 1D1R device features local conduction, being affected by the local conducting filament in the RS memory layer. Nevertheless, the increasing tendency of the reverse current density with the decreasing electrode area is weaker compared to that of the forward current density, as the interfacial

conduction through the diode still dominates in the reverse conduction. Therefore, the highest rectification ratio of the 1D1R was achieved as 8.4×10^8 at the smallest feature size, $2 \times 2 \mu\text{m}^2$. This is the highest value achieved in the rectifying RRAM systems that have been reported until recently.^{5-7, 10-18}

It is noteworthy that the rectification ratios of 1D1R in LRS, although the ratio happens to vary cell to cell mainly due to the inherent stochastic nature of filament formation in RS memory layer, are generally higher than those from the single diodes. Considering that the same reading voltage of $\pm 2\text{V}$ was allocated for measuring the rectifying properties of the diodes and 1D1R devices and that the rectification ratio decreases with decreasing reading voltage (inset of Figure 4.6a), smaller rectification ratio was expected to 1D1R devices than those of diodes due to the smaller voltage drop on the diode component in 1D1R devices. Nevertheless, rather increased rectification ratio of the 1D1R devices compared to the diodes implies that the mitigated line resistance effect in 1D1R far outweighs the reduced voltage application to the diode component. Apparently the thicker Au of 1D1R (70nm) than that of the diode (30nm) effectively decreased the wire line resistance.

In addition, the feature size dependent resistive switching property was examined. In Figure 4.6c, the electroforming with current compliance of 1mA was only available in 1D1R devices with electrode area below $1500 \mu\text{m}^2$. That is, electroforming in the $2300 \mu\text{m}^2$ electrode area was not possible due to its too high leakage, as shown by the black curve in Figure 4.6c. On the other hand, despite the successful electroforming in the devices of $1500 \mu\text{m}^2$ and $900 \mu\text{m}^2$, reset failed apparently due to the too strong filament formation during the

preceding electroforming process, reflected by their small LRS resistances (R_{LRS}). Only the successful electroforming followed by reset process was available as the electrode area scaled down to $452 \mu\text{m}^2$. It can be noted that the small R_{LRS} of such reset-failed 1D1R devices of large electrode area is not solely from the fluent current (small resistance) at the forward bias of the diode component, but also from stronger filaments formation in the memory layers, because otherwise the reset should have occurred even more readily at smaller voltages due to the fluent current flow allowed by the diodes. Indeed, Figure 4.7a evidences the substantial effect of the diode component (1D) as a load resistor to the memory component (1R) in 1D1R. The black curve in the figure presents an attempt to electroform a single memory device with the same feature size ($16\mu\text{m}^2$) and memory stack configuration Pt(20nm)/Ni(20nm)/Pt(20nm)/TiO₂(20nm)/Pt(20nm) with the 1D1R shown in Figure 4.3d. The I-V curves of Figure 4.3d are overlapped alongside for easier comparison. Even with the same I_{cc} applied for the electroforming process, the single memory device without the diode failed to perform a successful memory operation but to give a hard breakdown.

Such a load resistor effect of the diode combined with the electrode area dependent diode characteristics may affect advantageous to the downscaling of the 1D1R device. Considering that the conduction at the reset moment is of metallic filament, as can be inferred from the electrode area dependent current density characteristics of Figure 4.4a, resistance of the 1D1R device itself can be calculated by linearly subtracting the line resistances of top and bottom electrode wires (Figure 4.4b-c) from the resistance measured from the raw I-V

curves of Figure 4.3d: the red circles in Figure 4.7b. The blue half-filled square of Figure 4.7b represents the calculated resistance of the 1D1R devices. In addition, the reset current and reset voltage of the device was obtained in Figure 4.7c by taking into account the voltage drop on the wire line resistances. Being consistent with the aforementioned 1D1R devices with dot-shaped electrodes, only the reset current decreases with the decreasing feature size, while the reset voltage is hardly changed, reflecting that smaller filament is generated in smaller devices. As the forward current of the diode decreases with decreasing feature size, its effect as a load resistor to the memory becomes significant. The load resistor acts as a voltage divider during set process, by which the excess voltage application to the memory layer is prevented so that the over-formation of the filaments is mitigated. By taking advantage of such an increasing load resistor effect with the decreasing feature size, the resistance state of the LRS may be even more accurately controlled, which further improves the reliability of a multi-bit operation. Moreover, the increased R_{LRS} of the 1D1R devices according to the feature size scaling in terms of power consumption and reset voltage margin.

Based on the device properties presented above, a double layers stacked 1D1R device was fabricated as shown in Figure 4.7a-c. The overall stack for the double layers stacked device is, Pt/TiO₂/Ti/Ni/Pt/TiO₂/Pt/Au/Pt/TiO₂/Ti/Ni/Pt/TiO₂/Pt/Ta₂O₅/SiO₂. Several modifications on its stack from the previous planar 1D1R device was applied to make it appropriate for the double layers stacking, which are as follows. First, a thicker Au of 100nm than that of the previous single layer stacked 1D1R

device (70nm) was applied to further mitigate the line resistance issue, which interrupts both to form the sufficiently strong filament in the memory layer and to apply the enough reset voltage to the device during the 1D1R operation. Secondly, since it was proven previously that the electron injection through the bottom interface of the diode is mainly governed by the local injection through the TiO₂/Ti, the unnecessary Pt element that has previously been placed between Ti and Ni in the planar 1D1R device (of Figure 4.3) was eliminated. Lastly, the thickness of the TiO₂ layer comprising the diode, which has been 60nm in the planar 1D1R, was reduced to 40nm. It is mainly to reduce the damage on the top electrode of the lower layer 1D1R during the RIBE process for the oxides of the lower layer underneath the electrode. It was found that the diode rectifying characteristic is independent to its TiO₂ thickness, at least within the thickness range from 30nm to 60nm, which implies for the conduction governed by interfaces for both biases. The consequent 1D1R random access will be presented in Figure 4.12.

The device morphology for the double-layers stacked 1D1R device observed by AFM is presented in Figure 4.9b. With the longitudinal electrode being the shared top electrode (TE) of the lower layer (LL) and the bottom electrode (BE) of the upper layer (UL), the BE of LL is aligned with the TE of UL. Therefore, the devices at both layers are exactly placed in the same position, which corresponds to the square shaped brightest part at the center of the figure. Basically in the AFM image, the brighter image indicates higher level of surface whereas the darker image corresponds to the lower level. The accurate align status of the device, which is determined particularly by the alignment among

the BE of LL and the TE of UL, can be further confirmed by the SEM image of Figure 4.9c. The overall alignment for a 4x4x2 CBA used for demonstrating a random access operation is provided in Figure 4.12a. The smaller ME of the UL than that of the LL is ascribed to the effect of larger step of the device on the electrode patterning by lithography. The EDS analysis result for a double layers stacked device evidences that the chemical composition of the lower layer is stays intact even after the upper layer fabrication, which is reflected by the identical chemical composition for both layers. Especially, despite the high chemical potential gradient of Ti and O in the diode layer, no such diffusion of those elements is found in the diode component of the LL mainly owing to the RT fabrication method. It is noteworthy that the BE of UL for the device fabricated for random access operation in 4x4x2 CBA is comprised of Pt/Au/Pt (as shown in Figure 4.9a) being different from the device stack shown in Figure 4.9b, where Pt was added atop to avoid the electron injection through the TiO₂/Au interface for the memory operation of UL. The following random access operation, endurance characteristic, and the 2-bit memory operation shown in Figure 4.12 through Figure 4.13 are achieved based on this modified 1D1R device stack.

The normalized distribution of the operation parameters for the devices in each layer is provided in Figure 4.11. The significant electroforming voltage difference between the devices of different layers led to different memory window for the devices in each layer. Such a difference is mainly ascribed to significant roughness problem in the devices of UL, which can be confirmed in Figure 4.9d. After the deposition of a thick TiO₂ layer of the LL diode,

roughness of the device is worsened and hence the electroforming voltage for the UL devices become smaller than that of the LL devices due to the relatively inhomogeneous electric field occurring in the UL devices. The decreased forming voltage leads to more resistive LRS and less resistive HRS of UL devices than those of LL devices.

In Figure 4.12, a successful random access being free from the line resistance issue, and the interruption among cells during the electroforming and reading was demonstrated in 4x4x2 CBA with the feature size of $2 \times 2 \mu\text{m}^2$ shown in Figure 4.12a. In the figure, the longitudinal electrode is the shared electrode for both layers, as the TE and BE for LL and UL, respectively. While the BE of LL and the TE of UL are horizontally placed with one being lied upon the other, their electrode contact pads are placed at the opposite side. Therefore, every cell in both layers can be individually biased. As shown in the figure, all the cells at each layer were numbered from #1 to #16 according to their position. In Figure 4.12b, it was confirmed that even the cells at both layers with the longest electrode are successfully operated being free from the reset failure due to the line resistance issue. Figure 4.12c illustrates possible disturbances during a random access operation in double layers stacked CBA with rectifying RRAM devices. While selecting a cell according to the blue arrow in the figure, typical sneak current paths in both layers are expressed with the red arrows. In the worst case, all of the cells are in LRS and therefore the sneak currents issue is maximized. Particularly for the RRAM devices accompanied with high rectifying property, the amount of current flowing through a sneak path at the worst case is limited by the reverse biased cell, due to its far high resistance

compared to those of the two forward biased cells connected in series to it. Therefore, the total amount of sneak currents is determined by the number of reverse biased cells that contribute to the sneak current paths. In an arbitrary double layer stacked CBA comprised of N word- and bit- lines, number of the reverse biased cells concerned in the sneak current paths at the LL and the UL are $(N-1)^2$ and N , respectively. Therefore, the total sneak currents in this double layers stacked CBA is evaluated as in the equation shown in Figure 4.12c. On the other hand, as the sneak current paths can be considered parallel resistances comprised of unselected cells, the unselected cells cannot avoid the disturbance by the simultaneous voltage application while biasing a selected cell for a write operation. Such severe disturbances during writing a selected cell by the unintentional voltage application to the unselected cells have been revealed in Yoon et al..²⁴ According to the study, the most disturbed cell in each layer while applying voltage to a selected cell are determined as the red bars in Figure 4.12c. Based on this analysis, while conducting an electroforming followed by reset and set operations for cell #16 of LL, (as presented in Figure 4.10c) #9 of LL and #12 of UL become the most disturbed cells. Figure 4.12d confirms the successful operations of the two most disturbed cells regardless of such voltage disturbance during the preceding operation of cell#16 of LL. In order to check the reading disturbance, every cell except for a selected cell of #1 in LL was turned to LRS as in Figure 4.12e. The insets of Figure 4.12e prove that the rectification ratios for the LRS cells in both layers are approximated to be 10^8 . In Figure 4.12f, the HRS of the selected cell #1 was read at the initial state 1 where all of the cells in the CBA except for the selected cell were pristine states.

Then, after turning all of the cells in the LL to LRS, making state 2, the HRS of the selected cell was read. The selected cell in HRS was successfully read even at the worst case of state 3, where all of the cells except for the selected cell were turned to LRS. Then, finally, a successful 1D1R operation of the selected cell was carried out as in the inset of Figure 4.12f, evidencing the sneak current prevention of these 1D1R devices due to their high rectifying property.

The endurance characteristic of the 1D1R device is presented in Figure 4.13. An intriguing aspect of the 1D1R device is that its rectifying property can be further enhanced with the repetitive cycling. It is mainly attributed to the property of the diode. In Figure 4.13a, the increasing forward current and decreasing reverse current with the increasing number of cycle results in a significantly increased rectification ratio even more than an order of magnitude. (Inset of Figure 4.13a) This is a totally distinguished behavior from a normal diode degradation tendency due to the Joule heat generation, where not only the forward but also the reverse bias current suffer severe degradation. It is normally caused by the resistance that the electrons suffer during their thermionic injection through the Schottky barrier within the diode. However, for the RT sputtered diode case, the forward bias current increases while the reverse bias current decreases, therefore, the internal defect migration according to the repetitive electric field application is considered to attribute to the case. As the Pt/TiO₂ layer is most likely to be affected by the electric field due to its high Schottky barrier, an interlayer oxygen ion migration within the region may incur the barrier modulation according to the electric field. While applying a positive voltage to the Pt, oxygen ions can escape from the TiO₂ and

become ad atoms within the Pt electrode, which act as a catalyst to capture and reproduce the oxygens. The generation of oxygen vacancies adjacent to the Pt/TiO₂ layer would lead to the Schottky barrier decrease, whereas the recombination of the oxygen vacancies by the negative bias voltage application will recover the Schottky barrier increase. As for a 1D1R device in Figure 4.13b, although the forward current is somewhat fluctuating due to the stochastic formation of the filaments within the memory layer, the evenly decreasing reverse current leads to an eventual enhancement in its rectification ratio (inset of Figure 4.13b). As a consequence, according to the rectifying property dependency on feature size (proven in Figure 4.6) and cycle repetition, the highest rectification ratio of 1.4×10^9 , is achieved in the smallest feature size of $4 \mu\text{m}^2$ within a few tens of cycles at the reading voltage of $\pm 2\text{V}$. (Figure 4.13c) Nonetheless, because such an obvious current level change of the diode is most likely saturated within the several hundreds of cycles, the diode showed a stable endurance characteristic of over 10^8 . (Figure 4.10b) A cycle is comprised of alternately applied pulses with the height of $\pm 2\text{V}$ and the width of $2 \mu\text{s}$, in series to a reading pulse of $+1\text{V}$ with the width of $50 \mu\text{s}$. On the other hand, in Figure 4.13d, the endurance of the 1D1R device lasted up until 450 cycle. The obvious degradation of the 1D1R endurance characteristic compared to that of the diode may be attributed to the application of an incremental step pulse programming in the switching device. The incremental step pulse programming is the method generally used in the conventional NAND flash, in which the height of the pulse is gradually increased by 0.1V until the resistance of the device reaches the desired resistance range, which in this case was set up as $50,000 \Omega$ and $250,000$

Ω for LRS and HRS, respectively. Therefore, the method is highly appealing for minimizing the switching failure due to the operation parameter variation according to the repeated switching events. However, due to the multiple pulse application required for completing one cycle, severely accumulated stress to the device over the repeated cycling is very likely to degrade the endurance characteristic. In addition, the endurance characteristic of the 1D1R device may also be limited by the memory layer, or the oxygen diffusion barrier layer placed between the memory and diode layer. In this case, Ni was inserted as the oxygen diffusion barrier to prevent the oxygens sneaking into the bottom interface of diode during the set processes of memory layer. Further improvement in the endurance characteristic may be expected if provided with the insertion of other materials as an oxygen diffusion barrier layer.

A 2-bit operation consisting of four different resistance states is obtained in this 1D1R device of $4 \times 4 \mu\text{m}^2$. Figure 4.14a provides a normalized read current distribution for the three LRS and one HRS, whose state is determined by varying the I_{cc} during the set process in DC sweep mode operation. In Figure 4.14b, it is shown that such different I_{cc} range applied during the set processes gives clearly distinguished LRS states. To ensure the stability of four different resistance states, retention characteristics for each state was examined. For sake of simplicity, the LRS1 corresponding to the smallest resistance range and the LRS3 with the highest resistance range were tested in addition to the HRS characteristic. The resistance stability that lasts over 10^4 s at 85°C guarantees the 10 years retention. Little overlaps among the states proves a promising 2-bit operation that further reduces the cell size of the double layers stacked 1D1R

CBA from $2F^2$ down to F^2 , where F is the minimum feature size, or the node size.

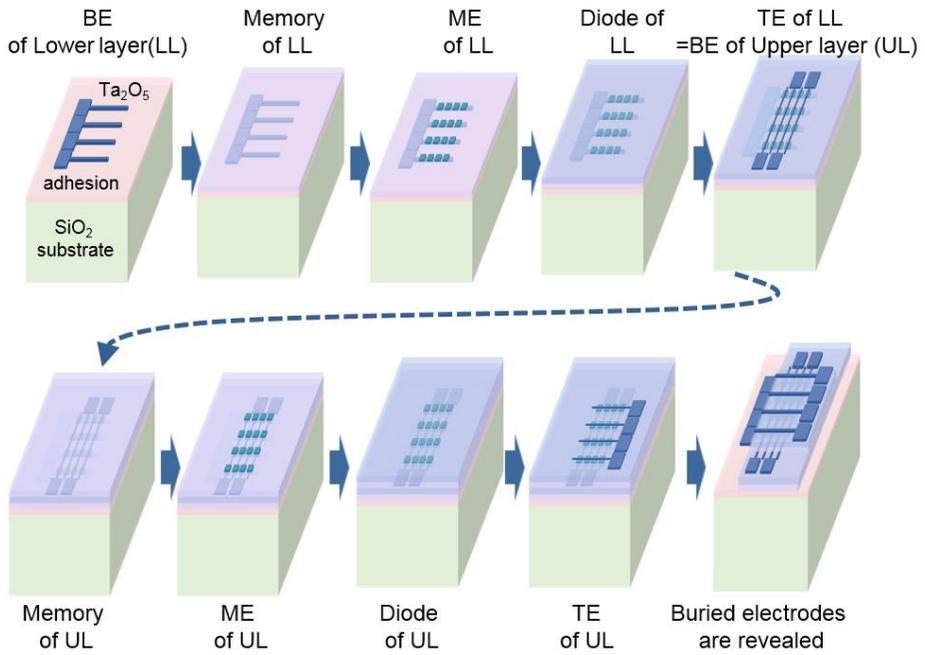


Figure 4.1 Overall fabrication process of the double-layers stacked 1D1R

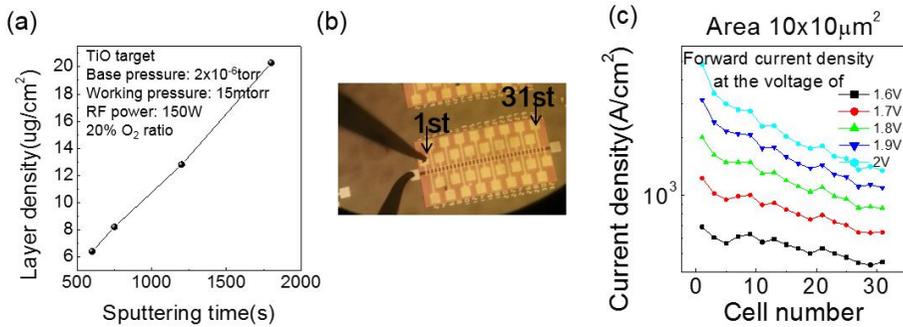


Figure 4.2 (a) Layer density of the RT sputtered TiO₂ (b) 1x32 diode CBA (c) forward current degradation according to the distance from the electrode contact pad.

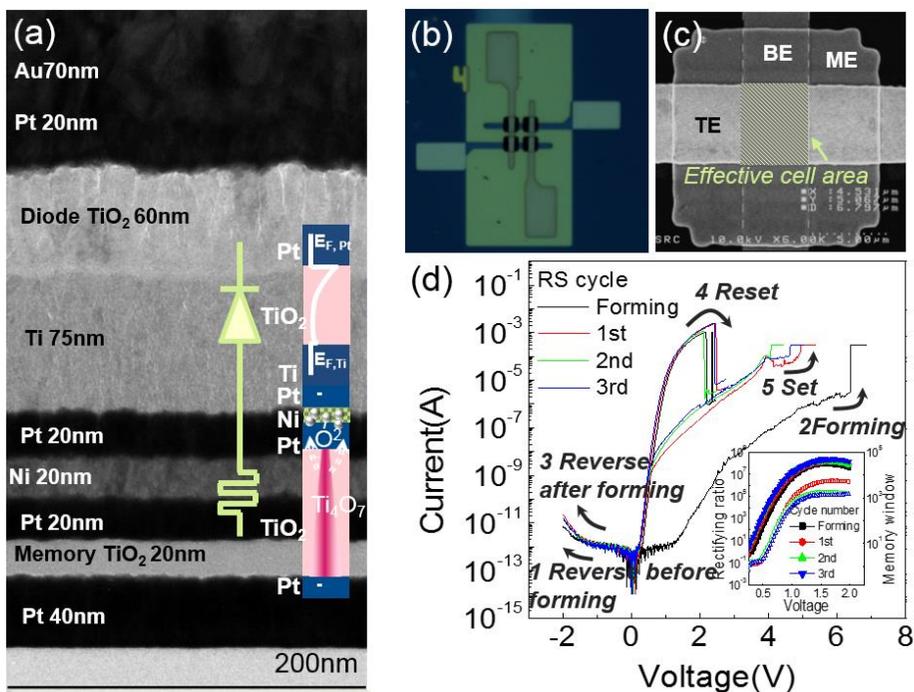


Figure 4.3 (a) Cross-sectional HRTEM image of the 1D1R (b) Top-viewed optical microscopy image of a 2x2 1D1R CBA (c) Top-viewed SEM image of a single 1D1R device (d) Typical I-V characteristics of 1D1R.

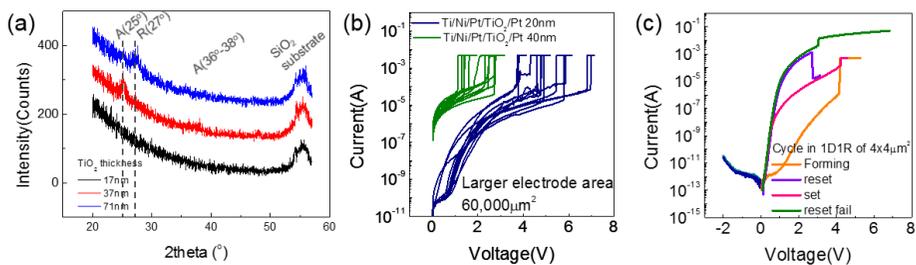


Figure 4.4 (a) Thickness dependent XRD patterns for the RT sputtered TiO₂ (b) Comparison in the leakage and dielectric breakdown characteristics of RT sputtered TiO₂ according to its thickness. (c) Resistive switching failure in the 40nm-TiO₂ memory case of 1D1R.

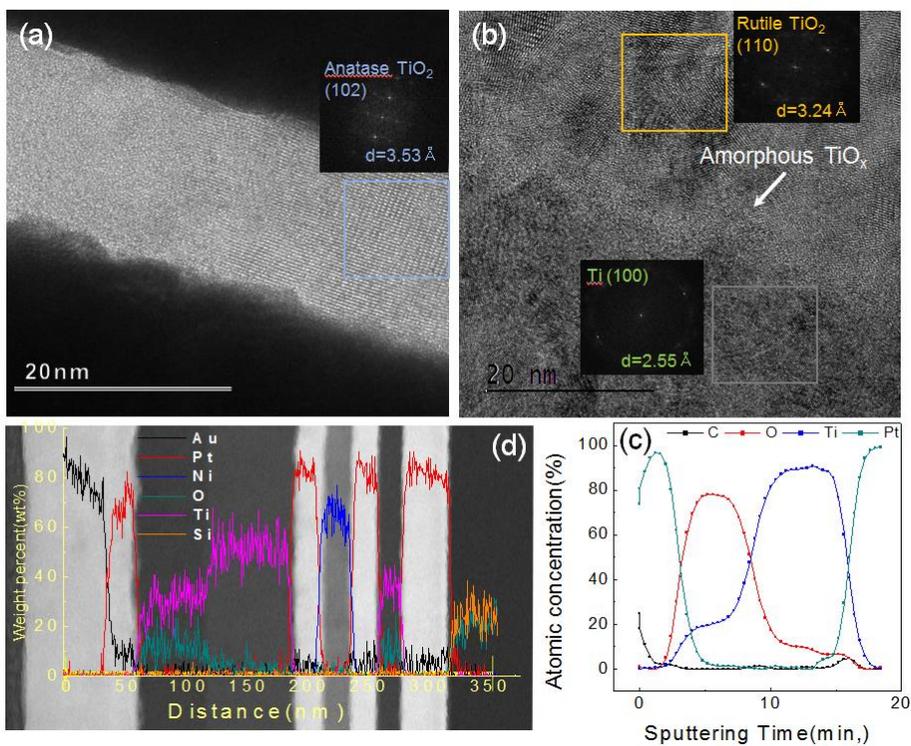


Figure 4.5 HRTEM analysis of the (a) memory layer (b) diode layer of the 1D1R. (c) AES chemical composition analysis of the diode (d) EDS chemical composition analysis.

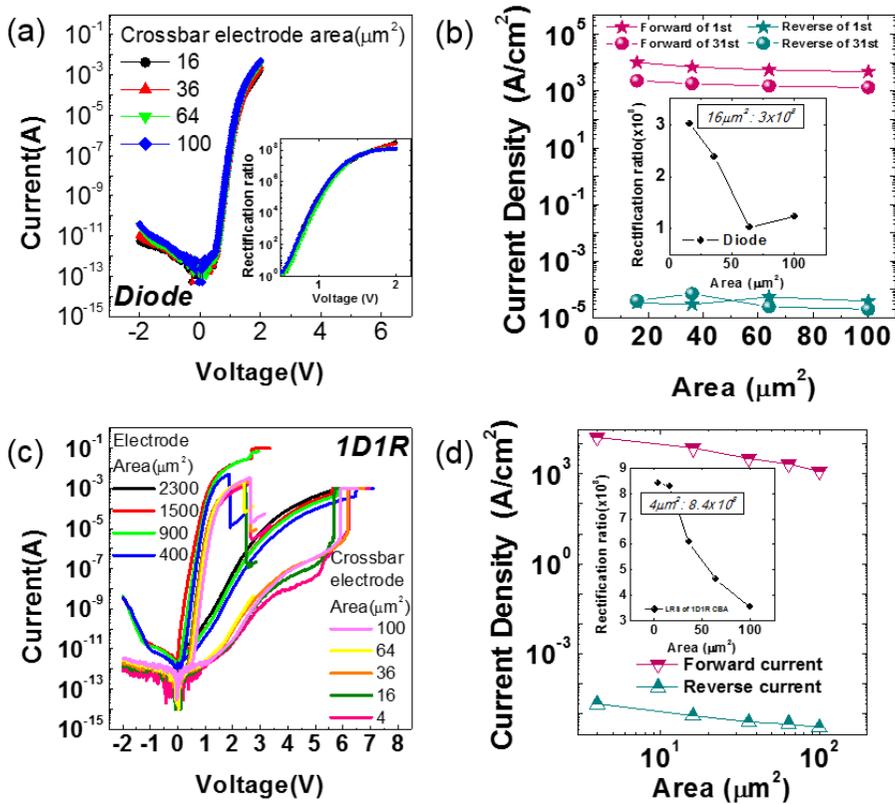


Figure 4.6 I-V curves and rectifying property of (a)(b) diode (c)(d)1D1R.

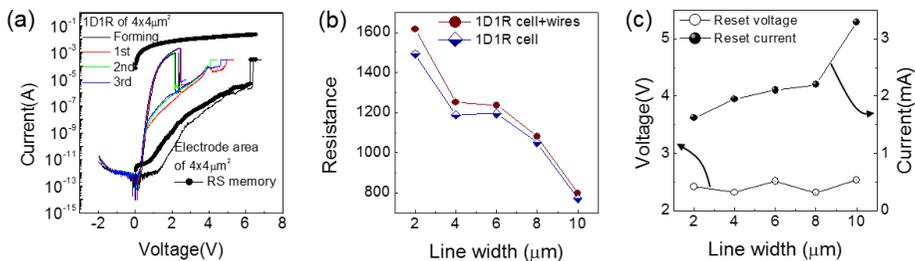


Figure 4.7 (a) Comparison between the I-V characteristics of a 1D1R device and a single memory device with the same materials stack applied for the memory layer (Ti/Pt/Ni/Pt/TiO₂/Pt) and the same electrode area ($4 \times 4 \mu\text{m}^2$) (b) Device resistance during the reset process and (c) reset current and reset voltage according to line width, for the node size

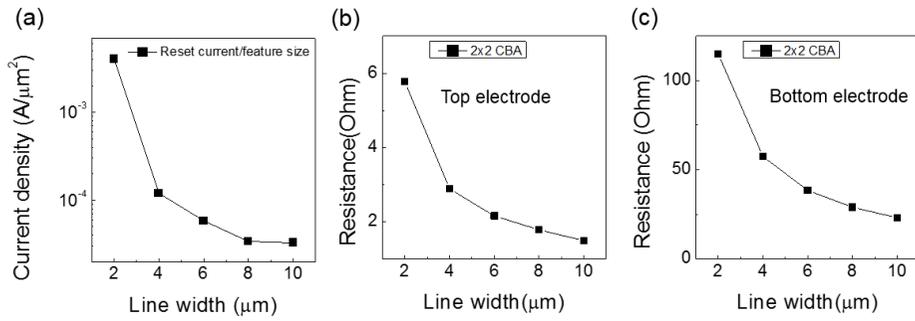


Figure 4.8 (a) Current density measured at the point immediately prior to the reset process according to line width. Resistance of the wires for of (b) top and (c) bottom electrode in 2x2 CBA.

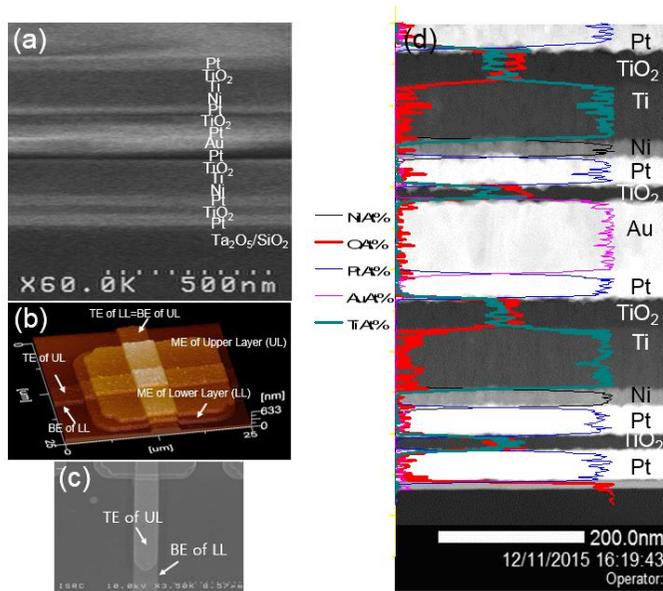


Figure 4.9 (a) SEM and (b) AFM image of the double layers stacked 1D1R device. (c) Alignment between TE of UL and BE of LL confirmed by SEM (d) EDS analysis for the double layers stacked 1D1R device.

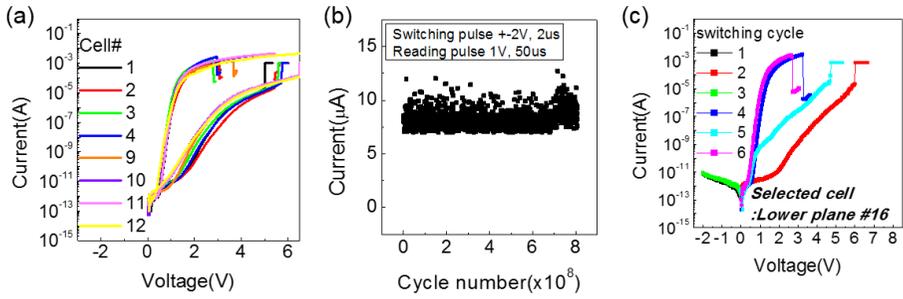


Figure 4.10 (a) Line resistance issue of the 1D1R device applied with a thinner Au (70nm) according to its cell number in 4x4 CBA (b) diode endurance characteristic (c) operation of a selected cell of #16 for examining the writing disturbance.

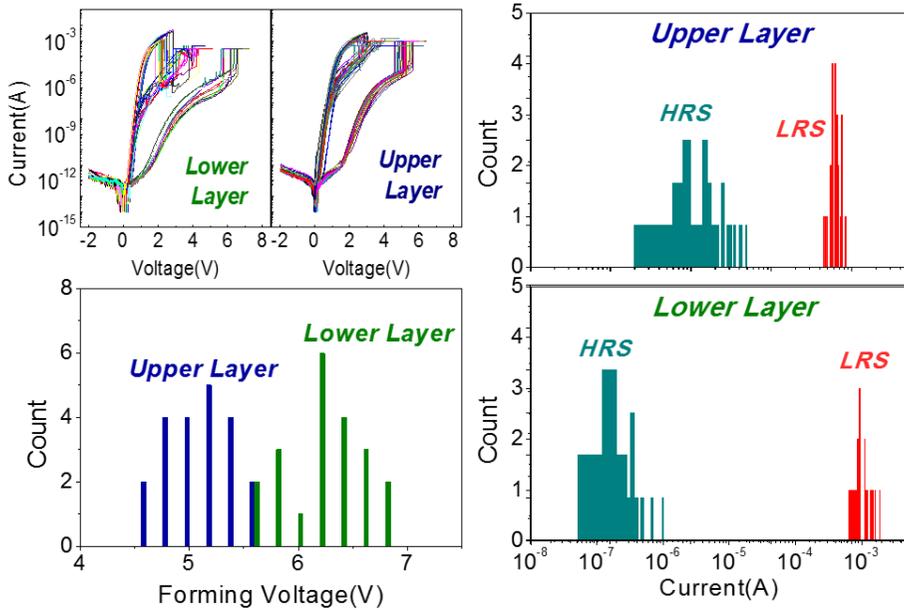


Figure 4.11 Resistive switching characteristics comparison for the upper and lower layers.

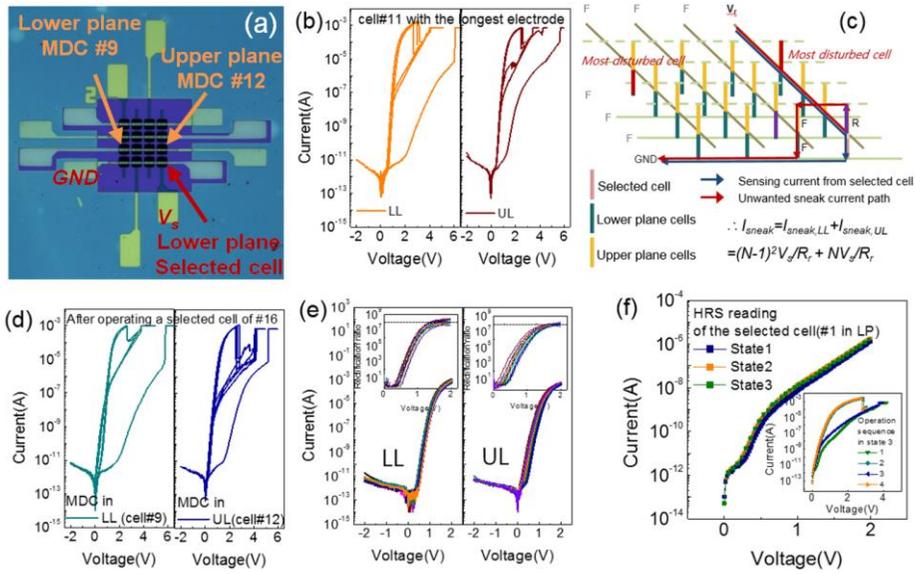


Figure 4.12 (a) Optical microscopy for 4x4x2 CBA (b) 1D1R operation in the cells at LL and BE with the longest wire length (c) Writing and reading disturbance in the CBA (d) 1D1R operation in the most disturbed cells in the CBA after the operation of a selected cell (e) LRS of the cells in the CBA except for the selected cell and their rectification ratio (insets) (f) HRS reading and 1D1R operation (inset) of the selected cell where the line resistance issue is alleviated.

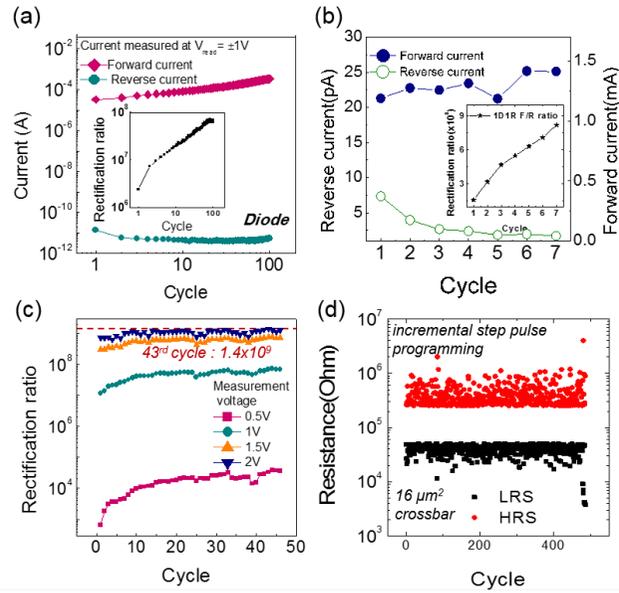


Figure 4.13 cycle dependent I-V characteristics of (a) diode (b) 1D1R device of $4 \times 4 \mu\text{m}^2$ (c) 1D1R device of $2 \times 2 \mu\text{m}^2$ (d) endurance characteristics obtained from a 1D1R device of $4 \times 4 \mu\text{m}^2$ measured using an incremental step pulse programming method

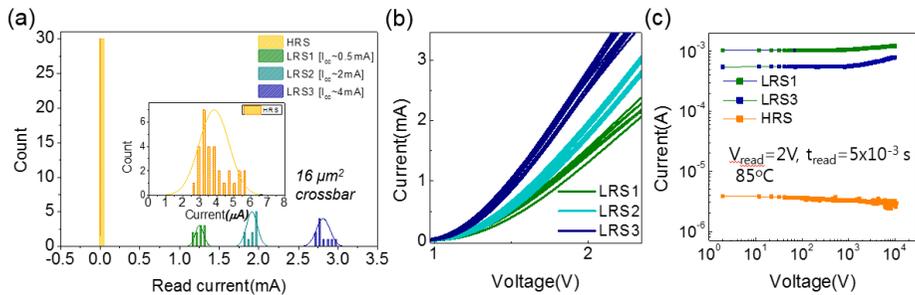


Figure 4.14 (a) Normalized read current and (b) I-V characteristics of 2-bit operation consisting of one HRS and three LRS determined by allocating different I_{cc} during the set operation in DC sweep mode. (c) Retention characteristic of the LRS1 and LRS3, each being the LRS with the lowest and the highest resistance range, in addition to a HRS.

4.4. Summary

While the announcement of the 3D X-point memory was a truly astonishing event in the community, the memory cell efficiency (ratio between the areas taken by the memory cells and total Si surface area) might not be optimally high. Considering the uncovered wafer image where ~250 chips presented on 300mm-diameter wafer, and the technology node (20 nm with $2F^2$ cell size) adopted, the estimated cell efficiency might be 30 – 35%, so in fact an even higher portion of the wafer surface was taken by periphery circuits. There could be many factors that resulted in this non-optimal aspect, but the limited performance of their cell selector might be a significant contributor to that problem. The crossbar RRAM presented here has an even reduced cell size of F^2 , being fully equipped with the ultimate requirements to compete with NAND flash: vertical integration, high selectivity, and multi-bit operation. A room temperature deposition method of diode and memory is adopted to avoid thermal budget issue during layer stacking process for a double layer crossbar memory. The deposition method led to an extremely high rectifying characteristic of diode by suppressing the oxidation of Ti electrode, which is more likely in high temperature processes. The rectification ratio of the 1D1R RRAM device is more than 1000 times increased to the previous reports on the ReRAM devices accompanied with rectifying property, meaning for the 1000 times increased memory density based on the reading margin evaluation in a crossbar array. Although the size of CBA demonstrated here is only $4 \times 4 \times 2$ and the smallest feature size remains in $2 \times 2 \mu\text{m}^2$, due to the limitation from a lab-scale fabrication, high cell efficiency in addition to high scalability of the 1D1R

device in both the rectification property and the cell resistance aspects will provide a valuable recipe toward the high density crossbar array integration.

4.5. Bibliography

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5. Conclusion

The analytical model for WM evaluation proposed in section 2 was applied to the fabricated 1D1R crossbar RRAM device fabricated in section 4. For an application to WM evaluation, the r_d is obtained from the rectification ratio measured at ± 2 V while R_{cell} is calculated by subtracting the wire resistance of the 2x2 CBA from the resistance at the point immediately prior to the reset in the raw I-V curves in Figure 4.3d. Figure 5.1a-b provide a pad-to-pad resistance measured for the bottom and top electrodes of this device, which corresponds to the bit and word lines of a crossbar array, respectively. From this value, the total wire resistance for each line width within the 2x2 CBA is calculated. On the other hand, the increasing current density of LRS with decreasing line width, as shown in Figure 5.1c, implies strong local conduction (conducting-filament (CF)-mediated mechanism for the URS). Therefore, the electrical conduction at such a high-voltage region immediately prior to the reset process is governed by the conduction through the CFs within the memory layer, and it has been well established that the CF in TiO_2 is composed of the Magnéli phase. Therefore, R_{cell} can be obtained by linearly subtracting the wire resistance from the resistance obtained from the raw I-V behavior.

Then, as mentioned above for the case of the URS rectifying RRAM in Figure 2.5c, the smaller set voltage of $\sim +5$ V compared to the breakdown voltage of ~ -15 V is adopted for the standard voltage for writing margin evaluation, giving $c=2$ with respect to the reset voltage of ~ 2.5 V.

The R_{wire} for a bit and word line can be evaluated from the aforementioned pad-to-pad resistance shown in Figure 5.1a and b. As illustrated in Figure 5.2a,

with F^2 being the feature size, F becomes the line width of the wires as well as the space between such wires. Therefore, R_{wire} , denoting the resistance of a wire element (or the wire resistance per cell), can be expressed in terms of resistivity of wires ρ_{wire} , line width F , and thickness of wires t , which turns out to be constant over all the ranges of the line width or the node size in this work, as follows:

$$R_{\text{wire}} = \rho_{\text{wire}} \frac{2F}{tF} = \rho_{\text{wire}} \frac{2}{t} \quad (17)$$

While an increased array size is obtained by shrinking the node size, a constant R_{wire} value is applied irrespective of the array size. As the metal electrodes in this work were composed of several layers whose material parameters could be deviated from the bulk values, the nominal R_{wire} can be estimated from the slopes of the best-linear-fitting plots using equation (20). The equation is obtained by substituting (17) into (19).

$$R_{\text{pad-pad}} = \rho_{\text{wire}} \frac{l}{tF} \quad (l: \text{pad to pad distance}) \quad (18)$$

$$\frac{\rho_{\text{wire}}}{t} = \frac{1}{l} \frac{d(R_{\text{pad-pad}})}{d\left(\frac{1}{F}\right)} \quad (19)$$

$$\therefore R_{\text{wire}} = \frac{2}{l} \frac{d(R_{\text{pad-pad}})}{d\left(\frac{1}{F}\right)} \quad (20)$$

In Figure 5.2a b and 5.2c, the R_{wire} of a word and bit line for this 1D1R device is calculated to be 0.61 and 13.1 Ω , respectively, where the difference is attributed to the materials and thickness adopted for each wire. Each plot was made from the $R_{\text{pad-pad}}$ shown in Figure 5.1a and b. The use of Au (130nm) in addition to Pt (50nm) in the word line wire can greatly decrease the resistance

by more than an order from that of the bit line wire, where only Pt (50nm) is used.

From the aforementioned experimental data, the evaluated WM is plotted in Figure 5.3 as a function of the array size, where the adopted parameters are $R_{\text{wireWL}}=0.61$, $R_{\text{wireBL}}=13.1$, $r_d=8.4 \times 10^8$, and $R_{\text{cell}}=1493 \Omega$, which were estimated from the $2 \times 2 \mu\text{m}^2$ device. Also, the corresponding array size allowing for a 10% voltage margin is shown in Table 2. Even with the highly promising value of $r_d=8.4 \times 10^8$, the available array size guaranteeing a 10% WM was only $\sim 10^4$, which is disappointing. This is mainly due to the high resistance of the bit line; for $R_{\text{wireBL}}=13.1$, $N=100$ means that the worst-case bit line resistance is as high as $\sim 1310 \Omega$, which is almost comparable to R_{cell} . This calculation indicates the importance of a small wire resistance for the stable operation of CBA. As the device that was fabricated in this work was just a prototype to demonstrate the feasible stacking of 1D and 1R which was not optimized for the WM aspect of CBA, the possible improvement of the array size was expected by varying several parameters, as shown in Figure 5.3.

When the R_{wireBL} was assumed to decrease to a value that was the same as that of the word line (0.61Ω), which could be readily accomplished in the experiment by adding an Au layer, the available array size drastically increased to $\sim 10^6$, confirming the critical importance of the wire resistance. Another tenfold increase could be accomplished by increasing the R_{cell} only threefold, which was also expected to be rather easy to do in the experiment. Increasing the r_d further to a 10^{10} value, however, did not improve the WM at all, suggesting that the experimentally achieved r_d of $\sim 10^9$ was already high enough.

When the r_d was assumed to decrease to 10^6 with the aforementioned decreased R_{wireBL} and increased R_{cell} , the WM decreased again, again demonstrating the importance of a high r_d . These calculations revealed that the optimized R_{wire} and R_{cell} are critical parameters for a high array size when a sufficiently high r_d is guaranteed.

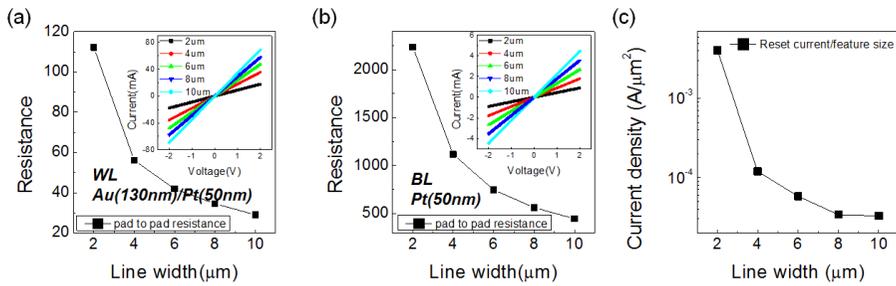


Figure 5.1 Pad-to-pad resistance according to the 2-10 μm line width of the (a) word line (top electrode) and the (b) bit line (bottom electrode). The insets represent the raw I-V data. (c) Current density in LRS measured at the voltage immediately before the reset process.

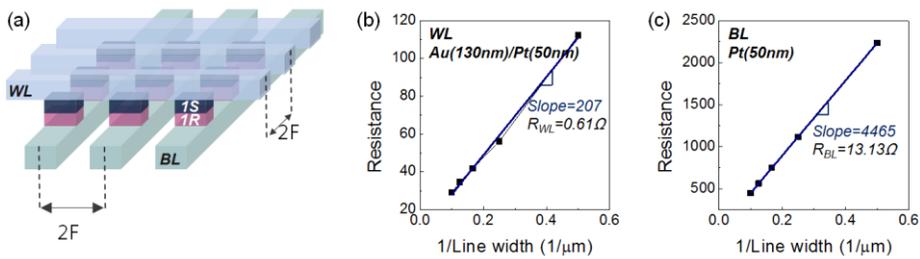


Figure 5.2 (a) Schematic of a 1 selector-1 resistor (1S1R) RRAM CBA with the node size F. R_{wire} from the slope of the pad-to-pad resistance-1/line width of a (b) word line and (c) bit line.

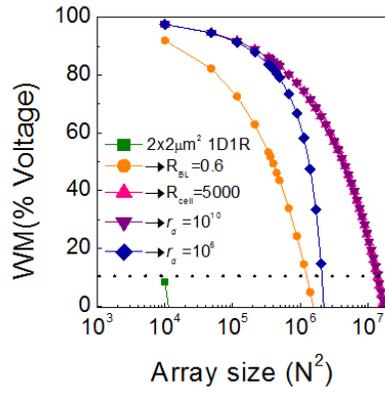


Figure 5.3 Percent writing margin for the current 1D1R device in addition to the cases applied with further improvements

국문 초록

정류특성이 동반되는 저항변화메모리를 이용한 3 차원 적층 구조의 크로스바어레이 제작 및 평가

저항변화 메모리는 전기적 신호에 따라 변하는 물질의 저항상태 간에 메모리 동작을 도모하는 차세대 비휘발성 메모리이다. 특히 저항변화 메모리는 선택소자로서 트랜지스터를 필요로 하지 않기 때문에 $4F^2$ 의 작은 단위 소자 크기 (cell size)을 구현 할 수 있는 크로스바 어레이 (Crossbar array)로 적용 가능하며, 이를 수직 적층한 구조에서는 매우 경제적인 메모리를 제작할 수 있다는 점에서 낸드플래시 (NAND flash) 메모리의 축소화 한계를 극복할 수 있는 고집적 저장 매체로서 주목받고 있다. 그럼에도 불구하고 크로스바 어레이에서의 간섭 전류는 실제 고집적 저항변화 메모리 구현을 방해하는 주요 장애 요소이다. 따라서 이러한 간섭 전류를 제거하기 위해 소자적으로는 개별 메모리 셀에 다이오드 (diode) 또는 문턱스위치 (threshold switch) 등의 이단 선택소자 (two-terminal selector)를 접합하거나, 회로적으로는 어레이에서의 전압 인가 방식 (voltage scheme)을 조절하는 등의 접근 방식 하에 활발한 연구가 진행되고 있다. 간섭 전류는 선택된 셀에 대한 병렬 저항 요소로 간주되기 때문에 주로 선택된 셀의 저항 상태를 확인하는 읽기 (reading) 동작에서 문제로 여겨진 반면, 선택된 셀에 전압을 인가하는 쓰기 (writing) 동작에서는 그 부정적인 영향이 간과되었다. 때문에 그 동안 간섭 전류의 억제를 목표로 한 연구들은 대부분 읽기 마진 (reading margin) 평가에 의존되어 왔다. 본 논문은 고집적 크로스바 어레이에서의 간섭 전류가 쓰기 동작에도 치명적인 문제를 야기하는 것을 밝히고, 이러한 관점에서 쓰기 마진

(writing margin)을 평가하는 방식을 제안한다. 이를 시작으로 이러한 간섭 전류를 효과적으로 억제할 수 있는 소자로서 컴플리멘터리 저항변화 메모리 (complimentary resistive switching memory)와 1 다이오드-1 저항변화메모리 (1Diode-1Resistive switching memory, 1D1R)의 제작과 이들의 배경 메커니즘에 대한 연구를 다룬다. 더 나아가, 1D1R 소자의 복층 구조를 구현하여 이의 동작을 평가한다.

첫 번째, 크로스바 어레이에서 간섭 전류를 고려한 쓰기 마진을 평가하는 연구에서는, 쓰기 동작 시 간섭 전류를 형성하는 원인인 선택되지 않은 소자들에 인가되는 전압이 해당 소자들의 저항 상태를 변화시킬 수 있는 요인임을 HSPICE 시뮬레이션을 통해 밝힌다. 다이오드 선택 소자를 삽입하여 정류특성이 동반되는 저항변화 메모리의 경우, 선택한 소자를 쓰기 위해 워드 라인 (word-line)에 인가하는 전압과 비등한 크기의 반대 방향의 전압이 다수의 선택하지 않은 소자들에 인가된다. 따라서 이러한 방해 전압이 인가되는 소자들의 저항 상태를 변화시키지 않는 전압 범위 내에서 쓰기 전압 마진이 결정된다. 한 편, 고집적 메모리일수록 간섭 전류로 인한 워드/빗 라인 (word/bit line)에서의 전압 강하가 두드러지고, 이로 인해 선택된 셀을 쓰는데 요구되는 전압 자체가 증가하기 때문에 주변 셀들에 인가되는 방해 전압도 증가하여 쓰기 마진은 더욱 줄어든다. 각 셀들에서 발생하는 간섭 전류의 양과, 이로 인한 워드/빗라인에서의 전압 강하를 고려한 계산을 통해 소자 종류와 상관없이 유용한 쓰기 마진 평가 모델을 도출하고, 이를 HSPICE 시뮬레이션 결과로 검증하였다.

이러한 간섭 전류를 억제할 수 있는 정류 특성이 동반된 저항 변화 메모리 시스템으로서 먼저 컴플리멘터리 저항변화 메모리에 대한 연구를 진행하였다. 컴플리멘터리 저항변화 메모리는 두 개의 양극성 저항변화

소자 (bipolar resistive switching memory, BRS)를 서로 반대 방향으로 직렬 연결하여 서로 다른 고저항 상태 간의 메모리 동작을 도모한다. 두 개의 저항변화 소자를 접합해야 하기 때문에 이 동작을 얻기 위해서는 다층의 박막 증착이 불가피하다. 이러한 다수 박막 증착의 복잡성을 개선하기 위해, 본 연구에서는 전압 인가를 통해 통해 금속성의 산소부족상인 마그넬리(Magnéli)로의 전이가 가능한 TiO_2 와 WO_3 를 이용하여 단일 산화물 박막층으로 이루어진 $\text{Pt/TiO}_2/\text{Pt}$, $\text{Pt/WO}_3/\text{Pt}$ 소자에서 단순히 전기적 자극을 통한 컴플리멘터리 저항변화 메모리 방식을 제안한다. 온도 의존 전류-전압 특성으로부터 스위칭이 발생하는 두 고저항 상태가 Pt/TiO_2 와 Magnéli/TiO_2 계면 상의 쇼트키 장벽을 통한 전도임을 확인하였으며, 이로부터 마그넬리 필라멘트가 일부 소멸되는 과정에서 국부적으로 발생한 다수의 산소 공공 결합에 의한 스위칭 모델을 확인한다. 또한 전압 펄스 분석을 통해 스위칭 과정에서 실시간으로 메모리에 흐르는 전류를 확인하고, 전압 승강 모드에서의 스위칭을 통해 구체적인 스위칭 메커니즘으로서 산소 공공 결합이 야기한 높은 공간 전하 밀도 (space charge density)에 의해 강화되는 국부적인 줄열이 전기장에 의한 산소 공공의 이동성 (mobility)을 높이는 스위칭 거동을 파악하였다.

궁극적으로 수직 적층이 가능한 고밀도 저항변화 메모리 특성을 얻기 위해 우수한 정류 특성의 쇼트키 다이오드를 접합한 저항변화 메모리를 개발하였다. 상부 어레이 증착시 하부 어레이가 겪을 수 있는 열적 피해 (thermal disruption)를 피하고자 상온 공정이 가능한 스퍼터 증착 방식으로 다이오드와 메모리 층에 삽입되는 TiO_2 산화물 박막을 증착하였다. 상온 공정 $\text{Pt/TiO}_2/\text{Ti}$ 다이오드에서는 기존에 보고된 원자층박막증착법 (Atomic Layer Deposition)을 통한 고온 공정 $\text{Pt/TiO}_2/\text{Ti/Pt}$ 다이오드에 비해 1000 배

정도 개선된 정류비 ($>10^8$) 를 확보할 수 있었으며, 이는 TiO_2 증착 과정에서 Ti 에 의한 TiO_2 의 불안정한 환원으로 인해 발생하는 TiO_2 내부의 불필요한 누설 전류 (leakage current)를 억제할 수 있기 때문임을 AES (Auger Electron Spectroscopy), EDS (Energy-dispersive X-ray spectroscopy) 조성 분석을 통해 확인하였다. 또한 소자 크기가 감소할수록 정전류의 증가와 정류 특성이 개선됨에 따라 축소화에 유리한 다이오드 특성을 확인하였다. 저항변화메모리와 다이오드를 접합한 1D1R 소자로부터 가장 작은 $2 \times 2 \mu m^2$ 소자에서 최대 정류비 8.4×10^8 가 동반되고 10^{34} 의 On/Off 비를 가지는 안정적인 메모리 특성을 확보하였다. 또한 복층 구조로 구현한 $4 \times 4 \times 2$ 크기의 크로스바 어레이에서 간접 전류로부터 자유로운 선택한 소자의 읽기, 쓰기 동작을 확인하였다.

핵심어: 저항변화메모리, 크로스바어레이, 간접전류, 쓰기 마진, 선택조자 요건, 컴플리먼트리 저항변화 메모리, 1다이오드-1저항변화메모리, 3차원 적층 저항변화 랜덤 액세스 메모리

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