Ph.D. DISSERTATION

Electrical characteristics of SnO_x transparent p-type semiconductor for thin film transistor applications

by

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Abstract

This dissertation investigates the structural, chemical and electrical properties of reactive sputtered SnO_x films at the various oxygen partial pressure (P_o) and post annealing temperature (T_A) for the potential p-channel oxide thin-film transistors. In addition, this dissertation also discusses the effect of the various interface layers on the electrical functionality of p-type SnO_x TFTs.

The 210 °C annealed SnO_x film prepared at the low P_o of 4% consisted of the dendrite morphology and metal Sn cluster. The resulting p-channel SnO_x thin-film transistors (TFTs) suffered from the marginal mobility and low $I_{ON/OFF}$ ratio, suggesting that these structural imperfections caused by the oxygen deficient non-stoichiometry hindered the effective hole carrier conduction and acted as the bulk trap states. The dendrite structure and metallic Sn cluster in the 210 °C annealed SnO_x could be eliminated by increasing P_o. Thus, the TFT with the p-type SnO_x film prepared at the high P_o = 8 % exhibited the high mobility of 2.8 $cm^2V^{-1}s^{-1}$ and excellent $I_{ON/OFF}$ ratio of ~10^3, which underscored the critical role of the homogeneous ordered structure without the Sn metal aggregate and abrupt dendrite structure. For the given optimal P_o (= 8 %) condition, the device performances such as the μ_{FE} and $I_{ON/OFF}$ ratio of the p-channel SnO_x TFTs were deteriorated with increasing T_A from 210 to 300 °C, which was attributed to the disproportionation reaction [$2SnO \rightarrow SnO_2$

+ Sn].

In addition, the complementary metal oxide semiconductor (CMOS) inverter using p-type SnO_x and n-type Zn-Sn-O (ZTO) thin films was demonstrated with the peak gain of -4.4. These results are comparable to those of other oxide CMOS reported previously.

The effect of various interface layers, such as thermally-grown SiO_2, 7 nm-SiN_x, Al_2O_3 and SiOF, on the bottom gate SnO_x TFT functionality was also studied.

SnO_x TFTs showed quite different electrical functionalities according to interface layers. The SnO_x TFT on the thermally-grown SiO_2 showed μ_{FE} of 2.8 $cm^2V^{-1}S^{-1}$ and $I_{ON/OFF}$ of 1.8×10^3 and V_{th} of 19 V. However, the SnO_x TFT on SiN_x showed marginal functionality. The μ_{FE}, $I_{ON/OFF}$ and V_{th} were degraded to 2.1 $cm^2V^{-1}S^{-1}$, 7.9 and over 40V, respectively. Conversely, the SnO_x TFT on SiOF exhibited best performance. The μ_{FE} and $I_{ON/OFF}$ were 3.1 $cm^2V^{-1}S^{-1}$ and 1.6×10^3, respectively. Interestingly, the V_{th} was shifted to 2 V.

From the XPS analyses and the resulting relative band structure, it was found that the marginal performance of SiN_x interface was originated from relatively small valence band offset and large tail state over VBM of SiN_x.

The fixed oxide charge and interface dipole, which could modulate flat band voltage, could not be causes of V_{th} shift in p-type SnO_x TFT on SiOF interface, because n-type ZTO TFT on SiOF did not show any V_{th} shift. To explain V_{th} shift in SiOF, Fermi level pinning at the interface was also suggested. High V_{th} of 19 V in

SnO_x TFT on SiO_2 might be attributed by Fermi level pinning near the VBM. However, in SiOF, fluorine atoms help reducing defect density at bulk or surface in the band gap. Therefore, Fermi level is less pinned near VBM and V_{th} can be shifted in negative direction (19 → 2 V). The explanation well supports the estimated $D_{it,\ max}$: 2.5×10^{13} (SiO_2) → 1.9×10^{13} (SiOF)

Keywords: Tin oxide, p-type oxide semiconductor, thin film transistor, complementary metal oxide semiconductor, oxygen pressure, annealing temperature, interface layer

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Chapter 1. Introduction

1.1 Overview

Metal oxide semiconductors (MOSs) have received remarkable attention as backplane materials for flat panel displays such as liquid crystal (LC)- and organic light emitting diode (OLED)-based displays due to their cost effective, low-temperature processability and high carrier mobility. Furthermore, in recent years, they have been studied extensively as a promising materials for emerging applications such as flexible and transparent electronics due to their outstanding characteristics, showing high optical transparency and high electrical conductivity [1, 2, 3].

A n-type In-Ga-Zn-O (IGZO)-based semiconductor has already been commercialized as backplane of flat panel display, yielding excellent device performance with electron mobility over 10 $cm^2V^{-1}s^{-1}$ [4]. However, p-type MOSs still need to be improved. The reasons of this discrepancy can be found in band structures of oxide semiconductors. MOSs have the conduction band (CB), which typically contains a conduction path generated by delocalized s-orbitals of metal ions, while the valence band maximum (VBM), as a conduction path of holes, is mainly composed of localized p-orbitals of oxygen ions. Due to the characteristics of MOSs, injected electrons in these thin films are easily transferred along the conducting path

and show good mobility regardless of structure ordering, in comparison to holes. Nevertheless, p-type MOSs have been persistently studied because they are necessary to fabricate inverters and/or logic circuits for low power consumption and transparent device applications, etc [3].

To date, extensive materials have been studied to adjust p-type semiconductor applications and most of those studies are focused on monovalent Cu based oxide materials with Cu 3d orbitals, which have similar energy level with O 2p orbitals and form hybridized orbitals with O 2p, showing low hole effective mass and good p-type conductivity [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. Especially, Cu_2O shows p-type conductivity with high hole mobility over 100 $cm^2V^{-1}s^{-1}$ [13]. However, TFTs with these Cu based oxides show poor performances with field effect mobility of ~1 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ of ~10^2 due to too high hole concentration or the high tail states and surface densities at the channel ~ insulator interface [10, 11, 12, 13, 17].

Another approach for good p-type properties is using materials, which have pseudo-closed ns^2 orbitals having energy level closed to O 2p orbitals [18, 19, 20, 21]. Among them, SnO is a promising candidate of p-type oxide semiconductors for TFTs applications [18, 22]. Sn 5s and O 2p orbitals of SnO compose hybridized orbitals which reduce localization of valence band edge, so that SnO have effective hole transport path and show high hole mobility [23, 24]. TFTs based on p-type SnO are expected to fulfil these requirements due to the particular nature of band

structure [24].

Recently, chemical positions and related process conditions for p-type SnO have been studied intensively to improve electrical functionality of p-type SnO [7, 25, 26, 27, 28, 29]. Moreover, it has been reported that the p-type SnO_x TFT fabricated in Sn rich condition shows excellent field effect mobility (μ_{FE}) of 6.75 $cm^2V^{-1}s^{-1}$, which is comparable to that of n-type oxide TFTs [29]. However, The comprehensive understandings about the process conditions, related characteristics of thin films and electrical functionality of TFTs with SnO_x, are still insufficient.

In this dissertation, the composition dependent structures and electrical properties of p-type SnO_x thin film prepared by reactive DC magnetron sputtering were comprehensively investigated by varying the process conditions such as oxygen partial pressures (P_o) and post annealing temperatures (T_A). In addition, comparative study about the effect of interface layers on the functionality of the bottom gate SnO_x TFT was conducted. This study will be helpful to provide the useful design concept for high performance p-channel SnO_x-based devices.

The organization of this dissertation is as follows. Chapter 2 gives brief descriptions based on the relevant literatures reviewed. Descriptions about electronic structures of metal oxide semiconductor, p-type metal oxide semiconductor (thermodynamics, crystallography, band structure and defect formation and so on) and thin film transistors (structure, operation mode and characterization) will be concerned. Chapter 3 explains the results of the study about the chemical composition

dependent structures and electronic properties of p-type SnO_x thin films and TFTs. In addition, complementary oxide semiconductor using p-type SnO_x and n-type Zn-Sn-O will be demonstrated. Chapter 4 explains the result of the investigations about the effect of various interface layers on the electrical functionalities of SnO_x TFTs.

Chapter 2. Literature Review

2.1 Oxide semiconductor : electronic structure and carrier transport mechanism

The electronic structure in amorphous oxide semiconductors is quite different from that in Si-based semiconductors. The properties of amorphous silicon are usually inferior to single crystalline silicon. For example, the mobility of a-Si:H is less than 2 $cm^2V^{-1}s^{-1}$ while that of c-Si is ~ 1500 $cm^2V^{-1}s^{-1}$. In silicon, the conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding ($sp3\sigma^*$) and bonding ($sp3\sigma$) states of Si hybridized orbitals, and its band gap is formed by the energy splitting of the σ^*-σ level [Fig. 2.1(a)] [30]. On the other hands, the amorphous oxide semiconductors have strong ionic property and charge transfer occurs from heavy metal ion to oxygen atoms [Fig. 2.1(b)]. When a metal ions and oxygen ions comes close, charge transfer occurs due to largely different electron affinity. This can be explained by the Madelung potential. The Madelung potential which is the difference of negative electrostatic potential of the cations and the positive electrostatic potential of the anions stabilizes the ionized states. Therefore, the conduction band minimum (CBM) is comprised of unoccupied the s orbitals of cations and the valence band maximum (VBM) is occupied O 2p orbitals shown by Fig. 2.1(c). The CBM consists of spherically spread s orbitals of the heavy metal

cations and their overlaps with the neighboring metal s orbitals are not affected largely by the disordered local structure [1]. As a result of this, the electron transport is not influenced and the amorphous oxide semiconductor has higher mobility than amorphous Si. Figure 2.2 shows the schematic orbital drawing for carrier transport path for Si-based and metal oxide semiconductors. In the amorphous structure, the strained chemical bonds of sp3 or p orbitals form deep and high density of localized states beneath CBM and above VBM [Fig. 2.2(a)]. Therefore, these localized states hinder the transport of electron hopping and resulted in lower device performance than c-Si semiconductor. On the other hands, in metal oxide semiconductor, large sized s-orbital of metal ion are overlapped directly between an adjacent atoms leading the current path of electron carrier as shown Fig. 2.2(b).

Nomura et al. found that the hall mobility (μ_e) increases with increasing carrier density (N_e) for all the IGZO films including crystalline film [4, 31]. This trend is opposite to that of simple crystalline semiconductors which exhibit the decrease of μ_e due to impurity scattering. Figure 2.3 shows the temperature dependence of hall mobility and carrier density in a-IGZO film. The mobility shows thermally activated behavior at $10^{17} < N_e$ while carrier concentration does not. In addition, $T^{-1/4}$ temperature dependence of the conductivity was reported and a percolation model is employed for electron transport in IGZO. According to this model, the distribution of potential barriers is existed around the conduction band edge due to ta random distribution of Ga^{+3} and Zn^{+2} ions in amorphous semiconductors as shown Fig. 2.4.

When the Fermi level is below the threshold energy, electron conduction is dominated by the percolation mechanism leading the flow of the electrons through the percolation path between potential energy barriers as shown in Fig. 2.4. Therefore, $T^{-1/4}$ temperature dependence of the conductivity can be observed. On the order hands, as the Fermi level is raised above the threshold energy, the carrier density is already degenerated and the electron transport is dominated by degenerated conduction.

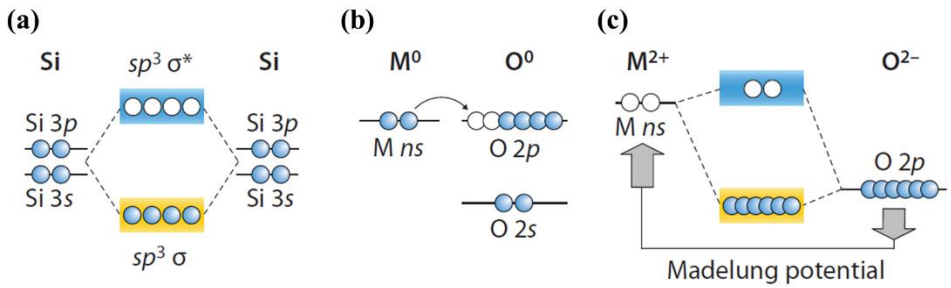

Figure 2.1. Schematic electronic structures of silicon and ionic oxide semiconductors. Bandgap formation mechanisms in (a) covalent and (b, c) ionic semiconductors [30].

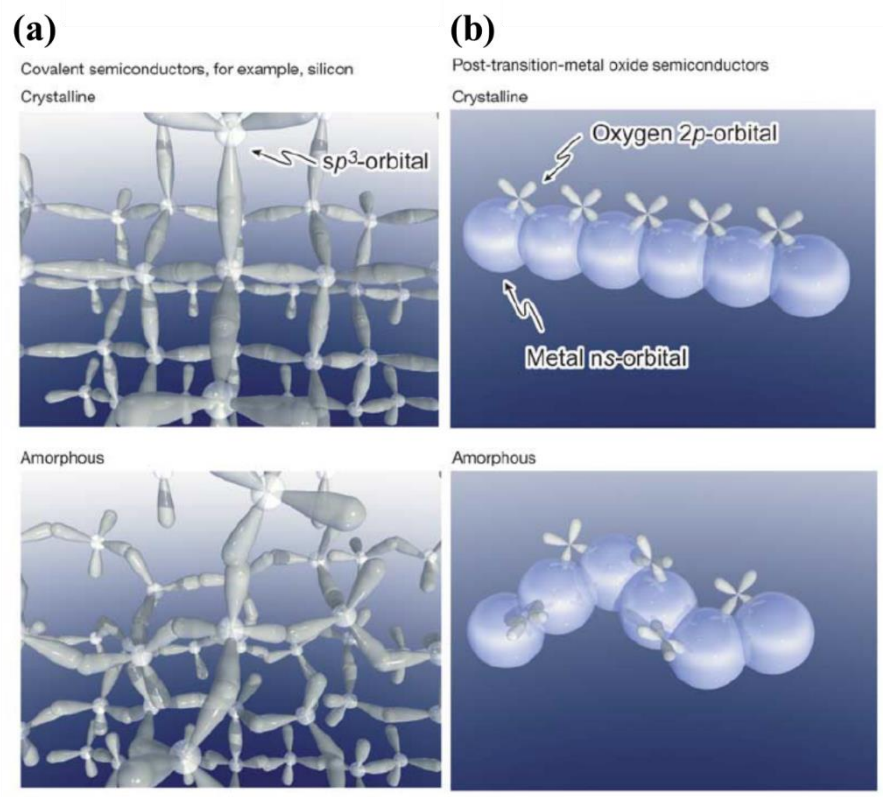

Figure 2.2. Schematic orbital structure of the conduction-band minimum in Si and in an ionic oxide semiconductor [1].

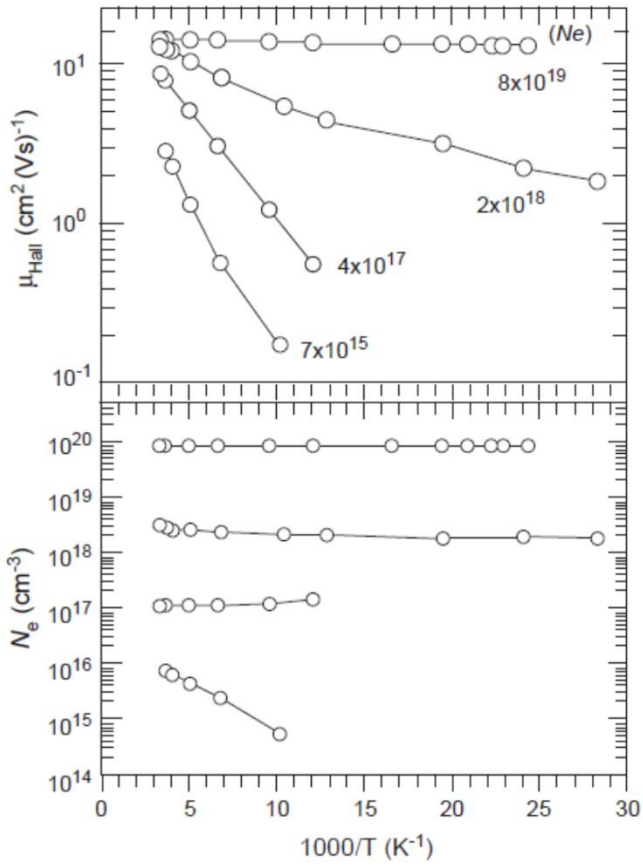

Figure 2.3. Temperature dependences of Hall mobility (μ_{Hall}) and carrier concentration (N_e) for a-IGZO [4].

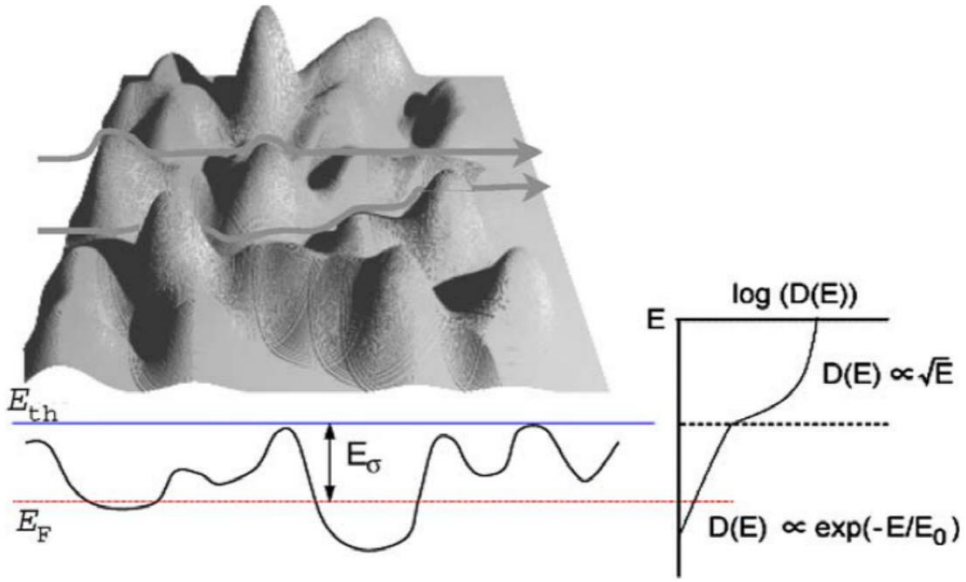

Figure 2.4. Schematic illustration of conduction and electronic structure around conduction band edge. An arrow is an electron conduction path. Potential distribution cross-section (left bottom). E_{th} and E_F denote threshold energy at above which carrier moves freely and Fermi level, respectively. Density of state (right) [32].

2.2 The p-type tin oxide

2.2.1 The overoview of p-type oxide semiconductors

As fore-mentioned in previous chapter, most of the oxide semiconductors have valence band maximum (VBM) which is mainly composed of localized O 2p orbitals, so that the band is very flat and hole effective masses are very large [33, 34].

To date, extensive materials have been studied to adjust p-type semiconductor applications and most of those studies are focused on monovalent Cu based oxide materials, such as $CuAlO_2$, $SrCu_2O_2$, Cu_2O, LaCuOS and so on. These materials have Cu 3d orbitals, which have similar energy level with O 2p orbitals and form hybridized orbitals with O 2p, and show low hole effective mass and good p-type conductivity [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. Especially, Cu_2O shows p-type conductivity with high hole mobility over 100 $cm^2V^{-1}s^{-1}$ [13]. However, TFTs with these Cu based oxides show poor performances with field effect mobility of ~1 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ of ~10^2 due to too high hole concentration or the high tail states and surface densities at the channel ~ insulator interface [10, 11, 12, 13, 17].

Another approach for good p-type properties is using materials, such as Bi_2O_3, PbO, and SnO. They have metal cations such as Bi^{3+}, Pb^{2+} and Sn^{2+} which have pseudo-closed ns^2 orbitals having energy level closed to O 2p orbitals [18, 19, 20,

21]. However Bi_2O_3 exhibit too low hole mobility and PbO does not show p-type conductivity [35]. Among them, SnO is a promising candidate of p-type oxide semiconductors for TFTs applications [18, 22]. Sn 5s and O 2p orbitals of SnO compose hybridized orbitals which reduce localization of valence band edge, so that SnO have effective hole transport path and show high hole mobility [23, 24]. TFTs based on p-type SnO are expected to fulfil these requirements due to the particular nature of band structure [24].

2.2.2 Thermodynamics of tin oxide

Stannic oxide (SnO_2) and stannous oxide (SnO) are two well known forms of tin oxide, which is attributed by dual valency of oxidation states: 2+ and 4+. Non-stoichiometric stannic oxide is an intrinsic n-type semiconductor in which structural defects, such as the oxygen vacancies and tin interstitials, generate free electrons raising the Fermi level close to the conduction band [3]. Stannous oxide is in contrast, much less characterized than stannic oxide, as well as the less abundant form of tin oxide. However, stannous oxide, as an intrinsic p-type semiconductor, has attracted attention for applications for a transparent oxide semiconductor.

Generally, SnO is known as to be hard to be prepared. To gain further insight about this, Sn–O phase diagram for atmospheric pressure is depicted in Fig. 2.5 [36]. SnO is observed in the phase diagram at temperatures below 543 ± 20 K. There are intermediate tin-oxide phases between SnO and SnO_2 at elevated temperature such as Sn_3O_4 and Sn_2O_3. In these intermediate oxides Sn is present as a mixture of Sn (2+) and Sn (4+) [37, 38, 39].

Heat of formation of SnO at 298 K is ΔH= -68 cal / mol compared to the ΔH = -138 cal / mol of SnO_2 [40], thus following reaction occurs:

$$SnO + \frac{1}{2}O_2 \rightarrow SnO_2 \qquad (2.1)$$

The study of the oxidation of SnO films to SnO_2 by Raman scattering, IR reflectivity and X-ray diffraction shows that the oxidation starts with an internal

disproportionation via the intermediate oxide phases such as Sn_3O_4 and Sn_2O_3 before external oxygen completes the oxidation to SnO_2 [41].

$$x\ \ \mathrm{SnO} \rightarrow \quad Sn_xO_y + (x-1)\ \ Sn \qquad (2.2)$$

This indicates that stannic oxide is the thermodynamically most stable form of tin oxide.

$$Sn_xO_y + (x-1)\ \ Sn + \ \ O_2 \rightarrow SnO_2 \quad (2.3)$$

Especially, (001)-textured SnO layers convert into (101)-textured SnO_2 films. This is attributed by the by the structural similarities between the tin matrix of the SnO (001) plane and that of the SnO_2 (101) plane. Because of this structural similarity essentially only the incorporation of an additional oxygen layer is required to obtain the final SnO_2 structure [41, 42] (see Fig. 2.6).

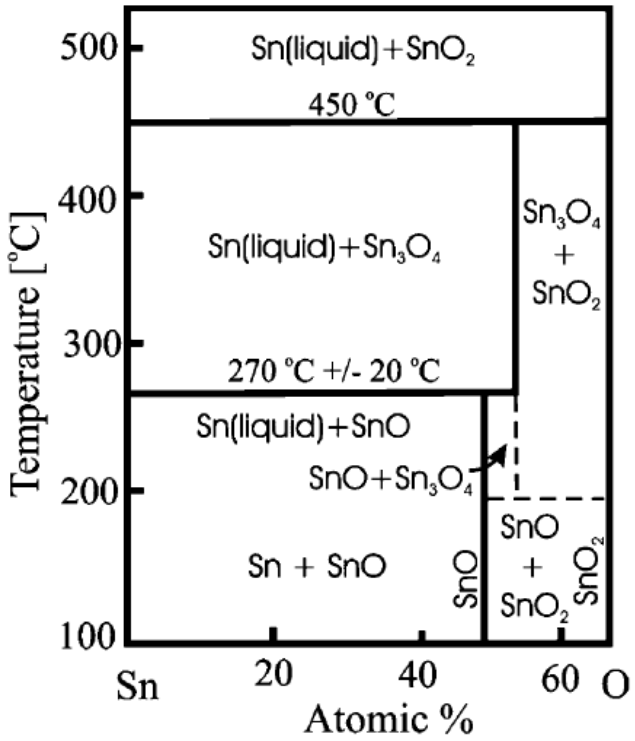

Figure 2.5. The Sn – O phase diagram [36].

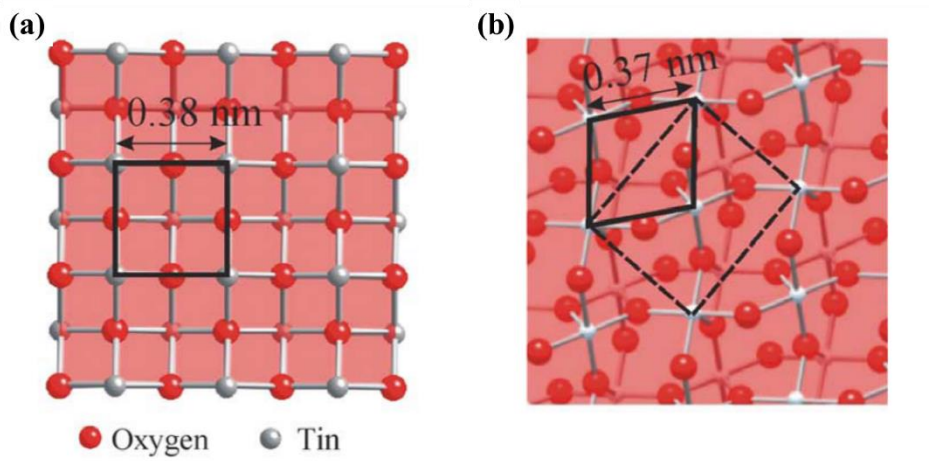

Figure 2.6. Comparison of the structure of the (a) SnO (001) and (b) SnO_2 (101) surfaces [43].

2.2.3 Crystal structure

Stannous oxide (SnO) has a tetragonal unit cell with the litharge structure (P4/nmm), isostructural to PbO [See Fig. 2.7(a), (b)]. The lattice constants are a = b = 3.7960 Å and c = 4.816 Å [43, 44]. Each Sn and O atom is fourfold coordinated with a bond length of 2.23 Å. The structure is layered in the [001] crystallographic direction with a $Sn_{1/2}$–O–$Sn_{1/2}$ sequence and a van-der-Waals gap between two adjacent Sn planes of 2.52 Å. The electron charge clouds between the Sn planes screen the positive charge of the Sn^{2+} ions, so that the Coulombic repulsion between adjacent Sn layers can be reduced [45, 46, 47]. These charge clouds are generated from Sn 5s electrons which do not participate in the bonding and so that they are known as lone pairs [48] [See Fig. 2.7(c)].

Compared to stannous oxide (SnO), stannic oxide (SnO_2) has the rutile structure with tetragonal unit cell (P42/mnm). The lattice constants are a = b = 4.7374 Å and c = 3.1864 Å. All Sn and oxygen atoms are six-fold and three-fold coordinated, respectively [49] [See Fig. 2.7(d), (e)].

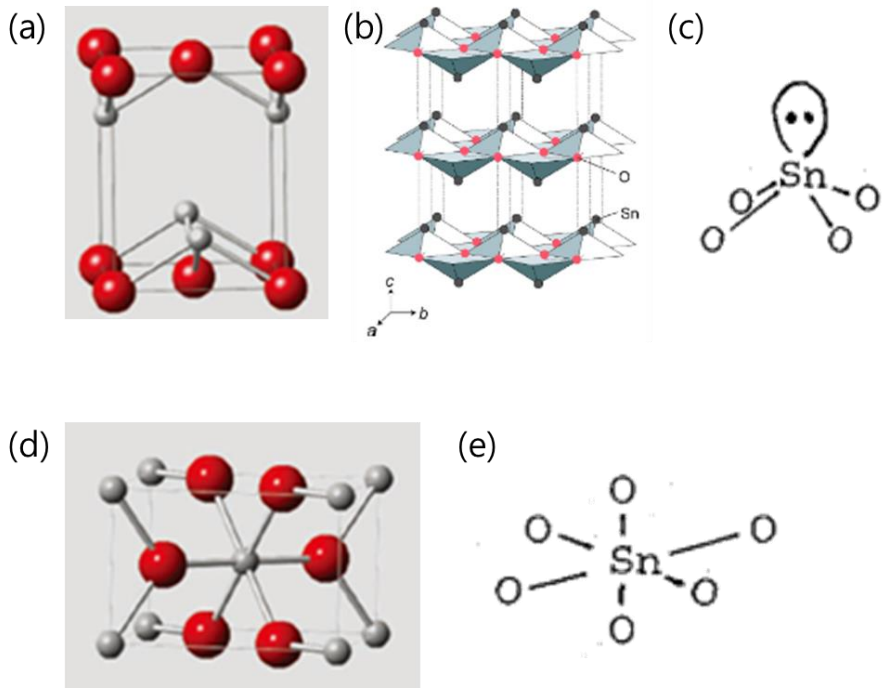

Figure 2.7. Comparison of the crystal structure of stannous oxide (a-c) and stannic oxide (d-e) [3, 50] .

2.2.4 Band structure

Metal oxide semiconductors (MOSs) have the conduction band (CB), which typically contains a conduction path generated by delocalized s-orbitals of metal ions, while the valence band maximum (VBM), as a conduction path of holes, is mainly composed of localized p-orbitals of oxygen ions. Due to the characteristics of MOSs, injected electrons in these thin films are easily transferred along the conducting path and show good mobility regardless of structure ordering, in comparison to holes. Nevertheless, p-type MOSs have been persistently studied because they are necessary to fabricate inverters and/or logic circuits for low power consumption and transparent device applications, etc [3].

The electronic structure of stannous oxide is different from typical n-type oxide semiconductors. Figure 2.8 shows calculated band structure of stannous oxide [50]. According to this result, stannous oxide has an indirect band structure. The VBM is located in between the Γ and M points and the CBM is located at the M point. In the valence band, the energy at the Γ point is very close to the energy of the highest occupied point. The VB region at high energy of stannous oxide has contributions of the Sn 5s, Sn 5p, and O 2p orbitals, but very close to the valence band maximum (VBM), Sn 5s and O 2p have almost equal contributions, slightly dominated by the Sn 5s orbitals [50]. The VB edge localization becomes reduced by almost equal contributions of the Sn 5s and O 2p orbitals at the VBM, so that stannous oxide shows

enhanced hole mobility and finally p-type characteristics [19, 24, 35, 50].

Near the VBM, a large difference in the curvature is observed between the Γ-X, Γ-M, and Γ-Z directions. The effective hole mass in the Z direction near the Γ point is smaller than in the M and X directions, suggesting anisotropic conductivity of p-type SnO. Holes may hop easier via lone pairs in the inter-layer than in the intra-layer region [50].

The simplified band structure of stannous and stannic oxide are compared in Fig. 2.9 [24]. Stannous oxide shows the VBM hybridization which is attributed by the almost equal contributions of Sn 5s and O 2p orbitals. The conduction band minimum (CBM) of stannous oxide is mainly contributed by Sn 5p.

Figure 2.10 shows the estimated band structure of SnO by Ogo et al. [51] from the ultra violet photoelectron spectroscopy (UPS) measurements of SnO_2. They have estimated the ionization potential of SnO to be 5.8eV with an indirect fundamental band gap of 0.7 eV and CBM to be around 2.7 to 2.9 eV above VBM based on the optical determination of the band gap.

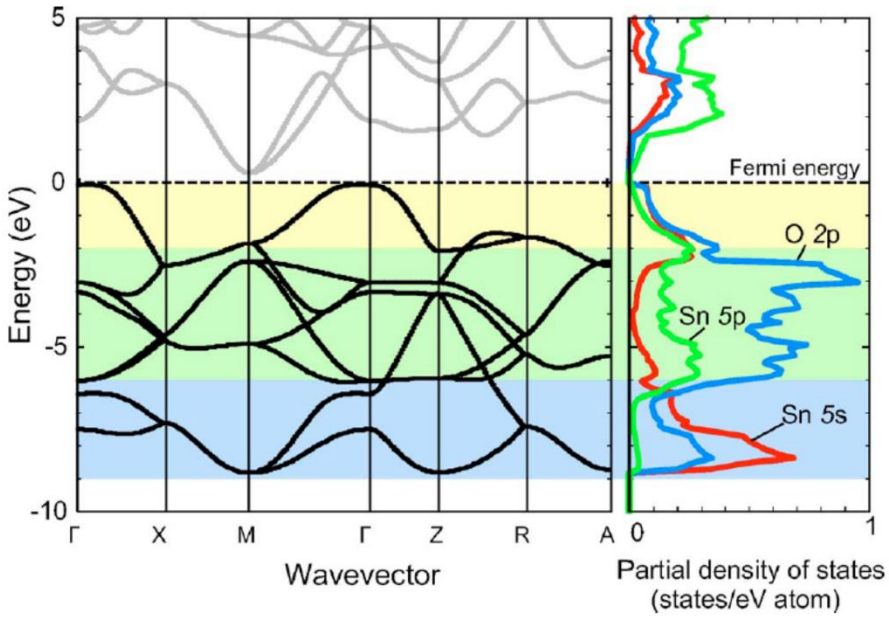

Figure 2.8. Band structure of stannous oxide [50].

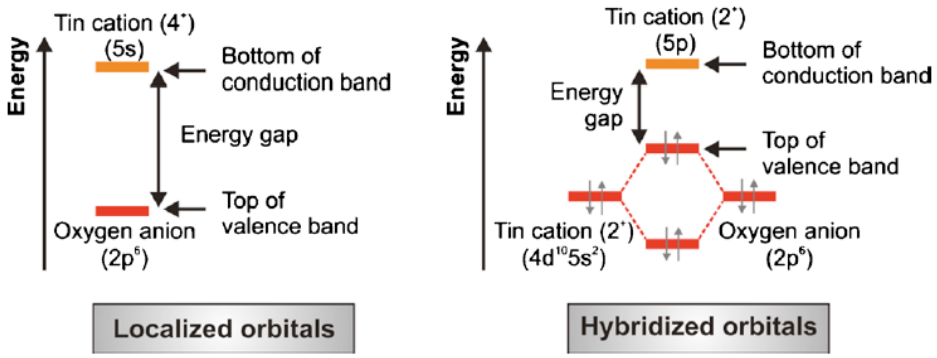

Figure 2.9. Comparison between the band structures of SnO_2 and SnO [24].

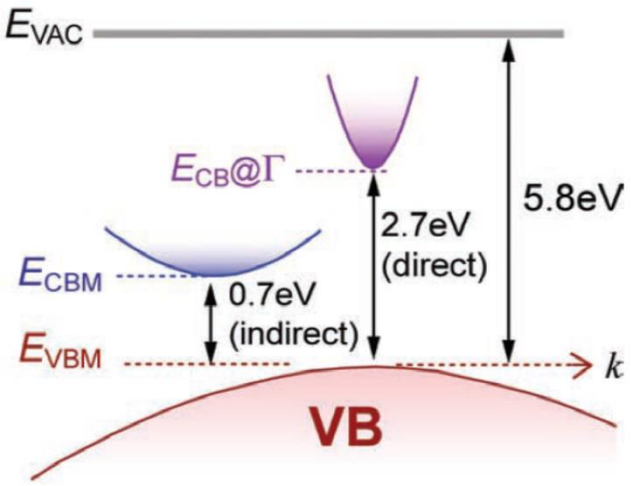

Figure 2.10. Schematic illustration of the band structure of SnO [35, 50, 51].

2.2.5 Native defects in tin monoxide

Figure 2.11 shows the defect formation energies and concentrations of SnO which are reported by Togo et al. from their first principles calculations and the characteristics of native defects in SnO are summarized in Table 2.1 [50]. They suggested that p-type characteristics of SnO is originated from Sn vacancies (V_{Sn}) which are acceptor like defect and have the lowest formation energy among native defects in SnO. They also showed that the donor-like defects Sn interstitial (Sn_i) and oxygen vacancy (V_O) have a only tiny concentration which is insufficient for compensating the holes generated by the V_{Sn} and that the oxygen interstitial (O_i) concentration is comparable to that of the V_{Sn}, but it does not contribute to the conductivity due to it's neutral characteristics [50].

The hole, which is a p-type carrier, can be generated by an ionization of V_{Sn} and the formation of hole can be understood with following reaction (Kröger-Vink notation) regardless of the participating of V_O [52]:

$$SnO \leftrightarrow Sn_{Sn}^{x} + O_O^{x} + V_{Sn}^{2-} + 2h^{+} \quad (2.4)$$

$$SnO \leftrightarrow Sn_{Sn}^{x} + O_O^{x} + V_{Sn}^{2-} + O_i^{2-} + V_O^{2+} + 2h^{+} \quad (2.5)$$

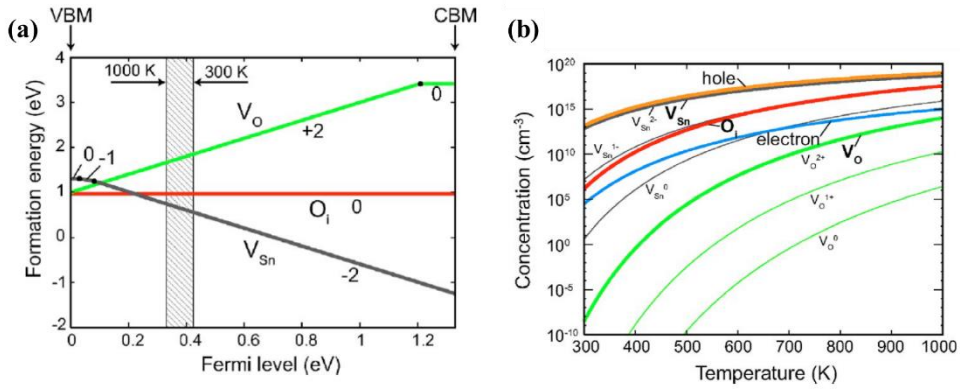

Figure 2.11. Schematic illustration of the band structure of SnO [50].

Table 2.1. Summarized characteristics of native defects in SnO

	$\mathbf{V_{Sn}}$	$\mathbf{O_i}$	$\mathbf{V_O}$	$\mathbf{Sn_i}$
Character-istics	Acceptor like (shallow)	neutral	Donor like (shallow)	Donor or acceptor like (with E_F)
Formation E	lowest	low	high	too high
Concentration	high	Comparable to V_{Sn}	low	-

2.3 Thin film transistors (TFTs)

2.3.1 Device structure

Thin film transistors (TFTs) are basically composed of gate electrode, a dielectric layer, semiconductor layer and source-drain (S/D) electrode. TFTs can be discerned by the position of gate electrode and S/D electrode: top / bottom gate and co-planner / staggered structure. According to these classification, basic four types of structure for TFTs are depicted in Fig. 2.12. In the bottom-gate TFTs structure, the gate electrode is positioned on the substrate. The gate insulator and semiconductor layer are placed sequentially on the gate. In contrast, the top-gate TFTs structure has gate layer on the top of structure and the gate insulator and semiconductor layer are placed beneath the gate layer. In staggered structure, the source-drain are placed on opposite of the semiconductor. On the other hand, the co-planner TFTs structure has the source-drain on the same side of the semiconductor. A staggered structure TFTs with bottom-gate usually have easier processing and enhanced electrical properties especially for a-Si:H TFT device. The bottom gate also plays to screen a light from the back light unit. Because a-Si:H is sensitive to the lights, this configuration is widely used for the fabrication of TFTs with a-Si:H as a channel layer in the display device. In contrast, a coplanar top-gate structure is generally fabricated for poly-Si TFTs. The poly-Si TFTs should be

crystallized using following process at high temperature. The co-planner top-gate configuration can be shield the degradation of device properties resulted from the crystallization process [3].

In this dissertation, the staggered bottom gate TFTs were fabricated.

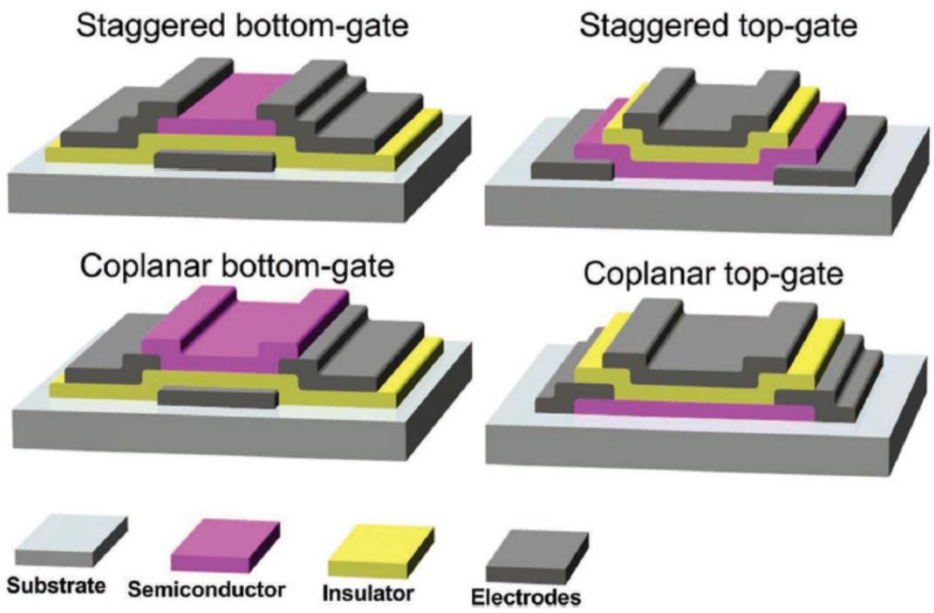

Figure 2.12. Typical device structures for TFTs [3].

2.3.2 Operation of TFTs

The operations of TFTs are able to be described by controlling carrier flow from the source electrode to the drain electrode, which can be modulated with channel conductivity via gate electrode bias voltages. Generally, TFTs can operate in either enhancement mode or depletion mode. When the TFTs operate in enhancement mode, the devices are normally off-state and it needs to apply gate voltage to set the device at on-state (accumulated in carriers). While in depletion mode, the devices are normally on-state and it is necessary to apply gate voltage to set the device to off-state (depleted in carriers) [53].

The ideal energy band diagram of p-channel oxide TFTs are depicted in Fig. 2.13. The energy band diagrams are represented with changes of field via gate voltage and charge carriers at the interface between the channel and insulator layer [52, 54].

1) Equilibrium mode

Figure 2.13(a) shows the device at equilibrium state where the gate voltage is applied at 0 V. When zero gate voltage is applied, the conductivity of the semiconductor is significantly low. There is no flow of charges through the channel layer because of no difference of the Fermi level (E_F) between the semiconductor and metal. However, if the intrinsic Fermi levels of gate and semiconductor are quite different, the internal field between gate and semiconductor exists in equilibrium state,

which can induce either holes to be accumulated or depleted in the semiconductor/insulator interface [53, 54].

2) Depletion mode

When a positive gate bias ($V_{GS} > 0$) is applied [See Fig. 2.13(b)], E_F in the gate electrode is lowered compared to E_F in semiconductor and cause the downward band bending. The concentration of holes decrease and a depletion region is created in the vicinity of semiconductor/insulator interface. This is called the depletion state. As the positive gate bias increases, the energy band of the semiconductor/insulator interface is bent up more and depletion region extend through the whole semiconductor. In the depletion state, the conductivity of channel is very low so that only small current can flow through the channel layer although source-drain voltage (V_{DS}) are applied [53, 54].

3) Accumulation mode

When a negative gate bias ($V_{GS} < 0$) is applied [See Fig. 2.13(c)], E_F in the gate is raised compared to E_F in semiconductor leading the band to be bent upwards. The holes are drawn and accumulated at the semiconductor/insulator so that hole concentration increases and the active channel layer is generated near the semiconductor/insulator interface. This is the accumulation state of the p-type TFTs. If the negative drain to source voltage (V_{DS}) is applied, holes are injected from the

source electrode into the channel and drifted toward drain electrode. Here, the absolute value of current ($|I_{DS}|$) increases linearly with V_{DS} and become saturated after pinch-off occurs [53, 54].

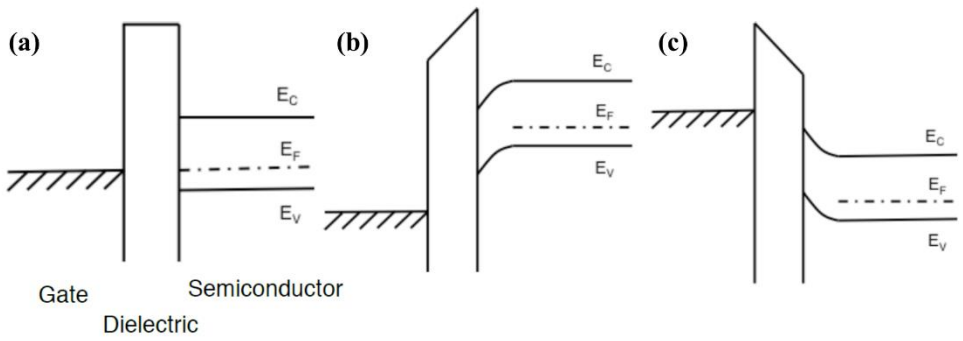

Figure 2.13. Ideal energy band diagrams of p-type TFTs for several gate bias conditions: (a) equilibrium, (b) depletion (V_{GS} > 0 V), and (c) accumulation (V_{GS} < 0 V) [52]

2.3.3 Characteristic parameters

The analysis of TFTs devices are typically characterized by using metal oxide semiconductor field effect transistor (MOSFET) drain current equations. Characteristic parameters of TFTs including drain current (I_{DS}), on/off ratio ($I_{ON/OFF}$), channel mobility (μ), and threshold voltage (V_{th}), subthreshold swing (SS) can be obtained from log I_{DS}-V_{GS} relations.

1) Drain current (I_{DS})

Depending on the applied source/drain voltage (V_{DS}), two different operation regimes can be observed: linear regime and saturation regime [55, 56].

For linear regime ($V_{DS} < V_{GS} - V_{th}$),

$$I_{DS} = C_i \mu_{FE} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (2.6)$$

where C_i, μ_{FE}, W, L are the capacitance of gate insulator per unit area, field-effect mobility, channel width and length, respectively.

For saturation regime ($V_{DS} \geq V_{GS} - V_{th}$),

$$I_{DS} = C_i \mu_{sat} \frac{W}{2L} (V_{GS} - V_{th})^2 \quad (2.7)$$

where μ_{sat} is the saturation mobility.

2) Channel mobility (μ)

Mobility is related to the efficiency of carrier transport in materials, so a key parameter to characterize device performance. The average mobility of carrier transport in a channel layer and affected by several scattering mechanisms, such as lattice vibrations, ionized impurities, grain boundaries and other structural defects [55]. The most common method for determining the channel mobility is MOSFET drain current equations [55, 56] :

effective mobility (μ_{eff}) for low V_{DS} :

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L}(V_{GS} - V_{th})} \tag{2.8}$$

where g_d is conductance expressed as follows:

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}}|_{V_{GS}\ =constant} \tag{2.9}$$

field effect mobility (μ_{FE}) for low V_{DS} :

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_{DS}} \tag{2.10}$$

Where g_m is transconductance expressed as follows:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}\ =constant} \tag{2.11}$$

saturation mobility (μ_{sat}) for high V_{DS} :

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2}{\frac{1}{2} C_i \frac{W}{L}} \tag{2.12}$$

3) Subthreshold swing (SS)

The subthreshold swing, SS are estimated from a log plot of the transfer characteristics. SS is the inverse of the maximum slope in the transfer characteristics. A small value of SS is desirable because it shows how fast TFTs turn on from off state [55, 56].

$$SS = \left(\frac{dlog(I_{DS})}{dV_{GS}}|_{\max\ I_{DS}}\right)^{-1} \qquad (2.13)$$

4) Drain current $I_{ON/OFF}$ ratio

This is a parameter for switching device and defined as the ratio between the highest measured current to the lowest measured current [55, 56].

5) Threshold voltage (V_{th})

Threshold voltage is the V_{GS} where an accumulation layer or conductive channel is formed in the vicinity of semiconductor/gate insulator interface. V_{th} can be extracted via either linear extrapolation of the I_{DS}-V_{GS} curve at low V_{DS} (linear regime) or extrapolation from $I_{DS}^{1/2}$ - V_{GS} plot [55, 56]. Figure 2.14 shows the transfer and output characteristics of p-type oxide TFT [57].

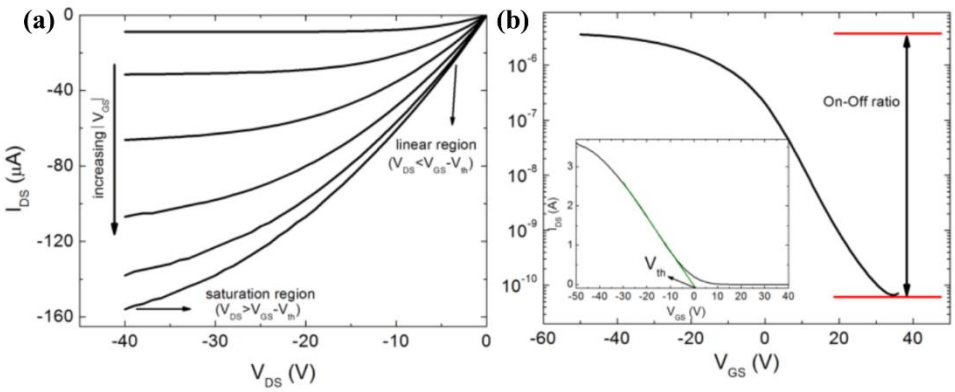

Figure 2.14. Typical (a) output and (b) transfer characteristics of a n-type oxide TFT [57].

Chapter 3. Composition-Dependent Structures and Electrical Properties of p-type SnO_x Thin Film Prepared by Reactive DC Magnetron Sputtering.

3.1 Introduction

Metal oxide semiconductors (MOSs) have received remarkable attention as backplane materials for flat panel displays such as liquid crystal (LC)- and organic light emitting diode (OLED)-based displays due to their cost effective, low-temperature processability and high carrier mobility. Furthermore, in recent years, they have been studied extensively as a promising materials for emerging applications such as flexible and transparent electronics due to their outstanding characteristics, showing high optical transparency and high electrical conductivity [1, 2, 3].

A n-type In-Ga-Zn-O-based semiconductor has already been commercialized as backplane of flat panel display, yielding excellent device performance with electron mobility over 10 $cm^2V^{-1}s^{-1}$ [4]. However, p-type MOSs still need to be improved. The reasons of this discrepancy can be found in band structures of oxide semiconductors. MOSs have the conduction band (CB), which typically contains a conduction path generated by delocalized s-orbitals of metal ions, while the valence band maximum (VBM), as a conduction path of holes, is mainly composed of localized p-orbitals of

oxygen ions. Due to the characteristics of MOSs, injected electrons in these thin films are easily transferred along the conducting path and show good mobility regardless of structure ordering, in comparison to holes. Nevertheless, p-type MOSs have been persistently studied because they are necessary to fabricate inverters and/or logic circuits for low power consumption and transparent device applications, etc [3].

Stannous oxide (SnO) as a p-type MOS has a relatively large optical band gap of 2.7 eV, providing high transmittance of above 80 % in visible light [19, 27]. Recently, it has been reported that in a SnO film delocalized 5s orbitals of Sn^{2+} at the VBM could be controlled to be similar energy level of oxygen (*O*) 2p orbitals, producing high hole mobility in FETs [50]. It is known that Sn has the dual valency of 2+ and 4+ at the oxidation states. As a n-type semiconductor, SnO_2 (Sn^{4+}) has a rutile structure with a tetragonal unit cell: Sn and O atoms have coordination numbers of 6 and 3, respectively. In contrast, SnO (Sn^{2+}) as a p-type MOS has a layered litharge structure with $Sn_{1/2}$-O-$Sn_{1/2}$ sequence in [001] direction, where each Sn and O atom form a tetragonal unit cell with $a = b = 3.7960$ Å, and $c = 4.8160$ Å [43, 44].

Due to the dual valency of Sn, Sn-based oxide films sputtered under an oxygen pressure contain various phases, i.e., metallic Sn, SnO, and SnO_2. Recently, it has been reported that the oxidized states of Sn in the corresponding thin films drastically affect the ordered structures, yielding discernible electrical properties in TFTs [7, 25, 26, 27, 28, 29]. Accordingly, systematical studies related to the oxidation state-dependent electrical properties of SnO_x films still require to achieve high electrical

device performance.

Here, the chemical compositions and ordered structures of the SnO_x thin films deposited by a reactive DC magnetron sputtering process were systematically controlled varying the oxygen partial pressure during deposition and post thermal treatments. The electrical properties of the corresponding SnO_x thin films in TFTs were investigated with various analysis techniques.

3.2 Experimental

3.2.1 Materials and sample preparation

A thermally-grown 100-nm-thick SiO_2 layer on a highly-doped Si wafer was used as a gate dielectric. SnO_x thin films were deposited on SiO_2/Si substrate by reactive DC magnetron sputtering with a Sn target (3 inch, 99.999%) under a processing pressure of about 5×10^{-3} Torr (0.67 Pa): the target to substrate distance was about 15 cm and 50 W of plasma power was applied. Oxygen partial pressure ($P_o = O_2 / (Ar + O_2)$, %) was varied from 4 to 12 %.

The as-deposited SnO_x thin films were further annealed at various temperatures (T_A) ranging from 150 to 300 ºC, inside an Ar-purged tube furnace (above 5 Torr (666.61 Pa)) for 1 h, in order to minimize external oxygen participation in film formation. Then, 70 nm-thick Pt electrodes as top contact source/drain (*S/D*) electrodes were deposited on patterned SnO_x thin films using e-gun evaporating through a shadow mask (channel width, W = 300 μm and channel length, L = 1000 μm) and *S/D* electrodes, respectively.

3.2.2 Characterization

Thicknesses of all the SnO_x thin films were measured using spectroscopic ellipsometry (SE, ESM-300, J.A. Woollam). Chemical compositions in these SnO_x films were analyzed by X-ray photoelectron spectroscopy (XPS, VG Thermo Scientific, Sigma Probe) with a monochromatic Al K_α source ($\geq$ 15 keV). Synchrotron-based grazing-incidence X-ray diffraction (GIXD) was performed for these SnO_x films on SiO_2/Si substrates at 9A and 6D beamlines of the Pohang Accelerator Laboratory, Korea. Crystalline phases in these SnO_x films were characterized using transmission electron microscopy (TEM, Tecnai F20, FEI). Additionally, the film morphologies were observed using scanning electron microscopy (SEM, Sigma, Carl Zeiss) and atomic force microscopy (AFM, Multimode 8, Bruker).

Resistivity and carrier concentration of the SnO_x thin films were evaluated by four point probe (CMT-SR1000N, Advanced Instrument Technology), and Hall mobility was also measured using (HL 5500PC, Bio-Rad) based on van der Pauw method [58]. Electrical characteristics of the SnO_x TFTs were measured at room temperature using a semiconductor parameter analyzer (HP4155A, Hewlett-Packard).

3.3 Chemical compositions of SnO_x thin films

The chemical composition in the SnO_x films fabricated at various P_o conditions were calculated based on the XPS spectra deconvoluted. To minimize the contribution of the native oxide layers on the topmost SnO_x films, Ar sputtering conducted on all the samples, before XPS analysis. Figure 3.1 shows XPS core level spectra of *Sn* $3d_{5/2}$ and *O* 1s of 15-nm-thick SnO_x films fabricated at different P_o conditions ranging from 4 to 12 %, before and after thermally-annealed at 210 ºC for 1 h. Figure 3.2 and 3.3 show deconvoluted XPS spectra of Sn $3d_{5/2}$ and O 1s, respectively, for the SnO_x thin films prepared at P_o 4, 8 and 12%. Note that all the binding energies of the chemical composition were calibrated from the peak position of *C* 1s at 284.8 eV.

The binding energy states of *Sn* $3d_{5/2}$ core level in XPS spectra were indicated around 484.4, 485.9, and 486.6 eV, originating from oxidized states of Sn with three different oxidation numbers (i.e., Sn^0, Sn^{2+}, and Sn^{4+}, respectively) [59, 60]. First, XPS spectrum of *Sn* $3d_{5/2}$ core level in SnO_x sample prepared at P_o = 4 % indicated large portions of Sn^0 and Sn^{2+}. With increasing in P_o, the as-deposited films contained a lesser portion of Sn^0, which completely disappeared at P_o = 12 %: in this case, the portion of Sn^{4+} state was also indicated (see the red curves around at 486.6 eV in Fig. 3.2). After thermally-annealing at 210 ºC for 1 h, it was found that most of metallic Sn atoms were oxidized to form SnO in the annealed films, as determined by XPS analysis. Additionally, XPS spectra of *O* 1s core level in these SnO_x films showed

discernible oxygen states, depending on P_o and thermal annealing. The binding energies of O-Sn^{2+} and O-Sn^{4+} were assigned as 529.8 and 530.4 eV, respectively [27, 59, 60, 61, 62, 63].

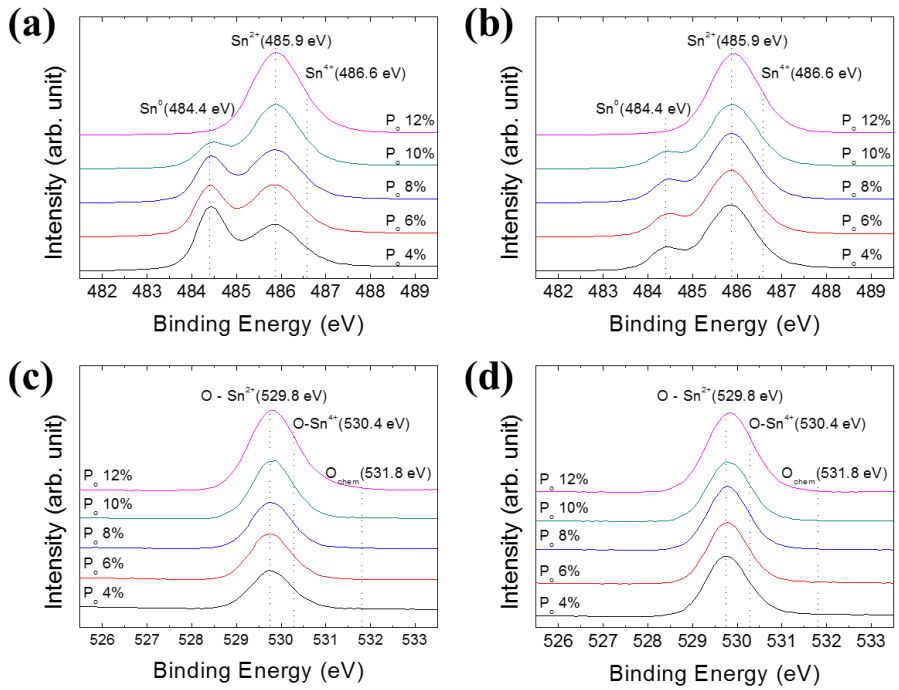

Figure 3.1. XPS spectra of (a, b) *Sn* $3d_{5/2}$ and (c, d) *O* 1s core levels in the 15 nm thick SnO_x thin films deposited on SiO_2 dielectrics at various P_o (4 to 12 %), before (a, c) and after (b, d) thermally annealing at 210 °C for 1 h.

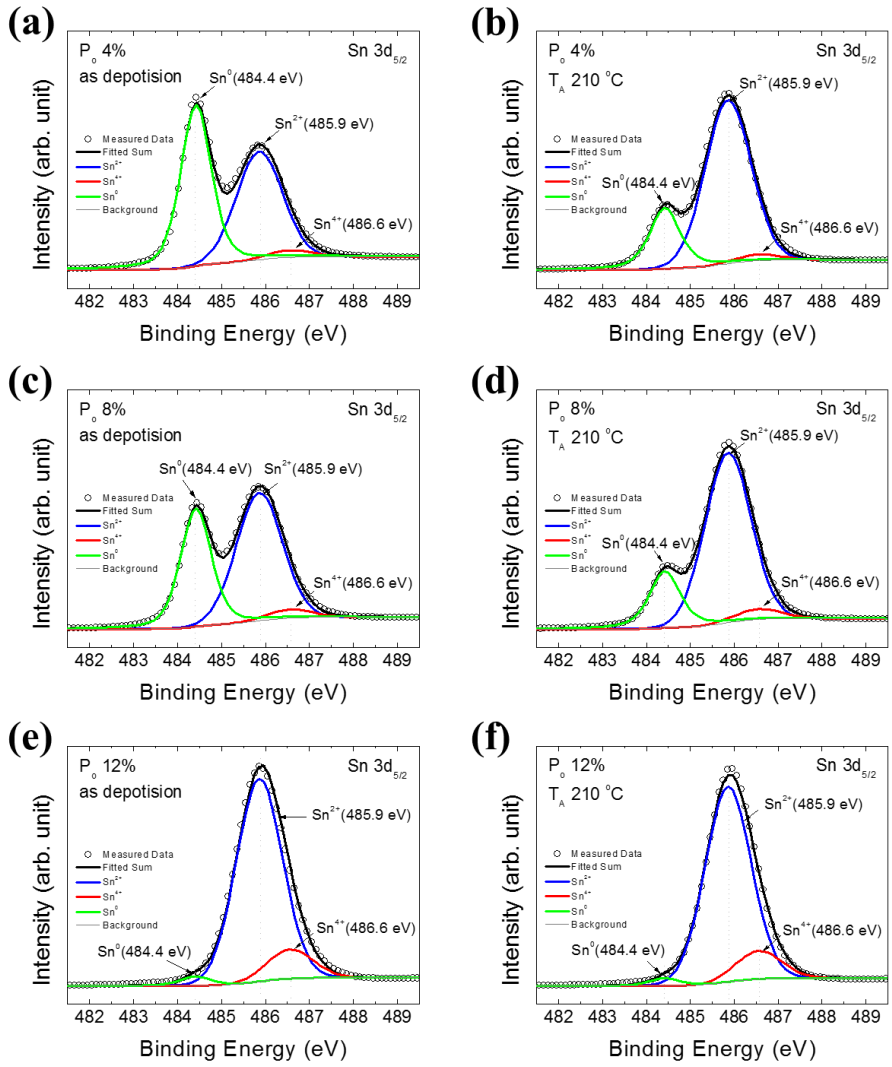

Figure 3.2. Deconvoluted XPS spectra of Sn $3d_{5/2}$ before and after thermally-annealing at 210 ºC for 1h: before annealing (a, c, e), after annealing (b, d, f); P_o = 4 % (a, b), 8 % (c, d) and 12 % (e, f), respectively.

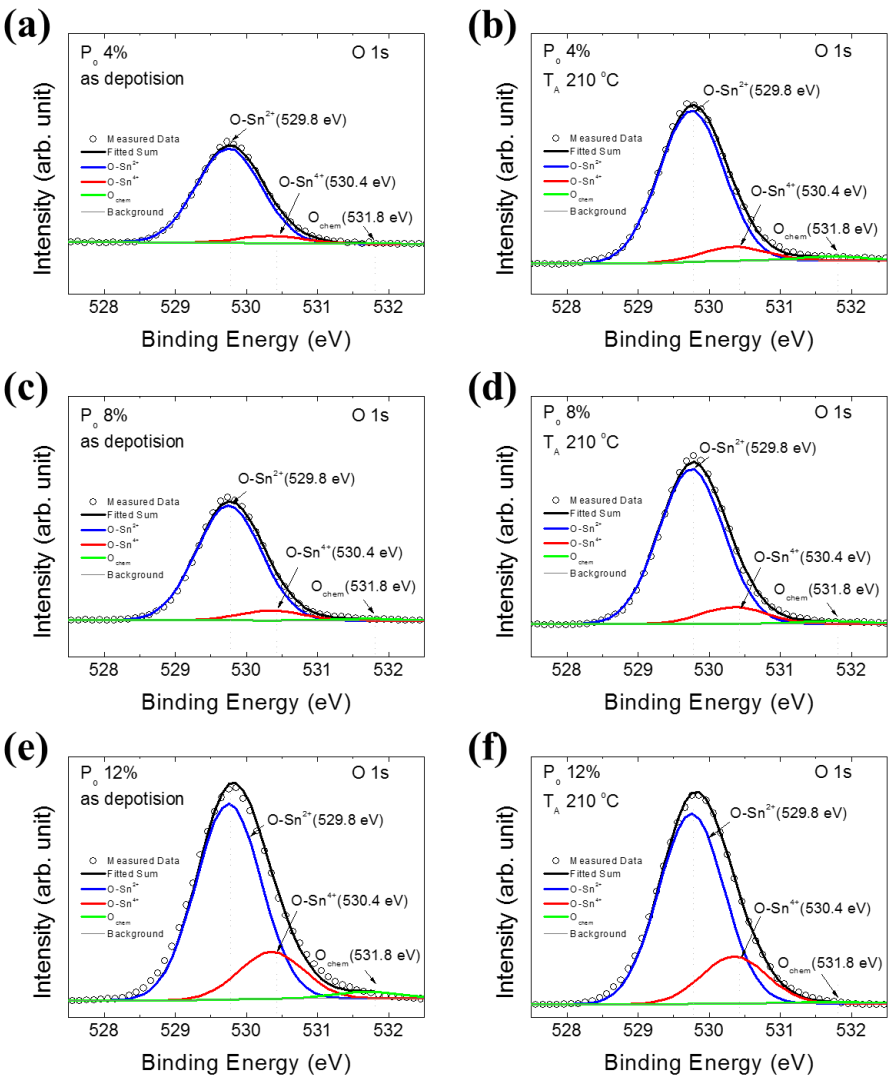

Figure 3.3. Deconvoluted XPS spectra of O 1s before and after thermally-annealing at 210 ^{o}C 1h: before annealing (a, c, e), after annealing (b, d, f); P_o 4 % (a, b), P_o 8% (c, d), P_o 12 % (e, f), respectively.

The chemical compositions of SnO_x thin films were calculated from the deconvoluted XPS spectra. Figure 3.4 represents variations in the oxygen content and oxidized Sn states (Sn^0, Sn^{2+}, Sn^{4+}) in the SnO_x films fabricated at different P_o conditions, before and after annealing at 210 ^oC for 1 h. These variations are also summarized in Table 3.1. The oxygen content in as-deposited SnO_x thin films increased monotonically from 24.3 to 43.5 % with increasing P_o from 4 to 12 %. As the portions of Sn^0 decreased from 52.2 to 3.3 % with an increase in P_o, the portions of Sn^{2+} and Sn^{4+} increased from 45.0 to 84.7 % and 2.8 to 12.1 %, respectively. During annealing, the metallic Sn atoms in the as-deposited films seemed to be mostly oxidized to Sn^{2+}, instead of Sn^{4+}, as determined by the XPS analysis [see Fig. 4.3.4(b)]: the composition of Sn^{4+} in the SnO_x films was almost constant before and after annealing.

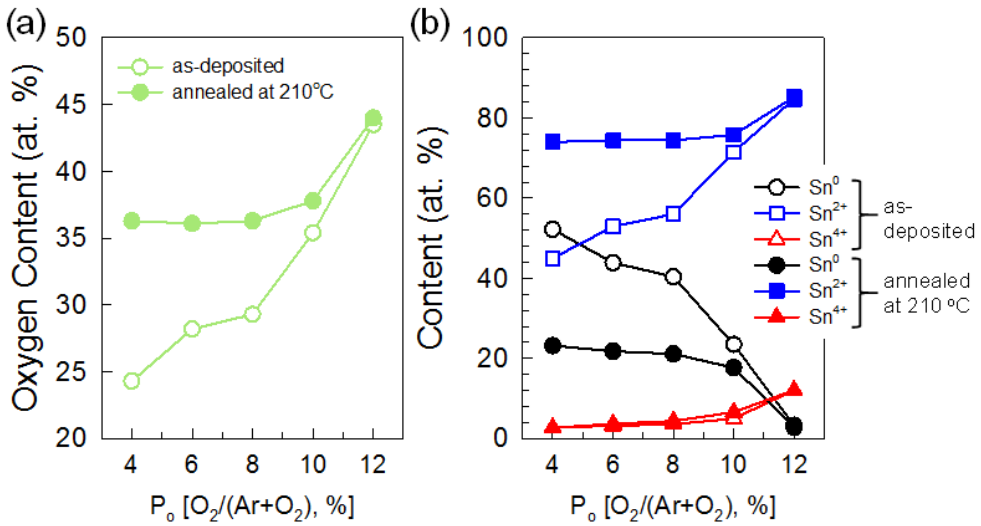

Figure 3.4. Variations of chemical compositions in the SnO_x films fabricated at different P_o conditions before and after annealing at 210 °C for 1 h: (a) Oxygen and (b) Sn^0, Sn^{2+}, and Sn^{4+}.

Table 3.1. Variations in chemical composition of Sn (Sn^0, Sn^{2+}, and Sn^{4+}) and oxygen content in the SnO_x films fabricated at different P_o conditions, before and after annealing at 210 °C for 1 h.

P_o (%)	as-deposited (at.%)				210 °C-annealed (at.%)			
	Sn^0	***Sn^{2+}***	***Sn^{4+}***	***O/Sn+O***	***Sn^0***	***Sn^{2+}***	***Sn^{4+}***	***O/Sn+O***
4	52.2	45.0	2.8	24.3	23.2	74.0	2.7	36.3
6	43.9	52.9	3.2	28.2	21.8	74.4	3.7	36.1
8	40.4	56.0	3.6	29.3	21.1	74.4	4.4	36.3
10	23.5	71.5	5.0	35.4	17.7	75.8	6.6	37.8
12	3.3	84.7	12.1	43.5	2.8	85.2	12.1	44.0

3.4 Crystal structure of SnO_x thin films

The ordered structures of these films were characterized by synchrotron-based GIXD and TEM analyses. First, two dimensional (2D) GIXD was performed for 15-nm-thick SnO_x films, which revealed Sn, SnO, and SnO_2 phases with different portions, depending on P_o and thermal annealing. Among the as-deposited SnO_x films, the only 4 and 6 % P_o-processed samples on SiO_2/Si substrates showed the weak X-ray reflections at Q = 2.155, 2.250, 3.048 $Å^{-1}$ [see Fig. 3.5(a) and (b)], originating from (200), (101), and (220) crystal planes in a β-phase of Sn (JCPDS No. 01-086-2264) [64, 65, 66], while the higher P_o-processed films showed only hollow ring at Q = 2.064 $Å^{-1}$ in the 2D GIXD patterns [see Fig. 3.5(c) and (d)], indicating amorphous structure.

After annealing at 210 ^oC for 1 h, the SnO_x films, except for P_o > 10 %, showed intense X-ray reflections in 2D GIXD patterns, indicating ordered phases of metallic or oxidized Sn (see Fig. 3.6). Below P_o = 10 %, intense X-ray reflections in 2D GIXD patterns of the annealed films were corresponded to poly-crystalline SnO (JCPDS No. 01-085-0712), as well as the residue of β-phase Sn (arrow-marked peaks in Fig. 3.6). For the 4 and 6 % P_o-processed samples after annealing, typical X-ray reflections were indicated at Q = 1.297, 2.101, 2.334, and 2.594 $Å^{-1}$, originating from (001), (101), (110), and (002) planes, respectively: a = b = 3.7960 Å, c = 4.8160 Å [44]. These reflections were distributed anisotropically along the Debye rings in the 2D

GIXD patterns, suggesting that the crystalline aggregates of SnO were preferentially oriented with respect to the substrates. Unlikely, the P_o = 8 % annealed sample showed quite discernible orientations of (101), (110), and (200) crystal reflections. However, high oxygen-contained SnO_x films (fabricated at P_o = 10 and 12 %) showed amorphous-like structures even after annealing, suggesting that the existence of the minor SnO_2 phase degraded the crystallization of a SnO matrix (approximately 76 %, determined by XPS analysis). Based on the XPS and GIXD results, it was found that the ordered structures in the SnO_x films decreased with an increase in SnO_2 composition [27].

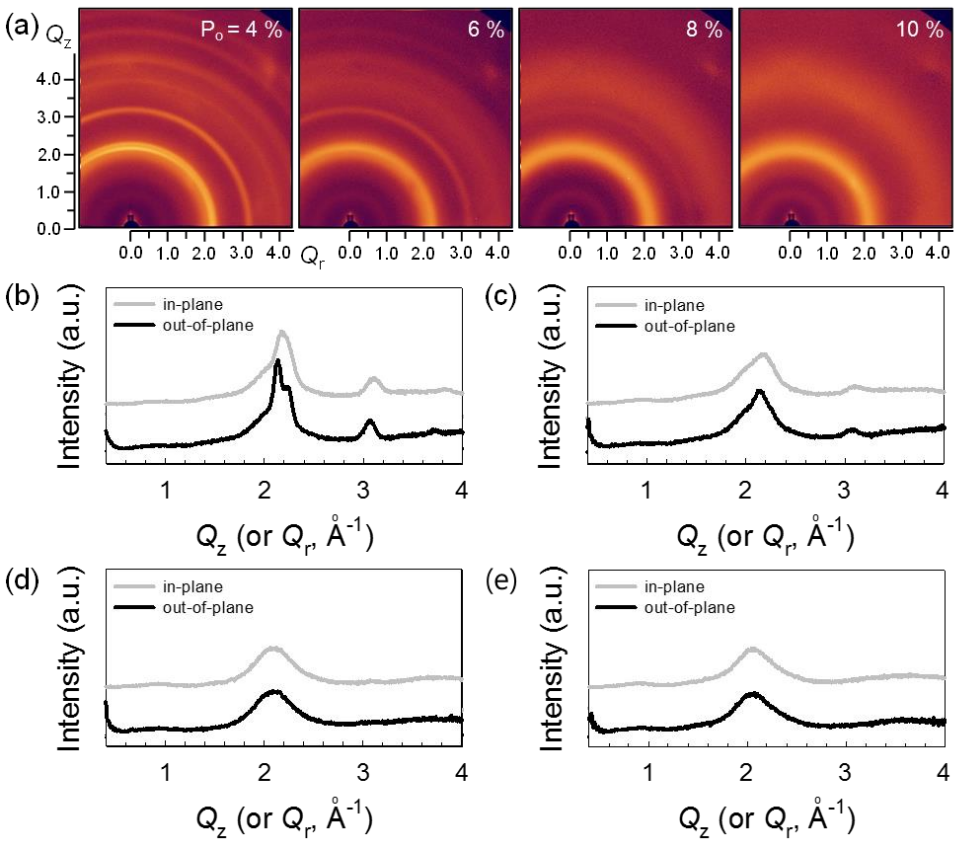

Figure 3.5. (a) The 2D GIXD patterns of the as-deposited SnO_x films fabricated at P_o = 4, 6, 8, and 10 %. (b-e) the 1D in-plane and out-of-plane X-ray profiles extracted from (a): fabricated at P_o = (b) 4, (c) 6, (d) 8 and (e) 10 %.

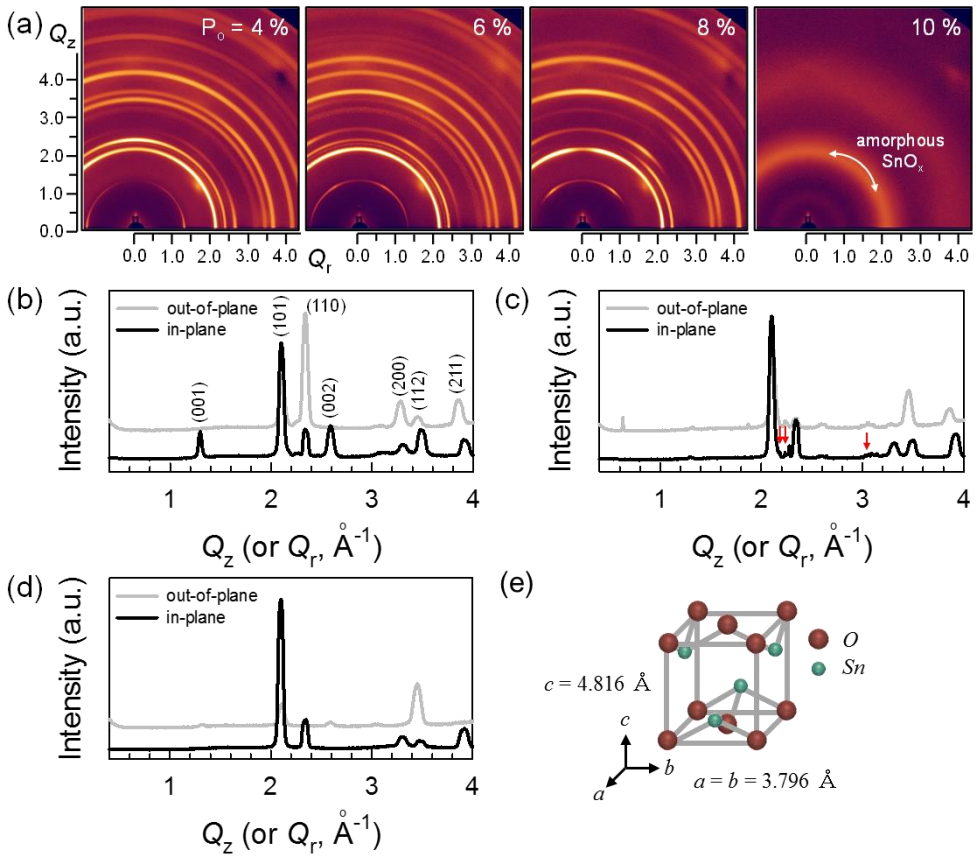

Figure 3.6. (a) The 2D GIXD patterns of the 210 ºC-annealed SnO_x films fabricated at P_o = 4, 6, 8, and 10 %. (b-d) The 1D in-plane and out-of-plane X-ray profiles extracted from (a): fabricated at P_o = (b) 4, (c) 6 and (d) 8 %. (e) The unit cell of the SnO lattice [43, 50]. (Weak X-ray reflections red-arrow marked in (c) correspond to β-phase of Sn).

Figure 3.7 shows in-plane TEM micrographs of 15 nm thick SnO_x thin films fabricated at P_o = 4 and 8 % conditions, respectively, after annealing at 210 °C for 1 h. The 4 % P_o-processed SnO_x film mostly contained SnO aggregates, where (001) and (101) crystal planes were oriented laterally along the film in-plane. Additionally, less-ordered regions with 5 – 10 nm gaps were indicated between the highly oriented crystal grains [see the arrow-marked region in Fig. 3.7(a)]. Unexpectedly, in the 8 % P_o-processed SnO_x film, the orientations of (110) and (101) crystal planes were changed and aligned vertically along the film in-plane. As shown in Fig. 3.7(b), the angle between (110) and (101) planes was indicated as about 64 °, similar to a tetragonal unit cell of SnO: $a = b$ = 3.7960 Å, c = 4.160 Å [44]. The result suggested that in the 8 % P_o-processed film the [001] direction (c-axis) of SnO was tilted with 29.13° with respect to the substrate, which was matched with the 2D GIXD result [see Fig. 3.6(a)]. As a result, the TEM micrographs showed that the SnO_x thin films annealed at 210 °C had different crystal orientations, depending on the supplied P_o during the film fabrication [67].

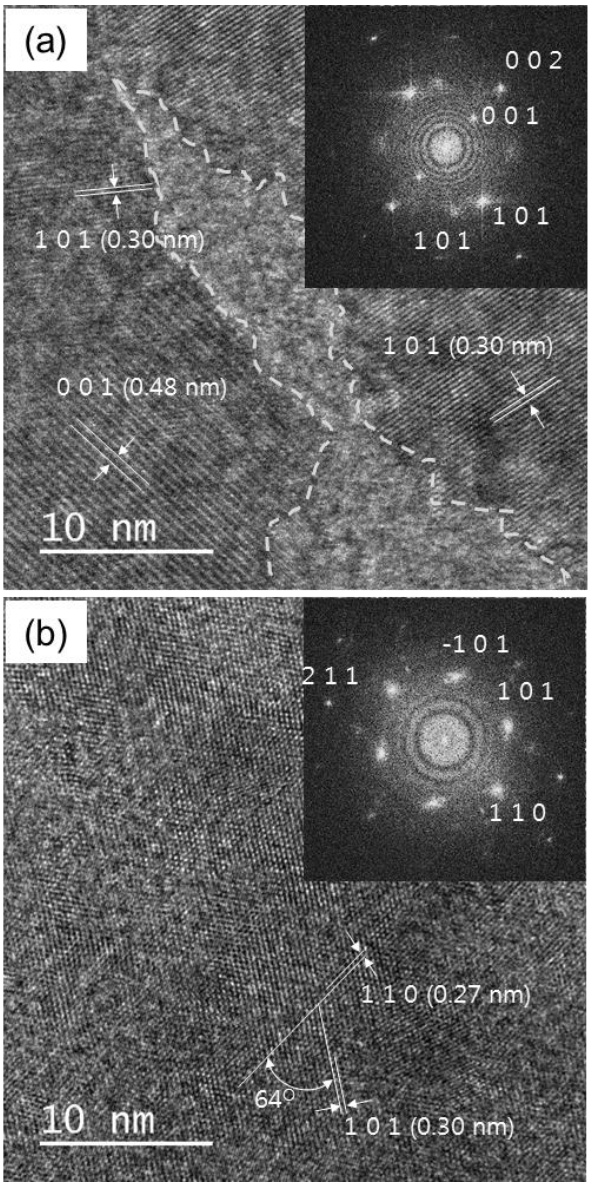

Figure 3.7. High-resolution TEM micrographs (plan-view) of 15-nm-thick SnO_x films fabricated under P_o of (a) 4 and (b) 8%, and both subsequently annealed at 210 ºC for 1 h.

3.5 Surface morphology of SnO_x thin films

Additionally, morphologies of the SnO_x thin films were investigated using SEM and AFM. Figure 3.8 and 3.9 show SEM micrographs of the SnO_x thin films fabricated at different P_o conditions before and after thermal-annealing at 210 ^oC. All the as-deposited films showed very smooth and feature-less morphologies, regardless of P_o (see Fig. 3.8). After annealing, however, these treated films showed discernible morphologies, depending on the processing history, P_o. 4 % P_o-supplied SnO_x film showed minor dendritic and cluster-type phases with a width of approximately 100 nm onto the major nanocluster phase with several tens of nm size. The dendrites and aggregates decreased with increasing P_o, and they were completely disappeared at P_o 10 % (see Fig. 3.9). The clusters were indicated as metallic Sn aggregates, as determined by energy dispersive X-ray spectroscopy (EDS) analysis (see Fig. 3.10).

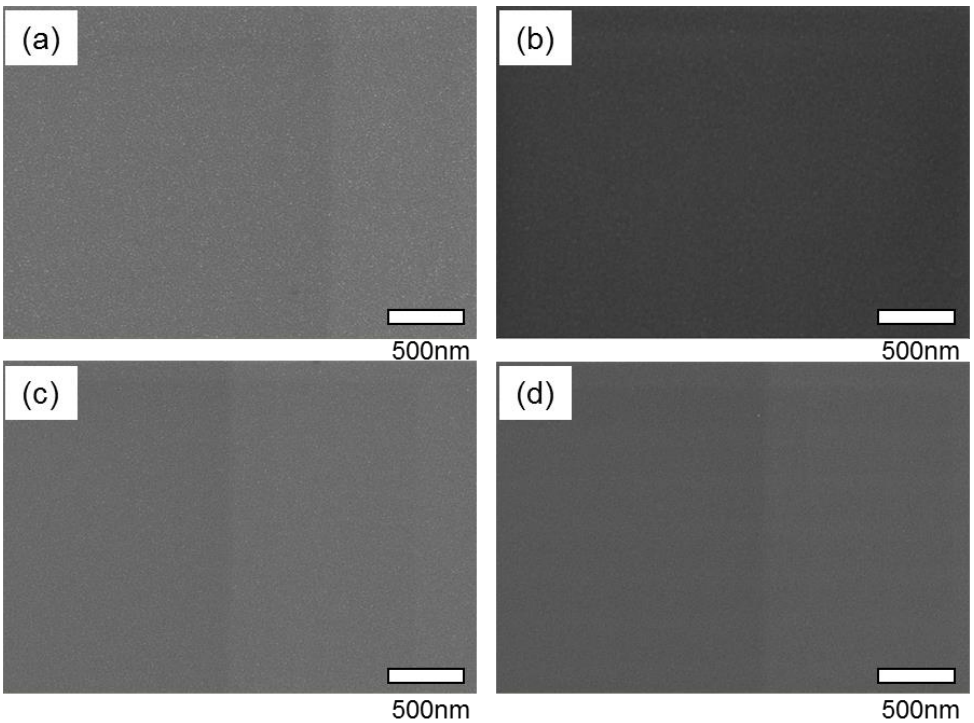

Figure 3.8. SEM images of as-deposited SnO_x thin films (15nm) fabricated with different partial oxygen pressures: P_o = (a) 4, (b) 6, (c) 8 and (d) 10 %.

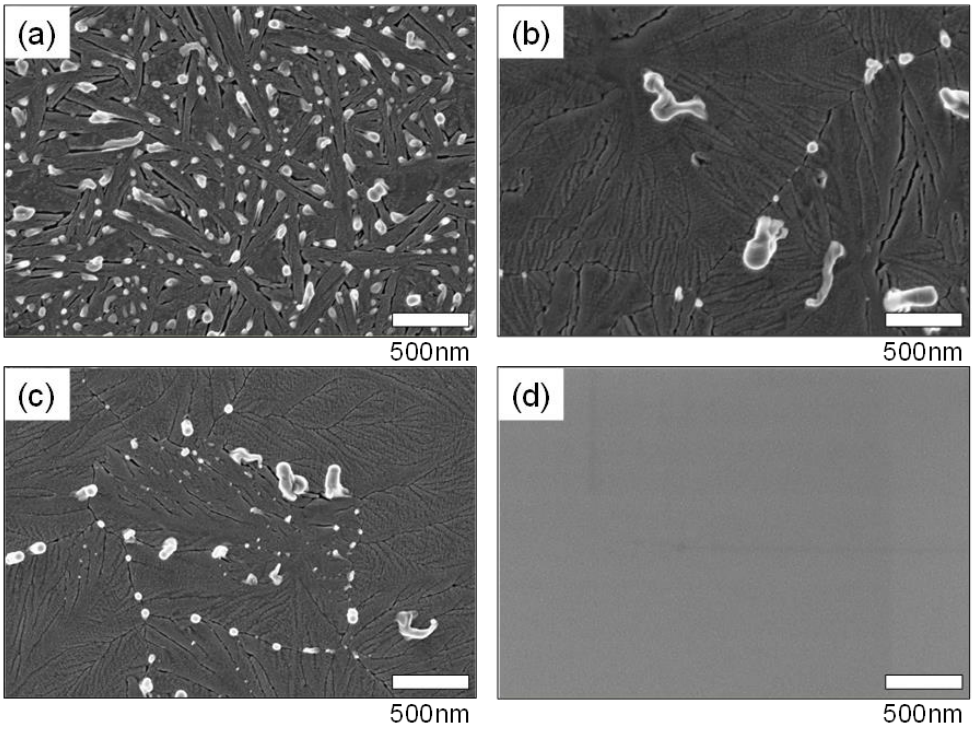

Figure 3.9. SEM images of the 210 oC, 1h annealed SnO_x films (15nm) fabricated with different partial oxygen pressures: P_o = (a) 4, (b) 6, (c) 8 and (d) 10 %.

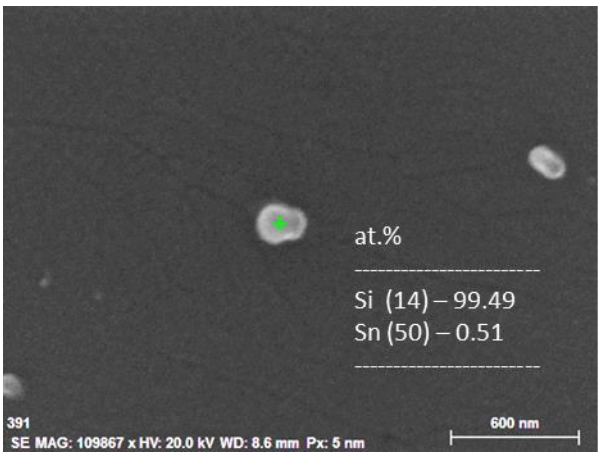

Figure 3.10. Atomic compositions from Energy Dispersive X-ray Spectroscopy (EDS) analysis for the nanocluster phase in SnO_x thin films (15nm) deposited on Si substrate at P_o = 8 % and thermally-annealed at 210 ºC for 1 h.

Numbers of studies have shown that the evolution of dendrite structures are enhanced when crystal growth rate exceeds mass transport rate of ions and molecules those are necessary for crystal growth. This process is Mass transport limited crystal growth (see Fig. 3.11) [68, 69]. Especially, Boggs et al. [70] suggested reasonable mechanisms for the dendritic crystal growth of polycrystalline SnO phase during crystallization of SnO thin films under oxygen deficient condition; The areas adjacent to the crystallized SnO lattices become depleted in oxygen, as the oxygen is captured and consumed to SnO lattices, consequently, further growth of SnO crystals must be directed toward the areas that are richer in oxygen (see Fig. 3.12).

The SnO_x thin films in this work are all deposited deficient in oxygen and thermally annealed also in oxygen deficient ambient, too. Accordingly, the evolution of dendritic structures on the surface of annealed SnO_x thin films in this work, is attributed by the dendritic crystal growth of polycrystalline SnO phase under oxygen deficient environment. In consequence, metallic Sn compositions of the oxygen deficient areas adjacent dendrite structures would become higher and higher and finally exceed their solubility limit. Phase separation from the areas adjacent dendrite structures would evolve and then lead to form metallic Sn clusters. This is well in agreement with gradual appearance of dendrite structures and metallic Sn clusters with increasing P_o from 4 to 8 %: increasing oxygen contents in the films. The reason why thermally-annealed SnO_x film at P_o = 10 % shows uniform surface is that the films have not been crystallized yet.

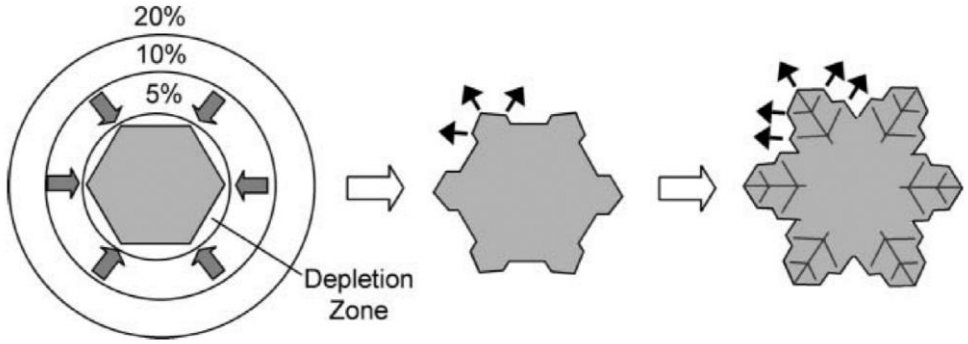

Figure 3.11. Schematic diagram of the mass transport limited crystal growth [68, 69].

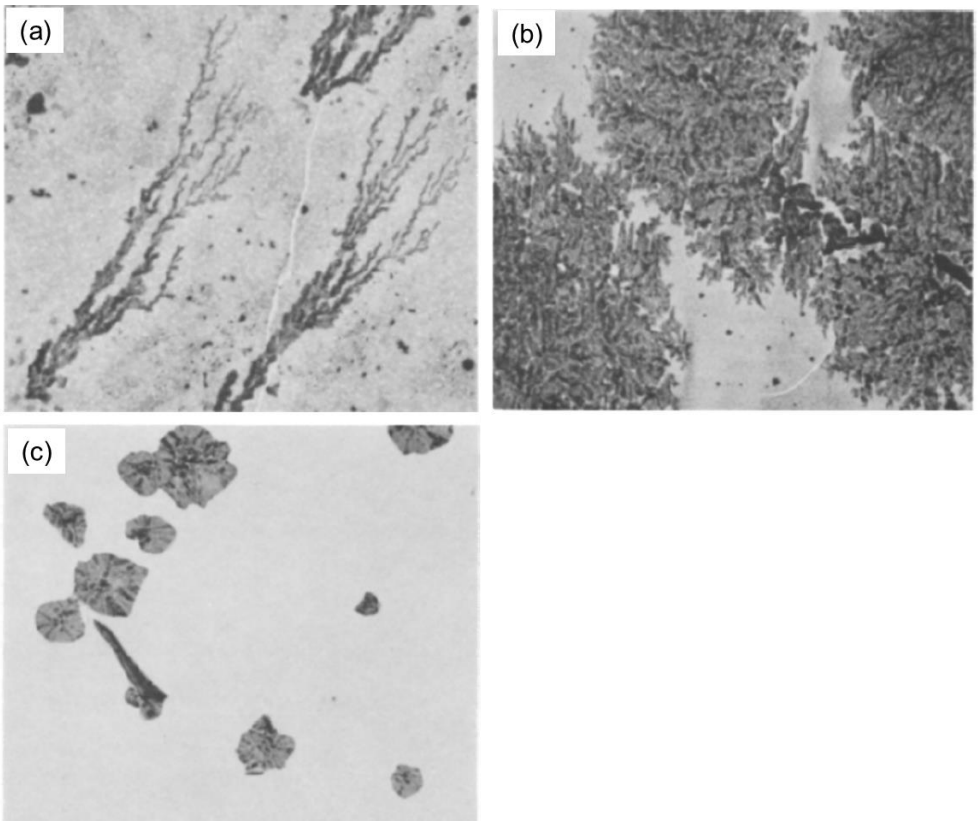

Figure 3.12. Crystal growth of tin oxide layer on the surface of bulk tin which were annealed at 190 ºC in oxygen environment with different pressures: (a) 10^{-4} mmHg (1.33×10^{-2} Pa), (b) 10^{-3} mmHg (1.33×10^{-1} Pa), (c) 10^{-2} mmHg (1.33 Pa) [70].

Figure 3.13 and 3.14 show the detailed AFM topographies of these SnO_x thin films before and after thermally-annealing at 210 ^oC for 1h, respectively. The morphological trend was well matched with that observed by SEM. Root mean square (RMS) surface roughness of as deposited SnO_x thin films deposited at P_o 4, 6, 8 and 10 % is 1.07, 0.82, 0.61, 0.47 nm, respectively, and all the films have very uniform surfaces. After thermally-annealed at 210 ^oC for 1 h, RMS surface roughness is 20.5, 2.1, 1.1, 0.45 nm, respectively: the surface roughness become smaller with increasing P_o.

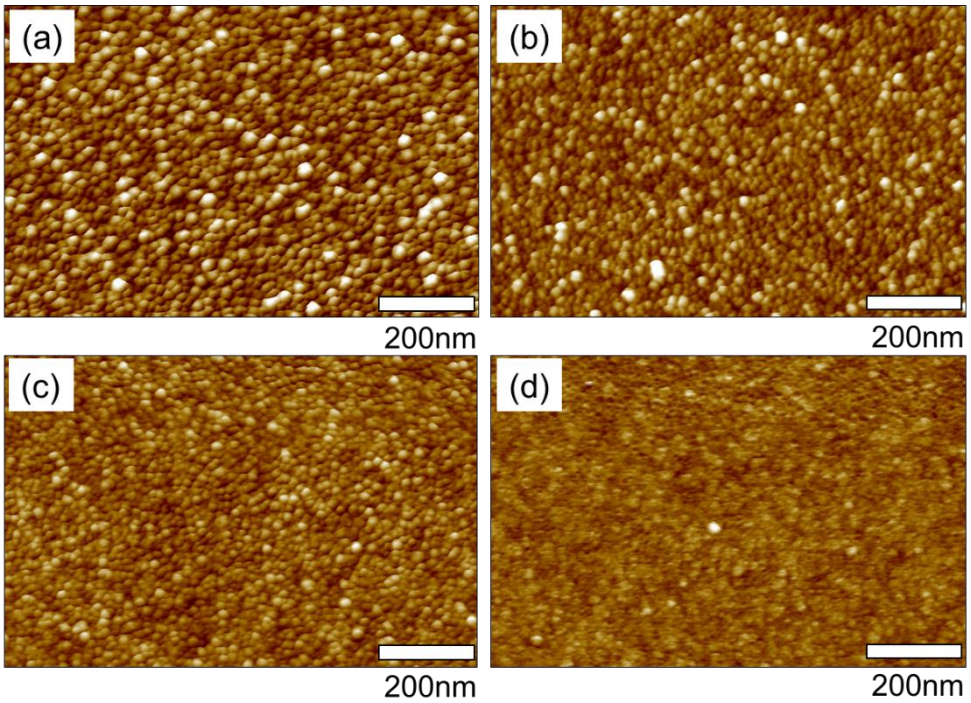

Figure 3.13. AFM topographies of as-deposited SnO_x thin films (15 nm) fabricated with different partial oxygen pressures: P_o = (a) 4, (b) 6, (c) 8 and (d) 10 %.

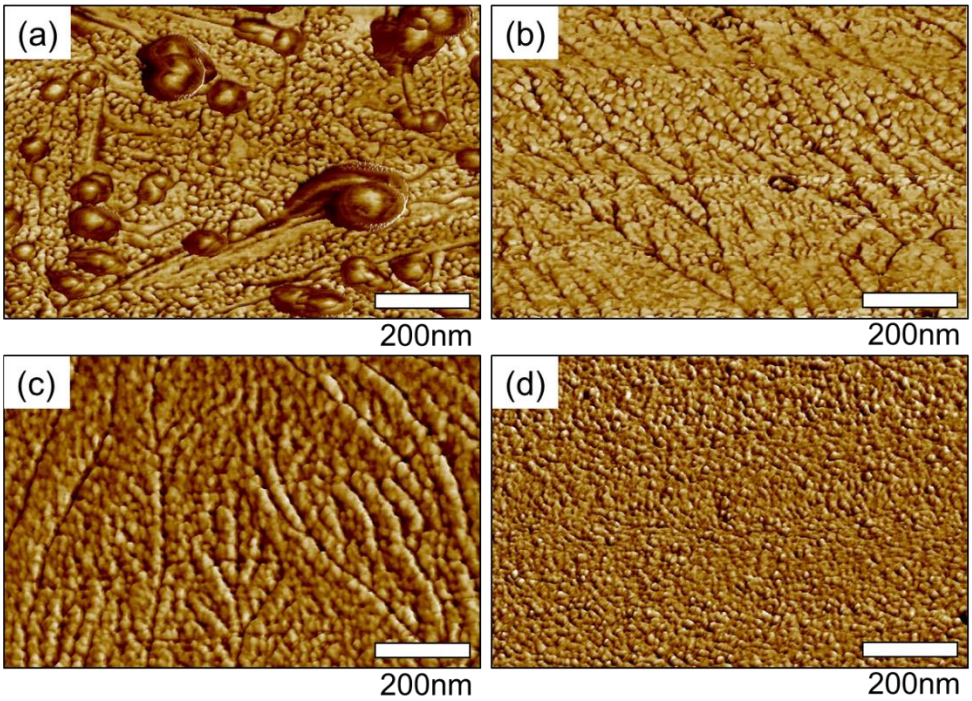

Figure 3.14. AFM topographies of the 210 ºC, 1 h annealed SnO_x thin films (15 nm) fabricated with different partial oxygen pressures: P_o = (a) 4, (b) 6, (c) 8 and (d) 10 %.

3.6 Electrical properties of SnO_x thin films

The electrical properties such as electrical resistivity (ρ), net free carrier concentration and Hall mobility (μ_{Hall}) of the SnO_x thin films were evaluated. Figure 3.15 shows the ρ values of 15-nm-thick SnO_x thin films as a function of the P_o (4 - 12 %) and T_A (165 - 300 ^oC). The ρ value for the as-deposited SnO_x film at the P_o = 4 % was 10^{-1} Ωcm, suggesting the feasibility as a semiconductor. The increasing P_o during the film preparation allowed the resulting SnO_x film to be more resistive. Thus, the as-deposited SnO_x film at the P_o = 10 % showed the increased ρ value of 10^2 Ωcm. In contrast, the SnO_x film at the P_o = 12 % exhibited an insulator-like property where it is difficult to measure the ρ value because of the high contact resistance. The ρ values of the SnO_x films could be tailored by controlling the T_A. The thermal annealing at T_A = 165 °C caused the resistivity of the SnO_x film to increase by 1 - 3 orders of magnitudes compared to those of as-deposited films. When the as-deposited films were annealed at $T_A \geq 210$ °C, the SnO_x films prepared at P_o = 4 - 8 % exhibited the T_A independent ρ values ranging from 10^0 to 10^1 Ωcm. On the other hand, the SnO_x films at $P_o \geq 10$ % showed the insulator-like behaviors. Based on the evolution of chemical states and the crystal structures aforementioned, the increased ρ values with increasing P_o for the as-deposited films is well consistent with the fact that the metallic Sn compositions decreased with increasing P_o. The oxidative deposition would reduce the metal Sn fraction, leading to the enhanced electrical resistance. On

the other hand, the strong T_A-dependent ρ value variations for the SnO_x films at P_o = 4 - 8 % seem to be associated with the microstructure transition from amorphous SnO_x to polycrystalline SnO phase. It is noted that the amorphous phase for the insulator-like SnO_x films at $P_o \geq 10$ % was maintained after the thermal annealing with various T_A.

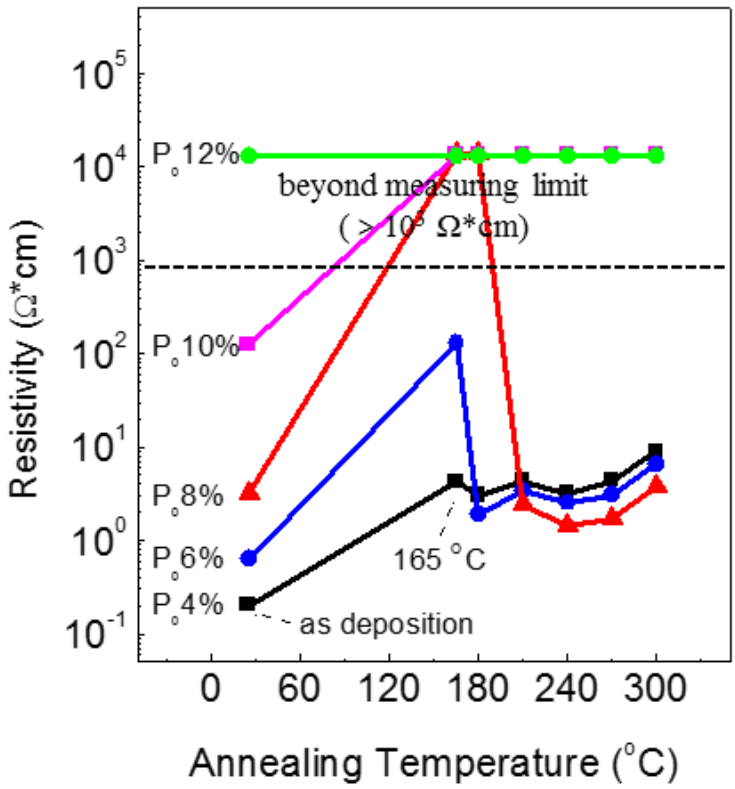

Figure 3.15. The resistivity of SnO_x thin films (15 nm) deposited at various oxygen partial pressure (P_o = 4 - 12 %) before and after thermally-annealed (165 - 300 °C).

The Hall effect measurement was further performed for the semiconducting SnO_x films (T_A = 210 °C) exhibiting the relatively thermal stability. The net carrier concentration and μ_{Hall} values for the SnO_x thin films as a function of P_o are depicted in Fig. 3.16 and summarized in Table 3.2. The dominant carrier conduction for the SnO_x films at P_o = 4 - 8 % was determined to be p-type. The net hole concentration (N_h) for the SnO_x films monotonously decreased from 4.35×10^{18} to 1.81×10^{18} cm^{-3} with increasing P_o. It is understandable that the SnO_2 phase with the n-type conductivity incorporated as a result of increasing P_o can partially compensate the free hole carriers in the overall SnO_x film (see Table 3.1 and 3.2), leading to the reduction in the N_h value [27]. Conversely, the μ_{Hall} values for the SnO_x films increased from 1.1 to 5.5 $cm^2V^{-1}s^{-1}$ with increasing P_o. The crystallographic preferential orientation and topological evolution of the SnO_x film depending on the P_o can be considered as the plausible origin for this μ_{Hall} variation. The electronic structure reported by Togo el al.[50] suggests that the stannous oxide (SnO) has the anisotropic band structure in its Brillouin zone. The curvature of *E-k* diagram in [001] direction (Γ-Z) is larger than those in [100] direction (Γ-X) and [110] direction (Γ-M) near the VBM. It means that the effective hole mass (m^*_h) in [001] direction is the smallest among the various directions (see Fig. 2.8). It predicts that the SnO_x film at P_o = 4 % show the higher mobility than that at P_o = 8 % because the volume fraction of [001] orientation parallel to the in-plane direction is higher substantially for the SnO_x film at P_o = 4% as shown in Fig. 4.4.2 and 4.4.3, which is not the case. In general,

the carrier mobility is proportional to the product of the mean scattering time and inverse effective mass. Therefore, it is inferred that the carrier scattering mechanism plays a critical role in determining the carrier mobility. Indeed, the SnO_x film at P_o = 4 % suffered from the microstructural inhomogeneities such as the metallic Sn aggregate and dendrite structure. These imperfections are likely to act as strong scattering centers, which is responsible for its degraded mobility.

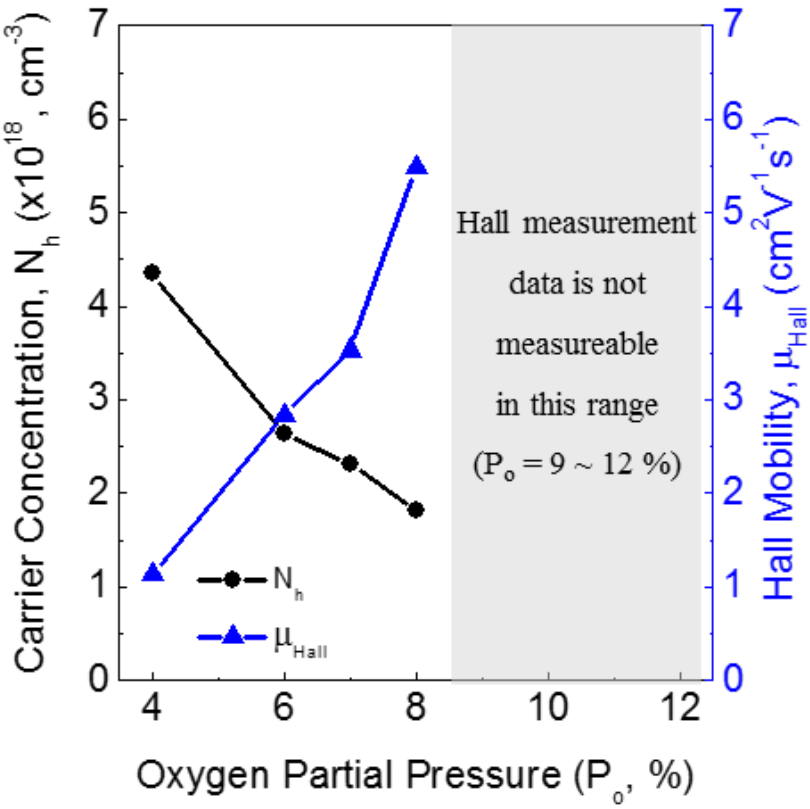

Figure 3.16. The carrier concentration (N_h) and the Hall mobility (μ_{Hall}) of SnO_x thin films annealed at 210 °C from the Hall effect measurement.

Table 3.2. Summary of the carrier concentration (N_h) and the Hall mobility (μ_{Hall}) of SnO_x thin films annealed at 210 °C from the Hall effect measurement.

P_o (%)	N_h (cm^{-3})	μ_{Hall} ($cm^2V^{-1}s^{-1}$)	Note
4	4.35×10^{18}	1.14	p-type
6	2.64×10^{18}	2.84	p-type
8	1.81×10^{18}	5.49	p-type

The Hall effect measurement data of the the SnO_x thin films and TFTs, fabricated the P_o = 10 and 12 %, were not available due to their too high resistivity.

The electrical functionality of these p-type semiconducting SnO_x films was further evaluated in the resulting thin-film transistors (TFTs). Figure 3.17 shows the representative transfer characteristics for the bottom gate SnO_x TFTs with the 15-nm-thick channel at P_o = 4, 6, and 8 %. The field-effect mobility (μ_{FE}) and subthreshold gate swing (*SS*) were calculated using the following equations (2.10) and (2.13), respectively. The maximum bulk trap density ($N_{SS,max}$) and interfacial trap density ($D_{it,max}$) were evaluated from the equation (3.1) where the $N_{SS,max}$ ($D_{it,max}$) value was estimated by setting the $D_{it,max}$ ($N_{SS,max}$) term to be zero.

$$SS = qk_B\ T(N_{SS,max}t_{ch} +\ \ D_{it,max}\ )/[C_{\mathrm{i}}\log(e)] \qquad (3.1)$$

C_i is the capacitance per unit area of the gate dielectric (34.5 nFcm^{-2}), q is the electron charge, k_B is the Boltzmann constant and T is the absolute temperature, and t_{ch} is the channel layer thickness (15 nm) [71]. All the SnO_x TFTs exhibited the p-type conduction irrespective of the P_o values. The SnO_x TFT prepared at P_o = 4 % showed the marginal μ_{FE} of 1.1 cm^{2}V^{-1}s^{-1} and weak current modulation capability of 6.8. The device performance of the SnO_x TFTs was improved by increasing the P_o value. The high μ_{FE} of 2.8 cm^{2}V^{-1}s^{-1} and reasonable $I_{ON/OFF}$ ratio of 1.0 × 10^3 were achieved for the SnO_x TFT at P_o = 8 % as shown in Fig. 3.17 and Table 3.3. These μ_{FE} and $I_{ON/OFF}$ ratio are comparable to or better than the those results reported in the literature for the other p-channel oxide TFTs [6, 51, 71, 72]. This superior performance of the SnO_x

TFT at P_o = 8 % underscores the importance of the homogeneous ordered structure, which is free of the Sn metal aggregate and abrupt dendrite structure. It would be interesting to discuss why the SnO_x TFT at P_o = 4 % suffered from the low $I_{ON/OFF}$ ratio of 6.8. The high off-state I_{DS} indicates the difficulty in the full depletion of the bulk semiconducting SnO_x film. In the other word, the quasi Fermi level (E_F) in the SnO_x film near the gate dielectric/semiconductor interface is strongly pinned due to the huge N_{SS} value because the E_F cannot move upward without the trap filling [73]. Indeed, the extracted $N_{SS,max}$ value for the SnO_x TFTs at P_o = 4 % is the largest (1.5×10^{20} $eV^{-1}cm^{-3}$). Conversely, the $N_{SS,max}$ value for the SnO_x TFTs at P_o = 8 % was reduced to 2.0×10^{19} $eV^{-1}cm^{-3}$. The superior transporting properties of the SnO_x TFTs at P_o = 8 % was clearly reflected into the higher I_{DS} level of the output characteristics [see Fig. 3.17(b)].

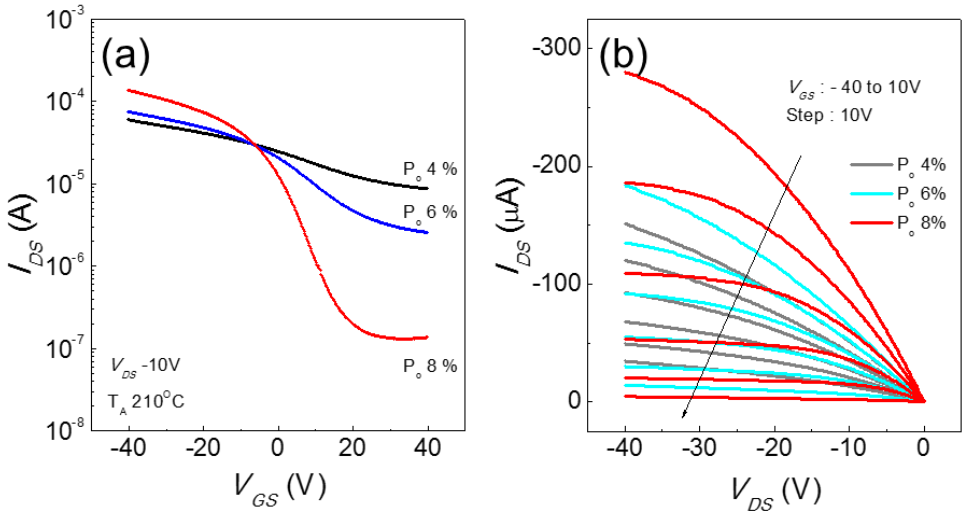

Figure 3.17. Transfer (a) and output characteristics (b) of the bottom gate structure SnO_x (15 nm) TFTs fabricated at various oxygen partial pressures (P_o = 4, 6, 8 %) and thermally annealed at 210 °C.

Table 3.3. Summary of electrical characteristics of the SnO_x TFTs the $I_{ON/OFF}$ ratio, the field effect mobility (μ_{FE}), the subthreshold swing (*SS*) and the maximum bulk trap density ($N_{SS,max}$) and interface trap density ($D_{it,max}$). The SnO_x TFTs are fabricated at various oxygen partial pressures (P_o = 4 - 12 %) and thermally annealed at 210 °C.

P_o (%)	$I_{ON/OFF}$	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	*SS* (V/dec)	$N_{SS,max}$ ($eV^{-1} cm^{-3}$)	$D_{it,max}$ ($eV^{-1} cm^{-2}$)
4	6.8×10^{0}	0.73	62.9	1.52×10^{20}	2.28×10^{14}
6	2.9×10^{1}	1.21	27.6	6.64×10^{19}	9.96×10^{13}
8	1.0×10^{3}	2.80	8.47	2.03×10^{19}	3.05×10^{13}

The electrical properties of the the SnO_x thin films and TFTs, fabricated at P_o = 10 and 12 %, were not measurable due to their too high resistivity.

Figure 3.18 shows the transfer characteristics of the p-channel SnO_x TFTs at P_o = 4, 6, and 8 % at T_A between 150 and 300 °C. The extracted $I_{ON/OFF}$ and μ_{FE} are summarized in Fig. 3.19. As shown in Fig. 3.19, the qualitatively similar trend for the p-channel SnO_x TFTs at P_o = 4, 6, and 8 % at T_A = 210 °C was preserved for the higher T_A (240, 270, and 300 °C). Interestingly, the μ_{FE} and $I_{ON/OFF}$ ratio for the SnO_x TFTs at the given P_o condition were degraded with increasing T_A from 210 to 300 °C. For example, the 300 °C annealed SnO_x TFTs (P_o = 8 %) showed the μ_{FE} of 1.0 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ ratio of 1.6×10^2. This behavior can be also attributed to the structural transition involving the chemical state of Sn ion and microstructure inhomogeneity as the phase separation from 2SnO to SnO_2 plus metallic Sn, which is thermodynamically driven above T_A = 250 °C [74, 75].

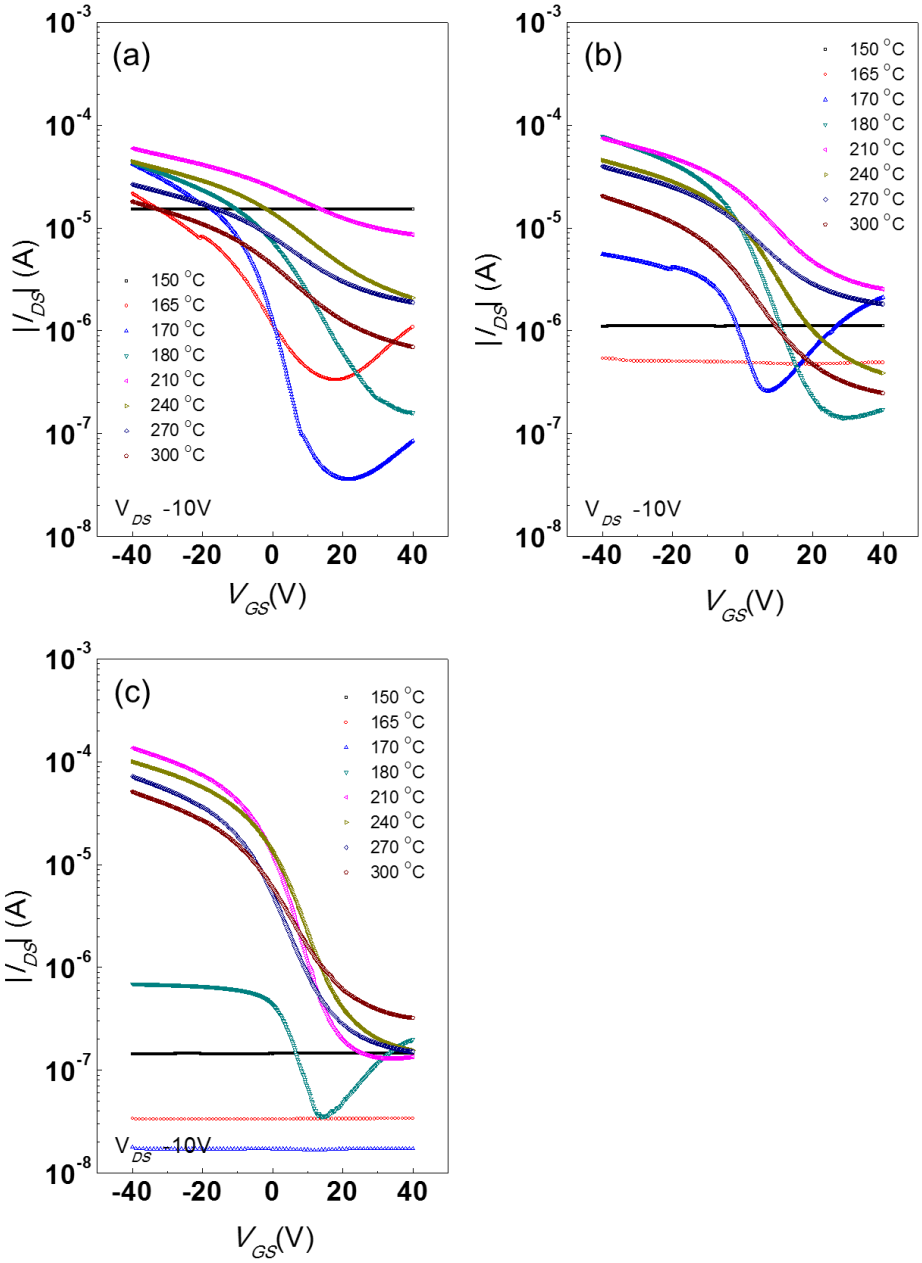

Figure 3.18. The transfer characteristics of the p-channel SnO_x TFTs at P_o = 4 - 8 % at T_A = 150 - 300 °C: P_o = (a) 4, (b) 6 and (c) P_o 8 %.

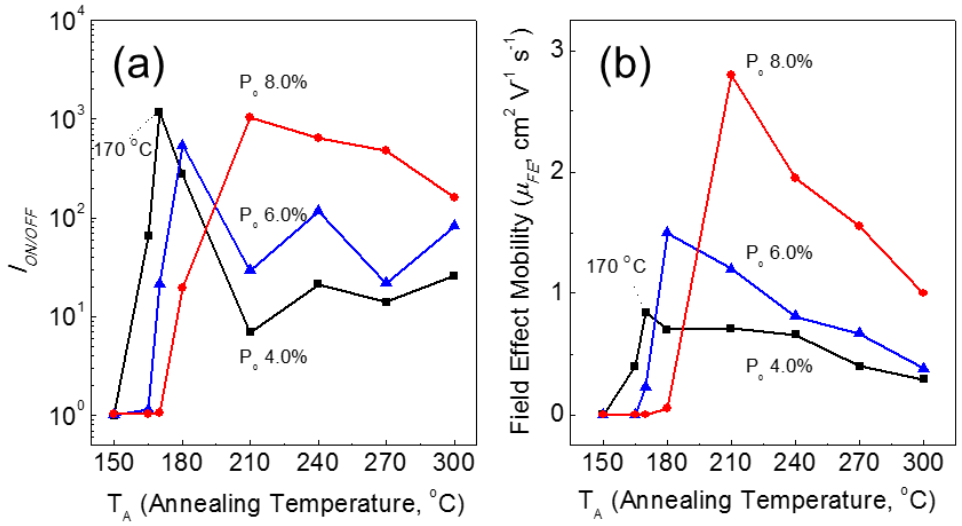

Figure 3.19. TFTs performance extracted from transfer characteristics, (a) $I_{ON/OFF}$ ratio and (b) field effect mobility (μ_{FE}), of the bottom gate structure SnO_x (15 nm) TFTs fabricated at the conditions of P_o = 4 - 8 % and T_A = 150 - 300 °C.

3.7 Complementary metal oxide semiconductor (CMOS)

The complementary metal oxide semiconductor inverter was fabricated using SnO_x thin films as a p-channel and Zn-Sn-O (ZTO) thin films as a n-channel. A thermally-grown 100 nm-thick SiO_2 layer on a heavily p doped Si wafer used as a gate dielectric. 15 nm-thick SnO_x thin film was deposited by DC reactive sputtering using 3 ” metal Sn target with 50 W DC power and at P_o = 8 % and 15 nm-thick Zn-Sn-O thin films was deposited using 3 ” Zn-Sn-O target (Zn : Sn = 1 : 1) with 100 W RF power and in Ar gas. Process pressure was 5 mTorr (0.67 Pa). After channel deposition, 70 nm Pt layer as a S/D electrode was deposited by e-gun evaporation. All channels and electrode were patterned by shadow mask. The fabricated inverter device was carefully annealed in Ar purged tube furnace [above 5 Torr (666.61 Pa)] for 1 h at 250 ^oC, where the lowest temperature n-type Zn-Sn-O channel shows reasonable performance. Figure 3.20 shows (a) fabrication process, (b) fabricated CMOS inverter and (c) schematic diagram of inverter circuit. Transfer characteristics of the resulting NMOS, PMOS and voltage transfer characteristics of CMOS inverter are presented in Fig. 3.21. The gain ($\partial V_{out}/\partial V_{in}$) was extracted from the voltage transfer characteristics of CMOS inverter with V_{DD} = 10 V, and the peak gain of -4.4 was obtained and transferred V_{out} was saturated at 10 V. These performances are comparable to other results, which have been reported [3, 51, 76].

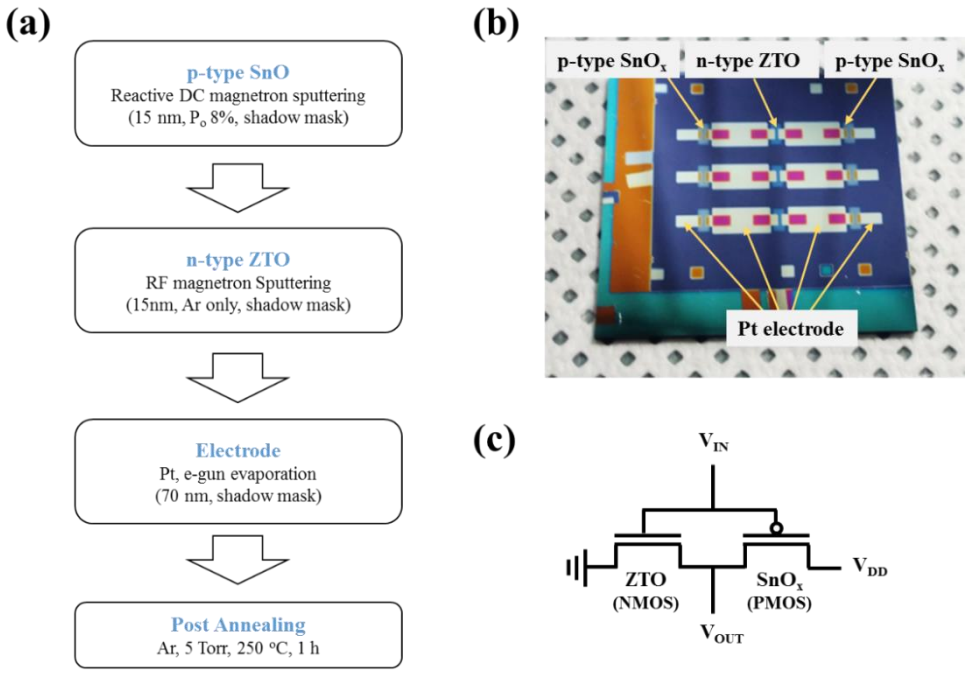

Figure 3.20. CMOS inverter fabricated in this dissertation: (a) process flow, (b) fabricated CMOS inverter and (c) schematic circuit diagram

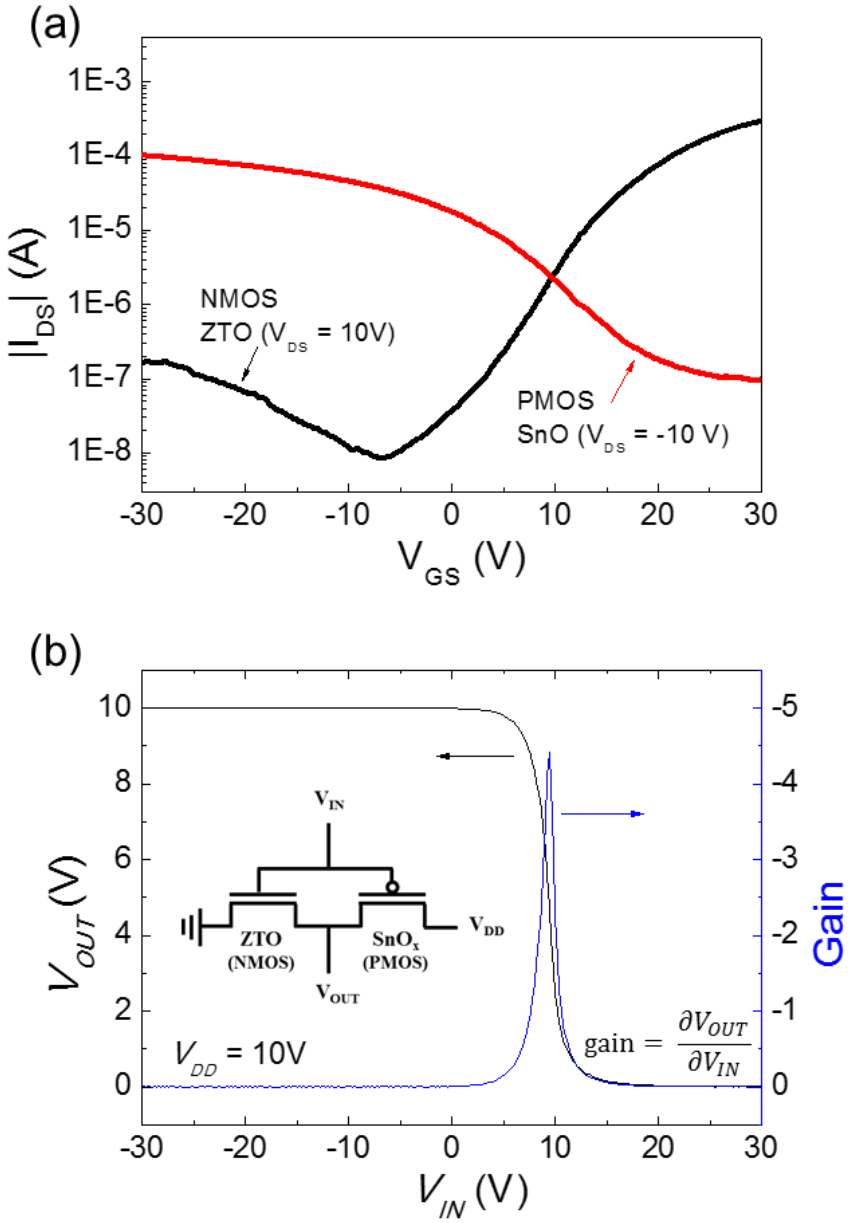

Figure 3.21. (a) Transfer characteristics of NMOS and PMOS. (b) Voltage transfer characteristics and gain of fabricated CMOS inverter.

3.8 Summary

The chemical, structural and electrical properties of the SnO_x thin film prepared by reactive DC sputtering were tailored by controlling the oxygen partial pressure (P_o = 4 -~ 12 %) and post annealing temperature (T_A = 150 - 300 °C). The as-deposited SnO_x thin films were found to be the oxygen-deficiency state irrespective of the P_o whereas the chemical state of Sn ions in the annealed SnO_x films strongly depended on the P_o. The higher P_o condition in the range between 4 and 8 % for the annealed SnO_x films favors the formation of the SnO/SnO_2 phases and the suppression of metallic Sn phase.

Simultaneously, the preferential orientation of SnO_x films was changed from (001), (101) face to (101), (110) face with increasing P_o. The SnO_x film at low P_o of 4% consisted of the dendrite morphology and metallic Sn clusters, which is enhanced by the oxygen deficient stoichiometry. This structural inhomogeneity was weakened with increasing P_o and finally disappeared at P_o = 10 %.

These P_o and T_A dependent chemical and structural properties of the SnO_x films were reflected into the electrical performance of the resulting TFTs. The TFT with the SnO_x channel at P_o = 4 % and T_A = 210 °C exhibited the marginal μ_{FE} of 1.1 $cm^2V^{-1}s^{-1}$ and low $I_{ON/OFF}$ ratio of 6.8, which could be attributed to the structural imperfections such as the rough dendrite structure and metallic Sn cluster in the SnO_x film. High μ_{FE} of 2.8 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ ratio of ~10^3 were achieved for the p-type

TFTs with the SnO_x channel layer at P_o = 8 % and T_A = 210 °C, which underscored the critical role of the homogeneous ordered structure without the Sn metal aggregate and abrupt dendrite structure.

The electrical performances such as the μ_{FE} and $I_{ON/OFF}$ ratio of the SnO_x TFTs at P_o = 8% were deteriorated with increasing T_A from 210 to 300 °C, indicating that the disproportionation reaction [$2SnO \rightarrow SnO_2 + Sn$] should be avoided to secure the optimal transistor performance. The comprehensive understanding of P_o and T_A-dependent chemical, structural and electrical properties of the SnO_x films would provide the useful design concept for the high performance p-channel SnO_x-based TFTs.

In addition, the complementary metal oxide semiconductor inverter was fabricated using SnO_x thin films as a p-channel and Zn-Sn-O (ZTO) thin films as a n-channel. The peak gain of -4.4 was obtained and transferred V_{out} was saturated at 10 V. These results are comparable to those of oxide CMOS which have been reported, previously.

Chapter 4. Effect of Interface Layer on the Electrical Functionality of SnO_x TFTs

4.1 Introduction

Metal oxide semiconductors (MOSs) have been studied extensively as a promising materials for emerging applications such as flexible-transparent electronics, logic circuit and/or inverter for low power consumption due to their outstanding characteristics, showing high optical transparency and high electrical conductivity [1, 2, 3].

However, to date, only n-type oxide semiconductors such as In-Ga-Zn-O (IGZO) have been commercialized showing excellent device performance with electron mobility over 10 $cm^2V^{-1}s^{-1}$ [4]. This is attributed by typical band characteristics of MOSs. The conduction band (CB) of MOSs typically contains a conduction path generated by delocalized s-orbitals of metal ions, while the valence band maximum (VBM), as a conduction path of holes, is mainly composed of localized p-orbitals of oxygen ions, so that the band is very flat and hole effective masses are very large. Thus, p-type oxides have very low carrier mobility compared to their n-type counterpart. That is, strong localization of orbitals at the VBM is the main obstacle to gain high performance p-channel oxide TFTs [1, 3, 56, 77, 78].

To reduce the localization behavior in the valence band and enhance p-type conductivity, MOSs which have metal cation whose energy levels are comparable to those of the p-orbitals of oxygen ions have been extensively studied [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22].

Especially, tin monoxide (SnO) have received increasing attentions as a promising p-type semiconductor material. In SnO, the delocalized 5s orbitals of metal ion (Sn^{2+}), which have very close energy level and intensity to 2p orbitals of oxygen ion (O^{2-}) at the VBM, reduce localization of valence band edge. As a result, SnO have effective hole transport path and show high hole mobility [23, 24].

Recently, p-type SnO_x TFTs which shows enhanced field effect mobility (μ_{FE}) of 6.75 $cm^2V^{-1}s^{-1}$, comparable to those of n-type MOS TFTs, has been reported [29]. Including above result, most of studies about p-type SnO_x have focused on the enhancement of p-type characteristics by modulating process conditions such as process pressure, oxygen partial pressure and annealing temperature. However the functionalities of p-type SnO_x TFTs are still suffered from high I_{OFF} (off current) of 10^7 - 10^8 A or high V_{th} of over 10 V [7, 28, 29, 79, 80].

Considering with V_{th}, the interface between gate dielectric and semiconductor have been studied extensively in Si-based devices [81, 82, 83, 84, 85, 86]. However the effects of interface are still not much known with p-type SnO_x TFTs. Here, the comparative study about the effect of interface on p-type SnO_x was conducted. For this study, 7-nm-thick interface layers such as SiN_x, Al_2O_3 and SiOF (fluorine doped

silicon dioxide) were deposited on the thermally-grown SiO_2 gate dielectric, and the effect of interface layers, including a thermally-grown SiO_2 only as a control device, on the electrical functionalities of p-type SnO_x TFTs were investigated.

4.2 Experimental

The 7 nm of thin dielectric layers such as SiN_x, SiOF and Al_2O_3 were deposited on a thermally-grown 100nm-thick SiO_2 layer of highly p-doped Si wafer. The SiN_x and SiOF layers were deposited by plasma enhanced chemical vapor deposition (PECVD, 85 ^oC) and Al_2O_3 layer was deposited by plasma enhanced atomic layer deposition (PEALD, 200 ^oC)

The fabrication process of p-type SnO_x TFTs was basically same with aforementioned process in section 3.2 with fixed oxygen partial pressure (P_o) of 8 % and annealing temperature (T_A) of 210 ^oC. Figure 4.1 shows the fabricated device structure.

The surface topography of interface layers was analyzed with AFM (JEOL, JSPM-5200), and the valence band offset between the interface layers and SnO_x channel layer was estimated based on the results of XPS (VG Thermo Scientific, Sigma Probe) analysis. Electrical characteristics of the SnO_x TFTs were measured at room temperature using a semiconductor parameter analyzer (HP4155A, Hewlett-Packard).

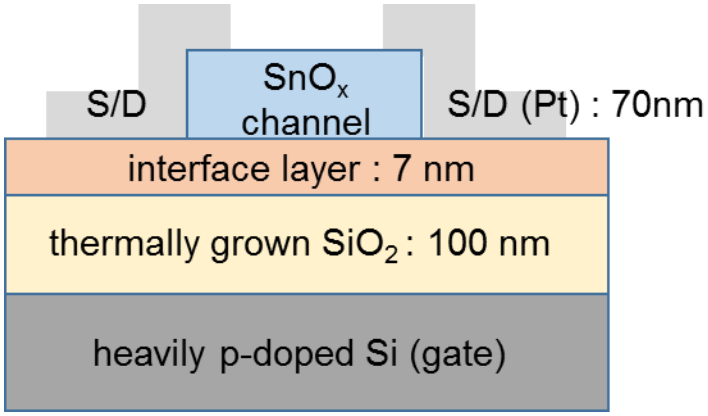

Figure 4.1. The schematic diagram of the SnO_x TFT with the 7 nm-interface layer between SiO_2 layer and SnO_x channel layer.

4.3 Electrical functionality of p-type SnO_x TFTs with interface layer

The comparative study of the effect of various interface layers on the electrical functionality of the bottom gate p-type SnO_x TFTs was conducted. Figure 4.2 shows the representative transfer characteristics and output characteristics for TFTs with various interface layers: SiN_x, Al_2O_3, SiOF and a thermally-grown 100 nm-thick SiO_2 as a control device.

The $I_{ON/OFF}$, field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold gate swing (SS) were extracted with the method mentioned in chapter 2.3.3 and the maximum bulk trap density ($N_{SS,max}$) and interfacial trap density ($D_{it,max}$) were evaluated from the equation (4.1) where the $N_{SS,max}$ ($D_{it,max}$) value was estimated by setting the $D_{it,max}$ ($N_{SS,max}$) term to be zero. Table 5.1 shows summarized parameters mentioned above.

Changes of the capacitance per unit area of the gate dielectric (C_i) due to additional interface layer were calculated with relative permeability reported [56, 87, 88]. The results show that the capacitances of gate dielectrics with interface layers decrease by 6.5 % or less compared to those of thermally grown 100 nm-thick SiO_2 layer: SiN_x 3.0 %, Al_2O_3 3.5 % and SiOF 6.5 %, respectively. Because neglecting these variations does not affect to interpret the test results, the capacitance per unit area of the gate dielectric (C_i) was fixed at 34.5 $nFcm^{-2}$ (100 nm-thermally-grown SiO_2 layer).

The control device of p-type SnO_x TFT showed μ_{FE} of 2.8 $cm^2V^{-1}s^{-1}$ and current modulation capability ($I_{ON/OFF}$) of 1.8×10^3. Those results were well consistent with the previous results in chapter 3.6. Compared to this, the SnO_x TFT with SiN_x interface layer showed the marginal μ_{FE} of 2.1 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ of 7.9. While the SnO_x TFT with SiOF interface layer showed the best μ_{FE} of 3.1 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ of 1.6×10^3. The SnO_x TFT with Al_2O_3 interface layer showed degraded μ_{FE} of 2.5 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ of 8.1×10^2 compared to those of the control device.

Interestingly, V_{th} of the SnO_x TFT with SiOF interface layer was considerably changed in negative direction (V_{th} = 2.0 V) compared to that of the control device (V_{th} = 19 V).

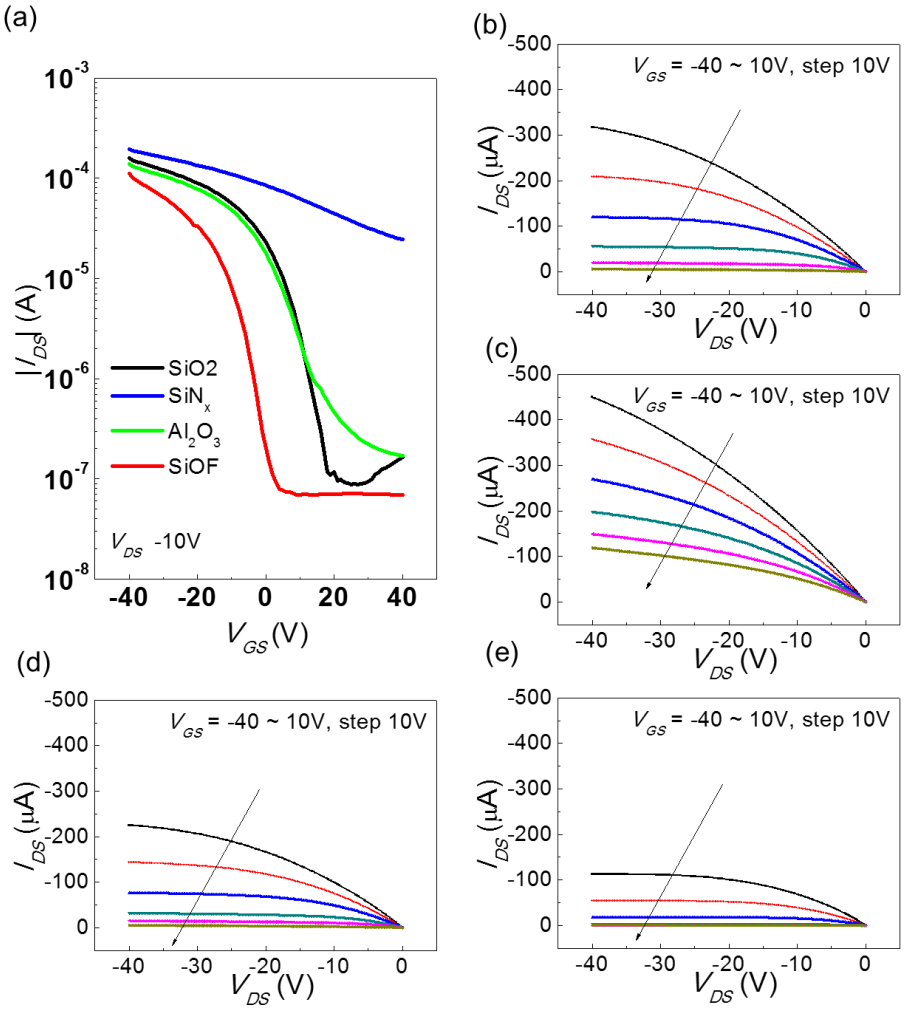

Figure 4.2. Transfer (a) and output characteristics (b-e) of the bottom gate structure SnO_x (15 nm) TFTs with various interface layers: (b) SiO_2 (control device), (c) SiN_x, (d) Al_2O_3 and (e) SiOF

Table 4.1. Summary of electrical characteristics of the SnO_x TFTs with various interface layers including the $I_{ON/OFF}$ ratio, I_{ON} current, the field effect mobility (μ_{FE}), threshold voltage (V_{th}), the subthreshold swing (SS) and the maximum bulk trap density ($N_{SS,max}$) and interface trap density ($D_{it,max}$).

Interface Layer	**SiO_2 (control device)**	**SiN_x**	**Al_2O_3**	**SiOF**
$I_{ON/OFF}$	1.8×10^{3}	7.9×10^{0}	8.1×10^{2}	1.6×10^{3}
I_{ON} (A)	1.6×10^{-4}	1.9×10^{-4}	1.4×10^{-4}	1.1×10^{-4}
μ_{FE} ($cm^2V^{-1}s^{-1}$)	2.8	2.1	2.5	3.1
V_{th} (V)	19.0	over 40.0	21.5	2.0
SS (V/dec)	6.9	29.9	10.2	5.4
$D_{it,\,max}$ ($eV^{-1}cm^{-2}$)	2.5×10^{13}	2.5×10^{14}	3.7×10^{13}	1.9×10^{13}
$N_{SS,\,max}$ ($eV^{-1}cm^{-3}$)	1.6×10^{19}	1.7×10^{20}	2.5×10^{19}	1.3×10^{19}

4.4 Surface topography of the interface layer

To consider the plausible cause of variations in performance of the SnO_x TFTs with related to interface layers, At first, the surface topography of the interface layers were analyzed with AFM. As shown Fig. 4.3, the surface of thermally-grown 100 nm-thick SiO_2 layer and 7 nm-thick Al_2O_3 layer deposited by ALD process show very smooth morphologies with root mean square (RMS) surface roughness (R_q) of 0.20 nm or less. The surface of 7 nm-thick SiN_x layer deposited by CVD process shows also smooth and feature-less morphologies with R_q of 0.55 nm. The surface of 7 nm-thick SiOF layer deposited by CVD process shows worst surface morphology with R_q of 1.09 nm which is highest value among those of the surfaces with or without interface layer. However, the TFT which have SiOF interface layer showed best electrical performance. As a result, the plausible relations between TFT performance and surface morphologies of underlying interface layer could not be found.

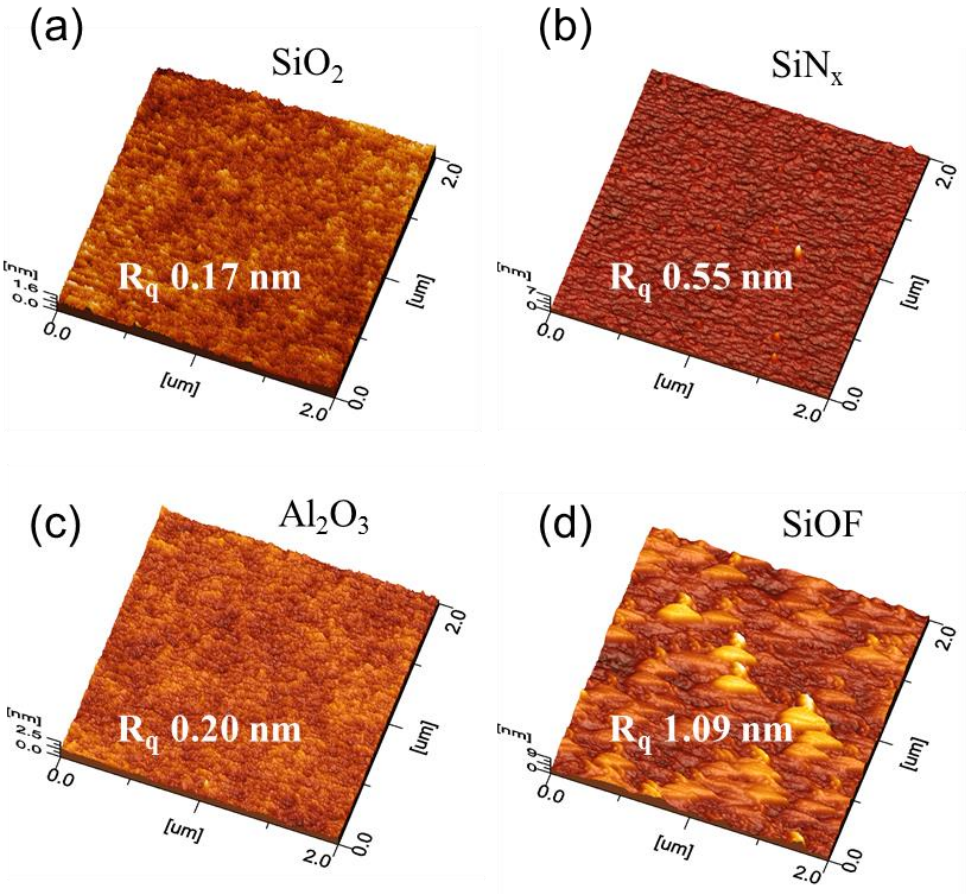

Figure 4.3. AFM topographies of the 7 nm-thick interface layers on 100 nm-thick thermally grown SiO_2 after thermally annealing at 210 ^oC for 1 h in Ar purged [5 Torr (666.61 Pa)] tube furnace.

4.5 Relative band structure of SnO_x TFTs with interface layer

The relative band structures of SnO_x channel layer and SiO_2 gate dielectric with interface layers such as SiN_x, Al_2O_3, SiOF were further analyzed by XPS analyses using a monochromatic Al-Kα source. All the samples were annealed at 210 ^oC for 1 h in Ar purged [5 Torr (666.61 Pa)] tube furnace. Ar sputtering conducted only on the SnO_x thin films to eliminate surface oxidation layer. While gate dielectrics with or without interface layers were analyzed on their surfaces. Note that all the binding energies of the chemical compositions were calibrated from the peak position of *C* 1s at 284.8 eV.

The valence band spectra of the SnO_x, SiO_2, SiN_x, Al_2O_3 and SiOF are depicted in Fig 4.4(a) and (b). The extracted positions of valence band maximum (VBM) and estimated band diagrams are also depicted in Fig. 4.4(c) and (d), respectively.

The valence band spectra of the SnO_x thin films are almost same irrespective of underlying layers. While the valence band spectra of the interface layers are quite different from each other [see Fig. 4.4(a) and (b)].

Relative VBM positions of SiO_2, SiN_x, Al_2O_3 and SiOF layers are approximately 4.7, 3.1, 1.7 and 4.5 eV below with respect to VBM of the SnO_x, respectively. As shown in Fig. 4.5(d), the VBM of SiN_x is relatively close to VBM of SnO_x. It is well known that SiN_x have large tail states in vicinity of VBM [89, 90, 91]. Thus the

marginal performances of small $I_{ON/OFF}$ and low μ_{FE} are attributed by high trap density near VBM of SiN_x interface, which can induce Fermi level pinning or hole trapping.

Figure 4.5 shows estimated band diagram of the SnO_x TFT, which was fabricated on the thermally-grown 100 nm-thick SiO_2 (control device). The estimated ionization potential of the p-type SnO_x is approximately 5.25 eV. This value is in the range of previously reported ionization potentials of p-type SnO_x: 4.4 ~ 5.8 eV [23, 51, 92].

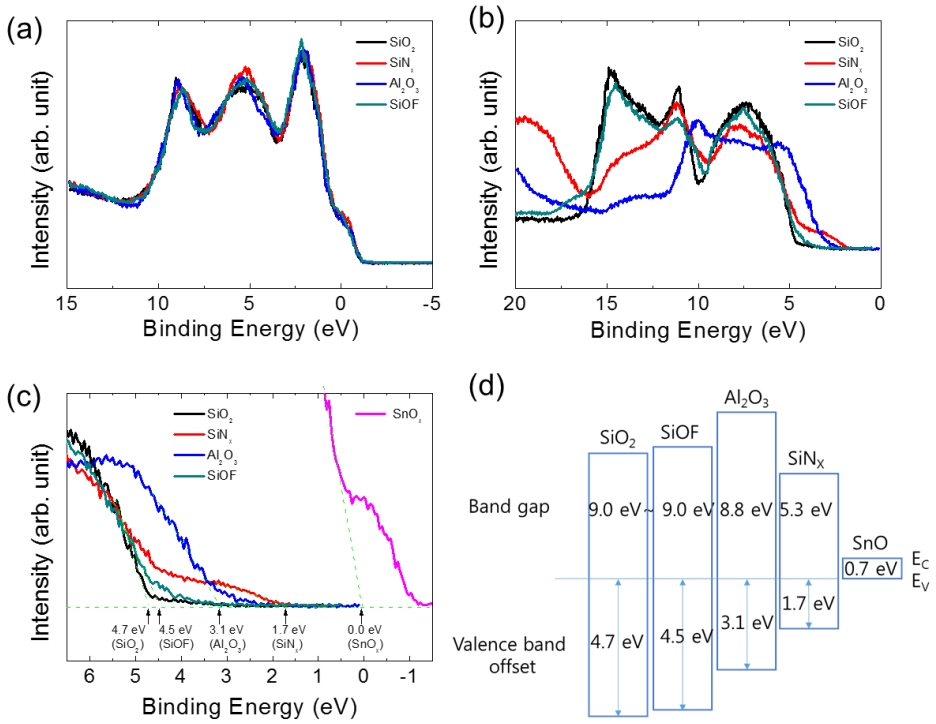

Figure 4.4. XPS valence band spectra of (a) the SnO_x channel layers which deposited on each 7 nm-thick interface layer and (b) gate dielectrics with interface layer of SiN_x, Al_2O_3, SiOF and which has only thermally-grown SiO_2. (c) Extracted valence band offset with respect to the valence band maximum of the SnO_x thin films and (d) estimated relative band structures.

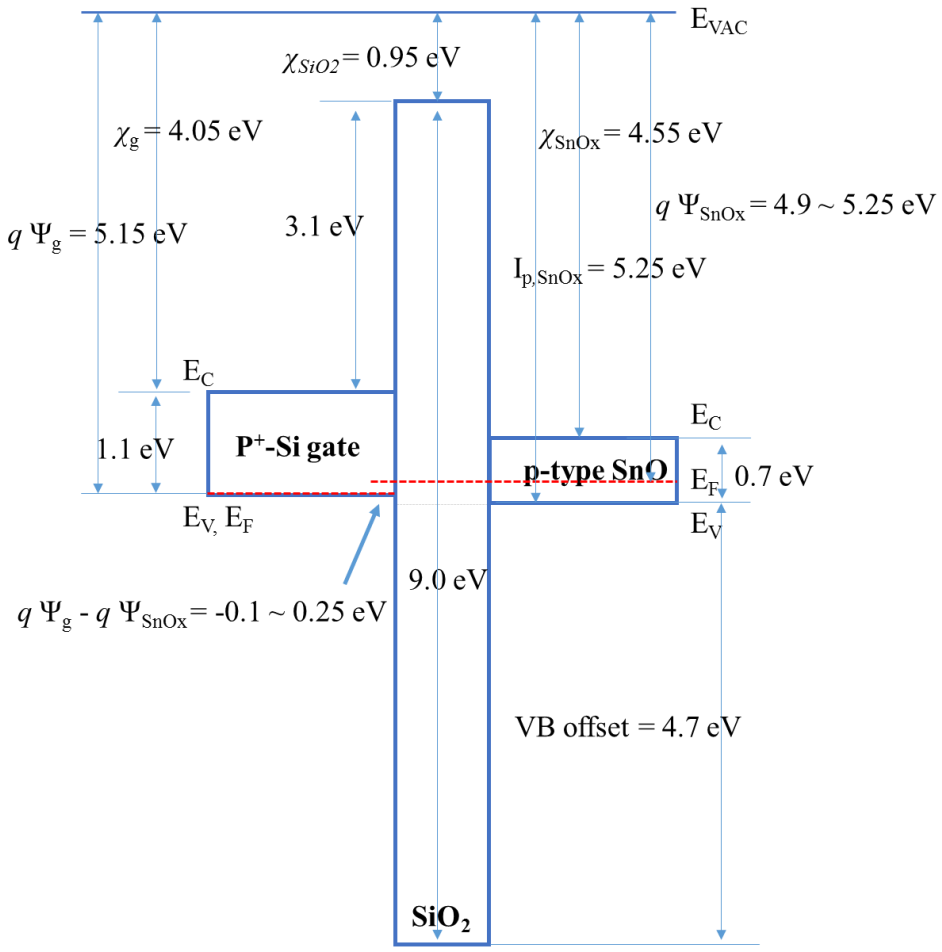

Figure 4.5. Estimated ideal band structure of the SnO_x TFT, which was fabricated on the thermally-grown 100 nm-thick SiO_2.

4.6 V_{th} shift mechanisms of the SnO_x TFT with SiOF interface layer

Threshold voltage (V_{th}) and flat band voltage (V_{fb}) of metal oxide semiconductor TFTs can be expressed with equations as follows [93] (see also Fig. 4.6):

$$V_{th} = V_{fb} + 2\varphi_B + \frac{\sqrt{qN_a \, 2\varepsilon_s 2\varphi_B}}{C_i} \quad (4.1)$$

$$V_{fb} = \psi_g - \psi_s - \frac{Q_i}{C_i} \quad (4.2)$$

where $2\varphi_B$ is surface band bending at threshold condition, N_a is acceptor concentration, ε_s is permeability of semiconductor, C_i is the capacitance per unit area of the gate dielectric, q is the electron charge, ψ_g and ψ_s are the gate and semiconductor work functions and Q_i is a oxide charge such as fixed oxide charge, oxide trapped charge, mobile oxide charge and so on.

Here, φ_B is characteristics of semiconductor layer which is closely related with acceptor concentration. That is, it is characteristics of channel layer.

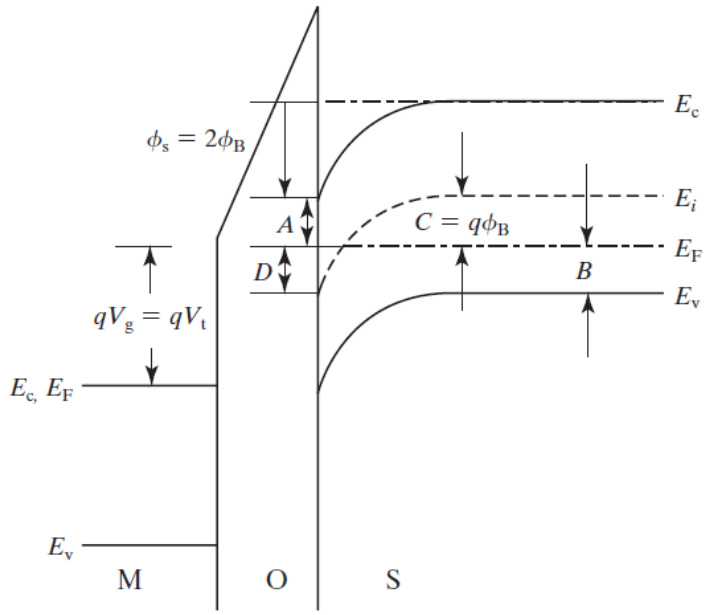

Figure 4.6. Band diagram of NMOS at the threshold condition [93].

Considering with V_{th} position, the V_{fb} modulating techniques using interface layer between gate dielectrics and semiconductor (or gate) have been extensively investigated in Si based devices. For example, the dielectric interface layers can induce interface dipole and modulate effective work function (EWF) of gate [83, 84, 85, 86, 94]. In addition, the dielectric interface layers can also induce differences in oxide charge [94, 95, 96]. Thus the V_{th} shift in this study could be attributed by changes of EWF or oxide charge originated from the SiOF interface layer. However, V_{th} shift in this manner should take place in same direction irrespective of PMOS or NMOS [54]. To make it clear, V_{th} shift of n-type Zn-Sn-O TFT fabricated on the SiOF interface layer was also evaluated. The results were depicted in Fig. 4.7.

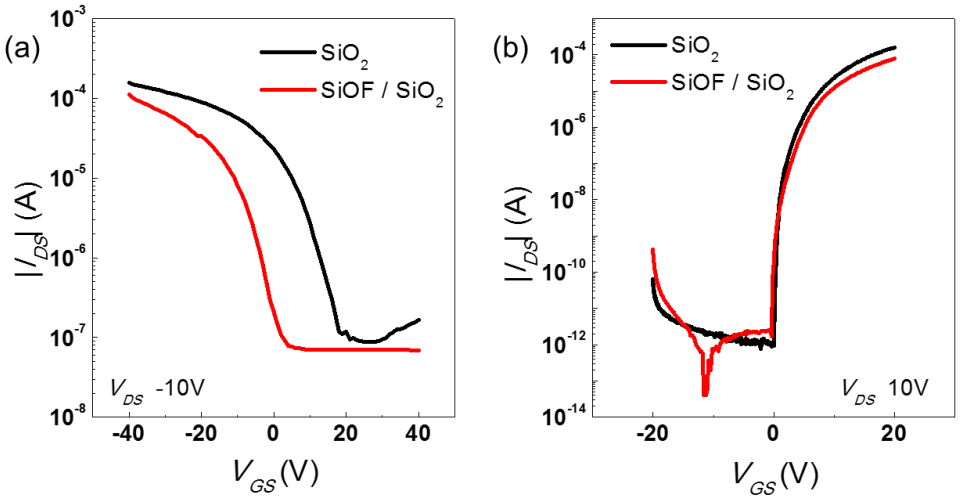

Figure 4.7. Transfer characteristics of (a) p-type SnO_x TFT and (b) n-type Zn-Sn-O TFT with or without SiOF interface layer.

As shown in Fig. 4.7, V_{th} of the n-type Zn-Sn-O TFT did not changed. Conversely, the p-type SnO_x TFT with SiOF interface layer showed large V_{th} shift of -17 V. Because PMOS and NMOS TFT showed quite different V_{th} shift, either oxide charge or interface dipole couldn't be adequate explanations for the V_{th} shift in p-type SnO_x TFT in this case [54].

To explain these, Fermi-level pinning at the interface between semiconductor and gate dielectric was considered [82, 97]. High V_{th} of 19 V in the p-type SnO_x TFT fabricated on SiO_2 can be understood by Fermi level pinning at the interface of SiO_2 and SnO_x, which is attributed by high interface state density (D_{it}) at the interface. Conversely, SiOF interface layer, fluorine atoms doped in SiO_2 help reducing defects at bulk or surface in the band gap of SiO_2 [98, 99, 100, 101, 102]. Therefore Fermi level become less pinned at SiOF and SnO_x interface compared to SiO_2 and SnO_x interface. Thus the p-type SnO_x TFT can show more improved performances including V_{th} close to 0 V. The explanation well supports the estimated $D_{it,\ max}$ in chapter 4.3: 2.5×10^{13} (SiO_2) → 1.9×10^{13} (SiOF).

However, significant V_{th} shift is not observed in the n-type Zn-Sn-O TFT fabricated on SiOF. This might be attributed by the similarity of the interface state densities in vicinity of conduction band minimum (CBM) irrespective of SiOF or SiO_2 interface layer.

4.7 Summary

Comparative study about the effect of interface layers on the bottom gate SnO_x TFT functionality was conducted. 7 nm-thick-interface layers such as SiN_x, Al_2O_3 and SiOF were deposited on 100nm-thick thermally-grown SiO_2 gate dielectric layer and p-type SnO_x TFTs were fabricated on those interface layers.

Electrical functionalities were quite different with related to interface layer. The SnO_x TFT without interface layer showed μ_{FE} of 2.8 $cm^2V^{-1}S^{-1}$ and $I_{ON/OFF}$ of 1.8 × 10^3 and V_{th} of 19 V. Compared to this, the SnO_x TFT on SiN_x interface layer showed much poor performance. The μ_{FE}, $I_{ON/OFF}$ and V_{th} was degraded to 2.1 $cm^2V^{-1}S^{-1}$, 7.9 and over 40 V (not showing obvious off current characteristics within the gate bias sweep range), respectively. Conversely, the SnO_x TFT on SiOF interface layer showed best performance. The μ_{FE} and $I_{ON/OFF}$ was 3.1 $cm^2V^{-1}S^{-1}$ and 1.6 × 10^3. Interestingly, V_{th} was shifted to 2 V.

The RMS surface roughness of the interface layer, R_q was varied from 0.17 to 1.09 nm according to interface layer. But the differences in TFT functionality could not be explained by R_q.

From the relative band structure analyzed XPS, it was found that VBM of SiN_x is 1.7 eV below with respect to VBM of p-type SnO_x channel. In addition, SiN_x is well known to have large valence band tail in band gap. Thus the poor performance of the

SnO_x TFT with SiN_x interface layer is attributed by large gap states above the VMB of SiN_x, which can induce Fermi level pinning near the VBM of SnO_x or hole trapping.

For V_{th} shift in SnO_x TFT with SiOF interface layer, it was also found that n-type Zn-Sn-O TFT with SiOF interface layer did not show V_{th} shift. Therefore, fixed oxide charge and interface dipole, which could modulate flat band voltage, were excluded from considerable causes.

Instead, Fermi level pinning at the interface between SnO_x and gate dielectric was suggested. High V_{th} of 19 V in SnO_x TFT on SiO_2 might be attributed by Fermi level pinning near the VBM. In SiOF, fluorine atoms help reducing defects at bulk or surface in the band gap. Therefore, reduced D_{it}, compared to SiO_2, at the interface between SnO_x and SiOF can attribute to weakening Fermi level pinning near VBM of SnO_x. As a result, SnO_x TFT with SiOF interface layer showed negative-shifted V_{th}. Estimated $D_{it,\,max}$ of the SnO_x TFT with SiOF interface layer compared to that of SiO_2 gate dielectric is in good agreement with this explanation: $D_{it,max}$ 2.5×10^{13} (SiO_2) → 1.9×10^{13} (SiOF)

5. Conclusions

In this study, the composition dependent structures and electrical properties of p-type SnO_x thin film prepared by reactive DC magnetron sputtering were comprehensively investigated and the oxide CMOS inverter was also demonstrated. In addition, comparative study about the effect of interface layers on the functionality of the bottom gate SnO_x TFT was also conducted.

At first, the chemical, structural and electrical properties of the SnO_x thin film prepared by reactive DC sputtering were tailored by controlling the oxygen partial pressure (P_o = 4 - 12 %) and post annealing temperature (T_A = 150 - 300 °C).

The as-deposited SnO_x thin films were found to be the oxygen-deficiency state irrespective of the P_o whereas the chemical state of Sn ions in the annealed SnO_x films strongly depended on the P_o. The higher P_o condition in the range between 4 and 8 % for the annealed SnO_x films favors the formation of the SnO/SnO_2 phases and the suppression of metallic Sn phase. Simultaneously, the preferential orientation of SnO_x films was changed from (001), (101) face to (101), (110) face with increasing P_o. The SnO_x film at low P_o of 4% consisted of the dendrite morphology and metallic Sn clusters, which was enhanced by the oxygen deficient stoichiometry. This structural inhomogeneity was weakened with increasing P_o and finally disappeared at P_o = 10 %. These P_o and T_A dependent chemical and structural properties of the SnO_x films were reflected into the electrical performance of the resulting TFTs. The TFT with the SnO_x

channel at P_o = 4 % and T_A = 210 °C exhibited the marginal μ_{FE} of 1.1 $cm^2V^{-1}s^{-1}$ and low $I_{ON/OFF}$ ratio of 6.8, which were attributed to the structural imperfections such as the rough dendrite structure and metallic Sn cluster in the SnO_x film. High μ_{FE} of 2.8 $cm^2V^{-1}s^{-1}$ and $I_{ON/OFF}$ ratio of ~10^3 were achieved for the p-type TFTs with the SnO_x channel layer at P_o = 8 % and T_A = 210 °C, which underscored the critical role of the homogeneous ordered structure without the Sn metal aggregate and abrupt dendrite structure. The electrical performances such as the μ_{FE} and $I_{ON/OFF}$ ratio of the SnO_x TFTs at P_o = 8% were deteriorated with increasing T_A from 210 to 300 °C, indicating that the disproportionation reaction [$2SnO \rightarrow SnO_2 + Sn$] should be avoided to secure the optimal transistor performance.

In addition, the complementary metal oxide semiconductor (CMOS) inverter was fabricated using SnO_x thin films as a p-channel and Zn-Sn-O (ZTO) thin films as a n-channel. The peak gain of -4.4 was obtained and transferred V_{out} was saturated at 10 V. These results are comparable to those of oxide CMOS reported previously.

And lastly, the effect of interface layers on the bottom gate SnO_x TFT functionality was also comparatively investigated. 7 nm-thick-interface layers such as SiN_x, Al_2O_3 and SiOF are deposited on 100 nm-thick thermally-grown SiO_2 gate dielectric layer, and SnO_x TFTs were fabricated on those interface layers.

SnO_x TFTs showed quite different electrical functionalities according to interface layers. The SnO_x TFT on thermally-grown SiO_2 showed μ_{FE} of 2.8 $cm^2V^{-1}S^{-1}$ and $I_{ON/OFF}$ of 1.8×10^3 and V_{th} of 19 V. However, in the SnO_x TFT with SiN_x interface

layer, the μ_{FE}, $I_{ON/OFF}$ and V_{th} were degraded to 2.1 $cm^2V^{-1}S^{-1}$, 7.9 and over 40 V (not showing obvious off current characteristics within gate bias sweep range), respectively. Conversely, the SnO_x TFT with SiOF interface layer exhibited best performance. The μ_{FE} and $I_{ON/OFF}$ was 3.1 $cm^2V^{-1}S^{-1}$ and 1.6×10^3. Interestingly, V_{th} was shifted to 2 V.

From the relative band structure analyzed XPS, it was found that VBM of SiN_x is 1.7 eV below with respect to VBM of p-type SnO_x. In addition, it is well known that SiN_x have large valence band tail in band gap. Thus poor performance of the SnO_x TFT with SiN_x interface layer was attributed by large gap states above the VMB of SiN_x, which could induce Fermi level pinning near the VBM of SnO_x or hole trapping.

To explain V_{th} shift in SnO_x TFT with SiOF interface layer, Fermi level pinning at the interface between SnO_x and gate dielectric was also suggested. Fixed oxide charge and interface dipole, which could modulate flat band voltage, were excluded from the consideration because n-type Zn-Sn-O TFT on SiOF interface layer did not show V_{th} shift compared to that of SiO_2. High V_{th} of 19 V in SnO_x TFT on SiO_2 might be attributed by Fermi level pinning near the VBM. However, in SiOF, fluorine atoms help reducing defect density at bulk or surface in the band gap. Therefore, Fermi level is less pinned near VBM and V_{th} can be shifted in negative direction (19 → 2 V). Estimated $D_{it,\ max}$ is in good agreement with this explanation: $D_{it,max}$ 2.5×10^{13} (SiO_2) → 1.9×10^{13} (SiOF)

The comprehensive understanding of P_o and T_A-dependent chemical, structural,

electrical properties of the SnO_x films and the interface-dependent electrical functionality of the SnO_x TFT would provide the useful design concept for the high performance p-channel SnO_x-based TFTs.

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Abstract (in Korean)

본 논문에서는 p형 산화물 트랜지스터로의 적용을 목적으로, 반응성 스퍼터링 공법으로 제작한 SnO_x 박막에 대해, 증착 중의 산소 분압 (P_o) 및 후열처리 (T_A) 온도가 박막의 구조적, 화학적, 전기적 특성에 주는 영향에 대해 연구하였으며, p형 SnO_x TFTs의 전기적 특성에 영향을 주는 다양한 계면층의 영향에 대한 연구도 함께 진행하였다.

상대적으로 낮은 4%의 산소분압에서 제작하고, 210 °C에서 후열처리를 진행한 SnO_x 박막에서는 dendrite 모폴로지와 금속 Sn 클러스터가 관찰되었고, 이 박막을 이용해 제작한 p형 SnO_x 트랜지스터는 낮은 이동도와 $I_{ON/OFF}$ 비율을 보였다. 이는 산소가 부족한 non-stoichiometry에 의해 발생한 박막 내부의 구조적 결함이 벌크 트랩 상태로 작용하여 hole carrier의 효과적인 전도를 방해하였다는 것을 의미한다. 이러한 dendrite 구조와 금속성 Sn 클러스터는 박막 증착 중의 산소 분압을 높임으로써 제거할 수 있었다. 상대적으로 높은 8%의 산소분압에서 제작된 p형 SnO_x 트랜지스터는 2.8 $cm^2V^{-1}s^{-1}$의 높은 이동도와 10^3 수준의 좋은 $I_{ON/OFF}$ 비율을 보였고, 이를 통해 금속성 Sn 응집체와 abrupt한 dendrite 구조가 없는 균일한 ordered 구조가 매우 중요한 역할을 하는 것을 알 수 있었다. 최적의 조건으로 확인된 8% 산소분압에서 제작한 p형 SnO_x 트랜지스터의 이동도와 and $I_{ON/OFF}$ 비율 등의 성능은 후열처리 온도를 210 °C 에서 300

°C로 증가시킴에 따라 열화되었는데, 이는 disproportionation 반응 [2SnO → SnO_2 + Sn]으로 설명할 수 있다.

또한 본 연구에서는 p형 SnO_x 및 n형 Zn-Sn-O (ZTO) 박막을 이용해 Complementary Metal Oxide Semiconductor (CMOS) 인버터를 제작하여, 산화물 CMOS에 대해 문헌 상의 보고와 비교할만한 수준인 -4.4의 peak gain을 얻었다.

열적으로 성장시킨 SiO_2, 7 nm 두께를 갖는 SiN_x, Al_2O_3 및 SiOF와 같은 다양한 계면층들이 bottom gate 구조의 p형 SnO_x 트랜지스터의 성능에 주는 영향에 대해서도 연구하였다. SnO_x 트랜지스터는 계면층에 따라 매우 다른 전기적 특성을 보였는데, 열적으로 성장시킨 SiO_2 위에 제작한 SnO_x 트랜지스터는 2.8 $cm^2V^{-1}S^{-1}$의 이동도와 1.8×10^3의 $I_{ON/OFF}$ 비율 및 19V의 V_{th}를 보인 반면, SiN_x 위에 제작한 트랜지스터는 2.1 $cm^2V^{-1}S^{-1}$의 이동도와 7.9 의 $I_{ON/OFF}$ 비율 및 40V 이상의 V_{th}와 같이 열화된 성능을 보였다. 반면에 SiOF 위에 제작한 트랜지스터는 3.1 $cm^2V^{-1}S^{-1}$의 이동도와 1.6×10^3의 $I_{ON/OFF}$ 비율과 같이 향상된 성능을 나타내었고, V_{th}의 위치도 2V로 이동하였다.

XPS 분석 및 상대적인 밴드 구조의 비교를 통해, SiN_x 계면층의 열등한 성능은 상대적으로 작은 valence band offset과 Valence Band Maximum (VBM) 근처에서의 큰 tail state에 기인하는 것을 확인하였다.

SiOF 계면층 위에 제작한 p 형 SnO_x 트랜지스터의 V_{th} 이동을 설명하기 위해, flat band voltage 의 변화를 유발할 수 있는 fixed oxide charge

와 interface dipole 등을 고려하였지만, SiOF 계면층 위에 제작한 n 형 ZTO 트랜지스터에서는 V_{th} 이동이 발생하기 않았기 때문에, 본 연구에서는 이들을 가능한 원인에서 배제하고, V_{th} 이동을 설명하기 위해, 계면층에서의 Fermi level pinning 을 제안하였다. SiO_2 계면층 위에 제작한 SnO_x 트랜지스터에서의 높은 V_{th} 는 VBM 근처에서의 Fermi level pinning 에 의한 것일 수 있다. 그런데, SiOF 계면층 위에서는 fluorine 원자들이 band gap 내의 bulk 또는 surface 의 defect density 를 줄이는 역할을 하여, VBM 근처에서의 Fermi level pinning 덜 발생하게되고, 결과적으로 V_{th} 가 음의 방향으로 이동할 수 있다(19 → 2 V). 이러한 설명은 $D_{it,\ max}$ 의 계산된 추정치가 감소 [2.5×10^{13} (SiO_2) → 1.9×10^{13} (SiOF)] 하는 것과도 잘 일치한다.

Keywords: 주석산화물, p형 산화물 반도체, 박막 트랜지스터, Complementary Metal Oxide Semiconductor (CMOS), 산소분압, 후열처리 온도, 계면층

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