공학박사학위논문

A Study of Bottom Gate MILC Polycrystalline Silicon TFTs and Reduction of the Leakage Current

하부 게이트 구조를 가지는 저온 다결정 실리콘 박막 트랜지스터와 누설전류 감소에 대한 연구

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석 기 환

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by
Ki Hwan Seok

Under Supervision of Prof. Seung Ki Joo

February 2017

School of Material Science and Engineering

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석 기 환

석 기 환의 박사학위 논문을 인준함

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Abstract

A Study of Bottom Gate MILC Polycrystalline Silicon TFTs and Reduction of the Leakage Current

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Nowadays the display market meets the transitional period of change. In the past decade, the main stream of display market is move from Cathode Ray Tube (CRT) to Liquid Crystal Display (LCD) and now, it is move from LCD to Active Matrix Organic Emitting Diode (AMOLED). The main reason of this transition is due to the requirement of extremely high resolution display and need of the advanced display for example the transparent and foldable display. The LCD which is the most basic devices among the flat panel displays, use amorphous silicon Thin Films Transistor (TFT) in order to control the each pixels. Even if the field effect mobility of

amorphous silicon TFTs is less than 1 cm^2/Vs, it is high enough to operate the LCD because LCD is voltage controlled device. However, unlike with LCD, the AMOLED needs high field effect mobility because of current controlled device. So, polycrystalline silicon TFTs should be used for AMOLED display. Among the several method of crystallization, we used the Metal Induced Lateral Crystallization (MILC) for phase transform from amorphous to polycrystalline.

In the structure point of view, the LCD have to use bottom gate structure, because of light exposure from back side, so bottom electrode could block the light at the channel inversion layer. Otherwise, AMOLED have to use top gate structure, because of the crystallization process. The Excimer Laser Annealing (ELA) method is widely used for crystallization in commercial area. The bottom gate structure could not be used for ELA process, because of bottom electrode twisted and damaged. In order to use LCD manufacturing line for making AMOLED, polycrystalline silicon bottom gate structure must be fabricated. Therefore, in this experiment, we focus on the fabrication of bottom gate MILC polycrystalline silicon TFTs and its electrical properties.

The first step for bottom gate structure is the crystallization of Plasma Enhanced Chemical Vapor Deposition (PECVD) amorphous

silicon layer. Low Pressure Chemical Vapor Deposition (LPCVD) amorphous silicon layer could be crystallized in hydrogen ambient. However, the PECVD amorphous silicon layer could not be crystallized in hydrogen ambient annealing. The main difference between PECVD and LPCVD amorphous silicon layer is silicon hydrogen bonding configuration. Using Fourier Transform Infrared Spectroscopy (FT-IR), the silicon-hydrogen bonding configuration is measured. The PECVE has Si-H bonding and LPCVD has $Si-H_3$ bonding. The Si-H bonding is more stable than $Si-H_3$ bonding, so in furnace annealing LPCVD has faster crystallization ratio than PECVD layer. And the binding energy of silicon-hydrogen is lower than silicon-nickel (nickel metal is widely used for metal catalyst). In hydrogen ambient, the silicon atoms are easily connected with hydrogen, so the lateral growth rate is much slower in hydrogen ambient. So, lateral crystallization of PECVD silicon layer is obtained in vacuum condition furnace annealing.

We could fabricate the bottom gate MILC polycrystalline silicon TFTs using PECVD silicon layer in vacuum furnace annealing. However, because of metal silicide and metal contamination in silicon layer, relatively high leakage current level is main drawback of MILC polycrystalline silicon. In order to reduce the leakage current, we

applied two types of novel structure. The first one is called 'Overlap/off-set' structure. Overlap/off-set structure is describe that the vertically overlap region between bottom gate electrode and doped source/drain area. With this structure, the leakage current is decreased due to the depletion region under reverse bias gate voltage. Second structure is 'Direct/Indirect junction' which is represented the contact between doped source/drain and channel inversion layer. With indirect junction structure, the leakage current is reduced because of reduction of tunneling process. With direct junction structure both on current and off current is higher than indirect junction.

The mechanism of on current differs to that of leakage current. The on current is the result of carrier movement from source to drain passing by the channel inversion layers. And the leakage current is also the flow of carriers, but the carriers are generated not only from the source or drain region but also from defect states such as the metal silicide defect center. Normally, the leakage current occurs by three types of mechanisms: thermal activation, generation from the defect center in the middle of the band gap, and tunneling. With wide depletion region, the tunneling current is reduce mainly. In conclusion, in this research, we could fabricate the bottom gate structure MILC

polycrystalline silicon TFTs and applied novel structure for reducing leakage current which is called ‘overlap/off-set’ and ‘direct/indirect junction’ structure.

Keyword: Metal Induce lateral Crystallization, Thin Film Transistor, Bottom Gate Structure, Field Effect mobility.

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Figure 6-4 Levinson & Proano method to calculate trap state density (Nt) from the current-voltage characteristics

Chapter 1

Introduction of Display

1.1 Cathode Ray Tube (CRT)

The Cathode Ray Tube (CRT) is a display device with vacuum tube, more than one electron gun and a phosphorescent panel. When the electron guns emit the electron to the phosphorescent panel, image is displayed on the screen. The cathode ray is discovered by Johann Hittorf in 1876. He investigate that from the cathode (negative electrode), some unknown rays were emitted, indicating the rays were traveling in vacuum tube. In 1890, Arthur Schuster demonstrated cathode rays could be deflected by electric fields, and William Crookes showed they could be deflected by magnetic fields. The CRT used a heavy and large box shape modules because it need

relatively long distance for electron gun emitting. For safety reason, the front screen is made of thick glass substrate to block the electron emission. Before 2000s, CRT is main stream of display market, even if the heavy frame and large space charging. Since 2000s late, the main stream of display is move from CTR to Flat Panel Display (FPD) such as Liquid Crystal Display (LCD) and Plasma Display Panel (PDP) because of lower manufacturing cost and power consumption, and less weigh and bulk. Because of electron guns, CRT has area limitation.

1.2 Flat Panel Display (FPD)

The Flat Panel display (FPD) is viewing devices using thin substrate and thin film technology in order to reduce device thickness and weight. There are two kinds of devices of FPD, volatile and static. The volatile display need the thin film transistors which could maintain pixel current and voltage, and refresh the pixel capacitance during each frame. So volatile display need power source in operation. Otherwise, Static FPD is remain display image and text on the screen even if the power is off.

1.2.1 Liquid Crystal Display (LCD)

A LCD is one on the FDP device and volatile display. The LCD is not a self-emitting devices, so LCD need light source which is called back light unit [1.1-1.4]. The most widely used light source as a back light unit is cold cathode fluorescent lamp [1.5- 1.7], and now light emitting diode is also used for reducing power consumption [1.8]. LCD have replaced the heavy, bulky CRT display in almost application such as television, mobile display, computer monitor and aircraft. LCD screens are available in a wide area of screen size than CRT. The main drawback of CRT and PDP is image burn-in problem which is fixed image on a screen for a longtime exposed. In LCD screen, it is free from burn-in problem because LCD to not use the electron gun and phosphorescent light emission. In basically, LCD is consisted of two glass substrate, front substrate and back plane. First, in font substrate, color filter is deposited on the glass. LCD is not a self-emitting devices, so it need a light source, called back light unit. The back light unit is white light source. In order to describe image and motion, red, green and blue color is need. On the back plan there

are thin film transistors (TFT). Each pixel need at least one transistor to operate image presentation. Each pixel of an LCD typically consists of a layer of molecules aligned between two ITO electrodes [1.9], and two polarizing filters (parallel and perpendicular), the axes of transmission of which are (in most of the cases) perpendicular to each other. Without the liquid crystal between the polarizing filters, light passing through the first filter would be blocked by the second (crossed) polarizer. Before an electric field is applied, the orientation of the liquid-crystal molecules is determined by the alignment at the surfaces of electrodes. Three kind of liquid crystals are used for manufacturing LCD devices, Twisted Nematic [1.10], In Plain Switching [1.11] and Vertical Alignment [1.12]. Twisted Nematic (TN) material is used in LCD at fist. The rod shape LC is twisted between front and back substrate. This TN mode is low cost fabrication process and has low power consumption because of simple operation. However, it has low viewing angle. Because of low viewing angle properties, it could not be used for large area display. Second one is Vertical Alignment (VA) panel. This VA display is investigated due to the disadvantage of TN panel. With VA pane, Good contrast ratio is obtained which means

deeper black is represented than TN mode. However, late response time is main problem, so it is not suitable for motion video. And other problem is 'MURA' which is caused by touch screen with finger [1.13], especially in mobile smartphone. Touch the screen is main communication method to use smartphone, but with VA mode, it induce ‘MURA’ problem. The last one mode is In Plain Switching (IPS) panel. With IPS panel Mura problem is not observed and good viewing angle and good contrast ratio is also obtained.

1.2.2 Active Matrix Organic Light Emitting Diode (AMOLED)

An organic light-emitting diode (OLED) is a light-emitting diode (LED) in which the light emitting layer is a layer of organic compound that emits light in response to an electrical carrier flow. OLEDs are used to create digital displays in devices such as television screens, and mobile phones. Hong Kong-born American physical chemist Ching W. Tang and his co-worker Steven Van Slyke at Eastman Kodak fabricate the first practical OLED device in 1987 [1.14]. This

was a pioneer for the display technology. This device used a two-layer structure with separate hole transporting and electron transporting layers [1.15]. The recombination and light emission occurred in the organic layer at the between of two transporting layer. This resulted in a reduction in operating voltage and improvements in efficiency. A typical OLED is composed of a layer of organic materials on a glass substrate. These organic materials have conductivity levels ranging from insulators to conductors, considered organic semiconductors. The highest occupied and lowest unoccupied molecular orbitals (HOMO and LUMO) of organic semiconductors are matched to the valence and conduction bands of inorganic semiconductors. During display operation, a voltage is applied to the OLED. An electrons flows throughout the device from cathode to anode, as electrons are injected into the LUMO of the organic layer at the cathode and withdrawn from the HOMO at the anode. Electrostatic forces make the electrons and the holes towards each other and they recombine forming an exciton which means the state of the electrons and holes pair. So the frequency of this radiation (color of the light) depends on the band gap of the material, in this case the difference in energy between the HOMO and LUMO.

Chapter 2

Background and Motivation

2.1 Low Temperature Polycrystalline Silicon (LTPS)

The polycrystalline silicon layer is considered as an important materials in semiconductor area since 1970s [2.1, 2.2]. In 1970s metal-insulator-semiconductor structure [2.3] is proposed and many research group have investigated this structure as display and integrated circuit [2.4, 2.5]. This polycrystalline silicon layer used for electrode if it has low enough resistivity comparing with metal layer, and used for silicon active layer. The polycrystalline silicon has several advantages when it is used for active layer, such as low cost process, large area substrate. Therefore polycrystalline silicon is widely used in semiconductor industries. Here, the most important

step and fabrication process is crystallization. In display industries, thin film transistors (TFTs) is fabricated using polycrystalline silicon especially Active Matrix Organic Light Emitting Diode (AMOLED) [2.6−2.9]. The main difference of Liquid Crystal Display (LCD) [2.10, 2.11] and AMOLED is the operation ways. LCD is voltage driving device and AMOLED is current driving device. TFTs in LCD device act as a switching element which control the on/off state of each pixel. However, in AMOLED TFT as a driving element, so it need high field effect mobility. In case of amorphous silicon TFTs, field effect mobility is lower than 1 cm^2/Vs, otherwise, in case of polycrystalline silicon TFTs, it has high enough field effect mobility (20 ~ 200 cm^2/Vs) [2.12]. In order to fabricate polycrystalline silicon TFTs on the glass substrate (Eagle XG, Corning Inc.), low temperature crystallization process is needed because of melting point of glass substrate is around 600 ℃ which is called Low Temperature Polycrystalline Silicon (LTPS).

In figure 2−1, several LTPS methods is presented. First one is Solid Phase Crystallization (SPC) [2.13, 2.14]. SPC has many advantages, such as low−cost process and easy to apply large area application. However, relatively high fabrication temperature and

longtime step (about more 12 hours) is main drawback of SPC. It is hard to apply to display devices because display mush use glass substrate. Second one is Excimer Laser Annealing process (ELA) [2.15, 2.16]. This ELA is used for crystallization in manufacturing of AMOLED display in commercial area. ELA has been widely used in industry, but there are still many serious disadvantages to doing so. For instance, ELA uses an expensive XeCl laser that results in a high manufacturing cost for AMOLED displays, and the laser scanning process results in non-uniformity due to the liquid-solid phase transformation. In terms of the structure, ELA cannot produce a bottom gate structure that is common in Liquid Crystal Display (LCD) devices because metal gate damage is caused during laser scanning. In our research group, we have investigated the production of bottom gate polycrystalline silicon TFTs for use in LCD product lines without the need to construct new facilities. SPC and ELA both have critical problems in producing commercial devices due to the high crystallization temperature and the laser scanning process that each respectively require. In 1996, the MILC process was introduced as a crystallization method that uses a metal catalyst at a temperature below 550 ℃ [2.17, 2.18]. MILC has advantages in overcoming the

limitations of SPC and ELA.

2.1.1 Metal Induced Lateral Crystallization (MILC)

The crystallization rate is affected by metal catalyst. With metal catalyst, crystallization temperature become lower, and this is call MIC. This MIC is observed from many metal species such as Au, Ni, Al, Sb, In, Pb, and Ti [2.19−2.24]. Among these metal, Ni, Pb and Ti make formation of metal−silicide compounds. There are much of investigation of crystallization rate and temperature with Ni, Pb and Ti metal catalysts. However, metal silicide in silicon bulk layer is considered as an impurities which is caused trap state in band diagram, and this impurities induced degradation of electrical properties [2.25, 2.26]. In order to reduce the metal contamination in silicon layer, our group applied new crystallization method called MILC. Especially, nickel metal is widely used for MILC because the lateral growth of nickel silicide is faster than other metal catalysts. In figure 2−2 schematic image of MIC and MILC process with nickel metal. The amorphous silicon layer under nickel thin layer is crystallized by MIC phenomenon. The nickel silicide is spread from

polycrystalline area to amorphous silicon area. This is lateral growth, called MILC. In SEM image in figure 2-2 shows the diffusion of nickel silicide. In figure 2-3, schematic image of MILC mechanism is described. The relatively week bonding of silicon atoms in amorphous silicon layer breaks if the nickel layer is deposited by sputtering. This separated silicon atoms makes nickel silicide molecules at the interface of nickel and amorphous silicon. In annealing process, nickel metal atoms move using 'hopping' mechanism and remained space is called nickel vacancy. This silicon atoms with nickel vacancy has similar lattice length with crystal silicon lattice. Therefore this remained silicon fairs make crystal silicon phase in furnace annealing. The driving force of this MILC process is related with molar free energy. Figure 2-4 shows schematic equilibrium molar free energy diagram as a function of atomic percentage with nickel silicon contact [2.27]. The $NiSi_2$ formation has lowest molar free energy which means in MILC process, nickel and silicon atoms are existed this $NiSi_2$ form.

2.2 Material Properties of Amorphous and Polycrystalline Silicon

The disorder of atomic structure is one of the important properties that distinguishes polycrystalline from amorphous silicon layer. Order of atomic structure, celled periodicity is key point of theory of semiconductor. Because of this periodicity, the function of electrons and holes are calculated with quantum state of each atoms momentum, which is called Bloch's theory. However, disorder of atomic structure need different point of view. Figure 2-5 shows normalized pair distribution function of crystal state, amorphous state and gas state as a function of pair separation [2.28]. In free gas state, distribution of neighbor atoms are existed randomly, which means there is no order and periodicity in gas state. However, in crystal state, the distribution of neighbor atoms are fixed at certain place. The amorphous state has both characteristics. In short range order, atoms are arranged in periodicity. But in long range order, it looks like gas state which has disorder atomic structure.

Figure 2-6 shows density of state distribution of amorphous silicon

(solid line) and crystal silicon (dash line). This represent the band diagram, the band tail, and the defect state in the band gap. The perfect crystal state shows conduction band and valence band which is defined by quantum physics. The amorphous silicon has short range order, so it has similar band diagrams which means that amorphous silicon has conduction band and valence band. Otherwise, it has long range disorder, so there is band tail state which is described as extended state into the forbidden band gap area.

This tail state modify the edge of conduction and valence band. And there is defect state in forbidden region (in band gap region), because of dangling bonds. In case of crystal silicon, one silicon atom is connected with other four silicon atoms and hydrogen atoms especially at the surface. But in case of amorphous silicon, there is vacancy defects which is called dangling bonds. This dangling bonds described that no atomic bond with silicon atoms. These defect state define the electrical properties of silicon layer by controlling trap state.

2.3 Electrical Properties Polycrystalline Silicon Thin Films Transistors

2.3.1 Mobility

The carrier mobility of field effect transistor (FET) is called field effect mobility. Field effect mobility is measured in two ways, saturation mode and linear mode.

$$I_D = \mu_{FET} C_{ox} \frac{W}{L} [(V_G - V_{TH}) V_D]$$

The transconductance is defined as

$$g_m = \frac{\partial I_d}{\partial V_G}$$

Therefore, the field effect mobility is defined as

$$\mu_{FET} = \frac{L}{C_{ox} W V_D} g_m$$

2.3.2Threshold Voltage (V_{TH})

In order to calculate the threshold voltage (V_{TH}), non-zero flat bond voltage is considered, at first. This non-zero flat band voltage is caused from fixed oxide charge (Q_f) and work function difference (ψ_{ms}) between the gate material and the semiconductor. Threshold voltage is gate voltage which induce a channel inversion layer in semiconductor material.

$$V_{TH} = V_{FB} + 2\varphi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\varphi_B)}}{C_{ox}} = \left(\varphi_{ms} - \frac{Q_f}{C_{ox}}\right) + 2\varphi_B + \frac{\sqrt{4\varepsilon_s q N_A \varphi_B}}{C_{ox}}$$

2.3.3 Sub-threshold Slope

Sub-threshold slope is the parameter which could define how sharply the transistor is turn-on by gate voltage sweep. This sub-threshold slope is defined as the gate voltage need to induce a drain-current change of one order of magnitude.

$$Slope = \frac{d(lnI_d)}{dV_G(ln10)}$$

2.3.4 Leakage current

The mechanism of on current differs to that of leakage current. The on current is the result of carrier movement from source to drain passing by the channel inversion layers. And the leakage current is also the flow of carriers, but the carriers are generated not only from the source or drain region but also from defect states such as the metal silicide defect center [2.29]. Normally, the leakage current occurs by three types of mechanisms: thermal activation, generation from the defect center in the middle of the band gap, and tunneling. Figure 2-7 shows each mechanism of leakage current in MILC TFTs using energy band diagram. The Lightly Doped Drain (LDD) structure is typically applied to reduce the leakage current and pinning current level. The intrinsic layer between the doped source/drain region and the gate insulator on the IJ-TFTs acts similar to the LDD structures, so the leakage current and pinning current is decreased.

2.4 Structure of Thin Film Transistors (Top gate vs Bottom gate)

2.4.1 Top Gate Structure MILC Thin Film Transistor

Figure 2-8 show fabrication flow of top gate MILC TFTs. Each fabrication step is explain below. Step (1) show glass substrate and buffer layer. The corning Eagle XG glass is used as substrate, the thickness is 0.64mm. 300 nm of silicon oxide is deposited on the glass substrate for buffer layer using Plasma Enhanced Chemical Vaper Deposition (PECVD) at 350 °C with SiH_4, Ar and N_2O gas mixture. Step (2) shows amorphous silicon layer deposition. The amorphous silicon layer is deposited by Low Pressure Chemical vapor Deposition (LPCVD) at 550 °C. Step (3) is nickel deposition using sputter at room temperature. Step (4) is nickel remove and annealing. Nickel is removed by H_2SO_4 solution in order to reduce nickel contamination in crystallized silicon layer. Furnace annealing at 550 °C during 2 hours in hydrogen ambient for MILC. Step (5) is gate insulator deposition. Before gate insulator deposition, RCA cleaning is done foe remove

particles and native oxide foe thermal annealing. 100 nm of silicon nitride is deposited using PECVD at 350 °C with SIH_4, NH_3 and Ar gas mixture. Step (6) is metal deposition and metal etching. MoW metal is used for electrode using sputter at 300 °C. Gate electrode is etched by photolithography and wet etching system using H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchant. Step (7) is Ion Mass Doping (IMD) and activation process. We used IMD for source/drain doping. And activation process is proceeded by furnace annealing in hydrogen ambient during 1 hour. All of the fabrication processes were carried out in a 1000-class clean room.

2.4.2 Bottom Gate Structure MILC Thin Film Transistor

Figure 2-9 show fabrication flow of bottom gate MILC TFTs. Each fabrication step is explain below. Step (1) is glass substrate, buffer and gate electrode. The corning Eagle XG glass is used as substrate, the thickness is 0.64mm. 300 nm of silicon oxide is deposited on the glass substrate for buffer layer using PECVD at 350 °C with SiH_4, Ar and N_2O gas mixture. 300 nm MoW is deposited as gate electrode at 300 °C using sputter. Gate electrode is etched by photolithography

and wet etching system using H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchant. Step (2) is gate insulator deposition. 100 nm of silicon nitride is deposited using PECVD at 350 °C with SIH_4, NH_3 and Ar gas mixture. Step (3) is amorphous silicon deposition. Unlike top gate structure, bottom gate need PECVD amorphous silicon layer because of LPCVD thermal damage to gate electrode and in-situ process. After gate insulator deposition, amorphous silicon layer is deposited using PECVD without break vacuum system. Step (4) is etch stopper deposition. 200 nm of silicon oxide is also deposited using PECVD as etch stopper. Etch stopper is etched by etch etching system using buffer oxide etchant. Step (5) is p+ amorphous silicon layer deposition and separation step. A p+ amorphous silicon layer is also deposited sing PECVD at 350 °C. Step (6) is nickel deposition, nickel remove and annealing. 5 nm nickel layer is deposited using sputter. Nickel is removed by H_2SO_4 solution in order to reduce nickel contamination in crystallized silicon layer. Two kinds of annealing is done, first one is crystallization. Unlike LPCVD, PECVD amorphous silicon layer is annealed in vacuum condition for crystallization. We will explain this phenomenon in chapter 3. Second one is hydrogenation which is annealed in hydrogen ambient during 1 hour.

2.5 motivation of this thesis

Nowadays ELA crystallization method is widely used for fabrication of AMOLED display devise. Because of this ELA method, there are critical limitation such as TFT structure. ELA method use high energy XeCl laser exposure during crystallization. In case of top gate structure, ELA method could be used for crystallization because only silicon layer is deposited on substrate. However, in case of bottom gate structure, there are other layer under amorphous silicon layer such as gate electrode and gate insulator. During high energy lase exposure, metal gate electrode get thermal damage and it cause metal twisting and crack. Therefore, it is hard to fabricate bottom gate TFT AMOLED using ELA method.

As we mention above, main stream of display market is move from LCD to AMOLED. LCD used amorphous silicon TFT with bottom gate structure. Amorphous silicon TFT is used for LCD because it' s electrical properties is high enough to operate LCD display. LCD is not self-emitting device, which means it have to use other light source, called Back Light Unit. Amorphous silicon is unstable material called meta-stable material. Because of that, photo-current is

generated when the amorphous silicon is exposed under light. This is main reason of degradation of electrical properties. So LCD must use bottom gate structure and all established manufacturing line is existed foe bottom gate structure. If we could fabricate AMOLED with bottom gate structure using MILC crystallization method, all the established manufacturing line is used for AMOLED.

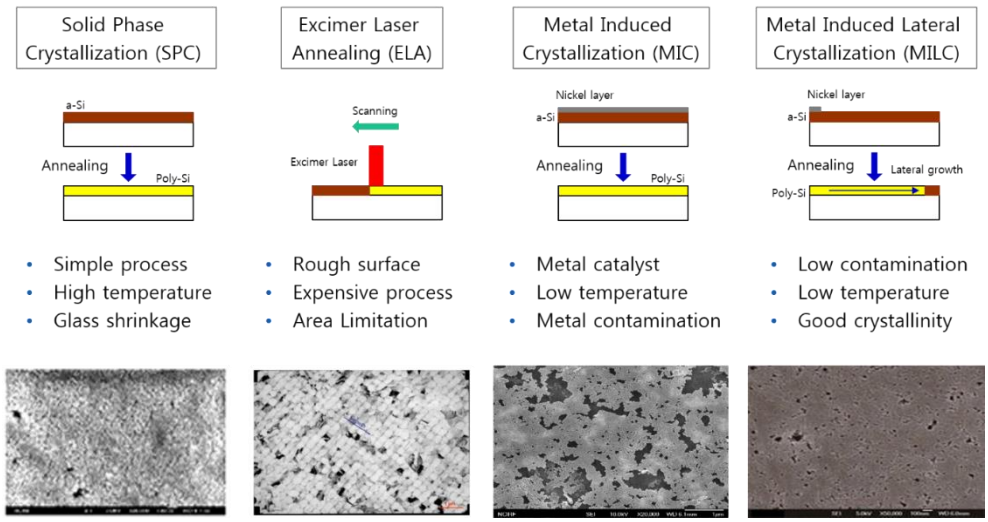


Figure 2-1 schematic image of crystallization methods (1) SPC, (2) ELA, (3) MIC, (4) MILC and its properties, SEM images.

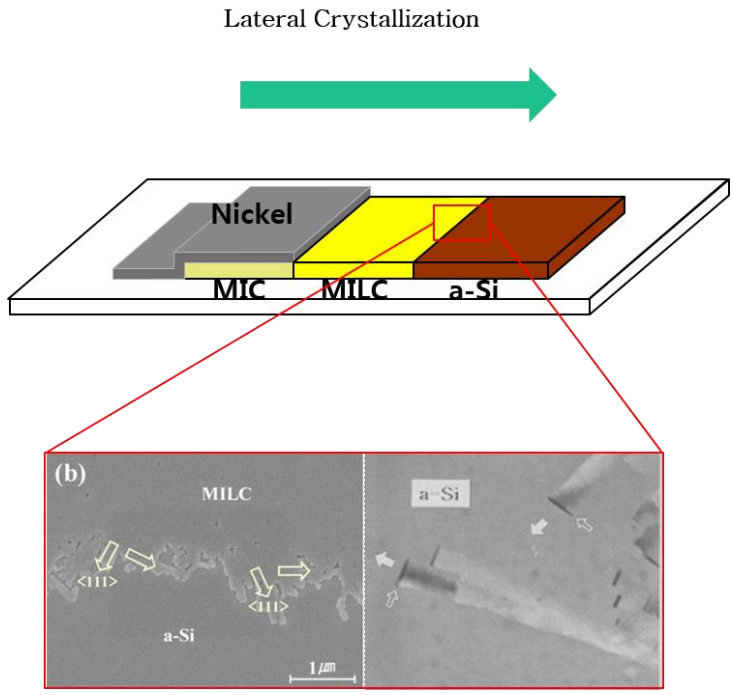


Figure 2-2 schematic image of crystallization mechanism of MILC and SEM image at the interface of polycrystalline silicon and amorphous silicon.

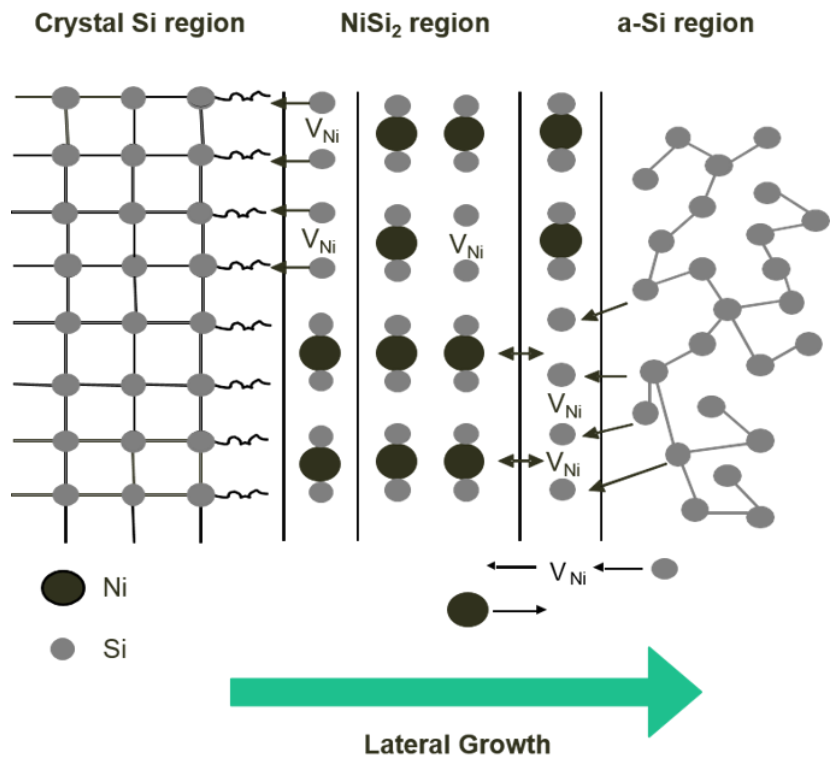


Figure 2-3 Detail mechanism of MILC using concept of nickel silicide compounds.

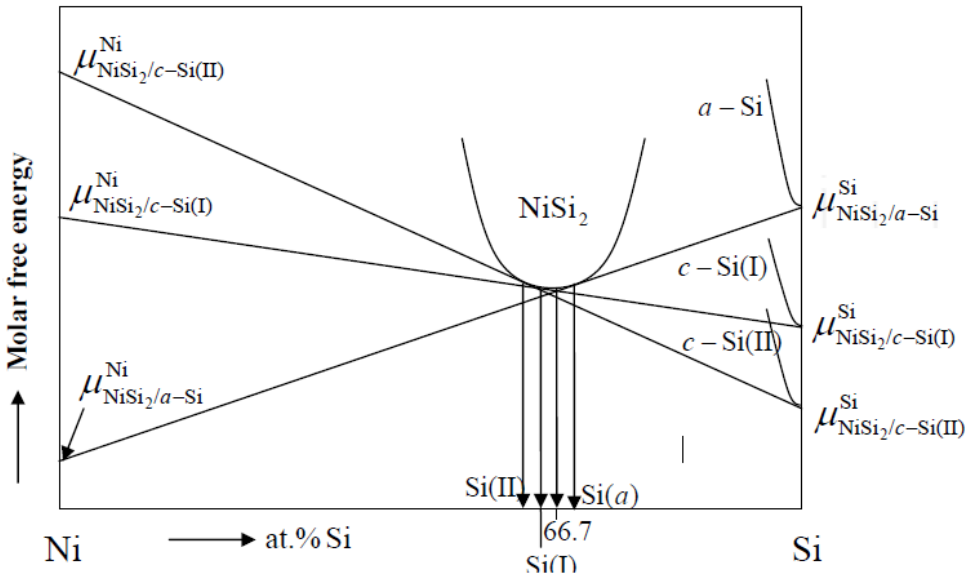


Figure 2-4 Schematic equilibrium molar free energy diagram for $NiSi_2$ in contact with a-Si, C-Si [2.27].

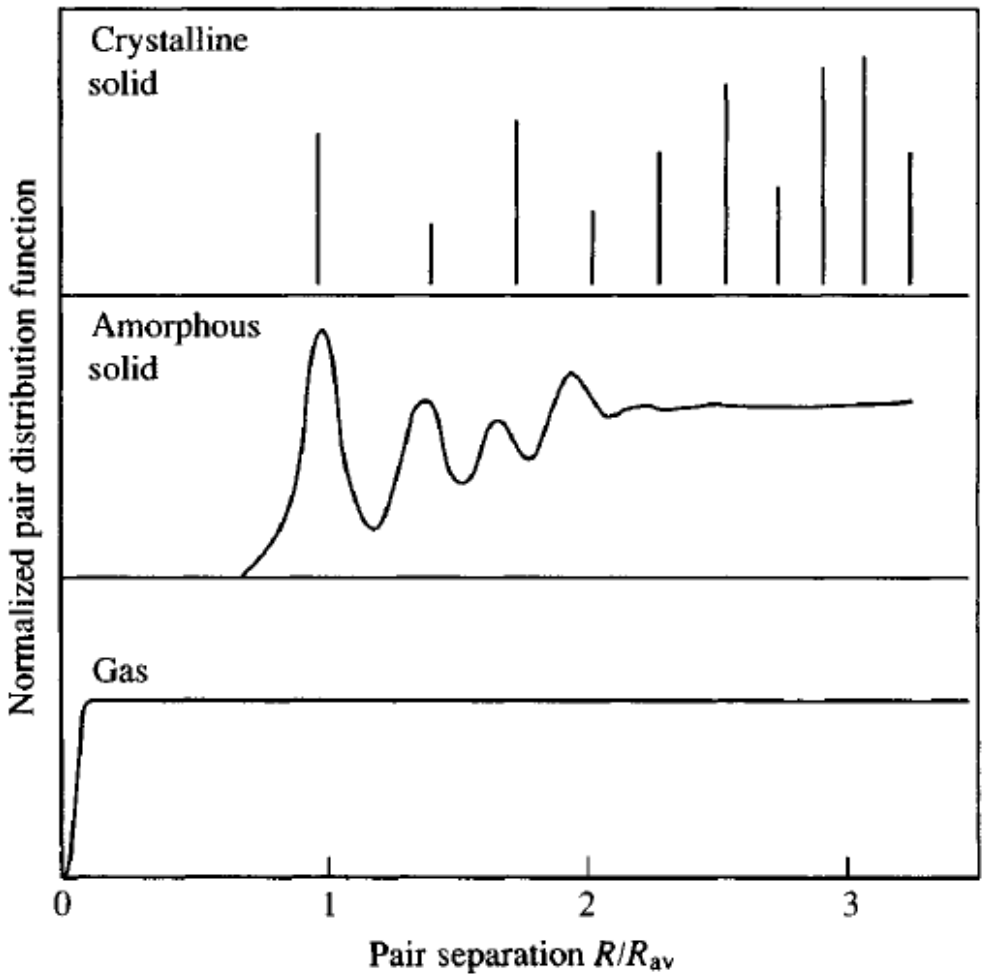


Figure 2-5 Schematic diagram of the atom pair distribution functions for a crystalline and amorphous solid and a gas, scaled to the average separation of nearest neighbor atoms, R_{av}, showing the different degree of structural order [2.28].

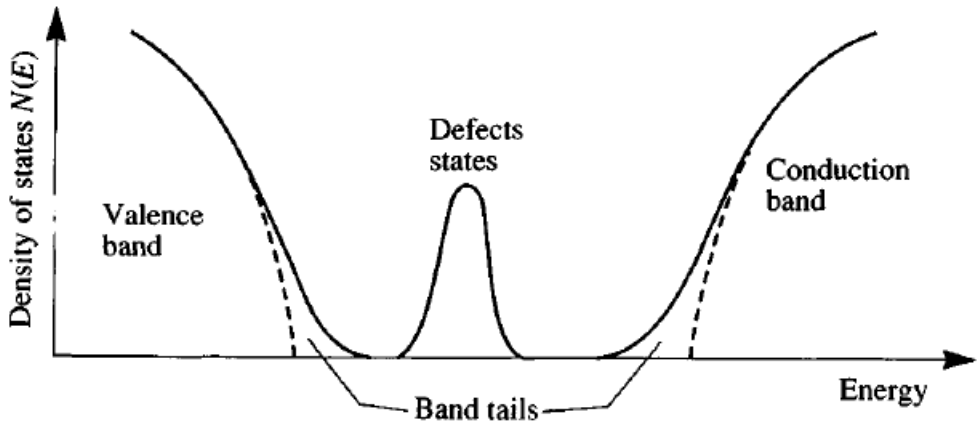


Figure 2-6 Schematic density of states distribution for an amorphous semiconductor showing the bands, the band tails, and the defect states in the band gap. The dashed curves are the equivalent density of states in a crystal [2.28].

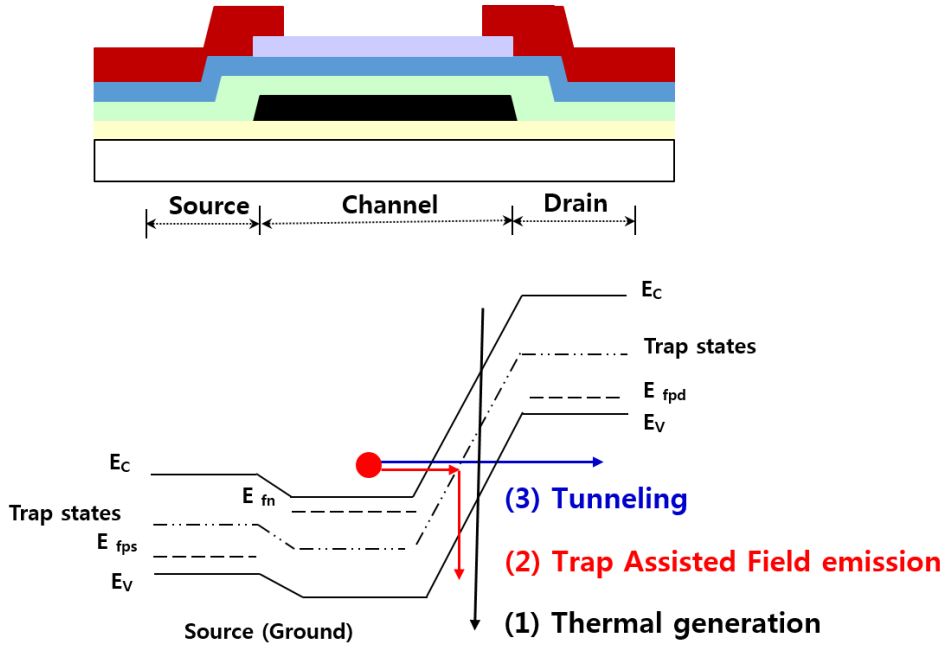
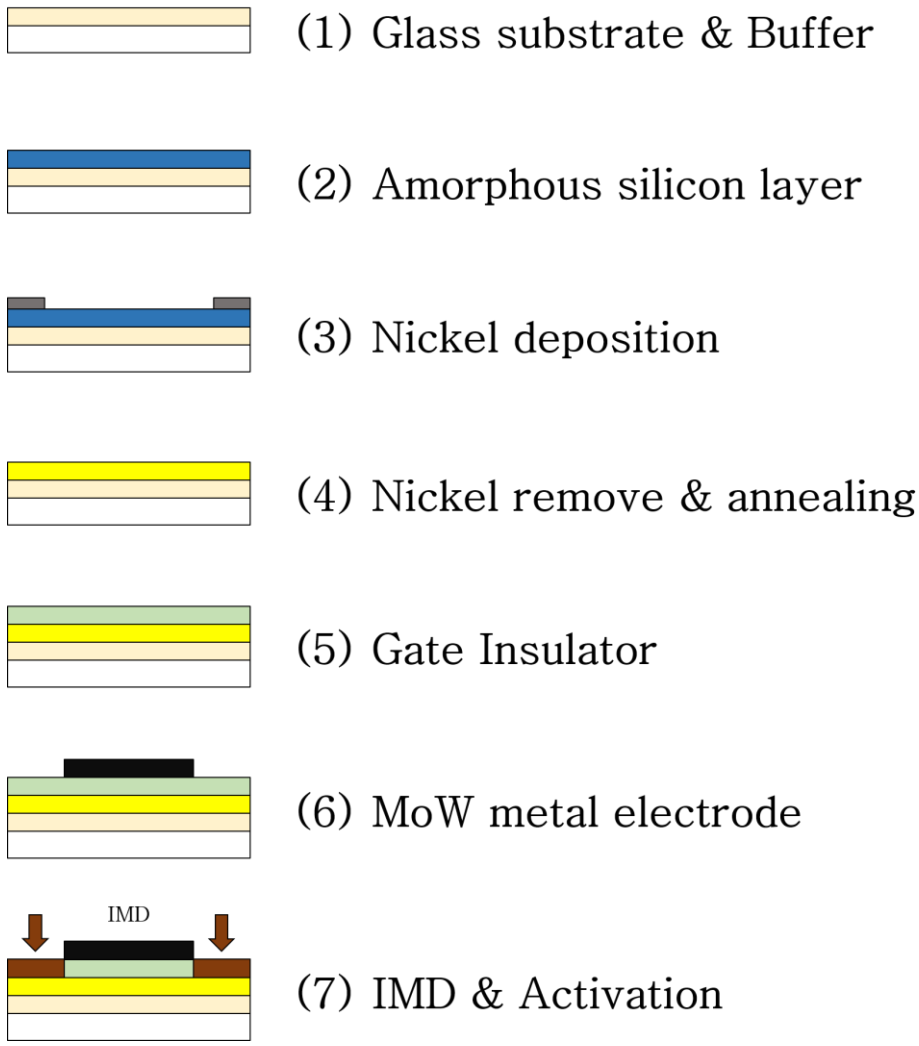
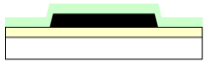


Figure 2-7 Schematic band diagram of mechanism of MILC TFTs leakage current



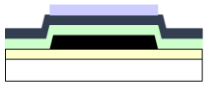
2-8 schematic fabrication flow of top gate MILC polycrystalline TFTs

(1) Glass substrate & Buffer & Electrode

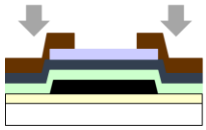


(2) Gate Insulator

(3) Amorphous silicon



(4) Etch Stopper



(5) P+ silicon & separation

(6) Nickel deposition & remove & annealing

2-9 schematic fabrication flow of bottom gate MILC polycrystalline TFTs

Chapter 3

Crystallization of Low Pressure Chemical Vapor Deposition and Plasma Enhanced Chemical Vapor Deposition Amorphous Silicon Layer

A polycrystalline silicon layer which is crystallized by metal induced crystallization (MIC) and Metal Induced Lateral Crystallization (MILC) methods is investigated for electronic devices such as thin film transistors and solar cells. Until now, the crystallization mechanism of MIC and MILC has not been understood clearly. In this research, we deposited amorphous silicon using different deposition processes: low pressure chemical vapor deposition and plasma enhanced chemical deposition. Also, in the crystallization process, we used two types of annealing conditions: hydrogen ambient and vacuum ambient. Among the four samples analyzed, the fastest MIC and MILC rate was observed for the sample of low pressure chemical vapor deposition

process in vacuum annealing crystallization. We assume that the gap between low pressure chemical vapor deposition and plasma enhanced chemical vapor deposition is due to the silicon hydrogen bonding configuration. Therefore, Fourier Transform Infrared spectroscopy is used to confirm the difference in the silicon hydrogen bonding between samples. From this result, we determined that plasma enhanced chemical vapor deposition provides more stable silicon–hydrogen bonding than low pressure chemical vapor deposition. This bonding configuration can be related with crystal growth rate.

3.1 introduction

Many different studies have been performed to crystallize a thin film amorphous silicon layer to polycrystalline silicon using Metal Induced Crystallization (MIC) and Metal Induced Lateral Crystallization (MILC) [3.1−3.5]. Unlike with other crystallization methods such as Solid Phase Crystallization (SPC) [3.6, 3.7] and Excimer Laser Annealing (ELA) [3.8], these MIC and MILC methods need a metal catalyst such as nickel or platinum to overcome the potential energy for changing the phase from amorphous to polycrystalline. Compared with amorphous silicon in thin film transistor (TFT) devices, MIC and MILC polycrystalline silicon layers as channel regions have greater field effect mobility and electrical performance [3.9]. However, the relatively high leakage current is the most significant disadvantage, and is caused by the metal silicide defect state which is formed during crystallization [3.10−3.12]. Therefore, our research group previously focused on how to decrease the leakage current with an MIC or MILC polycrystalline silicon layer [3.13, 3.14] caused by metal silicide defect [3.15−3.17]. However, in this report, we concentrate on the role of the deposition method of thin film

amorphous silicon, as it is very important in determining the crystallization and crystallization growth rate. Two approaches have been used to produce a thin film amorphous silicon layer: Plasma Enhanced Chemical Vapor Deposition (PECVD) and Low Pressure Chemical Vapor Deposition (LPCVD). Our previous TFTs is fabricate using LPCVD silicon layer, because PECVD silicon layer cannot be crystallized under hydrogen ambient annealing. So in this experiment, we investigate relationship between annealing condition and crystallization rate with deposition system to figure out why PECVD silicon layer cannot be laterally crystallized in hydrogen ambient.

3.2 Experiment

Figure 1 shows schematic image of this experiment process and structure. A 100 nm amorphous silicon layers used in this research is deposited using PECVD and LPCVD on the Eagle XG glass substrate. PECVD use SiH_4 gas at 350 ℃, process pressure is 300 mTorr, power is 15 W and deposition rate is 10 nm/min. LPCVD also use SiH_4 gas at 500 ℃ and deposition rate is 2 nm/min. Figure 3-1 (a) shows specific pattern which is described with two pads and one channel connecting two pads is defined photolithography. The channel region length is 80 ㎛. For etching, reactive ion etching (RIE) equipment is used with O_2 and SF_6 gas mixture at room temperature. In order to phase transform from amorphous silicon to polycrystalline, metal induced crystallization (MIC) and metal induced lateral crystallization (MILC) is used. A 5nm nickel metal layer is deposited on amorphous silicon layer using sputter at room temperature for MIC and MILC. Before nickel metal deposition, native oxide on amorphous silicon surface is removed by HF cleaning for making nickel silicide configuration. We could see nickel patterning on figure 3-1 (b). Length between nickel pad is 150 ㎛. On right side pad,

nickel metal is deposited entire area, otherwise, on left side pad just half area is covered by nickel metal layer. For crystallization, 4 kinds of furnace thermal annealing is applied; 500 ℃ hydrogen ambient, 580 ℃ hydrogen ambient, 500 ℃ vacuum ambient and 580 ℃ vacuum ambient. The entire fabrication process was carried out in a 1000-class clean room.

3.3 Result and discussion

Figure 3-2 and 3-4 shows an optical microscope image of the MIC and MILC results in hydrogen ambient annealing in a furnace. It shows the results of PECVD and LPCVD, respectively. As we mention above, a 5 nm nickel layer is deposited in half of the region of the left side and in the full region of the right side. Therefore, not only MIC but also lateral crystallization could be observed in one sample. MIC occurs at this nickel pad region and lateral crystallization spreads from the nickel pad to the middle bridge region. At 500 ℃, MILC phenomenon is not observed, which means this temperature isn't high enough to induce lateral crystallization. Otherwise, at 580 ℃, lateral crystallization is observed both PECVD and LPCVD case. Figure 3-3 and 3-5 show the optical microscope image of MIC and MILC in vacuum ambient furnace annealing. Figure 3-3 and 3-5 represent the result of PECVD and LPCVD, respectively, similar with figure 3-2 and 3-4. In vacuum ambient condition, MIC and lateral crystallization occur in both the PECVD and LPCVD silicon layers. However, the lateral crystallization speeds of the PECVD and LPCVD silicon layers differ somewhat. With the PECVD silicon layer, only a

small region of the lateral crystallization area was observed; on the other hand, with LPCVD, the rate of MILC is too fast, so that only the crystallized polycrystalline silicon layer is observed. From these results, we can conclude that the LPCVD silicon layer has a faster crystallization rate than the PECVD silicon layer. Also, in vacuum ambient condition, both the PECVD and LPCVD silicon layers have a faster crystallization rate than when in the hydrogen ambient condition.

Figure 3-6 shows the rate of lateral crystallization growth for all 4 samples. The squares represent the PECVD sample and the circles represent the LPCVD samples. The solid squares and circles represent samples with hydrogen ambient furnace annealing and the empty squares and circles represent samples with vacuum ambient furnace annealing. Regardless of temperature, the LPCVD sample in vacuum ambient annealing has the highest lateral crystallization rate and PECVD hydrogen has the lowest lateral crystallization rate. For example, in vacuum ambient condition, the LPCVD silicon samples have more than 75 μm at both 500 ° C and 580 ° C.

In order to determine the main difference between the PECVD and LPCVD silicon layers, we conducted measurements using Fourier

Transform Infrared (FT-IR) spectroscopy. Figure 3-7 shows the FT-IR analysis measurements of the PECVD and LPCVD amorphous silicon layers. In these measurements, we focus on the silicon hydrogen bonding in the amorphous silicon layer. The silicon hydrogen bonding normally appears in area of around 2000 ~ 2100 cm^{-1} in FT-IR measurement. The silicon hydrogen bonding configuration could affect the deposition of the hydrogenated amorphous silicon. For example, among the various types of silicon hydrogen bonding, Si-H bonding is more stable than $Si-H_2$ and $Si-H_3$ bonding because it has a higher binding energy. For the deposition temperature case of less than 300 ℃, the temperature is the main factor. Between 200 ℃ and 300 ℃, further Si-H bonding occurs in amorphous silicon due to the decomposition of $Si-H_2$ bonding by thermal energy. However, above 300 ℃, the temperature is no longer an important factor for the configuration of silicon hydrogen bonding. In this condition, the deposition method is the main aspect of silicon hydrogen bonding. In this research, PECVD is deposited at 350 ℃ and LPCVD is deposited at 550 ℃; the silicon hydrogen bonding configuration changes according to the deposition method, not according to temperature. In figure 4-7, the red line indicates the

FT−IR spectroscopy peak of amorphous silicon deposited by PECVD. This peak is located at 2000 cm^{-1}. The 2000 cm^{-1} peak represents the Si−H stretching bonding, which means one silicon atom connects with one hydrogen atom. The schematic molecular structure of the Si−H bonding can be observed adjacent to the PECVD peak. Otherwise, the black line refers to the FT−IR spectroscopy peak of the amorphous silicon deposited by LPCVD. This LPCVD TF−IR peak is located in the 2100 cm^{-1} ~ 2300 cm^{-1} region and could be de−convoluted with two peaks of 2150 cm^{-1} and 2250 cm^{-1}. As can be seen in figure 3−7, the first 2150 cm^{-1} peak (peak 1) represents the $Si-H_3$ structure and the 2250 cm^{-1} peak (peak 2) represents the oxidized Si−H (O−Si−H) bonding [3.18−3.20].]. The center of peak 1 is 2157 cm^{-1} and the Full Width at Half Maximum (FWHM) is 132.8. The relative peak area is 47.5 % and peak height is 32. The center of peak 2 is 2251 cm^{-1} and the FWHM is 51.8. The relative peak area is 52.49 % and peak height is 91.

MIC and MILC are novel crystallization methods in which a metal catalyst such as nickel or platinum is used. In the MIC and MILC processes, the metal catalyst breaks down the amorphous silicon and rearranges the polycrystalline silicon phase. Therefore, the break

down ratio and speed are important factors of the MIC and MILC speeds. The results shown in figure 3-6 illustrate that the PECVD silicon samples have low MILC speed, which means it is more difficult to break down PECVD amorphous silicon atoms configuration than those of LPCVD. From this result, we assumed that the PECVD amorphous silicon samples have more stable binding energy than the LPCVD sample. Also, the result shown figure 3-7 supports this assumption. As mentioned above, the 2000 cm^{-1} peak is more stable than the 2100~2200 cm^{-1} peak. The general silicon hydrogen bonding configuration is represented in table 3-1, In a vacuum condition, the rate of MILC is faster than in a hydrogen condition. During MIC and MILC, the decomposed silicon atoms need to make $NiSi_2$ molecules for induce crystallization. However, in the hydrogen annealing condition, making Si-H bonding is easier than Ni-Si bonding; the decomposed silicon atoms therefore carry out further Si-H bonding. Figure 3-8 shows illustration of metal induced crystallization, especially in vacuum ambient (a) and in hydrogen ambient condition (b). During metal induced crystallization, amorphous silicon bonding which has relatively week bonding than crystal silicon bonding is broke easy during furnace annealing. In case

of vacuum annealing, in figure 3-8 (a), decomposed silicon atoms are commonly connected with nickel atoms to make nickel silicide ($Ni-Si_2$). However in hydrogen ambient annealing, in figure 3-8 (b), decomposed silicon atoms make silicon hydrogen bonding because the binding energy of Si-H is lower than Si-Ni bonding. (H-Si: 2.17 eV, $Ni-Si_2$: 3.15 eV). So, if there atmosphere is hydrogen rich condition during annealing, silicon dangling bonds make silicon hydrogen bonding more frequently than silicon nickel bonding. At the high temperature annealing, silicon-hydrogen bonding breaks easier than silicon-nickel bonding, because the dissociation energy of silicon-nickel is 3.37 eV and silicon hydrogen is 3.03 eV. After silicon-hydrogen bonding broken, silicon-nickel bonding is formed and this bonding is more stable than silicon-hydrogen bonding. Therefore, the crystallization rate in hydrogen annealing is slower than in vacuum condition. We could therefore conclude that LPCVD in vacuum ambient annealing condition has the fastest MILC.

3.4 summary

We investigated polycrystalline silicon layers for electronic devices such as TFTs. In this research, we focus on the MIC and MILC rates in hydrogen and vacuum ambient conditions with two different samples: PECVD and LPCVD. The results showed that LPCVD in vacuum condition has the fastest crystallization rate. In the amorphous silicon layer, many types of Si−H bonding occur, and the PECVD and LPCVD samples have different types of bonding; in the PECVD, the Si−H bonding is dominant and in LPCVD, the Si−H3 bonding is dominant. Because of this distinction, the MIC and MILC rates differ somewhat.

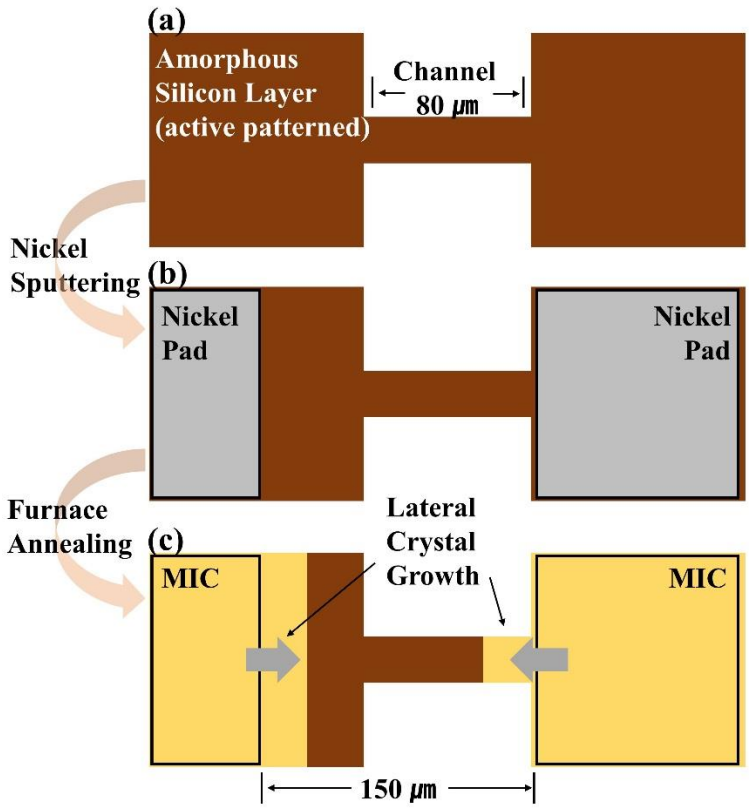


Figure 3-1 (a) schematic image of amorphous silicon layer and tis pattern, (b) nickel deposition pattern, (c) result of furnace annealing for 1 hours

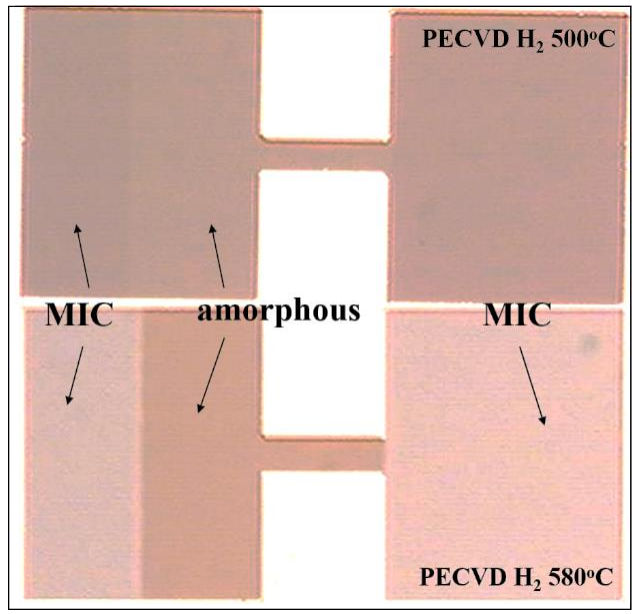


Figure 3-2 PECVD amorphous silicon layer annealed (500 ℃, 580 ℃) in hydrogen ambient

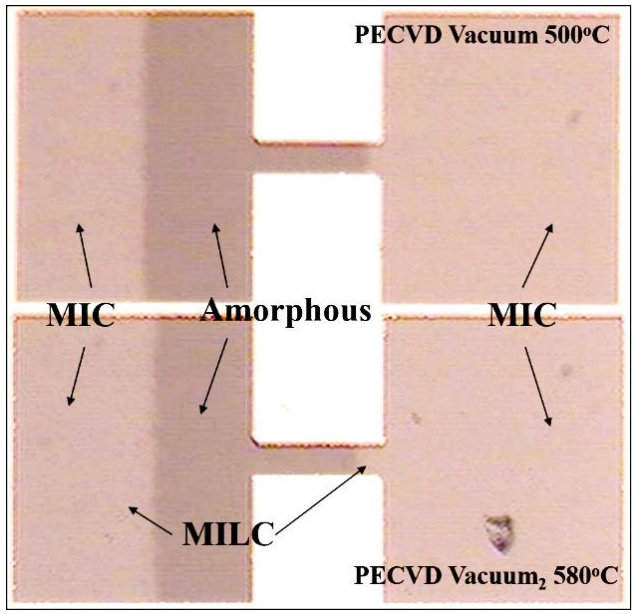


Figure 3-3 PECVD amorphous silicon layer annealed (500 ℃, 580 ℃) in vacuum condition

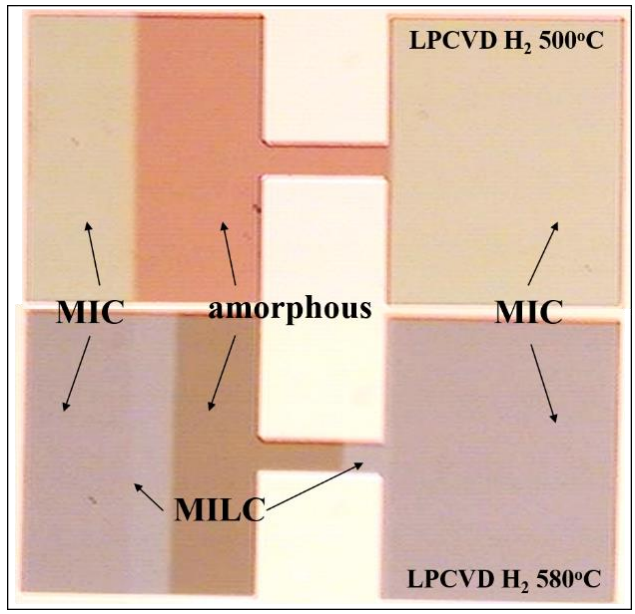


Figure 3-4 LPCVD amorphous silicon layer annealed (500 ℃, 580 ℃) in hydrogen ambient

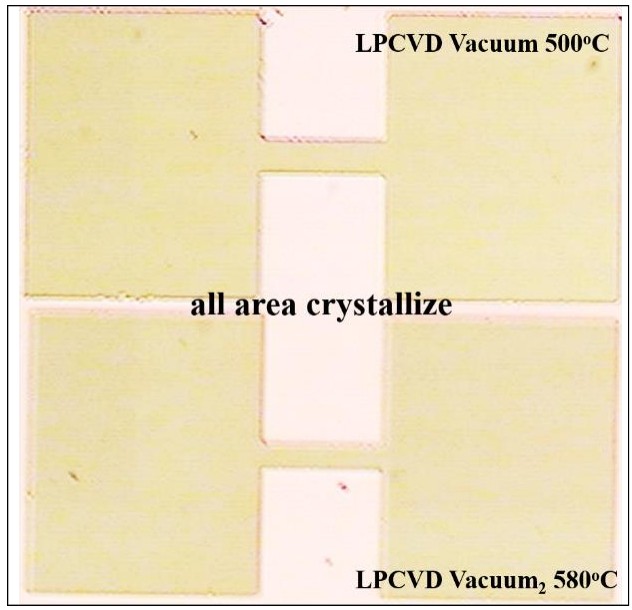


Figure 3-5 LPCVD amorphous silicon layer annealed (500 ℃, 580 ℃) in vacuum condition

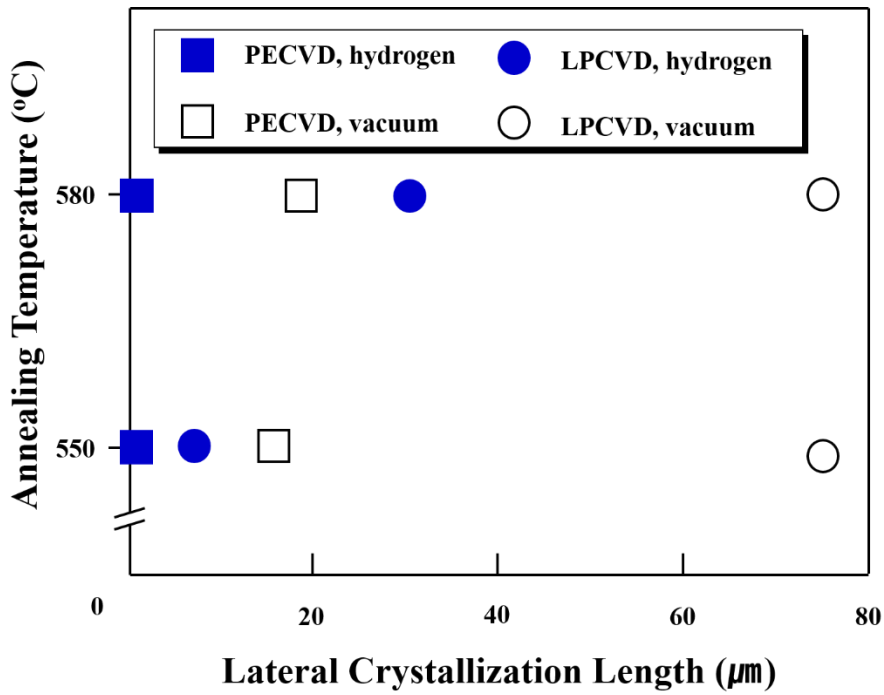


Figure 3-6 Lateral crystallization growth rate of 4 types of samples at 500 ℃ and 580 ℃

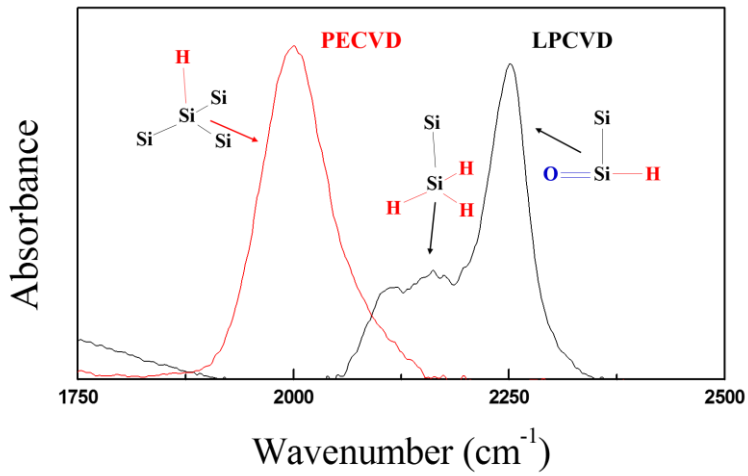


Figure 3-7 FT-IR measurement of PECVD (red line) and LPCVD (black line) amorphous silicon layer

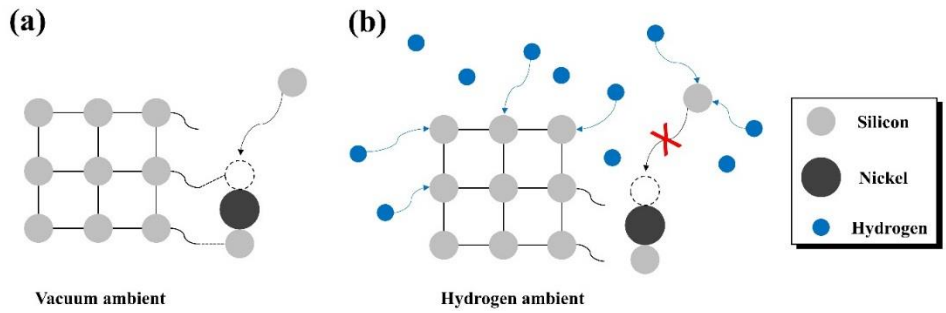


Figure 3-8 Schematic illustration of metal induced crystallization (a) in vacuum ambient and (b) in hydrogen ambient

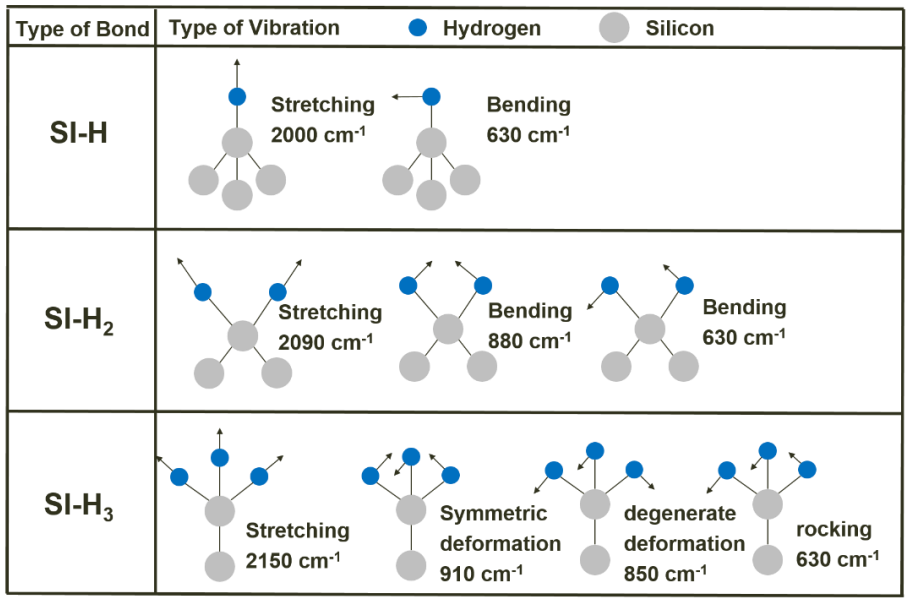


Table 3-1 Silicon Hydrogen bonding configuration

Chapter 4

Suppression of Leakage Current with Overlap and Off-set Structure at Source-Gate/Drain-Gate Junction on Metal Induced Lateral Crystallization Polycrystalline Bottom Gate Thin Film Transistors

A polycrystalline bottom gate thin film transistor structure cannot be currently fabricated using laser annealing crystallization because doing so causes thermal damage to the metal electrode. In this study, a polycrystalline bottom gate thin film transistor is successfully fabricated using metal-induced lateral crystallization. However, this method results in a relatively high leakage current because metal silicide defects are caused by the metal catalyst. An overlap/off-set structure is applied in this experiment to reduce the leakage current.

The overlap/off-set structure has a lower leakage current than a normal structure, and the overlap/off-set length also affects the electrical properties of the transistor. In this experiment, the subthreshold slope is also improved in a relative sense. Therefore, metal-induced lateral crystallization can be applied to produce a bottom gate structure in polycrystalline silicon transistors, and this method can be used to develop a manufacturing system for use in the liquid crystal display industry.

4.1 Introduction

Recently, polycrystalline silicon Thin Film Transistors (TFTs) have been further developed by investigating the use of Active Matrix Organic Light Emitting Diode (AMOLED) technology in transparent or foldable displays [4.1−4.4]. Amorphous silicon TFTs have a quite low field effect mobility of less than 1−2 cm^2/Vs, and polycrystalline silicon TFTs have field effect mobility of 100−200 cm^2/Vs, which is sufficiently high to operate as driving and switching transistor in AMOLED devices [4.5]. To achieve a phase transform from an amorphous phase to a polycrystalline phase, the crystallization process must be added as a fabrication process. Until now the several crystallization methods have been developed, including Solid Phase Crystallization (SPC) [4.6, 4.7], Excimer Laser Annealing (ELA) [4.8, 4.9], Metal−Induced Lateral Crystallization (MILC) [4.10, 4.11], etc. Of these, ELA has been widely used in industry, but there are still many serious disadvantages to doing so. For instance, ELA uses an expensive XeCl laser that results in a high manufacturing cost for AMOLED displays, and the laser scanning process results in non−uniformity due to the liquid−solid phase transformation. In

terms of the structure, ELA cannot produce a bottom gate structure that is common in Liquid Crystal Display (LCD) devices because metal gate damage is caused during laser scanning. Even if SPC does not use a laser scanning process, it cannot be used for display fabrication due to the high crystallization temperature that causes thermal damage on the glass substrate.

In our research group, we have investigated the production of bottom gate polycrystalline silicon TFTs for use in LCD product lines without the need to construct new facilities. SPC and ELA both have critical problems in producing commercial devices due to the high crystallization temperature and the laser scanning process that each respectively require. In 1996, the MILC process was introduced [4.10] as a crystallization method that uses a metal catalyst at a temperature below 550 ℃. MILC has advantages in overcoming the limitations of SPC and ELA. However, the main drawback of using MILC to produce TFTs is that it results in a relatively high leakage current, which is an important operating parameter for TFTs. This high leakage current is caused by metal silicide contamination in the TFT channel area that results from the metal used as the catalyst during crystallization. The metal silicide produced during

crystallization exists as a defect in the active area [4.12], and moreover, it is impossible to produce a polycrystalline grain of uniform size during the MILC process. This means that the grain boundary is formed during crystallization, and defects from the metal silicide are segregated at the grain boundary with a defect energy level also existing in the forbidden region of the bandgap. As a result, a relatively high leakage current occurs as opposed to those of devices fabricated using SPC and ELA [4.13-4.16].

The mechanism that produces the leakage current is quite different from that for the on-current. The on-current flows due to carrier diffusion through the channel region when an electrical field is applied as a gate voltage. In contrast, the leakage current is caused by generation and recombination of free carriers at the metal silicide defect sites. There are two ways to reduce the leakage current.

(1) Develop a new TFT structure to reduce the defect states.

(2) Carry out a defect free process through electrical or chemical modification.

In this study, we investigated the production of a modified bottom gate structure decrease leakage current (as an example of option (1) above), and this method produces overlap/off-set MILC poly bottom

gate TFTs. A Lightly Doped Drain (LDD) structure has been studied for a long period of time due to the reduction in the leakage current [4.17−4.23]. A comparison with the LDD reveals that the overlap/off−set structure has unique area that as a non−doped intrinsic region exactly between the gate and the source or drain. This novel MILC poly bottom gate structure can effectively reduce the leakage current.

4.2 Experiment

We applied the inverted staggered bottom gate structure that is commonly used in the LCD industry. The glass substrate used is the Corning Eagle XG glass (0.63t). A 100nm thick SiO_2 buffer layer was deposited on the glass substrate via Plasma Enhanced Chemical Vapor Deposition (PECVD) at a temperature of 350 ℃. Molybdenum tungsten (MoW) as a gate electrode was deposited via sputtering on the buffer layer at 300 ℃, and photolithography and wet etching were applied to pattern the gate electrode. After etching, the samples were cleaned using Isopropyl alcohol (IPA) to remove the remaining etchant at the corner of the patterns. Both the gate insulator and a silicon layer were deposited via PECVD at 350 ℃. 100 nm of silicon nitride were deposited using NH_3, Ar and SiH_4 gas mixture, and a 100 nm amorphous silicon layer was deposited using SiH_4 gas only.

To make an etch stopper, 100 nm of silicon oxide were deposited on an amorphous silicon layer using PECVD with a SiH_4, Ar and N_2O gas mixture. In particular, the etch stopper was etched using a Buffer Oxide Etchant (BOE) solution in a wet etching method, and in this process, the overlap and off-set area was defined by shifting the

etch stopper. Then, the p+ doping layer is deposited using PECVD with a SiH_4, B_2H_6 gas mixture at 350 ℃. The dry etching method was applied to produce an active layer and a separation region using Reactive Ion Etching (RIE). 5 nm layer of nickel was deposited on the amorphous silicon layer to produce nickel silicide, which is used as catalyst during crystallization. 2 hours of furnace annealing was then applied in a vacuum for MILC, and another 2 hours of furnace annealing were carried out in hydrogen ambient for dopant activation and hydrogen passivation. The electrical properties were measured using an Agilent System.

All of the fabrication processes were carried out in a 1000-class clean room. Figure 4-1 shows a schematic of the overlap/off-set structure performed in this experiment. Figure 4-1 (a) corresponds to the source-gate area, and Figure 4-1 (b) corresponds to the drain-gate area. In the case of the top gate MILC TFTs, LDD, Gettering [4.24], and Seed Induced Lateral Crystallization [4.25] were applied to reduce the leakage current, which is caused by the nickel silicide defects. During fabrication, the ion implantation or ion mass doping method is not used for the MILC bottom gate, and instead, PECVD p+ layer is deposited for the doped source/drain

region. Therefore, it is difficult to apply an LDD structure. In this experiment, the overlap/off-set structure was performed using an etch stopper shift. The main part distinguishing it with the LDD structure is the overlap/off-set that has a completely intrinsic region between the gate and source or gate and drain.

4.3 Results and Discussion

We produced bottom gate polycrystalline TFT devices without laser crystallization. Figure 4-2 (a) shows the drain current as a function of the gate voltage. The gate voltage sweeps from -15 V to 5 V, and the drain voltage is fixed at 0.1 V. When compared with conventional top gate MILC TFTs, the bottom gate has an improved quality in the slope, mobility and minimum level of the leakage current. However, this conventional bottom gate MILC TFT has a high leakage current with a positive gate voltage increase (which is called a pinning current). The high positive gate voltage means that there is a turn off voltage in the TFTs operation, so an increase in the positive gate voltage results in an increase in the electric field between the drain and gate, causing more generation of free carriers in the metal silicide defect state [4.12].

The overlap/off-set structure is investigated in this paper to produce a low pinning current. Figure 4-2 (b) shows the electrical measurements of the overlap/off-set structure in the bottom gate MILC TFTs. The filled circle represents the source off-set structure, which means that the doping area in the source region is separated

with the gate metal, as shown in Figure 4-1. On the other hand, an empty circle represents the drain off-set structure. Compare with the source off-set and drain off-set structure, V_{th} and the subthreshold slope are constant regardless of the structure. The mobility (205, 170 cm^2/Vs, respectively) is high enough to operate devices in both structure. The on-current value is quite similar, regardless of the off-set area, but the off-current is considerably different as an off-set region.

As mentioned above, the leakage current mechanism is quite different from that of the on-current. The on-current is a result of carrier flow from the source to the drain, through the channel. The leakage current is also due to carrier movement, but the carriers in this case are not from the source or drain but rather from the defect state, such as from the interface fixed charge and the metal silicide defect. The leakage current is thus generated using three kinds of mechanisms: thermal activation, trap generation in the forbidden band gap, and tunneling. Polycrystalline silicon layer is not a single crystal, so during crystallization, there must be excited grain boundaries at the interface of the crystallized regions, which are amorphous areas. The lowest leakage current level is affected by carrier generation in

the trap state in the bandgap forbidden region (second mechanism of leakage current generation). The pinning current is to with tunneling between the drain and the gate (third mechanism of leakage current generation). In the case of the drain off-set structure, the minimum leakage current level and pinning current are lower than the source off-set structure. Therefore, the drain off-set structure has enhanced electrical properties when compared to the source off-set structure, especially in the reverse operation region.

Figure 4-3 (a) shows an optical microscopy image of the overlap/off-set structure with four kinds of different off-set lengths: 0, 1, 2 and 3 ㎛. The overlap/off-set length effect is investigated, and the overlap/off-set region is defined with silicon oxide etch stopper etching and shifting above the channel area. In Figure 4-3 (b), the black line is 0 ㎛, red is 1 ㎛, blue is 2 ㎛ and green is 3 ㎛ for the electrical characteristics of the drain off-set structure. If an overlap/off-set structure is not applied, then the highest pinning current value is observed, as we can see with the black line in the graph. This means that it is necessary to fabricate an MILC bottom gate TFTs with overlap/off-set structure to reduce the leakage current. In the case of 2 ㎛ overlap/off-set structure, it show the

most enhanced electrical characteristics comparing with others. In Table 4-1, the detailed electrical properties are shown for several length of overlap/off-set structure. Comparing with the 1 ㎛overlap/off-set structure, that with 2 ㎛ has a wide depletion region between the doped drain area and channel area. This depletion region have n-type properties with positive gate voltage. As mentioned above, tunneling is the main reason for the pinning current, so a longer off-set length results in lower pinning current values. However, when the TFT is fabricated with 3 ㎛ of overlap/off-set, it has a higher leakage current and a pinning current than with the 2 ㎛ structure. Therefore, there should be an optimum off-set length in this bottom gate structure (in this case 2 ㎛). With a longer off-set length than 2 ㎛, the depletion region is so wide that it results in an increase in the resistance between the drain and the channel. Moreover, if the depletion region between the drain and the channel becomes wider, the tunneling current is not only reduced but free carrier generation is also induced by the metal silicide defect in the polycrystalline silicon layer.

In order to remove the free carrier effect on the leakage current, electrical stress is applied before measurement [4.14]. Detailed

condition of electrical stress is explained in ref. [4.14]. Figure 4-4 (a) shows the electrical characteristic of various overlap/off-set lengths under electrical stress. Without electrical stress, it is difficult to investigate a pure overlap/off-set length effect because free carriers are generated from the bulk polycrystalline silicon layer and between silicon and gate insulator interface. The inner graph in Figure 4-4 (a) shows the subthreshold region to investigate the subthreshold slope with different overlap/off-set lengths. The subthreshold slope increases as the overlap/off-set length becomes wider (0.18, 0.18, 0.22, 0.24). Figure 4-4 (b) shows the subthreshold slope and the pinning current as a function of the overlap/off-set length with electrical stress. When the overlap/off-set length increased, the pinning current was reduced. On the other hand, the subthreshold slope declined. If the overlap/off-set region increased, the depletion region between the gate and drain also expanded and the pinning current is continuously deceased. It means free carriers from the defect center is removed by electrical stress. Table 4-2 indicate the electrical properties with electrical stress in overlap/off-set structure.

4.4 Summary

In this work, we produced MILC polycrystalline bottom gate TFTs with low leakage and low pinning current values due to an overlap/off-set source/drain structure with electrical stress. With etch stopper shift, this new structure could be fabricated easily. Moreover, the overlap/off-set length also affected the electrical properties of the TFTs. These characteristics are adequate to operate AMOLED and flexible display devices.

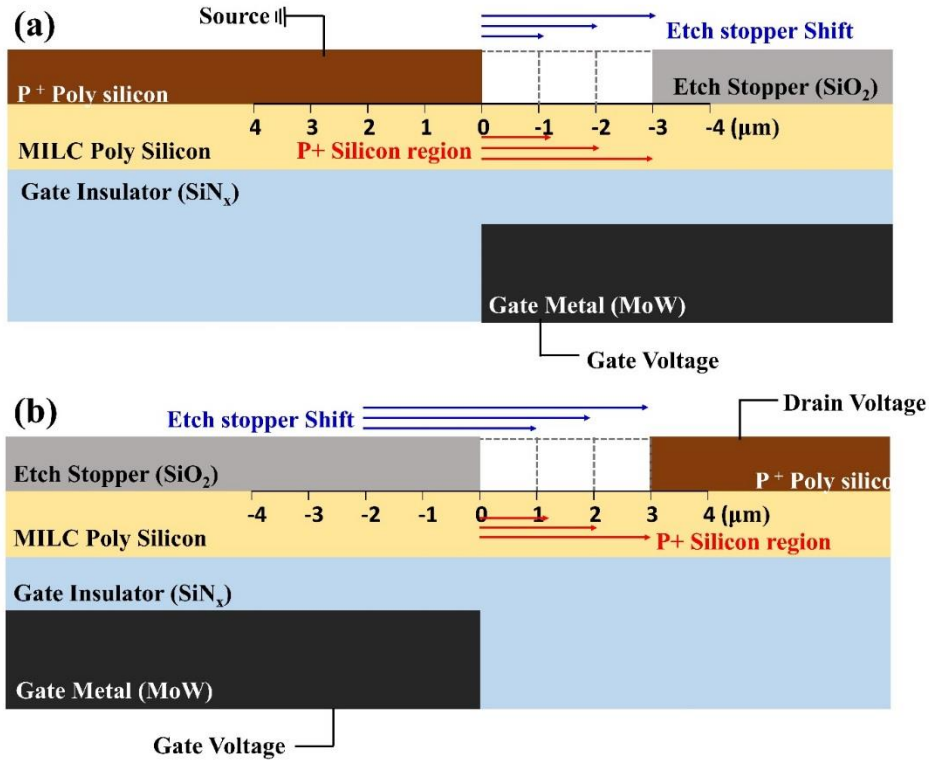


Figure 4-1 Schematic image of overlap/off-set structure bottom gate TFTs (a) at source region and (b) at drain region

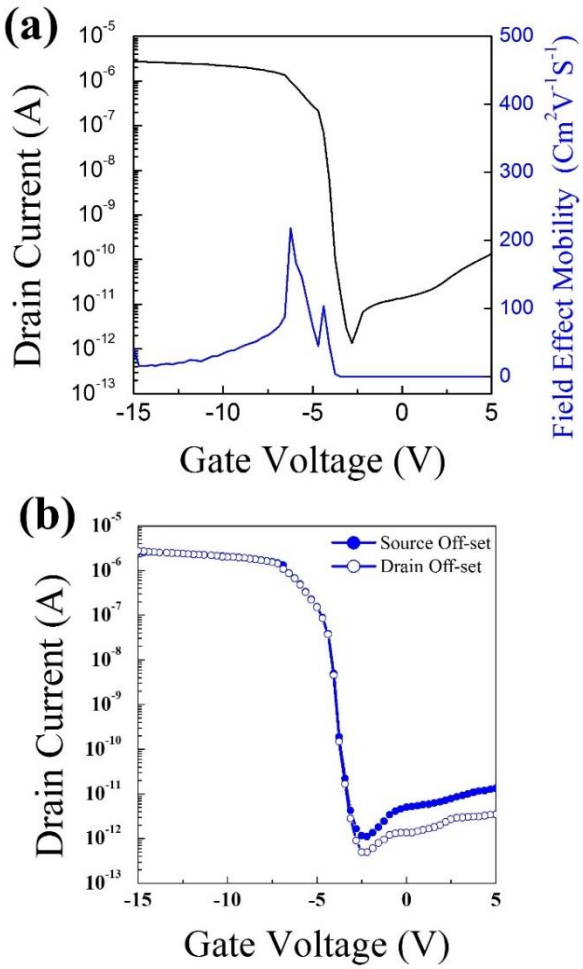


Figure 4-2 (a) I-V characteristics of MILC bottom gate TFTs, (b) I-V characteristics of drain off-set structure (empty circle) and source off-set structure (filled circle)

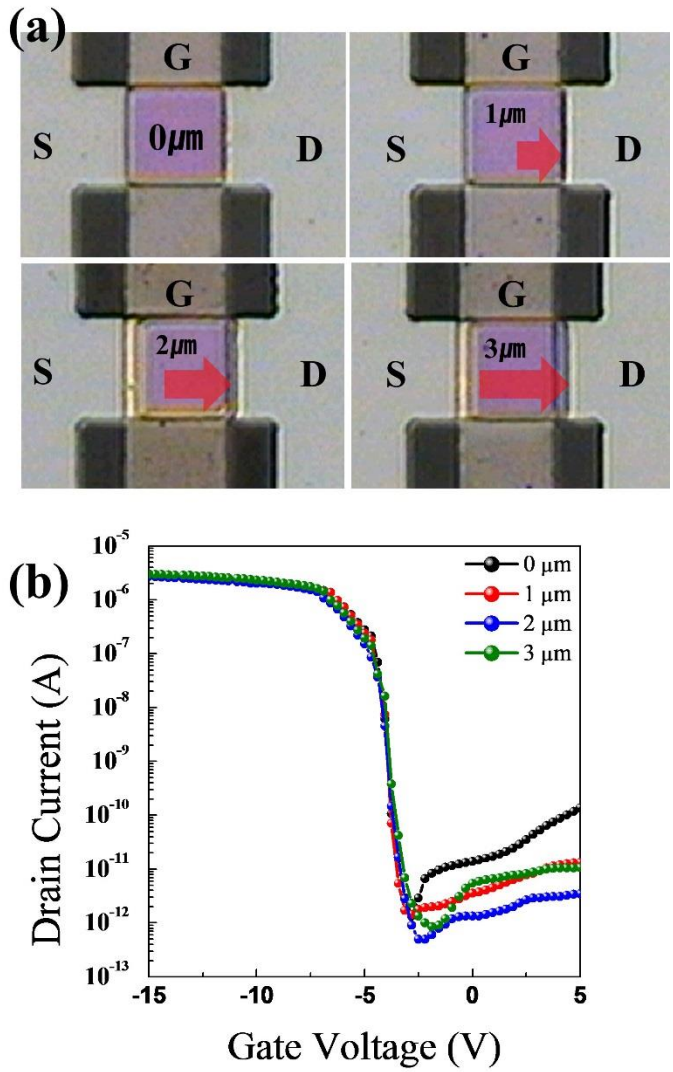


Figure 4-3 (a) Microscope optical image of overlap/off-set region at channel area (b) I -V characteristics with various drain off-set length (from 0 to 3 ㎛)

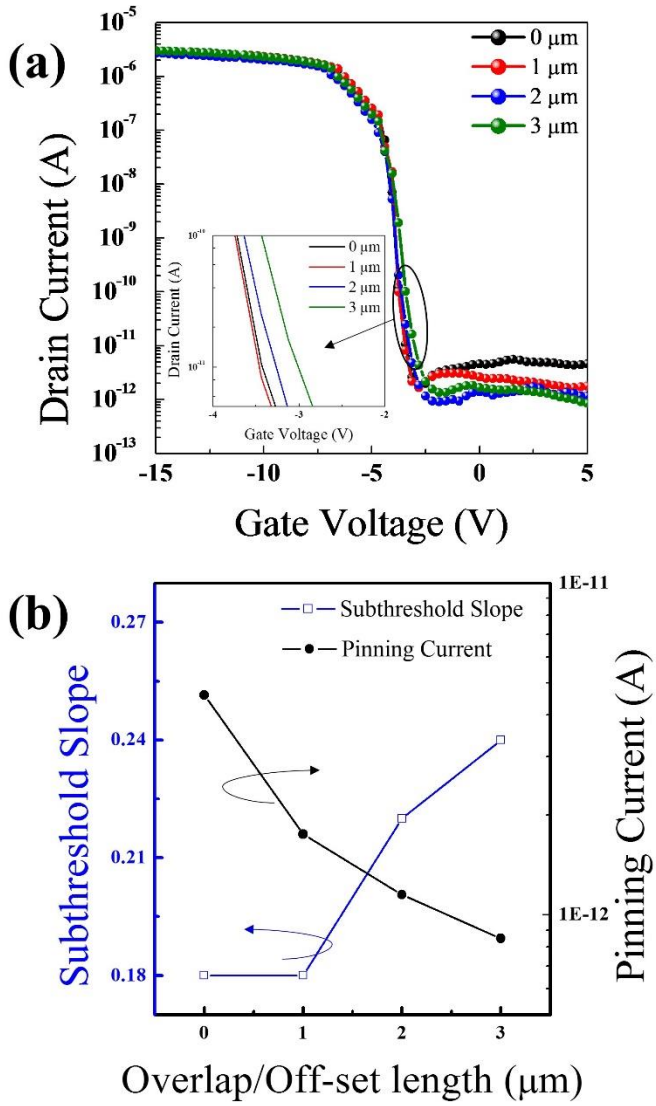


Figure 4-4 (a) Drain current as a function of gate voltage with various overlap/off-set length (b) Sub-threshold slope and pinning current as a function of overlap/off-set length

	0 ㎛	1 ㎛	2 ㎛	3 ㎛
V_{TH} (V)	−5	−5	−5	−5
Slope (V/dec)	0.18	0.19	0.21	0.19
Mob. (cm^2/Vs)	188	186	170	218
I_{ON} (10^{-6})	2.69	2.74	2.72	3
I_{OFF} (10^{-12})	2.81	1.35	0.46	8.6

Table 4−1 Detail electrical properties of Bottom gate MILC poly−Si TFT with various drain off−set

	0 ㎛	1 ㎛	2 ㎛	3 ㎛
V_{TH} (V)	−5	−5	−5	−5
Slope (V/dec)	0.18	0.18	0.22	0.24
Mob. (cm^2/Vs)	196	196	171	213
I_{ON} (10^{-6})	2.67	2.92	2.65	2.99
I_{OFF} (10^{-12})	1.99	1.48	0.87	1.31

Table 4−2 Detail electrical properties of Bottom gate MILC poly−Si TFT with various drain off−set under electrical stress

Chapter 5

Direct/Indirect Contact between Channel Inversion Layer and Doped Source/Dain region on Metal Induced Lateral Crystallization Polycrystalline Silicon Bottom Gate TFTs

Top gate-structured thin film transistors have a channel inversion region that is directly connected to the doped source/drain area. This stands in contrast with normal bottom gate-structured thin film transistors that have a channel inversion region on the downward facing side of the silicon layer regardless of the crystallinity. In this experiment, we fabricate a bottom gate thin film transistor with a direct contact junction between the channel inversion layer and the doped source/drain area and subsequently analyze its electrical properties. The leakage current of the indirect contact structure is

lower than that of a direct contact structure, and we calculate the variation in the specific contact resistance according to differences in the intrinsic silicon thickness in order to confirm the effect that the intrinsic silicon thickness has on the bottom gate direct/indirect contact structure.

5.1 Introduction

The characteristics of thin film transistors (TFTs) have a significant influence on the fabrication of high-performance display devices [5.1, 5.2]. Nowadays, the mainstream display industry has moved away from using Cathode Ray Tube (CRT) displays to both Liquid Crystal Displays (LCD) [5.3, 5.4] and Active Matrix Organic Light Emitting Diode (AMOLED) [5.5, 5.6] displays, called Flat Panel Display (FPD). As such, TFT technologies are indispensable to further improve display devices [5.7-5.9]. TFTs can be fabricated using two different structures, the so-called 'top gate' and 'bottom gate' structures. The bottom gate structure is used in most LCD devices that are produced for the display market because metal electrodes can block the back light during operation. In addition, TFTs act as a switching element in the LCD device, and amorphous silicon has adequate properties to operate such TFTs. However, AMOLED displays and High-Definition (HD) LCD [5.10, 5.11] require the use of high-performance devices, so the polycrystalline silicon layer with a top gate structure is generally used. The bottom gate structure cannot be applied because the metal electrode can be damaged and

deformed during laser crystallization in the Excimer Laser Annealing (ELA) [5.12–5.15] process.

To date, various silicon crystallization methods have been investigated and developed, including the commonly–used Solid Phase Crystallization (SPC) [5.16–5.18] and ELA. However, SPC cannot be applied in display fabrication due to the crystallization temperature. SPCs needs a high temperature of about 900 ° C, which is higher than the melting point of a glass substrate (600 ° C). In 1992, the ELA process was first presented as a crystallization method that makes use of the excimer laser scanning process [5.19]. Although a glass substrate can be used in the ELA process, there are some disadvantages to doing so, including the non–uniformity resulting from the laser scanning process, rough surface due to a liquid–solid phase transformation, and the need for expensive laser equipment. Moreover, the bottom gate structure cannot be applied to produce TFTs from a structural point of view because, as we briefly mentioned, the metal electrode can be damaged.

This means that if we the bottom gate structure can be applied with polycrystalline silicon, manufacturing facilities used for LCD fabrication could be employed to produce other advanced display

devices, such as AMOLED displays. Our research group has investigated the feasibility of producing polycrystalline silicon TFTs intended for LCD products without the need for new facilities. In 1996, Metal Induced Lateral Crystallization (MILC) was introduced as a crystallization method that makes use of a metal catalyst at a temperature below 550 ° C [5.20]. Thus, it is possible to fabricate large-area display devices on a glass substrate regardless of the TFT structure.

The difference between the top gate and bottom gate structures is not only the position of the metal electrode. In the case of the top gate structure, the channel inversion layer is produced at the top of the active silicon layer, and it creates a direct junction with the doped source/drain region. In the case of the bottom gate, the channel inversion layer is produced at the bottom of the silicon layer, and it creates an indirect junction due to the existence of an intrinsic silicon layer between the doped region and the channel inversion area. Therefore, we fabricate an indirect contact as well as a direct contact structure for the bottom gate TFTs of this study, and we analyze the electrical properties of the TFTs with direct/indirect contact between the channel inversion and the doped source/drain region.

5.2 Experiment

Figure 5-1 shows a comparison of the fabrication flow for an Indirect Junction TFT (IJ-TFT) and a Direct Junction TFT (DJ-TFT) structure. The red arrow on the left side indicates the schematic for the IJ-TFT structure fabrication flow, and the blue arrow on the right side is for the DJ-TFT fabrication flow. A 300-nm silicon oxide (SiO_2) buffer layer is deposited on a glass substrate (Corning Inc. Eagle XG, 106 mm x 106 mm) via Plasma Enhanced Chemical Vapor Deposition (PECVD) with a SiH_4, Ar, and N_2O gas mixture to block impurity diffusion. Thereafter, 300-nm of molybdenum tungsten ($Mo_{0.9}W_{0.1}$) are deposited as the metal electrode layer via sputtering. The deposition temperature is set to room temperature with a deposition rate of about 100 nm/min. The metal electrode is etched using photolithography with H_3PO_4 + CH_3COOH + HNO_3 + H_2O etchant.

A 100-nm of silicon nitride (SiN_x) as a gate insulator is deposited via PECVD using a SiH_4, Ar, and NH_3 gas mixture at 350 ° C, and the deposition rate is of about 20 nm/min. A 50-nm amorphous silicon layer is deposited on the gate insulator via PECVD using a non-

vacuum breaking process at 350 ° C with SiH_4 gas for 5 minutes. 10-nm of SiO_2 are deposited as the etch stopper layer via PECVD at 350 ° C. The next process consists of an etching step, and in this process, we are able to distinguish the structure for each of the IJ-TFT and DJ-TFT. In the IJ-TFT, the etch stopper is etched only with Buffer Oxide Etchant (BOE), otherwise in the DJ-TFT, not only the etch stopper but also an amorphous silicon layer is etched via Reactive Ion Etching (RIE) with SF_6 and O_2 gas at room temperature. After etching, a 300nm p+ amorphous silicon layer is deposited via PECVD using SiH_4 and B_2H_6 gases, and the p+ amorphous silicon layer, intrinsic amorphous silicon and gate insulator layer are etched via RIE. A 5 nm nickel layer is then deposited on the source and drain area for the MILC process via sputtering at room temperature. Finally, furnace annealing in a vacuum is administered for 2 hours and in a hydrogen atmosphere for 1 hour. The electrical properties were then measured using an Agilent System, and all of the fabrication processes were carried out in a 1000-class clean room.

5.3 Result & discussion

Figure 5-2 shows the drain current as a function of the gate voltage for both the (a) IJ-TFT TFT and (b) DJ-TFT TFT. The drain voltage is set to -0.1 V, -1 V, -2 V, -3 V and -4 V in this measurement, and the gate voltage is swept from -20 V to 5 V. The intrinsic silicon layer is 50 nm thick, and the p+ doped silicon layer is 300 nm thick. The IJ-TFT structured TFTs have slightly higher current and lower leakage current than the DJ-TFT. Otherwise, the subthreshold slope and threshold voltage is constant regardless of the structure. Figure 5-2 (c) shows the leakage current, and the pinning current changes as a function of the drain voltage from 0.1 V to 4 V. A comparison of these two structures reveals that the leakage current and pining current for the IJ-TFT is lower than that for the DJ-TFT. The pinning current is defined as the leakage current when a high reverse bias gate voltage is applied. In this experiment, the pinning current is measured as the current when the gate voltage is 5 V. Figure 5-2 (d) shows the change in the on/off ratio as a function of the drain voltage. The change in the on/off ratio is similar to that of the leakage current. These results indicate that a lower leakage

current and the larger on/off ratio are a result of the difference in the structure. Figure 5-3 presents a side view schematic for the (a) IJ-TFT and (b) DJ-TFT to analyze the effect of the structure on the electrical characteristics. As mentioned above, the main point to distinguish the IJ-TFT and DJ-TFT is the existence of an intrinsic layer under the source/drain region, and the carriers flow from the source to the drain through the channel area. In the case of the IJ-TFT, the carriers pass not only the inversion channel area but also intrinsic region to arrive source/drain region. At this time, the intrinsic silicon layer act as a depletion region, so the free carriers that are generated cannot go through the barriers through tunneling, and therefore, the pinning current is reduced.

In contrast, for the DJ-TFT, the carriers pass only the channel inversion area, so the energy band diagram between the source/drain and the channel area exhibits a sharp curve. In the case of the MILC polycrystalline silicon top gate structure with direct contact, the high leakage current and the pinning current are the main limitations to their use in display devices. Therefore, another structure has to be applied to reduce the leakage current, such as a Lightly Doped Drain (LDD) structure, and an additional mask needs to be fabricated.

However, the indirect contact of the bottom gate-structured TFTs acts like an LDD structure without the need for an additional mask. We assume that the intrinsic layer plays an important role in the electrical properties of the TFT, so effect that the thickness of the intrinsic layer has is investigated with three different samples (50 nm, 100 nm, 200 nm). Figure 5-4 (a) graphs the measurements obtained for the electrical properties with different intrinsic thicknesses for both the IJ-TFT and DJ-TFT. The black lines represent the results for the 50-nm intrinsic silicon layer, the red lines represent that of the 100-nm intrinsic layer, and the blue lines represent that for 200 nm. The dashed lines are the results for the IJ-TFT, and the solid lines are those for the DJ-TFT. The leakage current continuously increase as the thickness of the intrinsic layer increases. The defect density in the channel layer increases because the grain boundary and the trap state at the center of the defects increase as the intrinsic silicon layer thickness increases. With an intrinsic silicon layer that is 50 nm thick, the on-current and off -current almost have similar values, which means that the 50-nm thickness is not sufficient to have an effect on the operation of the TFTs. However, a thick intrinsic silicon layer effects changes on the

on-current and off-current. In particular, an intrinsic layer of 200 nm results in a dramatic reduction of the on-current of the IJ-TFT relative to that of the DJ-TFT. In addition, the increase in the leakage current in the DJ-TFT is also larger than that of the IJ-TFT due to the free carrier generation. Figure 5-4 (b) shows the change in the on-current and off-current as a function of the intrinsic silicon thickness. We can easily assume that this phenomenon has been caused by the effect of the intrinsic silicon layer.

We explain the effect of the intrinsic silicon layer by calculating the specific contact resistance [5.21-5.23] of each structure. Figure 5-5 (a) shows the specific contact resistance calculated for the four different intrinsic silicon layer samples (0 nm, 50 nm, 100 nm and 200 nm) with a fixed a 300 nm p+ doped silicon layer. The specific contact resistance increases as the thickness of the intrinsic layer increases. Figure 5-5 (b) shows the specific contact resistance and on-current as a function of the intrinsic silicon layer thickness, and the behavior of the specific contact resistance and on-current can be seen to be exactly opposite. Although the on-current is collected at the source/drain region, it is hard to collect carriers diffused from channel inversion area due to the high specific contact resistance.

Therefore, a thick intrinsic silicon layers results in a marked decrease in the on-current due to the relatively higher specific contact resistance.

5.4 Conclusion

In this research, we have fabricated indirect (IJ-TFT) and direct (DJ-TFT) contacts between channel inversion layers and the doped source/drain region. We measured the electrical properties for these TFTs with different structures. The indirect contact structure results in TFTs with a higher on-current and lower leakage current than those obtained with a direct contact structure. These results suggest that the intrinsic silicon layer under the doped source/drain region has an effect on the electrical properties. We experimented with intrinsic silicon layers of different thicknesses and can conclude that a thicker silicon layer results in a low on-current and a high leakage current. This deterioration in the electrical properties can be explained by the specific contact resistance. If the intrinsic silicon layer is 200 nm thick, the specific contact resistance is 3-4 times higher than when there is no intrinsic layer. Therefore, even if the direct contact structure is similar as the top gate structure, the indirect structure exhibits better electrical characteristics.

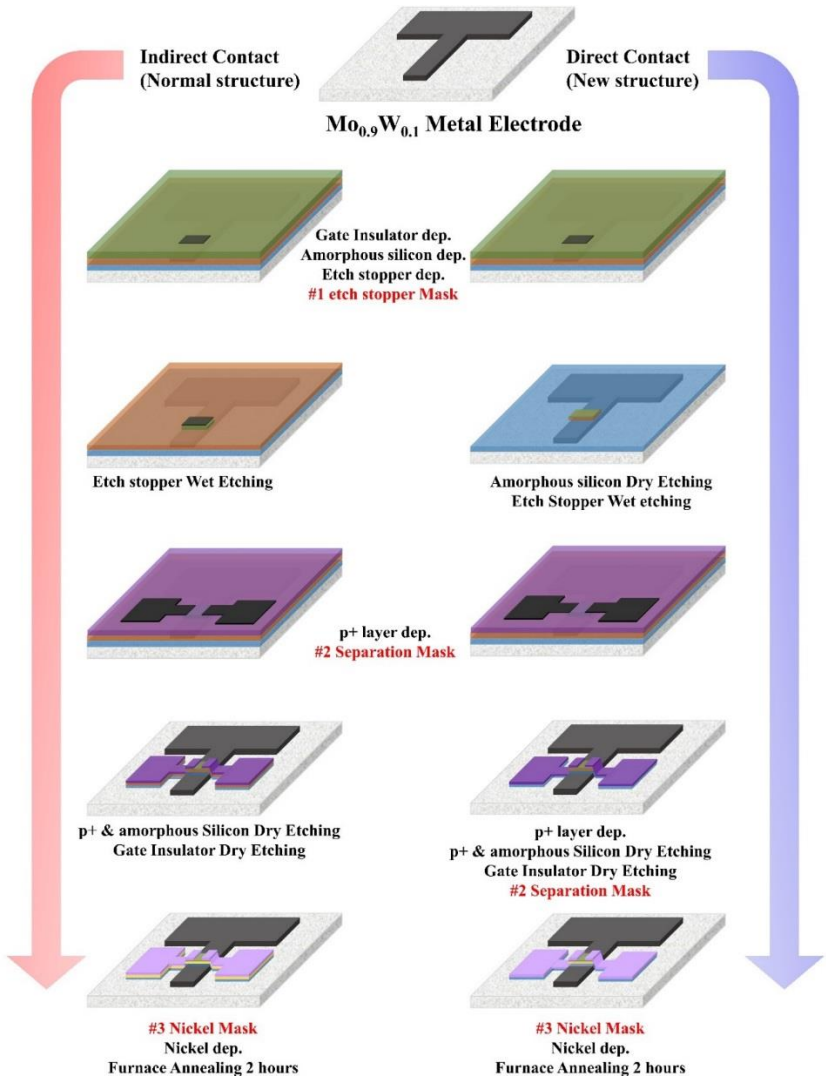


Figure 5-1 Schematic image of fabrication flows of bottom gate polycrystalline silicon thin film transistors with direct junction structure (right side, blue arrow) and indirect junction structure (left side, red arrow)

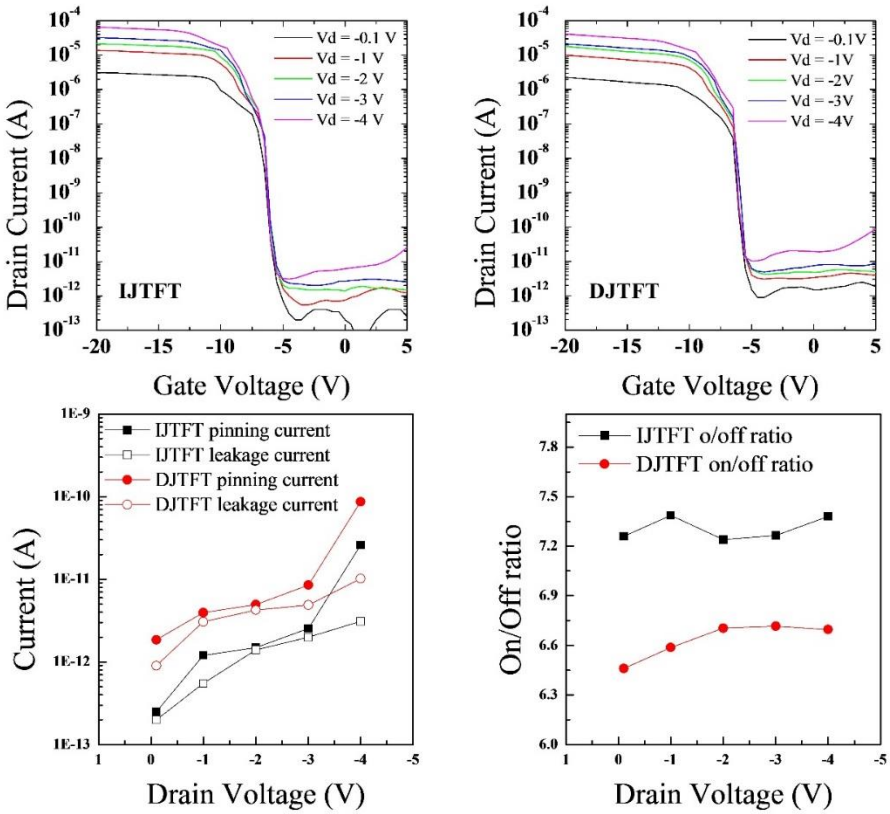


Figure 5-2 The electrical properties of IJ-TFTs (a) and DJ-TFTs (b). (Drain voltage is increased from -0.1V to -4 V: -0.1 V - Black line, -1 V - Red line, -2 V - Green line, -3 V - Blue line, -4 V - Violet line), (c) the leakage current and pinning current density of DJ-TFTs and IJ-TFTs as a function of drain voltage, (d) the on/off ratio of DJ-TFTs and IJ-TFTs as a function of drain voltage

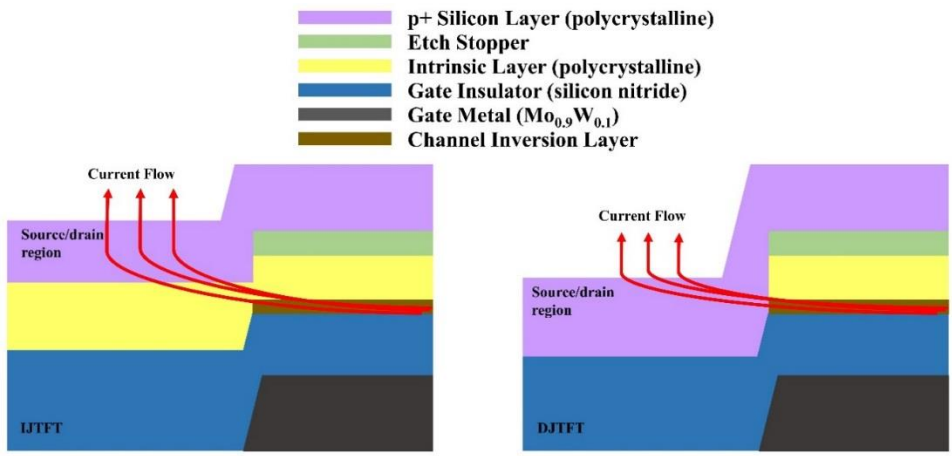


Figure 5-3 Side view schematic image for the IJ-TFT and DJ-TFT and its current flow from channel area to source/drain region.

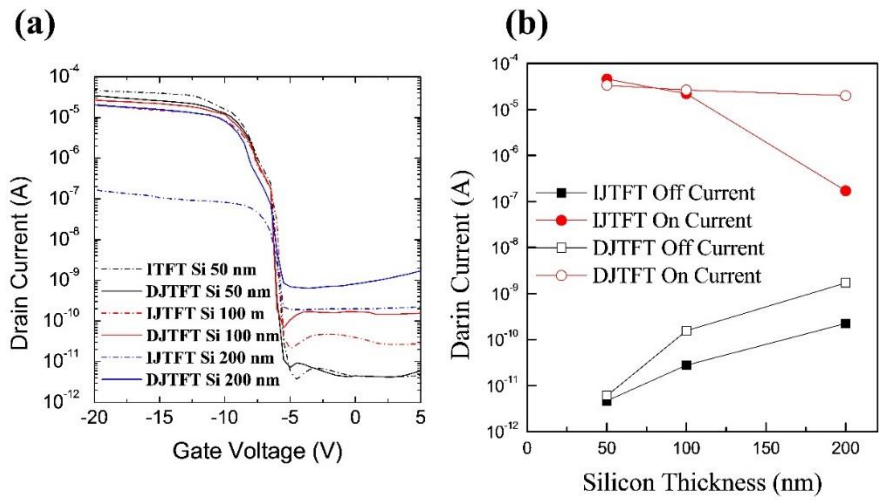


Figure 5-4 The result of (a) electrical properties of IJ-TFT and DJ-TFT with various thickness of intrinsic silicon layer between a doped source/drain and a gate insulator layer, (b) on/off current density as a function of intrinsic silicon layer thickness.

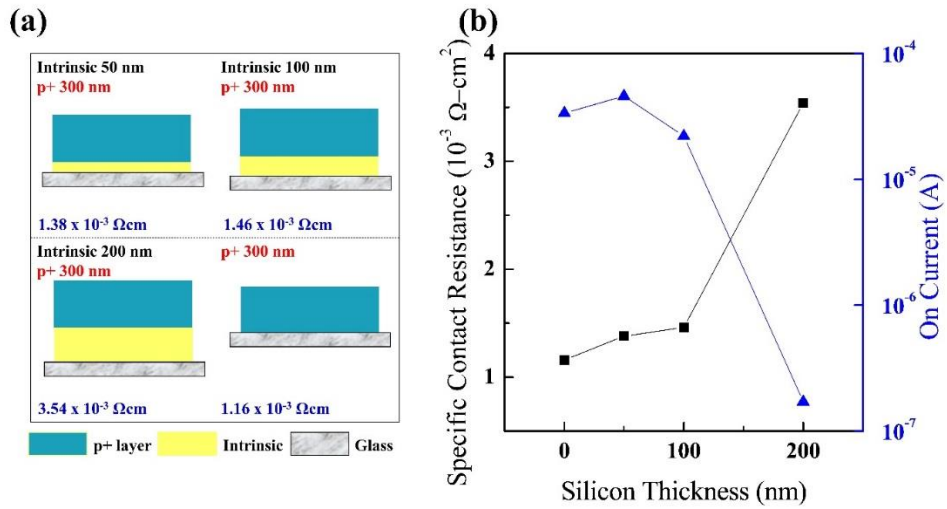


Figure 5-5 (a) Schematic four kinds of samples used in this experiment and calculated specific contact resistance, (b) specific contact resistance and on current density as a function of intrinsic silicon layer thickness

Chapter 6

Edge cut process for reducing Ni content at channel edge region in metal induced lateral crystallization Poly-Si TFTs

Abstract Nickel silicide is main issue in Polycrystalline silicon Thin Film Transistor (TFT) which is made by Metal Induced Lateral Crystallization (MILC) method. This Nickel silicide acts as a defect center, and this defect is one of the biggest reason of the high leakage current. In this research, we fabricated polycrystalline TFTs with novel method called Edge Cut (EC). With this new fabrication method, we assumed that nickel silicide at the edge of the channel region is reduced. Electrical properties are measured and trap state density also calculated using Levinson & Proano method

6.1 introduction

In the past few decades, Liquid Crystal Displays (LCDs), which consist of amorphous silicon thin film transistors (TFTs), have led the display market. However, with the requirement for flexible [6.1] and foldable [6.2] displays, it is natural that the Active Matrix Organic Light Emitting Diode (AMOLED) would be developed. To make a more precise high resolution display, it is necessary that innovative material TFTs possess high field effect mobility [6.3] and low leakage current [6.4]. Compared with an amorphous silicon TFT in an LCD, poly silicon TFTs have a high enough field effect mobility. To make enhanced poly silicon TFTs, it is important to make a good quality poly silicon layer. There are several ways of converting amorphous silicon to a poly silicon layer, such as Solid Phase Crystallization (SPC) and Excimer Laser Annealing (ELA) [6.5]. Currently, near-commercial grade poly silicon TFTs have been made by ELA technology. But this ELA technology needs a scanning process, which causes an overlap problem in fabrication [6.6]. Also the laser is expensive in initial development cost and there is a

uniformity problem caused by overlap scan of laser. The SPC method cannot be used to make an AMOLED display, because of the fabrication temperature. In order to make an SPC poly silicon layer, the process temperature has to be higher than 900 ℃, but the melting point of glass substrate is around 600 ℃. On the other hand, Metal Induced Lateral Crystallization (MILC) was investigated in 1996 [6.7], without any scanning process or extremely high temperature process [6.8]. It means that there is no limitation of substrate with MILC technology. However, the biggest obstacle in the MILC process is the relatively high metal contamination at the grain boundary, which leads to high leakage current and results in device degradation. Nickel is used just as a catalyst to induce crystallization, so nickel contamination in the channel region is not too much, except at the edge region. This nickel silicide is well known as a main factor that causes reliability degradation and performance degradation [6.9–6.11].

6.2 Experiment

In this research, we fabricated two types of MILC polycrystalline silicon TFTs with self-aligned coplanar structures, to compare the effect of nickel silicide at the channel edge area. The first one is called 'Normal' and second is 'Edge Cut' (EC). The main difference between these two TFTs is the crystallization process. For device fabrication, a 100 nm silicon oxide (SiO_2) buffer layer was deposited on an Eagle XG glass substrate by Plasma Enhanced Chemical Vapor Deposition (PECVD) at 350 ℃. Thereafter an 100 nm amorphous silicon layer was deposited by Low Pressure Chemical Vapor Deposition (LPCVD) using SiH_4 gas at 500 ℃. After the LPCVD process, three further steps were followed, which were active patterning, nickel deposition and crystallization. In the Normal case, and after LPCVD deposition, the active pattern was defined by photolithography and Reactive Ion Etching (RIE) using SF_6 and Ar mixed gas. A 5 nm nickel film was deposited on both sides of the channel area, using the lift-off method. Furnace annealing was

carried out at 550 ℃ for crystallization, for two hours in H_2 ambient.

Figure 1 (a) shows three steps for the Normal TFT. It shows that after crystallization, the nickel silicide was segregated at the channel edge region because of the fixed channel area. The nickel silicide could not spread beyond the channel area. Figure 1 (b) is the Edge Cut process. After LPCVD deposition, the nickel film was deposited first. Thereafter, furnace annealing was carried out for crystallization. During crystallization, the nickel silicide could spread freely due to the non-fixed channel area. After crystallization, the active pattern was defined, the same as for the Normal process. In the case of the Edge Cut TFT process, the amount of nickel silicide at the channel edge region is reduced. A 100 nm gate insulator was deposited by PECVD using SiH_4 and NH_3 gases at 350 ℃. A 200 nm molybdenum tungsten (MoW) film was deposited by sputtering for gate electrode. The gate electrode was etched by H_3PO_4, CH_3COOH, HNO_3 and H_2O mixed solution, by photolithography method. The gate insulator was etched by RIE. In order to define the source/drain junction, the samples were doped by an ion mass doping (IMD) system using B_2H_6 source gas diluted with 80% of H_2 gas. The accelerating voltage and

RF power were 17 keV and 150 W, respectively. The electrical properties were measured by Agilent System. The entire fabrication process was carried out in a 1000-class clean room.

6.3 Result and Discussion

In Figure 1 we could assume that there is more nickel silicide in the Normal case than in the EC case at the edge of the channel region in the 'Normal' case at the edge of the channel region. With a getter layer we could see the nickel silicide distribution in the polycrystalline silicon layer. Figure 2 shows the gettering image and optical image after the gettering process. On the polycrystalline silicon layer, a 50 nm amorphous silicon layer was deposited by PECVD at 350 ℃. With furnace annealing at 550 ℃ for one hour, nickel silicide spread up with crystallization. In the microscope optical image in Figure 2, the white region is the polycrystalline region, which is caused by nickel silicide spreading up, and the black region is an amorphous region due to the nickel silicide free area. Even though the getter layer has two distinct areas, it doesn't mean that the bottom silicon layer is partially crystallized. It shows the distribution of nickel silicide in the polycrystalline silicon layer. Especially at the channel edge region, the whole area was crystallized, which means the nickel silicide is segregated at this edge. We could

easily reduce the nickel silicide by removing the nickel silicide segregated edge region.

Figure 3 shows the electrical characteristics of the Normal and EC TFTs. This graph shows drain current as a function of gate voltages. The TFTs have 10 ㎛ width and 10 ㎛ length and gate voltage is changed from −35 V to 10 V. Two drain voltages were applied: 0.1 V and 2 V. The black filled line represents the Normal polycrystalline silicon TFT and the white filled line is the EC polycrystalline silicon TFT. The main difference between the Normal and EC TFTs is their leakage current values. The Normal TFT has 7.66 x 10^{-11} A, while the EC TFT has 1.93 x 10^{-11} A. And the On current is also higher in the EC TFT (at 6.89 x 10^{-5} A compared to 5.19 x 10^{-5} A in the 'Normal' TFT). This electrical improvement is caused by the reduction in nickel silicide at the channel area. It was reported that the main reason for leakage current in the MILC polycrystalline TFTs in the reverse bias region is the trap states that are generated by nickel silicide in the channel region. In our novel fabrication method, the amount of nickel silicide is reduced, so leakage current is also reduced. Figure 4 shows the calculated trap density at the grain boundary, using the Levinson and Proano method [6.12, 6.13]. The

grain boundary potential barrier height is related to the carrier concentrations inside the grain and the trapping states located at the grain boundaries. Based on this consideration, the amount of trap state density (N_t) can be extracted from the current-voltage characteristics of poly-Si TFTs. Grain boundary trap density could be calculated at low drain voltage with a gate voltage which is higher than the threshold voltage. The slope gained from ln [$I_D/(V_G - V_{FB})$] as a function of $1/(V_G - V_{FB})^2$ graph, is used for the trap density calculation. Equation (1) is induced by considering the mobility under a low gate voltage

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^{\,2}\sqrt{\varepsilon_{ni}\varepsilon_{si}}}{C_{ox}^{\,2}(V_G - V_{FB})^2}) \qquad (6.1)$$

From this equation (6.1) we can extract equation (6.2), which expresses the trap density.

$$N_t = \frac{C_{ox}}{q}\sqrt{|Slope|} \qquad (6.2)$$

where ε_{Si} and ε_{ni} are the Si and SiN_x dielectric constants, respectively. The flat band voltages V_{FB} were defined as the gate voltage that yields the minimum drain current at a drain voltage of −0.1 V. The

result shown is that the grain boundary trap density is decreased when the 'Edge Cut' process is applied.

6.4 conclusion

In this report, we focus on the nickel silicide at the edge of the channel region, which is the main area of a TFT's electrical properties. The nickel silicide contamination in the channel region is reduced with the EC process, which is a small change to the fabrication process compared with the 'Normal' MILC poly silicon TFT fabrication process. To prove our assumption, we capture the optical images of the MILC process, measure the electrical performance of both our Normal and EC TFTs, and calculate the grain boundary trap density using the Levinson and Proano method.

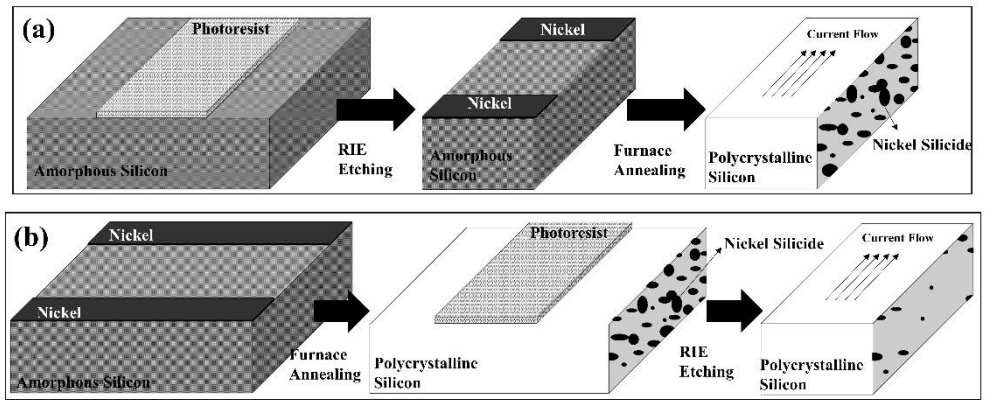


Figure 6-1 Schematic image of nickel silicide segregation of (a) 'Normal' MILC poly silicon channel and (b) 'Edge Cut' MILC poly silicon channel.

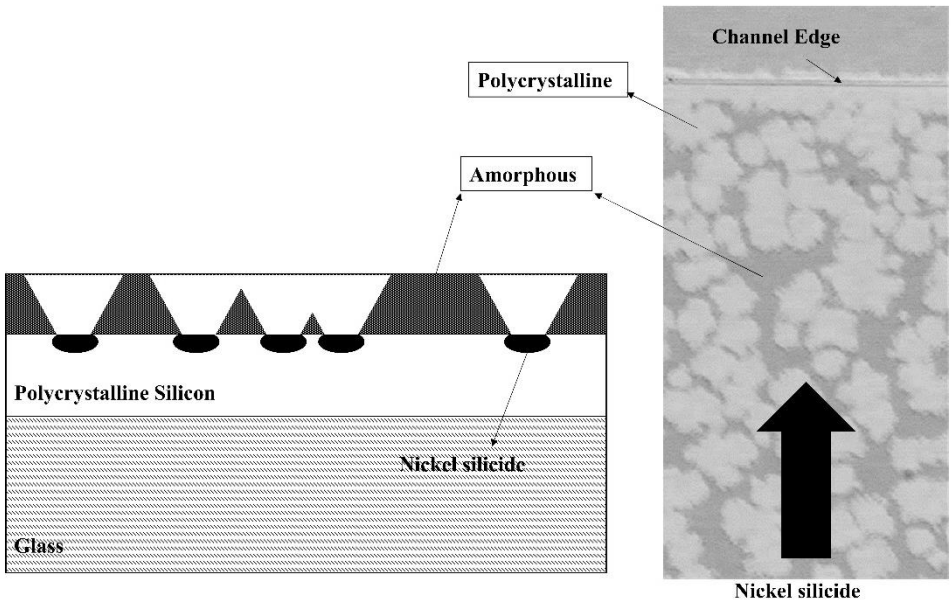


Figure 6-2 Gettering process and microscope optical image of after gettering.

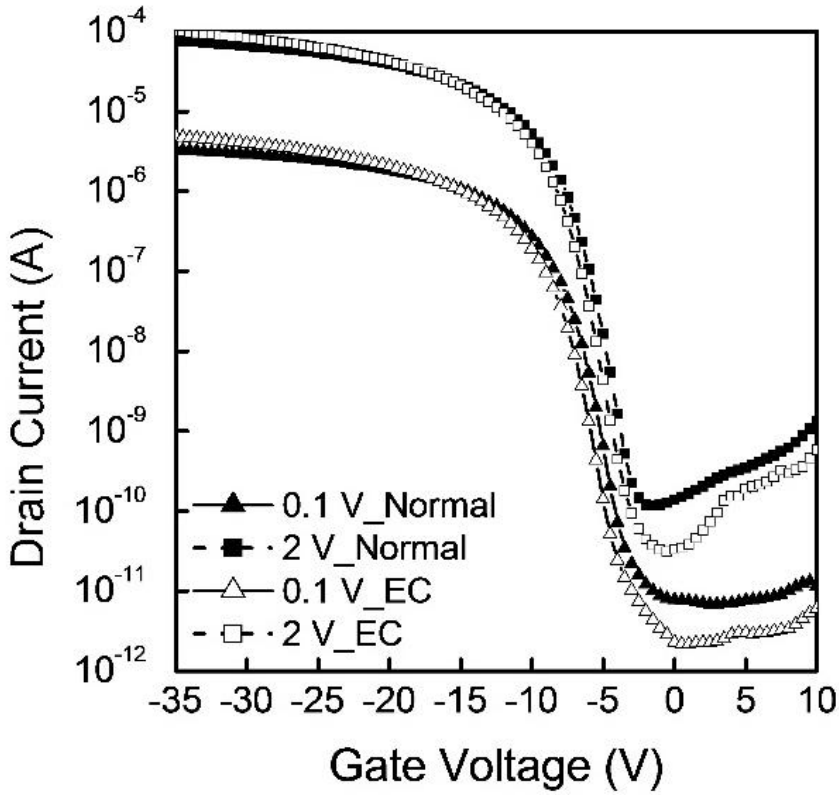


Figure 6-3 Electrical characteristics of normal and edge cut thin film poly silicon transistor at 0.1 and 2 V.

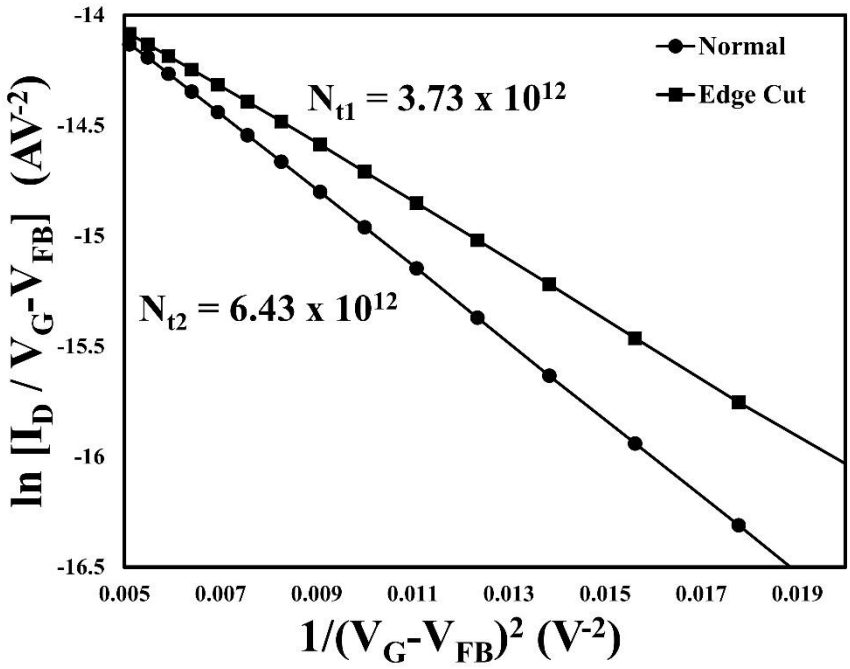


Figure 6-4 Levinson & Proano method to calculate trap state density (N_t) from the current-voltage characteristics

Chapter 7

Conclusion

Metal Induced Lateral Crystallization (MILC) has been investigated for fabricating polycrystalline silicon Thin Film Transistors (TFT). Until now, top gate structure TFTs are manufactured and fabricated for Active Matrix Organic Light Emitting Diode (AMOLED) because of crystallization issue. Excimer Laser Annealing (ELA) crystallization is used for polycrystalline silicon layer in commercial area. ELA need high energy laser exposure step, and this exposure induced thermal damage if there is metal layer below amorphous silicon layer. So before we fabricate bottom gate structure polycrystalline silicon TFTs, we have to find out appropriate crystallization method such as MILC process.

For fabrication of top gate structure polycrystalline silicon TFTs with MILC crystallization process, the furnace annealing at 550 ℃ in

hydrogen ambient is used with Low Pressure Chemical Vapor Deposition (LPCVD). However, in case of Plasma Enhanced Chemical Vapor Deposition (PECVD), crystallization is not observed in hydrogen ambient annealing process. The vacuum annealing process is need for crystallization of PECVD amorphous silicon layer. The silicon hydrogen bonding configuration of LPCVD and PECVD is measured using Fourier Transform Infrared spectroscopy (FT-IR). The results shows that LPCVD has $Si-H_3$ bonding and PECVD has Si-H bonding mainly. The Si-H bonding has higher bonding dissociation energy than $Si-H_3$ bonding. Our group research the PECVD crystallization process, because of bottom gate structure. In order to fabricate the bottom gate structure, LPCVD silicon layer cannot be used because of high deposition temperature.

Using PECVD amorphous silicon layer, bottom gate structure MILC polycrystalline silicon TFTs has been fabricated. The main drawback of MILC polycrystalline silicon layer is metal contamination. MILC need metal catalyst such as nickel and aluminum, so remained metal contamination is inevitable phenomenon. This metal acts as defect center which induce relatively high leakage current because of free carriers. In order to reduce leakage current of bottom gate structure,

we applied two kinds of structure which is called "overlap/off-set structure" and "direct/indirect structure".

1) overlap/off-set structure

With shifting of etch stopper, overlap/off-set structure could be fabricated. To investigate effect of off-set length, for kinds of samples are fabricated (1㎛, 2㎛, 3㎛ and 4㎛). With 2㎛ off-set structure at drain region has the lowest leakage current.

2) direct/indirect structure.

Unlike top gate structure, bottom gate has indirect junction between doped source/drain region and channel inversion layer. In this experiment, direct junction structure is fabricate and measured electrical properties to compare with indirect junction structure. With direct junction structure, relatively high leakage current is obtained, however, with thick intrinsic silicon layer, operation current of indirect junction is decreased dramatically.

Therefore, bottom gate structure MILC polycrystalline silicon TFTs is fabricated with PECVD amorphous silicon layer in vacuum ambient furnace annealing. In order to overcome high leakage current which is induced from metal defect center, overlap/off-set and

direct/indirect structure is investigate. From this result, bottom gate TFTs could be used for manufacturing of AMOLED.

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국문 초록

하부 게이트 구조를 적용한 금속 측면 유도 결정화 다결정 실리콘 박막 트랜지스터의 제작과 누설전류 감소를 위한 연구

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지금 디스플레이 시장은 변화의 과도기를 맞고 있다. 과거 10 여년 전에 CRT 에서 LCD 로 변화한 시점과 같이 지금은 다시 LCD 에서 AMOLED 로 흐름이 변하고 있다. 가장 큰 이유는 높은 해상도에 대한 요구가 커졌고 또한 투명디스플레이, 접히는 디스플레이와 같은 차세대 디스플레이의 개발에 대한 연구도 같이 진행 되었기 때문이다. LCD 는 가장 기본적인 Flat panel Display 로 비정질 실리콘을 이용한 박막 트랜지스터를 기반으로 하는 디바이스이다. LCD 의 특성상 전압 구동 방식이기 때문에 낮은 전계 이동도를 가지는 비정질 실리콘 박막

트랜지스터로도 충분히 구동이 가능하다. 하지만 AMOLED 는 LCD 와 달리 전류 구동이기 때문에 전계 이동도가 높아야지만 충분한 구동이 가능하다. 그러므로 기존의 비정질 실리콘 박막 트랜지스터 (0.5~1 cm^2/Vs) 는 사용이 불가능 하고 다결정 실리콘 박막 트랜지스터(50~200 cm^2/Vs)를 사용해야 한다. 구조적인 관점에서도 LCD 는 기본적으로 bottom gate 를 적용하여 제작하지만 다결정 실리콘은 상부 게이트 구조를 사용한다. 이는 레이저를 이용한 결정화 특성상 상부 게이트 구조만을 이용할 수 밖에 없기 때문이다. 상업적으로 기존의 LCD 생산 라인을 사용할 수 없다는 단점이 존재한다. 그렇기 때문에 이 실험에서는 하부 게이트를 가지는 다결정 박막 실리콘 트랜지스터를 제작하고 그 전기적 특성을 분석하였다.

박막 트랜지스터를 제작하기에 앞서 PECVD 와 LPCVD 의 결정화 차이점에 대해서 연구 하였다. 상부 게이트에서는 LPCVD 비정질 실리콘을 이용하는데 큰 어려움이 없었다. 하지만 하부 게이트 구조로 가면서 LPCVD 를 적용하기에 힘들고 연속 공정이 필요하여 PECVD 사용이 필수적이게 되었다. 그러므로 PECVD 비정질 실리콘의 금속측면유도결정화 조건을 찾기 위한 실험을 진행하였다. LPCVD 와 PECVD 의 박막 특성을 FT-IR 를 사용하여 분석한 결과 PECVD 는 실리콘-수소 결합으로 이루어져 있고 LPCVD 의 경우 실리콘-3 가수소 결합으로 수소들이 존재한다. 즉 PECVD 비정질의 결정화 속도가 느린

이유는 좀더 안정한 결합이 실리콘-수소 결합으로 이루어져 있어 같은 에너지를 가하더라도 쉽게 분해되지 않기 때문에다. 그렇기 때문에 550 도 이상의 온도에서 진공분위기에서 결정화를 진행하면 PECVD 도 충분한 결정화 길이를 가질 수 있음을 알 수 있다.

PECVD 비정질 실리콘을 이용하여 하부 게이트 구조를 가지는 박막 트랜지스터를 제작하였다. 금속측면유도결정화 방식으로 결정화를 하였으므로 실리콘 내부의 금속함량이 높아 상대적으로 높은 누설전류를 가지게 된다. 이 누설전류를 감소시키기 위해 이 실험에서는 두 가지 다른 구조를 적용하여 실험을 진행하였다.

첫 번째 구조는 overlap/off-set 구조이다. 이는 하부 게이트 금속 전극과 도핑된 소스/드레인 영역이 수직적으로 중첩되는 영역을 의미한다. 이 구조를 사용하게 되면 누설전류가 감소하게 된다. 여러 원인이 있지만 off-set 영역에 공핍 영역이 넓어 지게 되어 투과 되는 전자가 줄어드는 것이 큰 이유이다. 두 번째 구조는 직접/간접 접합 구조를 적용하였다. 도핑 된 채널 영역과 채널 영역 간에 접합이 직접적으로 또는 간접적으로 연결 되었을 때 전기적 특성을 분석해 보았다. 간접적으로 연결된 경우 좀더 낮은 누설전류를 가지고 다른 전기적 특성에는 큰 차이가 업었다.

결론적으로 이 실험에서는 다결정 실리콘을 사용한 하부 게이트 구조의 박막 트랜지스터를 제작 할 수 있었고 상대적으로 높은 누설전류를

감소시키게 위해서 overlap/off-set 구조와 직접/간접 접합 구조를 적용하여 성공적으로 누설전류의 감소를 가져올 수 있었다.