Ph.D. DISSERTATION

All-Inkjet-Printed Flexible Organic Thin-Film Transistor / Circuit Fabrication and its Electrical Characterization

잉크젯 프린팅 공정을 이용한 유연성 유기 박막 트랜지스터 및 회로 제작과 전기적 분석에 대한 연구

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SEUNGJUN CHUNG

AUGUST 2012

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지도교수 홍 용 택

이 논문을 공학박사 학위논문으로 제출함

2012 년 8 월

서울대학교 대학원

전기컴퓨터 공학부

정 승 준

정승준의 공학박사 학위논문을 인준함

2012 년 8 월

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Abstract

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SEUNGJUN CHUNG

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTERSCIENCE

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Recently, inkjet-printed organic thin-film transistors (OTFTs) have attracted much attention for low-cost, large area, low-temperature, environmental-friendly and simply processed flexible electronics application, and their performance has improved significantly by designing good organic materials and optimizing fabrication conditions. Although inkjet-printing can be considered as next generation pattering method, and thus many research groups have widely studied for inkjet-

printing organic/inorganic materials for device structure and fabrication process optimization, inkjet-printed layer were only adopted partially to source/drain (S/D) electrodes or semiconductor layer due to difficulty of inkjet-printing process such as nozzle clogging, limitation of material and resolution, difficulty for fine pattern and film uniformity. Because of these technical issues, all-inkjet-printed OTFTs on flexible substrate, thus corresponding circuits typically show poor electrical performance and high voltage operation. In this dissertation, flexible OTFTs and circuit fabrication using inkjet-printing process and several approaches to improve their electrical characteristics are discussed. First, we demonstrated high-performance all-inkjet-printed OTFT array on flexible plastic substrate. For high-performance OTFT fabrication, optimization of the printing and thermal annealing conditions including substrate surface energy, ink-jetting control signals, thermal annealing procedure, and ink properties such as viscosity, speed, surface tension have been studied. From these optimized OTFTs, all-inkjet-printed inverter with p-type OTFTs on flexible plastic substrate was demonstrated. All-inkjet-printed

inverter showed good electrical performance showing high-gain value without any surface treatment by optimizing device structure and fabrication process, and simulation results supported these results. For further electrical performance improvement, surface treatment and interdigitated source/drain electrode structure were adopted. From these optimized conditions and efforts, drive OTFT showed mobility of 0.15 cm^2/V.s, on/off ratio of 2×10^5 and threshold voltage of -1.98 V. The fabricated inverter with a drive OTFT having interdigitated S/D structure showed a full up-down switching performance with a gain of -8.2 V/V at supply voltage of -20 V and a maximum gain as high as -20 V/V at supply voltage of -40 V. In addition, even after 1000-time bending stress test, marginal frequency response up to 50 kHz and an excellent stable performance with gain of -5.5 V/V at -20 V were sustained. Moreover, contact resistance issues and extraction between inkjet-printed silver electrode and organic semiconductors are also analyzed using transmission line method (TLM) and scanning kelvin probe microscopy (SKPM). From the various channel length from 14 to 113 μm, contact resistances of 2.18

MΩ·cm, 0.81 MΩ·cm for spin-coated TIPS-pentacene with inkjet-printed and evaporated silver electrodes were extracted, respectively. To support these results, contact resistances of 1.79 MΩ·cm, 0.55 MΩ·cm for evaporated pentacene with inkjet-printed and evaporated silver electrodes were also reported. Higher contact resistance for inkjet-printed silver electrodes can be explained in terms of their relatively poor surface properties at electrode edge that can cause small molecule grain or slight oxidation of surface during the printed silver sintering process. To improve contact properties, surface treatment using chemically-coupled PS-brush layer between inkjet-printed silver electrode and organic semiconductor was adopted, and this layer improve not only OTFT electrical performance but also contact properties showing potential drop reduction at contact region from SKPM analysis.

Furthermore, we also report high-performance and stable inkjet-printed stretchable silver electrodes for inkjet-printed stretchable OTFT fabrication. Highly conductive silver electrode was deposited directly on a ultra-violet ozone treated polydimethylsiloxane (PDMS) substrates having vertical wavy structures to enhance

adhesion between printed silver lines and PDMS surface resulting in high stretching performance. During slow (16.7 μm/sec) stretching test, resistance of the printed silver electrode was increased only by three times at 30 % tensile strain. Inkjet-printed silver electrodes also showed good mechanical stability during 1,000-time fast (1 mm/sec) cycling test with 10 % tensile strain, showing maximum resistance change of less than 3-time.

Keywords: Inkjet-printing, Organic semiconductor, Organic Thin-film transistor, flexible OTFT, Silver electrode

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Chapter 1

Introduction

1.1 Motivation and Overview

After transistor invention, information display technology has been developed dramatically allowing much smaller device size. Especially, silicon based transistor lead to significant improvement for computing device, sensor, memory device and expanding other electronic application. As these technologies are further improved, the demands for thinner / lighter device on flexible and rugged substrate using low-cost and simple fabrication process are increased for rollable, bendable and wearable device / circuit fabrication. Although thin film transistor (TFT) is necessary for flexible electronics, especially display application, high-temperature, high-vacuum and various chemical treatment for patterning and etching processes required for conventional silicon device fabrication are incompatible with flexible substrate such

as plastic or steel substrate. To overcome these issues on fabrication processes, organic field-effect transistors (OFETs) have attracted much attention to substitute amorphous silicon (a-Si) TFT for large area flexible electronics application in low-temperature process and their performances have improved significantly by designing good organic materials and optimizing fabrication conditions organic thin-film transistors. Since first demonstration of field-effect conduction using small molecular organic semiconducting materials in 1964 [1], their interests for active layer deposition in OTFT device have increased significantly due to its easy processing capability, large-area process, light weight, low-temperature manufacturing, and excellent flexibility. Although OTFT also has many disadvantages or technical issues such as poor mobility, switching performance, uniformity and stability, its electrical characteristics have improved dramatically showing better mobility than that of a-Si (0.5 - 1 cm^2 /V.s) during the last ten years [2]-[5], electrical performance is improved to demonstrate active-matrix organic light-emitting diode (AMOLED) display successfully.[6]-[7] Generally, for OTFT fabrication, although vacuum deposition and photo-lithography processes are widely used to deposit each layer and obtain the electrode or gate dielectric patterns, high vacuum system, various shadow masks and photo-patterning using photo-resist (PR) are the obstacles to realize low-cost, large area display applications with simple process. Moreover, conventional photolithography processes using several photo-

masks, toxic gas and organic solvent are very complex, time consuming and not environment-friendly process resulting in high-cost product. Therefore, solution process, especially direct-printing process is regarded one of the most promising candidates to substitute conventional vacuum processes due to its low-temperature, ultra-low-cost, maskless and easy process capabilities compared with conventional vacuum deposition device fabrication methods which is important in implementing ultra-low-cost, flexible, large-area electronic devices such as interconnection, organic thin-film transistors (OTFTs), polymer light-emitting diode (PLED) and radio frequency identification (RFID) tag [8]-[12], and it is also compatible process on flexible plastic substrate [13]-[15]. Various printing techniques have been also widely used in the printed electronics industry, including screen printing, offset printing, gravure, flexography, and eventually roll-to-roll process is expected for high-throughput systems.

As shown in figure 1.1, inkjet-printing process is much simpler without any material waste and contamination from mask contact or PR deposition / strip compared with conventional photolithography. Because of these powerful advantages, inkjet-printing method is widely used for OTFTs fabrication to deposit electrodes or active layers resulting in simple and low-cost device on flexible substrate. Although all-inkjet-printed devices have been reported in 2008 and 2009 [16]-[17], their electrical performances were not suitable for device application

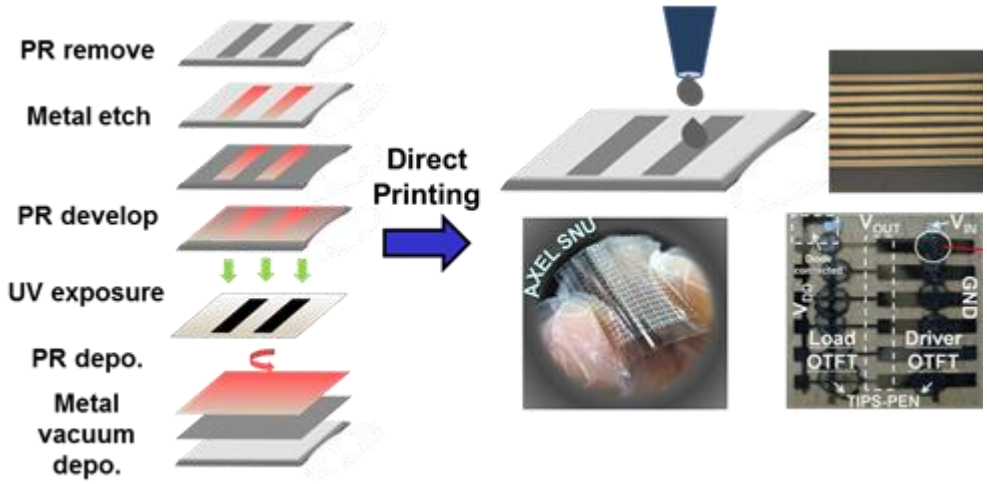


Figure 1.1 Inkjet-printing process comparing with conventional photolithography patterning

because of low mobility of 0.002 and 0.0035 $cm^2/V{\cdot}s$ and on/off ratio of 10^3. To fabricate high performance electrical devices, inkjet-printing process has been typically applied to only a part of the TFT structure in terms of source/drain (S/D) electrodes or active layer because of poor reliability, low-resolution, limitation of materials, surface roughness properties of the inkjet-printed layer, adhesion properties between inkjet-printed layers although the inkjet-printing process itself is simple and cost-effective [8]-[11]. Therefore, most of other researchers fabricated solution processed OTFTs using spin-coated polymer insulation layer on patterned gate electrodes such as indium-tin-oxide (ITO), chromium (Cr), aluminum (Al) or

heavily doped silicon/SiO_2 substrates for high device performance [13], [15], [18]-[19]. In 2011, all-inkjet-printed OTFTs having mobility of 0.06 cm^2/V.s and 0.01 cm^2/V.s are also reported, more improved electrical performance is necessary to demonstrate more complex circuit application. [9], [20] Moreover, inkjet-printing method has critical disadvantage for high resolution electronic applications in comparison with photolithography method due to nozzle size limitation, surface energy matching adhesion properties between each layers, surface tension and viscosity of limited ink materials which determine that it can be printed. In addition, poor uniformity in terms of coffee ring effect and edge waviness of metal electrodes can affect to device electrical performance.[21] Therefore, inkjet-printed metal line should be guaranteed high resolution, high conductivity, good uniformity and reliability for electrical and mechanical properties for flexible electrical device applications. Although high conductive silver line with 40 μm line width on flexible arylite substrate and OTFTs using 50 μm line width and channel length on silicon substrate were demonstrated using inkjet printing method in 2008 and 2009 respectively,[22]-[23] the demands of inkjet-printing technology for more narrow and uniform conductive line are increasing to substitute conventional photo-lithography technology.

In this thesis, we report inkjet-printing process optimization for low-cost all-inkjet-printed OTFT / circuit applications and its electrical characteristics analysis. To overcome above mentioned technical / material issues, carefully optimized materials and process conditions were adopted. Moreover, by adopting optimized structure and surface treatment between gate dielectric layer, S/D electrodes and semiconductor layer to improve interface characteristics, we obtained better OTFT and inverter electrical performances which are comparable with those of conventional vacuum deposited OTFTs. Their electrical characteristics are analyzed by various approaches from electrical and material point of views. Furthermore, we also investigate the contact properties and its improvement for high-performance electrical application. Finally, we report the potential of stretchable printed electronics by showing high-performance inkjet-printed stretchable electrode.

1.2 Materials and Equipment for Inkjet-Printed Organic Thin-Film Transistor (OTFT) and inverter

Electronic ink is classified to organic/inorganic ink according to material properties and conductive / insulating / semiconductor ink according to their electrical properties. In this chapter, we report the electronic inks and inkjet-printing systems for OTFT and circuit fabrication on flexible substrate.

1.2.1 Conductive Ink Materials

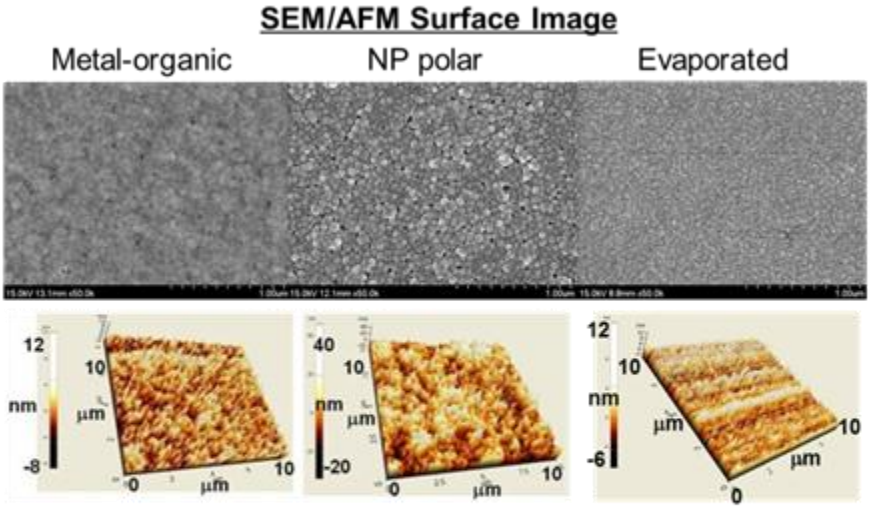
Since conductive ink is typically used as gate and S/D electrode in TFT structure as well as interconnection, conductive ink should be guaranteed its conductivity. Moreover, low-cost, low-energy barrier for carrier injection to semiconductor layer, good surface roughness and low sintering temperature are necessary for high-performance OTFT fabrication on flexible substrate. In addition, clean edge formation in S/D electrode is also required to obtain uniform electrical field which affect TFT electrical performance.[21] By considering these requirements, metallic, conductive polymer and carbon based conductive inks are most promising candidates. Among these conductive inks, although conductive polymers have been studied by many research groups due to its low-cost, low-temperature process and good flexibility for electrode applications, their resistivity

is much higher than that of metal electrodes, and thus it is hard for polymers to be applied to display backplane or other integrated circuits due to very high RC-delay in spite of conductive polymers such as poly(ethylenedioxythiophene)/ poly(styrene sulfonic acid) (PEDOT/PSS) and polyaniline (PANI) which have shown good conductivity for electrodes of TFTs since conductivity of doped-polyacetylene was reported in 1977. [13], [24]-[27] Although carbon based conductive materials such as graphene and carbon nanotube (CNT) are also regarded as one of promising candidate for electrode or interconnection due to its good strength and flexibility, more stable and well-dispersed carbon based inks having higher conductivity are required to adopt display backplane application.[28]-[32].

Metallic ink has great potential to adopt for printed electronic application due to its high conductivity, stability and disperse property. There are two types of metallic ink. One is metal-organic precursor ink, and the other is nanoparticle ink. In metal-organic precursor ink, soluble metal cluster and complex are dissolved in organic solvent in molecular scale which is reduced over sintering temperature. Therefore, metal-organic precursor ink has transparent appearance and little nozzle clogging. Moreover, after metal-organic precursor ink is thermally reduced, it has good surface roughness comparing with that of nanoparticle ink. However, inkjet-printed silver electrode using metal-organic precursor ink has low aspect ratio due to limitation of metal contents, and requires relatively high temperature comparing

with nanoparticle ink because thermal energy over reduction temperature is essential to obtain conductive metal film. On contrast, in nanoparticle ink, metal nanoparticles such as gold, silver, copper and nickel having diameter of tens of nanometers are dispersed in organic solvent. Therefore, by controlling metal contents in organic solvent, high-aspect ratio electrode implementation is obtained easily. As figure 1.2 shows the scanning electron microscope (SEM) and atomic force microscopy (AFM) images for inkjet-printed silver film using metal-organic precursor ink and nanoparticle silver ink, and thermally evaporated silver films for reference, inkjet-printed thin-film using metal-organic precursor ink has better surface roughness of 2.12 nm in root-mean-square (RMS) value which is comparable with that of thermally evaporated silver film. However, inkjet-printed silver film using nanoparticle ink which has silver contents of 35 wt% has much poor surface morphology property showing surface roughness of 10.18 nm in RMS value. In this dissertation, from these results, we conclude that metal-organic precursor silver ink is more suitable to fabricate OTFT electrodes.

Although gold nanoparticle (Au NP) inks can produce electrodes with high work function (5.1 eV) that is well matched with the organic semiconductor materials HOMO (highest occupied molecular orbital) level (5.07~5.3 eV), many research groups have used various types of silver inks. [17] [23], [33]-[34] It is noted that bottom-contact structure that has been widely used for all-printed OTFT



Scan size (10 µm X 10 µm)	Metal-organic	NP polar	Evaporated
Peak-to-Valley (nm)	18.65	80.20	16.27
Root-Mean-Square (nm)	2.12	10.18	2.04

Figure 1.2 SEM / AFM images and surface roughness values for inkjet-printed silver film using metal-organic precursor and nanoparticle inks and thermally evaporated silver film for reference

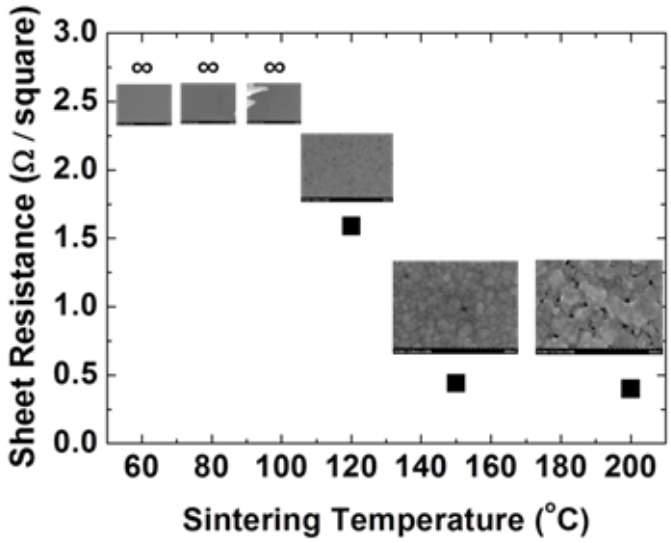
implementation,[9], [20], [23] additional treatment processes are typically required for both silver and gold electrodes for high device performance. Therefore, the electrodes work function is not the only major factor for device performance improvement. In addition, metal-organic precursor Ag ink has the following three advantages: Material cost, low-sintering temperature, surface roughness. Au NP ink is generally more expensive than silver ink. Moreover, since Au NP ink is not widely commercially available yet, many research groups are using home-made gold NP ink for source/drain (S/D) electrode deposition. For bottom contact structures, OTFTs with silver S/D electrodes show comparable electrical performance in terms of mobility and on/off ratio with the previously reported results.[35]-[37] In addition, silver ink sintering process can be performed easily at low temperature. On the other hand, in previously reported results, the printed electrodes using Au NP ink need to be sintered using laser processing systems [16] or at high temperature (~250 ℃) [36]. Commercial metal-organic silver ink was printed on low-temperature substrate and sintered in a convection oven and at relatively low-sintering temperature of 150 °C, resulting in a few μΩ·cm resistivity. Therefore, silver ink can be considered to be suitable device fabrication on flexible plastic substrate. Moreover, the metal-organic type silver ink produces good surface roughness in the printed electrodes. It is well noted that surface roughness can affect electrical performance of OTFT. From our experiments, surface roughness of the inkjet-printed silver electrodes

using NP ink showed much larger than that of inkjet-printed silver electrode using metal-organic precursor type silver ink as above mentioned.

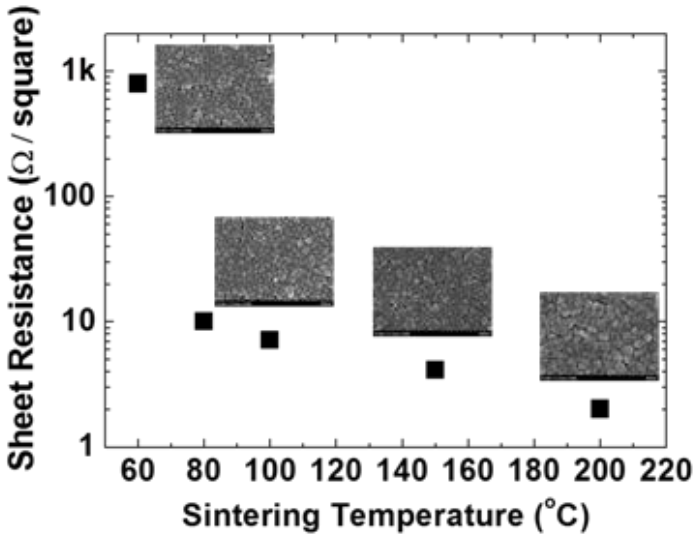
Figure 1.3 shows effect of sintering temperature on resistivity of silver film for metal-organic precursor and nanoparticle inks. Because metal-organic precursor ink required sintering temperature over silver cluster and complex reduction temperature to obtain conductive silver film, its resistivity sintered under 120 ℃ is almost infinite. As temperature is increased, silver cluster and complex are reduced resulting in large silver grain corresponding significant resistivity decrease. On contrast, nanoparticle ink required only the enough temperature to evaporate organic solvent and aggregate the silver nanoparticle for resistivity reduction. Therefore, the electrical conductivity of inkjet-printed silver film sintered at 60 ℃ is also measured although its resistance value is somewhat high. As sintering temperature is increased, its conductivity is also increased by reducing grain boundary corresponding large silver grain which indicates that sintering temperature dominantly determines conductivity of silver film. From these experiment results, we conclude that metal-organic precursor ink required the high temperature over critical reduction temperature. On the other hand, although there is no critical sintering temperature, as sintering temperature is increased, film conductivity is also increased in case of nanoparticle ink. Therefore, these two types of silver ink can be adopted by considering process conditions and purpose such as coefficient of thermal expansion

of substrate or maximum process temperature.

In addition, high-aspect ratio of printed silver film is also important for low resistive electrode or interconnection to reduce RC-delay on display backplane or integrated circuit. To get high aspect ratio inkjet-printed film, there are two methods; one is drop spacing reduction which means the distance reduction between each drop, and the other is multi-times printing. Between these methods, multi-times printing is more effective to obtain high aspect ratio from our experiment, and it will be further discussed at chapter 2.4. Figure 1.4 shows the effect of multi-time printing on aspect ratio of inkjet-printed silver film for metal-organic precursor and nanoparticle inks. In metal-organic precursor ink, multi-times printing mainly fills the void on films from solvent evaporation due to low silver contents resulting in small thickness increase. On contrast, in case of nanoparticle ink, as printing times increase, the film thickness is also increased by stacking each layer. Therefore, silver ink choice is important for its application demands.

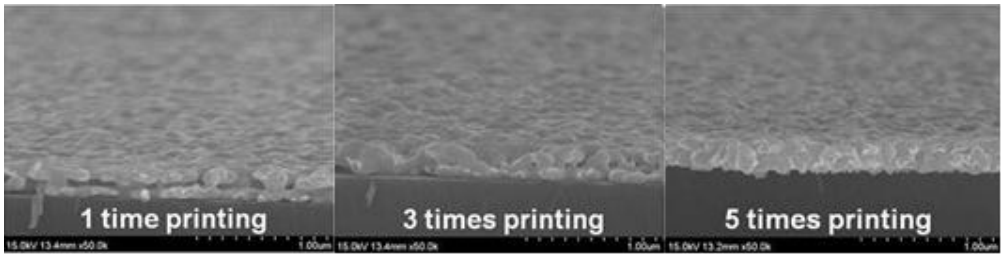


(a)

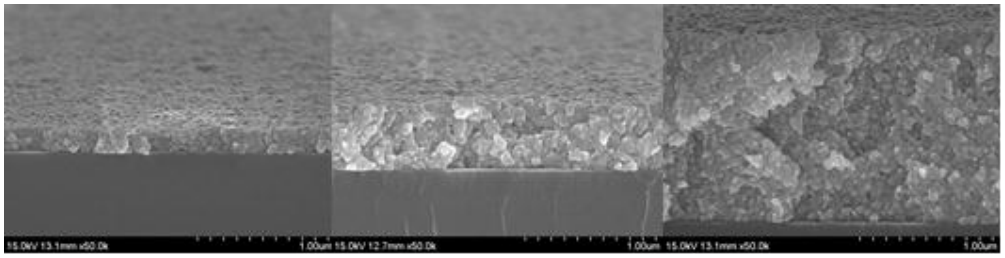


(b)

Figure 1.3 Effect of sintering temperature on resistivity of inkjet-printed silver film for (a) metal-organic precursor and (b) nanoparticle inks



(a)



(b)

Figure 1.4 Effect of multi-time printing on aspect ratio of inkjet-printed silver film for (a) metal-organic precursor and (b) nanoparticle inks.

1.2.2 Dielectric Ink Materials

Gate dielectric layer properties dominantly affect OTFT performance because it is not only to insulate between the gate and, the semiconductor layer and the S/D electrodes, but also determine the molecular ordering of the organic semiconductor where the channel area for charge transport. Therefore, high-quality gate dielectric should be guaranteed the good insulating performance, low unwanted impurity, low trapping site and smooth surface roughness. Moreover, its interfacial matching, especially surface energy matching is also critical to avoid dewetting or swelling phenomenon during upper layer deposition in solution process. The gate dielectric layer materials are classified in two types: one is inorganic and the other is organic material. In recent years, several inorganic metal oxide materials, such as magnesium oxide, titanium dioxide, and barium titanate [38]-[40], have been used as high-permittivity materials for low power consumption TFT or integrated circuit fabrications. In addition, by adopting self-assembly-monolayer (SAM), high-performance OTFTs under low operation voltage are also widely studied. [41]-[42]. Although, these advantages of solution processed inorganic gate dielectric materials or surface treatment lead to high-performance OTFT and circuit demonstration, more improved insulating performance comparing with organic and vacuum evaporated dielectric layer is required. Moreover, they are not suitable on flexible

plastic substrate due to high-temperature process over 200 ℃ and its poor flexibility. Therefore, many technical issues are remained to adopt all-inkjet-printed electrical application.

Organic gate dielectric materials are the most promising candidates for printed electronic application. The most commonly used soluble organic dielectric materials are cross-linked poly(4-vinylphenol) (PVP), polyvinylalcohol (PVA), Poly(methyl methacrylate) (PMMA) and polystyrene (PS) which required relatively low curing temperature under 200 ℃ showing good electrical insulating performance [6], [9], [43]-[44] (Fig.1.5). To adopt these materials on printed electronics, its viscosity and surface tension should be optimized for well-jetted ink droplet by controlling their concentration and crosslinking agent which is cross-linker of the PVP molecular with high viscosity. Moreover, curing conditions critically affect gate dielectric layer surface which determines the interfacial properties. To obtain high-performance printed gate dielectric layer, coffee ring effect-free on printed area edge and good surface roughness without pin-hole which also determine leakage characteristic should be guaranteed. (This study is reported at chapter 2.3) [45]. In effort for high-performance electronic application, although many research groups also widely studied for high-k polymer dielectric such as cyanoethylpullulan and poly(vinylidene fluoride/trifluoroethylene) [P(VDF–TrFE)] and low-k polymer dielectric such as benzocyclobutene (BCB) due to their high-

permittivity and being less susceptible to ionic impurities, respectively,[46]-[47] more researches for better insulating performance and permittivity characteristics are required.

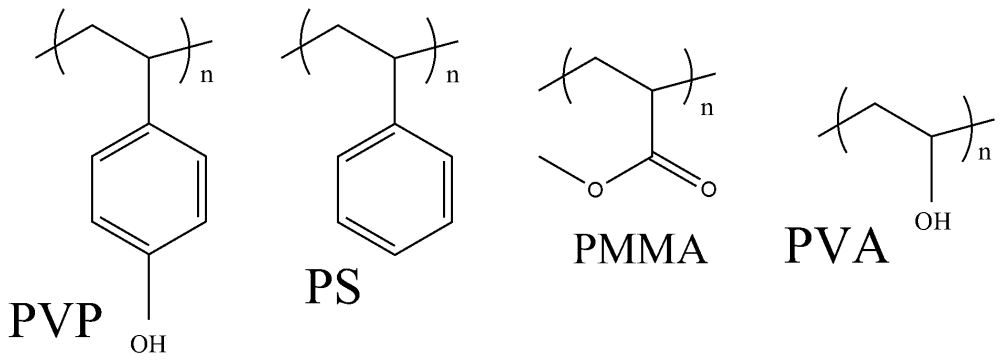


Figure 1.5 Organic dielectric materials

1.2.3 Semiconductor Ink Materials

For several decades, electrical performance of organic semiconductor materials based on π-conjugated molecule are improved significantly, and it has been adopted on e-paper or other display applications.[6]-[7], [19] Among these materials, pentacene is one of the most promising candidates due to its high mobility up to 5 cm^2/V.s.[48] However, pentacene film was only achieved by high-cost vacuum deposition due to its insolubility in organic solvent. Therefore, pentacene cannot use in inkjet-printed applications. Although as soluble organic semiconductor, polymeric organic semiconductor such as P3HT, F8T2, F8BT and PQT12 conjugated polymer have been also attracted much attention to substitute pentacene, [13], [49]-[51] their electrical performances, especially carrier mobility is poor to adopt electronic application. Thus, for high-performance soluble organic semiconductor, 6, 13-bis(triisoprophylsilylethynyl) pentacene (TIPS-pentacene) was developed (Fig 1.6).[52] Two bulky functionalized groups are attached at pentacene backborn permanently which enable the molecules to be dissolved in organic solvent. Moreover, these attached functionalized groups also induce strong π-stacking of the molecules to enhance intermolecular orbital overlap resulting in high mobility > 1cm^2/V.s, and in recent years, inkjet-printed double shot using orthogonal solvent TIPS-pentacene OTFT having 16 cm^2/ V.s was reported [53]-[54]. In addition, it is

compatible on flexible substrate due to low annealing and drying temperature. Although soluble pentacene-precursor semiconductor also has attracted much attention which is un-functionalized pentacene readily transformed into pentacene upon heating near 200 ℃, high-temperature annealing during > 1 hour causes film degradation resulting in poor electrical performance. For high-performance OTFT fabrication with TIPS-pentacene active layer, many research groups have studied to optimize TIPS-pentacene deposition conditions such as solvent dependency, annealing temperature and ambient conditions. In addition, various surface treatments on gate dielectric layer and S/D electrodes such as hexamethyldisilazane (HMDS) and pentaflorobenzenethiol (PFBT), blended TIPS-pentacene with PS or p-type polymers are also reported. [15], [19], [41]-[42] In 2011, although solution-processed silicon TFT is also demonstrated using liquid silicon [54], their processes required highly complex photolithography process in high temperature to obtain single silicon grain. Therefore, it is difficult to adopt large-area flexible platform.

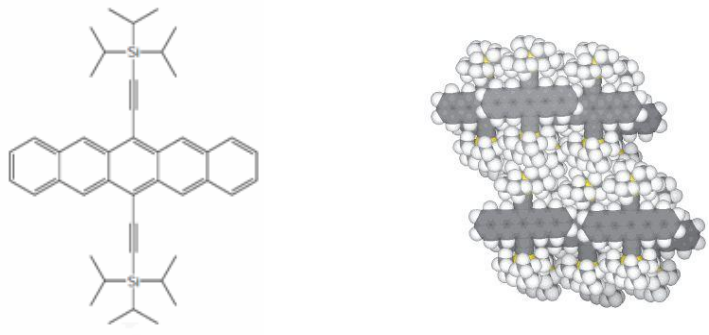


Figure 1.6 Chemical structure (left) and solid-states ordering of TIPS-pentacene (right) [52]

1.2.4 Inkjet-Printing Systems

The experiments in this thesis were performed by using piezoelectric (drop-on-demand) inkjet-printer DMP-2831 model which enables multi-nozzle printing on various substrate temperatures up to 60 ℃. The ink-cartridges are classified 10 picoliter (pl) and 1 pl cartridges determined by nozzle diameter. Nozzle diameter of 10 pl and 1 pl cartridge are 21 μm and 9 μm corresponding drop size are about 50 μm and 25 μm in case of silver ink on PVP insulator layer, respectively. (These results are dependent on ink material and surface energy of substrate.) To obtain the well-inkjet-deposited thin-film, many inkjetting and thermal conditions are optimized including ink material, sintering/curing temperature, substrate temperature, surface energy, and the voltage waveform. In these conditions, voltage waveform is regarded as the most important parameter to obtain fine-defined ink droplet. The voltage waveform is applied to expand or shrink the piezoelectric-plate to eject the ink from the reservoir which is determined by the ink conditions such as its viscosity, surface tension and boiling point. Figure 1.7 shows the sequence of inkjetting process depending on the applied waveform. In start state, piezoelectric plate compresses slightly to prepare the inkjetting. In first phase, piezoelectric plate is back to a neutral state showing nozzle meniscus. Then, as applied voltage is increased, piezoelectric plate compresses the reservoir resulting to eject the ink. After ink droplet is ejected, piezoelectric plate is back in step by step to obtain well-

defined ink droplet without long ink tail. Detail voltage waveform parameters such as voltage increment gradient, duration, and a number of steps are determined by ink viscosity, boiling point, and surface tension. By optimizing these conditions, well-defined ink droplet from multi-nozzle was obtained resulting in high-quality inkjet-printed thin-film formation.

Because the maximum temperature of substrate (~ 60 ℃) is insufficient for in-situ sintering the conductive or insulating inks, convention oven and programmed furnace are used for conductive Ag ink and PVP insulting ink thermal annealing in ambient condition, respectively.

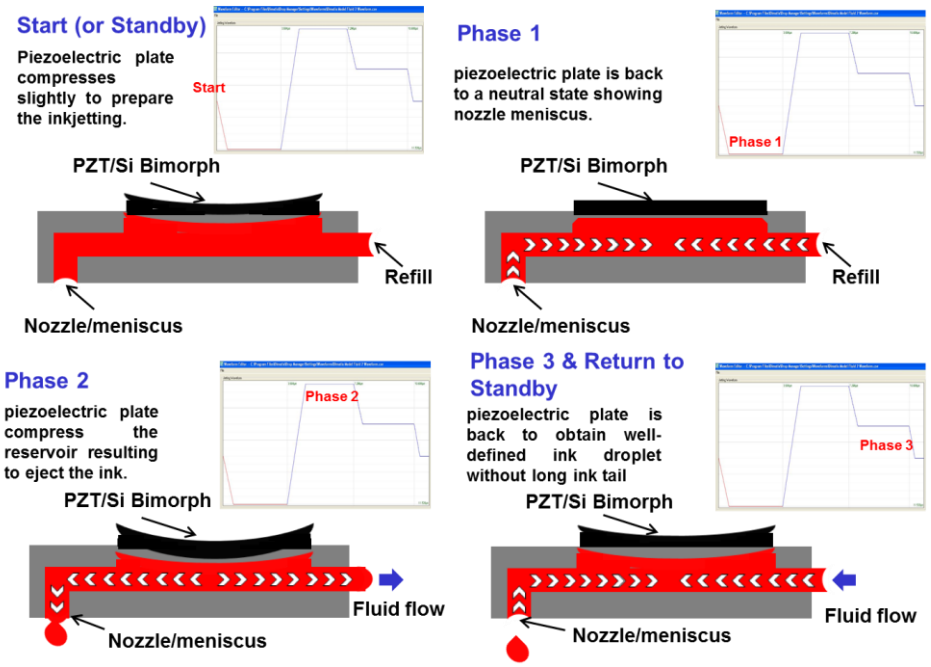


Figure 1.7 Ink ejection process depending on voltage waveform changes corresponding piezoelectric plate compression / decompression. [56]

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Chapter 2

All-Inkjet-Printed OTFT Array on Flexible Substrate

2.1 Introduction

Recently, organic thin-film transistors (OTFTs) have attracted much attention for large area, low-temperature flexible electronics application, and their performance has improved significantly by designing good organic materials and optimizing fabrication conditions [1]-[5]. In addition, in order to further reduce the fabrication cost and to further simplify the fabrication process, a direct inkjet-printing process has been widely used in ultra-low-cost, flexible, large-area electronics applications. Since the direct inkjet-printing process can be easily

adapted to TFT fabrication processes, optimization of the printing conditions including substrate surface energy engineering, ink-jetting control signals, thermal annealing procedure and ink formulation have been studied a lot to improve OTFT performance [1]-[5].

However, in most cases, inkjet-printing process have been typically applied to formation of source/drain electrodes or an active semiconductor layer in a bottom contact TFT structure because there are, in general, limitations in reliability, resolution, available material, surface roughness of the inkjet-printed layer and adhesion between inkjet-printed layers [3], [6]-[8]. First of all, inkjet-printing method has critical disadvantage for high resolution electronic applications such as narrow source/drain pattering for TFT or electrical wiring in comparison with photolithography method due to nozzle size limitation, adhesion properties between each layer, surface tension and viscosity of limited ink materials which determine that it can be printed. Therefore, although all-inkjet-printed devices have been reported only recently [9], [10], electrical performances are relatively poor in comparison with the conventionally fabricated OTFTs using a vacuum or a spin-coating process. To implement high performance all-inkjet-printed OTFTs, highly conductive electrodes and gate dielectric layer with good insulating and surface roughness properties are required, which can be obtained from optimization of the ink formulation, inkjet-printing process and their thermal annealing conditions.

Moreover, although highly conductive silver line with 40 μm line width on flexible arylite substrate and OTFTs using 50 μm line width and channel length on silicon substrate were demonstrated using inkjet printing method in 2008 and 2009 respectively [7], [11], the demands of inkjet-printing technology for narrower and uniform conductive line are increasing to substitute conventional photo-lithography technology.

In this chapter, we report all-inkjet-printed OTFTs with silver electrodes as gate and source/drain electrodes. Although soluble conductive polymers such as Poly(ethylenedioxythiophene)/ poly(styrene sulfonic acid) (PEDOT/PSS) and polyaniline (PANI) showed good performance for electrodes of OTFTs [1], [12], their high resistivity can limit application of polymeric conductors only to contact electrodes. Therefore, highly conductive metal ink such as silver ink is preferred in both contact and line electrode application. By optimizing inkjet-printing and annealing conditions, we obtained reasonably good device performance from OTFTs with silver electrodes, and organic dielectric layer. From these optimized processes, we also report high resolution and uniform conductive line formation on flexible substrate and its applications to OTFTs array using inkjet-printing method. To overcome above mentioned problems and fabricate high-performance narrow conductive line, we have studied optimized inkjetting from 1 picoliter (pl) cartridge which have 9 μm diameter nozzles and sintering conditions on flexible plastic

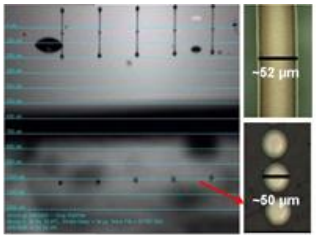
substrates. From carefully optimized inkjetting and sintering conditions, we obtained highly uniform and conductive narrow line with width of from 25 to 38 μm and thickness of from 70 to 320 nm by increasing inkjet-printing time. In additions, electrical and mechanical stress tests were performed to adopt high-power and flexible electronics. Finally, we fabricated all-inkjet-printed OTFTs arrays with 2-time-printed narrow source/drain electrodes on flexible plastic substrate corresponding very short average channel length of 11 μm which results show smallest channel length using commercial inkjet-printing system.

2.2 Inkjet-Printing Materials and Processes Optimization for OTFT Fabrication on Conventional Glass Substrate

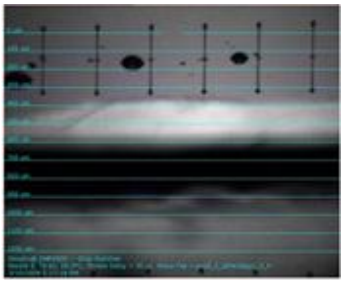
For all-inkjet-printed OTFTs fabrication, we used bare glass (Eagle 2000TM) substrates cleaned by a standard solvent cleaning process (acetone, isopropylalchol, and deionized water sequentially in an ultrasonic bath during 20 min, respectively) and it was dried at 200 °C in a convection oven for 30 min. For bottom gate electrode formation, a transparent metal-organic precursor type ink, INKTEC TEC-IJ-010, which has 15 wt% silver contents and viscosity from 9 to 15 cps, was inkjet-printed by using a piezoelectric (drop-on-demand) inkjet-printer (Dimatix DMP-2831). Substrate temperature was maintained at 60 °C during the inkjet-printing process to vaporize silver ink solvent quickly, resulting in better surface properties, film uniformity and shiny appearance. Inkjetting conditions were carefully optimized to obtain a highly conductive layer by controlling a waveform voltage, a cartridge temperature, an ink drop velocity and a fire frequency considering silver ink properties. The silver ink was printed with a drop velocity of about 5 m/s, and a drop spacing of 25 μm which means distance between ink drops. These two parameters determine thickness and width of the silver electrodes. Figure 2.1 (a) shows capture images of ink droplet and drops that formed a well-defined electrode. After the gate electrode was printed, the substrate was annealed at 150 °C for 30 min

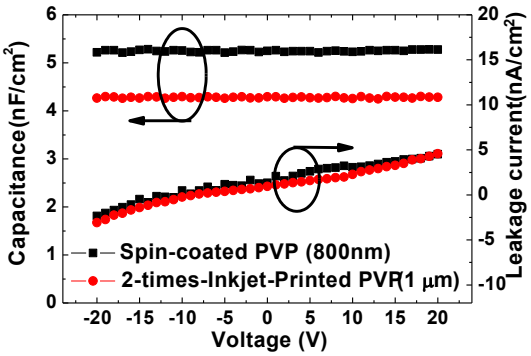
in convection oven under atmospheric environment. We obtained a sheet resistance of 0.2 Ω/□ from the 200 nm thick silver electrodes, which corresponds to specific resistance of 4 μΩ·cm. On the fabricated silver gate electrode, poly(4-vinylphenol) (PVP) solution was inkjet-printed to form a gate dielectric layer. Cross-linked PVP is one of the most widely used organic insulation layer materials due to its good insulating performance and relatively low-temperature thermal curing condition. However, PVP solution jetting conditions should be optimized to obtain a well-defined gate dielectric layer because PVP solvent can easily result in cartridge nozzle clogging. PVP solution was composed of 10 wt.% of PVP and 2 wt.% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) dissolved in propylene glycol methyl ether acetate (PGMEA) as a solvent. All chemicals were purchased from Sigma-Aldrich. PVP and CLA concentrations are critical factors to make a spherical shape of ink droplets which help forming a well-defined gate dielectric layer [Fig. 2.1 (b)]. It is noted that relative composition of these two materials determines viscosity and insulation properties of the PVP and surface energy property of the printed films [13]. PVP solution was inkjet-printed at room-temperature in order to prevent fast solvent evaporation which was found to degrade the quality of the printed film. Drop spacing of 25 μm was used for uniform dielectric film formation. To further improve surface and insulation property, we inkjet-printed two times producing 1 μm thick PVP layer. Ramping up to 200 ℃

followed by 2-h soaking process was used, which produced a well-defined PVP gate dielectric layer with 4.3 nF/cm2 and less than 0.5 nA/cm2 at 0.2 MV/cm. The inkjet-printed PVP layer shows electrical characteristics similar to the spin-coated PVP layer as shown in Fig. 2.1 (b). Root-mean-square (RMS) value of surface roughness of the printed PVP layer was smaller than 4.1 nm for 10 μm by 10 μm scan area. After PVP dielectric layer was fabricated, silver source/drain electrodes were inkjet-printed by using the same conditions as those used for the gate electrode formation. Channel width (W) and length (L) of the fabricated OTFTs were 250 and 60 μm, respectively. Finally, 1 wt.% of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) dissolved in 1,2-dichlorobenzene was inkjet-printed at room temperature to form 2 × 2 mm2 active layer. Figure 2.1(c) shows optical capture image of the TIPS-pentacene ink drops and molecular structure of TIPS-pentacene.

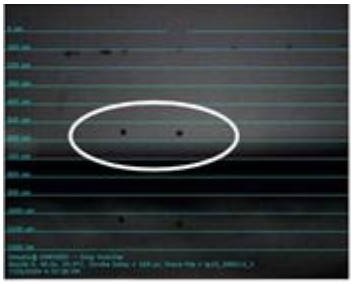


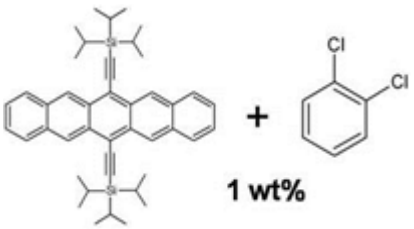
(a)





(b)





(c)

Figure 2.1 Optical capture images for (a) silver ink drop and silver line (b) PVP solution drop and inkjet-printed PVP insulation performance comparing with that of spin-coated PVP layer (c) TIPS-pentacene drop from 10 pl cartridge with 21 μm diameter nozzles

It is noted that no surface treatment of the gate dielectric layer was used because PVP layer shows good interface characteristics with TIPS-pentacene [14]. TIPS-pentacene is one of the most widely studied p-type organic semiconductor materials due to its high electrical performance and solubility in various organic solvent [1], [3], [15], [16]. To analyze the active layer formation method effect on OTFT electrical performances, TIPS-pentacene active layers were also formed at room temperature using spin-coating and drop-cast methods. In both cases, the active layers were not defined. After the TIPS-pentacene deposition, all films were dried in air at room temperature for an hour to maintain solvent rich environment during the solvent evaporation process. Thicknesses of the inkjet-printed, spin-coated, and drop-cast TIPS-pentacene layers were 280, 70, and 320 nm, respectively. Because 1,2-dichlorobenzene, which is an aromatic solvent, has a high-boiling-point, there will be enough time for molecules to self-assemble forming a highly ordered structure after the solvent was evaporated completely [6], [16]. We also fabricated OTFTs with the same structure, but with pentacene active semiconductor layer to compare interface properties between semiconductor and gate insulator layers. Pentacene was deposited using a thermal evaporator at 10-6 Torr on 60 °C substrate, with a deposition rate of 0.3 Å/s. The pentacene active area was defined by shadow mask as 1.5mm by 1mm and its thickness was 60 nm. Figure 2.2 shows optical microscope images of the fabricated OTFTs. It is noted that there are some

structures in the inkjet-printed [Fig. 2.2 (a)] and drop-cast [Fig. 2.2 (c)] films in comparison with the spin-coated [Fig. 2.2 (b)] one. We believe that spinning and drying during the spin-coated process can affect the crystalline structure formation, resulting in rather uniform and small crystalline structure for the spin-coating films. Details of the crystalline structure for the films will be discussed later. In all-inkjet-printing processes, inkjet-cartridge with 21 μm diameter nozzles and a capacity of 10 pl ink were used.

To measure the electrical properties of the OTFTs, current-voltage (I-V) characteristics of the fabricated OTFTs were measured in a dark box using Agilent 4155C semiconductor parameter analyzer. Thicknesses and surface profiles of metal and organic layers were measured using both TENCOR Alpha-step 500 and atomic force microscopy (AFM) from Park System. X-ray diffraction (XRD) measurements of the pentacene and the TIPS-pentacene films were performed using a Mac Science powder diffractometer (M18XHF-SRA) using Cu Kα radiation (λ = 1.54 Å). All devices fabrications and measurements were executed in air-ambient..

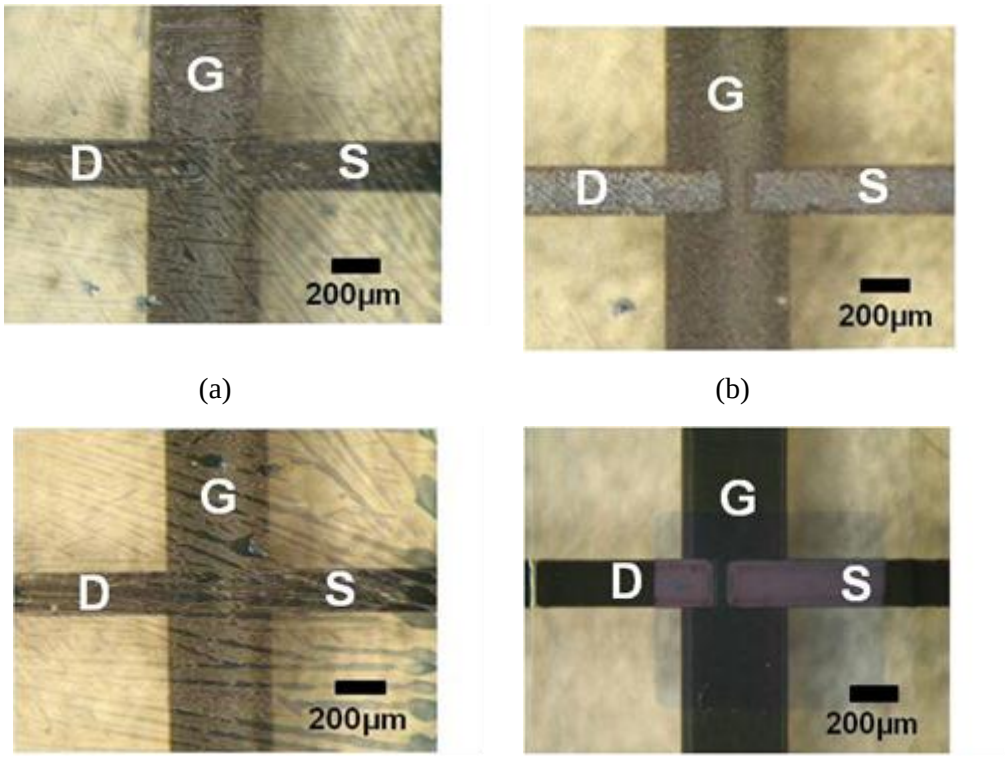
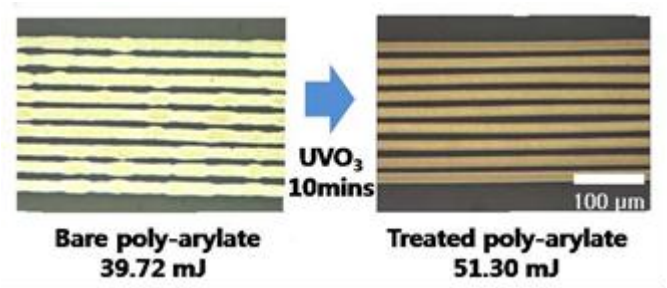


Figure 2.2 Optical microscope images for OTFTs with various TIPS-pentacene deposition methods including (a) inkjet-printing (b) spin-coating (c) drop-cast (d) reference evaporated pentacene on inkjet-printed TFT structure.

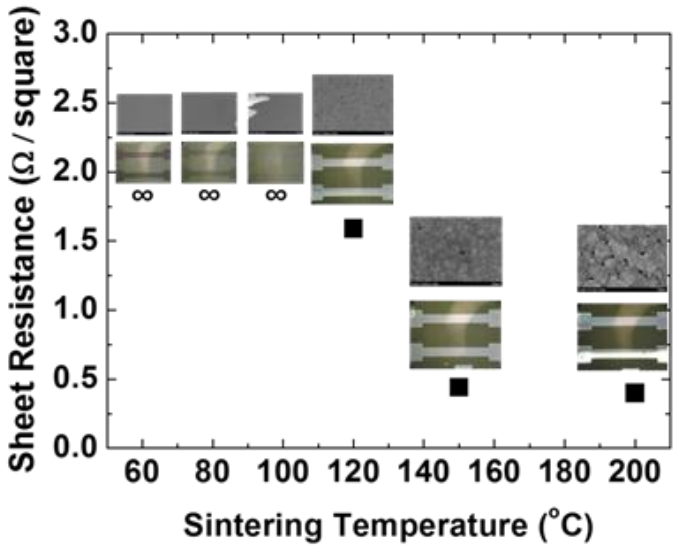
2.3 Inkjet-Printing Materials and Processes Optimization for OTFT Array Fabrication on Flexible Plastic Substrate

For inkjet-printed flexible OTFT array fabrication, we used ultraviolet (UV) ozone treated flexible poly-arylate substrates having 200 μm thickness. Poly-arylate substrate which has good flexibility is suitable for high temperature process because it has high glass transition temperature (Tg) of 330 ℃. In addition, it was reported that its surface energy is suitable to fabricate narrow conductive line using silver ink by preventing ink materials spread on substrate [11]. Although poly-arylate substrate has good thermal and mechanical properties for printed electronic applications, we used ultraviolet (UV) ozone treatment for poly-arylate substrate to obtain more clean-edged narrow line by increasing surface energy corresponding hydrophilic substrate. After UV ozone exposure treatment for 10 minutes, poly-arylate surface energy was increased from 39.72 mJ to 51.30 mJ, and we obtained clean-edge inkjet-printed silver lines without waviness comparing with those on untreated poly-arylate substrate (Fig. 2.3 (a)). For electrode deposition, piezoelectric (drop-on-demand) inkjet-printer (DMP-2831 from Dimatix corp.) and transparent metal-organic precursor type silver ink (INKTEC corp. (TEC-IJ-010) were also used. Although conductive polymers such as Poly(ethylenedioxythiophene)/ poly(styrene sulfonic acid) (PEDOT/PSS) and polyaniline (PANI) show good performances for

electrodes of TFTs [5], [17], [18], their resistivity are much higher than that of metal electrodes, and thus it is hard for polymers to be applied to display backplane or other integrated circuits due to very high RC-delay. Among metallic inkjet-printable inks, silver ink is the most widely used and commercialized, because gold is very expensive and copper is not suitable for TFT electrodes due to its high diffusion properties. Inkjet-printed narrow silver line can be affected by many inkjetting parameters and conditions such as voltage waveform, drop-speed, drop-spacing, nozzle size and nozzle temperature. First of all, in piezoelectric inkjet-printing system, voltage waveform should be optimized to make well-defined ink droplet because inkjetting and ink-drop-speed are controlled by supplied voltage waveform. Inkjet-printed silver ink droplet should be spherical and short ink-drop-tail is required to obtain uniform silver line. Drop-spacing and speed can also affect line uniformity, shape, thickness and width because these parameters determine amount of jetted silver ink. The gate electrodes were inkjet-printed on the 60 °C substrate with optimized inkjetting conditions considering ink characteristics including a drop velocity of about 6~7 m/s, drop frequency of 5 kHz, and a drop spacing of 25 μm which means distance of each ink-drop and determines silver ink drop quantity to obtain better surface properties, film uniformity and electrical conductivity, and then it was annealed at 150 °C for 20 minutes in convection oven under atmospheric



(a)

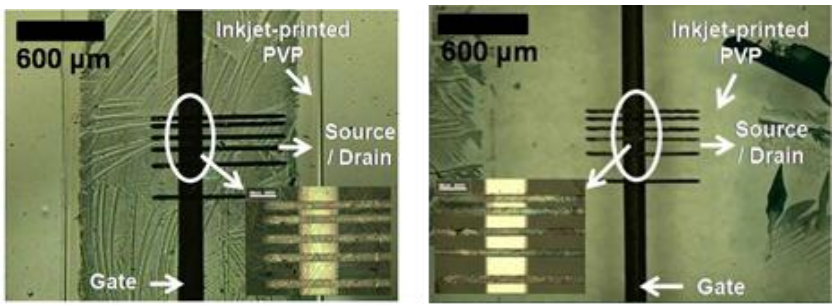


(b)

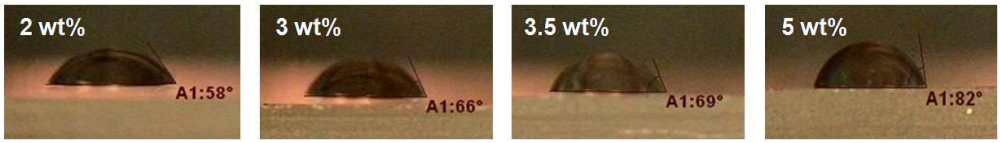
Figure 2.3 (a) Silver ink drop from 1pl cartridge with nozzle size of 9 μm and inkjet-printed silver droplet with 25 μm diameters on 60 ℃ substrate. (b) Optical and SEM images and electrical conductivity of inkjet-printed silver electrode depending on sintering temperature.

environment. Gate electrode showed high conductivity (0.5 Ω/□) (Fig. 2.3 (b)) which had a surface roughness of 2.37 nm in root-mean-square (RMS) value and 20.71 nm in peak-to-valley value throughout a scanning area of 10 ×10 μm^2. On inkjet-printed silver gate electrode, PVP solution was inkjet-printed as gate dielectric layer. Cross-linked PVP is one of the most widely used organic insulating materials due to its good insulating performance and low-temperature thermal curing condition. For PVP inkjetting process, temperature conditions should be optimized because PVP solvent can be dried easily resulting cartridge nozzle clogging, and substrate temperature also affects surface roughness of inkjet-printed PVP layer. The PVP solution was composed of 10 wt% of PVP and 2 wt% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) dissolved in propylene glycol methyl ether acetate (PGMEA) as a solvent from Sigma-Aldrich Corp. PVP and CLA concentration was critical factor to make a spherical shape of the ink droplet, since this factor determines the PVP solution viscosity. Especially, CLA concentration affects surface energy of PVP gate dielectric layer corresponding adhesion properties change with active layer. Figure 2.4 shows the relationship between CLA concentration in PVP solution and TIPS-pentacene dissolved in 1,2 dichlorobenzene adhesion properties. While TIPS-pentacene active layer was well-deposited on inkjet-printed PVP layer making good channel regions between source/drain electrodes when 2 wt% CLA was used (fig.2.4 (a)), TIPS-pentacene active layer did

not well-deposited on inkjet-printed PVP gate dielectric layer with 3.5 wt.% CLA. In magnified images figure 2.4 (b), there are no TIPS-pentacene active layer channels between source/drain electrodes on PVP layer, just only deposited on silver electrodes. In recently reported results, gate dielectric layer surface energy is very important factor for organic semiconducting layer deposition using solution process, therefore, many research groups have studied surface treatment or self-assembling monolayer (SAM) to control surface energy resulting in good adhesion properties of solution processed active layer [1], [19], [20]. To verify the relationship between CLA concentration and surface energy of inkjet-printed PVP layer, contact angle measurement was performed using deionized water. From figure 2.4 (c), contact angle was increased from 58° to 82° as increasing CLA concentration from 2 wt.% to 5 wt.% corresponding hydrophobic surface properties because poly(melamine-co-formaldehyde) CLA is terminated with methyl groups.[19] PVP layer with 2 wt.% CLA which had good adhesion properties with TIPS-pentacene showed similar contact angle with reported gate dielectric layer contact angle measurement results using deionized water for well-deposited TIPS-pentacene layer [1], [3], [19], [20]. Moreover, it is noted that hydrophilic dielectric surface property is more suitable for semiconductor film deposition using solution processing method [20]. From these experiments and results, we confirmed CLA concentration in PVP solution affects inkjetting condition for well-defined ink-droplet and surface energy which determine



(a) (b)

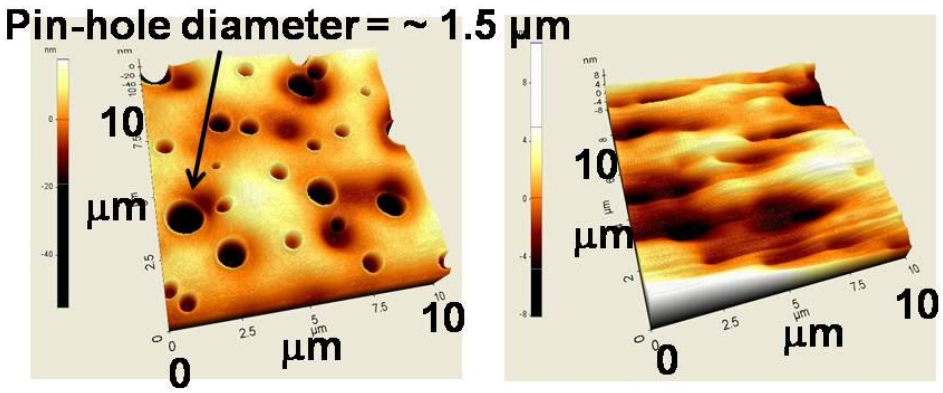


(c)

Figure 2.4 Optical images for TIPS-pentacene active layer deposition on inkjet-printed PVP gate dielectric layer with different PVP CLA concentration with (a) 2 wt.% (b) 3.5 wt.%. (c) Contact angle measurement results using deionized water on inkjet-printed PVP with different CLA concentration from 2 wt.% to 5 wt.%.

TIPS-pentacene adhesion properties, therefore, this parameter should be optimized for well-defined channel region corresponding high performance device. Optimized PVP solution was inkjet-printed on room-temperature substrate using drop spacing of 25 μm for uniform dielectric film. Thermally curing condition was also critical factor to obtain good surface properties. When inkjet-printed PVP layer was cured in flat curing condition, there are many pin-holes with diameter of 1.5 μm and depth of 60 nm because of rapid temperature increase (fig. 2.5). Pin-hole problem is reported as the reason for high gate leakage current and poor channel formation [6]. Because it determines the interface between active and gate dielectric layer where the charge carriers transport, the dielectric layer surface morphology should be improved. For elimination of pin-hole formation, we adopted ramping curing condition, and could reduce surface roughness effectively. Inkjet-printed PVP layer was thermally soft-cured on ramped hot-plate from 60 °C up to 100 °C for 30 mins and 100 °C hot-plate for 20 mins. Then, PVP solution was inkjet-printed again on previously printed PVP layer to reduce gate leakage current and obtain better surface roughness. Finally, 2-times-inkjet-printed PVP dielectric layer was cured in 4 °C/min ramped furnace from room-temperature up to 200 °C for 1 hour to obtain the cross-linked gate dielectric layer. By using this strategy, we could reduce surface roughness from near 11 nm to 3 nm in RMS value and obtain nearly 900 nm thickness. Our inkjet-printed PVP layer showed good insulation performance (3.8 nA/cm2 at 0.6 MV/cm) and it

showed lower gate leakage current comparing with reported inkjet-printed PVP layers insulation performance [6], [21].



(a) (b)

Figure 2.5 AFM images for inkjet-printed PVP gate dielectric layer surface using (a) flat curing condition, (b) ramping curing condition.

2.4 Experimental

2.4.1 All-Inkjet-Printed OTFT on Glass Substrate with Conventional Structure

Figure 2.6 shows the transfer characteristics of the fabricated OTFTs in (a) linear (V_{DS} = -5 V) and (b) saturation regimes (V_{DS} = -40 V). We obtained saturation mobility of 0.06, 0.03 and 0.09, and 0.04 $cm^2\ V^{-1}\ s^{-1}$, on/off ratio of 10^4, 3×10^3 and 10^4, and 10^4, threshold voltage of -1.4, -5.1 and -2.8, and 0.48 V for OTFTs with inkjet-printed, spin-coated and drop-cast TIPS-pentacene active semiconductor layers, and evaporated pentacene active semiconductor layer, respectively. It is also noted that, by using optimized inkjet-printing and annealing conditions, the electrical performances of the all-inkjet-printed OTFTs showed better performance than those of previously reported all-inkjet-printed OTFTs and are comparable to those of previously reported OTFTs with spin-coated PVP dielectric layer and/or thermally evaporated gold source/drain electrodes [22], [23]. This means that the inkjet-printed silver electrodes are suitable for the gate/source/drain and inkjet-printed PVP gate dielectric layer is well-matched with TIPS-pentacene active semiconductor layer.

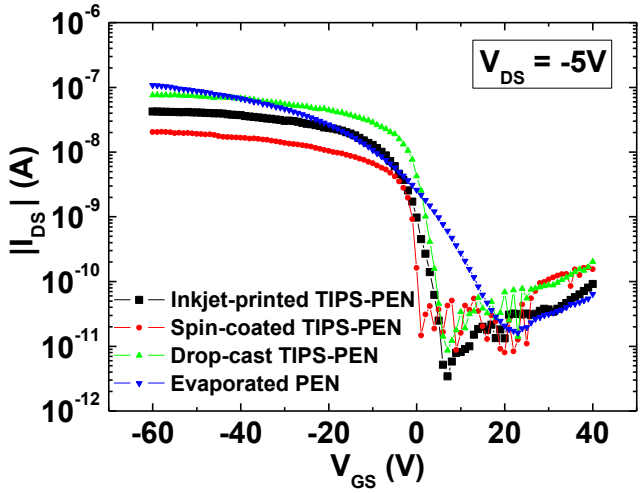
It is noted that drain current of all solution-processed TIPS-pentacene OTFTs becomes saturated as V_{GS} increases in negative direction while I_{DS}-V_{GS} characteristic

of the pentacene OTFT shows linear behavior as shown in Fig. 2.6 (b). This indicates that, for bottom-contact OTFTs with the inkjet-printed silver source/drain electrodes, TIPS-pentacene OTFTs show relatively poor contact resistance performance in comparison with the pentacene OTFT. Contact resistance can be analyzed by using a transmission line method (TLM) and we will report details of the contact resistance analysis of the solution-processed and evaporated OTFTs elsewhere.

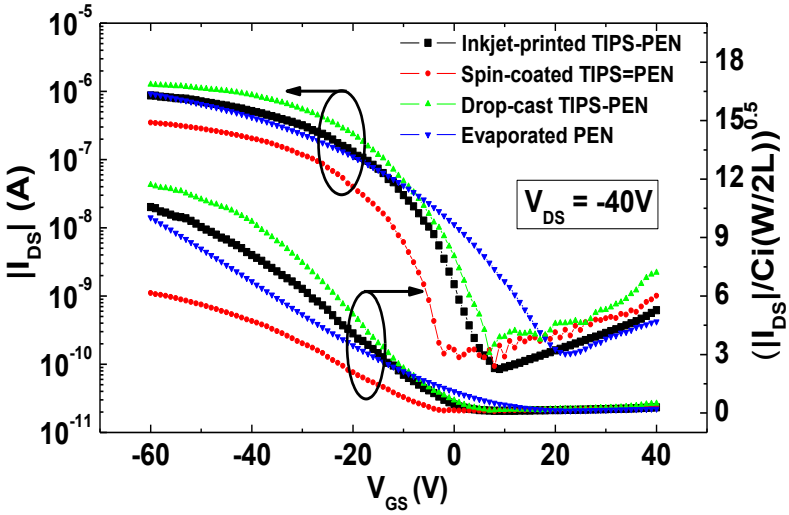
Figure 2.6 (a) shows that the TIPS-pentacene OTFTs have good switching performances with sub-threshold swing values of 3.17, 1.11, and 1.91 V/dec, for inkjet-printed, spin-coated, and drop-cast TIPS-pentacene OTFTs, respectively. These values are extracted between 10^{-11} and 10^{-9} drain current and are much smaller than that of the OTFT with the evaporated pentacene active layer (6.77 V/dec). As we mentioned, the surface energy of PVP dielectric layer is well-matched with that of TIPS-pentacene surface, making better interface properties than evaporated pentacene active semiconductor layer [14]. Using the defect density of insulator-semiconductor interface from amorphous silicon (a-Si) TFT model related to the sub-threshold as shown eq. (1) [24], we can extract $N_{SS}^{\max}$ values of 1.41×10^{12}, 4.75×10^{11} and 8.34×10^{11}, and 3.03×10^{12} cm^{-2} eV^{-1} for OTFTs with inkjet-printed, spin-coated and drop-cast TIPS-pentacene, and evaporated pentacene active semiconductor layers, respectively.

$$N_{SS}^{\max} = \left(\frac{SS \log(e)}{kT/q} - 1 \right) \frac{C_{ins}}{q^2} \quad (\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}), \qquad (1)$$

where *SS*, *k*, *T*, *q* and C_{ins} represent the sub-threshold swing value (V/dec), the Boltzmann constant ($\mathrm{eV\,K^{-1}}$), temperature (K), the absolute value of the electron charge (C) and the unit-area capacitance of the gate dielectric layer ($\mathrm{F/cm^2}$), respectively. From these results, it is confirmed that the inkjet-printed PVP and TIPS-pentacene active semiconductor layers show similar defect density to that of the spin-coated PVP or SiO_2 gate dielectric layer and TIPS-pentacene active semiconductor layer [14], [19].



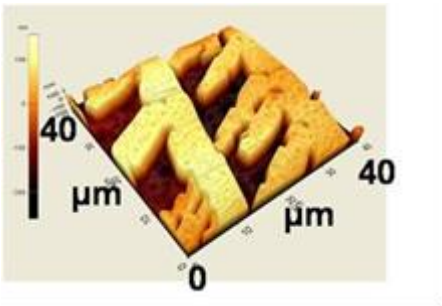
(a)



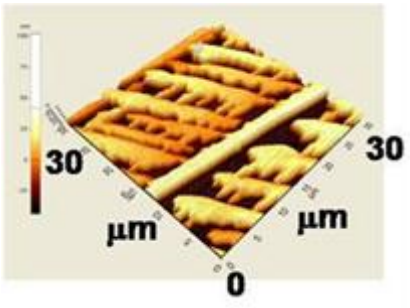
(b)

Figure 2.6 (a) OTFT transfer characteristic of (a) linear (V_{DS} = -5 V) and (b) saturation (V_{DS} = -40 V) regimes.

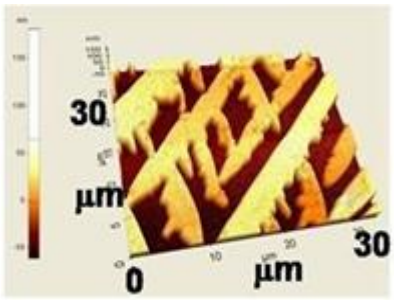
To further analyze crystalline structure affected by the active semiconductor layer deposition methods, we performed AFM and XRD measurements for all TIPS-pentacene and evaporated pentacene active semiconductor layers on the inkjet-printed PVP layer. The AFM images in Fig. 2.7 show that all the active semiconductor layers have crystalline structures even on the inkjet-printed PVP dielectric layer. TIPS-pentacene layers, unlike the pentacene layer, show longer c-axis structure although its size and shapes are different depending on the fabrication processes. Functional side groups of TIPS-pentacene attached to the central benzene ring of the pentacene molecule produce this orthorhombic crystal structure, and the molecular dimension along the side groups is larger than that along the pentacene molecule, resulting in a lower inter-planar spacing. It is known that this molecular structure renders TIPS-pentacene better stability for oxygen or water than the evaporated pentacene [25]. In addition, formation of the large crystalline structure for the inkjet-printed and drop-cast TIPS-pentacene layers is confirmed. Slow solvent evaporation at room temperature produces highly ordered molecular structure and thus better electrical performance in comparison with the OTFTs with spin-coated TIPS-pentacene layer because spin-coating process has different effect on the TIPS-pentacene solvent evaporation.



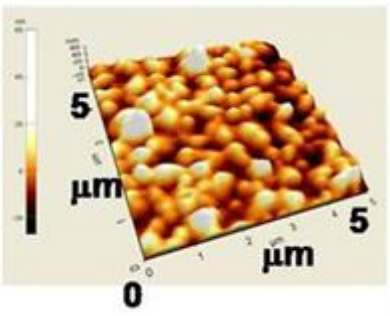
(a)



(b)



(c)



(d)

Figure 2.7 AFM images for active semiconductor layer on inkjet-printed PVP gate dielectric layer: (a) inkjet-printing, (b) spin-coating, (c) drop-cast, and (d) reference evaporated pentacene.

Crystallinity of the TIPS-pentacene layers was estimated from the XRD measurement. Figure 2.8 shows XRD results for TIPS-pentacene and evaporated pentacene films on the inkjet-printed PVP layer. The evaporated pentacene and TIPS-pentacene films show peaks at 5.2, 10.5, and 15.9, and 5.6, 11.3, and 17.1° in 2θ values for n = 1, 2, and 3, respectively. From Bragg's law as shown in eq. (2), the XRD result for the pentacene active layer shows the (00l) plane with an average interlayer spacing of 15.6 Å which is consistent with the previously reported results for pentacene films having orthorhombic structure [26]. For TIPS-pentacene active layers, there are same peaks at 2θ = 5.2° for the inkjet-printed, spin-coated and drop-cast films, which corresponds to an average layer separation of 16.8 Å. This value is also similar to that in a previous report and identical to that of the c-axis unit cell [3], [14], [15].

$$2d\sin\theta = n\lambda, \quad (2)$$

where d, θ, n and λ are the interplanar distance, the scattering angle, an integer determined by the order given and the wavelength (here, λ is 1.54 Å), respectively. Although XRD patterns of the inkjet-printed, spin-coated and drop-cast TIPS-pentacene layers show peaks at the same theta values, inkjet-printed and drop-cast TIPS-pentacene showed much higher intensity which means their films had better

and stronger molecular ordering than the spin-coated TIPS-pentacene film. It is closely related to the higher performance of OTFTs with the inkjet-printed and drop-cast films. In case of the spin-coated film, although active semiconductor layer film can be uniformly formed, solvent can be quickly evaporated in comparison with inkjet-printed or drop-cast films, leading to reduction in TIPS-pentacene crystallization time for the same high boiling point solvent used.

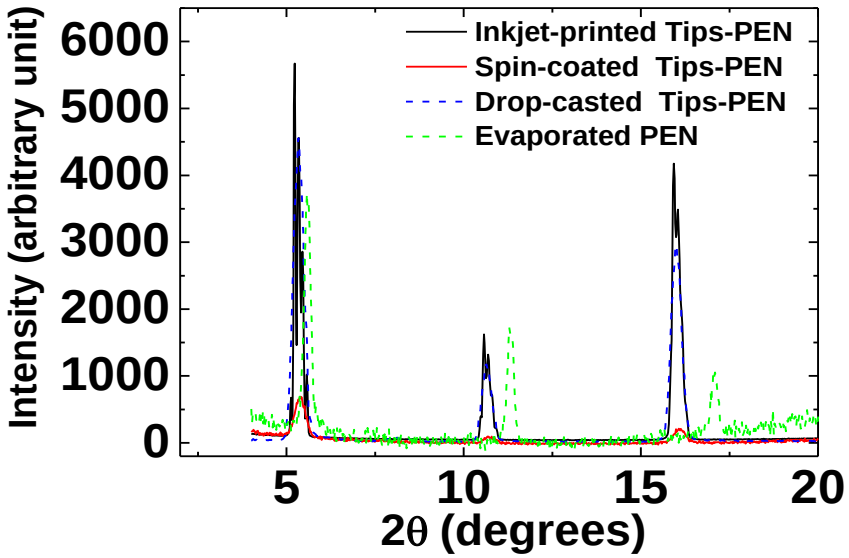


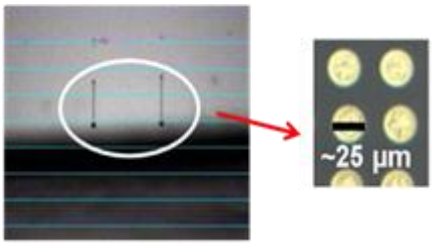
Figure 2.8 XRD spectra for inkjet-printed, spin-coated, drop-cast TIPS-pentacene and reference evaporated pentacene on inkjet-printed PVP dielectric layer.

2.4.2 All-Inkjet-Printed OTFT array on Flexible Plastic Substrate with Narrow S/D Electrodes

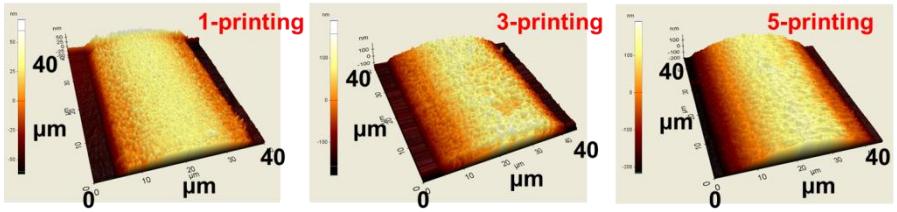
For narrow S/D electrode fabrication, nozzle size and amount of silver ink drop are critical factor. Although some research groups fabricated narrow silver line with 25 μm line width using 10 pl cartridge with nozzle diameters of 21 μm by increasing nozzle temperature up to 55 ℃ [27], high nozzle temperature can cause non-uniform narrow line because it reduces ink viscosity corresponding fast ink drop and long ink-drop-tail. Moreover, nozzle clogging problem shoud be solved in high temperature nozzle temperature. Therefore, we optimized inkjetting conditions from 1 pl cartridge with nozzle diameter of 9 μm by controlling voltage waveforms, drop speed of 10 ~ 12 m/sec, drop spacing of 25 μm and nozzle temperature of 32 ℃. From our optimized inkjetting conditions, one droplet of silver ink emitted from the cartridge with 9 μm diameters made a circle with about 25 μm diameters when it was dropped on the substrates (Fig. 2.9 (a)). For inkjet-printed S/D electrode application, demands for highly conductive narrow line fabrication with high-aspect ratio are also increased for high-power small scale and vertical structure devices. To increase narrow silver line thickness, there are two methods; reduction of drop spacing and multi-time-printing method. By reducing drop spacing, although large quantity ink was jetted on hydrophilic substrate, we could not obtain high-aspect ratio narrow silver lines because silver ink did not covered vertically, but spread

laterally (fig. 2.9 (b)). When the other method, multi-time-printing, was used, we could increase narrow silver line thickness up to 320 nm by 5-times-printing, because sequently jetted silver ink stacked vertically on soft annealed previously inkjet-printed silver line on 60 ℃ substrate (fig. 2.9 (c)). Moreover, electrical conductivity is also improved by increasing printing time due to fill up vacancy of silver line (fig. 2.9 (d)). When multi-time-printing method was performed, substrate temperature is critical factor to obtain narrow and well-defined silver line because it determines soft annealing of previously inkjet-printed silver line. To verify substrate temperature effect, we fabricated silver line on substrate with various temperatures using multi-time-printing method. From figure 2.9 (e), when silver lines were inkjet-printed using multi-time-printing method on room temperature substrate, line edge and surface were not clean corresponding large line width from 47 to 73 μm because sequently jetted silver ink was spread laterally. By increasing substrate temperature, we obtained clean line-edge and 5-time-printed line width of 38 μm on 60 ℃ substrate because high substrate temperature stimulates silver ink solvent evaporation and prevent to broad sequently jetted ink on previously printed narrow line. After narrow silver lines were inkjet-printed, finally, silver lines on poly-arylate substrate were sintered at 150°C for 20 minutes in oven under atmospheric environment. From optimization of inkjetting and annealing conditions, we fabricated high-aspect ratio narrow silver lines which had thickness from 70 nm to

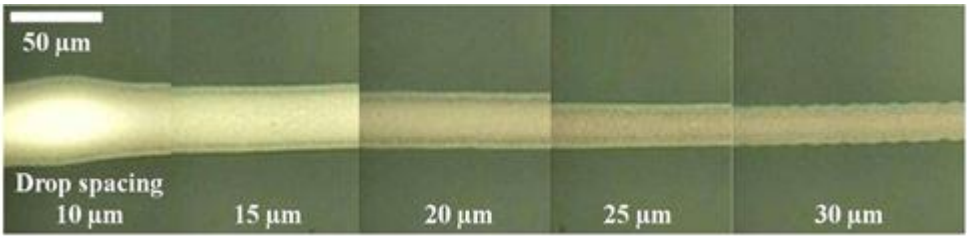
320 nm by increasing printing time and good uniformity without any coffee ring effect. Moreover, these results are better than recently published works from other groups because their width and height of 5-time-print narrow silver lines were 40 µm and 250 nm, respectively [7], [17], [28].


~25 μm

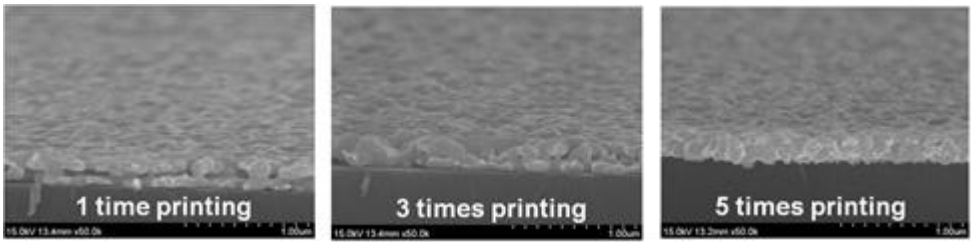
(a)


1-printing
3-printing
5-printing
40
μm
0
W : 26.8 μm T: 70 nm
W : 35.3 μm T: 190 nm
W : 37.6 μm T: 280 nm

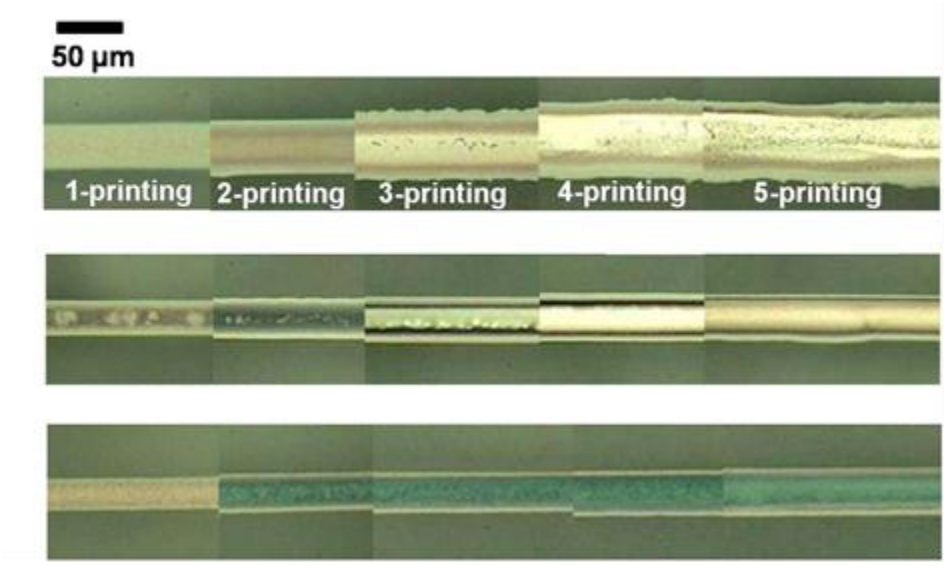
(b)


50 μm
Drop spacing
10 μm
15 μm
20 μm
25 μm
30 μm

(c)


1 time printing
3 times printing
5 times printing

(d)



(e)

Figure 2.9 (a) Silver ink drop from 1 pl cartridge with nozzle size of 9 μm and inkjet-printed silver droplet with 25 μm diameters on 60 ℃ substrate. (b) AFM images for inkjet-printed narrow silver lines with different printing time.

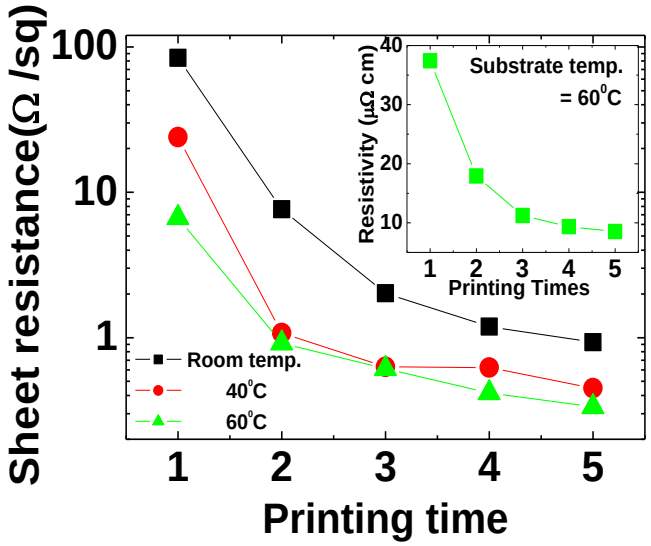
(c) SEM images for inkjet-printed narrow lines on silicon substrate with different printing time.

(d) Inkjet-printed silver lines with different drop-spacing and corresponding different line widths.

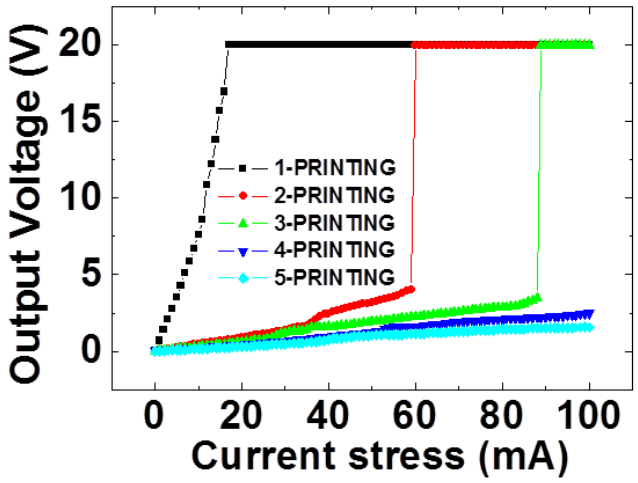
(e) Multi-time-printed silver lines on different substrate temperature: (up) room temperature, (middle) 40 ℃ (bottom) 60 ℃.

From measured line width, thickness and resistance, sheet resistance and corresponding specific resistivity of 5-time-print narrow silver lines were 0.33 Ω/□ and up to 8 μΩ·cm, respectively (fig. 2.10 (a)) From figure 2.10, electrical resistance can be reduced by increasing inkjet-printing time because of high uniformity and silver density. Especially, specific resistance of 5-times-printed narrow silver line shows 5-times electrical conductivity of bulk silver (1.6×10^{-6} Ω·cm) [29]. Moreover, in 5-times-printed narrow silver line, maximum current flow capacity up to 100 mA (8.22 mA/μm^2) was also suitable for electronic applications such as organic light-emitting diodes or OTFTs (fig. 2.10 (b)), and these electrical properties also have competition comparing with recently published works from other group [11].

Mechanical stability of conductive line on flexible electronics is also important to increase stability and reliability of inkjet-printed small scale devices. To verify this property of inkjet-printed narrow S/D electrodes, bending test was performed using bending test machine system. Because mechanical bending stress is determined by bending curvature and speed, we performed 1000 times bending test under bending curvature maximum 7 mm and speed from 20 mm/min to 80 mm/min (Figure. 2.10 (c)). As we expected, 1-time-printed silver line resistance is increased above 4-times than that of 5-times-printed silver line by increasing bending curvature and speed, because of its poor surface uniformity and low silver density comparing multi-time-printed silver line although silver has good ductility.


Sheet resistance(Ω /sq)
100
10
1
1
2
3
4
5
Printing time
Room temp.
40°C
60°C
Resistivity (μΩ cm)
40
30
20
10
1
2
3
4
5
Printing Times
Substrate temp.
= 60°C

(a)


Output Voltage (V)
20
15
10
5
0
0
20
40
60
80
100
Current stress (mA)
1-PRINTING
2-PRINTING
3-PRINTING
4-PRINTING
5-PRINTING

(b)

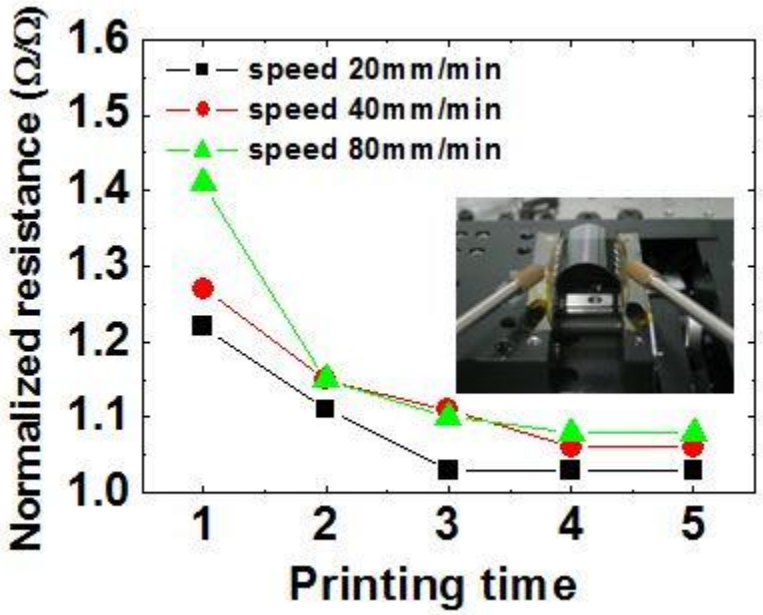
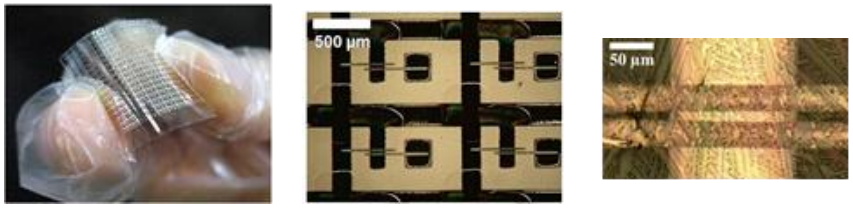
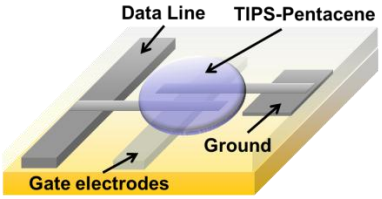


Figure 2.10 Electrical and mechanical properties of inkjet-printed narrow lines with different printing-time and substrate temperatures including (a) sheet resistance (Calculated specific resistance results is also included in inset) (b) current flow capacity, and (c) bending test results with bending curvatures of 7mm and speed from 20mm/min to 80mm/min.

By using these optimized narrow S/D electrodes, we fabricated all-inkjet-printed OTFTs array with 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene) active layer on flexible poly-arylate substrate, a 33 μm S/D electrodes line width corresponding short channel length, 11 μm in average value (fig. 2.11). As you can see from OTFT optical image and performance from figure 2.11, narrow silver line S/D electrodes were well-defined and mobility of 0.05 $cm^2/V \cdot S$, threshold voltage of 1.14 V and on/off ratio of 4×10^3 were obtained. These results show better electrical performance than previously published results with all-inkjet-printed OTFTs [9]-[10]. We expect the performance of OTFT with narrow silver S/D electrodes can be improved by using PVP surface treatment for more uniform and well-crystallized TIPS-pentacene.



(a) (b) (c)



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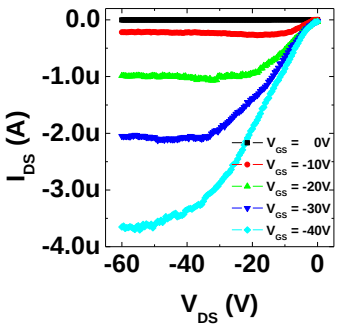

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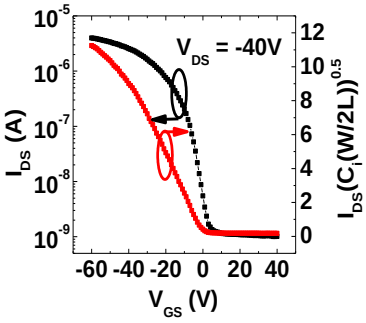

(f)

Figure 2.11 All-inkjet-printed OTFTs with narrow S/D electrodes (a) 12 × 18 OTFTs array on 20 mm × 20 mm poly-arylate substrate (b) optical microscope image of OTFTs array (c) optical microscope image of OTFT with TIPS-pentacene active layer (d) Schematic view of OTFT (e) output characteristics and (f) normalized transfer characteristic.

2.5 Conclusion

In this chapter, we report all-inkjet-printed OTFTs array with narrow S/D electrode on flexible substrate. By using carefully optimized inkjetting and sintering conditions including surface treatment, substrate temperature and printing parameters, highly conductive and uniform silver electrodes with clean-edge and high aspect-ratio were fabricated. In addition, the inkjet-printed TIPS-pentacene layer showed similar crystallinity properties to the drop-cast TIPS-pentacene layer resulting in better OTFT performance than OTFT with the spin-coated TIPS-pentacene layer. Especially, for high conductive narrow S/D electrodes with short channel length fabrication, multi-time-print method was adopted, and obtained well-defined narrow silver line with line width of 38 μm, thickness of 320 nm by 5-time-printing. From electrical properties measurement, high conductivity and electrical stability of multi-time-printed narrow silver lines were shown. For flexible electronics applications, mechanical stability test was also performed, and multi-time-printed narrow silver line shows much better stability. Finally, by using optimized narrow silver line in OTFTs application, we confirmed narrow silver line can be used at OTFTs array as S/D electrodes with short channel length. Therefore, multi-printing method and fabrication conditions optimization are necessary to obtain high resolution inkjet-printed electronic applications, for example, RFID tags or OTFTs.

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Chapter 3

All-Inkjet-Printed Inverter on Flexible Substrate

3.1 Introduction

Nowadays, solution-processed organic electronic devices have attracted much attention due to their low-cost, non-vacuum and environment-friendly processability [1], [2]. Among several solution process methods, inkjet-printing technology is one of the most promising candidates because tens micrometer feature patterns can be directly printed without using any photomasks [3], [4]. Moreover, inkjet-printing method enabled large area and low-temperature fabrication process on flexible substrates for various electronic applications such as active-matrix display, RFID, sensor and microelectronic circuits [5]–[7]. Therefore, many research groups have studied inkjet-printing systems, inkjet-printable materials for electrodes, insulators

and semiconductors, and optimization of patterning conditions for high quality inkjet-printed layers [8], [9]. Although high performance organic thin-film transistors (OTFTs) can be fabricated from solution-processable organic semiconducting materials, most of the reported devices were fabricated using a spin-coated polymer insulation layer on photolithography patterned gate or heavily doped silicon/silicon dioxide substrates [10]–[12]. Only recently, all-inkjet-printed OTFTs on flexible plastic substrate were reported but devices showed relatively low mobility and poor on/off ratio [13], [14]. In last years, although we also have already demonstrated the potential of all-inkjet-printed inverter consisting of OTFTs with a conventional gate and source/drain overlap structure having better electrical characteristics, TFT performance was marginal and supply voltage was as high as -40 V in order to obtain a gain of about -7.8 V/V [15]. In addition, even though fully self-aligned OTFTs were fabricated to minimize the overlap capacitance resulting in better electrical performance of printed organic inverter with low RC-delay, their OTFTs mobility and inverter switching performance were not comparable with those of conventional vacuum-processed OTFTs and inverter [16]. Therefore, surface treatment on gate dielectric layer or any other additive layer is required for high-performance circuit application. In this chapter, we report high-performance an all-inkjet-printed inverter using two p-type OTFTs on flexible substrate, and its electrical performance. Optimized inkjet-printed silver electrodes, poly-

4vinylphenol (PVP), and TIPS-pentacene were used as gate, source/drain (S/D), gate dielectric layer, and semiconductor layer, respectively. In order to obtain further improved electrical performance, interdigitated S/D structure was used in drive OTFT for a full up-down switching performance. Moreover, chemically coupled coil-like chlorosilane-terminated polystyrene (PS–Si(CH_3)$_2$Cl, PS-brush) layer in contrast to SAM which is highly sensitive to deposit conditions, such as temperature, humidity, and impurities, which affect the electrical performance and reproducibility was deposited between organic gate dielectric and semiconductor layers to remove the hydroxyl group at the gate dielectric/semiconductor interface resulting in excellent electrical performance under low operation voltage [17], [18].

3.2 Materials and Equipment for Inverter Fabrication

For all-inkjet-printed OTFT fabrication, we used poly-arylite substrates with 200 μm thickness from Ferrania Corp. because it was reported that surface energy of the poly-arylate substrate was suitable to fabricate high-quality inkjet-printed silver electrodes [8]. After substrate was cleaned with isopropylalchol and deionized water sequentially in an ultrasonic bath for 5 minutes respectively, its surface was exposed to ultraviolet (UV) ozone for 10 minutes to increase surface energy from 40 mJ to 50 mJ. After UV ozone treatment, silver ink spreads less laterally but stacks vertically, resulting in well-defined gate electrodes. A piezoelectric (drop-on-demand) inkjet printer (DMP-2831, Dimatix Corp.) was used for all-inkjet-printing processes. For electrodes, transparent metal-organic precursor type silver (Ag) ink from INKTEC corp. (TEC-IJ-010, 20 wt.% Ag content) was used. For gate electrode fabrication, inkjetting and sintering conditions were carefully optimized to obtain highly conductive layers (0.4 Ω/square) without edge waviness and coffee ring effects. The Ag ink was printed with a drop velocity of about 5 m/s, a drop frequency of 5 kHz and a drop spacing of 25 μm by maintaining the substrate temperature at 60 °C and then the printed Ag line was annealed at 150 °C for 20 mins in convection oven under atmospheric environment. For metal-organic type Ag inks, the printed electrodes started to appear shiny when annealed at temperatures over 120 °C and

large Ag grain packaging was observed when annealed in 150 °C convection oven, which directly related to high conductivity for the printed electrodes. On the gate electrode (500 μm width and 200 nm thickness), poly-4-vinylphenol (PVP) solution was inkjet-printed to form a gate dielectric layer. Cross-linked PVP is one of the most widely used organic insulating materials due to its good insulating performance and low cross-linking temperature [10], [19]. Considering surface energy and wetting properties, we optimized formulation of the PVP (M_w ~25,000): 10 wt.% of PVP and 2 wt.% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) in propylene glycol methyl ether acetate (PGMEA) solvent. All chemicals were purchased from Sigma-Aldrich Co. PVP and CLA concentration is critical in providing appropriate surface property for the following printed layer. In addition, thermal curing condition is also important to reduce number of pin-holes [20]. Therefore, we used a ramping curing condition (ramping at 4 °C/min and soaking at 200 °C for 20 minutes) and 2-times-printing of PVP, providing 900 nm thick PVP layer with good insulation performance (3.8 nA/cm^2 at 0.67 MV/cm). Its insulating performance shows more than 20 times better than recently reported inkjet-printed gate dielectric insulating layer which was formed from the organic-inorganic hybrid precursor solution (100 nA/cm^2 at 0.6 MV/cm) [14]. After PVP gate dielectric layer formation, silver source/drain electrodes were inkjet-printed using the same printing and sintering conditions as the gate electrode. For source/drain (S/D) electrodes

fabrication, interdigitated S/D electrodes were defined by inkjet-printing method using same Ag ink for gate electrode fabrication which had channel width / length of 250 μm / 90 μm and 14000 μm / 100 μm for load and drive OTFT, respectively. After S/D electrodes deposition, PS-brush surface treatment was performed on UV ozone treated PVP gate dielectric layer. Prepared 0.4 wt.% chlorosilane-terminated PS (M_w = 26.8 k) which was dissolved in toluene was drop-cast in channel area using micropipette, and then baked on 110 ℃ hot-plate for 1 hour. After it was rinsed in toluene, reducible solvent was evaporated in vacuum for 10 minutes. Finally, TIPS-pentacene dissolved in toluene was printed in channel area, and then dried in air ambient. The electrical characteristics of the transistors and the inverters were measured with a semiconductor parameter analyzer (Agilent 4145B). The inverter measurements were carried out with an oscilloscope (Tektronix 3032B) and a function generator (Tektronix AFG3021)). XPS analysis was performed using Axis-HSI (Kratos Inc) with Al in Mg/Al dual anode and power of 10 mA and 15 kV. Thicknesses and surface profiles of metal and organic layers were measured using both TENCOR Alpha-step 500 and atomic force microscopy (AFM) from Park System. Mechanical Bending stress test was performed by using a home-made automatic stretching equipment.

3.3 Surface Treatment for Electrical Characteristics Improvement

To achieve better OTFT electrical performance improvement, full integration of surface treatment process between gate dielectric layer and organic semiconductor layer which access to high-performance materials such as self-assembly monolayers (SAM) or ultra-thin-film like polystyrene (PS) to induce highly ordered π-conjugated organic semiconductor layer and interfacial properties having minimized charge traps due to surface polar groups, as well as optimization of the printing processes and device structure are necessary.[21]-[25] Although it is well-known that PS film provide sufficient hydrophobic and smooth surface which can passivize the hydroxyl groups and prevent water absorption on the gate dielectric layer, [26], [27] it is easily swelled and delaminated under exposure to the organic solvents that dissolve semiconductor materials, which indicates that PS film is not a suitable monolayer for solution-processible organic semiconductors. To overcome these problems, many research groups reported vertically phase-separated π-conjugated films obtained from semiconductor / dielectric polymer blend solutions or chemically coupled PS-film with gate dielectric layer. [28]-[30] Among these promising candidates, chemically coupled PS-film was adopted on all-inkjet-printed inverter fabrication because it can be fabricated using inkjet-printing method with simple process at low-temperature and is stable in thermal stress. Moreover, this

layer not only removes the hydroxyl groups at the gate dielectric/semiconductor interface, but provides sufficient surface energy corresponding good organic semiconductor ink wetting property. In addition it also decreased the number of interfacial charge traps from surface polar moieties on the PVP dielectric and minimizes the diffusion and absorption of moisture and oxygen into the semiconductor-dielectric interface caused electrical performance degradation resulting in highly improved OTFTs electrical performance.[30]

3.4 Experiments and Results

First, we fabricated an all-inkjet-printed inverter on flexible plastic substrates without interdigitated S/D structure and surface treatment as shown in Fig.3.1, which consists of one diode-connected load OTFT (W/L = 247/47 μm/μm) and one drive OTFT (W/L = 1650/52 μm/μm). For easy fabrication of multiple devices next to each other, PVP gate dielectric layers of each transistor for six inverters are printed together as indicated with red rectangulars in Fig. 3.1. For simulation, SMARTSPICE from Silvaco Corp. and embedded RPI amorphous silicon (a-Si) TFT models (level = 35) were used. Figure 3.2 shows measured transfer and output characteristics of the all-inkjet-printed OTFTs which were compared with the simulation results. Mobility of 0.02 $cm^2/V{\cdot}s$, on/off ratio of 10^4 and threshold voltage of -1.2 V were extracted from the measured transfer characteristics. Its electrical performances were comparable to those of previously reported OTFTs using spin-coated polymer gate dielectric layer and/or thermally evaporated gold source/drain electrodes [11] and much better than the recently reported all-inkjet-printed OTFTs [13], [14].

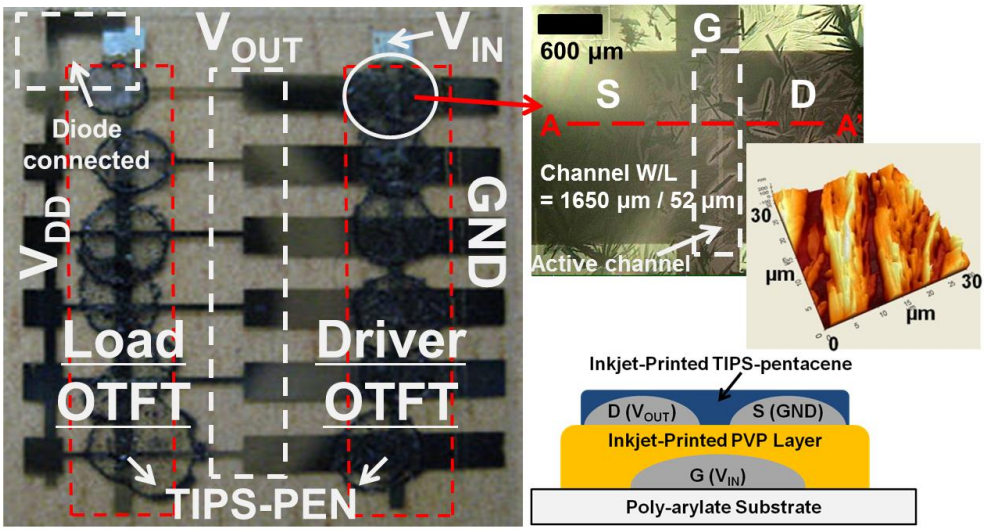
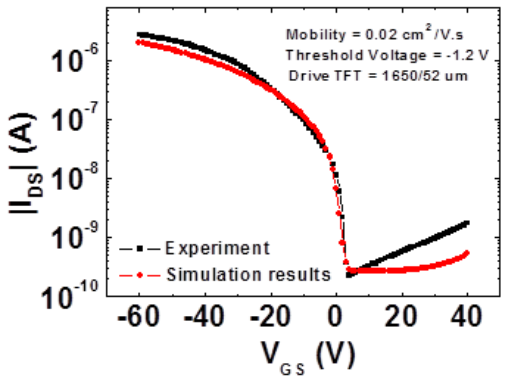
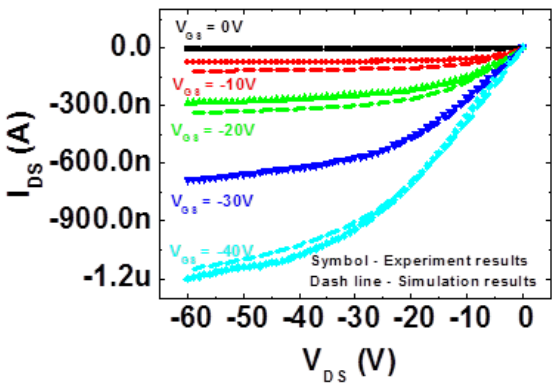


Figure 3.1 Optical images of six all-inkjet-printed inverters and magnified one of the drive OTFT using TIPS-pentacene active layer. (2-times-printed PVP layer is indicated by red rectangulars) AFM image of TIPS-pentacene active layer in channel area and cross-section view (A-A') of OTFT are also included.

From the AFM measurement, we also confirmed that a well-crystallized TIPS-pentacene active layer was formed, showing similar images as previously reported results [19]. We obtained the sub-threshold swing (SS) average value of 2.52 V/dec that was extracted between 10^{-10} and 10^{-8} drain current levels. It should be noted that considering bottom contact structure, inkjet-printed Ag S/D electrodes and avoidance of any additional surface treatment, device performances are good enough for all inkjet-printed OTFT circuit fabrication. Based on the measured results, we fit parameters of RPI a-Si TFT model and corresponding simulation results were used to design inverters with two p-type OTFTs. Figure 3.3 shows measured inverter operation for input voltage from -50 V to 20 V in both negative (denoted as 1) and positive (denoted as 2) sweep direction. Although switching properties show hysteresis phenomenon, clear inverter operation and high voltage gain with maximum value of 7.8 were obtained as shown in inset of Fig.3.3. This hysteresis behavior was observed with little changes for repeated input voltage sweeps in both directions. Since it may come from defect states such as charge traps at interface between PVP and TIPS-pentacene layers or structural defects in TIPS-pentacene semiconductor layer film [31], it is expected that this hysteresis can be further reduced if we optimize PVP/TIPS-pentacene interface with additional surface treatment and/or cure TIPS-pentacene in solvent-rich environment for further reduction in defect state formation.



(a)



(b)

Figure 3.2 (a) Transfer and (b) output characteristics of all-inkjet-printed OTFT in saturation regime (V_{DS} = -40 V) compared with simulation results using RPI amorphous silicon TFT model, SMARTSPICE.

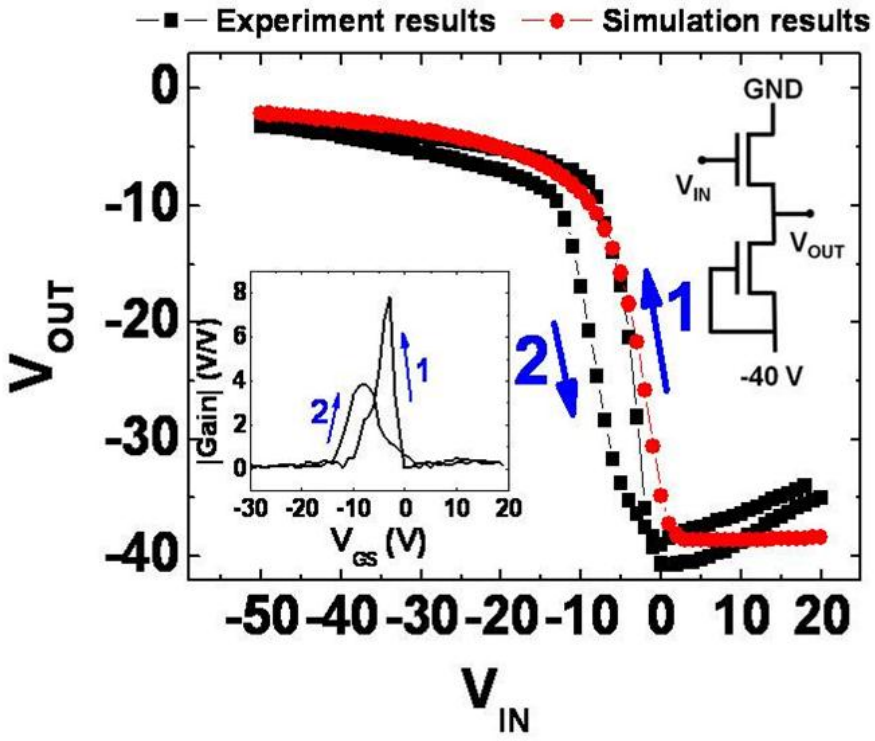


Figure 3.3 All-inkjet-printed enhanced mode inverter consisted with two p-type OTFTs switching performance compared with simulation results using amorphous silicon TFT model (Inverter voltage gain and circuit schematic are included in inset)

In addition, it is noted that the operation voltage of the fabricated inverter in high as in most OTFT-base inverters [10], [11], we believe that relatively high operation voltage of the fabricated inverter can be further reduced by introducing inkjet-printable high-k dielectric, high performance organic semiconductor materials, and short channel formation [32]. To verify all-inkjet-printed inverter operation, switching performance was also compared with simulation results. The results were well-matched showing similar switching behavior and voltage gain. The reason for output voltage change in the positive input voltage region is gate leakage current increment of the drive OTFT at high positive gate bias regime.

For better electrical characteristics, we also fabricated an all-inkjet-printed inverter which consists of one diode-connected load OTFT (W/L = 250/70 μm/μm) and one drive OTFT (W/L = 14000/100 μm/μm) with interdigitated S/D structure and surface treatment on PVP gate dielectric layer on flexible Arylite substrate as shown in Fig.3.4. For full swing V_{OUT} transition, interdigitated S/D structure was used in the drive OTFT for large W/L ratio. AFM image shows well-crystallized TIPS-pentacene structure at channel region on PS-brush treated PVP gate dielectric layer. For surface treatment on PVP layer, PS-brush was dissolved in toluene with 0.4 wt.% and stirred at room temperature with 300 rpm for 1 hour. Because the PS-brush is chemically coupled with the hydroxyl groups [30], the PVP layer was treated by UV ozone with 28 mW/cm^2 for 10 minutes to increase the hydroxyl

groups. After prepared PS-brush solution was inkjet-printed onto UV ozone treated PVP layer, baked on 110 ℃ hot-plate for 1 hour in air for chemical coupling reaction. Finally, it was rinsed in toluene to remove the reducible PS-brush material on PVP layer. The chemically coupled PS-brush layer provide sufficient surface energy corresponding good organic semiconductor ink wetting property, decreased the number of interfacial charge traps from surface polar moieties on the PVP dielectric and minimizes the diffusion and absorption of moisture and oxygen into the semiconductor-dielectric interface caused electrical performance degradation resulting in highly improved OTFTs electrical performance[30].

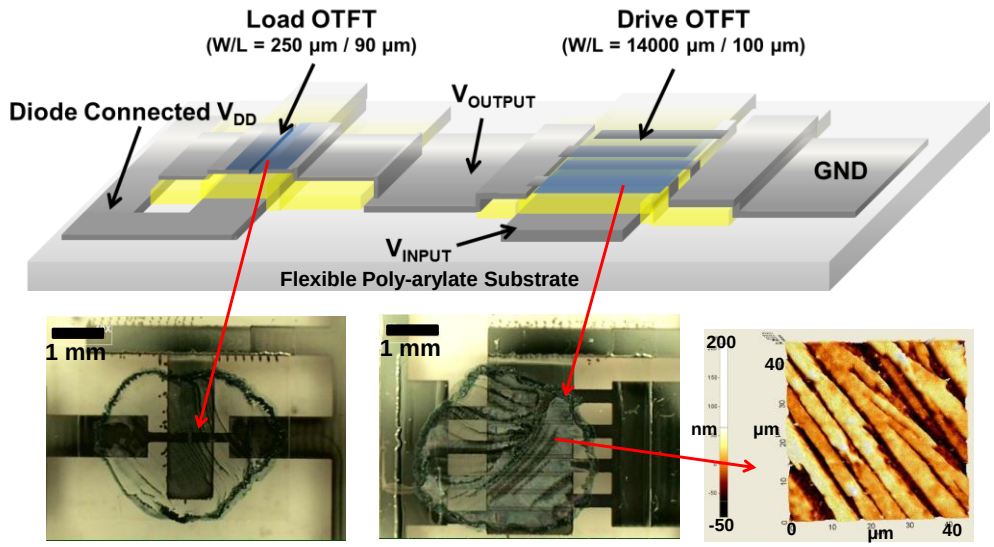
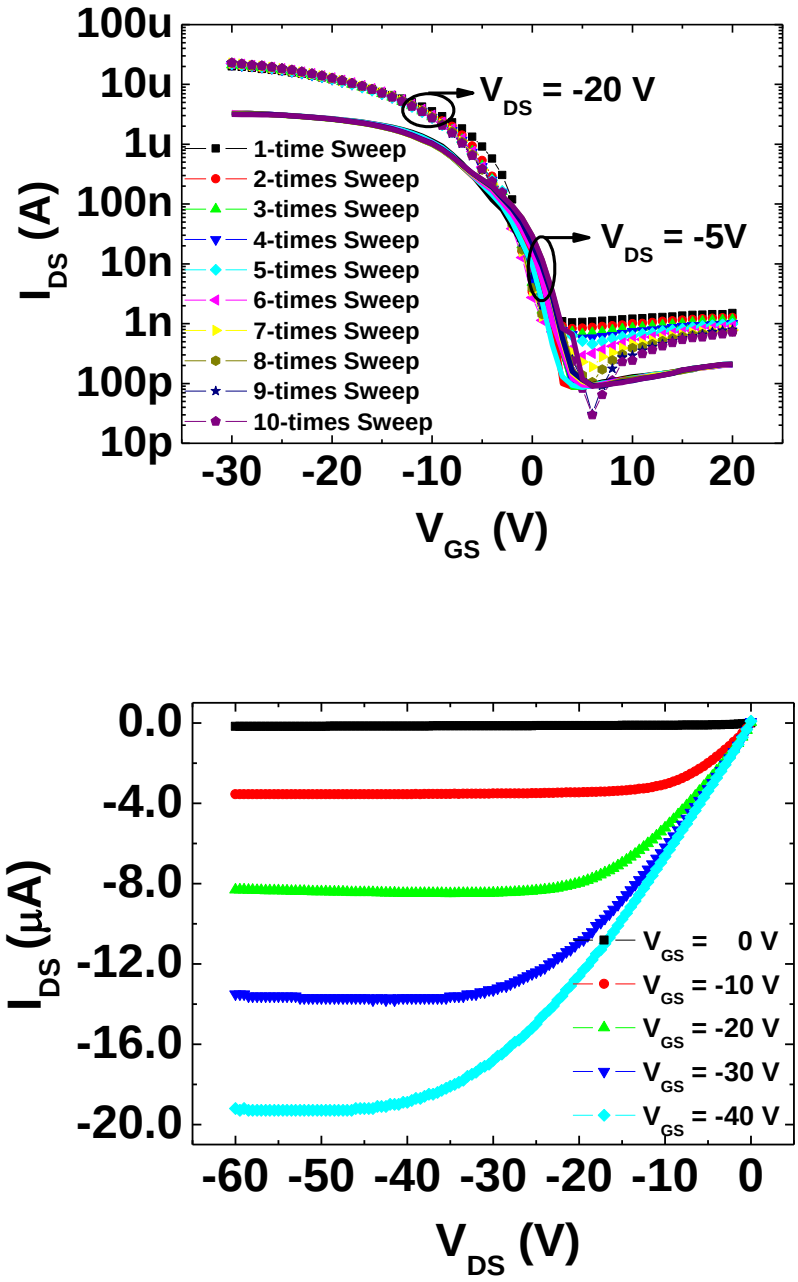
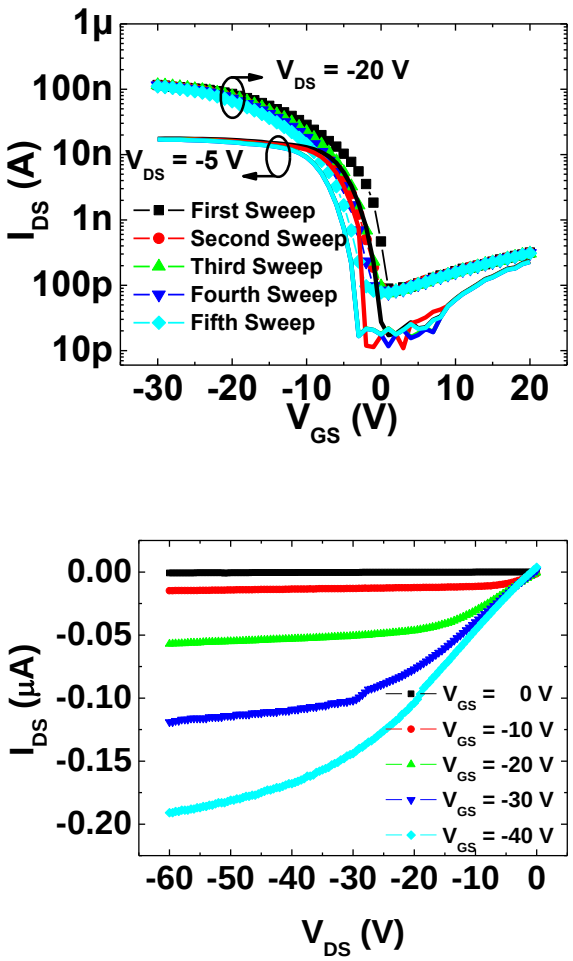


Figure 3.4 Schematic, optical, and AFM images of all-inkjet-printed inverter using two p-type OTFTs. AFM image shows well-crystallized TIPS-pentacene structure at channel region on PS-brush treated PVP gate dielectric layer.

Figure 3.5 shows transfer and output characteristics of all-inkjet-printed drive OTFT (a) with and (b) without PS-brush surface treated, respectively. When PS-brush surface treatment was performed on PVP gate dielectric layer, there were no threshold voltage change nor any electrical performance degradation at 10-time V_{GS} sweep, showing high mobility of 0.15 cm^2/V.s, on/off ratio of 2 x 10^5, threshold voltage of -1.98 V, and sub-threshold swing value of 2.27 V/decade at V_{DD} of -20 V. Moreover, good contact properties between inkjet-printed S/D electrode and TIPS-pentacene active layer was showed in low V_{DS} regime even though PS-brush treatment was also performed on S/D electrodes. Its electrical performance was much better than previously reported results of all-inkjet-printed OTFT from other and our group under low-operation voltage.[14]-[16] These better performance came from efficient surface treatment removing the hydroxyl group at the gate dielectric/semiconductor interface. On the other hand, OTFTs without PS-brush surface treatment showed poor electrical performance including mobility of 0.01 cm^2/V.s, on/off ratio of 10^4, threshold voltage of 0.53 V. In addition, turn-on voltages were also shifted to negative direction due to interfacial trap between PVP gate dielectric layer and TIPS-pentacene active layer under several gate-source voltage sweeps. To verify the chemical coupling with the PVP gate dielectric layer surfaces and PS-brush, X-ray photoelectron spectroscopy (XPS) was further performed as shown in figure 3.6. The XPS profiles of the PS-brush treated PVP layer contained


100u
10u
1u
100n
10n
1n
100p
10p
I_DS (A)
-30
-20
-10
0
10
20
V_GS (V)
V_DS = -20 V
V_DS = -5V
1-time Sweep
2-times Sweep
3-times Sweep
4-times Sweep
5-times Sweep
6-times Sweep
7-times Sweep
8-times Sweep
9-times Sweep
10-times Sweep
0.0
-4.0
-8.0
-12.0
-16.0
-20.0
I_DS (μA)
-60
-50
-40
-30
-20
-10
0
V_DS (V)
V_GS = 0 V
V_GS = -10 V
V_GS = -20 V
V_GS = -30 V
V_GS = -40 V

(a)



(b)

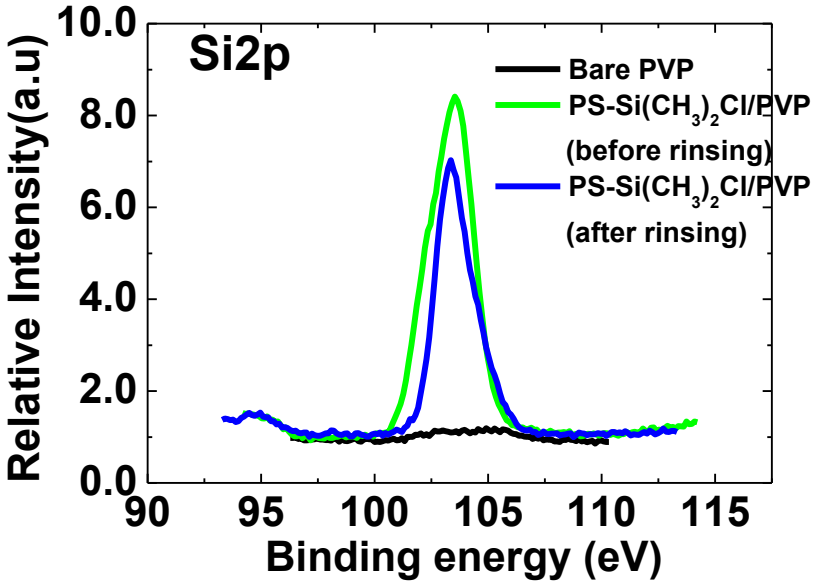
Figure 3.5 All-inkjet-printed p-type OTFT (a) transfer characteristics for V_{DS} of -5 V (line) and -20 V (symbol) during 10-time V_{GS} sweep from 20 V to -30 V, and output characteristics with PS-brush treatment, and (b) transfer characteristics for V_{DS} of -5 V (line) and -20 V (symbol) during 5-time V_{GS} sweep from 20 V to -30 V, and output characteristics without PS-brush treatment.

an strong Si2p intense peak near binding energy of 103 eV due to the Si2p orbitals of silicon moieties in the PS backbone, whereas the peaks were detect hardly on PVP layer and PVP layer with UV ozone treatment. After rinsing the PS-brush treated PVP layer using toluene, although the Si2p profile showed a slight intensity drop, there was also strong Si2p peak relatively. On the other hands, N1s intense peak near binding energy of 397 eV which is strongly shown on PVP layer was barely detected on PS-brush treated PVP layer because chemically coupled PS-brush monolayer was covered on PVP gate dielectric layer as shown in Fig.3.6 (b). Moreover, figure 3.6 (c) showed that same Ag3d intense peaks were detected on PS-brush treated and untreated Ag S/D electrode which indicate this surface treatment do not affect on Ag S/D conductivity and other properties. The above analyses for the PS–Si$(CH_3)_2$Cl treated PVP gate dielectric layer indicate that, after thermal annealing and rinsing, PS–Si$(CH_3)_2$Cl chains near the UV ozone treated PVP surface are chemically coupled with polar moieties to form a monolayer-thick PS brush without any damages on Ag S/D electrodes.

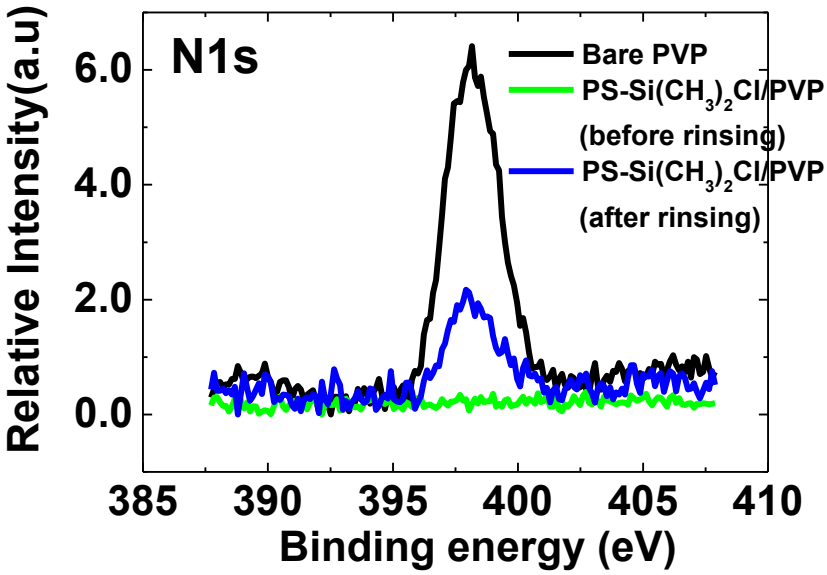
Figure 3.7 shows electrical characteristics of all-inkjet-printed inverter on flexible substrate with and without PS-brush treatment. By adopting surface treatment and interdigitated S/D structure, sharp transition property was obtained with high voltage gain values up to 19.8 V/V for supply voltage, V_{DD} from -5 V to -40 V. However, smooth transition with poor voltage gain values and $V_{transition}$ shift were shown when

untreated PVP gate dielectric layer was adopted due to interfacial traps and polar moieties under several gate voltage sweep although interdigitated S/D structure was adopted. In negative V_{INPUT} regime, PS-brush treated inverter showed very low V_{OUTPUT} under 0.1 V which is indicated that resistance ratio between on-state of load OTFT and on-state of drive OTFT was very large due to large W/L ratio difference. These results were also different with those of inverter with untreated PVP layer showing poor V_{OUTPUT} characteristics in negative V_{INPUT} regime due to low $I_{ON\_drive\ OTFT}$. Moreover, full-swing transition was obtained in positive V_{INPUT} regime showing large V_{OUPUT} similar with V_{DD} which means $I_{ON\_load\ OTFT}$ is much larger than $I_{OFF\_drive\ OTFT}$. All-inkjet-printed inverter with PS-brush treatment also showed a stable operation under 10-time V_{INPUT} sweep showing similar voltage gain value without $V_{transition}$ shift as shown in Fig. 3.7(c). For further mechanical flexibility investigation, bending stress test was performed, and stable electrical properties were obtained after 1000-time bending stress test with speed of 10 mm/sec and bending radius of 5 mm with perpendicular direction with channel as shown in Fig. 3.7 (d). Although the obtained gain value have been slightly reduced from -8 to -5.5 V/V for V_{DD}=-20 V after the bending stress test, it also showed sharp transition property without $V_{transition}$ shift during 1000-times bending test. The fabricated inverter also showed excellent frequency response characteristics at 1 kHz resulting in a propagation delay of only 0.36 ms from 1.4 V to 8.2 V due to its high carrier mobility, good

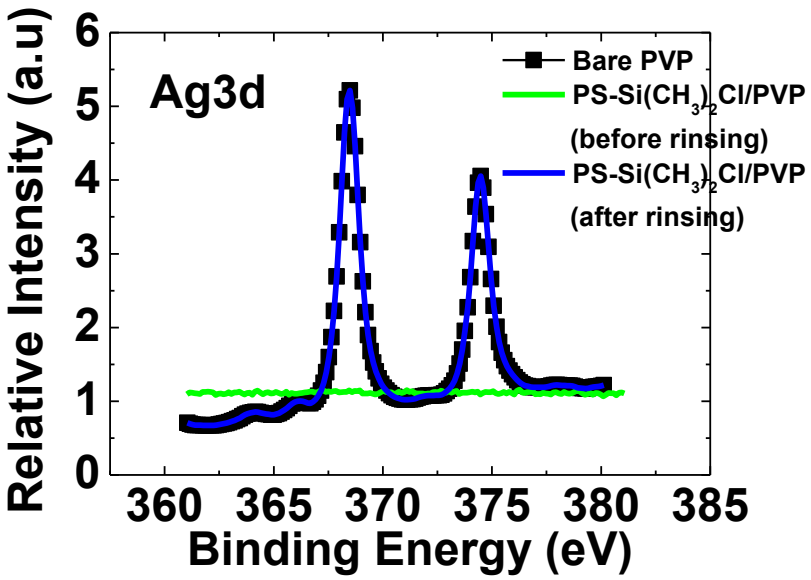
switching performance and electrically stable operation, and its marginal frequency response was up to 50 kHz pulse as shown in fig. 3.8.


Si2p
Bare PVP
PS-Si(CH3)2Cl/PVP
(before rinsing)
PS-Si(CH3)2Cl/PVP
(after rinsing)
Relative Intensity(a.u)
Binding energy (eV)
10.0
8.0
6.0
4.0
2.0
0.0
90
95
100
105
110
115

(a)

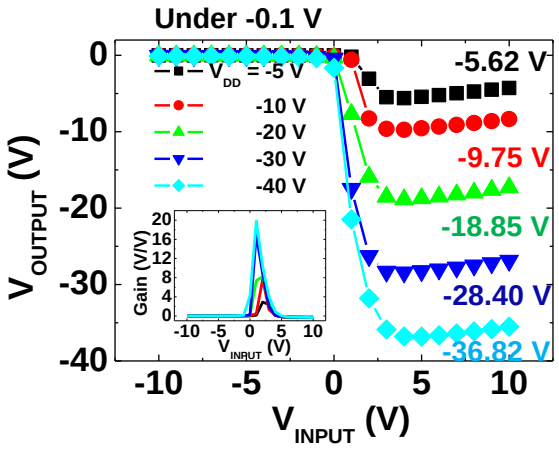

N1s
Bare PVP
PS-Si(CH3)2Cl/PVP
(before rinsing)
PS-Si(CH3)2Cl/PVP
(after rinsing)
Relative Intensity(a.u)
6.0
4.0
2.0
0.0
385
390
395
400
405
410
Binding energy (eV)

(b)

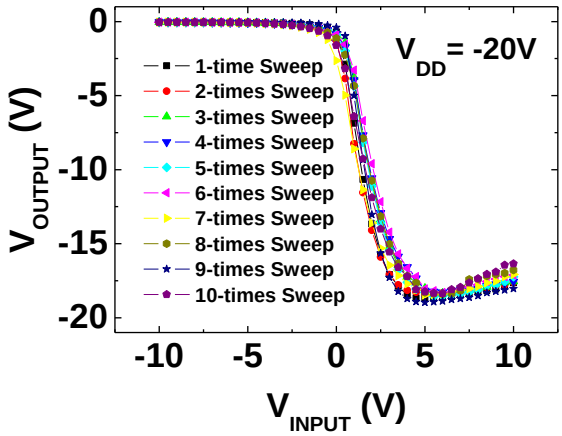


(c)

Figure 3.6 XPS profiles for PS-brush treated PVP gate dielectric layer ((a) Si2p and (b) N1s) and (c) Ag S/D electrodes

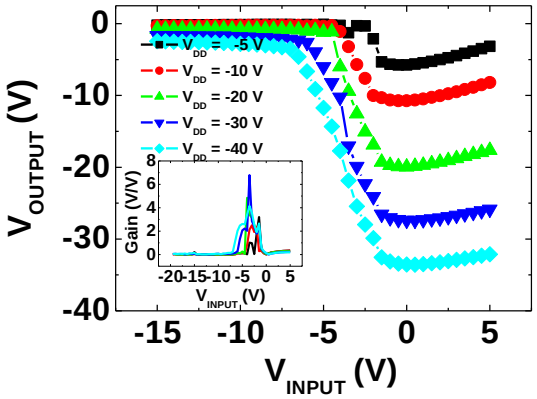


(a)

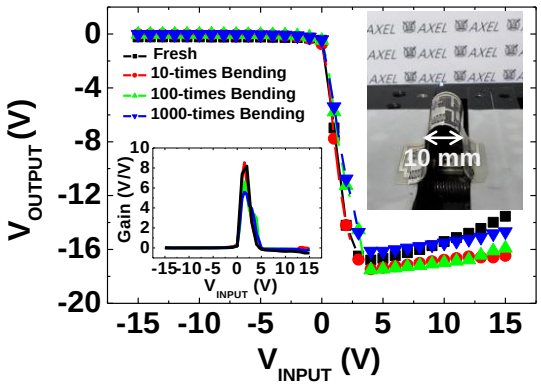


(b)

Figure 3.7 All-inkjet-printed inverter with PS-brush treatment (a) switching performance depending on V_{DD} from -5 V to -40 V and (b) switching performance on V_{DD} of 20 V during 10-times sweep, and without PS-brush treatment

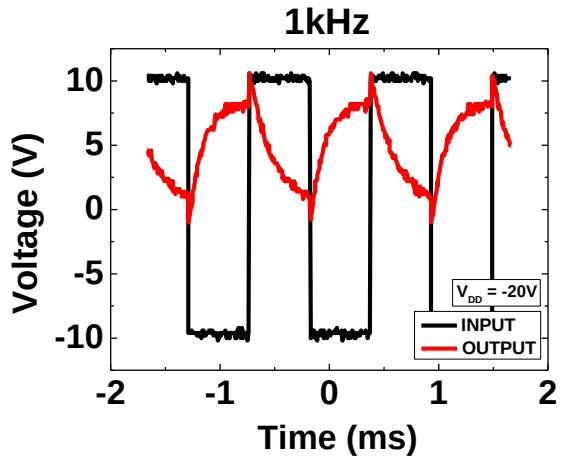


(a)

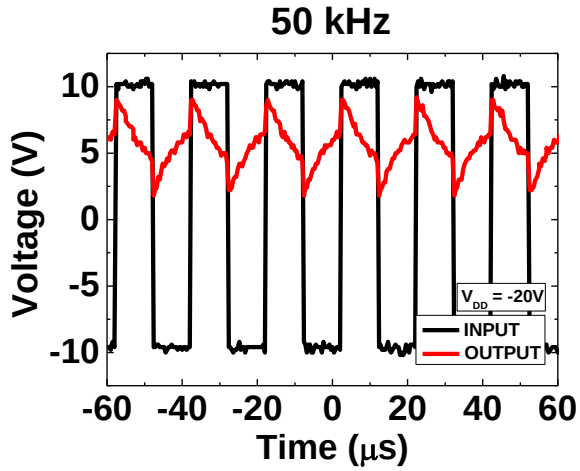


(b)

Figure 3.8 All-inkjet-printed inverter with PS-brush treatment (a) switching performance depending on V_{DD} from -5 V to -40 V. (b) All-inkjet-printed inverter switching performance on V_{DD} of -20 V under mechanical bending stress. (Voltage gain depending on V_{DD} is also included in inset.)



(a)



(b)

Figure 3.9 All-inkjet-printed inverter frequency responses after 1000-times bending stress at (a) 1 kHz resulting propagation delay of only 0.36 ms from 1.4 V to 8.2 V, and (b) marginal frequency of 50 kHz

3.5 Conclusion

In summary, high-performance all-inkjet-printed p-type organic inverter was fabricated on flexible substrate. Inkjet printing process such as inkjetting, sintering/curing conditions were carefully optimized, and especially, chemically coupled chlorosilane-terminated PS-brush layer on PVP gate dielectric layer dramatically improved OTFTs electrical performance and stability including mobility, on/off ratio, operation voltage and stable threshold voltage under several gate voltage sweeps. The PS-brush layer on PVP dielectric layer surface was verified using XPS analysis. From these optimized OTFTs performance, the fabricated inverter with two p-type OTFTs showed full-swing switching performance with high voltage gain value during 10-time V_{INPUT} sweep, and its characteristic also kept under 1000-times mechanical bending stress with speed of 10 mm/sec and bending radius of 5 mm. Moreover, good frequency response was observed showing marginal frequency of 50 kHz. From these optimized process and excellent performance, we believe that inkjet-printed electronics have great potential to substitute conventional photolithography patterning process in low-cost and environment friendly.

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Chapter 4

Contact Resistance Analysis of Inkjet-Printed Bottom-Contact OTFT

4.1 Introduction

Recently, organic thin-film transistor (OTFT) has attracted much attention due to its low-temperature, non-vacuum device fabrication procedure, which can be applied to low-cost, flexible and large-area electronics applications [1-5]. For OTFT fabrication, solution process, especially, inkjet-printing method is considered as one of the most promising candidates due to its ultra-cost-effective, maskless, low-temperature, non-vacuum and time-saving process compared with conventional vacuum deposition or spin-coating fabrication methods. Moreover, inkjet-printing process is a non-contact printing process without any contact damages or contamination issues. Therefore, inkjet-printing technique including equipment

development, optimization of the printing process conditions and ink materials, has been widely studied for high performance inkjet-printed device implementation [6]-[8].

For inkjet-printed OTFT fabrication, bottom-contact TFT structure is typically used because relatively high temperature sintering process is required for the printed source/drain (S/D) electrodes and ink solvent can damage bottom layer, especially semiconductor layer, when S/D electrodes are printed at the end of the OTFT fabrication process. Therefore, their electrical contact performance is generally poor in comparison with top-contact OTFTs that are typically fabricated by conventional vacuum process, due to high parasitic resistance [9]. Most of all, in bottom-contact OTFTs, interface properties between organic semiconductor layer and S/D electrodes mainly determine the carrier injection and movement because S/D electrodes, dielectric and semiconductor layer are adjacent [10]. For better performance, therefore, many research groups have studied the surface treatment on gate dielectric layer and S/D electrodes for good adhesion and contact characteristics [11-13]. In addition, as device dimension and required power consumption are decreased, contact resistance dominantly affects device performance. Therefore, investigation of parasitic resistance, especially series contact resistance between organic semiconductor layer and inkjet-printed S/D electrodes is important for high speed, low-power consumption and reliable printed device/circuit performance at

low voltage operation [14].

In this chapter, we report contact resistance analysis between inkjet-printed silver S/D electrodes and organic semiconductor layers in bottom-contact OTFTs using transmission line method (TLM). Inkjet-printed silver electrodes, spin-coated poly (4-vinylphenol) (PVP) and thermally evaporated pentacene were used as gate and S/D electrodes, gate dielectric layer and semiconductor layers, respectively. For TLM analysis, S/D electrodes with various channel length from 15 to 111 μm were printed using nozzle of 1 picoliter ink-drop volume. OTFTs with evaporated top- and bottom-contact silver and top- and bottom-contact gold electrodes were also fabricated for reference. To obtain well-defined each layers, ink-jetting conditions including ink drop size, drop speed and frequency, nozzle temperature and curing conditions were carefully optimized [15].

4.2 OTFTs Fabrication for Contact Resistance Extraction

Figure 4.1 shows OTFTs fabrication procedure for contact resistance extraction between inkjet-printed silver electrodes and thermally evaporated pentacene semiconductor layer. Corning Eagle2000^{TM} bare glass substrate was used after cleaning in ultrasonic baths of acetone and isoprophyl alcohol for 20 and 10 minutes, respectively, and rinsed by deionized water. After the glass substrate was dried at 200 ℃ in oven, silver gate electrodes were inkjet-printed on the substrate whose temperature was maintained at 60 ℃. Inkjet-printed silver electrodes which have shiny appearance, clean-edge and better surface properties were obtained after the substrate was annealed at 150 ℃ for 30 minutes in a convection oven under atmospheric environment. Width and thickness of the inkjet-printed gate electrode were about 510 μm and 200 nm, respectively. We used silver metal-organic precursor type silver ink from INKTEC corp. (TEC-IJ-010) which has silver contents of 20 wt.% and a drop-on-demand inkjet printer from DIMATIX corp. (DMP-2800 series). The droplets having 10 picoliter volume were emitted from several nozzles with a diameter of about 21 μm, resulting in a circle having diameter of 50 μm on the cleaned glass substrate. The silver ink was printed with a drop velocity of about 5~6 m/s, optimized waveform for well-defined spherical ink droplet shape, and a drop spacing of 25 μm which means distance between each ink

drops. From these optimized conditions, clean-edge and high-conductive silver electrodes (0.4 ~ 0.6 Ω/□) were fabricated. It is noted that the metal-organic Ag ink produce good surface roughness (~ 2~3 nm in RMS value) of the printed electrodes, which is similar to that of the evaporated silver electrodes. Furthermore, silver ink is widely commercially available at much lower price in comparison with gold ink. On the printed silver gate electrodes, PVP was spin-coated for gate dielectric layer

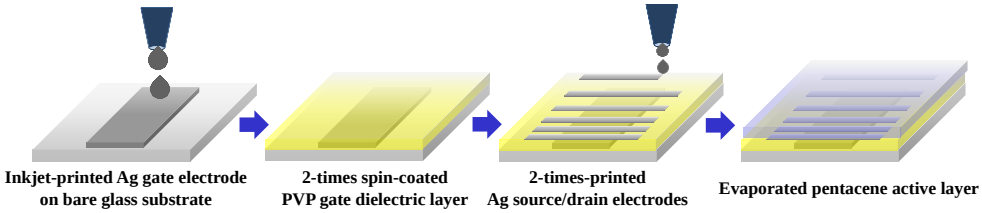


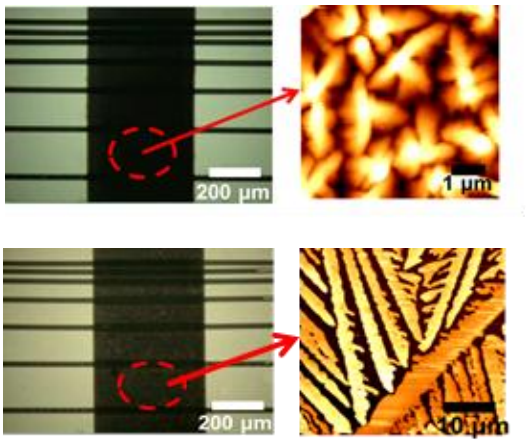
Figure 4.1 OTFTs fabrication process with narrow S/D electrodes for contact resistance extraction between inkjet-printed silver electrodes and evaporated pentacene semiconductor layer / spin-coated TIPS-pentacene.

.

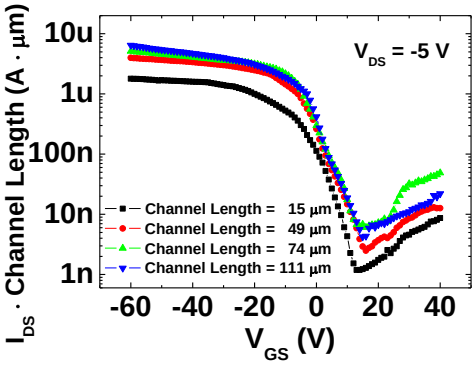
deposition. PVP is widely used as insulating layer material due to its good insulating performance and low temperature curing process [16, 17]. PVP solution was composed of 15 wt.% of PVP and 3 wt.% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) in propylene glycol methyl ether acetate (PGMEA) as a solvent. The solution was stirred using a magnetic spin bar at room temperature for 24 hours in air. PVP, CLA, and PGMEA were purchased from Sigma-Aldrich Co. PVP solution was spin-coated at 500 rpm for 5 seconds, then 4000 rpm for 30 seconds and thermally soft annealed at temperatures of 100 ℃ for 10 minutes on hot-plate. To minimize leakage current and surface roughness, we performed spin-coating again using the same coating and soft annealing conditions. After two-time spin coating, the PVP layer was annealed at 200 ℃ for 30 minutes in furnace. The thickness of the gate dielectric layer was about 1.2 μm. After the gate dielectric layer was deposited, silver S/D electrodes were also inkjet-printed with the same silver ink used for gate electrode fabrication. For contact resistance extraction between inkjet-printed silver electrodes and evaporated pentacene semiconductor layer using TLM, S/D electrodes should have narrow width and form various channel lengths with clean-edge in channel region because edge-waviness of S/D electrodes affect current flow between source/drain (I_{DS}) due to current concentration on wavy-peak areas [18]. To satisfy these requirements, 1 picoliter volume ink cartridge which has 9 μm nozzle diameters was used. Silver S/D electrodes were two-times inkjet-

printed on the spin-coated PVP gate dielectric layer at 60 ℃ to obtain more smooth surface and high conductivity, and then annealed at 150 ℃ for 20 minutes in a convection oven under atmospheric environment. Two-times printed S/D electrodes showed a sheet resistance of 1.2 Ω/□, having width and thickness of about 30 μm and 120 nm, respectively. Finally, pentacene and TIPS-pentacene were deposited by a thermal evaporation at 10^{-6} torr on 60 ℃ substrate, with a deposition rate of 0.3 Å /s and spin-coating method, respectively. The pentacene active area was defined by a shadow mask with opening of 1.5mm by 1mm. Thickness of the deposited evaporated pentacene and TIPS-pentacene layer was 60 nm and 120 nm, respectively. OTFTs with the inkjet-printed narrow S/D electrodes having channel length of 15 μm showed saturation mobility of 0.02 $cm^2/V{\cdot}s$ and 0.02 $cm^2/V{\cdot}s$, threshold voltage of 2.15 V and -2.4 V, and on/off ratio of 10^3 and 10^3 at V_{DS} of -20 V for evaporated pentacene and TIPS-pentacene OTFT, respectively. Figure 4.2 (a) shows optical images and atomic force microscope (AFM) images of the evaporated pentacene and TIPS-pentacene active layer on channel area for OTFTs with various channel length from 15 μm to 111 μm (AFM scan size is 5 μm by 5 μm for evaporated pentacene active layers). AFM image showed well-defined pentacene grain toward lateral direction, indicating that spin-coated PVP gate dielectric layer on inkjet-printed silver gate electrode has good surface roughness. The deposited pentacene film showed similar crystallinity with the previously reported results [11],

[13]. Figure 4.2 (b) shows channel length normalized transfer characteristic of the evaporated pentacene OTFTs with bottom-contact inkjet-printed silver S/D electrodes at drain-source voltage of -5 V. For OTFTs with short channel length (L=15 μm), the normalized drain-source current level was lower than other OTFTs with longer channel lengths because that of contact resistance more dominantly affects device performance as channel length gets short, leading to lower drain-source current. OTFTs with evaporated top- and bottom-contact silver and top- and bottom-contact gold S/D electrodes on inkjet-printed silver gate / spin-coated PVP gate dielectric layer were also fabricated for reference. To measure the electrical properties of the fabricated OTFTs, their current-voltage characteristics were measured in a dark box using Agilent 4155C semiconductor parameter analyzer. Thicknesses and surface profiles of metal and organic layers were measured using both TENCOR Alpha-step 500 and AFM from Park System. All fabrication processes and measurements were performed in air-ambient condition.



(a)

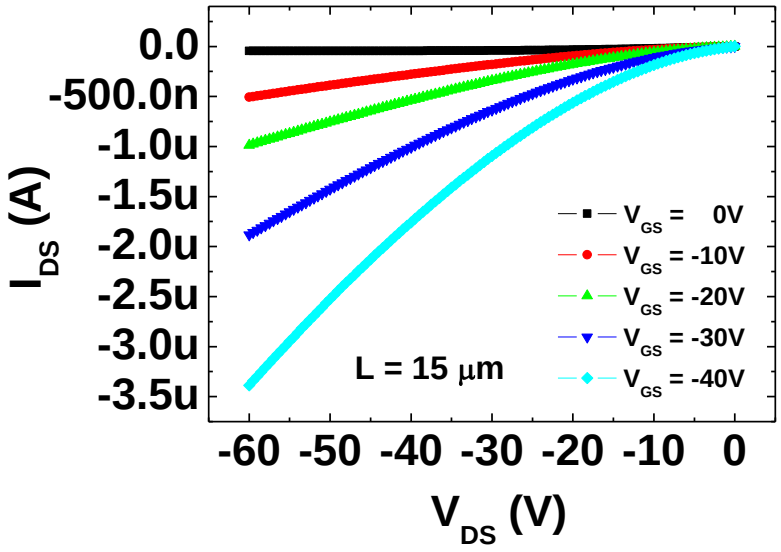


(b)

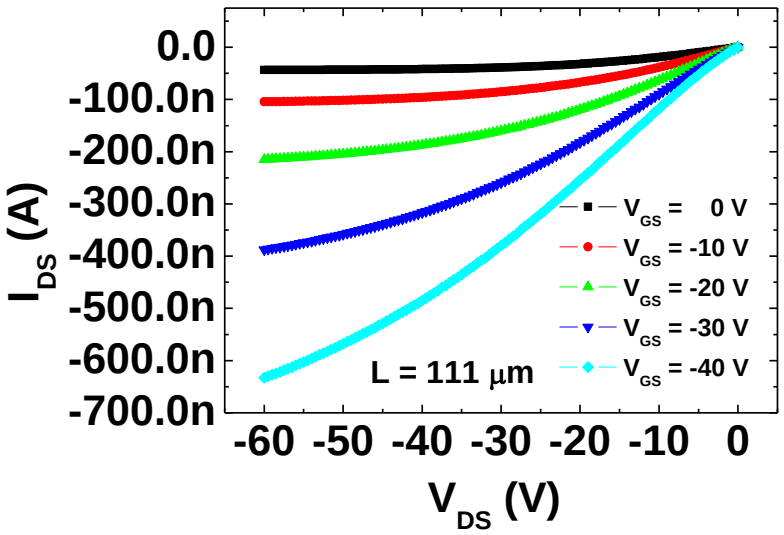
Figure 4.2 (a) Optical and AFM images of bottom-contact structured OTFTs channel area with inkjet-printed narrow silver S/D electrodes having various channel lengths and evaporated pentacene (top) / TIPS-pentacene (bottom). (b) Channel length normalized transfer characteristic of evaporated pentacene OTFTs with bottom-contact inkjet-printed silver S/D electrodes at drain-source voltage of -5 V.

4.3 Contact Resistance Extraction using Transmission Line Method

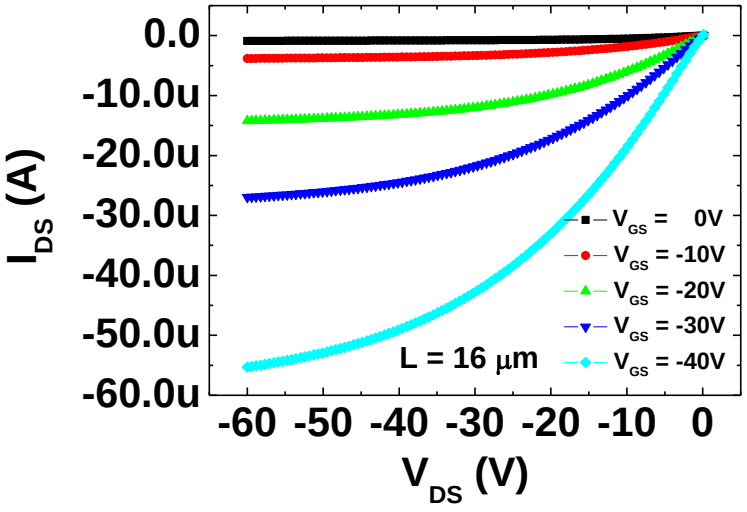
Figure 4.3 (a) and (b) show output characteristics of OTFTs with inkjet-printed S/D electrode for two different channel lengths. As mentioned above, channel resistance gets lower for OTFTs with shorter channel lengths, leading to current increase, at given bias voltages, while contact resistance gets relatively larger, resulting in S-shape behavior at low V_{DS} regime as shown in Fig. 4.3 (a). S-shape behavior is closely related to the parasitic resistance and gets less apparent when the channel length increases as shown in Fig. 4.3 (b). However, for top-contact OTFT structure, effect of the contact resistance is hardly observed even for the short channel devices as shown in Fig. 4.3 (c) since the staggered structure of gate and S/D can enhance carrier injection when biases are applied to each electrodes. In order to further analyze this contact resistance effect, we used TLM analysis. Since total resistance (R_{ON}) of the on-state OTFT operated in linear regime can be expressed as a summation of channel resistance ($R_{channel}$) and parasitic resistance ($R_{parasitic}$), contact resistance can be extracted by using the following equation [19-22].


0.0
-500.0n
-1.0u
-1.5u
-2.0u
-2.5u
-3.0u
-3.5u
I_DS (A)
-60 -50 -40 -30 -20 -10 0
V_DS (V)
L = 15 μm
V_GS = 0V
V_GS = -10V
V_GS = -20V
V_GS = -30V
V_GS = -40V

(a)


0.0
-100.0n
-200.0n
-300.0n
-400.0n
-500.0n
-600.0n
-700.0n
I_DS (A)
-60 -50 -40 -30 -20 -10 0
V_DS (V)
L = 111 μm
V_GS = 0 V
V_GS = -10 V
V_GS = -20 V
V_GS = -30 V
V_GS = -40 V

(b)



(c)

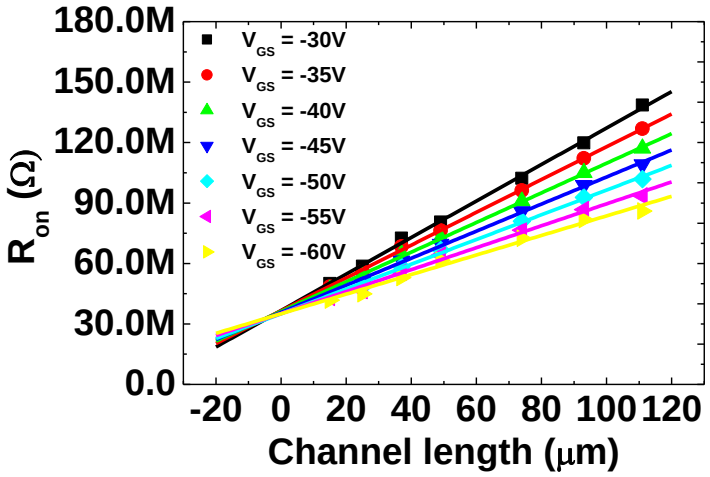
Figure 4.3 Output characteristics of evaporated pentacene OTFTs with bottom-contact inkjet-printed silver S/D, which have short channel length of (a) 15 μm, and long channel length of (b) 111 μm, and (c) top-contact evaporated gold S/D with channel length of 16 μm

$$R_{ON} = R_{channel} + R_{parasitic}$$

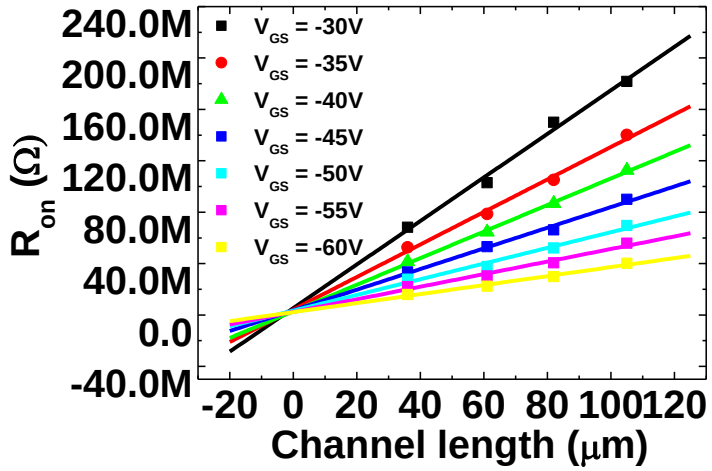
$$= \frac{L+2\Delta L}{WC_{ins}\mu_{FEi}(V_{GS}-V_T-\frac{V_{DS}}{2})}+2R_O$$

,where W, L, ΔL, V_{GS}, V_{DS} , μ_{FEi}, C_{ins}, V_T, and R_O are channel width, channel length, difference between effective channel length and mask (or patterned) channel length, gate-to-source voltage, drain-to-source voltage, intrinsic mobility, channel capacitance per unit area, threshold voltage and parasitic resistance at high V_{GS}, respectively. From the above equation, R_O can be extracted from linear plot of R_{ON} versus different channel lengths for various V_{GS}, by obtaining the intersection with y-axis as shown in Fig. 4.4. OTFT transfer characteristics in the linear regime were obtained at V_{DS} of -5 V and used for parameter extraction. By using TLM method, width normalized extracted R_O values for V_{GS} = -30 to -60 V were extracted to be about 1.79 MΩ·cm and 0.55 MΩ·cm, for bottom-contact inkjet-printed and evaporated silver S/D electrodes, respectively, as shown in Fig. 4.4 (a) and (b). To confirm quality of the evaporated pentacene and procedure of our analysis, we extracted the contact resistance of other reference OTFTs. As shown in Fig. 4.4 (c), (d), and (e), 0.06, 0.34 and 0.008 MΩ·cm were obtained for OTFTs with top-contact evaporated silver S/D, bottom-contact and top-contact gold S/D electrodes, respectively. The extracted values of these devices are consistent with the previously

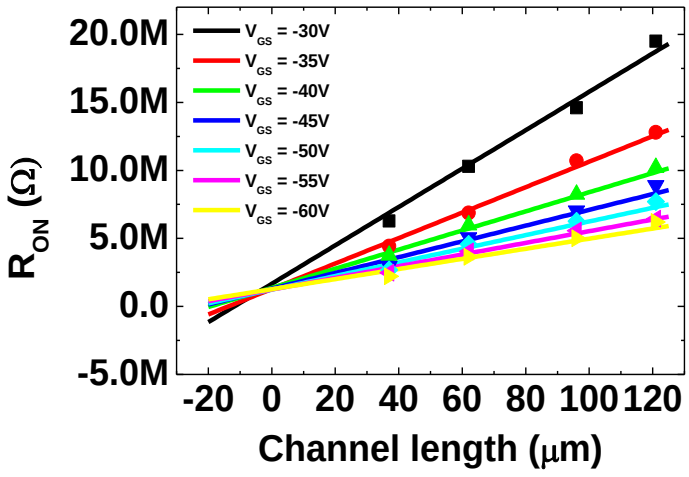
reported results [9], [23]. All the extracted values are summarized in Table 4.1. For the inkjet-printed silver electrodes, edge profile can affect the carrier injection properties because the printed electrodes are thicker than the semiconductor layer in comparison with the evaporated electrodes (70 nm) and often show rough surface at their edges. As shown in Fig. 4.5, there is larger area of small molecule packaging and poor ordering near the inkjet-printed silver S/D electrodes compared with that near the evaporated silver S/D electrodes. It was reported that small grain size near sides of the S/D electrodes could lead to poorer ordering of pentacene molecules and thus, higher contact resistance [10]. In addition, slight oxidation during 150 ℃ silver ink sintering process can be also expected to increase contact resistance between S/D electrodes and pentacene layer. Although acid-treatment can remove oxidation layer on the printed electrodes if any, it may not be appropriate for organic gate dielectric in all-inkjet-printed OTFTs. Instead, we are under current investigation of surface treatment compatible with the organic gate dielectric layer. Our preliminary results show that organic treatment can reduce oxygen component on the printed silver electrodes, which is expected to improve OTFT performance.


180.0M
150.0M
120.0M
90.0M
60.0M
30.0M
0.0
R_on (Ω)
V_GS = -30V
V_GS = -35V
V_GS = -40V
V_GS = -45V
V_GS = -50V
V_GS = -55V
V_GS = -60V
-20 0 20 40 60 80 100 120
Channel length (μm)

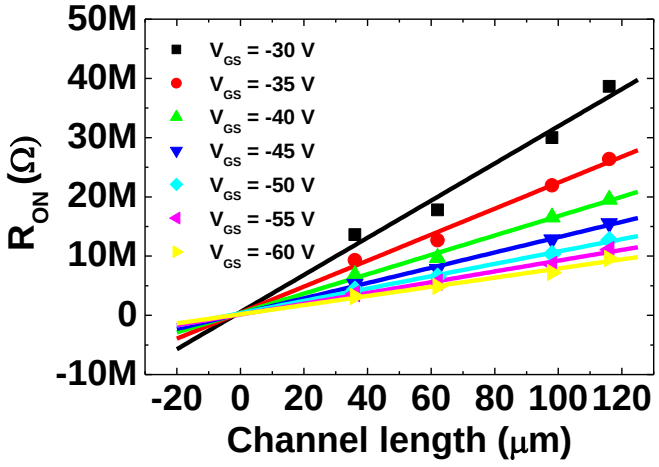
(a)


240.0M
200.0M
160.0M
120.0M
80.0M
40.0M
0.0
-40.0M
R_on (Ω)
V_GS = -30V
V_GS = -35V
V_GS = -40V
V_GS = -45V
V_GS = -50V
V_GS = -55V
V_GS = -60V
-20 0 20 40 60 80 100 120
Channel length (μm)

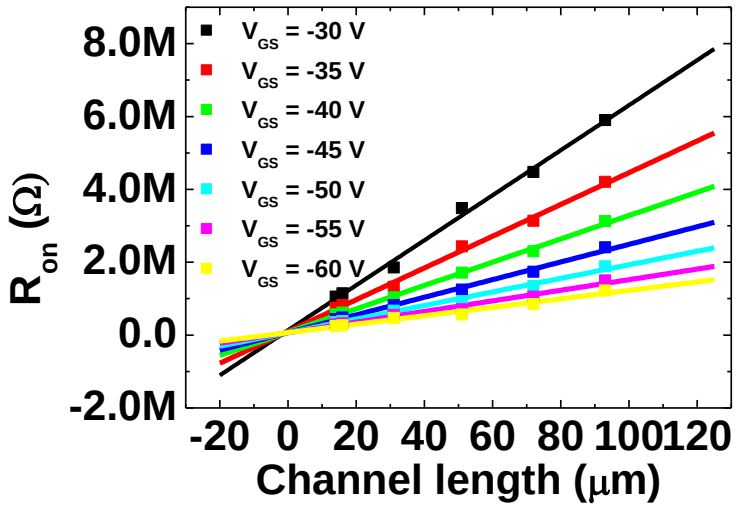
(b)


20.0M
15.0M
10.0M
5.0M
0.0
-5.0M
R_ON (Ω)
V_GS = -30V
V_GS = -35V
V_GS = -40V
V_GS = -45V
V_GS = -50V
V_GS = -55V
V_GS = -60V
-20 0 20 40 60 80 100 120
Channel length (μm)

(c)

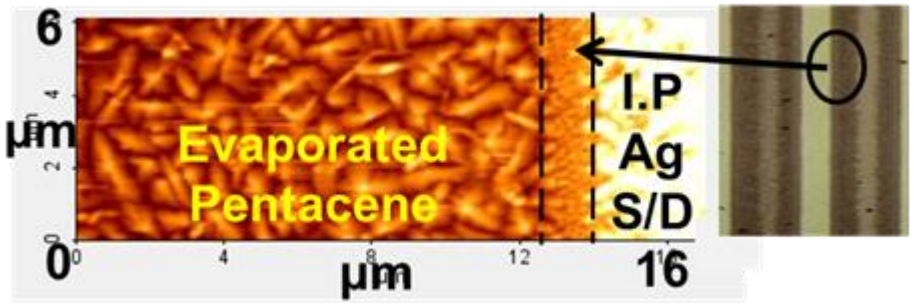

50M
40M
30M
20M
10M
0
-10M
R_ON (Ω)
V_GS = -30 V
V_GS = -35 V
V_GS = -40 V
V_GS = -45 V
V_GS = -50 V
V_GS = -55 V
V_GS = -60 V
-20 0 20 40 60 80 100 120
Channel length (μm)

(d)

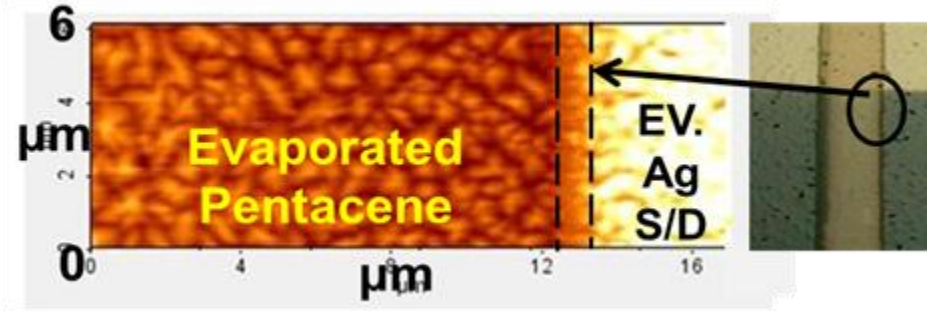


(e)

Figure 4.4 TLM results for OTFTs with (a) bottom-contact inkjet-printed / (b) bottom-contact evaporated / (c) top-contact evaporated silver S/D electrodes and (d) bottom-contact / (e) top-contact evaporated gold S/D electrodes.



(a)



(b)

Figure 4.5 AFM images of pentacene active layer for bottom-contact OTFTs with (a) inkjet-printed / (b) evaporated silver S/D electrodes.

Table 1 Summarized results for contact resistance between evaporated pentacene and various S/D electrodes

Top / Bottom Contact (TC / BC)	Inkjet-Printed Ag (BC)	Evaporated Ag (BC)	Evaporated Ag (TC)	Evaporated Au (BC)	Evaporated Au (TC)
Contact resistance (MΩ·cm)	1.79	0.55	0.06	0.34	0.008

For silver electrodes, energy level mismatch between silver electrode work function (4.52 ~4.74 eV) [24] and evaporated pentacene HOMO (highest occupied molecular orbital) level (5.07 eV) [25] can cause high hole-injection barrier corresponding to high contact resistance. This energy level mismatch seems to have more critical effect for the top-contact structure. The contact resistances of the silver and gold electrodes were similar for the bottom-contact structure while the gold electrode showed one-order of magnitude lower contact resistance for the top-contact structure as shown in Table 1. Therefore, for the printed S/D electrodes in bottom-contact structure, surface properties can have more effects on the contact resistance.

We also extracted contact resistance for all-solution processed OTFT with TIPS-pentacene active layer and inkjet-printed silver electrodes. All-solution processed OTFTs with inkjet-printed narrow S/D electrodes having channel length

of 14~15 μm showed saturation mobility of 0.02 $cm^2/V \cdot s$, threshold voltage of -2.4 V, and on/off ratio of 10^3 at V_{DS} of 20 V, and OTFT with TIPS-pentacene active layer shows lower sub-threshold swing value comparing to that with evaporated pentacene as previously reported results [16] as figure 4.6 shown. In output characteristics result, there is large S-shape at low V_{DS} regime due to high contact resistance which gets larger as channel length is shorted because channel resistance gets lower relatively (Fig. 4.7). Extracted contact resistance value of 2.18 MΩ·cm for OTFT with inkjet-printed silver S/D and TIPS-pentacene active layer was higher than those of other OTFTs because of poor surface properties and work function mismatching resulting in poor hole-injection property (Fig 4.8). Because of energy level mismatching between silver electrode work function (from 4.52 to 4.74eV) [24] and TIPS-pentacene HOMO (highest occupied molecular orbital) level (5.30 eV) [26], high hole-injection barrier corresponding high contact resistance values are expected, resulting in S-shape at output characteristics.

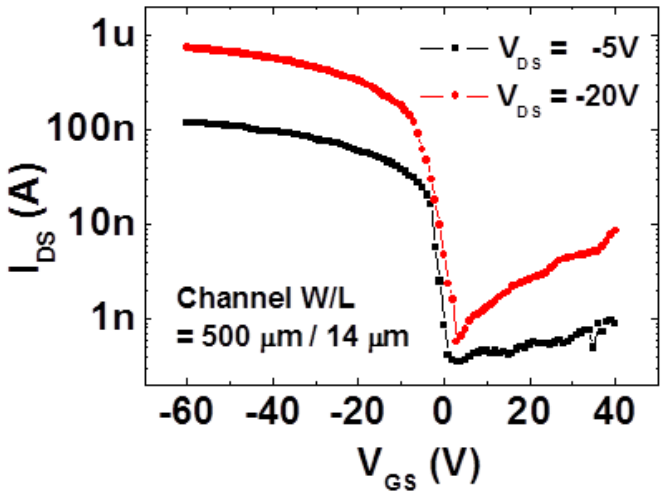
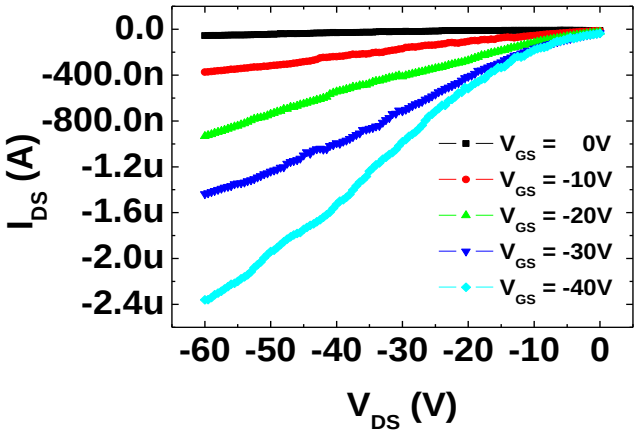
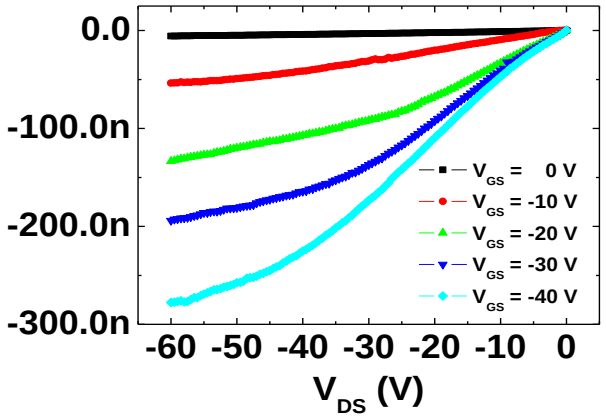


Figure 4.6 Transfer characteristics for all-solution processed short channel OTFTs with spin-coated TIPS-pentacene

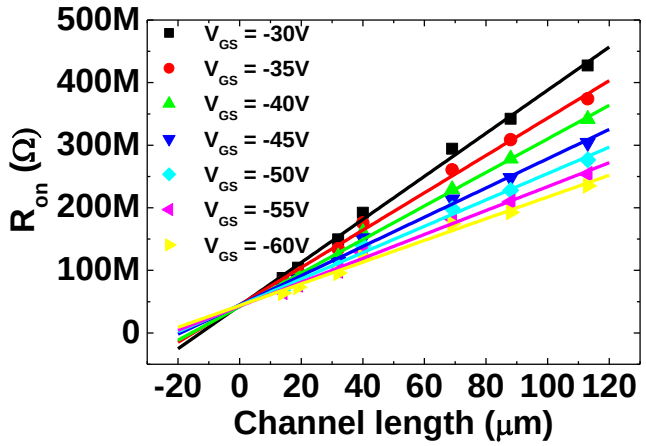


(a)

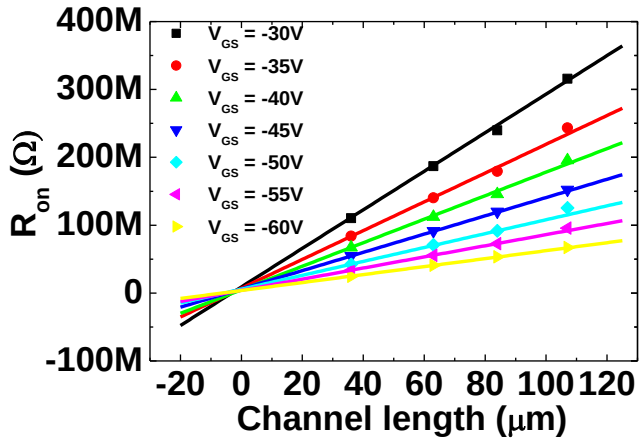


(b)

Figure 4.7 Output characteristics for all-solution processed OTFTs with different channel length of (a) 14 μm (b) 113 μm. Because contact resistance is more dominant in short channel OTFT relatively, large S-shape was appeared at low V_{DS} regimes in (a).



(a)



(b)

Figure 4.8 Contact resistance extraction results between (a) inkjet-printed silver electrodes and TIPS-pentacene (b) evaporated silver electrodes and TIPS-pentacene using TLM analysis.

4.4 Contact Properties Analysis between Inkjet-Printed Silver Electrode and Organic Semiconductor Layer using Scanning Kelvin Probe Microscopy (SKPM)

As mentioned in chapter 4.3, contact properties between source / drain (S/D) electrodes and organic semiconductor layer are very important, especially inkjet-printed OTFT having short channel operated in low voltage. Although transmission line method (TLM) analysis is widely used to extract parasitic resistance between S/D electrodes and semiconductor layer, several channel lengths and uniformly deposited active layer should be guaranteed to obtain contact resistance from the intersection with y-axis in linear plot of R_{ON} versus channel length at various $V_{GS.}$ Recently, scanning kelvin probe microscopy (SKPM) analysis is one of most powerful techniques to investigate contact properties and intrinsic semiconductor [27]-[30]. Especially, many research groups have studied the voltage drop between S/D electrodes and semiconductor layer to obtain contact resistance, intrinsic mobility extraction and voltage drop on grain boundary of organic semiconductor in bottom contact TFTs using SKPM method. However, they only reported the relative contact resistance and voltage drop on contact and channel region in polymer, amorphous phase or single crystal semiconductor TFTs [28]-[30]. In small molecule or high-crystalline organic semiconductor, especially TIPS-pentacene OTFT, effective channel investigation using potential distribution analysis is necessary because TIPS-pentacene OTFT shows electrical characteristics variance depending

on its crystalline size or direction. Moreover, contact properties improvement is also required for high-performance and low power consumption OTFT demonstration. In this chapter, we introduce the SKPM principle and its application in our research and investigate contact properties between inkjet-printed silver electrode and TIPS-pentacene semiconductor layer using SKPM resulting in contact resistance extraction from potential drop between inkjet-printed silver S/D and TIPS-pentacene active layer. In addition, we also report the contact properties improvement by adopting surface treatment on inkjet-printed silver electrode.

SKPM is one of electrostatic force microscopy (EFM) mode which is a technique used to map local electrical properties on a sample surface by measuring the electrostatic force between the surface and the tip where an AC voltage is applied. The resulting electrostatic signal provides information related to surface potential. Typically, EFM is classified into two modes: one is standard EFM and the other is enhanced EFM. Standard EFM mode measures topography image at first scan where van der waals force is dominant, and then electrostatic force is measured toward topography at second scan after the tips is lift off until van der waals force is neglected. Thus, from the second scan, the van der waals force free EFM signal can be obtained. Enhanced mode uses an external Lock-in Amplifier to apply AC bias of frequency ω to the EFM tip, and to separate the frequency ω component from the output signal. From the below equation,

$$F = F_a + F_{cap} + F_{coulomb}$$

where F, F_a, F_{cap} and $F_{coulomb}$ are force between tip and sample, repulsive atomic force on the tip, capacitance potential and coulomb force, respectively. External lock-in system supply AC voltage signal between tip and sample which is expressed in below equation.

$$V = -V_{surfacepotential} + V_{dc} + V_{ac}\cos(\omega t)$$

$$F = F_a(\vec{r}) + \frac{1}{2}\frac{dC(\vec{r})}{dz}\left(V_{dc} - V_s + V_{oc}\cos(\omega t)\right)^2 + E_s(\vec{r})C(\vec{r})\left(V_{dc} + V_{oc}\cos(\omega t)\right)$$

$$= \left(F_a(\vec{r}) + \frac{1}{2}\frac{dC(\vec{r})}{dz}\left(V_{dc} - V_s\right)^2 + \frac{1}{4}V_{OC}{}^2\frac{dC(\vec{r})}{dz} + E_s(\vec{r})C(\vec{r})V_{dc}\right)$$

$$+\left(\frac{dC(\vec{r})}{dz}\left(V_{dc} - V_s\right) + E_s(\vec{r})C(\vec{r})\right)V_{oc}\cos(\omega t) + \frac{1}{4}\frac{dC(\vec{r})}{dz}V_{oc}{}^2\cos(2\omega t)$$

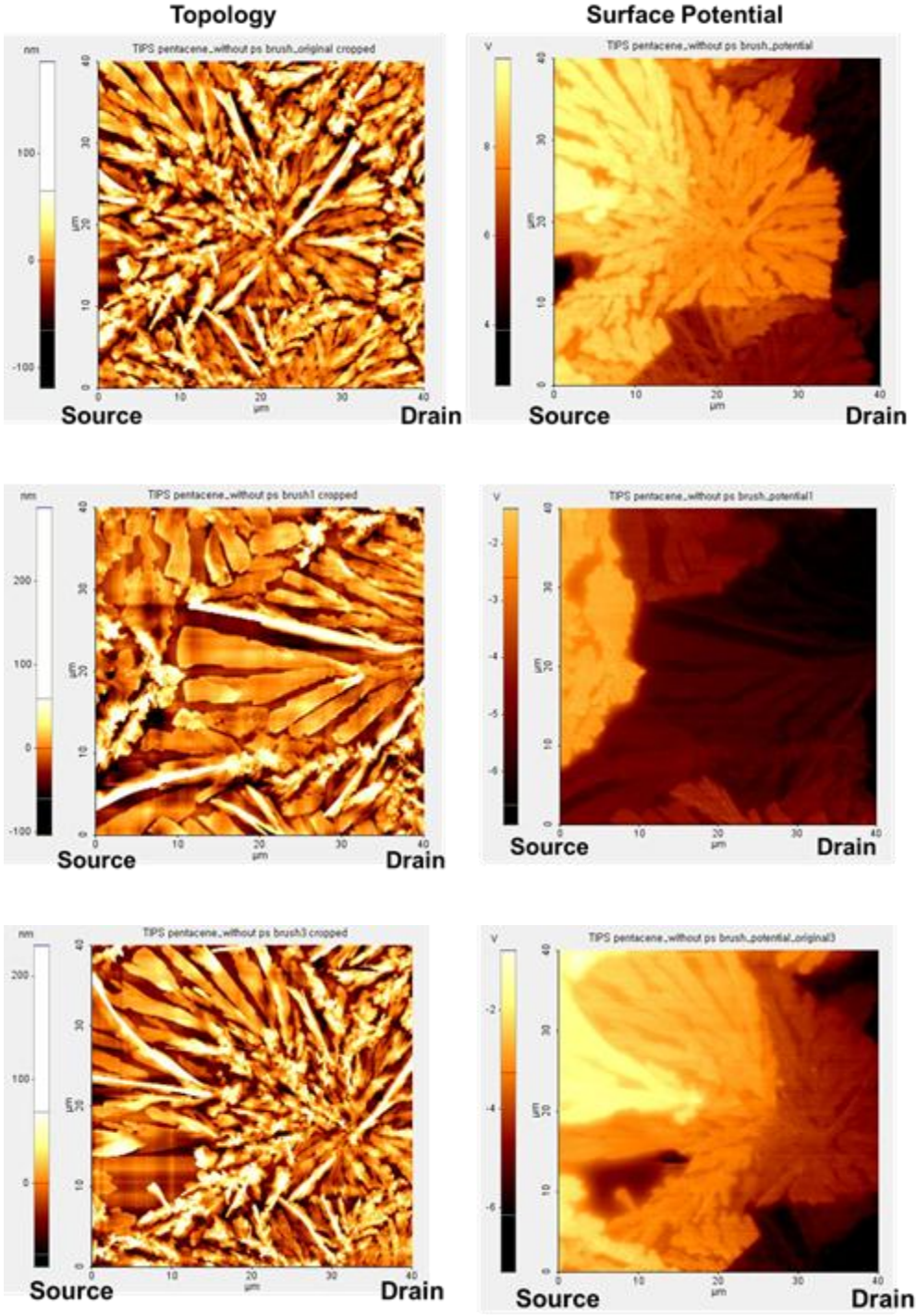
SKPM controls by feedback to keep $V_{oc}\cos(\omega t)$ term zero, which means that EFM amplitude and phase are zero and V_{dc} supply bias should be $V_{surface\ potential}$, thus we can measure the surface potential during just one time scanning.

For OTFTs fabrication, Corning Eagle2000™ bare glass substrate was used after

cleaned in ultrasonic baths of acetone and isoprophyl alcohol for 20 and 10 minutes, respectively, and rinsed by deionized water. After the glass substrate was dried at 200 ℃ in oven, silver gate electrodes were inkjet-printed on the substrate whose temperature was maintained at 60 ℃. Inkjet-printed silver electrodes which have shiny appearance, clean-edge and better surface properties were obtained after the substrate was annealed at 150 ℃ for 30 minutes in a convection oven under atmospheric environment. Width and thickness of the inkjet-printed gate electrode were about 1000 μm and 200 nm, respectively. We used silver metal-organic precursor type silver ink from inktec corp. (TEC-IJ-010) which has silver contents of 20 wt% and a drop-on-demand inkjet printer from DIMATIX corp. (DMP-2800 series). On the printed silver gate electrodes, PVP was spin-coated for gate dielectric layer deposition. PVP solution was composed of 15 wt.% of PVP and 3 wt.% of poly(melamine-co-formaldehyde) as a cross-linking agent (CLA) in propylene glycol methyl ether acetate (PGMEA) as a solvent. The solution was stirred using a magnetic spin bar at room temperature for 24 hours in air. PVP, CLA, and PGMEA were purchased from Sigma-Aldrich Co. PVP solution was spin-coated at 500 rpm for 5 seconds, then 4000 rpm for 30 seconds and thermally soft annealed at temperatures of 100 ℃ for 10 minutes on hot-plate. To minimize leakage current and surface roughness, we performed spin-coating again using the same coating and soft annealing conditions. After two-times spin coating processes, the PVP layer was

annealed at 200 ℃ for 30 minutes in furnace. The thickness of the gate dielectric layer was about 1.1 μm. After the gate dielectric layer was deposited, silver S/D electrodes were also inkjet-printed with the same silver ink used for gate electrode fabrication. Finally, 1 wt.% TIPS-pentacene which is dissolved in toluene was deposited by drop-cast method as active layer.

Figure 4.9 shows AFM and SKPM images for TIPS-pentacene active layer having various crystallinity size and growth direction while OTFT was operated in V_{GS} and V_{DS} of -10 V and -12 V, respectively. Although TIPS-pentacene active layer was well-grown on PVP layer showing large grain and good crystallinity in AFM images, actually their surface potential images which indicate effective carrier transport channel depend on crystallinity growth direction, cracks or layer packaging. Most of V_{DS} was dropped at grain boundary or perpendicularly grown TIPS-pentacene crystalline where large cracks or vacancy is showed, while there is nearly potential drop in common grain back-born. Therefore, for high-performance OTFT fabrication, crystallinity growth without any cracks and growth direction are very important, especially long channel OTFT and investigation for surface potential distribution in channel region is necessary as well as topography measurement.


Topology
Surface Potential
TIPS pentacene_without ps brush_original cropped
TIPS pentacene_without ps brush_potential
TIPS pentacene_without ps brush1 cropped
TIPS pentacene_without ps brush_potential1
TIPS pentacene_without ps brush3 cropped
TIPS pentacene_without ps brush_potential_original3
Source
Drain
nm
V
µm

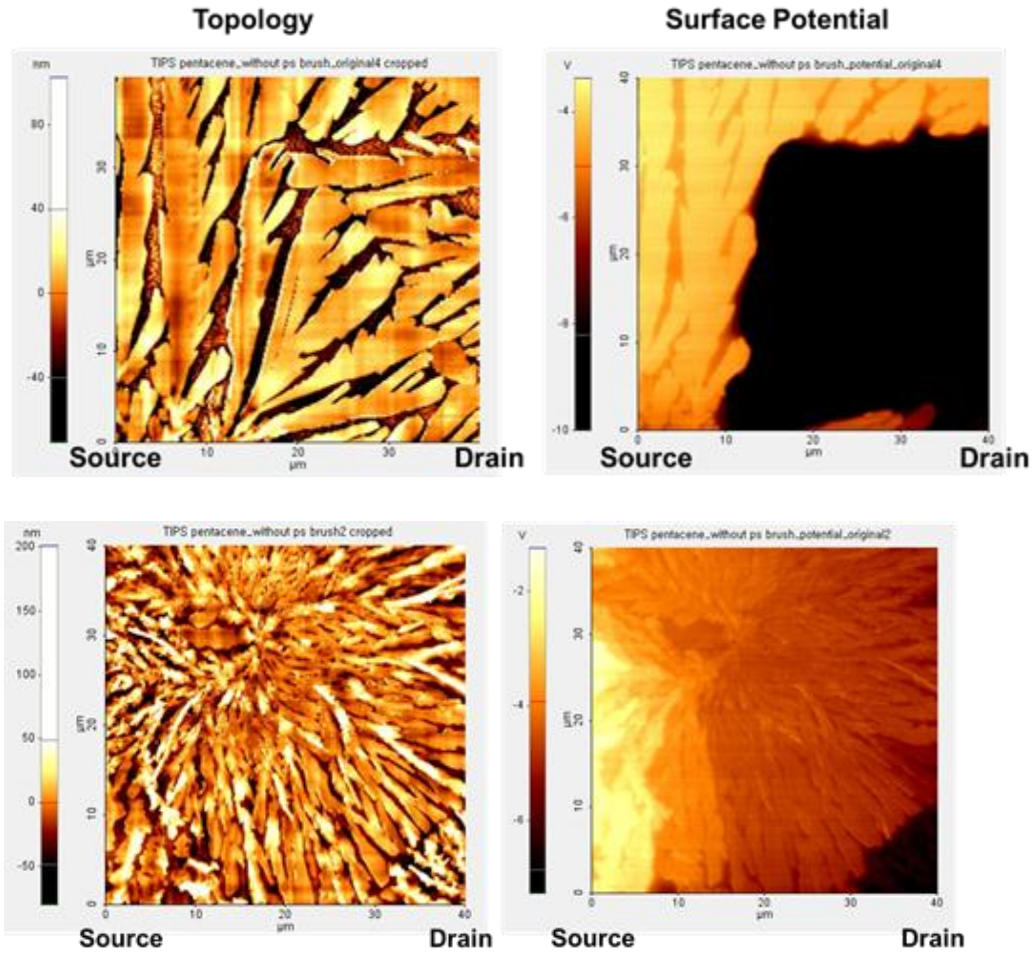
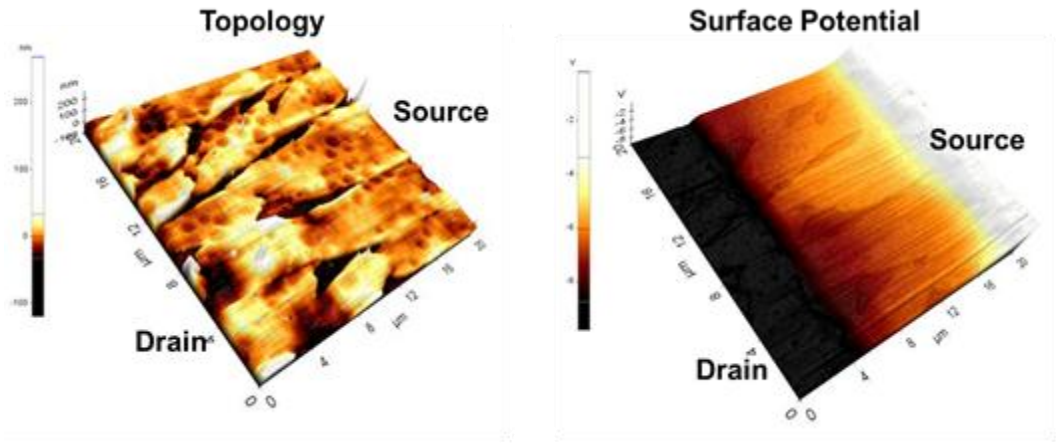


Figure 4.9 Various AFM (left) and SKPM (right) images depending on TIPS-pentacene crystallinity growth direction, cracks / vacancy or grain size during operation of OTFTs. There is large potential drop at grain boundary and cracks.

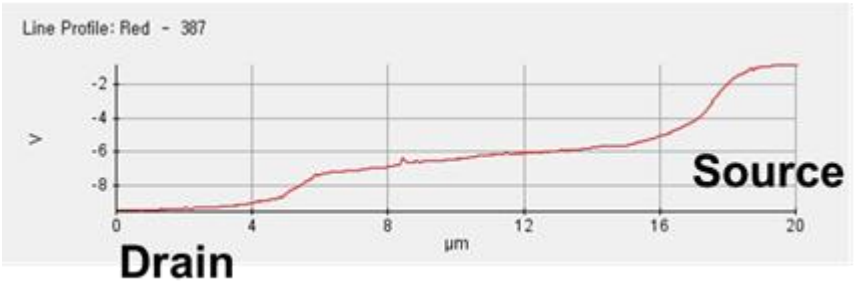
In short channel OTFT, because potential drop at contact between S/D electrodes and semiconductor layer is more dominant than potential drop at grain boundary or semiconductor itself [29]-[30], potential drop at contact area should be also investigated. Figure 4.7 shows AFM and SKPM images for inkjet-printed OTFT having channel length of 12 μm. Although channel region is not distinguished in AFM image because TIPS-pentacene layer covered not only channel area but also inkjet-printed S/D electrodes, there is clearly exposed channel region in SKPM images due to surface potential difference. As expected, voltage drop was occurred dominantly at contact region compared with channel region because of little grain boundary and crack on TIPS-pentacene active layer in short channel region. From these results, we conclude that when high-crystalline semiconductor is used as active layer, crystallinity size, grown direction and cracks on active layer which are main factor for potential drop at channel region are more important in long channel OTFT, while contact properties is more dominant in short channel OTFT. Therefore, work function modification, surface treatment or additional buffer layer between inkjet-printed silver electrode and TIPS-pentacene active layer is necessary for high-performance OTFT. To improve contact properties, PS-brush which is mentioned in chapter 3 was used for additional layer on silver S/D electrodes. For surface treatment on silver S/D electrodes, PS-brush was dissolved in toluene with 0.4 wt.% and stirred at room temperature with 300 rpm for 1 hour. Because the PS-brush is

chemically coupled with the hydroxyl groups, UV ozone treatment was performed with 28 mW/cm^2 for 10 minutes to increase the hydroxyl groups. Because UV ozone treatment can oxidize silver electrode resulting in its conductivity reduction, UV ozone treatment time was minimized. After prepared PS-brush solution was inkjet-printed onto UV ozone treated silver electrode and channel region, baked on 110 ℃ hot-plate for 1 hour in air for chemical coupling reaction. Finally, it was rinsed in toluene to remove the reducible PS-brush material. We expected PS-brush treatment to improve not only OTFT electrical characteristics by minimizing the number of polar moieties and interface trap but also contact properties between inkjet-printed silver S/D electrode and TIPS-pentacene active layer. Figure 4.10 shows optical, AFM and SKPM images for all-inkjet-printed OTFTs with / without PS-brush treatment. By adopting PS-brush treatment on PVP gate dielectric layer, TIPS-pentacene active layer was not only well-deposited corresponding better channel formation from optical and AFM images as mentioned in chapter 3, but better electrically effective channel which indicate higher conductive channel was also formed from SKPM image showing better electrical performance as shown figure 4.11. In addition, potential drop was also reduced from 4 V to 1.5 V at contact region which indicate it improve adhesion property of TIPS-pentacene on silver electrode corresponding to reduce contact resistance between silver S/D electrodes and TIPS-pentacene active layer. From figure 4.12, the chemically-coupled PS-brush layer

dramatically improve not only electrical performance including mobility and on/off ratio, but also charge injection property at low V_{DS} regime. To verify the chemically coupled PS-brush layer on inkjet-printed silver electrode, XPS analysis was also performed. As shown in figure 4.13, there is a C1s intense peak near binding energy of 284 eV due to the C1s orbitals of silicon moieties in the PS backbone, whereas the peaks were detect hardly on bare and UV ozone treated silver electrodes. From this XPS result, we conclude that PS-brush was chemically well-coupled not only on PVP layer, but also silver electrode.

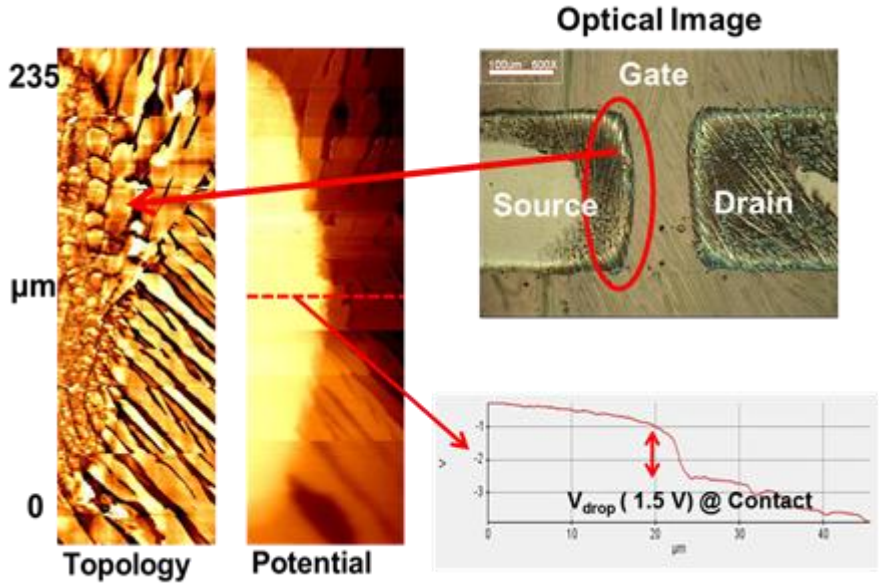


(a)

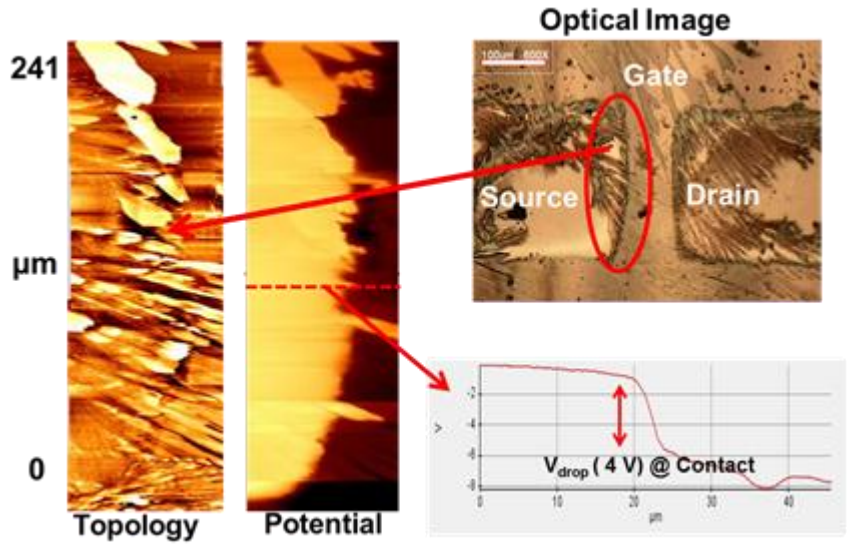


(b)

Figure 4.10 (a) AFM (left) and SKPM (right) images for short channel TIPS-pentacene OTFT, and (b) a voltage drop profile from source to drain electrode

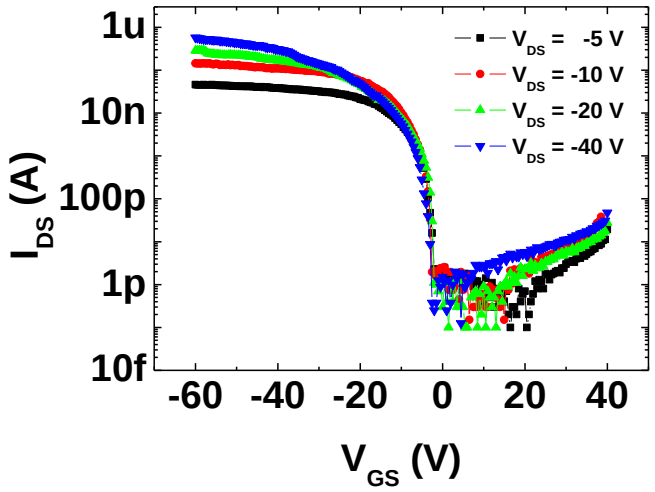


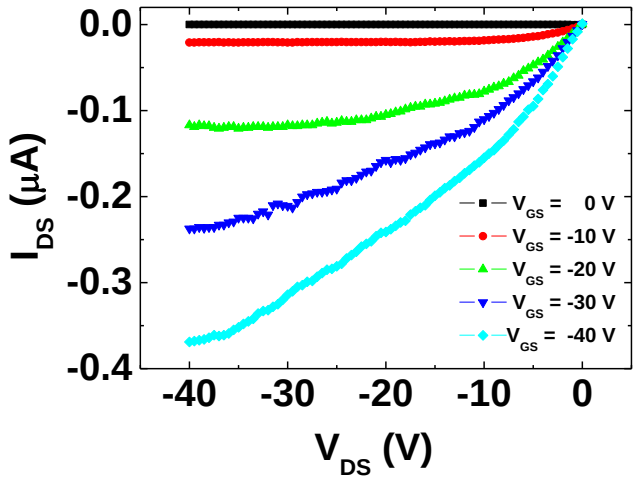
(a)



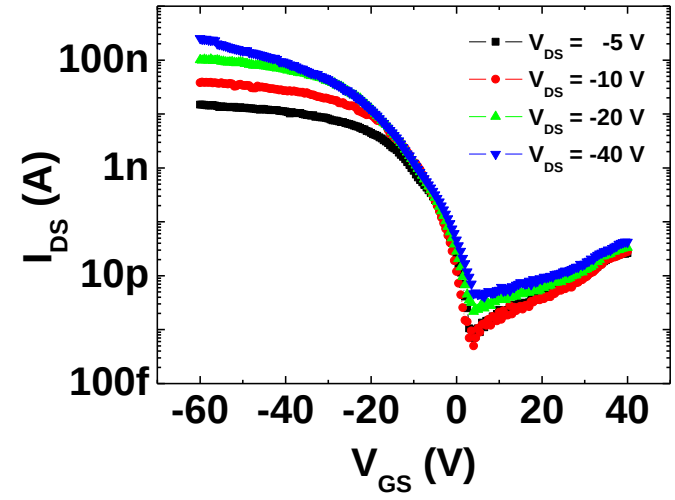
(b)

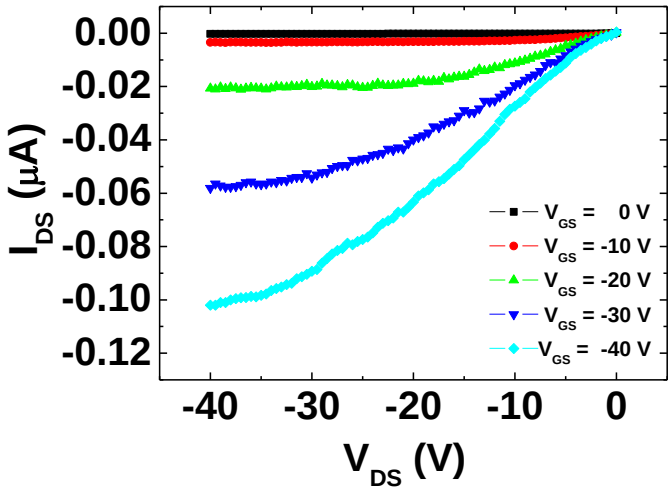
Figure 4.11 Optical, AFM and SKPM images of all-inkjet-printed OTFTs (a) with / (b) without PS-brush treatment on silver S/D electrodes.


1u
10n
100p
1p
10f
I_DS (A)
-60
-40
-20
0
20
40
V_GS (V)
V_DS = -5 V
V_DS = -10 V
V_DS = -20 V
V_DS = -40 V


0.0
-0.1
-0.2
-0.3
-0.4
I_DS (μA)
-40
-30
-20
-10
0
V_DS (V)
V_GS = 0 V
V_GS = -10 V
V_GS = -20 V
V_GS = -30 V
V_GS = -40 V

(a)





(b)

Figure 4.12 Electrical characteristics of all-inkjet-printed OTFTs (a) with / (b) without PS-brush treatment on silver S/D electrodes.

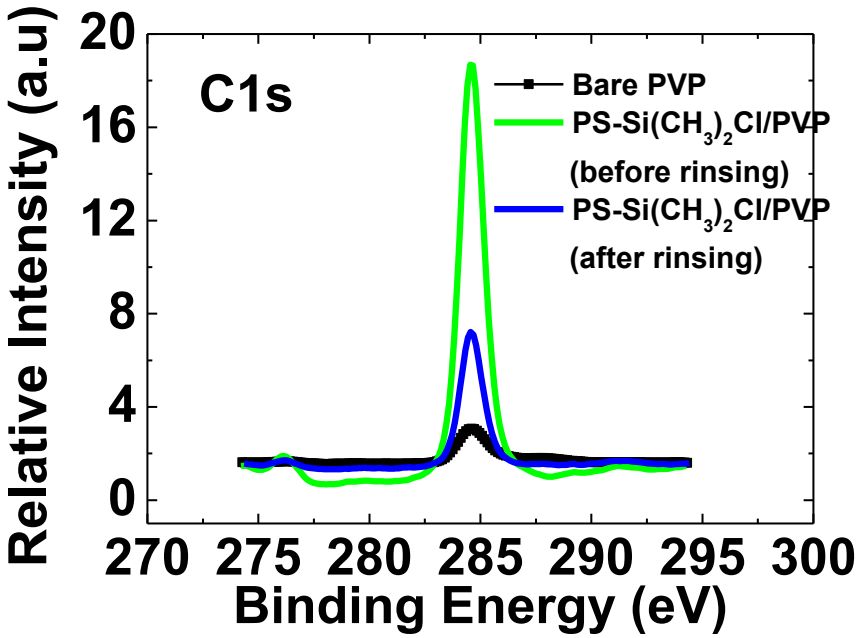


Figure 4.13 XPS C1s profile for PS-brush treated Ag S/D electrodes

4.5 Conclusion

In this chapter, we report contact resistance analysis between inkjet-printed silver S/D electrodes and evaporated pentacene and TIPS-pentacene semiconductor layers for bottom-contact OTFTs using TLM and SKPM analysis. Moreover, we also investigated the potential drop on channel and contact region by using SKPM analysis. The extracted contact resistance is larger than those in cases of the evaporated electrodes and top-contact structure. In order to further improve the contact properties and active layer deposition of the potentially all-inkjet-printed OTFTs, additional carrier injection layer insertion or surface treatment for the bottom-contact printed S/D electrodes and gate dielectric layer is necessary. By adopting PS-brush treatment, we obtained not only better electrical performance from well-deposited TIPS-pentacene active layer, but also better contact properties showing potential drop reduction at contact region. Therefore, from these results, surface treatment on gate dielectric and S/D electrode which is adjust with organic semiconductor layer is necessary for high-performance OTFT, especially short channel contact limited device and PS-brush is regarded as a promising candidate for surface treatment material.

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L. C. Teague, O. D. Jurchescu, C. A. Richter, S. Subramanian, J. E. Anthony, T. N. Jackson, D. J. Gundlach, and J. G. Kushmerick, “Probing stress effects in single

crystal organic transistors by scanning Kelvin probe microscopy" *Appl. Phys. Lett.* vol. 96, 203305 (3pp), 2011.

Chapter 5

All-Inkjet-Printed Stretchable OTFTs on Elastomeric Substrate

5.1 Introduction

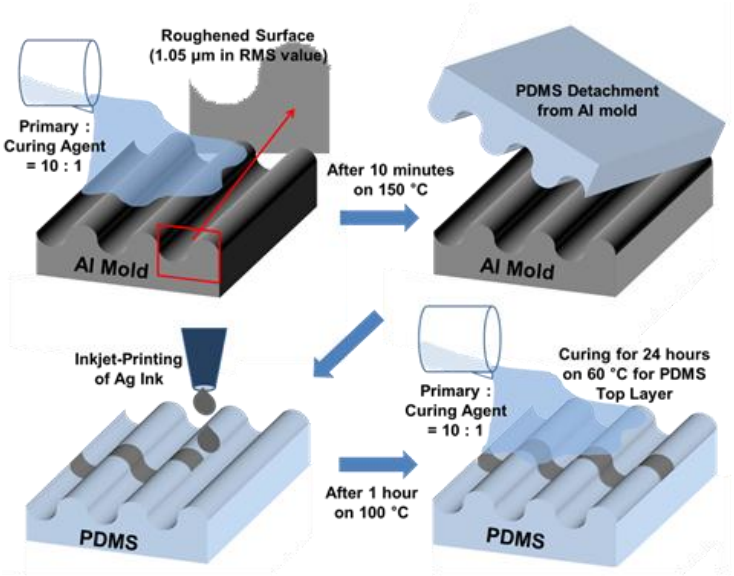
Recently, stretchable electronics has attracted much interest for applications including flexible display, wearable electronics and biomedical devices [1]-[3]. Because stretchable display is one of most promising candidates for next generation display, many research groups have studied highly stretchable materials for electronic device fabrication, especially interconnection deposition [4]. Minimization of resistance change under externally applied stress is one of the most important factors for highly reliable and stable electrical operation. For high performance stretchable electrodes with low resistance, several formation methods were reported including electro-plating [5], liquid alloy metal filling [5], evaporated

thick metal film transfer from a rigid substrate to a compliant substrate [7]-[8], and vacuum evaporation on modified compliant substrates [9]-[10]. In most cases, either complicated or expensive vacuum processes have been used although the stretchable electrodes showed reasonable performances. Especially, directly deposited thick metal films on a compliant substrate typically show poor stretchability [11]. Stress accumulation and temperature increase should be well controlled during relatively long deposition process for better performance [10]. In order to reduce the fabrication cost and to further simplify the fabrication process, a direct inkjet-printing process can be adopted since it has been widely used in flexible large-area electronics applications because of its ultra-low-cost, environment friendly, non-vacuum and easy process property. In addition, by increasing the number of printings, thick and low-resistance metal electrodes can be obtained [12]. Although inkjet-printing conditions for high electrical performance electrodes, such as inkjetting, annealing and substrate treatment, have been well optimized for silicon dioxide, glass and flexible plastic substrates [13], there are key issues of adhesion and thermal annealing for elastomeric substrates like poly(dimethylsiloxane) (PDMS). Moreover, in recently published results, stretchable inkjet-printed electrodes on PDMS substrate showed poor stretching performance due to poor adhesion property between silver ink and PDMS substrate from Lacour's group [14] Therefore, in this chapter, we report high performance stretchable electrode under

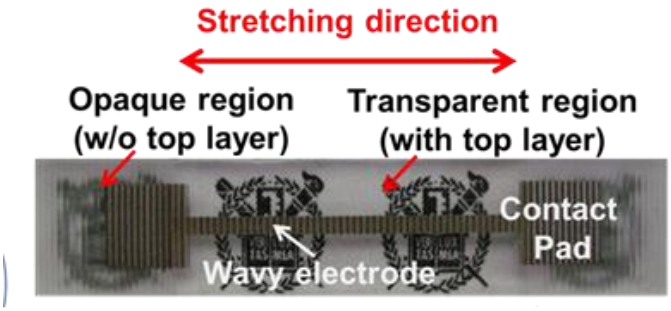
lateral tensile strain stress using optimized inkjet-printing process. To obtain high-performance stretchable electrode, surface roughness and wave structured elastomeric PDMS substrate were adopted. Ultraviolet (UV) ozone treatment and intentionally roughened surface improved adhesion between highly conductive silver nano particle ink and the PDMS surface. Two-times printed silver electrodes showed low resistance and stably repeated stretching properties on the wave structured PDMS substrate.

5.2 High-Performance Inkjet-Printed Stretchable Electrode Fabrication on Wavy Elastomeric Substrate

Figure 5.3 shows procedure of fabricating inkjet-printed silver (Ag) electrodes on a wave structured elastomeric PDMS substrate that has intentionally roughened surface. Wavy structure improved stretching performance of the printed Ag electrode, which will be later discussed in detail. Mixture of PDMS (Sylgard 184, Dow Corning) and curing agent with 10:1 weight ratio was poured on an aluminum (Al) mold having wavy patterns with period and amplitude of 200 μm. Surface of the Al mold was intentionally roughened by wire-electro discharging machining (wire-EDM), resulting in surface roughness of 1.05 and 5.14 μm in average root-mean-square (RMS) and peak-to-peak values, respectively. After baked for 10 minutes on 150 ℃ hot plate in air, the PDMS substrate was detached, which had both wavy structure and rough surface transferred from the Al mold. It is noted that the roughened surface provides both good adhesion of fluids [14]-[15] and uniform distribution of film stress for Ag line when tensile strain is applied [10].



(a)



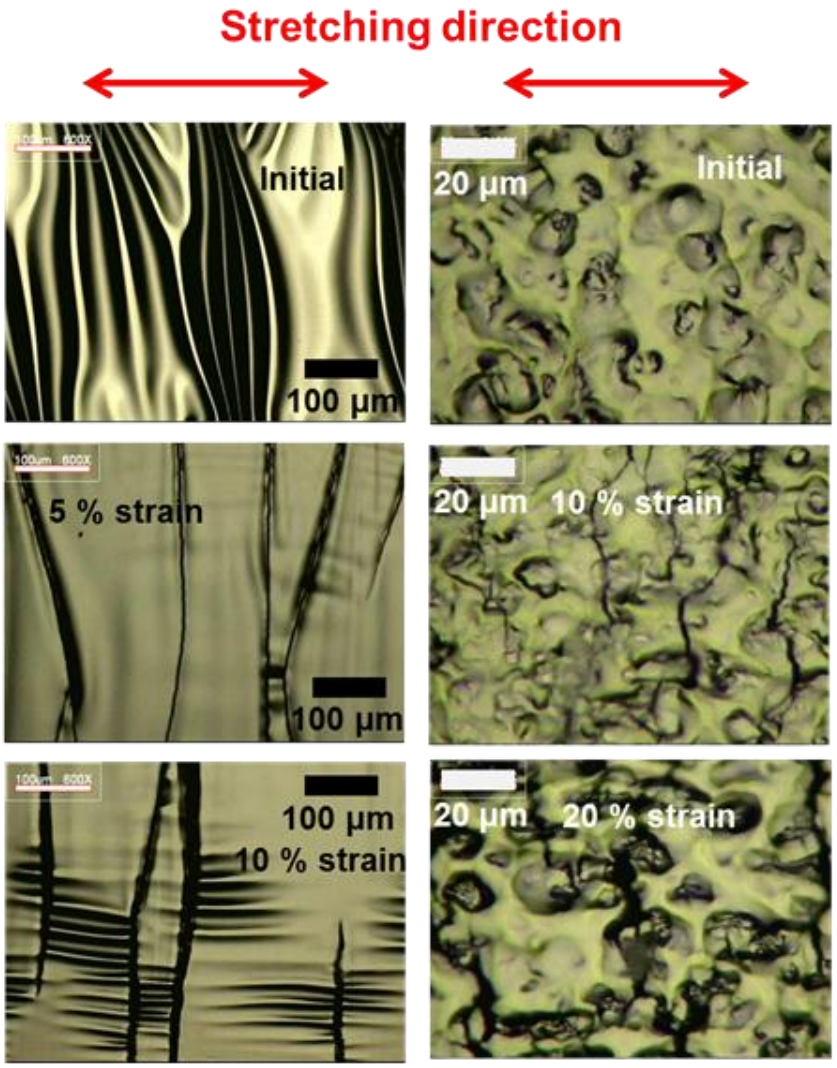
(b)

Figure 5.1 (a) Process flow of the inkjet-printed stretchable Ag electrode on wavy Elastomeric substrate. (b) optical top-view image for stretchable electrode with top-layer and stretching direction. (Pad size: 1 mm by 1mm, Line width : 1 mm)

For high conductive inkjet-printed silver electrode, nano particle type silver ink (DGP-40 from ANP Corp.) having silver content of 32 wt.% was used. Since silver

nano particle was dispersed in polar solvent (triethylene glycol monoethyl ether), adhesion property was very poor on the PDMS substrate which has strong hydrophobic property showing contact angle of 116 °, Which was measured by using a typical method with a sessile drop of deionized (DI) water. For better adhesion property, UV ozone surface treatment with 28 mW/cm^2 was performed for 20 minutes, resulting in surface energy increase, thus making PDMS surface more hydrophilic without any surface damage. Contact angle was decreased from 116 ° to 65 ° when measured using DI water. After surface treatment, silver ink was printed on the wave structured PDMS substrate maintained at 60 ℃ by using a piezoelectric (drop-on-demand) inkjet-printer (DMP-2831 from Dimatix corp.). Inkjetting conditions were carefully optimized to obtain well deposited silver electrodes by controlling a waveform voltage, a cartridge temperature (33 ℃), ink drop velocity (6~7 m/sec), and drop spacing considering silver ink characteristics. Especially, drop spacing of 20 μm was used to obtain uniform silver electrodes because each silver ink droplet forms a circle with 40 μm diameter when dropped on the UV ozone treated PDMS substrate. After inkjet-printing process, it was sintered on 100 ℃ hot-plate for 1 hour. 2-times-printed silver electrodes having width of 1 mm, length of 20 mm, effective length of 32 mm (when the wavy structure is considered), and thickness of 1.6 μm, show resistance of near 14 Ω that corresponds to sheet resistance of 0.44 Ω/□. On top of the printed Ag electrodes, top PDMS layer

was covered except for the contact pad area and the substrate was cured on 60 ℃ hot-plate for 24 hour in air (“wave structured PDMS with top layer”). We also fabricated reference inkjet-printed silver electrodes on three types PDMS substrate: PDMS without surface roughening and wavy structure (“bare PDMS”), PDMS with only surface roughening (“rough PDMS”) and roughened wave structured PDMS without top PDMS layer (“wave structured PDMS without top layer”). All three PDMS substrates were treated with UV ozone under the same conditions before printing Ag ink. Stretching test was performed by using a home-made automatic stretching equipment and electrical properties of the stretched electrodes were measured by using Keithely 2420 that is controlled by a computer. All measurements were performed in air. Figure 5.4 shows optical images of initial and laterally stretched inkjet-printed silver electrode on bare and rough PDMS substrates. The stretching direction is indicated with an arrow in Fig. 5.4. On bare PDMS substrate (Fig. 5.4 (a)), many wrinkles were observed in the initial state



(a) (b)

Figure 5.2 Optical images of initial and laterally stretched inkjet-printed silver electrodes on two types of substrate. (a) Bare PDMS (up: initial, middle: 5 %, down: 10 % tensile strain) , (b) Rough PDMS (up: initial, middle: 10 %, down: 20 % tensile strain).

because of poor adhesion property and mismatch of coefficient of thermal expansion (CTE) between silver electrode (1.8×10^{-5}/K) and PDMS substrate (3.1×10^{-4}/K) [16]. When lateral tensile stress was applied, the initial vertical wrinkles disappeared with the tensile strain and changed into several cracks. In addition, horizontal wrinkles were newly formed due to poor adhesion and Poisson contraction of the PDMS substrate [9], [17], [18]. When surface roughness and both surface roughness and wavy structures were introduced, adhesion and stretching performance were much improved. On rough PDMS substrate (Fig. 5.4 (b)), crack evolution with tensile strain is very similar to that of the evaporated silver electrodes [10]. We reported that surface roughness can improve stretching performance of the electrodes by releasing strain stress when the external stress was applied [10]. For the printed electrodes, surface roughness can also enhance adhesion with the substrate. If the structure of surface roughness is known for a surface with the static contact angle (θ) of 45° ~ 90°, it is possible to predict fluid spreading on the rough surface by using below equation [15].

$$\theta_C = \arctan\left(\frac{2\delta}{\lambda} + 1\right)$$

,where θc, δ, λ , are the critical contact angle, the height of peak and distance between the peak to peak of the surface roughness, respectively. If θ is smaller than

θ_c, the fluid will well spread. For rough PDMS substrate, δ and λ are in region of 2.5 ~ 4.5 μm and 9 ~ 15 μm, respectively, resulting in θ_c of 53.1 º ~ 63.4 º. Considering that average θ of silver ink on bare PDMS are 51.3 º and 67.0 from six samples before and after UV ozone treatment, respectively, our experimental results were consistent with the equation. In our case, surface roughness helps the silver ink well spread on the PDMS substrate and thus, produces better adhesion properties when UV ozone treatment was performed.

Figure 5.5 shows resistance changes of silver electrodes on the wave structured PDMS with top layer for applied 20% strain in 1 cycle with various strain stress speeds. Normalized resistance (R_{norm}) was defined as a ratio of resistance measured at a specific tensile strain to the initial resistance. Although R_{norm} increases with the strain stress speed, the printed Ag electrodes show good and stable stretching performance even at very fast strain speed (~1 mm/sec), having resistance change of less than two times of initial resistance under 20 % tensile strain stress. Optical images of the stretched line do not show much difference for both initial and 20 % tensile conditions. Figure 5.6 (a) shows comparison of R_{norm} variation for various PDMS substrates. R_{norm} was measured every 0.2 sec by applying the tensile strain with 16.7 μm/sec. As expected, Ag electrode on the wave structured PDMS with top layer shows the best stretching performance less than 3 times increase at 30 % strain stress because of both good adhesion property and releasing the tensile

strain stress. Moreover, by using top layer, peak and valley area were stretched evenly in contrast with wave structured PDMS without top layer which is stretched unevenly, leading to stress concentration in valley area and poorer stretching performance.

We also performed 1,000 times cycling test at high speeds of 1 mm/sec with 10 % tensile stress to verify the stability of the inkjet-printed silver electrodes for samples of the wave structured PDMS with top layer (Fig.5.6 (b)). Minimum R_{norm} measured when strain is released was little changed and the maximum R_{norm} measured when stretched gradually increased during the cycling test, resulting in lower than three after 1,000 cycles. It is noted that this stretching stress conditions are much harsher than those used in previously reported results [12], [19]-[20]. When the cycling test was performed at slow (66.7 μm/sec) speed, R_{norm} increased only up to 1.25 after 1,000 cycles. These results show similar stretching performance with the evaporated silver electrodes on the wave structured PDMS that was previously reported [9].

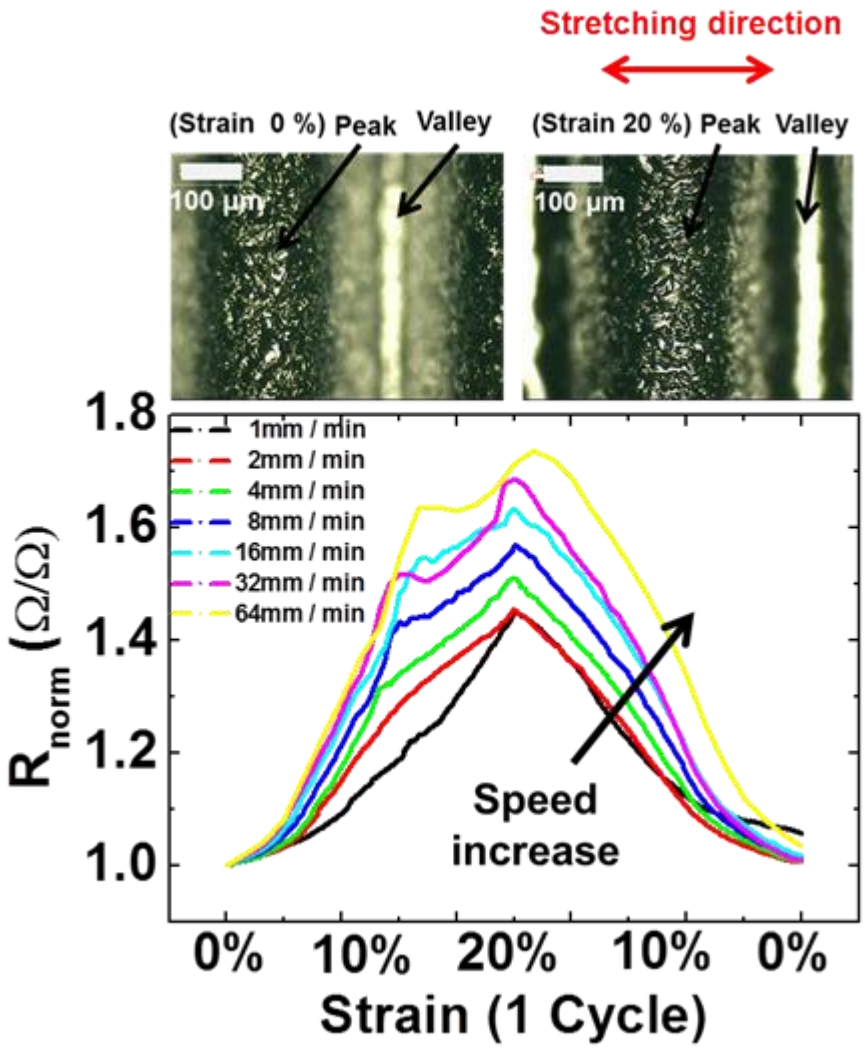
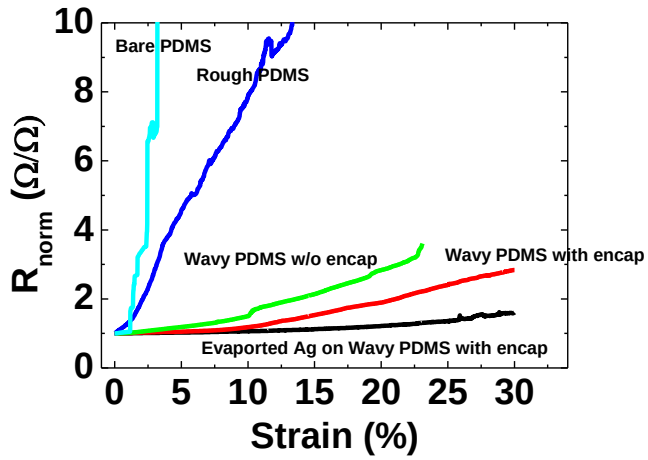
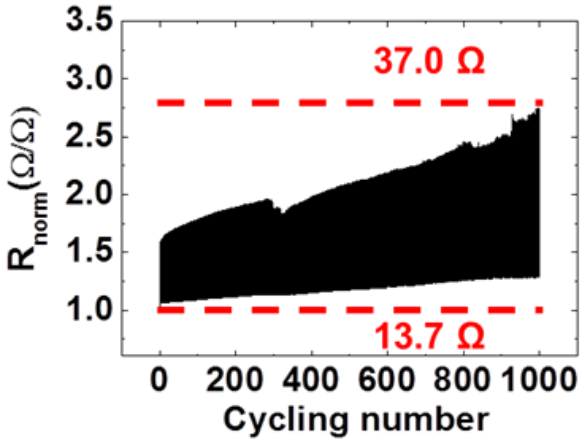


Figure 5.3 R_{norm} changes for wave structured PDMS with top layer sample under 20% strain cycle with various stretching speed from 1 mm/min to 64 mm/min



(a)



(b)

Figure 5.4 R_{norm} changes for (a) samples on various PDMS substrates for stretching speed of 1 mm/min (b) the wave structured PDMS with top layer sample under fast (60 mm/min) cycling strain stress.

5.3 Conclusion

In conclusion, first, high performance stretchable inkjet-printed Ag electrodes on surface treated wave structured PDMS substrates were successfully fabricated for highly stretchable TFT fabrication. UV ozone treatment and roughened surface improved adhesion between the printed ink and PDMS substrates, and the wavy structure provided good and stable stretching performance for the printed Ag electrodes. The inkjet-printed stretchable silver electrodes showed good stretchable performance at low-to-high speed strain stress and good stability in 1,000 times cycling test under fast strain stress.

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Chapter 6

Conclusion

In this these, we report the all-inkjet-printed OTFT and inverter fabrication on flexible plastics substrate. By optimizing inkjet-printing process including materials, sintering/curing temperature, surface energy, inkjetting conditions and waveform, high electrical performance OTFTs were demonstrated. To reduce the overlap capacitance and device dimension, all-inkjet-printed OTFTs array having narrow S/D electrode with short channel of 9 μm using 1 pl cartridge were also fabricated, and they also showed good electrical performance comparing with conventional inkjet-printed OTFTs and those using spin-coated method.

By using optimized OTFTs, we successfully demonstrated high performance TIPS-pentacene p-type OTFTs and inverter with good switching performance showing a gain of 7.8 at supply voltage of V_{DD}= -40 V on flexible substrate. For further electrical performance improvement, interdigitated S/D electrodes structure

and surface treatment on PVP gate dielectric and inkjet-printed Ag electrodes were adopted. After PS-brush surface treatment was performed between organic gate dielectric and semiconductor layers, OTFT performance was significantly improved by more than 3 times showing mobility of 0.15 cm^2/V.s, on/off ratio of 2×10^5 and threshold voltage of -1.98 V. The fabricated inverter with a drive OTFT having interdigitated S/D structure also had better electrical performance at various V_{DD} showing full up-down switching performance with a gain of -8.2 V/V at supply voltage of -20 V and a maximum gain as high as -20 V/V at supply voltage of -40 V. Moreover, even after 1000-time bending stress test, frequency response up to 50 kHz and an excellent stable performance.

For inkjet-printed OTFT fabrication, bottom-contact TFT structure is typically used because relatively high temperature sintering process is required for the printed S/D electrodes and ink solvent can damage bottom layer. From these reasons, their contact properties between S/D electrodes and active layer are poor comparing with those from top-contact structure and vacuum deposited TFT. Therefore, contact resistance between inkjet-printed Ag S/D electrodes and TIPS-pentacene active layer are also investigated by using all-solution-processed OTFTs with various channel length from 14 μm to 113 μm. To support our experiment results, contact properties between inkjet-printed Ag S/D electrode and evaporated pentacene active layer, evaporated Ag S/D electrode and TIPS-pentacene / evaporated pentacene active

layers, and evaporated gold S/D electrodes and evaporated pentacene active layer were also investigated. For further investigation, the potential drop analysis on channel and contact region by using SKPM analysis was performed. From SKPM measurement results, effective channel formation and potential drop on TIPS-pentacene crystalline boundary and S/D edge were observed. To reduce potentials drop which indicate contact resistance, PS-brush treatment was performed on inkjet-printed S/D electrodes. When PS-brush treatment was performed, we obtained not only well-deposited TIPS-pentacene active layer, but also improved contact properties, and their results were supported by XPS analysis.

We also reported high-performance inkjet-printed stretchable electrode fabrication. UV ozone treatment and roughened surface improved adhesion property between the printed Ag ink and PDMS substrates by controlling surface energy and fluid spreading, respectively, and the wavy structure provided good and stable stretching performance for the printed Ag electrodes. The inkjet-printed stretchable Ag electrodes showed good stretchable performance at low-to-high speed strain stress and good stability in 1,000 times cycling test under fast strain stress.

From these experiments, we believe that inkjet-printed electronics have great potential to substitute conventional photolithography patterning process in low-cost and environment friendly. Moreover, these researches can be adapted to inkjet-printed stretchable electronics in future.

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국문 초록

최근 유기박막트랜지스터를 잉크젯 프린팅 공정을 이용하여 대면적으로 저가격, 저온 공정으로 쉽고 친환경 적으로 제작할 수 있어 유연성 전자 소자 및 회로 응용에서 많은 관심을 받고 있다. 또한 유기 재료와 공정 조건의 최적화를 통해 그 성능 또한 향상 되고 잉크젯 프린팅 공정 또한 장비 개발을 통해 발전하고 있다. 잉크젯 프린팅 공정이 차세대 패터닝 공정으로 주목 받고 있고 그에 따라 많은 연구 그룹들이 소자의 구조 및 공정 조건 최적화를 위해 잉크젯 프린팅 공정이 가능한 유/무기 재료에 대해 연구를 진행하고 있지만, 노즐 막힘 현상, 물질과 해상도의 한계, 깨끗한 패터닝의 어려움, 그리고 필름의 균일성 등과 같은 공정상 어려움의 이유로 소스/드레인 전극 이나 반도체 층 형성에만 적용되고 있는 실정이다. 위와 같은 기술적 이슈 때문에 유연성 기판 위에 전 인쇄 공정으로 제작된 유기박막트랜지스터는 대부분 좋지 못한 성능과 높은 전압 동작을 보여주고 있다. 본 학위 논문에서는 이러한 문제점 해결 방안을 제시하고, 잉크젯 프린팅 공정으로 이용한 유연성 유기박막트랜지스터 및 회로 제작과 전기적 특성 향상을 위한 다양한 접근에 대해 논의한다.

첫 번째로 전 인쇄 공정으로 유연성 플라스틱 기판 위에 제작된 고 성능 유기막막트랜지스터 제작을 보고한다. 고 성능 소자 제작을 위해, 표면 에너지 최적화, 잉크 젯팅 조절, 열처리 과정, 속도, 점도, 표면 장력 등을 고려한 잉크

조건과 같은 프린팅 공정과 열 처리 조건에 대해 연구하였다. 위의 최적화 된 유기박막트랜지스터를 사용하여 유연성 플라스틱 위에 전 인쇄 공정으로 제작된 p-타입 인버터를 제작하였다. 이렇게 제작된 인버터는 표면처리 없이 소자 구조 및 공정 최적화를 통해 높은 전압이득을 가지는 좋은 전기적 특성을 보여주었지만, 더 향상된 전기적 특성을 얻기 위해 interdigitated 구조를 가지는 소스/드레인 전극 및 전열층과 유기 반도체층 사이에 표면 처리를 수행하였다. 좀 더 최적화 된 조건과 노력으로, 0.15 $cm^2/V.s$ 의 전하 이동도와 2×10^5 의 점멸비, 그리고 -1.98 V 의 문턱 전압을 가지는 드라이브 유기 박막 트랜지스터을 제작할 수 있었다. Interdigitated 구조를 가지는 소스/드레인 전극을 사용함으로써 -20 V 를 인가하였을 때 -8.2 V/V 의 전압 이득을 가지는 풀 스윙 스위칭 특성을 얻을 수 있었고 -40 V 를 가했을 때는 최고 -20 V/V 의 전압 이득을 얻을 수 있었다. 또한 10 mm/sec 의 속도와 5 mm 의구부림 직경 조건에서의 1000 번의 구부림 테스트 후에도 최대 50 kHz 의 주파수 응답과 -20 V 를 인가하였을 때 -5.5 V/V 의 전압 이득을 가지는 안정된 특성을 보여주고 있으며, 이러한 결과들은 현재까지 보고된 전 인쇄 공정으로 제작된 인버터 중 가장 좋은 특성을 보이고 있다. 또한 잉크젯 프린팅 공정으로 제작된 은 전극과 유기 반도체 간의 접촉 저항 또한 transmission line method (TLM) and scanning kelvin probe microscopy (SKPM) 을 통해 분석하였다. 14 에서 113 μm 의 다양한 채널 길이를 통해 용액 공정으로 제작된 TIPS-pentacene 층과 잉크젯 프린팅으로 제작된 은 전극과 진공 증착된 은 전극에 대해 각각 2.18 MΩ·cm 와 0.81 MΩ·cm 의 접촉 저항 값을 얻을 수 있었다.

이 결과를 뒷받침하기 위해서 진공 증착한 pentacene 층과 잉크젯 프린팅 공정으로 제작된 은 전극과 진공 증착으로 제작된 은 전극에 대해 각각 1.79 MΩ·cm, 0.55 MΩ·cm 의 접촉 저항 값 또한 얻을 수 있었다. 잉크젯 프린팅 공정으로 제작된 은 전극에서 더 높은 접촉 저항 값을 얻은 이유는 전극 가장자리에서의 상대적으로 좋지 못한 표면 특성이 작은 유기 반도체 결정을 유도하고, 소결 공정 중 산화된 은 전극 표면이 접촉 저항을 높인 다는 것으로 설명할 수 있다. 이러한 접촉 저항의 특성을 높이기 위해 표면 처리의 일환으로 polystyrene-brush 물질을 잉크젯 프린팅 공정으로 제작된 은 전극과 유기 반도체 사이에 처리함으로써 이 표면 처리층이 유기 박막트랜지스터의 특성을 높일 뿐 아니라 반도체 층과 금속층 간의 접촉 특성 또한 향상 시킬 수 있다는 것을 SKPM 분석 결과로 확인하였다.

추가적으로 인쇄 공정으로 제작된 신축성 박막 트랜지스터 제작을 위한 고성능 신축성 배선을 보고한다. UV-ozone 처리가 된 PDMS 기판 위에 전도성 높은 은 전극을 직접 프린팅 하였고, 잉크과 기판과의 접착성을 높이고 높은 전도성을 얻기 위해 표면 거칠기와 wavy 구조를 가지는 PDMS 기판을 사용하였다. 느린 신축성 테스트 동안 인쇄 공정으로 제작된 은 전극은 30 %의 스트레스 동안 저항이 단 3 배 증가 값을 보일 뿐 아니라 잉크젯 프린팅 공정으로 제작된 은 전극은 10%의 1000 번의 빠른 반복 스트레스 테스트에서도 저항 변화 3 배 이하의 좋은 기계적 특성을 보임을 확인하였다.

주요어: 잉크젯 프린팅, 유기 반도체, 박막 트랜지스터, 유연성 유기박막트랜지스터, 은 전극

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