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PH.D. DISSERTATION

A STUDY ON INTERFACE CIRCUITS
FOR CMOS-INTEGRABLE
BIO-CHEMICAL SENSORS

CMOS와 집적 가능한 생화학 센서를 위한
인터페이스 회로에 관한 연구

BY

HYUNJOONG LEE

AUGUST 2012

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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ABSTRACT

A STUDY ON INTERFACE CIRCUITS FOR CMOS-INTEGRABLE BIO-CHEMICAL SENSORS

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In this study, several methods were invented and verified by the silicon for the readout of CMOS-integrable bio-chemical sensors. These sensors are generally capacitive or resistive. In many cases, integrable capacitor-type sensors are in the form of micro-electro-mechanical system (MEMS) sensors and integrable resistor-type sensors are in the form of various nanowire sensors. To get benefit from high-density CMOS-integration and to characterize the sensing environment sufficiently, these sensors are made into array. For the detecting of signals from capacitor-type sensors, the scheme using charge amplifier has been invented and developed. For the detecting of signals from resistor-type sensors, schemes using current-mode detection have been invented and developed. In any type of sensors, schemes to extend dynamic range or methods to compensate for the variation of sensor's initial values in array structure are considered and developed.

In the first study for the readout of capacitive sensors, a low-complexity CMOS circuit for reading out monolithically integrated differential capacitive sensors has been proposed. It directly converts the differential capacitance of a MEMS sensing device to a frequency by accumulating the charges produced by repeated charge integration and charge conservation. A prototype chip was designed and fabricated in 0.35 μm CMOS technology. Experimental results show that differential capacitance is linearly converted to output frequency.

In the second study for the readout of capacitive sensors, a more accurate capacitance-to-frequency converter has been presented, which produces a single pulse stream in a wide range of frequencies. This circuit saves residual charges and accumulates them when discharging an integrator capacitor. Implemented in 0.35 μm CMOS technology, the proposed circuit improves the accuracy from about 6% to 0.13%.

In the third study for the readout of capacitive sensors, a low-complexity interface circuit for capacitive sensors has been presented which are integrated into sensor microsystems. To reduce hardware cost while keeping high resolution, a first-order delta-sigma modulator (DSM), which balances the charge from the capacitive difference between the sense and reference capacitors with the charge from a fixed-quantity capacitor, is employed. A charge-mode digital-to-analog converter and a successive approximation register are utilized to automatically calibrate the zero point of the interface circuit, which may shift further than a dynamic range. A prototype circuit fabricated in a 0.35 μm CMOS process. Its DSM operates at a sampling frequency of 1MS/s with an oversampling ratio of 128. This circuit can read a capacitive difference

from -0.5pF to +0.5pF with a 0.49fF resolution. Capacitive offset that causes the zero point to shift can be cancelled in the range from -2pF to +2pF with a 31.25fF resolution.

In the first study for the readout of resistive sensors, a sensor readout integrated circuit for the carbon nanotube (CNT) bio-sensor array has been presented. The heart of the proposed circuit is the low-power current-input continuous-time $\Delta\Sigma$ modulator that is capable of dynamic range extension. Experimental results show that the prototype chip, designed and fabricated in 0.18 μm CMOS process, achieves a dynamic range of 87.746dB and has a readout rate of 160kHz, which guarantees 1k sample/s per each sensor. It consumes 8.94 μW /cell considering the 16x10 sensors and its core area is 0.085mm².

In the second study for the readout of resistive sensors, a tin-oxide-decorated CNT network gas sensor system has been implemented on a single die. The deposition of metallic tin on the CNT networks, its subsequent oxidation in air, and the improvement of the lifetime of the sensors have also been shown. The fabricated array of CNT sensors contains 128 sensor cells for added redundancy and increased accuracy. The read-out integrated circuit (ROIC) combines coarse and fine time-to-digital converters to extend its resolution in a power-efficient way. The ROIC is fabricated using a 0.35 μm CMOS process, and the whole sensor system consumes 30mA at 5V. The sensor system was successfully tested in the detection of ammonia gas at elevated temperatures.

Keywords: interface circuit, CMOS, bio-chemical, capacitive, resistive, sensor.

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CHAPTER 1

INTRODUCTION

1.1 CMOS-INTEGRABLE BIO-CHEMICAL SENSORS

1.1.1 CAPACITIVE BIO-CHEMICAL SENSOR

Traditionally, capacitive sensors were utilized in many application fields such as pressure measurement, humidity measurement, and hazardous gas detection. In addition to these well-established applications, advances of various science fields have extended the applications of capacitive sensors.

For example, as a result of advances in the field of biochemistry for several decades, almost all areas of the life sciences became related to biochemistry. Many researches on this discipline require observations on bio-chemical reactions among bio-molecules, such as carbohydrates, lipids, proteins and nucleic acids. For instance, a specific biomolecular interaction such as DNA hybridization affects the change in stress on surfaces on which the bio-chemical event occurs. Observations on this kind of interactions often involve chemo-mechanical transduction.

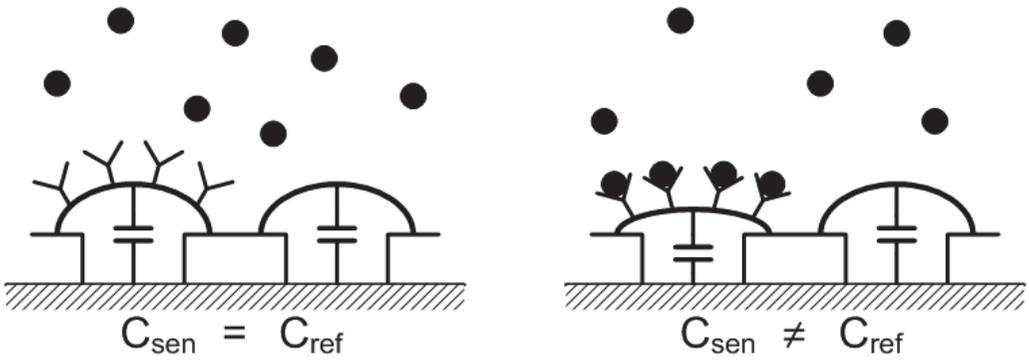


Fig. 1.1.1 Thin membrane transducer (TMT) [1.1.1].

Among several methods for this detection, recently developed thin membrane transducer (TMT) [1.1.1] provides the possibility of implementing a high-density and low-noise monitoring system, since the transducer is realized in micro-electro-mechanical system (MEMS), which can be compatible with mainstream semiconductor processes by integrating this transducer and the interface circuit monolithically into CMOS-based chip.

One set of TMTs can be seen as an electrically-modeled capacitive sensor, consisting of a reference capacitor C_R and a sense capacitor C_S as shown in Fig. 1.1.1. For the reference capacitor C_R , the surface of its capacitive membrane is not functionalized to accept any bio-molecules. Hence its capacitance is not directly related to bio-chemical reaction but related to any common mode signal generated by environmental fluctuations such as pressure variation, temperature variation, and flows or movements of the fluid, which can be a solution of bio-molecules. For the sense capacitor C_S , the surface is functionalized to accept specific bio-molecules, which generate pressure on the surface. This action deforms the sensing membrane and changes the capacitance of sense

capacitor. Now we can simply model both of the capacitances as below.

$$C_S = C_{S,DC} + \Delta C_{S,CM} + \Delta C_{S,BIO} \quad (1.1.1)$$

$$C_R = C_{R,DC} + \Delta C_{R,CM} \quad (1.1.2)$$

In the equation, subscript DC means that the value is an initial value of each capacitance, subscript CM indicates that the value is a common mode signal from environmental fluctuation, and subscript BIO means that the value is generated by any biomolecular reaction. Rejecting common mode signals by differential sensing gives the relation below:

$$\Delta C = C_S - C_R = (C_{S,DC} - C_{R,DC}) + \Delta C_{S,BIO}, \quad (1.1.3)$$

where $\Delta C_{S,CM} \approx \Delta C_{R,CM}$ and they are cancelled out since both membrane experiences almost same environmental fluctuations. $\Delta C_{S,BIO}$ is the value to be detected. One important point is that $C_{S,DC}$ and $C_{R,DC}$ are not perfectly cancelled out because of the deviation between both values caused by the accuracy of lithography technology and the functionalization of the sensing membrane. This value, $C_{S,DC} - C_{R,DC}$, is a DC offset and it is not a value of interest in general. Thus, it should be properly cancelled to prevent any loss in dynamic range of interface circuit.

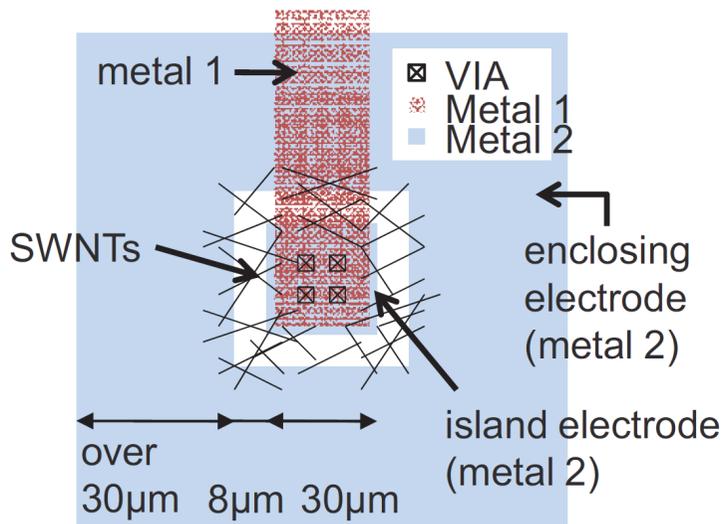


Fig. 1.1.2 CNT-based bio-chemical sensor node [1.1.5].

1.1.2 RESISTIVE BIO-CHEMICAL SENSOR

As noted in previous section, chemo-mechanical transduction can be a solution for observing biomolecular reaction and it can be detected by capacitive sensors. However, electro-chemical transduction can also be another solution for detecting biomolecular reaction.

Among several detection techniques of electro-chemical sensors, using conductometric devices composed of nanowires have rapidly become popular [1.1.2]-[1.1.4]. Specifically, devices based on carbon nanotube (CNT) are under active research since their fabrication method have become elaborate and diversified. A Result from

recent research demonstrated the feasibility for easy integration of CNT networks on pre-fabricated CMOS chip [1.1.5]. Along with the easiness of the fabrication, the electrical potential of the gate (which may be liquid) is nearly held to the potential of the enclosing electrode due to the larger electrical double layer capacitance between the gate and the enclosing electrode. This self-gating effect removes the need of additional reference electrode and eases the integration of sensor array onto CMOS chip [1.1.5].

The conductance of CNT-based electro-chemical sensor is modulated by electron donors or electron acceptors [1.1.4]. This property enables CNTs to be used as sensors for chemicals and bio-molecules. To enhance the understanding of conductance change in CNT-based sensors, the operating principle and the characteristics of the sensor are briefly described below.

As many previous researches revealed, there can be intrinsically metallic CNTs and semiconducting CNTs. For the semiconducting case, air-exposed pristine CNTs are known as hole-doped p-type semiconductors. This is because the CNT is naturally air-doped by oxygen in atmosphere, although the CNT itself is assumed to be n-type in vacuum [1.1.6]. Therefore, oxidizing molecule such as NO_2 increases the conductance of the CNT (decreases the resistance) and electron donating molecule such as NH_3 decreases the conductance of the CNT (increases the resistance). In detail, there exists binding affinity in NO_2 -CNT system hence the direct oxidizing mechanism works while there does not exist binding affinity in NH_3 -CNT system hence an indirect mechanism works in

NH₃ case. The possible mechanism is the interaction between NH₃ molecules and oxygen species which are pre-adsorbed on CNTs in air [1.1.7]. Along with these principles described above, CNTs' feature of being all surface reacting materials enables CNT-based sensors to work at room temperature. However, this type of sensor has problems of slow response-recovery time and low sensitivity when it is operated at room temperature. On the other hand, there already exist many semiconductor type sensors, such as SnO₂-based sensor which is n-type semiconductor. It shows good sensitivity and good response-recovery time, but it only works at elevated temperatures [1.1.8]. Therefore, several researches are conducted with the combination of SnO₂ and CNT to obtain good characteristics at room temperature [1.1.8]-[1.1.9].

For these SnO₂-CNT sensors, each research proposes their operating model. For the H₂ sensing, the conductance change depends on the surface coverage of the SnO₂ nanoparticles on the CNTs. Since the H₂ molecules interact with O⁻ adsorbates of SnO₂, exposing to H₂ increases the number of conducting electrons, large surface coverage of SnO₂ makes the whole sensor be n-type and small surface coverage of SnO₂ makes the sensor be p-type. In both cases, it is presumed that SnO₂ nanoparticles identify H₂, CNTs provide conducting path, and their cooperation allows detection at room temperature [1.1.9]. For the NH₃ sensing, similar mechanism on SnO₂ side and the cooperation of SnO₂ and CNT are speculated as H₂ case, along with the interaction between NH₃ and pre-adsorbed O₂ on CNT surface [1.1.8]. In this thesis, the differences of the characteristics between bare CNT-based NH₃ sensor and SnO₂-decorated CNT-based NH₃

sensor will be validated using the readout circuit proposed through the study.

Several additional studies on this CNT-based sensors revealed that each different application requires specific voltage across the CNT. For example, one research shows that a voltage below 1V is suitable for the detection of bio-molecules in a solution to prevent side-effects from the ionization of the buffer [1.1.10]. To fulfill this requirement, the interface circuit should be operated in a current-mode, which generates output current according to the variation of CNT's conductance with a pre-defined regulating voltage depending on each application.

1.1.3 REQUIREMENTS FOR HIGH-DENSITY INTEGRATION ON CMOS

Since the possibilities have been shown to integrate both capacitive bio-chemical sensors and resistive bio-chemical sensors with pre-fabricated CMOS chip, there should be some considerations for the requirements of integrated CMOS interface circuits. The main purpose of the integration is to make the whole sensor system compact and high-density. Thus the sensor structure should be in array format and the interface circuit should be compact enough while it should maintain appropriate resolution. In this study, several key approaches are considered to meet these requirements.

First, for the interface circuit to read capacitive output, approaches based on charge amplifier is proposed and developed. Particularly, repetitive charge integration is used to make the circuit compact, considering its relatively low operation speed. For further enhancement in resolution, residual charge is reused in successive study.

Second, for both the capacitive and resistive readout, the concept of delta-sigma modulation is used. Low order and high oversampling ratio (OSR) structure is easily adoptable with modest target resolution and slow operation speed.

Third, schemes to extend dynamic range or methods to compensate for the variation of sensor's initial values in array structure are considered and developed. An array format

is frequently used in sensor applications, because of its relative robustness against undesirable effects such as process variation and environmental noise. However, the distribution of the initial values for each sensor elements is inherently spread widely. For the capacitive sensor array using TMTs, the DC offset between C_S and C_R may vary from cell to cell. For the resistive sensor array using CNT networks, the conductance of each CNT networks may also vary. For this kind of bio-chemical applications, a circuit with a high signal-to-noise ratio (SNR) which also has a wide DR is too complicated and wasteful in power and area.

1.2 THESIS ORGANIZATION

The organization of this thesis consists of 2 main chapters, which describe interface circuits proposed through the study for capacitive bio-chemical sensors and resistive bio-chemical sensors. Each of subchapters in two main chapters is already published in journal paper or conference proceeding [1.2.1]-[1.2.5] in the course of the consecutive study for this thesis. In chapter 2, three consecutive methods [1.2.1]-[1.2.3] are proposed for the readout of capacitive sensors. In chapter 3, two consecutive methods [1.2.4]-[1.2.5] are proposed for the readout of resistive sensors. Finally, conclusions and summary of this dissertation are presented in chapter 4.

CHAPTER 2

INTERFACE CIRCUITS FOR CAPACITIVE BIO-CHEMICAL SENSORS

2.1 A CMOS DIFFERENTIAL-CAPACITANCE-TO-FREQUENCY CONVERTER UTILIZING REPETITIVE CHARGE INTEGRATION AND CHARGE CONSERVATION[†]

2.1.1 INTRODUCTION

Capacitive sensors are regularly employed in a wide variety of mechanical and chemical applications including pressure sensing, fingerprint recognition, hazardous gas detection, and the monitoring of biomolecular reactions. These sensors can be implemented within micro-electro-mechanical systems (MEMS), so as to achieve a higher density of devices and better compatibility with the complementary metal-oxide-

[†]This sub chapter is published in *IEE Electronics Letters* [1.2.1]. The author of the thesis is first author of the published paper.

semiconductor (CMOS) process [2.1.1]. Several methods of reading out capacitive sensors [2.1.2] have already been published, in which capacitance-to-voltage conversion is followed by voltage-to-digital conversion using a delta-sigma oversampling analog-to-digital (A/D) converter. But these circuits are relatively large and complicated. One of the alternative candidate circuits that offer the possibility of meeting this requirement is the capacitance-to-frequency converter (CFC) [2.1.3]. It produces a digitized output signal without requiring the complexity of an A/D converter, and thus reduces the hardware cost. In this study, a further simplified CFC circuit is proposed in which the capacitance-to-voltage conversion (CVC) and voltage-to-frequency conversion (VFC) stages are merged into a single direct CFC that only requires a single op amp in its core. The operations needed for the proposed circuit can be implemented with concise components since the circuit only converts the difference between two capacitances into an output frequency, without measuring their full values. The circuit is able to detect small changes in this differential capacitance, and hence in the quantity being measured by the sensor. The sign of this differential capacitance, indicating which of the two capacitances being compared is the larger, is also reported.

2.1.2 CIRCUIT DESIGN

A schematic drawing and timing diagram of the proposed CFC circuit core are shown in Fig. 2.1.1. The reference capacitor C_{REF} and the sensing capacitor C_{SEN} are

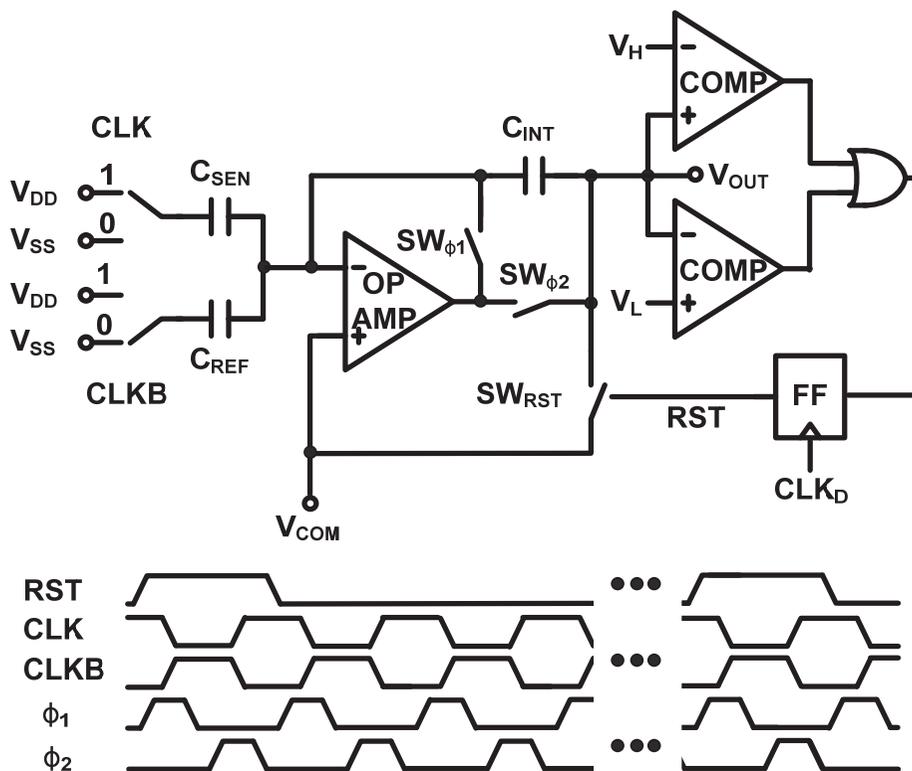


Fig. 2.1.1 Schematic and timing diagram of the proposed CFC.

connected to the negative input of the op-amp, and driven by the differential charge-pumping clocks CLK and $CLKB$. The presence of $SW_{\phi1}$ makes the circuit around the op-amp unity gain, maintaining the bottom electrodes of C_{REF} and C_{SEN} at the common voltage level V_{COM} . $SW_{\phi2}$ creates an integrator which transfers charge to the integrating capacitor C_{INT} . The circuit operates in three phases as follows:

- (1) Reset phase: At the beginning of a new cycle, $SW_{\phi1}$ and SW_{RST} are switched on to discharge C_{INT} completely. Now the output voltage V_{OUT} can go up or down depending on

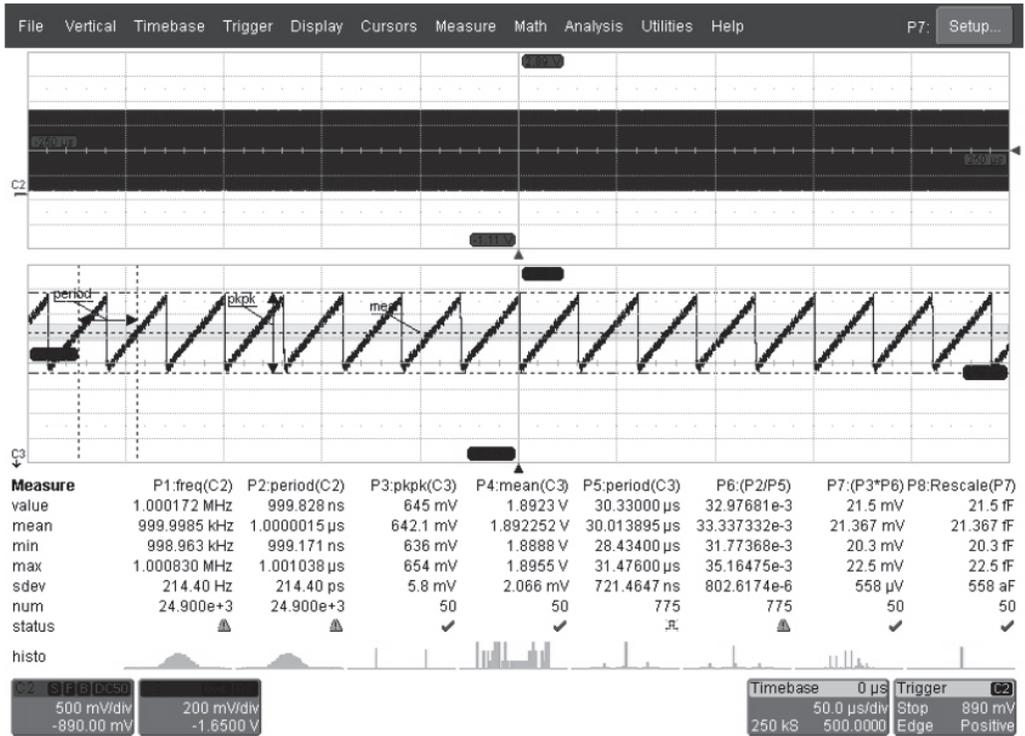


Fig. 2.1.2 V_{OUT} measured at $\Delta C = +7.5fF$.

the sign of the differential capacitance.

(2) Pump-In phase: $SW_{\theta 2}$ is turned on and CLK goes up while CLKB goes down. In this phase, charge corresponding to the difference between C_{REF} and C_{SEN} is transferred and then integrated by C_{INT} . The extent of the change in V_{OUT} during this phase can be expressed as follows:

$$\Delta V_{OUT} = \frac{(C_{SEN} - C_{REF})V_{DD}}{C_{INT}} = \frac{\Delta C V_{DD}}{C_{INT}} \quad (2.1.1)$$

(3) Toggle phase: $SW_{\theta 1}$ is turned on and CLK goes down while CLKB goes up. C_{INT} is

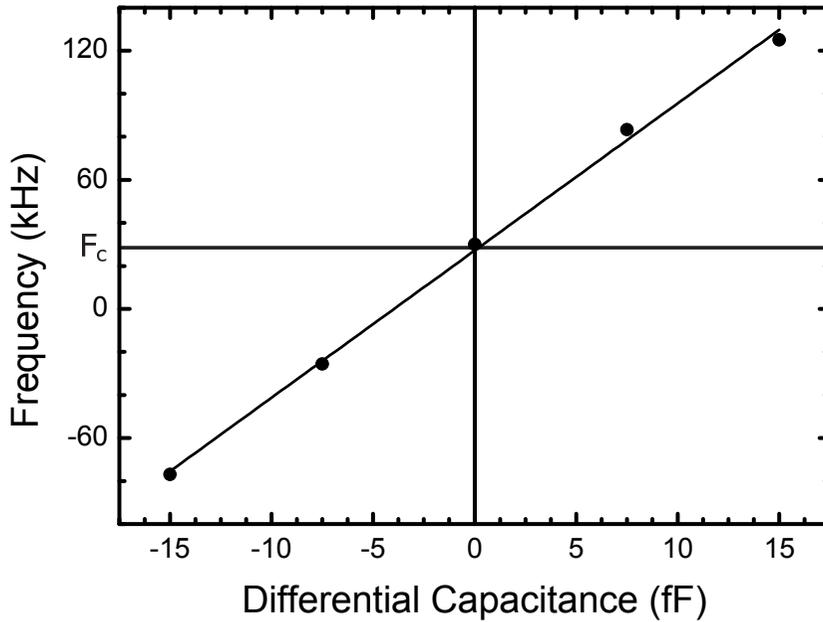


Fig. 2.1.3 Measured output frequencies under the varied differential capacitance ΔC , which ranges from -15fF to $+15\text{fF}$.

disconnected from the output, and thus the charge stored in C_{INT} is conserved.

Pump-In and Toggle phases are repeated until V_{OUT} reaches a predefined upper threshold V_{H} or lower threshold V_{L} . At this point, the cycle is complete and a new cycle starts from Reset phase. In this manner, the differential capacitance can be amplified while noise is averaged out.

The differential capacitance is measured by comparing the frequency f_{OUT} of the triangular waveform generated by the CFC with the frequency of a reference clock as

follows:

$$\Delta C = C_{INT} \times \frac{\sum_{k=1}^n \Delta V_{OUT}}{V_{DD}} \times n = C_{INT} \times \frac{V_{REF} - V_{COM}}{V_{DD}} \times \frac{f_{OUT}}{f_{CLK}} \quad (2.1.2)$$

where n is the number of clock cycles that pass during one cycle of the CFC. V_{REF} can be the upper threshold V_H or the lower threshold V_L , depending on the sign of the differential capacitance. The frequency of the RST pulse f_{RST} is the same as that of the triangular waveform produced by the CFC, allowing f_{RST} to be used as the 1-bit output pulse stream of the CFC.

Although the readout time depends on the capacitive difference in this scheme, the overall readout speed of the circuit is dependent on the size of the integration capacitor. Larger C_{INT} with fixed reference voltages, fixed supply voltage, and fixed clock frequency leads to slower readout speed. But in this case, the noise will be further averaged out. When C_{INT} is decreased, opposite result for the speed and the noise holds. If the clock speed is increased, the readout speed will be increased not at the cost of increased noise but at the cost of increased power consumption.

Later in the case that an array of sensing capacitors is provided, the proposed circuit can easily be extended like below without any significant modification. Each sensing capacitor is directly attached in parallel to the node where single sensing capacitor C_{SEN} was attached to. At the opposite node of each sensing capacitor, same clocking switch is

connected in series. Sensing specific cell is easily done by toggling only one switch connected to the selected cell. The other switches are not toggled hence unselected cells do not influence the operation of the circuit.

2.1.3 PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

To demonstrate the feasibility of the proposed scheme, a prototype chip was designed and fabricated in 0.35 μm CMOS technology with a 3.3V supply. A MEMS capacitive sensing device is monolithically integrated with the proposed CMOS CFC circuit. The MEMS device was processed after CMOS process is completed.

Experimental results show that the integrated CFC circuit and MEMS capacitive sensing device operates at clock frequency of 1MHz and consumes 660 μA at that speed. Fig. 2.1.2 shows the values of V_{OUT} produced by the converter circuit when measuring +7.5fF of differential capacitance. Fig. 2.1.3 shows an excellent linearity, with a conversion gain of 6.8376kHz/fF and a center frequency of 27.148kHz. Measurement outputs with negative signs are written as negative frequencies for convenience. Fig. 2.1.4 shows a microphotograph of the CFC circuit monolithically integrated with a differential MEMS capacitive sensing device on a single die.

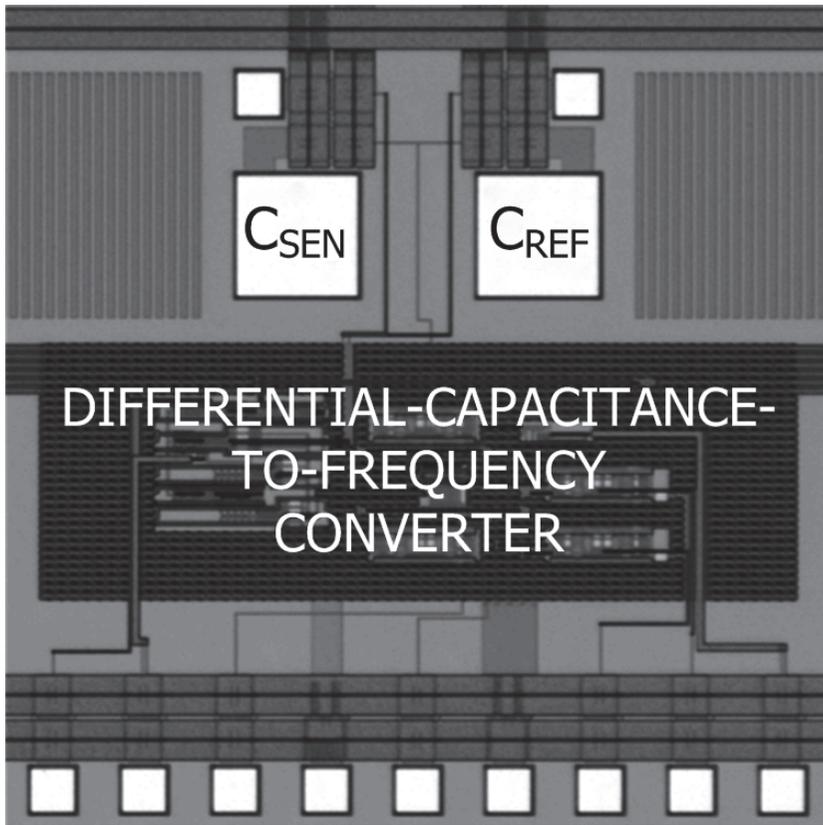


Fig. 2.1.4 Die microphotograph of the CFC monolithically integrated with differential capacitive sensing structure.

2.2 IMPROVING THE ACCURACY OF CAPACITANCE-TO-FREQUENCY CONVERTER BY ACCUMULATING RESIDUAL CHARGES[†]

2.2.1 INTRODUCTION

Producing and measuring a capacitive difference is a fundamental method of sensing which has many applications such as pressure and humidity measurements, and hazardous gas detection. The same technique can also be used in a microelectromechanical system (MEMS) to monitor various concurrent biomolecular reactions which change the stress on the surface of a mechanical element and thus the capacitance of a sense capacitor [2.2.1], [2.2.2]. By integrating readout circuits into the MEMS monolithically and having them handle a group of capacitive sensors, a high-density and low-noise monitoring system is attainable. In this system, an array of capacitive sensors is divided into multiple groups so that the sensors in a group may share a common reference capacitor. Furthermore, the sensor array elements in a group can be accessed by a single readout circuit, and the area cost of the system can be reduced. In this case, the corresponding output rate is approximately divided by the number of array elements due to time multiplexing and additional switches.

[†]This sub chapter is published in *IEEE Transactions on Instrumentation and Measurement* [1.2.2]. The paper is the result of collaborative work and the author of the thesis is second author of the published paper. Including the paper in this thesis was agreed by first author (Dong-Yong Shin) and corresponding author (Suhwan Kim) of the original paper.

Several circuits to read out the capacitive difference have already been published, which consist of a capacitance-to-voltage converter and an analog-to-digital converter (ADC) [2.2.3]–[2.2.6]. However, this form of circuit is too large and complicated to be integrated in such a high-density sensor system described above. An alternative candidate is the capacitance-to-frequency converter (CFC) proposed by Chiang *et al.*, which produces a single pulse stream and thus enables simple communication with the outside [2.2.7]. Although it produces a pulse stream without requiring the complexity of an ADC, the hardware cost can be reduced further by merging a capacitance-to-voltage converter (CVC) and a voltage-to-frequency converter (VFC) into a direct CFC that only requires a single op amp in its core, as proposed by Lee *et al.* [2.2.8]. However, the CFC due to Lee *et al.* suffers from nonlinearity that causes poor accuracy at higher frequencies. Chiang *et al.* addressed this nonlinearity by adding an automatic compensation circuit which observes an integrator output and controls a counter operating at a frequency 4 times higher than the operating clock frequency. Their compensation circuit was able to achieve an accuracy of about 5% at the cost of a circuit area comparable to the CFC. In this study, a compact direct CFC is presented in which accuracy is enhanced by utilizing the residual charges at the end of each output cycle instead of allowing them to drain away. Additionally, the dynamic frequency range of the CFC has been widened to match the operating clock frequency. This circuit can measure both large and small difference in capacitance, and hence in the quantity being sensed, with higher accuracy than previous circuits of this type.

2.2.2 PROPOSED CAPACITANCE-TO-FREQUENCY CONVERTER

2.2.2.1 Circuit Operation

Fig. 2.2.1 shows a schematic diagram of the proposed CFC, which converts the difference in capacitance between a sense capacitor C_S and a reference capacitor C_R into the output frequency f_{OUT} of an output pulse stream. The op amp OP and switched capacitors in Fig. 2.2.1(a) constitute an integrator that produces a staircase signal at V_{int} during low MAG. The height of each step in this signal is proportional to the capacitive difference, and is negative if C_S is smaller than C_R . When the staircase signal reaches a predetermined level V_{refp} or V_{refn} , one of comparators COMP1 or COMP2 produces a high level and the MAG signal goes high and passes a delayed version of Φ_3 to the output. Therefore, the output frequency f_{OUT} of the high-level pulse stream is also proportional to the difference between C_S and C_R , and can be as high as the frequency of the operating clock CLK. If C_S is larger than C_R , then the staircase signal approaches V_{refp} with a positive step and COMP1 determines the value of MAG, but COMP2 determines it if C_S is smaller than C_R . The direction of the difference between C_S and C_R is reported by SIGN or SIGNb. Waveforms from the simulated operation of the CFC are shown in Fig. 2.2.2.

In the earlier CFCs, integrator capacitor C_I is fully discharged when MAG becomes high; and then it is charged during the subsequent integrating operations until MAG

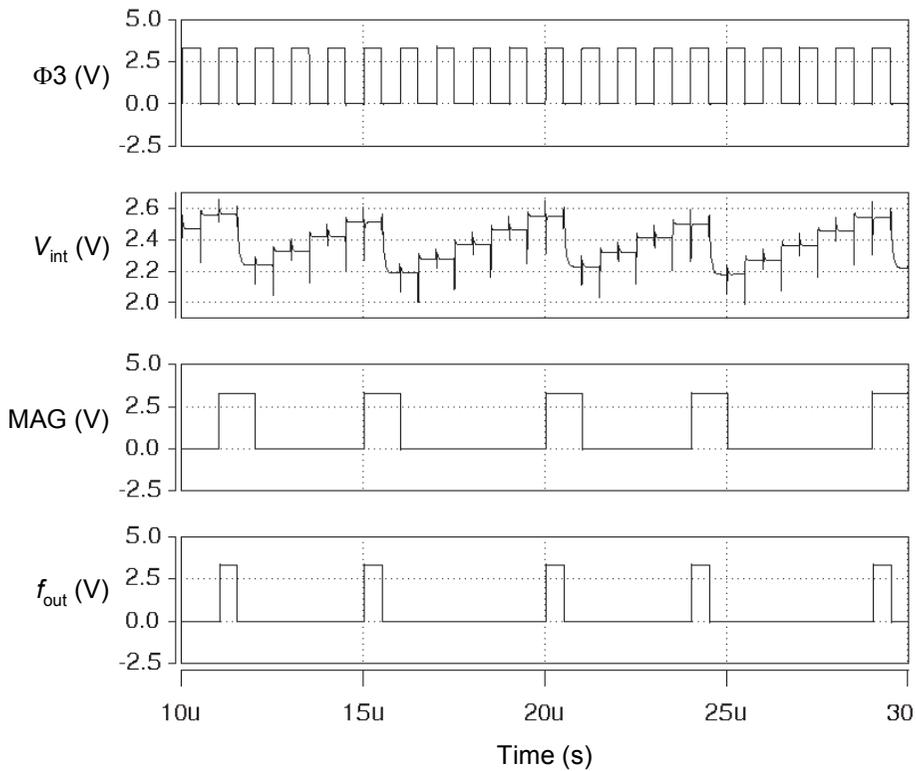


Fig. 2.2.2 Simulated waveforms from the proposed CFC. After Φ_3 changes, there are spikes on V_{int} and on the negative-input voltage of OP. They reflect the feedback operation of OP which makes its two input voltages meet. Outputs of COMP1 and COMP2 are sampled by rising Φ_3 before the spikes occur and change those outputs.

becomes high again [2.2.7], [2.2.8]. This is how the output frequency f_{OUT} is made to reflect the difference between C_S and C_R . However, some of the charge integrated into C_I , called the residual charge, is also discharged. Its magnitude is proportional to the voltage by which V_{int} exceeds a predetermined level, and thus reflects the difference between C_S and C_R . If these residual charges are saved in successive discharging steps, they are also integrated over multiple charging-and-discharging cycles. If these residual charges have significant magnitude, then accounting for them clearly improves the accuracy of the

CFC. The proposed CFC, shown in Fig. 2.2.1, utilizes a constant-quantity capacitor C_Q to discharge C_I by a constant amount and saves the residual charge.

Four signals $\Phi 1\sim\Phi 4$ are internally generated from a single clock CLK and used for controlling charge transfer through the switches. The signals $\Phi 1$ and $\Phi 2$ are non-overlapping clocks, and $\Phi 3$ is a delayed version of $\Phi 1$. According to these signals, the integrator operates in two steps as follows:

(i) Charge set: When $\Phi 3$ is high, the output of OP is directly connected to the negative input of OP by high $\Phi 1$. Therefore, OP supplies charge when C_S and C_R are respectively charged to $V_{\text{sen}} - (V_{\text{com}} + V_{\text{OS}})$ and $V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})$. V_{OS} is the input offset voltage of OP.

(ii) Charge transfer: Since $\Phi 1$ goes low before $\Phi 3$, the negative input of OP is floated before the capacitors are switched. This ensures charge conservation at that input when C_S and C_R are respectively charged to $V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})$ and $V_{\text{ref}} - (V_{\text{com}} + V_{\text{OS}})$ by low $\Phi 3$. At this time, the output of OP is connected to the negative input through C_I by high $\Phi 2$, and extra charges at C_S and C_R are transferred to C_I . Since the capacitors C_S and C_R are switched in the opposite direction, the charges transferred to C_I are proportional to the difference in capacitance.

When MAG is high, C_Q is also involved in the two-step operation. If MAGp is high, the law of charge conservation gives

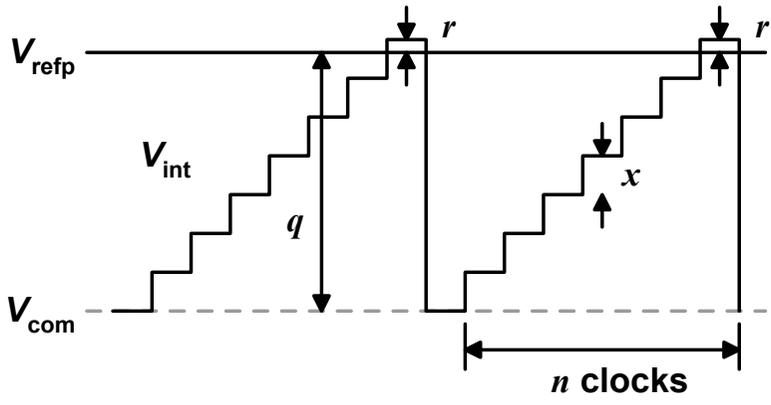
$$\begin{aligned}
& C_S [V_{\text{sen}} - (V_{\text{com}} + V_{\text{OS}})] + C_R [V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})] \\
& \quad + C_I [V_{\text{int1}} - (V_{\text{com}} + V_{\text{OS}})] + C_Q [V_{\text{com}} - (V_{\text{com}} + V_{\text{OS}})] \\
& = C_S [V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})] + C_R [V_{\text{ref}} - (V_{\text{com}} + V_{\text{OS}})] \\
& \quad + C_I [V_{\text{int2}} - (V_{\text{com}} + V_{\text{OS}})] + C_Q [V_{\text{refp}}' - (V_{\text{com}} + V_{\text{OS}})]
\end{aligned} \tag{2.2.1}$$

where V_{int1} and V_{int2} are respectively V_{int} before and after charge transfer. Thus, it can be obtained that

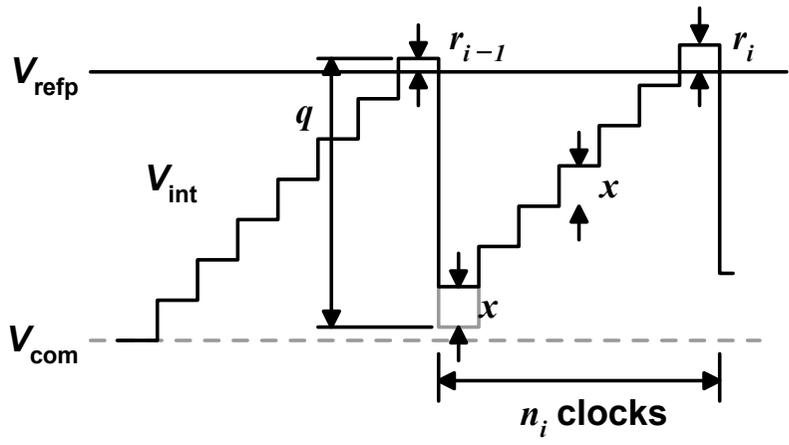
$$V_{\text{int2}} - V_{\text{int1}} = \frac{C_S}{C_I} V_S - \frac{C_R}{C_I} V_R - \frac{C_Q}{C_I} V_Q' \tag{2.2.2}$$

where $V_S = V_{\text{sen}} - V_{\text{SS}}$, $V_R = V_{\text{ref}} - V_{\text{SS}}$, and $V_Q' = V_{\text{refp}}' - V_{\text{com}}$. By setting V_S and V_R to the same value, the capacitive difference can be processed with the CFC. When MAG is low, C_Q stays connected to the supply voltage and the ground through parasitic capacitors of MOS switches without being involved in the two-step operation, and V_Q' in Eq. (2.2.2) reduces to zero. Eq. (2.2.2) shows that the operation of the integrator is not affected by V_{OS} . The switches are implemented as a CMOS switch which has an nMOS and a pMOS of the same size and does not cause severe charge injection [2.2.9]–[2.2.11].

In this scheme, the trend of the overall readout speed and the noise performance is the same as the previously proposed scheme in section 2.1. However the relative noise performance is enhanced compared to the previous scheme without any significant cost, due to accumulating residual charges. For the array extension, same method can be applied as the previously proposed scheme.



(a)



(b)

Fig. 2.2.3 Integrator operation and error calculation: (a) previous method and (b) proposed method.

2.2.2.2 Mathematical Analysis

For simplicity, only the situation is considered in which C_S is larger than C_R . However, a similar treatment applies when C_S is smaller than C_R . Fig. 2.2.3 illustrates two

input signals of a comparator COMP1, which are a staircase signal at V_{int} and a constant voltage of V_{refp} . If the same discharging method was used as previous circuits [2.2.7], [2.2.8], the staircase signal would exhibit the following relationship, as shown in Fig.2.2.3(a):

$$q = nx - r \quad (2.2.3)$$

where $q = V_Q = V_{\text{refp}} - V_{\text{com}}$, $x = (C_S V_S - C_R V_R)/C_I$, and $0 \leq r < x$. Therefore, the actual value to be measured is

$$\frac{x}{q} = \frac{C_S V_S - C_R V_R}{C_I V_Q} = \frac{1 + \frac{r}{q}}{n} \quad (2.2.4)$$

When an error of r/q is allowed, the value measured by the CFC is

$$\frac{\hat{x}}{q} = \frac{1}{n} = \frac{1}{1 + \frac{r}{q}} \cdot \frac{x}{q} \quad (2.2.5)$$

for the output frequency:

$$f = \frac{1}{n} f_{\text{op}} \quad (2.2.6)$$

Because n is a positive integer, the measured value \hat{x} is less than or equal to q ; and the accuracy is limited if n is near 1.

However, when the proposed method is applied, the following equation is obtained from the staircase signal shown in Fig. 2.2.3(b):

$$q - r_{i-1} = n_i x - r_i \quad (2.2.7)$$

where $q = C_Q V_Q' / C_L$, $x = (C_S V_S - C_R V_R) / C_L$, and $0 \leq r_i < x$ for a non-negative integer i .

After m iterations, it can be obtained that

$$\frac{x}{q} = \frac{C_S V_S - C_R V_R}{C_Q V_Q'} = \frac{1 + \frac{r_m - r_0}{mq}}{n_{\text{eq}}} \quad (2.2.8)$$

where

$$n_{\text{eq}} = \frac{n_1 + n_2 + \cdots + n_m}{m} \quad (2.2.9)$$

and n_{eq} is equivalent to n of Eq. (2.2.4). The value measured by the CFC is now

$$\frac{\hat{x}_{\text{eq}}}{q} = \frac{1}{n_{\text{eq}}} = \frac{1}{1 + \frac{r_m - r_0}{mq}} \cdot \frac{x}{q} \quad (2.2.10)$$

And the error is $(r_m - r_0) / mq$, for the output frequency:

$$f_{\text{eq}} = \frac{1}{n_{\text{eq}}} f_{\text{op}} \quad (2.2.11)$$

where $0 \leq f_{\text{eq}} < f_{\text{op}}$. This output frequency f_{eq} is a harmonic mean of the frequencies, each of which corresponds to n_i of Eq. (2.2.7). From Eqs. (2.2.5) and (2.2.10), the extent to which the proposed method enhances accuracy can be expressed with the following factor:

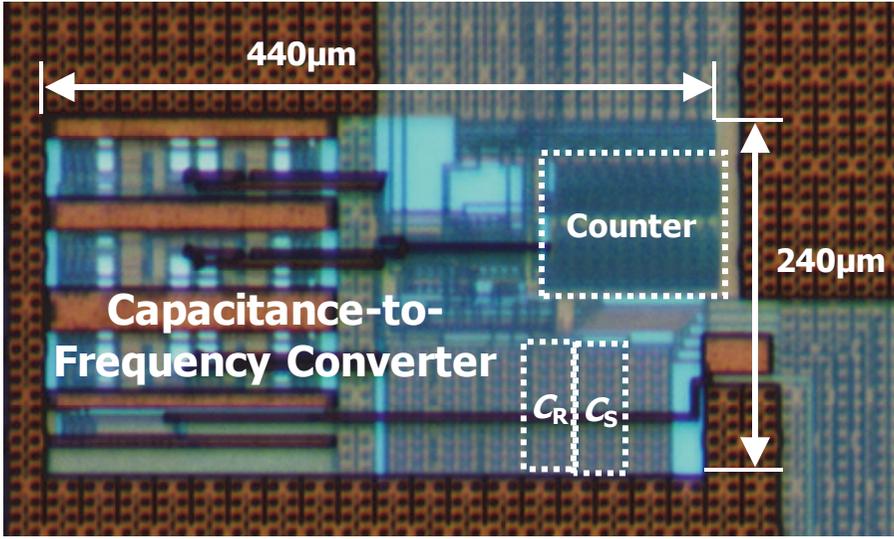


Fig. 2.2.4 Microphotograph of the proposed CFC equipped with a 10-bit counter.

$$\eta = \frac{\hat{x} - x}{\hat{x}_{\text{eq}} - x} = \frac{\frac{mr}{r_m - r_0} + \frac{r}{q}}{1 + \frac{r}{q}} > \frac{mr}{2(r_m - r_0)} \quad (2.2.12)$$

where $0 \leq r, r_0, r_m < x$. If it is assumed that $r_0 = 0$ and $r_m = r$, then Eq. (2.2.12) reduces to $\eta > m/2$. For the proposed method, m should not be less than 2, and therefore η is always larger than 1. If m is 1, this method reduces to the previous method. When the output is observed over some fixed time interval N , a smaller n yields a larger m , which improves the accuracy at higher frequencies. To detect a small x , N should be large, and this limits the dynamic response of a measurement system employing a CFC. Eq. (2.2.7) also shows that q is not affected by the input offset voltage of COMP1, which is not the case in previous circuits.

If the compensation technique due to Chiang *et al.* were to be applied to the proposed CFC over the complete range of the output frequency, n in Eqs. (2.2.3) to (2.2.6) would be replaced by $n + k/4$, where k is a non-negative integer that is less than 4. Eq. (2.2.12) would still be valid, even though r is less than $x/4$. Their technique changes the output frequency for smaller n by means of an additional fast clock, with a frequency 4 times higher than that of the operating clock, and requires analog-to-digital conversion and therefore, the circuit is complicated [2.2.7].

2.2.3 EXPERIMENTAL RESULTS

The proposed CFC has been designed and fabricated in a 0.35 μm double-poly four-metal (2P4M) CMOS process. It occupies only 240 \times 440 μm^2 , as shown in Fig. 2.2.4, including the capacitors C_S and C_R of 2pF for experimental purposes. And its op amp is designed in a two-stage folded cascode structure to achieve a gain of 77dB over a bandwidth of 18MHz at the cost of 0.5mW.

The circuit performance is summarized in Table 2.2.1. Eqs. (2.2.4) and (2.2.8) show that the CFC measures a charge difference in a ratio to a constant charge. Therefore, the CFC can be used in two modes: to measure a difference in capacitance, when V_S , V_R and V_Q are constant; or a difference in voltage, when C_S , C_R and C_Q are constant. The characteristics of the CFC are assessed in voltage measurement mode with V_R set to 1.65V. During

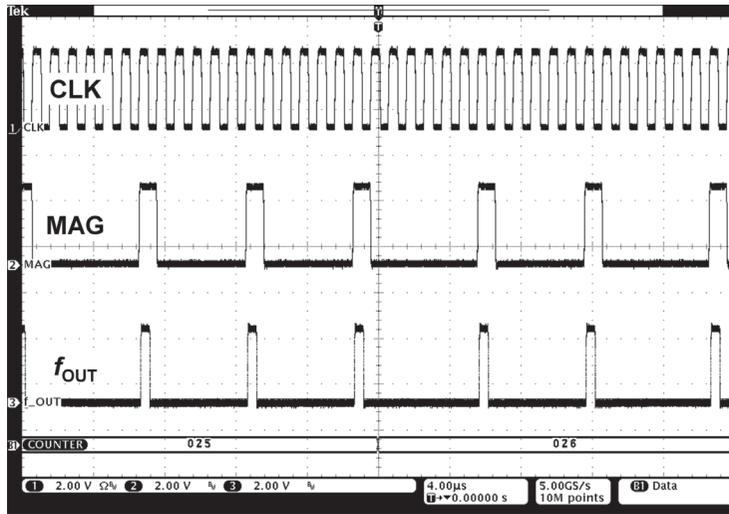
Table 2.2.1 Performance Summary of the Capacitance-to-Frequency Converter.

	[7]	This work
Technology	0.35 μ m 2P4M CMOS	0.35 μ m 2P4M CMOS
Power supply	3.2V	3.3V
Operating clock	2MHz	1MHz
Input capacitance	4-24pF	1.5-2.5pF ^a
Output frequency	0.5-500kHz	0-1MHz
Accuracy	\pm 5.14%	\pm 0.13%
Physical area	1.015mm ²	0.056mm ²

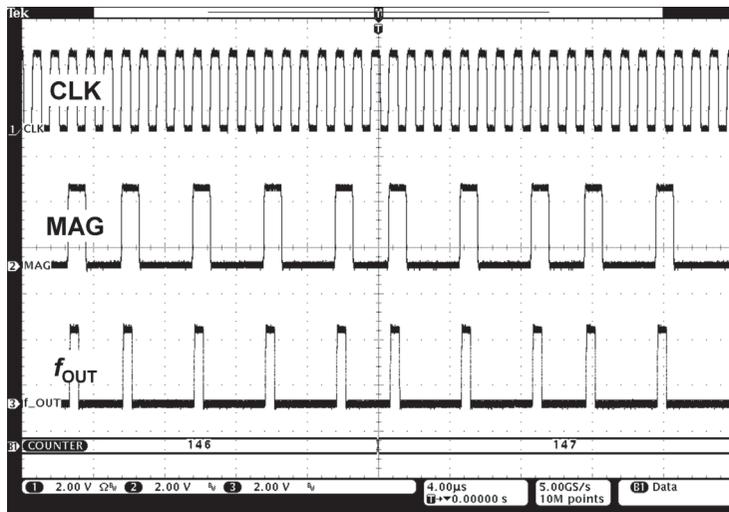
^a This value is estimated from using the relative deviation of voltage-mode measurements.

measurement, no specific technique was applied to protect the circuit from external electromagnetic interference. In that condition, a difference between V_S and V_R as small as 2mV, which corresponds to 2.4fF, could be measured with an accuracy of 1.2mV.

Pictures of the oscilloscope display during measurement are shown in Fig. 2.2.5, and measured output frequencies of the CFC are summarized in Fig. 2.2.6 with reference to the relative deviation of V_S from V_R . For example, measured outputs shown in Figs. 2.2.5(a) and 2.2.5(b) are when V_S are 1.7V and 1.4V which correspond to relative deviations of 0.03 and -0.15 in Fig. 2.2.6, respectively. These output frequencies were measured by using a 10-bit counter, operating at the same clock frequency as the CFC. The counter counts the number of clock cycles when MAG is high and thus a high-level pulse is seen at the output. When estimated for a given number of cycles, the output of the counter corresponds to $1/n_{eq}$ in Eq. (2.2.11).



(a)



(b)

Fig. 2.2.5 Oscilloscope display (a) V_S of 1.7V and (b) that of 1.4V.

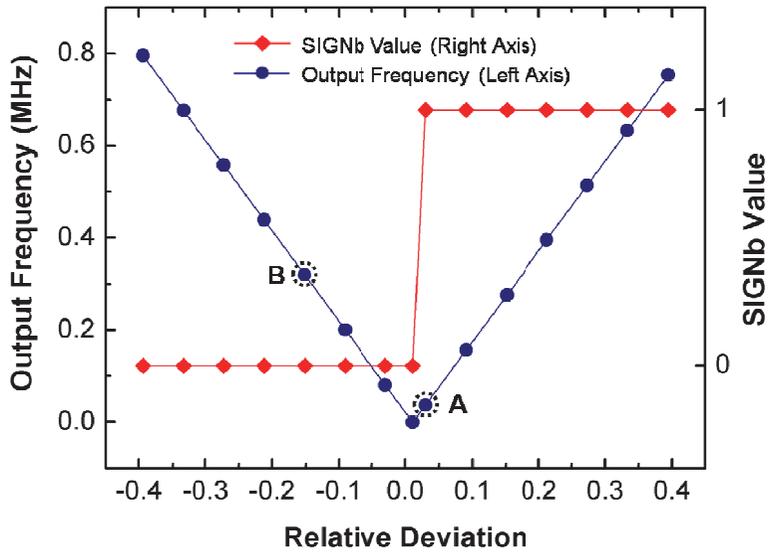


Fig. 2.2.6 Measured output frequency vs. relative deviation for the CFC. (A: Fig. 2.2.5(a), B: Fig. 2.2.5(b))

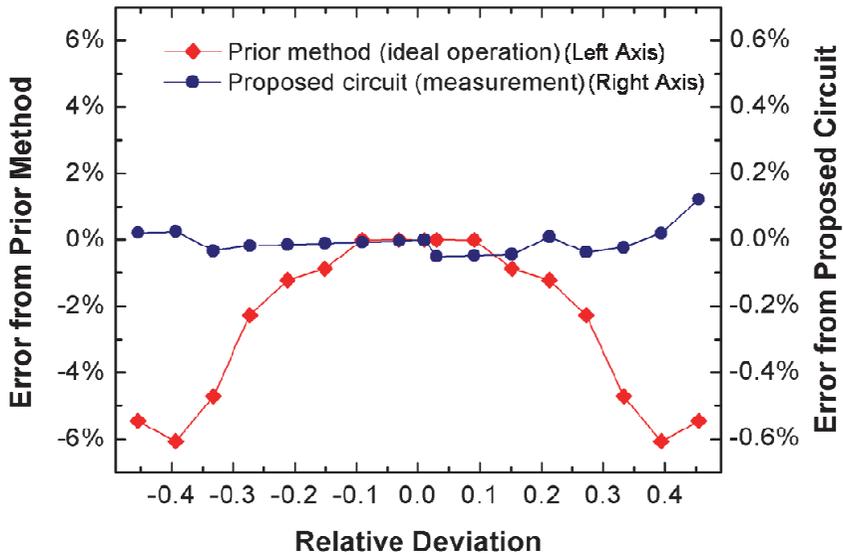


Fig. 2.2.7 Comparison between the simulated error of the prior compensation technique under ideal operating conditions and the experimentally measured error of the proposed circuit.

The sensing accuracy has been highly enhanced by the proposed CFC, as seen in Fig. 2.2.7. In this graph, errors are obtained for each measured point as the deviation of the measured output frequency from the expected output frequency. The errors are given in ratios to V_R , and worst-case errors of both prior and proposed methods correspond to accuracies in Table 2.2.1. When estimating errors from the prior compensation technique [2.2.7], a behavioral model was applied and the following relationship was obtained assuming ideal operation of circuit components: if

$$\frac{1}{a + \frac{b+1}{4}} < \frac{x}{q} < \frac{1}{a + \frac{b}{4}} \quad (2.2.13)$$

for non-negative integers a and b , then,

$$\frac{\hat{x}}{q} = \frac{1}{a + \frac{b+1}{4}} = \left\lceil \frac{4}{4 \cdot \frac{q}{x}} \right\rceil \quad (2.2.14)$$

when Eqs. (2.2.4) and (2.2.5) are referred to. The offset between C_S and C_R and that of C_Q were measured using Eq. (2.2.8), and their effect has been cancelled in Fig. 2.2.7.

2.3 A DELTA-SIGMA INTERFACE CIRCUIT FOR CAPACITIVE SENSORS WITH AN AUTOMATICALLY CALIBRATED ZERO POINT[†]

2.3.1 INTRODUCTION

Capacitive sensors, consisting of a reference capacitor C_R and a sense capacitor C_S , are adopted in many recent studies on a sensor microsystem. Reading a capacitive difference is the fundamental job of an interface circuit for such capacitive sensors. Several circuits to read out the capacitive difference have already been published, which include a capacitance-to-voltage converter and a delta-sigma modulator (DSM) for converting an analog voltage to a digital code [2.3.1], [2.3.2]. These circuits are complicated and large in area, and thus increase hardware cost when incorporated in a monolithic sensor microsystem.

Interface circuits that utilize delta-sigma modulation and directly convert a capacitance to a digital code [2.3.3]–[2.3.5] are a promising alternative. They utilize a switched-capacitor technique which balances the signal charge from C_S with the reference

[†]This sub chapter is published in *IEEE Transactions on Circuit and System-II* [1.2.3]. The paper is the result of collaborative work and the author of the thesis is second author of the published paper. Including the paper in this thesis was agreed by first author (Dong-Yong Shin) and corresponding author (Suhwan Kim) of the original paper.

charge from C_R using an integrating capacitor C_I , on which the average charge is zero. However, if a capacitive difference that is tiny compared to C_R is to be read, this technique requires a high-order DSM which increases the hardware cost. In most of applications, the capacitive difference varies usually in a small range compared to C_R . Therefore, if the charge from the difference between C_S and C_R is processed, this charge can be balanced with the charge from a fixed-quantity capacitor C_Q that is smaller than C_R . Such modification allows a first-order DSM to read a tiny difference that it could not read before.

Decreasing the magnitude of a balancing capacitor, however, disables the DSM to handle a large shift of the zero point in a way of subtracting it from digital codes: the zero point corresponds to a capacitive difference from no stimulus. In many practical situations, the capacitive offset which causes the zero point to shift is larger than a dynamic range of the capacitive difference. A shift of this magnitude can be cancelled by adding or subtracting a calibrated charge with additional capacitors during readout operation [2.3.3], [2.3.4]. However, whenever a capacitive sensor is placed in a new environment, or a specimen on the sensor is replaced by another, the zero point has to be recalibrated. This requires additional circuitry outside the interface circuit or user intervention. To provide a handy and compact solution to this problem, a successive-approximation register (SAR) and a charge-mode digital-to-analog converter (DAC) have been introduced into the interface circuit. Together with the op amp of the integrator in the DSM, the SAR and charge-mode DAC perform as a successive-approximation

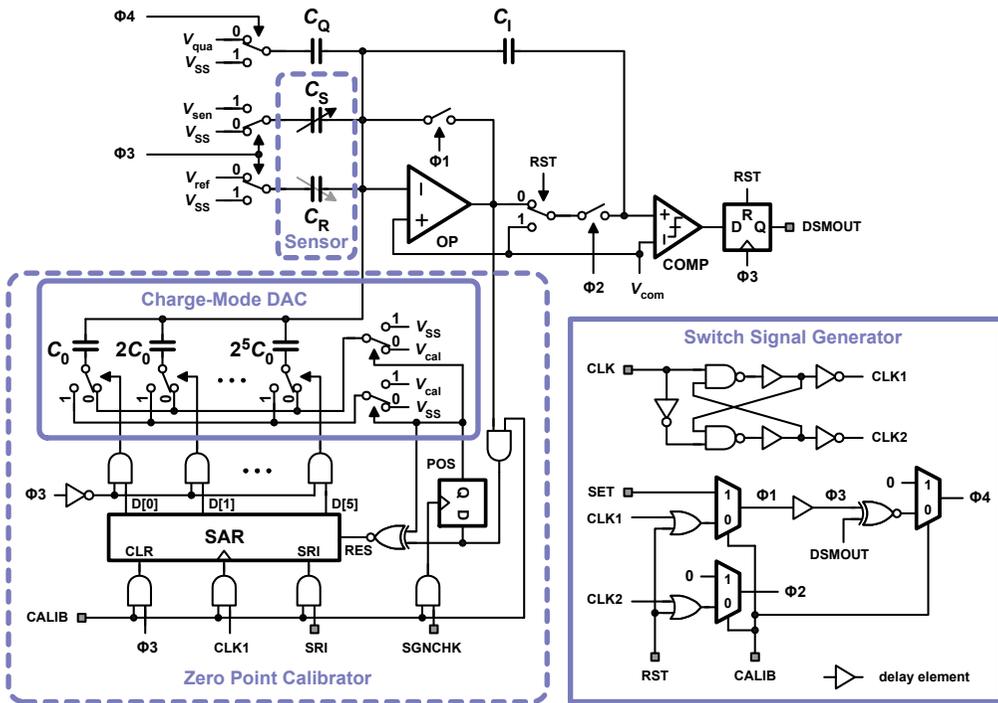


Fig. 2.3.1 Schematic diagram of the proposed delta-sigma interface circuit.

capacitance-to-digital converter (SAR-CDC) during calibration mode. This SAR-CDC measures the capacitive difference between C_S and C_R . Then, in readout mode, the charge-mode DAC adds or subtracts a calibrated amount of charge. Switching between the two modes can be simply achieved by controlling two digital signals. In this study, an interface circuit is presented which is designed for use in a wide variety of mechanical and chemical applications [2.3.6]. This circuit employs a first-order DSM and a zero-point calibrator, and monitors a sub-femtofarad change in capacitive difference at time intervals of sub-millisecond.

2.3.2 PROPOSED INTERFACE CIRCUIT FOR CAPACITIVE SENSORS

2.3.2.1 Delta-Sigma Interface Circuit

A schematic diagram of the interface circuit is shown in Fig. 2.3.1. The capacitive sensor under measurement also takes a part of a DSM so that the charge from $C_S - C_R$ is directly integrated at C_1 . All the capacitors including C_S , C_R , C_1 , C_Q , and the capacitors in the charge-mode DAC share a common electrode at the negative input of the op amp OP.

During readout, the zero-point calibrator is disabled by low CALIB: the SAR in the calibrator is reset to all zero by high CALIB and Φ_3 before measurement, and thus Φ_3 clock of the charge-mode DAC is masked out. Φ_1 and Φ_2 are respectively connected to the outputs CLK1 and CLK2 of the non-overlapping clock generator. Φ_3 is a delayed version of Φ_1 , and Φ_4 is the XNOR of Φ_3 and DSMOUT.

If Φ_1 or Φ_2 is high, the output of OP is fed back to the common electrode by direct connection or through C_1 . Thus, the common electrode is set to $V_{\text{com}} + V_{\text{OS}}$ by the feedback operation of OP, where V_{OS} means the input offset voltage of OP. When Φ_1 and Φ_3 are high, C_S and C_R are respectively charged to $V_{\text{sen}} - (V_{\text{com}} + V_{\text{OS}})$ and $V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})$ with reference to the common electrode. Then, they are respectively discharged to $V_{\text{SS}} - (V_{\text{com}} + V_{\text{OS}})$ and $V_{\text{ref}} - (V_{\text{com}} + V_{\text{OS}})$ when Φ_2 is high and Φ_3 is low. Because the

common electrode is floated during the discharging operation, the charges $-C_S (V_{\text{sen}} - V_{\text{SS}})$ and $-C_R (V_{\text{SS}} - V_{\text{ref}})$, which are taken off C_S and C_R , are transferred to C_I . Therefore, if the charge from C_Q is ignored, the integrator output increases by $[C_S (V_{\text{sen}} - V_{\text{SS}}) - C_R (V_{\text{ref}} - V_{\text{SS}})] / C_I$ regardless of the input offset voltage V_{OS} . When V_{sen} is set equal to V_{ref} , this integrator processes $C_S - C_R$. As a result, an autozero technique is used to cancel V_{OS} , which samples V_{OS} with C_S , C_R and C_Q , and also reduces $1/f$ noise at low frequencies [2.3.7].

The comparator COMP compares the integrator output with V_{com} , and the result is sampled by a D flip-flop (FF). Because the integrator output is initially set to V_{com} by RST, the output of the D FF, which is DSMOUT, indicates whether C_I is more positively or negatively charged than it was initially. If DSMOUT is low, C_Q is switched in the same direction as C_S , and therefore αC_Q is subtracted from C_R , where α is $(V_{\text{qua}} - V_{\text{SS}}) / (V_{\text{ref}} - V_{\text{SS}})$. Otherwise, C_Q is switched in the same direction as C_R , and αC_Q is added to C_R . Because the charge from C_Q is added or subtracted in this way, the charge from $C_S - C_R$ is balanced with that from C_Q regardless of its polarity. The number of low or high values at DSMOUT respectively corresponds to the number of $-\alpha C_Q$ or $+\alpha C_Q$ values, required for balancing $C_S - C_R$. Therefore, $C_S - C_R$ can be expressed as follows:

$$N_0 (C_S - C_R + \alpha C_Q) + N_1 (C_S - C_R - \alpha C_Q) = 0 \quad (2.3.1)$$

and thus

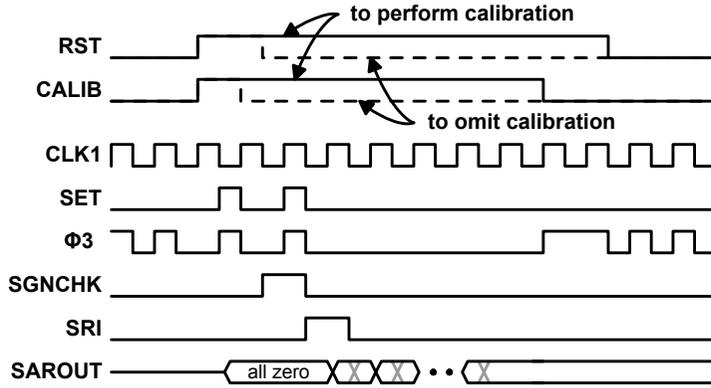


Fig. 2.3.2 Timing diagram of the zero-point calibrator.

$$C_S - C_R = \alpha C_Q (N_1 - N_0) / (N_1 + N_0), \quad (2.3.2)$$

where N_0 and N_1 respectively are the number of low and high values. This equation shows that the DSM can read a capacitive difference from $-\alpha C_Q$ to $+\alpha C_Q$. Provided that αC_Q is larger than the maximum magnitude of $C_S - C_R$, a smaller αC_Q allows a smaller capacitive difference to be read, for an integer ratio $(N_1 - N_0) / (N_1 + N_0)$ with the same precision.

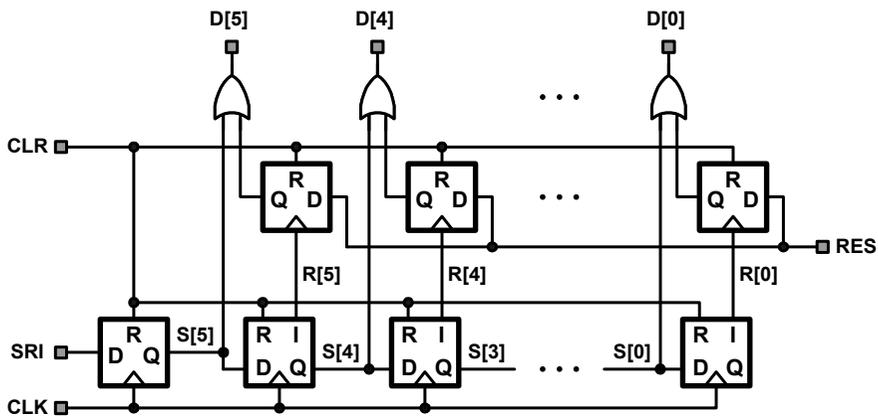
Compared to previously proposed two schemes in this thesis, the readout time does not depend on the capacitive difference since the output data DSMOUT is decimated by back-end counter with fixed number of bits. With this simple decimator, the number of clock cycles allowed to the counter corresponds to the oversampling ratio (OSR) of the circuit. Due to the nature of delta-sigma modulation, the readout speed and the noise performance is in trade-off relationship. For the array extension, same method can be applied as previously proposed schemes.

2.3.2.2 Automatic Calibration of the Zero Point

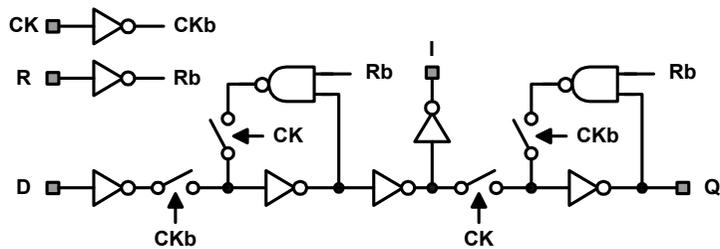
The offset or initial value of $C_S - C_R$ is cancelled by the capacitors in the charge-mode DAC during readout mode. However, a combination of those capacitors is determined by successive approximation during calibration mode, and stored in the SAR. The timing diagram of the calibrator is shown in Fig. 2.3.2. Note that calibration mode can be omitted by controlling CALIB and RST appropriately.

During calibration, $\Phi 2$ and $\Phi 4$ are set to low by high CALIB while $\Phi 1$ is connected to SET. Hence, COMP is disconnected from OP, C_Q is not switched, and C_1 is serially connected to the parasitic capacitance at the positive input of COMP.

When SET is high, the common electrode is driven at $V_{\text{com}} + V_{\text{OS}}$ by OP. Therefore, C_S and C_R are respectively charged with $C_S (V_{\text{sen}} - V_{\text{com}} - V_{\text{OS}})$ and $C_R (V_{\text{SS}} - V_{\text{com}} - V_{\text{OS}})$ when $\Phi 3$ is also high. At the same time, the SAR is reset to all zero. When SET is low, the common electrode is floated. Then, the electrodes of C_S and C_R that are on the other side of the common electrode are respectively switched to V_{SS} and V_{ref} by low $\Phi 3$. However, the charge-mode DAC remains still. If the common electrode were kept at $V_{\text{com}} + V_{\text{OS}}$, then C_S and C_R would be charged with $C_S (V_{\text{SS}} - V_{\text{com}} - V_{\text{OS}})$ and $C_R (V_{\text{ref}} - V_{\text{com}} - V_{\text{OS}})$, and charges of $-C_S (V_{\text{sen}} - V_{\text{SS}})$ and $-C_R (V_{\text{SS}} - V_{\text{ref}})$ might remain at the common electrode. These extra charges are redistributed over the capacitors that share the common electrode. If the total capacitance of those capacitors is C_{tot} , then the voltage V_- of the common electrode can be expressed as follows:



(a)



(b)

Fig. 2.3.3 (a) SAR and (b) its D flip-flop with an intermediate signal output.

$$V_- = [C_R (V_{ref} - V_{SS}) - C_S (V_{sen} - V_{SS})] / C_{tot} + (V_{com} + V_{OS}). \quad (2.3.3)$$

When V_{sen} is set equal to V_{ref} , OP tells the polarity of $C_S - C_R$ regardless of its input offset voltage: if $C_S - C_R$ is positive, OP produces a high level.

By using the first SET pulse, the polarity of $C_S - C_R$ is stored as POS at a D FF controlled by SGNCHK. This sets the direction in which the capacitors in the charge-

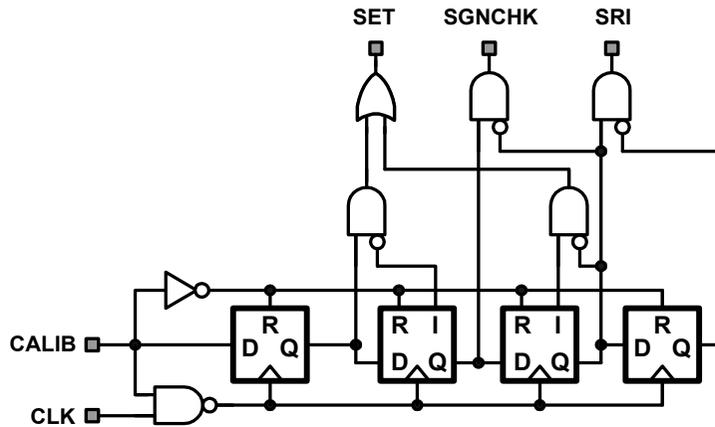


Fig. 2.3.4 Circuit to generate input signals of the calibrator.

mode DAC are switched by the SAR. They are switched in the same direction as C_R if POS is high; or switched oppositely if otherwise. Therefore, the values of those capacitors are added to or subtracted from C_R , after multiplication by $(V_{cal} - V_{SS}) / (V_{ref} - V_{SS})$.

After the second SET pulse, the extra charge at the common electrode is measured by cancelling it successively with the DAC capacitors. When an SRI pulse is input, the SAR, which is shown in Fig. 2.3.3, switches D[5] to high at the first rising edge of CLK1, and updates D[5] with the value of RES at the next falling edge. This operation is subsequently performed on D[4] to D[0]. If OP indicates a polarity change after cancellation, RES is set to low by an XNOR. Otherwise, RES is set to high.

It should be noted that the SAR switches in the opposite direction of Φ_3 during cancellation. Therefore, the capacitors chosen by the SAR are switched by an inverted

version of Φ_3 during readout mode. As described above, the calibrator requires the additional signals SET, SGNCHK, and SRI besides CALIB, but they can be generated by a simple circuit, as shown in Fig. 2.3.4. With the D flip-flop shown in Fig. 2.3.3(b), signals without glitches can be obtained.

2.3.3 EXPERIMENTAL RESULTS

A prototype circuit was designed in a $0.35\mu\text{m}$ double-poly four-metal (2P4M) CMOS process. In this design, C_Q , C_I and C_0 in Fig. 2.3.1 are sized at 0.5pF, 2pF, and 31.25fF respectively. Since this circuit processes charges from capacitors, its performance can be fully investigated by measuring voltage signals, instead of measuring capacitance changes. For this purpose, C_S and C_R of 2pF were also integrated in the circuit. However, the signal-generation circuit shown in Fig. 2.3.4 has been omitted, to avoid restricting the timing conditions during the experiment. The circuit has an active circuit area of 0.048mm^2 , and Fig. 2.3.5 is a photograph of it.

The DSM operates at a sampling frequency of 1MS/s with an OSR of 128. In the experiments, V_{ref} , V_{qua} and V_{cal} were set to half the value of V_{DD} , and a signal was applied to V_{sen} . Then the interface circuit measured $V_{\text{sen}} - V_{\text{ref}}$. The output characteristics of the interface circuit are shown in Fig. 2.3.6. Relative differences were estimated by dividing the difference by $V_{\text{ref}} - V_{\text{SS}}$, where V_{SS} is grounded. The DSM outputs were decimated

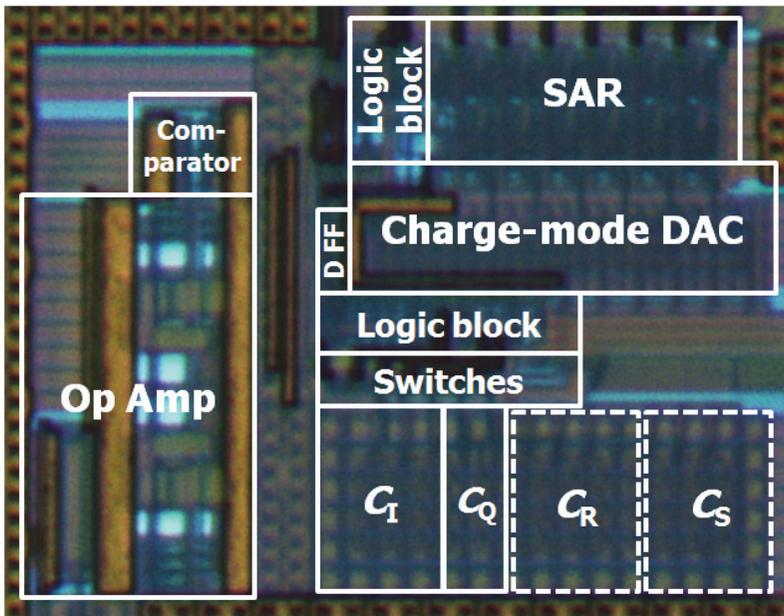


Fig. 2.3.5 Die photograph of the delta-sigma interface circuit.

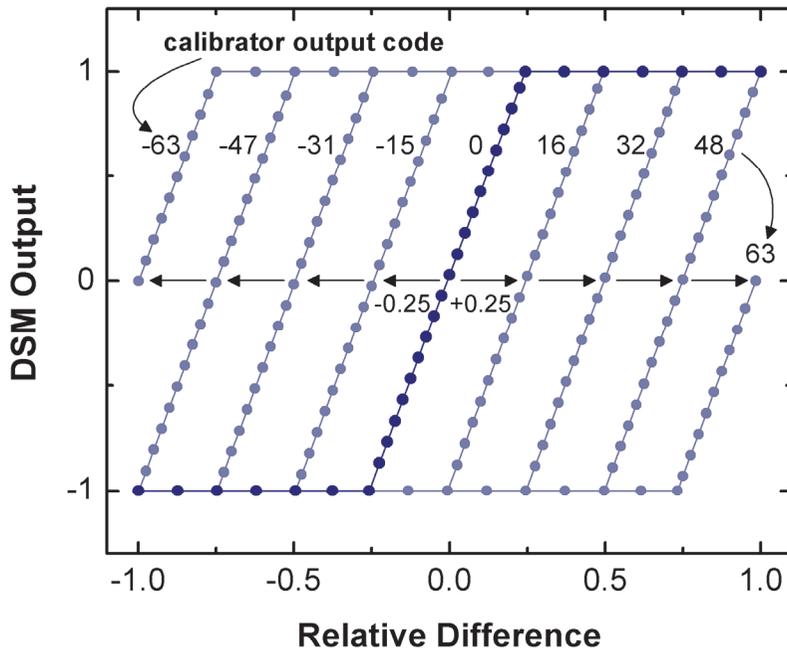


Fig. 2.3.6 Measured output characteristics of the interface circuit.

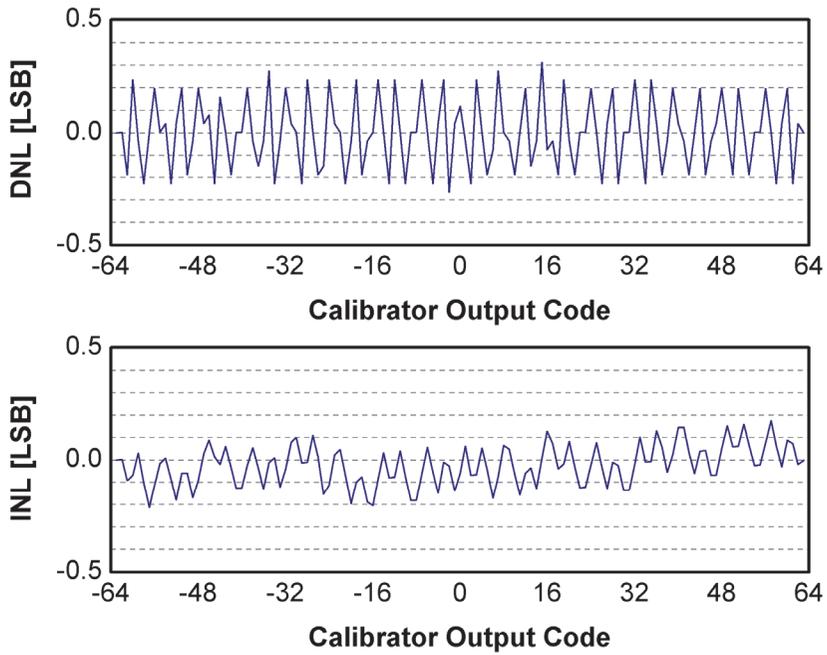


Fig. 2.3.7 Measured DNL and INL of the zero-point calibrator.

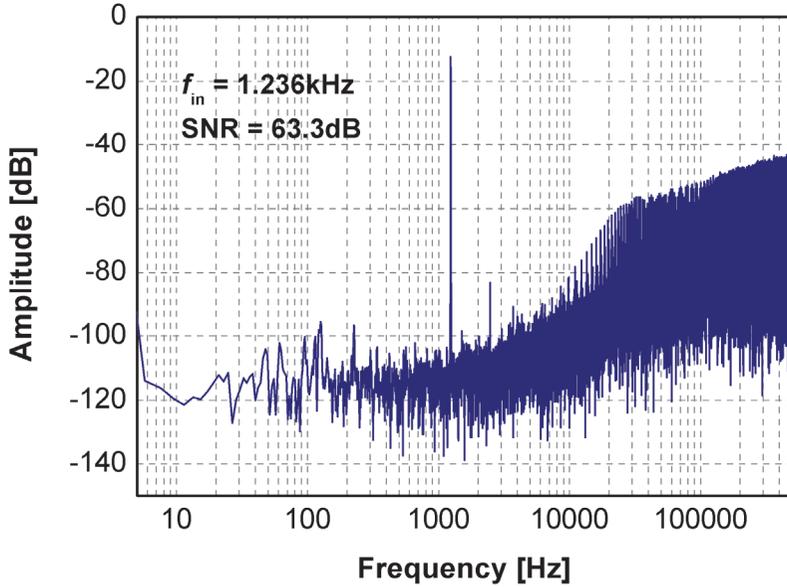


Fig. 2.3.8 Measured output spectrum of the DSM.

by using a Sinc^2 filter. As the initial offset measured by the zero-point calibrator shifts by multiples of 0.25, the input range of the DSM tracks it. The calibrator compensated for offsets from -1 to +1. The measured differential-nonlinearity (DNL) and integral-nonlinearity (INL) values of the calibrator are respectively within $\pm 0.32\text{LSB}$ and within $\pm 0.22\text{LSB}$, as shown in Fig. 2.3.7. The DNL and INL were measured with an SAR-CDC, which is configured in calibration mode and operates with a 1MHz clock. The SAR-CDC can be invoked repetitively by repeating CALIB, SET, SGNCHK, and SRI pulses while RST is high. Fig. 2.3.8 shows an output spectrum of the DSM for a sinusoidal input at 1.236kHz. This was obtained for a circuit operation without calibration mode. The measured signal-to-noise ratio (SNR) and effective number of bits were respectively 63.3dB and 10.2bit. This means that the DSM achieves an 11-bit resolution, that is, 0.49fF in capacitance.

CHAPTER 3

INTERFACE CIRCUITS FOR RESISTIVE BIO-CHEMICAL SENSORS

3.1 A CMOS READOUT INTEGRATED CIRCUIT WITH WIDE DYNAMIC RANGE FOR A CNT BIO-SENSOR ARRAY SYSTEM[†]

3.1.1 INTRODUCTION

Ever since carbon nanotubes (CNTs) are discovered by Iijima in 1991 [3.1.1], they have been treated as the most promising materials. Recently, CNTs demonstrate the sensitive modulation of its conductance to the charges adjacent to it [3.1.2]-[3.1.5]. This special property makes them to be used as chemical sensors for the voltage-mode detection of hazardous gasses such as NH₃ and NO₂. Several additional studies of CNT sensors show that there is a particular voltage across the CNT which is most suitable for each application. For instance, the detection of bio-molecules in an aqueous environment

[†]This sub chapter is published in *Proceedings of International Symposium on Low Power Electronics and Design* [1.2.4]. The author of the thesis is first author of the published paper.

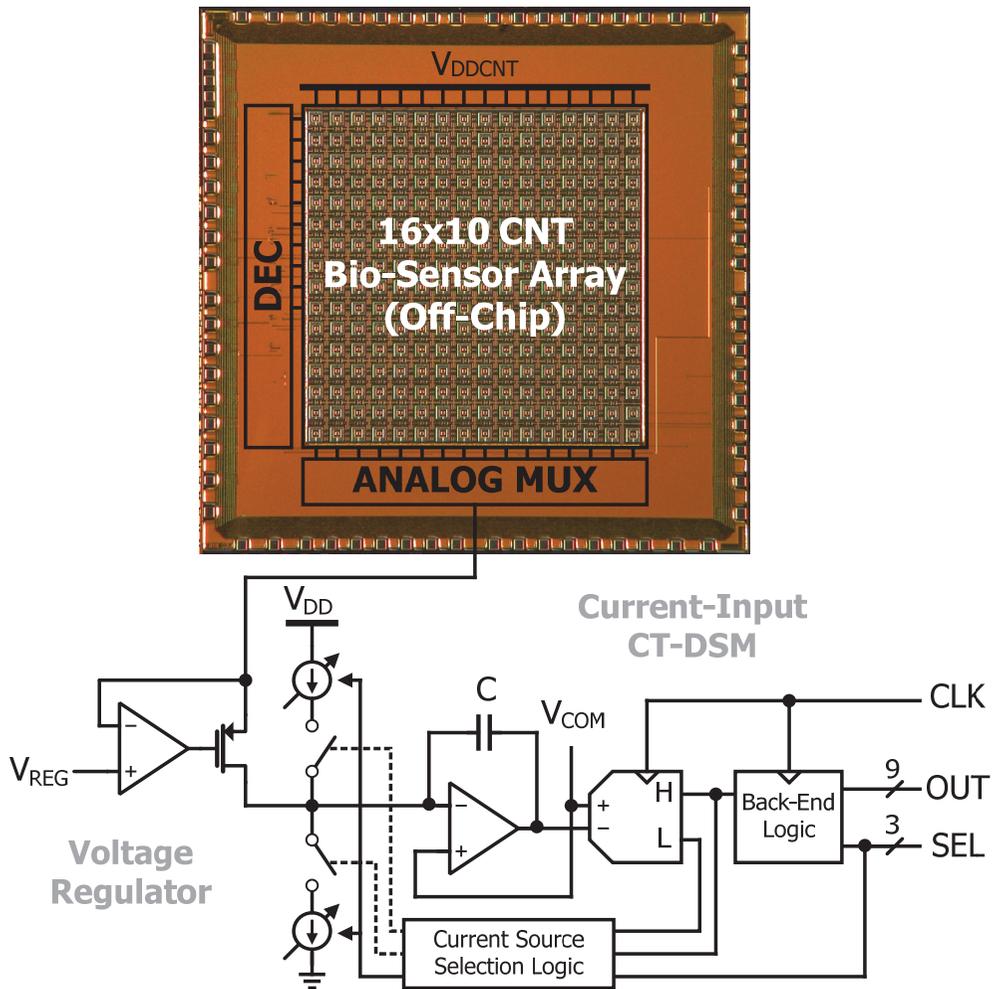


Fig. 3.1.1 Overall architecture of the proposed CNT ROIC.

requires a voltage below 1V to prevent side-effects caused by the ionization of the buffer solution [3.1.4]. Meeting this requirement involves current-mode detection which depends on the conductance characteristics of a CNT.

An array structure is frequently adopted in sensor applications, since it is known to

be relatively robust against undesirable effect such as process variation and environmental noise. In this case, the distribution of the initial conductance of CNT sensor elements is inherently spread widely. Therefore a readout circuit requires a wide dynamic range (DR) [3.1.5]. In general, a circuit with a high signal-to-noise ratio (SNR) which also has a wide DR is complicated and power hungry [3.1.6]-[3.1.8].

To cope with the problems described above, a low-cost and low-power current-to-digital conversion scheme is proposed for CNT sensors with dynamic range extension. Fig. 3.1.1 shows the overall architecture of the proposed readout integrated circuit (ROIC). The circuit consists of a voltage regulator and a current-input continuous-time $\Delta\Sigma$ modulator (CT-DSM), with a digital decimation filter. The voltage regulator sets voltage difference of $V_{DCCNT} - V_{REG}$ onto the CNT sensor, and the resulting current reflects the change in conductance. This current is then directly converted to a digital code by the current-input $\Delta\Sigma$ A/D converter.

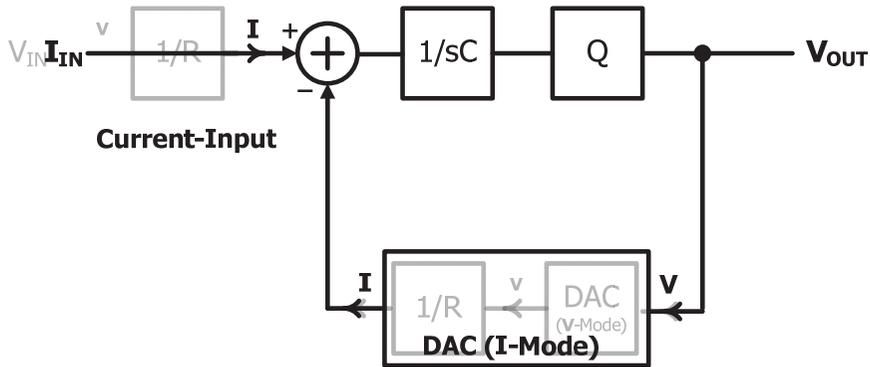


Fig. 3.1.2 A model of the current-input continuous-time $\Delta\Sigma$ modulator with 1st-order loop.

3.1.2 CIRCUIT ARCHITECTURE

Fig. 3.1.2 shows a model of the current-input continuous-time $\Delta\Sigma$ modulator with a 1st-order loop. The resistance of the loop coefficient of its linear model can be moved to the front of the input path and to the middle of the feedback path. Then the resistance R of the input path can be eliminated by transforming the input voltage V_{IN} to an input current I_{IN} by Ohm's law. Finally the resistance of the feedback path can be merged with that of the voltage-mode DAC, producing a current-mode circuit with a current DAC. In this structure, the full-scale input current $I_{IN(FS)}$ is determined from the full-scale output voltage $V_{OUT(FS)}$ and the feedback resistance R .

In a real implementation the resistance in the feedback path is implicitly included in that of the current DAC, so only the full-scale input current should be determined, which

is equal to $I_{DAC(MAX)}$, the maximum output current from the DAC:

$$I_{IN(FS)} = \frac{V_{OUT(FS)}}{R} = I_{DAC(MAX)} \quad (3.1.1)$$

This analysis can only be implemented as a circuit by eliminating the input resistance of the continuous-time $\Delta\Sigma$ loop and setting the maximum output current of the current DAC to the desired full-scale input current. Furthermore, if a 1-bit $\Delta\Sigma$ loop is adopted, a single current source supplying $I_{DAC(MAX)}$ may be sufficient. This makes the design both simple and effective because the full-scale input current is determined by the DAC alone. A similar analysis may be applied to a higher-order loop.

Fig. 3.1.3 shows the concept of the dynamic range extension scheme. In general, the DR is roughly proportional to the SNR. As already mentioned, an ADC of high SNR could be designed for sensor applications which require a wide DR, but a high-SNR circuit is an over-complicated way to achieve a high DR, and the high SNR would be wasted. Conversely, an ADC of moderate SNR will be less adaptive to variations in sensor characteristics because of its narrow dynamic range. In the proposed scheme, only one core ADC is utilized, and its full-scale input level is adjusted to match the range of the current input. This allows an ADC of moderate SNR to provide an extended DR, as shown in the rightmost diagram of Fig. 3.1.3. As a result, the total dynamic range DR_{TOTAL} of the circuit is given as follows:

$$DR_{TOTAL} = DR_{ADC} + (FS_{MAX} - FS_{MIN}) \quad (3.1.2)$$

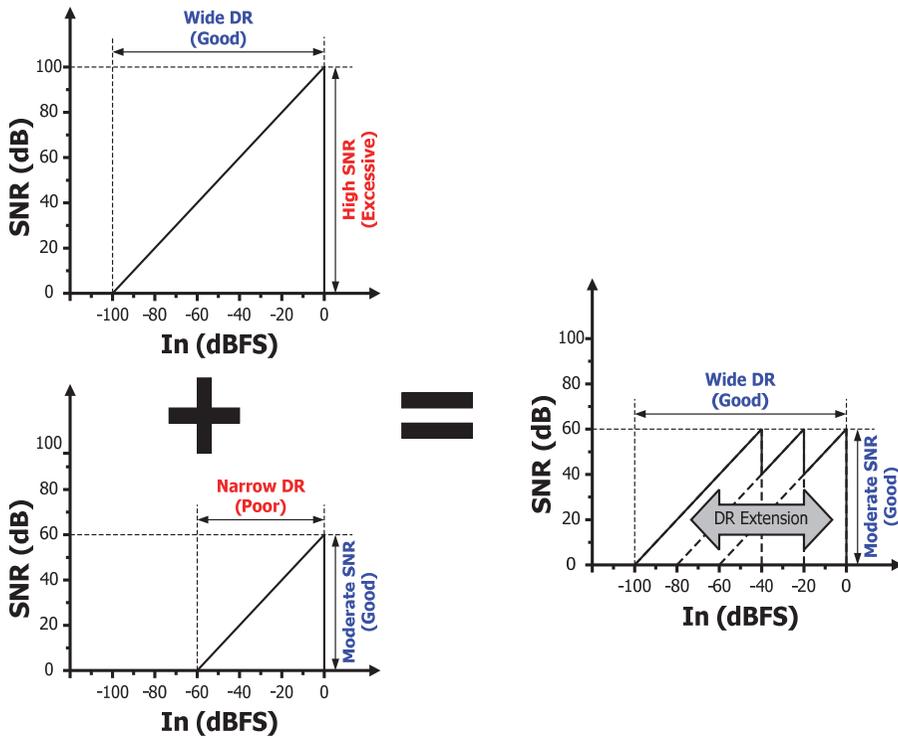


Fig. 3.1.3 The concept of the dynamic range extension scheme.

where DR_{ADC} is the dynamic range of the core ADC, FS_{MAX} is the maximum full-scale input, and FS_{MIN} is the minimum full-scale input, all expressed in decibels.

3.1.3 CIRCUIT IMPLEMENTATION

The schematic of the 1st-order 1-bit current-input continuous-time $\Delta\Sigma$ ADC for the sensor array is shown in Fig. 3.1.4. It is implemented as a bidirectional single-ended circuit, which consists of a current DAC with the capability for full-scale current

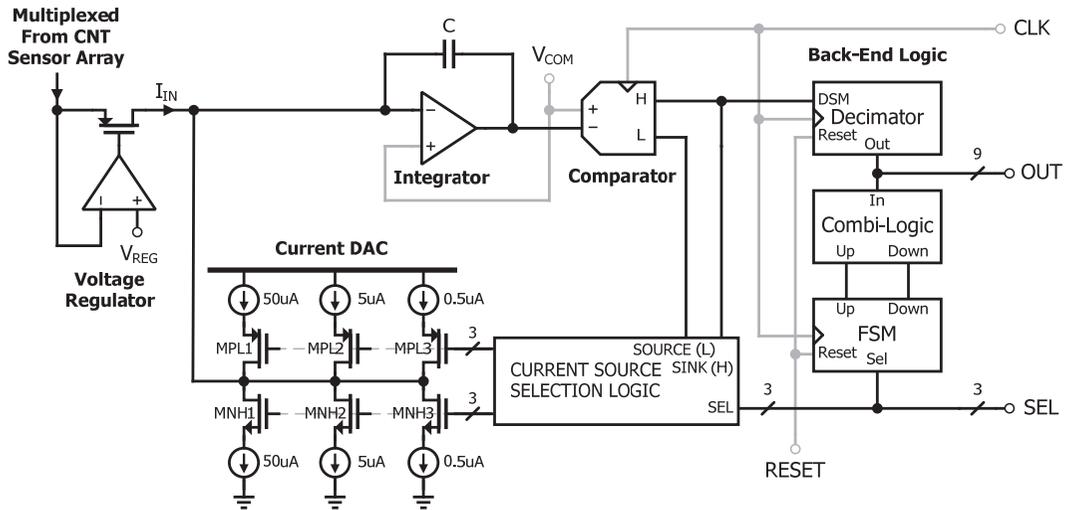


Fig. 3.1.4 1st-order 1-bit current-input continuous-time $\Delta\Sigma$ ADC with a voltage regulator for the ROIC.

adjustment, an integrator consisting of an op amp and an integrating capacitor C , a comparator acting as a 1-bit quantizer, and back-end logic. This logic decimates the $\Delta\Sigma$ modulator outputs and determines the correct full-scale current of the DAC for the range of the input.

3.1.3.1 Current DAC

The current DAC sources current into, or sinks current from the integrating capacitor, depending on the outputs H and L of the modulator loop [3.1.9, 3.1.10]. In the proposed design, three different full-scale currents of $50\mu\text{A}$, $5\mu\text{A}$ and $0.5\mu\text{A}$ are available. Combinational logic circuitry is added to select the current source for each range, following instructions from the back-end logic.

3.1.3.2 Integrator and Comparator

The value of the integrating capacitor C is primarily determined from the loop characteristics, such as the oversampling ratio (OSR). However, a linear model does not reflect exact operation of a feedback loop containing a 1-bit quantizer. So the loop is analyzed and simulated repeatedly, including the 1-bit quantizer and non-ideal op amp, until a proper condition is reached. The op amp in the integrator must have an appropriate DC gain and unity gain bandwidth (GBW). In a continuous-time implementation, a GBW frequency which is slightly higher than the sampling clock frequency is sufficient. The DC gain must be carefully chosen to correspond with the OSR.

To design the comparator as a 1-bit quantizer, a non-return-to-zero (NRZ) output is selected, which is easy to incorporate in this design. Attention must be paid to the clock jitter and the clock-to-output delay, caused by metastability; both of these can degrade the SNR.

3.1.3.3 Back-End Logic

The back-end logic consists of the decimator, the combinational logic which determines whether the current input level is in the currently selected full-scale range, and the finite-state machine (FSM) that controls which range should be selected.

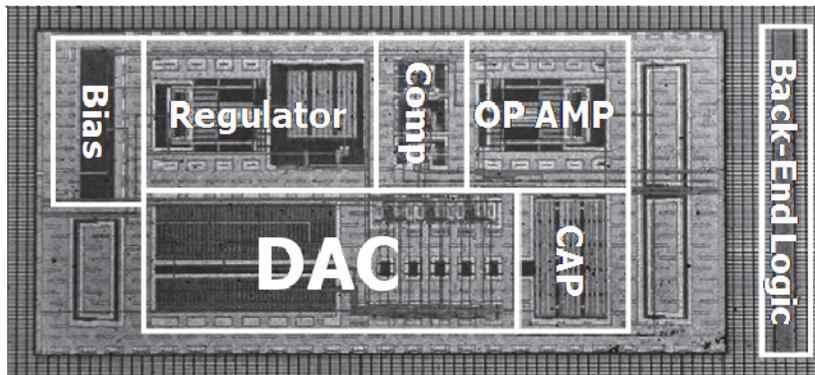


Fig. 3.1.5 Microphotograph.

This design is simplified by the use of a simple 1st-order sinc filter as the decimator [3.1.8]. The combinational logic observes the output of the decimator and generates an *UP* signal if the converted value exceeds an upper threshold or a *DOWN* signal if the converted value falls below a lower threshold. The FSM receives these *UP* and *DOWN* signals as inputs and changes the 3-bit control code *SEL* to select the appropriate current source for the current DAC which is then turned on. The transitive instant of the FSM output is synchronized to the rising edge of the clock and the output period of the decimator. In this design, upper thresholds are -26dBFS and -46dBFS, and lower thresholds are -28dBFS and -48dBFS, respectively. This allows a 2dB margin between the scale-up and scale-down thresholds, so as to prevent the circuit from falling into any metastable transition between two neighboring full-scale current ranges. If more reduced non-linearity in the transfer characteristic of the ROIC at each boundary crossing is preferred, the current DAC should be calibrated to guarantee more precision in the ratio among the currents of sources and sinks.

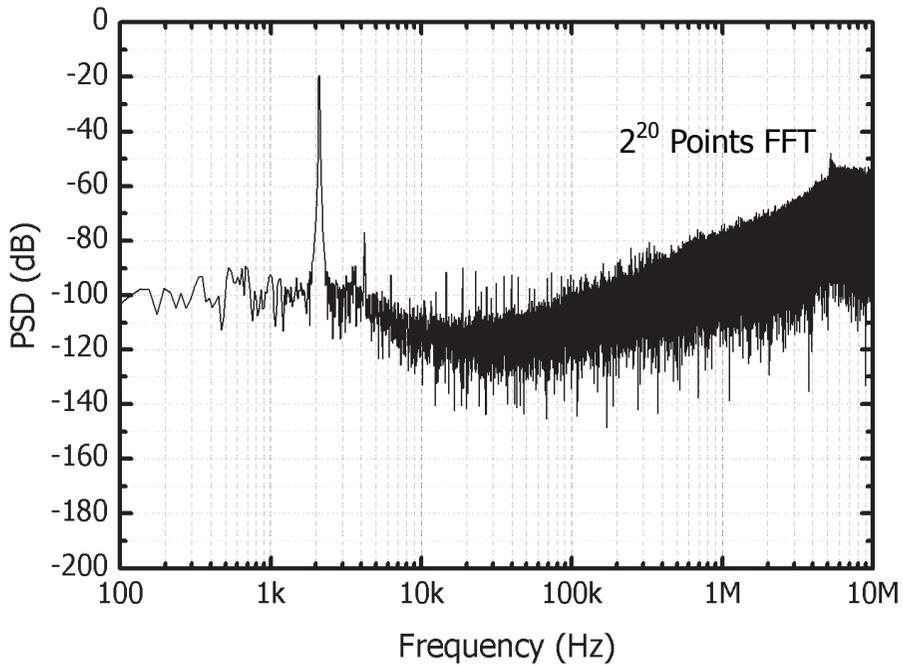


Fig. 3.1.6 Output power spectrum of the $\Delta\Sigma$ modulator.

3.1.4 EXPERIMENTAL RESULTS

The proposed circuit has been fabricated in a $0.18\mu\text{m}$ CMOS bulk technology. Fig. 3.1.5 shows its microphotograph. The core area is 0.085mm^2 . The ADC operates at 20.48MHz sampling clock frequency with 1.8V supply and it consumes $8.94\mu\text{W}/\text{cell}$ considering the 16×10 sensors. In-band frequency of 160kHz with the OSR of 64 enables the ADC to process maximum 16×10 cells at least $1\text{kS}/\text{s}$ conversion rate. Maximum full-scale input current for the readout circuit is $50\mu\text{A}$. In an AC test with a 2.101kHz

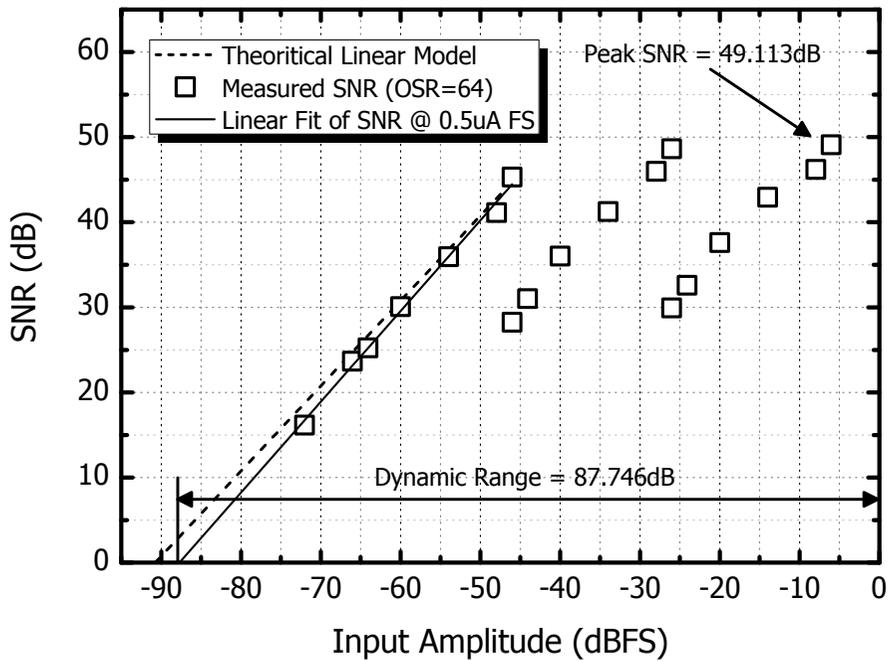


Fig. 3.1.7 Measured overall SNR characteristic with the extended dynamic range.

sinusoidal input, the measured SNRs were 49.113dB, 48.652dB and 45.316dB, for input currents of 25 μ A, 2.5 μ A and 250nA respectively. The output spectrum of the $\Delta\Sigma$ modulator at 25 μ A is shown in Fig. 3.1.6. A DC test demonstrated that the dynamic range extension scheme works properly.

The overall SNR characteristic with the extended dynamic range is shown in Fig. 3.1.7. Proposed circuit achieves a dynamic range of 87.746dB. Considering the allowed maximum full scale input current and the operating region of the regulator, the regulated voltage onto the CNT sensor can range from 50mV to 3.3V approximately. In this case, the measured dynamic range potentially corresponds to the resistance range from 1k Ω to

Table 3.1.1 Performance Summary.

Technology	0.18 μ m 1P6M CMOS
Supply Voltage	1.8V
Sampling Frequency	20.48MHz
In-Band Frequency	160kHz
Oversampling Ratio	64
Power Consumption/Cell	8.94 μ W/cell
Measured SNRs (2.101kHz Sinusoidal Input)	49.113dB (25 μ A Input)
	48.652dB (2.5 μ A Input)
	45.316dB (250nA Input)
Overall Dynamic Range	87.746dB

1.5M Ω . If extended upper bound of the measurable resistance is necessary, it is easily achievable since V_{DCCNT} is independent from the supply voltage of the ROIC, V_{DD} . Table 3.1.1 summarizes the design and performance parameter.

3.2 INTEGRATING METAL-OXIDE-DECORATED CNT NETWORKS WITH A CMOS READOUT IN A GAS SENSOR[†]

3.2.1 INTRODUCTION

The detection of chemicals is critical for processes such as industrial process control and environmental monitoring. Nanostructure sensors are small and consume little power, while also effectively detecting many chemicals in real time. Carbon nanotubes (CNT) are one promising candidate as an active element in such sensors because of high sensitivity resulting from large surface area. Carbon nanotubes (CNT) were initially characterized by Iijima [3.2.1] in 1991, and CNT-based chemical sensors were demonstrated in 2000 [3.2.2, 3.2.3]. The special geometry of the CNT makes it electrochemically active. Further, the electrical properties of a CNT network to be modulated by various chemicals such as NH₃ and NO₂. The sensing mechanism of a CNT differs between reactants, but it is generally known that electron-accepting molecules (e.g. NO₂) and electron-donating molecules (e.g. NH₃) can interact with CNTs directly or indirectly and modify the Fermi level. The result is that a CNT sensor can have lower resistance and operating

[†]This sub chapter is published in *MDPI Sensors* [1.2.5]. The author of the thesis is first author of the published paper.

temperature than an equivalent metal-oxide sensor. However, there are limitations dependent upon the device structure including irreversibility, long recovery time, and insufficient selectivity.

The two elementary types of CNT gas sensors: single aligned CNT devices and the simpler random network CNT type. In the case of a single aligned CNT, the sensors offer good sensitivity at room temperature, but the fabrication costs are high and the sensors offer limited selectivity with an irreversible response [3.2.2]. In response, metal-decorated CNT random network sensors have been researched [3.2.4, 3.2.5]. These devices are formed by covering or “decorating” metal particles on the surface of the CNTs to enhance sensitivity to certain gases compared with bare CNT networks. Furthermore, better selectivity can be obtained in sensors intended to detect natural gases because sensitivity depends strongly upon the type of metal deposited. Metal-decorated random-network CNT network sensors often display both better reversibility [3.2.4]-[3.2.8], and fabrication procedures are more easily scaled than the single-CNT type. Applying signal processing techniques such as pattern matching to the output of an array of metal-decorated CNT cells allows a multi-modal sensor to be constructed which is able to detect several different gases [3.2.9].

Nevertheless, metal-decorated random network sensors have a rather wide resistance range, unpredictable performance, and a limited selectivity. These difficulties can be overcome with a multi-cell CNT network structure, which averages out single-device

variations [3.2.9]. A recording system for this type of sensor has also been developed [3.2.10], but it is not appropriate for ubiquitous sensor networks because the CNT sensors and the read-out circuit are not integrated onto a single die. Furthermore, the bare CNT networks in the previous work suffer from poor reversibility and a short lifetime.

Therefore, in this work metal-oxide-decorated CNT network gas sensors are combined with a read-out circuit on a single die to produce a system suitable for ubiquitous sensor network applications. The chemistry that will be considered in this study is restricted to the detection of NH_3 gas using SnO_2 -decorated CNT networks. This scenario is sufficient to verify the operation of the sensor system, but its chemistry can easily be extended to many other gases.

In section 3.2.2 the fabrication of CNT network sensors is introduced, bare CNT networks are compared with metal-decorated CNT networks, and the measurement system is described. From section 3.2.3 to section 3.2.5 the single-die, multi-cell sensor architecture is introduced which includes a read-out circuit. Circuit design issues and the overall structure of the sensor system are all discussed in-depth. Section 3.2.6 covers the measured results and discussion topics related to this sensor system.

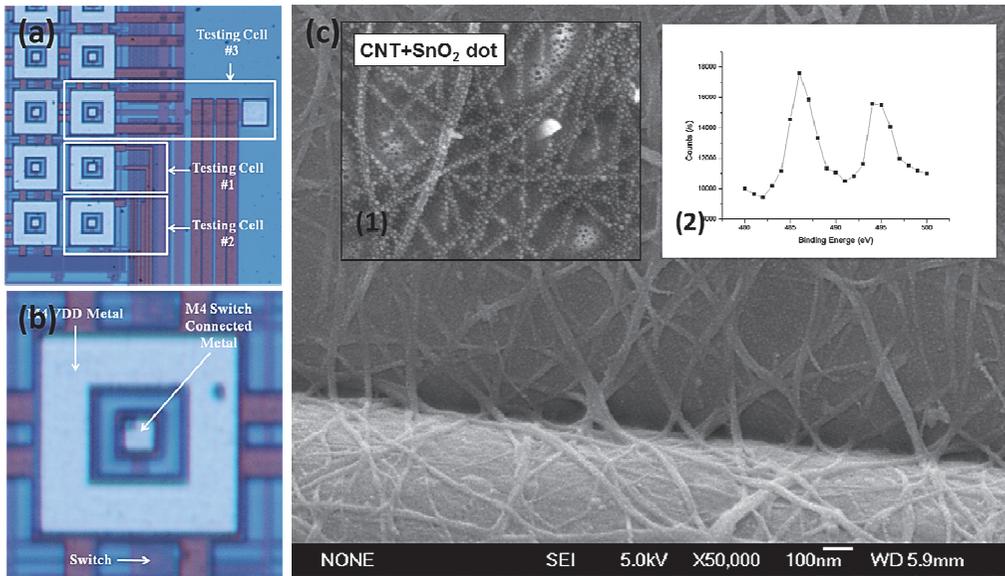


Fig. 3.2.1 CNT sensing cell information. (a) Optical image of CNT test cells. (b) Individual CNT cell. (c) SEM image of the SnO₂-decorated CNT network. (c.1) SEM image of the SnO₂-decorated CNT network at higher magnification. (c.2) Core-level XPS Sn3d spectrum indicating oxidation of the Sn.

3.2.2 EXPERIMENTAL: CARBON NANOTUBE SENSING CELL FABRICATION

To allow an array of metal-oxide-decorated CNT network sensors to share a die with an ROIC, concentric electrodes were fabricated on the die using conventional complementary metal oxide semiconductor (CMOS) processes, as shown in Figs. 3.2.1(a) and 3.2.1(b). The enclosing and island electrodes of each cell were constructed from a top metal layer (M4, Al), and the oxide layer applied during die passivation was partially eliminated from both electrodes to interface the sensors to the ROIC. Then the aluminum electrodes were gold-plated to reduce the contact resistance between electrodes and the

CNT network sensors. Platinum plating is generally considered more suitable for gas sensing applications, in which platinum acts as a catalyst. But gold-plated electrodes are more suitable for biological sensing applications, as reported in previous research [3.2.11]. To construct the CNT networks between the inner and outer electrodes, 0.05g p-type single-walled CNTs were immersed in a 1L bath of 1,2-dichlorobenzene, and the die was dipped into that solution [3.2.12, 3.2.13]. To avoid shorting the contact pads, the die was only immersed deeply enough to deposit the CNTs on the electrodes.

Subsequently, SnO₂ nanoparticles were deposited by thermal evaporation. The deposition was performed with a room-temperature chuck to avoid damage to the other CMOS devices on the die. The CNT-loaded CMOS circuits were attached to a 4 inch silicon wafer and put into an MH-1800 thermal evaporator, using 99.999% Sn as the metal source. Deposition was performed at a rate of 0.1Å/s for 100s, at a pressure of 7.0x10⁻⁶ torr. After deposition, the die was extracted from the chamber, and the metallic tin was naturally oxidized by air at room temperature.

Fig. 3.2.1(c) and Fig. 3.2.1(c) inset 1 show SEM images of the CNT network decorated with SnO₂ nanoparticles. It is shown that the CNTs have been homogeneously distributed between electrodes and connected into a network by the dip-coating process. The SnO₂ nanoparticles deposited on the CNT networks by evaporation are spherical, with diameters of 3-5nm. Because these dots of tin are so small, they are easy to oxidize. To check the extent of this oxidization, the chemical state of the SnO₂ was examined

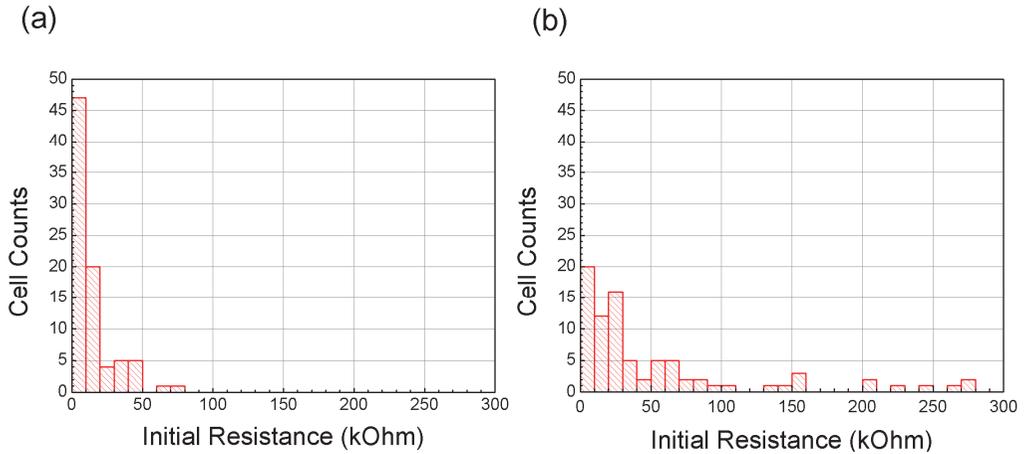


Fig. 3.2.2 CNT network initial resistances (a) Distribution of initial resistance for the bare CNT networks. (b) Distribution of initial resistance for the SnO₂-decorated CNT networks.

using a Sigma Probe X-ray photoelectron spectroscope (from ThermoVG, UK) with Al K radiation (1486.6eV). Inset 2 of Fig. 3.2.1(c) shows the core-level X-ray photoelectron spectroscopy (XPS) spectrum for Sn3d, which were calibrated to the hydrocarbon C1s line at 284.5eV. The Sn3d spectrum exhibits a double feature at 494.6eV (3d3/2) and 486.3eV (3d5/2). These peaks agree respectively with the values for the tin and oxygen that comprise the lattice structure of SnO₂ [3.2.14].

Fig. 3.2.2 shows the distribution of initial resistance for the bare CNT networks and the SnO₂-decorated networks. It is shown that the initial resistances of individual sensors are increased by the decoration processes, and that they are also widely distributed. Fully determining the reasons for these changes is beyond the scope of this study, but it can be speculated that two factors are involved: the depletion of charge in the CNTs and added

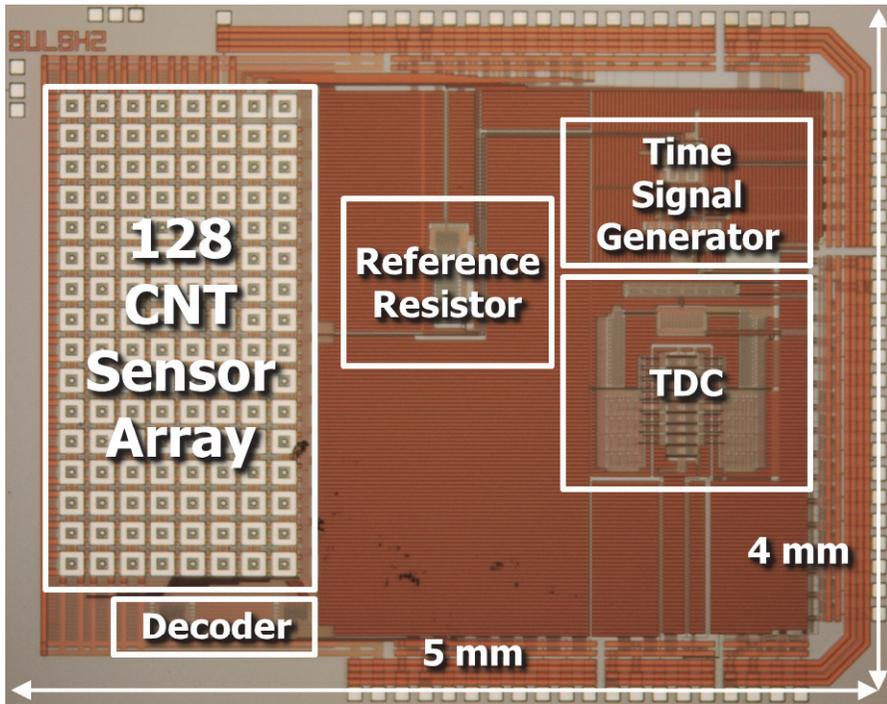
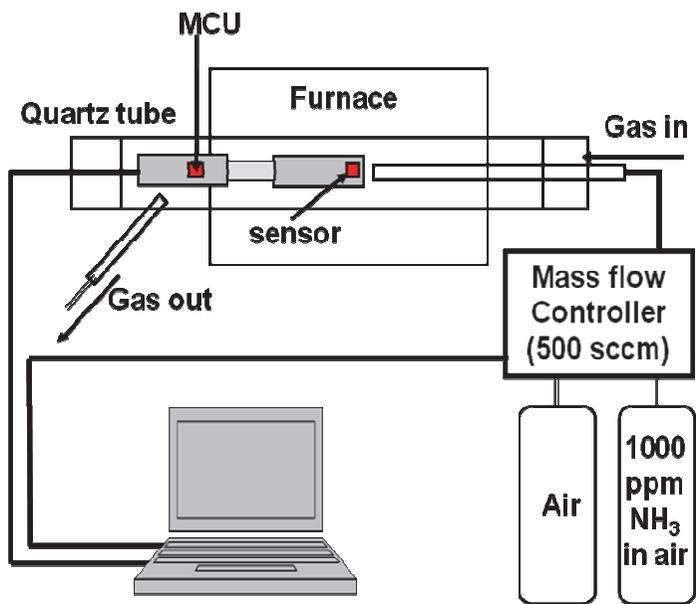


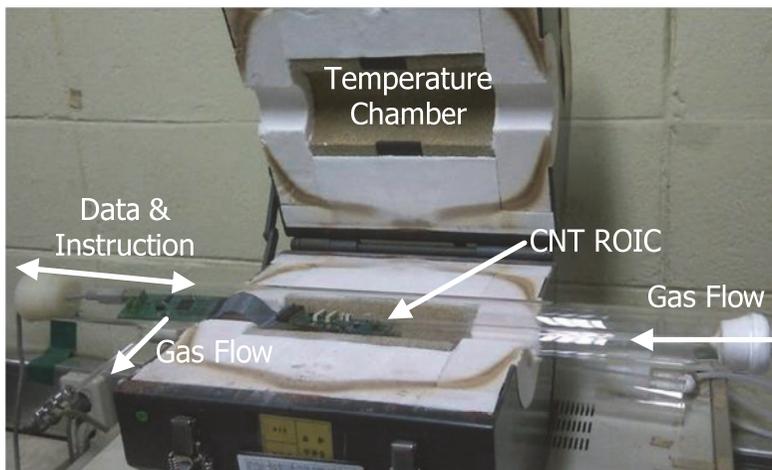
Fig. 3.2.3 Optical image of the CNT ROIC die.

charge centers after SnO_2 deposition; and damage to the CNT networks during SnO_2 deposition. These two factors are likely to obstruct currents flowing across the CNT networks and cause their resistance to increase.

The CNT ROIC chip was fabricated using a $0.35\mu\text{m}$ CMOS process, as shown in the photograph in Fig. 3.2.3. Integrating the CNT networks and the ROIC on the same die is done by locating the CNT cells on the left-hand side of the ROIC, while the pads are located on the right. With this layout, it is possible to dip the cells into the CNT solution as described above, while keeping the pads above the liquid to avoid introducing



(a)



(b)

Fig. 3.2.4 CNT sensor measurement system. (a) Schematic diagram showing the concept and operation of the temperature-controlled measurement system. (b) Photograph of the test equipment.

shorts between them. The CNT ROIC die is then connected to the PCB using the chip-on-board process, with the CNT sensor cells remaining exposed to react with gas. Fig. 3.2.4 shows the arrangements for testing the CNT ROIC. The experimental sensing setup utilizes mass flow controllers interfaced to a computer and a 38mm diameter quartz reaction tube. The circuit is powered via a USB connection to the computer, which serves as both a 5V power supply and data interface. In this manner, air (21% O₂/N₂, 99.999%) with or without 1000ppm of NH₃ gas can be introduced into a temperature-controlled environment while performing electrical characterization. This arrangement also promotes uniform flow across the array of CNT cells, which was fixed at 500cm³/s.

3.2.3 THE ROIC ARCHITECTURE

3.2.3.1 The CNT Cell Array Structure

The CNT cell array has 8 rows and 16 columns. There are three test cells, and the remaining 125 cells are connected to the read-out circuit core that measures their resistance. Fig. 3.2.1(b) shows the structure of one of the non-test cells. The outer ring of metal is connected to VDD and the metal at the centers is connected to the read-out circuit core. The passivation layer which was applied to both of these metal areas has been partially eliminated, as discussed in the previous section, to allow the cell to be interfaced to the read-out integrated circuit (ROIC). This process is the same as that used

to open pads.

Fig. 3.2.1(a) shows the structure of each of the three test cells in the array. The first of these cells is used to check whether the CNTs have been deposited satisfactorily, and for testing the switch circuit. In this cell, the outer and inner metal areas are both connected to the pad and the resistance of the CNT network deposited on that metal can be measured using a multimeter. This provides an initial check on CNT functionality which is independent of the ROIC. The input, output, and control signal lines of the switch are also linked to the pad, allowing the switch circuit to be tested without difficulty.

In the second test cell, the inner metal area is connected to the input signal line of the switch, which has its output signal and control signal lines are connected to the pad. This allows cell selection operations to be tested, as well as providing further verification of CNT functionality.

The third test cell has the same structure as the second, except that the inner metal area is connected to the pad and to the input signal line of the switch. This arrangement can be used to calibrate the ROIC, using a technique which will be described later.

Fig. 3.2.5 shows the arrangement of the CNT sensor array circuit. A 7-bit digital code, ROWSEL[0:2] and COLSEL[0:3], assigned from outside the chip selects a single sensor cell. A 3-bit row decoder and a 4-bit column decoder respectively determines the

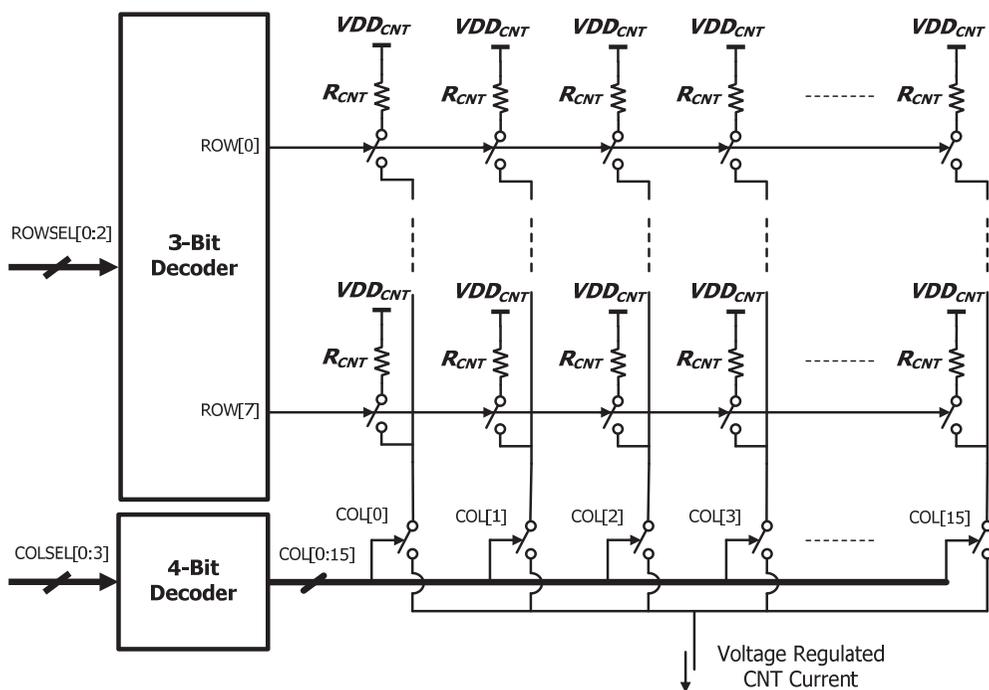


Fig. 3.2.5 Circuit schematic for CNT sensor array. Individual CNT cells can be measured via the 3 bit row decoder and 4 bit column decoder.

row and column of the cell. When a CNT cell is connected to the ROIC, there exists a constant voltage drop across the CNT cell. This results from the voltage regulation loop inside the ROIC and produces a steady current through both cell and ROIC allowing the resistance of the CNT networks to be measured.

3.2.3.2 Analog Front-End Circuit

There are two possible ways to read the resistance of the CNT network in a cell. A constant current can be generated through the cell and the voltage across it can be

measured, or a fixed voltage can be applied and the resulting current can be measured. The first method has good linearity because the resulting voltage is directly proportional to the resistance. But a complicated circuit is required to generate a constant current accurately. With the second method, the inverse proportionality, $I = V/R$, should be considered but the generation of a constant voltage is a much simpler task.

Here, a simple circuit is used in which a constant voltage is applied to the CNT cell and the resulting current charges a capacitor. The charging time is measured until the voltage across this capacitor exceeds a threshold. This charging time can be expressed as follows:

$$\Delta T = \frac{C \Delta V_{\text{Charge}}}{V_{\text{DD}} - V_{\text{Regulation}}} R. \quad (3.2.1)$$

Indirect measurement of the current as a charging time allows accurate measurements to be made by a simple circuit.

The simplest way of measuring the charging time of the capacitor is to count clock cycles. Then the dynamic range of the ROIC is only limited by the shortest and longest time that can be measured. The shortest detectable time is fixed by the clock period, but it can be extended by introducing a time-to-digital converter (TDC) circuit based on a delay-locked loop (DLL). This TDC circuit will be discussed in detail in the next section. The longest detectable time is determined by the number of bits in the clock cycle counter.

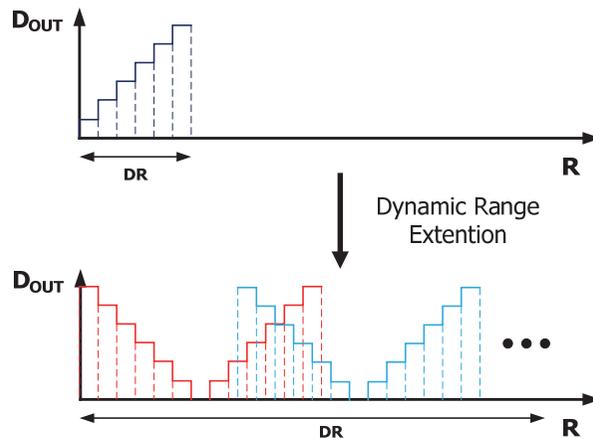


Fig. 3.2.6 Dynamic range extension scheme to allow a greater range of charging times of an output capacitor to be measured. The improved timing ranges allow greater accuracy for simple and effective on-chip measurement of the current.

The dynamic range extension scheme shown in Fig. 3.2.6 is used to increase the charging time that can be measured with a given range of detectable times. An on-chip switching reference resistor, a replica regulator and a replica time-signal generator, consisting of a comparator and a capacitor are introduced. The voltage drop across the cell and the on-chip reference resistor is the same, and each of the resulting currents charges an identical capacitor. The difference between the time required to charge these two capacitors is digitized by the read-out circuit. The resistance of on-chip reference resistor can be changed by a external digital code, which achieves a wide dynamic range.

Fig. 3.2.7 shows the on-chip reference string of $20\text{k}\Omega$ resistors. Its overall resistance can be set from $20\text{k}\Omega$ to $320\text{k}\Omega$, in steps of $20\text{k}\Omega$, by an externally supplied 4-bit code, REFRSEL[0:3].

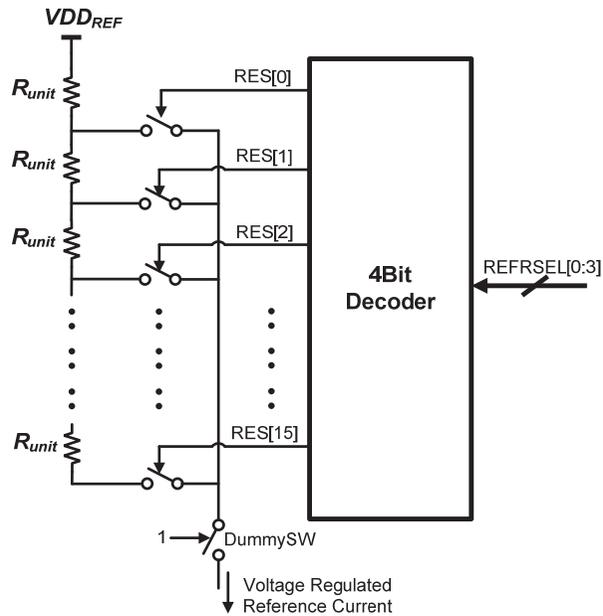


Fig. 3.2.7 The reference resistor string. Each resistor R_{unit} is $20k\Omega$, permitting the resistance to be dynamically varied from $20k\Omega$ to $320k\Omega$ in $20k\Omega$ steps.

Fig. 3.2.8 shows the analog front-end circuit of the CNT ROIC. An op-amp and a PMOS transistor maintain the voltage at nodes A and B at V_{Ref3} . When the INIT signal is high, the capacitors C_{REF} and C_{CNT} are discharged and the voltage at nodes C and D becomes V_{Ref1} . When the INIT signal goes low, two capacitors are charged and the voltages at nodes C and D increase. But the rates at which the voltages at C and D increase are different because the CNT network and the reference resistor can be expected to have different resistances. When the voltage at either node reaches V_{Ref2} , the START signal goes high; and when the second node also reaches V_{Ref2} , the STOP signal goes high. The T_{DIFF} signal which controls the clock cycle counter goes high with the START signal,

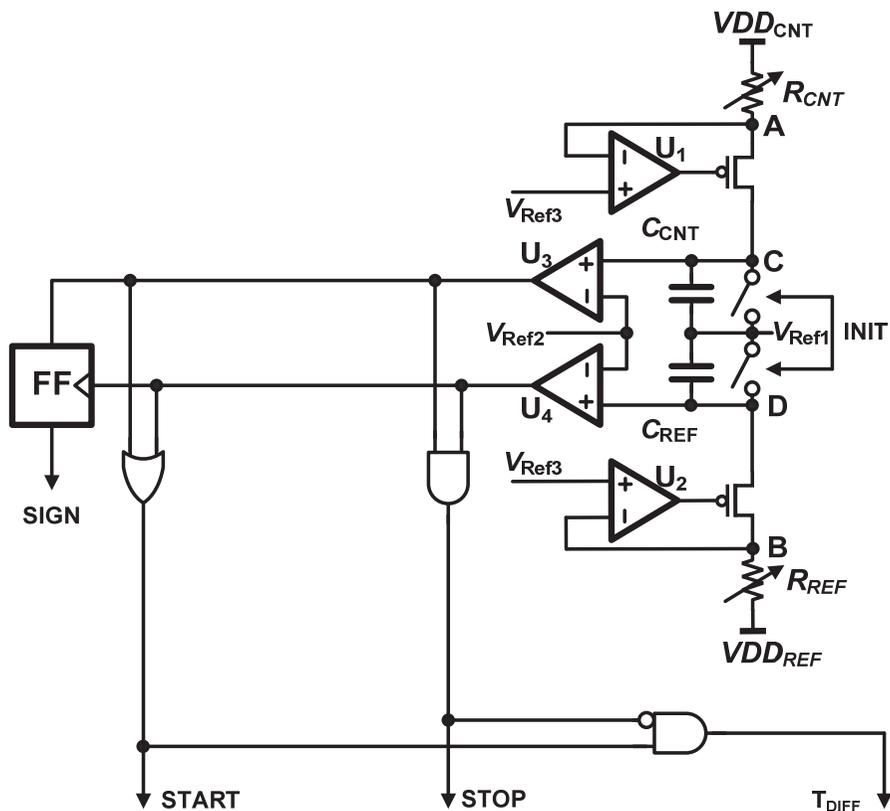


Fig. 3.2.8 The analog-front-end circuit of the CNT ROIC used for measurement of the current across the CNT sensor cell.

and then goes low again when the STOP signal goes high. The clock cycle counter and the DLL-based TDC together convert the time of the between arrival of the START and STOP signals to a digital code. These circuits will be discussed at next section. The SIGN signal indicates whether node C or node D reached V_{Ref2} first. If it was C, then the SIGN signal is high, but if it was D the SIGN signal is low. This SIGN signal and the encoded 12-bit output data can be used by the program in a controller or PC to determine the resistance of the CNT network at a selected cell.

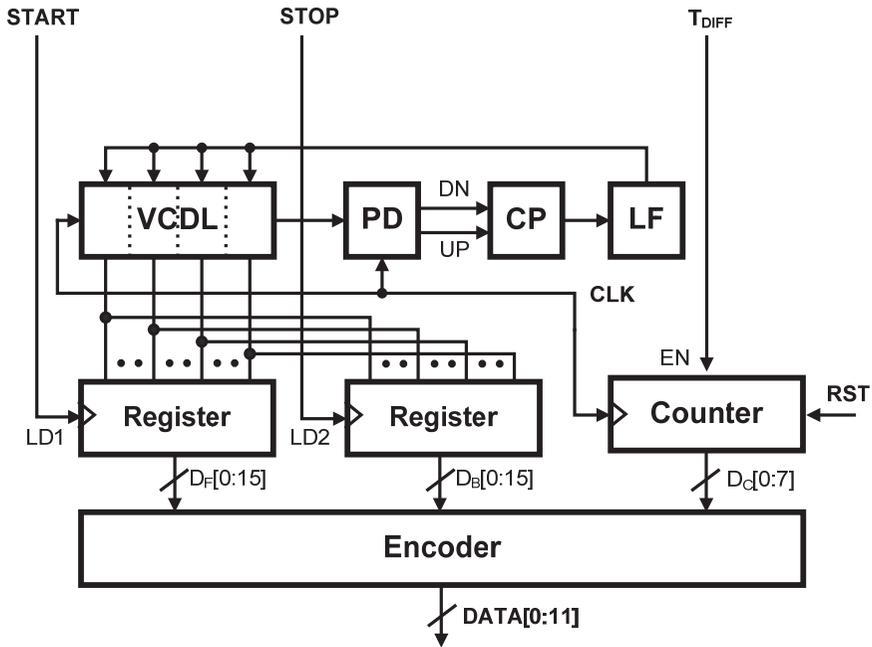


Fig. 3.2.9 Analog to digital TDC circuit in the CNT ROIC.

3.2.3.3 DLL-Based TDC

The T_{DIFF} signal generated by the analog front-end circuit is converted to a digital code by the TDC. The simplest form of TDC is a clock cycle counter. When the T_{DIFF} signal goes high the clock cycle counter is enabled, and it then operates until the T_{DIFF} signal goes low. With this arrangement, the maximum measurable time range is determined by the total number of bits of the clock cycle counter. For the design, 8 bits are selected.

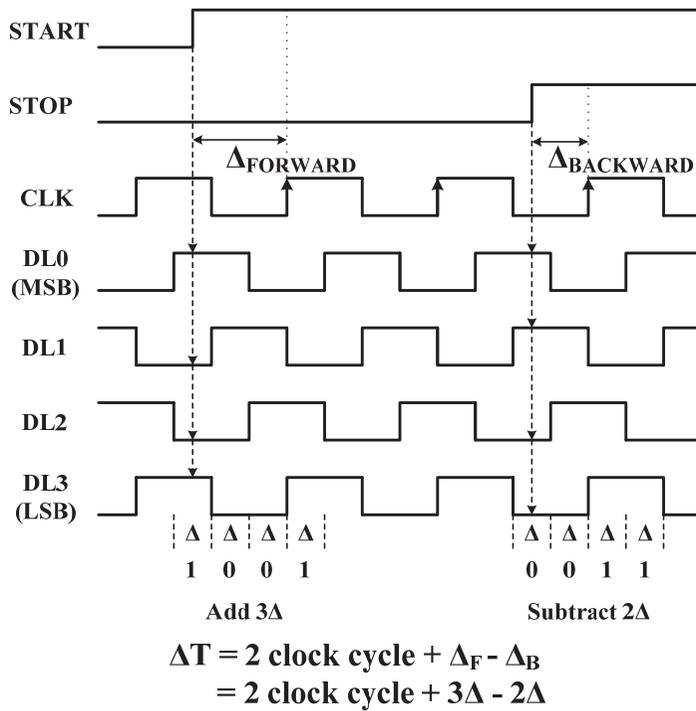


Fig. 3.2.10 Example of fine TDC operation (with 4 delay cells). The real design as 16 delay cells.

The resolution of this type of TDC is determined by the length of a clock cycle. This resolution can be improved by multiplying the clock frequency, but power consumption is directly proportional to this frequency. Instead, a DLL-based fine TDC is combined with a counter-based coarse TDC as shown in Fig. 3.2.9. A DLL is used to generate multi-phase clock signals in the fine TDC. Once the DLL is locked, assuming there is no harmonic lock problem, the DLL output clock is delayed by a single clock cycle with respect to the input clock. Thus the delay produced by each cell in the DLL is a clock period divided by the total number of delay cells. The START and STOP signals sample the clock phases and cause the states of the delay-line to be stored in registers. These

states fix times of arrival of the START and STOP signals within the clock period. The sampled code is changed to binary, and then added to, or subtracted from, the clock cycle counter code. Fig. 3.2.10 shows the operation of the fine TDC diagrammatically, using 4 delay cells. The actual design has 16 delay cells.

It has already been described that how a clock cycle counter is used to obtain a coarse time with a wide range. The delay-lines of the DLL obtain the fine time by interpolation within the period of the reference clock CLK. Thus the encoder receives three digital codes, D_{COUNTER} from the counter and D_{FORWARD} and D_{BACKWARD} from the delay-line registers. From this data it determines an n-bit digital code, D_{OUT} , which is the digital representation of T_{DIFF} signal as follows:

$$D_{\text{OUT}} = D_{\text{COUNTER}} \times 2^M + (D_{\text{FORWARD}} - D_{\text{BACKWARD}}). \quad (3.2.2)$$

3.2.4 CALIBRATION AND ERROR REDUCTION

3.2.4.1 Device Mismatch and Calibration

Although a circuit may be designed with matched sizes of MOS transistors or capacitors, they will not have truly identical dimensions in a real implementation because of technology limitations. This device mismatch effect is well known to cause problems such as op-amp offsets, and needs to be anticipated.

In the analog front-end circuit, the charging times of nodes C and D can be expressed by the following equations:

$$\Delta T_{\text{CNT}} = \frac{R_{\text{CNT}} \times C_{\text{CNT}} \times \Delta V'_{\text{CNT}}}{\text{VDD}_{\text{CNT}} - V'_{\text{Ref,CNT}}}, \quad \Delta T_{\text{REF}} = \frac{R_{\text{REF}} \times C_{\text{REF}} \times \Delta V'_{\text{REF}}}{\text{VDD}_{\text{REF}} - V'_{\text{Ref,REF}}} \quad (3.2.3)$$

Where $V'_{\text{Ref,CNT}} = V_{\text{Ref3}} - V_{\text{OS1}}$, $V'_{\text{Ref,REF}} = V_{\text{Ref3}} - V_{\text{OS2}}$, $\Delta V'_{\text{CNT}} = V_{\text{Ref2}} + V_{\text{OS3}} - V_{\text{Ref1}}$, and $\Delta V'_{\text{REF}} = V_{\text{Ref2}} + V_{\text{OS4}} - V_{\text{Ref1}}$. The four voltages V_{OS} are the offsets of the op-amps U_1 , U_2 , U_3 and U_4 . The digital code T_{DIFF} output by the ROIC can be related to ΔV_{CNT} and ΔV_{REF} as follows:

$$T_{\text{DIFF}} = \Delta T_{\text{CNT}} - \Delta T_{\text{REF}}. \quad (3.2.4)$$

From these two equations, R_{CNT} can be obtained as follows:

$$R_{\text{CNT}} = \left(\frac{\text{VDD}_{\text{CNT}} - V'_{\text{Ref,CNT}}}{C_{\text{CNT}} \times \Delta V'_{\text{CNT}}} \right) \times \left(\frac{R_{\text{REF}} \times C_{\text{REF}} \times \Delta V'_{\text{REF}}}{\text{VDD}_{\text{REF}} - V'_{\text{Ref,REF}}} + T_{\text{DIFF}} \right) \quad (3.2.5)$$

which can be rewritten as

$$R_{\text{CNT}} = E_{\text{MIS}} R_{\text{REF}} + T_{\text{DIFF}} \times \left(\frac{\text{VDD}_{\text{CNT}} - V'_{\text{Ref,CNT}}}{C_{\text{CNT}} \times \Delta V'_{\text{CNT}}} \right) \quad (3.2.6)$$

where E_{MIS} is the error due to the mismatch between the CNT network and the on-chip reference part in the analog front-end circuit, and is expressed as follows:

$$E_{\text{MIS}} = \left(\frac{\text{VDD}_{\text{CNT}} - V'_{\text{Ref,CNT}}}{\text{VDD}_{\text{REF}} - V'_{\text{Ref,REF}}} \right) \left(\frac{C_{\text{REF}}}{C_{\text{CNT}}} \right) \left(\frac{\Delta V'_{\text{REF}}}{\Delta V'_{\text{CNT}}} \right). \quad (3.2.7)$$

In the Equation (3.2.6), device mismatches cause errors in the values of both the

slope and the offset. These errors cannot be predicted, and thus the raw value of the digital output code of the ROIC need to be calibrated to obtain correct values of R_{CNT} . Test cell #3, which is described earlier, it used for this calibration which is performed as follows: First, the row and column selection digital codes are set to select the test cell #3. Second, the value of R_{REF} is set by selecting the code that corresponds to test cell #3. Third, R_{CNT} is set by connecting an external resistor of the appropriate value between the ROIC core and the inner metal region of test cell #3. Fourth, the ROIC is operated and the digital code T_{DIFF} is recorded. By repeating these steps, a table relating T_{DIFF} to R_{CNT} can be obtained. This table can subsequently be used to calibrate the ROIC's digital code to values of R_{CNT} .

3.2.4.2 Quantization Error and Noise

The quantization error in the ROIC is determined by these factors: the clock frequency, which determines the TDC's resolution; and the regulating voltage and gain of the time signal generator. Equation (3.2.4) can be modified to include the quantization error as follows:

$$T_{DIFF} = \frac{R_{CNT,Real} \times C_{CNT,Real} \times \Delta V'_{CNT}}{VDD_{CNT} - V'_{Ref,CNT}} - \frac{R_{REF,Real} \times C_{REF,Real} \times \Delta V'_{REF}}{VDD_{REF} - V'_{Ref,REF}} + Q \quad (3.2.8)$$

where the subscript 'Real' indicates a real value to be measured after the chip has been fabricated, and Q is the quantization error. Before calibration, the value of R_{CNT} has to be

calculated using design values which is indicated with the subscript ‘Designed’, as follows:

$$R_{\text{CNT,Calculated}} = R_{\text{REF,Designed}} + T_{\text{DIFF}} \times \left(\frac{V_{\text{DD,CNT}} - V_{\text{Ref,CNT}}}{C_{\text{CNT,Designed}} \times \Delta V_{\text{CNT}}} \right) \quad (3.2.9)$$

where the subscript ‘Calculated’ refers to a value measured by the ROIC, $V_{\text{Ref,CNT}} = V_{\text{Ref3}}$ and $\Delta V_{\text{CNT}} = V_{\text{Ref2}} - V_{\text{Ref1}}$. Combining Equations (3.2.8) and (3.2.9), it can be obtained that

$$R_{\text{CNT,Calculated}} = R_{\text{REF,Designed}} - E_1 R_{\text{REF,Real}} + E_2 R_{\text{CNT,Real}} + Q \times \frac{V_{\text{DD,CNT}} - V_{\text{Ref,CNT}}}{C_{\text{CNT,Designed}} \times \Delta V_{\text{CNT}}}$$

$$\text{where } E_1 = \left(\frac{V_{\text{DD,CNT}} - V_{\text{Ref,CNT}}}{V_{\text{DD,REF}} - V'_{\text{Ref,REF}}} \right) \left(\frac{C_{\text{REF,Real}}}{C_{\text{CNT,Designed}}} \right) \left(\frac{\Delta V'_{\text{REF}}}{\Delta V_{\text{CNT}}} \right) \quad (3.2.10)$$

$$\text{and } E_2 = \left(\frac{V_{\text{DD,CNT}} - V_{\text{Ref,CNT}}}{V_{\text{DD,CNT}} - V'_{\text{Ref,CNT}}} \right) \left(\frac{C_{\text{CNT,Real}}}{C_{\text{CNT,Designed}}} \right) \left(\frac{\Delta V'_{\text{CNT}}}{\Delta V_{\text{CNT}}} \right).$$

Under perfect calibration, $E_1=1$, $E_2=1$, $R_{\text{REF,Real}}=R_{\text{REF,Designed}}$, and the simplified equation is obtained:

$$R_{\text{CNT,Calculated}} = R_{\text{CNT,Real}} + \gamma Q, \text{ where } \gamma = \frac{V_{\text{DD,CNT}} - V_{\text{Ref,CNT}}}{C_{\text{CNT,Designed}} \times \Delta V_{\text{CNT}}}. \quad (3.2.11)$$

Now the quantization error can be minimized by minimizing γ . The value of $V_{\text{DD,CNT}}$, $V_{\text{Ref,CNT}}$ and ΔV_{CNT} cannot be chosen arbitrarily because of the limited operation range of the ROIC. This leaves C_{CNT} ($=C_{\text{REF}}$) as the most useful design parameter. In this case, it should be considered that the extent to which C_{CNT} can be varied is also limited, since the value of the capacitor is directly related to the area that it occupies on the chip. And the noise should also be considered when the value of C_{CNT} is selected.

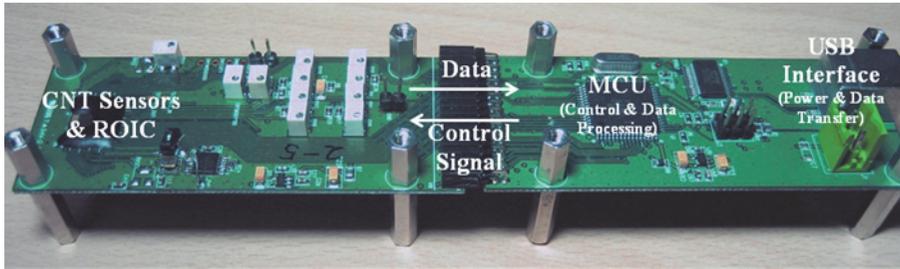


Fig. 3.2.11 CNT sensor board.

3.2.5 SYSTEM ARCHITECTURE

For measurement, the architecture was implemented onto a CNT sensor board as shown in Fig. 3.2.11. Its main components are the CNT ROIC, a micro-controller unit (MCU) and a USB interface. The ROIC is mounted on the board after deposition of the CNT on its die. The MCU sets the values and timing of the INIT, RESET, ROWSEL[0:2], COLSEL[0:3] and REFRSEL[0:3] signals. The digital data from the ROIC is sampled and stored by the MCU, which can transfer it to a PC over a USB interface, or directly calculate the resistance of the CNT network. All the components on this board are powered by the USB connection. The form factor of the ROIC section of the board is 35mm by 87mm, and the remainder occupies an area of 35mm by 80mm. The shape and size of the PCB were determined by the diameter of the measurement system and are not critical parameters.

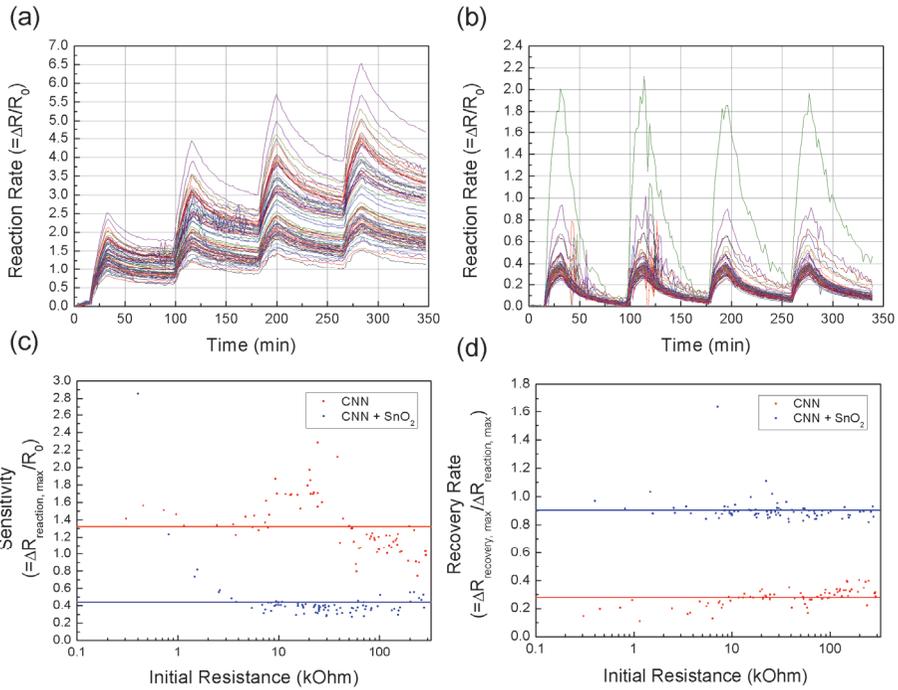


Fig. 3.2.12 (a) Response of the CNT-network cells to 1000ppm of NH₃ at 100°C: individual reaction rates of 77 cells. (b) Response of CNT-SnO₂ network cells to 1000ppm of NH₃ gas at 100°C: individual reaction rates of 83 cells. (c) Distribution of the sensitivity of the CNT-network cells and the CNT-SnO₂ network cells. (d) Distribution of the recovery rates of the CNT-network cells and the CNT-SnO₂ network cells.

3.2.6 MEASUREMENT AND RESULTS

The NH₃ sensing experiments were carried out at 100°C using the chamber shown in Fig. 3.2.4. The response of the CNT cells was measured over five cycles, each consisting of two phases: a reaction phase during which the 1000ppm NH₃ is added to the air flowing over the CNT network cells, and a second recovery phase during which CNT network cells are washed by unadulterated air. Operation of the ROIC was started about

15 minutes before the 2nd cycle, to allow time for initialization and stabilization. The duration of each reaction phase was approximately 15 minutes, and the recovery phase lasted around 60 minutes.

Fig. 3.2.12 shows the measured response of the CNT-network cells connected to the ROIC and mounted on the sensor board. The reaction rate $\Delta R/R_0$ is the change in resistance of each CNT-network cell divided by its initial resistance. Fig. 3.2.12(a) shows reaction rates of 77 CNT-network cells. The results from the remaining 48 cells were ignored due to excessive instability and noise. Fig. 3.2.12(a) indicates that most of the CNT network cells operate as expected, and that their resistance increases when NH_3 is introduced into the reaction chamber. However, there is a nontrivial drift that severely inhibits operational capabilities of this sensor, and suggests the network will have a short lifetime.

Therefore, using the SnO_2 decorated CNT processes discussed in section 3.2.2, modified sensing cells are fabricated. Fig. 3.2.12(b) shows the response of these SnO_2 -CNT network cells to exposure of 1000ppm of NH_3 gas at 100°C . In this case, 83 cells operate correctly with better performance and less deterioration from stage to stage. Figs. 3.2.12(c) and 3.2.12(d) shows the distribution of sensitivity and recovery rates, calculated using record-cycle data, across the sensors at 100°C ; normalized to the initial cell resistances. The SnO_2 -CNT network cells have a more uniform distribution than the plain CNT-network cells, the sensitivity of most of the cells lies near the average, except for

some low-resistance cells. Although the magnitude of the sensor responses is not constant, the recovery rates of the SnO₂-CNT-network cells are not only uniform, but also significantly better than the plain CNT. This suggests that ratios between the amounts of gas taken up and then released by the CNT networks are almost constant within a stage, but can vary from stage to stage. Increasing the temperature improves sensitivity, as it would be expected because of the higher activation energy. These results show how multi-cell networks not only achieve more reliable results, but also yield more information about the mechanisms operating in their cells.

CHAPTER 4

CONCLUSIONS

In this study, several methods were invented and verified by the silicon for the readout of CMOS-integrable bio-chemical sensors. For the detecting of signals from capacitor-type sensors, the scheme using charge amplifier has been invented and developed. For the detecting of signals from resistor-type sensors, the scheme using current-mode detection has been invented and developed.

In the first study for the readout of capacitive sensors [1.2.1], a cost-effective CFC circuit was proposed which uses a small number of components. By accumulating the charges produced by repetitive charge integration, the difference between two capacitances can be converted to an output frequency with good linearity. Experimental results showed that the circuit has a conversion gain of 6.8293kHz/fF, which makes it possible to detect small changes in differential capacitance.

In the second study for the readout of capacitive sensors [1.2.2], an enhanced-

accuracy capacitance-to-frequency converter for the capacitive sensors has been described, which is aimed at monitoring biomolecular reactions. The proposed CFC directly converts a capacitive difference of the sensor into a pulse frequency of a single pulse stream. By selecting pulses from a clock signal, a wide dynamic range of output frequencies has been achieved. Compared to about 6% with the prior compensation technique, the accumulation of residual charges achieves sensing accuracy as good as 0.13%. The CFC has a simple structure and only requires an active area of 0.056mm^2 in $0.35\mu\text{m}$ 2P4M CMOS technology.

In the third study for the readout of capacitive sensors [1.2.3], an interface circuit for capacitive sensors was presented which incorporates a first-order DSM and an SAR-CDC. The DSM only deals with a capacitive difference between sensor capacitors, and thus can read a capacitive difference from -0.5pF to $+0.5\text{pF}$, with a resolution as fine as 0.49fF . The sampling frequency of this circuit is 1MS/s with an OSR of 128. The SAR-CDC measures the initial offset of the capacitive sensor, and a set of capacitors selected by that circuit compensates for the offset. Then, the zero point of the interface circuit is calibrated. This procedure is automatically conducted by controlling only two digital signals. The SAR-CDC can read the offsets from -2pF to $+2\text{pF}$ with a resolution of 31.25fF . By employing simplified architectures for the DSM and SAR-CDC and letting them share an op amp, an circuit active area as small as 0.048mm^2 has been achieved. The measured power consumption was 1.44mW with a 3.3V supply.

In the first study for the readout of resistive sensors [1.2.4], a low-power CNT bio-sensor ROIC has been proposed which is based on a current-input continuous-time $\Delta\Sigma$ ADC with wide dynamic range. This design incorporates a DR extension scheme into the current-mode circuit, allowing it to achieve extended DR using only a simple ADC with a moderate SNR. This design was verified to be effective in sensor applications where a wide dynamic range is required and in which the design complexity and power consumption must be low for compatibility with large-scale CNT bio-sensor arrays.

In the second study for the readout of resistive sensors [1.2.5], a sensor system has been successfully constructed in which an array of CNT network cells was combined with an ROIC on a single die. The ROIC combines a counter-based coarse TDC with a DLL-based fine TDC to enhance resolution and reduce power consumption. An analog front-end circuit with simple regulation loops and capacitors generates a time-difference signal which is proportional to the difference between the resistance of a reference resistor and that of the CNT sensor. Using the proposed system, the limitations of bare CNT networks has been demonstrated and it has also been shown that how SnO₂-CNT networks can improve sensor lifetime and response sensitivity. The implementation of multiple SnO₂-CNT network cells on a single chip indicates a clear path towards a low-cost and reliable gas sensor for ubiquitous sensor network applications.

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한글초록

본 연구에서는 CMOS와 집적 가능한 생화학센서의 신호검출에 적합하도록 여러가지 인터페이스회로를 고안하고 CMOS 상에서 IC로 검증하였다. 많은 경우에 있어서, 집적 가능한 용량성 센서의 경우에는 MEMS 공정을 통해서 제작이 되고, 집적 가능한 저항성 센서의 경우에는 나노-와이어를 활용해서 제작이 된다. 이처럼, 집적을 통한 센서의 고밀도화 가능성을 십분 활용하기 위해서는 어레이 구조가 매력적이라 할 수 있다. 용량성 센서의 신호를 검출하기 위해서는 전하증폭기를 활용한 일련의 방법들을 제안하였고, 저항성 센서의 신호를 검출하기 위해서는 전류-모드 검출을 활용한 일련의 방법들을 제안하였다. 또한 두 가지 모두의 경우에 있어서, 어레이 구조에서 발생할 수 있는 센서 초기값의 넓은 산포를 보상할 수 있도록 동적 영역을 확장시키는 방법을 구현하고자 하였다.

용량성 센서의 검출을 위한 첫 번째 연구에서는, 함께 집적될 차동 용량 센서에 적합하도록 반복적인 전하 적분을 활용함으로써, 복잡도는 낮추면서도 정확도는 높은 CMOS 검출 회로를 제안하였다. 두 번째 연구에서는, 적분 캐패시터를 방전시킬 때 잔여 전하를 보존함으로써, 정확성이 더욱 향상된 검출 회로를 제안하였다. 세 번째 연구에서는, 낮은 복잡도는 유지하면서도 해상도를 향상시키기 위해 델타-시그마 변조 기법을 활용하면서, 캐패시터의 초기값

을 보상함으로써 검출 가능한 동적 영역의 손실을 줄이는 회로를 제안하였다.

저항성 센서의 검출을 위한 첫 번째 연구에서는, 배열 구조의 CNT 센서에 적합하도록 동적 영역 확장 기능 및 전류-모드 델타 시그마 변조 기법을 활용한 검출 회로를 제안하였고, 두 번째 연구에서는 TDC를 활용한 회로를 제안함과 동시에 CNT-SnO₂ 센서망을 구현된 CMOS 회로상에 함께 집적하여, 통합된 시스템으로 NH₃ 가스 검출을 성공적으로 시행하였다.

주요어: 인터페이스 회로, CMOS, 생화학적 센서, 용량성 센서, 저항성 센서.

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