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공학박사 학위논문

Advanced Device Architectures for Organic Logic Elements and Nonvolatile Memory Cells

유기 논리 소자와 비휘발성 메모리를 위한

고성능 소자 구조

2013 년 2 월

서울대학교 대학원

공과대학 전기컴퓨터공학부

김민회

(Min-Hoi Kim)

Advanced Device Architectures for Organic Logic Elements and Nonvolatile Memory Cells

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이 논문을 공학박사 학위논문으로 제출함

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Abstract

Advanced Device Architectures for Organic Logic Elements and Nonvolatile Memory Cells

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Organic electronics has attracted much attention due to their low-cost, large-area, and flexible electronic device applications such as flexible displays, radio frequency identification tags, and sensor sheets. Especially, numerous approaches for the high performance organic thin-film transistors (OTFTs) have been studied due to their driving and switching capability. Recently, for the commercialization of the OTFTs, not only a single device but electronic functional blocks which consist of various types of OTFTs are studied. One of the great ways to obtain both high performance of single device and integration of various OTFTs is to design new device architectures. In order to fabricate new device structures, new patterning process is required, since the

conventional patterning process such as photolithography cannot be used for organic materials due to the damage of organic materials during photolithography.

In this thesis, new device physics and process technology of the advanced device architectures are presented for the enhancement of the performance of the single OTFT and the realization of the electronic functional blocks. Especially, it is presented that the underlying physical mechanism comes from the interface between the gate insulator and the organic semiconductor. First, the general overview of the organic electronics and the operation principles of the OTFTs are introduced. It is demonstrated how the parameters of the OTFTs, organic inverters, and ferroelectric OTFTs affect the device performance.

In the viewpoint of the single device, it is presented how device architectures have an influence on the performance of the OTFTs. In order to obtain saturated high drain current at low voltage, the chevron gate configuration is designed and fabricated. Furthermore, the short channel effect and current modulation is physically analyzed. For the high performance OTFTs with the n-type polymer semiconductor, the dual-gate architecture is introduced. The dual-gate architecture allows the threshold voltage and mobility to be controlled by the biasing the counter gate electrode.

Next, combination of the two different types of the OTFTs for the novel electronic functional blocks is demonstrated. The interface between First, the control mechanism for interfacial charges in an OTFT by the introduction of a surface polarized layer (SPL), which generates a transverse dipolar field, is

demonstrated. The concept of such SPL enables to develop a high noise-margin full-swing unipolar inverter on a single substrate. The transverse dipolar field of the SPL of a fluorinated polymer which is placed between the organic semiconductor and the gate insulator plays an essential role in the accumulation of holes at the interface due to the surface dipoles of the fluorinated polymer. Owing to the interfacial holes, the OTFT with the SPL operates in a depletion mode and its magnitude lies between the on-current and off-current of a conventional OTFT with no SPL. This directly allows the high noise-margin and the full-swing capability of an organic unipolar inverter with zero gate load OTFT.

Second, paraelectric/ferroelectric bilayer architectures in ferroelectric OTFT for nonvolatile memory array are demonstrated. The paraelectric buffer layer (PBL) on the ferroelectric layer plays an essential role in screening the electric field of the ferroelectric dipole and reducing the roughness of the insulator. It is found that the OTFTs with the bilayer structure exhibit high switching on-off current ratio and low memory on-off current ratio. Through the selective formation of the bilayer structure, the ferroelectric memory OTFTs are integrated with the selection OTFTs having the bilayer structure. Through this configuration, ferroelectric memory array without crosstalk between memory cells and voltage-readable multistate ferroelectric memory cell are demonstrated.

In conclusion, through this thesis, it is presented that the advanced device architectures enhanced the performance of the single device and realized the electronic functional blocks. Approaches of increasing the drain current and

controlling the threshold voltage, introduced here, are expected to provide a basis for realizing many applications of the OTFTs. Moreover, the device physics and the integration technique for the organic inverter and ferroelectric circuit will provide a platform for the organic logic elements and nonvolatile memory cells.

Keywords: organic thin-film transistor, interfacial interactions, chevron gate configuration, dual gate, organic inverter, ferroelectric nonvolatile memory

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Chapter 1. Introduction

1.1 Organic Electronics

The era of the ubiquitous world in which individuals are able to connect to on-line network anyplace and anytime has been coming. This trend requires a huge number of electronic devices for wireless connection and novel display. Therefore, the fabrication compatibility to low cost and large-area process is needed. Organic electronics has great potential for satisfying these technological requirements. Organic electronics is a branch of electronics dealing with carbon-based conducting and semiconducting materials. The organic electronic devices are attractive because they can take advantage of organic materials such as light weight, low-cost, and capability of large-area, flexible device fabrication [1]. Recently, organic light-emitting diode (OLED), one of the examples of the organic electronic devices, was already commercialized. Organic thin-film transistor (OTFT) and organic photovoltaic cell (OPV) are widely expected to appear next in consumer products. Among these organic electronic devices, OTFTs have attracted much attention due to their switching and driving capability.

In contrast to the charge transport in inorganic Si semiconductor, the charge transport in organic material is generally the hopping-based transport, in which mobility increases with increasing temperature. Exceptionally, in organic single crystals, the band-like transport is observed. That is, the negative temperature dependence of mobility is shown [2]. However, since

most of the organic materials are disordered and partially ordered, the mobility of carrier is limited. Due to this low performance, the applications of the organic electronic materials head for optoelectronic application or low-cost and low-performance circuits.

For high performance OTFTs and organic circuits, stability and self crystallinity of the organic semiconducting materials are basic requirements. Together with these material properties, geometric factors such as channel length (L), channel width (d), and insulator thickness (d), interface between organic semiconductor and gate insulator or organic semiconductor and source/drain electrode, and fabrication process should be carefully considered. Geometry, interface, and fabrication process of OTFTs are significantly affected by the device architecture. Therefore, together with the development of the stable organic semiconducting materials with high crystallinity, new device architecture for high performance OTFTs are strongly required.

1.2 Organic Thin-Film Transistor

1.2.1 Operation of Organic Thin-Film Transistor

Organic thin-film transistors (OTFTs) have been expected to be promising devices due to large-area, low-cost, and flexible electronics for applications in displays, sensors, and memories [3-5]. The first OTFT with polyacetylene as a organic semiconductor was fabricated by F. Ebisawa et. al. [6]. The mobility of this device is very low. However, owing to the numerous technological approaches, the mobility had been progressively increased and finally exceeded 1 cm^2/Vs in 1997 [7].

As shown in Fig. 1.1, the device structure of the OTFT is classified three. Figs. 1.1(a) and (b) show bottom-gate structure where the gate electrode is below the semiconductor. Top-gate structure is shown in Fig. 1.1(c). Because most organic semiconductors are easily vulnerable during the fabrication process, the formation of organic semiconductors on the insulator is much convenient than top-gate structure where the gate insulator is formed on the semiconductor. However, top-gate structure exhibits more potential for the stable operation owing to its self-encapsulation of organic semiconductor by the gate insulator and gate electrode. According to the fabrication procedure of organic semiconductors and source/drain electrodes, top contact structure (Fig. 1.1(a)) and bottom contact structure (Fig. 1.1(b)) are distinguished. In the bottom contact structure where source/drain electrodes are deposited on

the insulator; the electrodes are easily patterned by means of conventional photolithography. This cannot be used in top-contact structure, because organic semiconductors are damaged by the solvent and ultra-violet (UV) during photolithography. However, in the viewpoint of contact resistance, top contact shows lower resistance than bottom contact.

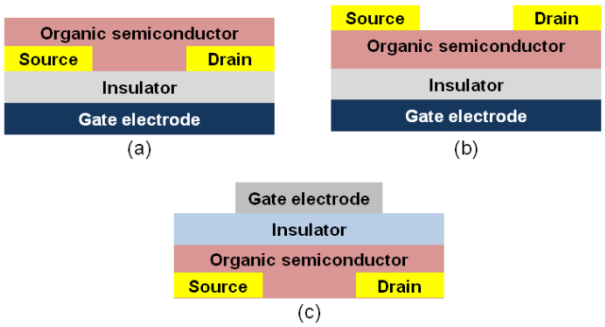

Figure 1.1 The architectures of OTFTs. (a) bottom-gate bottom contact, (b) bottom-gate top contact, and (c) top-gate bottom contact

Figure 1.2 shows the transfer curve and the operation parameters of an OTFT. On-off current ratio is the ratio of the maximum drain current (I_{on}) and the minimum drain current (I_{off}). Threshold voltage (V_{th}) is the intersection of the extrapolating line of the square root of the drain current and lateral axis. Turn-on voltage (V_{on}) is the gate voltage where the drain current begins to increase exponentially. Subthrehold slope (SS) is the slope of the logarithmic value of the drain current.

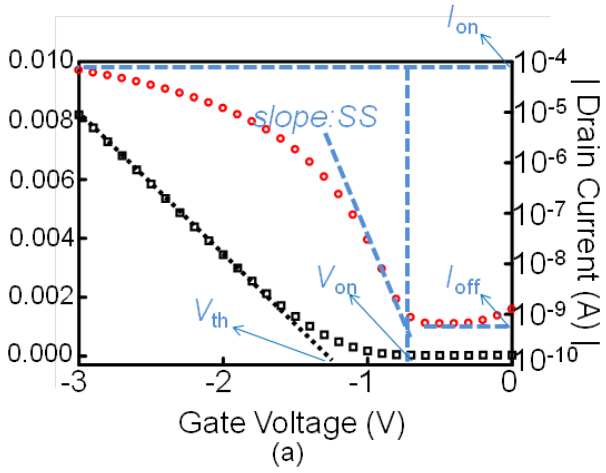

Figure 1. 2 A transfer curve and operation parameters of an OTFT.

For the p-type OTFT, the drain current in the linear regime where drain voltage (V_D) is smaller than the difference between gate voltage (V_G) and threshold voltage to negative direction ($V_D > V_G - V_{th}$) and $V_G < V_{th}$ is

$$I_D = \frac{W}{2L} C_i \mu [(V_G - V_{th}) V_D - \frac{1}{2} {V_G}^2] \quad (1.1)$$

Where W and L are the width and length of the channel, C_i is the intrinsic capacitance of the gate insulator, and μ is the mobility. The drain current in the saturation regime where $V_D > V_G - V_{th}$ is

$$I_D = \frac{W}{2L} C_i \mu (V_G - V_{th})^2 \quad (1.2)$$

For large drain current, L should be short, μ should be high, and C_i should be high. For low voltage operation, C_i should be high, that is, the dielectric constant and thickness of an insulator (d) should be high and thin, respectively, because $C_i = \varepsilon_0\varepsilon_r/d$.

1.2.2 Organic inverter

An inverter is the basis of the design for more complicated electronic logic circuits. When input voltage (V_{in}) is high, output voltage (V_{out}) is low, and vice versa. In organic electronic circuits, the unipolar inverters with p-type organic semiconductors are widely used [8-12] due to the deterioration of the n-type semiconductor under ambient environment in air and humidity [13]. Two types of unipolar inverters are shown in Figure 1.3(a). Since the fast operation speed is able to be obtained in a saturation load inverter (left of Fig. 1.3(a)) in spite of the low noise margin and non-full-swing, this inverter is used for high speed circuit. In contrast to the saturation load inverter, the zero gate load inverter (right of Fig. 1.3(a)) shows high noise-margin and full-swing behavior even though the speed is slower than the saturation load inverter. The zero gate load inverter consists of two types of OTFTs, enhanced mode OTFT for a driving transistor and depletion mode OTFT for a load transistor. For p-type OTFTs, the enhanced mode OTFT is the OTFT with negative V_{th} and the depletion mode OTFT is with positive V_{th}. The static characteristics of the zero gate load inverter are shown in the voltage transfer curve (VTC) in Fig. 1.3(b). The trip voltage (V_{trip}) is the value of V_{in} where $V_{in} = V_{out}$ in VTC. The maximum gain is defined as the maximum values of dV_{out}/dV_{inmax}. The noise margins at the high level (NM_H) = $V_{OH} - V_{IH}$ and at the low level $NM_L = V_{IL} - V_{OL}$, where the symbols are defined in Fig. 1.3(b). While high gain is required for the amplification of the electrical signal, for the stable operation, high noise-margin is needed. For this zero gate load inverter

with high-noise margin, it is required to integrate the enhanced mode OTFT with the depletion mode OTFT in a single substrate. Because the mode of the OTFT is dominantly affected by the interface between the gate insulator and the organic semiconductor, two different interfaces are should be fabricated in a single substrate. However, it is not easy to fabricate two different interfaces in a single substrate due to the difficulty in patterning polymeric insulators. Therefore, new device architecture which leads two different interfaces is strongly required.

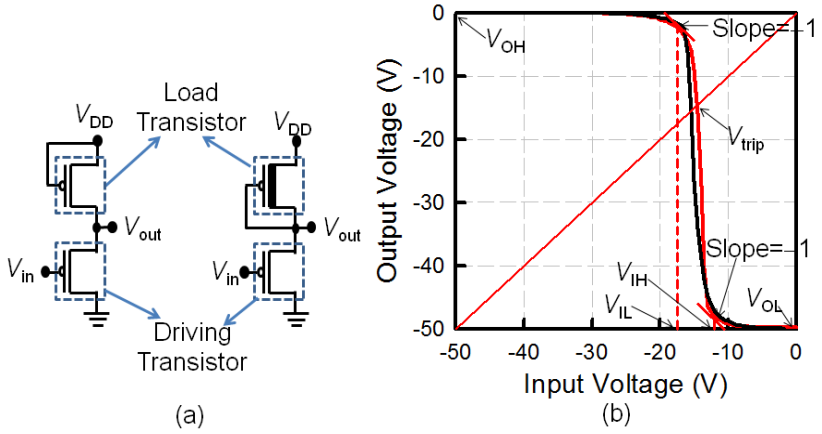

Figure 1. 3 (a) a saturation load unipolar inverter (left) and zero gate load unipolar inverter (right). (b) Voltage transfer curve and parameters of an inverter.

1.2.3 Ferroelectric Organic Thin-Film Transistor

The ferroelectric organic thin-film transistor (FeOTFT) in which a ferroelectric layer is used as an insulator is one of the most promising candidates for the alternative memory device challenging to the inorganic based flash memory due to its excellent properties such as nonvolatile, electrically reversible memory states, and low-cost per a bit [14,15]. Figure 1.4(a) shows the transfer curves of the typical FeOTFT with the p-type organic semiconductor. Clear hysteresis behavior is observed due to the polarization of the ferroelectric insulator. The accumulated charges in the organic semiconductor (Q_P) at low V_D and V_G is

$$Q_P = C_{ferro}(V_G + \frac{P_r}{C_{ferro}} - V_{th}) \quad (1.3)$$

Where C_{ferro} is the capacitance of the ferroelectric insulator and P_r is the remnant polarization of the ferroelectric insulator. When the ferroelectric layer is polarized from bottom to top (negative values of P_r), holes are attracted and accumulated in the organic semiconductor. In this case, I_D is large even at V_G = 0 V, which is the state 1 in Fig. 1.4(a). With the top-to-bottom polarization (positive values of P_r), electrons are attracted but not allowed to be accumulated because the high energy barrier between p-type organic semiconductor and source/drain electrodes prevents electrons to be injected to the organic semiconductor. Therefore, channel current between source and drain electrodes is very low and therefore, leakage current is the main origin of I_D and I_D is very low, which is the state 0 in Fig. 1.4(a). The memory on-off

ratio is the ratio of the drain current in state 1 (I_{D1}) and state 0 (I_{D0}). The stability of the memory states in the FeOTFT are shown in Fig. 1.4(b). The state 1 and the state 0 are clearly retained and distinguished with time.

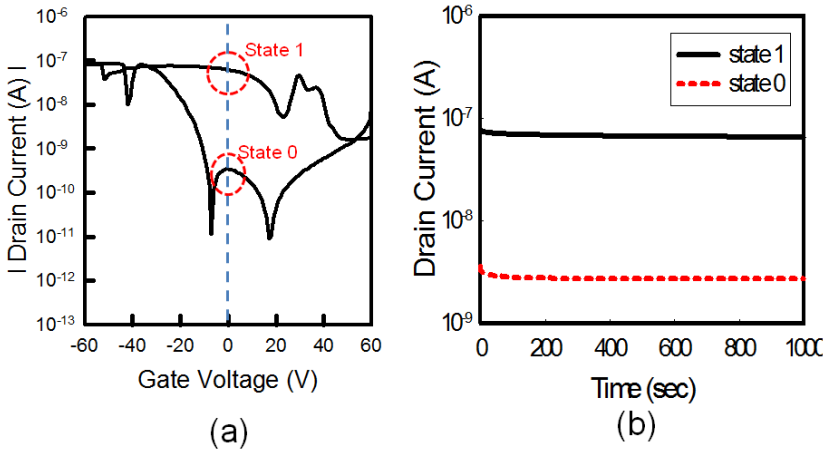

Figure 1. 4 (a) transfer curve of the FeOTFT. State 1 and state 2 represent the states at V_G = 0 V in a forward sweep and a backward sweep. (b) Drain current as a function of time.

In order to store large information, highly integrated ferroelectric memory is required. In this case, for each memory cell, a paraelectric OTFT (POTFT) and a FeOTFT should be integrated. Due to the difficulty in patterning ferroelectric polymer, integration of FeOTFT and POTFT is one of the significant challenges for fabrication of large-information-store memory. Therefore, new device architecture which allows to integrate the POTFTs and the FeOTFTs is needed.

1.3 Outline of Thesis

This thesis contains five chapters including **Introduction** and **Conclusion**. As an introductory part, **Chap. 1** provides the brief introduction of organic electronics and the background and the important key parameters of OTFTs. The general principles and key factors of organic inverters and FeOTFTs are introduced. The motivation of this research on the new device architecture for high performance OTFTs and organic circuits is also introduced.

In **Chapter 2**, the enhancement of the performance of OTFTs in the single device level is introduced. First, it is presented that the a chevron-type (CT) gate configuration of a short channel top-contact OTFT, made of a polymeric edge support together with a thin AlO_X insulator, has large saturated drain current at a low operating voltage. The shape of the polymeric edge support was varied with the thermal treatment and the channel length (L) was self-defined by oblique deposition of metal onto the substrate with the help of the polymeric edge support. Next, in the n-type polymer FETs with dual gate electrodes, how the bias voltage affects the electrical properties is presented. Their electrical characteristics including the hysteresis, the mobility, and the threshold voltage were measured as a function of the sweeping voltage at one gate electrode under the condition that the other gate was floated or biased.

In **Chap. 3** and **4**, the fabrication of organic electronic functional block by modifying the device structure of OTFTs is presented. The control mechanism of the interfacial charges in an OTFT by the introduction of a surface polarized layer (SPL), interfaced with an organic semiconductor is

demonstrated. The SPL generates a transverse dipolar field, which enables to develop a high noise-margin full-swing unipolar inverter on a single substrate. How the transverse dipolar field of the SPL of a fluorinated polymer, placed between the organic semiconductor and a gate insulator, plays an essential role in the accumulation of holes at the interface and the noise-margin of the organic inverter is described. In addition, the effect of the structural modification in OTFT on the realization of the ferroelectric memory array is presented. How the paraelectric buffer layer (PBL) on the ferroelectric layer plays an essential role in screening the electric field of the ferroelectric dipole and roughness of the insulator are described.

Finally, **chap. 5** gives brief summary and some concluding remarks for this thesis.

Chapter 2. Functional Organic Thin-Film Transistor

2.1 Short Channel OTFTs for High Drain Current

2.1.1 Introduction

Although the performance of the OTFTs have been drastically improved over the past decades, low drain current limited intrinsically by the charge carrier mobility is still one of the problems encountered for practical applications such as displays [16] and radio frequency identification tags [17]. Therefore, it is very important to achieve high drain current of the OTFT for organic circuits requiring low operating voltage and low power consumption [18].

Considering that the drain current of the OTFT is inversely proportional to the channel length (L), the scaling down of L will effectively increase the drain current. Moreover, a short channel is needed for further high-speed applications because the cut-off frequency is proportional to $1/L^2$ [19]. For constructing a short channel, a bottom-contact OTFT structure is simpler than a top-contact structure since the channel length on a micrometer scale can be easily defined prior to the formation of an organic semiconducting layer using a high-resolution patterning technique such as an electron-beam lithography

[20] or an excimer laser exposure [21]. From the viewpoints of the electrical properties such as the contact resistance between an organic semiconductor and source/drain electrodes, a top-contact OTFT structure is desirable. In the top-contact case, the channel length is typically about 40μm, which is limited by the resolution of a shadow mask [22]. Below the channel length of 40μm, an elastomeric stamping technique or a membrane mask technique has been employed [23, 24]. Recently, a step-edge structure [25] and a three-dimensional structure [26] have been proposed to fabricate short channel top-contact OTFTs. Note that both of them yield no saturation of the output curve in the entire range of the operation voltage, and thus the integration of the OTFTs into electronic circuits is limited. In principle, for a typical dielectric constant of 3–4, the thickness of a gate insulator should be less than a tenth of *L* to obtain the saturation behavior of drain current since the electric field from a gate electrode to a channel should be strong enough to ignore a short channel effect [27]. This means that a short channel top contact structure having a thin insulator is required for large saturated drain current of the OTFT.

In this chapter, a chevron-type (CT) gate configuration of a short channel top-contact OTFT, made of a polymeric edge support together with a thin AlOx insulator, which has large saturated drain current at a low operating voltage is demonstrated. In our CT gate configuration, the shape of the polymeric edge support was varied with the thermal treatment. *L* was self-defined by oblique deposition of Au onto the substrate with the help of the polymeric edge support. For large drain current, *L* was optimized by

controlling the geometric condition of the polymeric support. In order to obtain the saturation behaviour of the drain current, the dielectric properties of AlOx were investigated as a function of the layer thickness through the O_2 plasma treatment.

2.1.2 Chevron gate configuration

The geometrical structure of a polymeric edge support and the fabrication steps of the CT-OTFT are shown in Fig. 2.1. The polymeric edge support shown in Fig. 2.1(a) was produced using a photoresist (AZ Electronic Materials, AZ1512) which was spin-coated on a glass substrate and then patterned by photolithography. Six types of the polymeric edge supports were prepared and baked initially at 110 ◦C for 10 min. Except for one type, the remaining five types were subsequently baked at 125 ◦C, 140 ◦C, 155 ◦C, 170 ◦C and 185 ◦C for 1 min, respectively, to produce different edge angles as shown in Fig. 2.1(b). A 50 nm thick Al layer was thermally deposited onto the edge support on the substrate as shown in Fig. 2.1(c). The Al layer was then placed under O_2 plasma for 7 min to self-grow the AlO_X insulator whose optimal thickness was determined from the MISM capacitor above, as shown in Fig. 2.1(d). Pentacene is thermally deposited onto the AlO_X insulator under the condition that the substrate was inclined at an angle of α = 25◦ as shown in Fig. 2.1(e). Such inclination of the substrate produces the symmetric, uniform deposition of pentacene in the CT gate configuration. The thickness of the pentacene layer was 50 nm. In 10^{-6} Torr, The Au source and drain electrodes were thermally deposited on the pentacene film at an inclination angle of β = 55◦ for the substrate as shown in figure Fig. 2.1(f). The thickness of Au was 60 nm.

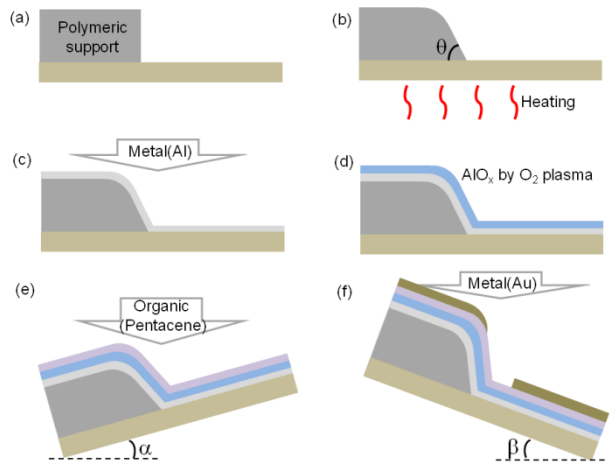

Figure 2. 1 Fabrication processes of the CT-OTFT: (a) a polymeric edge support made of a photoresist, (b) thermal treatment of the polymeric edge support, (c) metal deposition for a gate electrode, (d) O2 plasma treatment for a self-grown gate insulator, (e) organic semiconductor deposition at the inclination angle of α for an active layer, (f) metal deposition at the inclination angle of β for source and drain electrodes.

The channel width (W) was fixed to be 1mm, but the channel length (L) varies with both the shape and the angle of the edge support in addition to the inclination angle (β). The oblique deposition of Au in the CT gate configuration allows us to self-define the channel length (L).

The effect of the thermal treatment on both the shape and the edge angle of the polymeric support made of a photoresist (AZ1512) is described. The FE-SEM images shown in Fig. 2.2(a), (b), (c) and (d) correspond to the cross-

sectional views of four polymeric edge supports that were thermally treated at different temperatures of 110 ^{O}C, 125 ^{O}C, 140 ^{O}C and 155 ^{O}C.

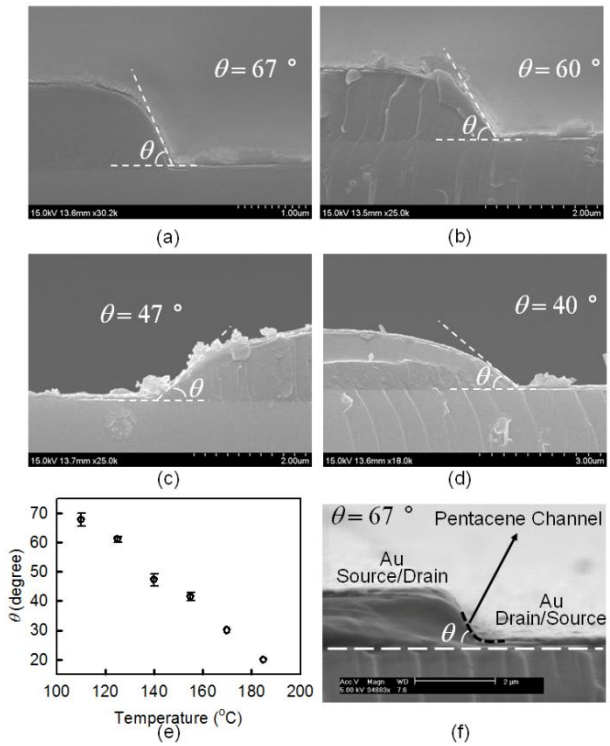

Figure 2. 2 FE-SEM images of four kinds of polymeric edge supports treated thermally at (a) 110 ^{O}C, (b) 125 ^{O}C, (c) 140 ^{O}C and (d) 155 ^{O}C. (e) The edge angle θ as a function of the thermal treatment temperature. The error bars are the standard deviation of five different samples from two batches. For the thermal treatment of 170 and 185 ^{O}C, one sample was used. (f) The FE-SEM image of a fabricated CT-OTFT with a polymeric edge support treated at 110 ◦C. The angle θ denotes the edge angle between the side of the polymer edge support and the substrate surface, a black dashed line represents the pentacene channel, and a white dashed line represents the substrate surface. The cross-sectional images of our CT-OTFTs were obtained with a field emission-scanning electron microscope (FE-SEM) (Hitachi, S-48000).

Since the photoresist undergoes deformations above a hard-baking temperature (110 ^{o}C) [28], the geometric shape of the polymeric edge support becomes rounded with increasing the thermal treatment temperature beyond 110 ^{o}C. Thus, the edge angle (θ) between the side of the polymeric support and the substrate surface was decreased and the edge shape became substantially rounded at high temperatures as shown in Fig. 2.2(e). The error bars in Fig. 2.2(e) represent the standard deviation of five samples from two batches and show the reproducibility and the controllability of the polymeric edge angle by the thermal treatment. The edge angles of the six polymeric edge supports treated at different temperatures of 110, 125, 140, 155, 170, and 185 ◦C were about 67◦, 60◦, 47◦, 40◦, 30◦ and 20◦, respectively. Figure 2.2(f) shows the cross-sectional FE-SEM image of our CT-OTFT with a polymeric edge support thermally treated at 110 ^{o}C. It is clear that source and drain electrodes are well separated by oblique deposition of Au, producing the self-defined *L* due to the presence of the polymeric edge support. The mean free path of the Au during thermal deposition process is 5.1 m using the below equation,

$$\lambda = \frac{kT}{P\sigma^2\sqrt{2}}$$

Here, λ, *k*, *T*, *P*, and σ are mean free path, Boltzmann constant, temperature, pressure, and diameter of molecule, respectively. During thermal deposition, the distance from Au boat to samples is about 30 cm which is much smaller than mean free path of Au, and thus the separation of Au is guaranteed. *L* of

the CT top-contact OTFT, denoted by a black dashed line in Fig. 2.2(f), was measured to be about 1.7μm.

2.1.3 Thin self-grown AlO_X

The insulating properties of various AlOx layers in both metal(Al)–insulator(AlOx)–metal(Au) (MIM) capacitors and metal(Al)–insulator (AlOx)–semiconductor (pentacene)–metal(Au) (MISM) capacitors. A total of 45 samples with 50 nm thick Al were used in the MIM. Five sets where each set consists of nine samples were exposed to O_2 plasma for 0.5 min, 1 min, 3 min, 5 min and 7 min, respectively. In the MISM case, a total of 15 samples with 50 nm thick Al were used. Five sets where each set consists of three samples were similarly exposed to O_2 plasma as the MIM case. Under O_2 plasma, a very thin AlO_X insulator (about 5 nm) was known to be self-grown on the top of the remaining Al electrode [29,30]. In all cases, the surface roughness of AlO_X was about 3.4 ± 0.3 nm. The O_2 plasma treatment was performed at a power of 75W under a pressure of 0.1 Torr with a flow rate of 100 sccm. For the MISM, thermal deposition of pentacene (Sigma Aldrich, used as purchased) was carried out onto the AlOx insulator at a deposition rate of 0.05 nm s^{-1} at 10^{-6} Torr. The pentacene thickness was varied to examine the current leakage mechanism. As a top electrode in either the MIM and the MISM, a 60 nm thick Au layer was thermally deposited on the top of the AlO_X layer.

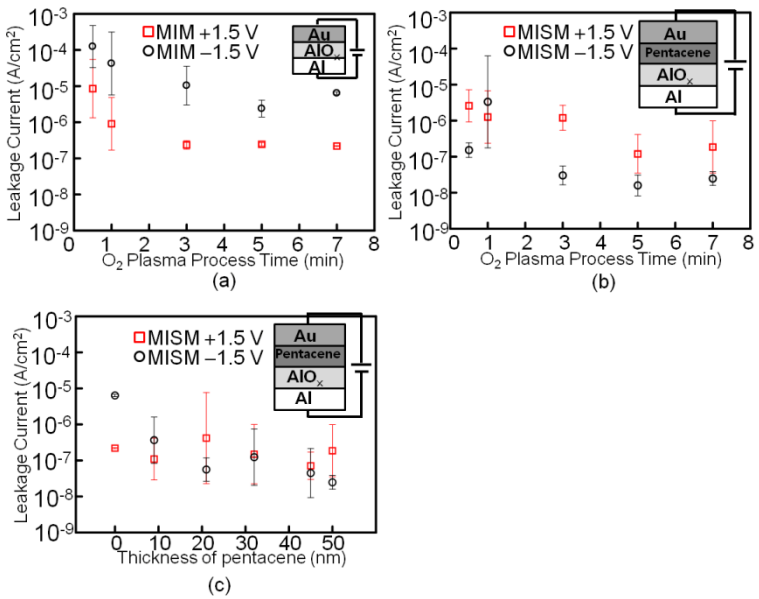

Figure 2. 3 (a) Leakage current density of MIM capacitors as a function of the O_2 plasma treatment time. The error bars represent the logarithmic standard deviation of nine different samples. (b) Leakage current density of MISM capacitors as a function of the O_2 plasma treatment time. (c) Leakage current density of MISM capacitors as a function of the thickness of pentacene. The error bars in (b) and (c) represent the logarithmic standard deviation of three different samples. Squares and circles denote leakage current density at + 1.5 V and that at − 1.5 V, respectively.

It is discussed how the O_2 plasma treatment influences the current leakage in the AlO_X insulator. In the case of the MIM where the top and bottom electrodes are different, the magnitude of the leakage current should depend on the direction of an external electric field [29]. The leakage current densities in the MIM capacitors were measured as a function of the O_2 plasma treatment time at a fixed voltage of $\pm$ 1.5 V (or an electric field of about±3

MV/cm) in Fig. 2.3(a). They decrease monotonically with increasing the O_2 plasma treatment time and become nearly constant above a few minutes of the O_2 plasma treatment. Note that beyond a certain thickness (about 5 nm) of the AlOx insulator, the current leakage is essentially blocked [30]. The leakage current density for a positive electric field (from the Au electrode to the Al electrode) and that for a negative electric field were 2×10^{-7} Acm^{-2} and 6×10^{-6} Acm^{-2}, respectively. The asymmetry in the current leakage results from a built-in electric field from Al to Au which is attributed to the Fermi level alignment between the two electrodes. Similar behavior was experimentally observed and theoretically analyzed in the previous works [29,31,32]. In describing the current leakage in a top-contact OTFT, it is more physically reasonable to use a MISM structure than a MIM structure. The leakage current densities in the MISM capacitors were measured as a function of the O_2 plasma treatment time in figure 2(b). They show a decay behavior similar to the MIM case. For the positive electric field, the current density remained almost the same but for the negative electric field, it diminished drastically (about 2×10^{-8} Acm^{-2}). This is due to the hole transport in the pentacene layer which is a p-type semiconductor. For the fabrication of our CT-OTFTs, the O_2 plasma treatment time was chosen to be 7 min for the preparation of the AlO_X layer showing the least current leakage. For understanding the disparity of the leakage current between two polarities of the electric field, the thickness of the pentacene layer in the MISM structure was varied as shown in Fig. 2.3(c). The O_2 plasma treatment time was 7 min. As clearly shown in Fig. 2.3(c), the leakage current at the positive electric field (or the applied voltage of + 1.5 V)

is essentially independent of the thickness of pentacene while the leakage current at the negative electric field shows a decay behavior. This comes from the accumulation or the depletion of the holes in the pentacene layer depending on the polarity of the electric field. As shown in Fig. 2.3(c), the leakage current density in the MISM capacitor with 50 nm thick-pentacene is two orders of magnitude smaller than that in the MIM. This means that the leakage current is reduced when the active region of the pentacene is extended to entirely cover the intersectional areas of both the gate–source and gate–drain like in the CT-OTFT structure as shown in Fig. 2.3(f).

2.1.4 Electrical characteristic of short channel CT-OTFT

Electrical characteristic of short channel CT-OTFT and a conventional lateral top-contact OTFT were evaluated, which was fabricated as a reference device whose channel width and channel length were 1mm and 50μm, defined through a shadow mask, respectively. The electrical characteristics of the CT-OTFTs were measured using a semiconductor parameter analyzer (Hewlett-Packard Co., HP4155A) at room temperature under ambient environment.

Figure 2.4(a) shows the transfer curves of five OTFTs that were fabricated using the polymeric edge supports treated thermally at 110 ◦C, 125 ◦C, 140 ◦C, 155 ◦C and 170 ◦C, respectively, at V_D = −2.5V. The channel lengths were 1.7μm, 1.2μm, 1.0μm and 0.8μm for the polymer supports treated at 110 ◦C, 125 ◦C, 140 ◦C and 155 ◦C, respectively. For the polymeric edge support treated at 170 ◦C, the off-current of the CT-OTFT becomes relatively high (about 30 nA) since the source and drain electrodes are not well defined due to imperfect masking of Au atoms on the pentacene layer during oblique deposition. The drain current at V_G of −3V and the on–off current ratio were shown as a function of the thermal treatment temperature for the polymeric edge support in Figure 2.4(b). The error bars represent the standard deviation of five samples from two batches. From Figure 2.3(e) and 2.4(b), it is clear that the drain current is inversely proportional to the polymer edge angle (or the channel length). Note that the channel length was achieved as short as 0.8μm in the CT-OTFT. The drain current increases with the treatment temperature. The on–off current ratio was about 10^5.

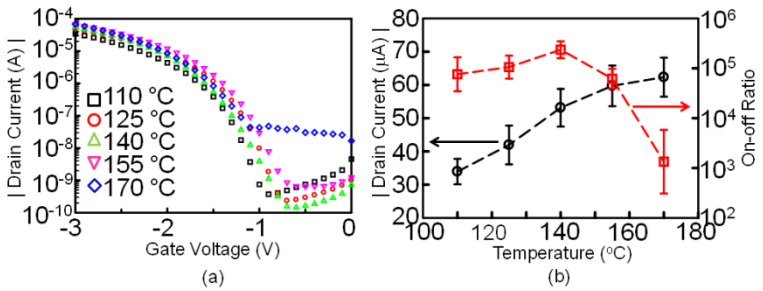

Figure 2. 4 (a) The transfer curves of five different CT-OTFTs. Squares, circles, up-triangles, down-triangles, and diamonds represent the transfer curves for thermal treatment at 110 ◦C, 125 ◦C, 140 ◦C, 155 ◦C and 170 ◦C, respectively. (b) The drain current at $V_G = -3$ V and $V_D = -2.5$ V and the on–off ratio as a function of the thermal treatment temperature. The error bars represent the standard deviation deduced of five different samples from two batches.

As shown in Figure 2.4 (b), the CT-OTFT with the polymeric edge support treated at 170 ◦C shows a low on–off current ratio (less than 10^4) due to less separation of the source and drain electrodes as described above. In describing the relationship between the edge angle (θ) and the inclination angle (β) for self-defining L, the sum of θ and β should be larger than 90◦ which is the critical angle for defining well-separated electrodes. The angle of β was fixed at 55◦. Since θ is smaller than 40◦ for the thermal treatment temperature at 170 ◦C, ($\theta + \beta$) is then just about 90◦. In this case, Au atoms tend to be partly deposited in the channel region during oblique deposition, thereby resulting in a relatively large off-state current on the pentacene surface in the CT-OTFT. This surface current reduces the on–off current ratio, which is clearly shown in Figure 2.4(b). No self-masking effect by the

polymeric edge support is expected to define L if the sum of θ and β is not larger than 90◦. Therefore, if β has a different value, θ is limited by this equation.

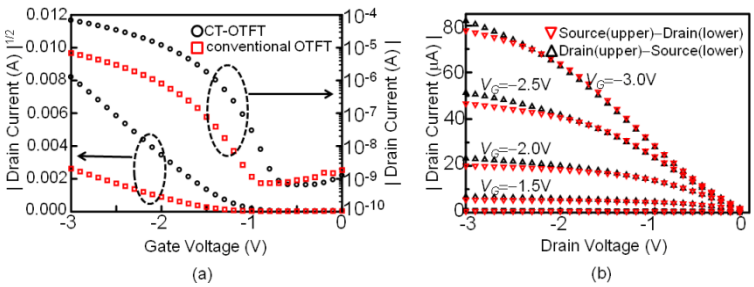

Figure 2. 5 (a) The transfer characteristics of the CT-OTFT with the polymeric edge support treated at 155 ◦C and a conventional top-contact OTFT at $V_D = -2.5$ V. (b) The output characteristic curves of the CT-OTFT when interchanging the source and the drain electrodes: upper source and lower drain electrodes (down-triangles) and upper drain and lower source electrodes (up-triangles). The curves were obtained with varying V_G from 0 to – 3 V in a step of − 0.5 V.

From the transfer characteristics of the CT-OTFT with the polymeric edge support treated at 155 ◦C shown in Fig. 2.5(a), the field-effect mobility in the saturation region was obtained as about 0.030 $cm^2 V^{-1}s^{-1}$ with the help of the measured value of 1.2 μFcm^{-2} for the capacitance of the AlO_X insulator of 5 nm thick. The threshold voltage was determined to be − 1.3 V from the linear fit of the data in Fig. 2.5(a). For a conventional top contact OTFT, the mobility and the threshold voltage were about 0.27 $cm^2 V^{-1}s^{-1}$ and − 1.5 V, respectively. For a short channel OTFT, as only the channel length decreases,

the channel resistance decreases but the contact resistance remains unchanged. In this case, the mobility decreases [27,33,34]. At the operating voltage of −3V, the drain current per channel width was measured as large as 80 μAmm^{-1} for our CT-OTFT with L = 0.8μm while it was about 7.4 μAmm^{-1} for a conventional top contact OTFT with L = 50 μm. This indicates that both the channel length, being one of the geometrical parameters, and the mobility play a critical role in the magnitude of the drain current in the OTFT for practical applications. It is clear that from the output characteristic curves shown in Fig. 2.5(b), the drain current becomes saturated when the AlO_X insulator is sufficiently thin (about 5 nm). It should be noted that both a step-edge OTFT [25] and a three-dimensional OTFT [26] exhibit often no saturation of the drain current depending on the electrode configuration. In our CT-OTFT, however, due to the geometrical symmetry, the electric properties are found to be always preserved within 5% regardless of the drain current direction. Such electrical symmetry gives more freedom to design various integrated circuits.

Usually, when thin insulators are used, gate current (I_G) is not negligible due to large leakage current, which induces the reduction of the on-off current ratio and the overestimation of the mobility. Fig. 2.6(a) shows the transfer curve with I_G. I_D/I_G is about 10^3 at V_G = −3 V. This ratio can be improved by reducing the overlap length (L_{over}) in MISM structure. L_{over} of the fabricated device is 2 mm, which is the sum of the overlap lengths in top ($L_{over,top}$) and bottom ($L_{over,bot}$) as shown in Fig. 2.6(b). If L_{over} is reduced to 0.2 mm, I_D/I_G is to be improved to 10^4.

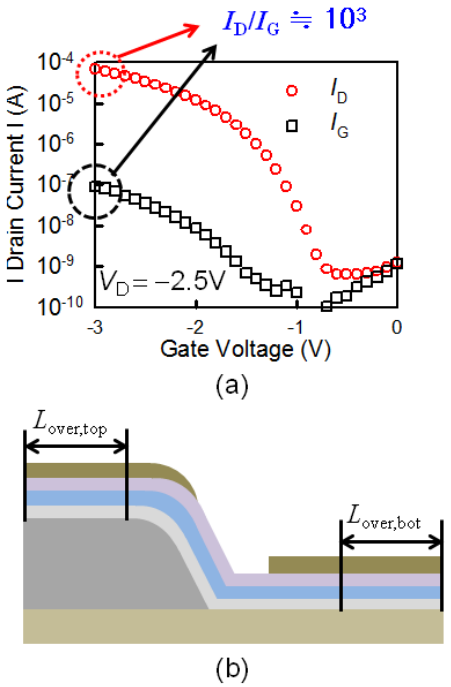

Figure 2. 6 (a) Transfer curve with gate current (b) Overlap length in CT-OTFT.

2.1.5 **Summary**

The chevron-type gate configuration of a short channel top-contact OTFT with a polymeric edge support was presented, showing large saturated drain current needed for practical applications. The drain current per channel width was as large as 80 μAmm^{-1} at an operating voltage of –3 V in the CT-OTFT with a self-defined channel of L = 0.8 μm. The short channel was easily formed by oblique deposition of Au onto the polymeric edge support. For different channel lengths, the thermal process based on a laser heating method may be employed. An optimized AlO_X insulator of about 5 nm enables us to produce the saturation of the drain current in the output curves. Due to the geometrical symmetry in the electrode configuration of our CT-OTFT, the electrical properties were well preserved when the source and the drain electrodes were interchanged. It is concluded that our concept of a polymeric edge support together with a thin insulator for a top-contact OTFT would provide a new scheme of designing a variety of organic electronic circuits that require large saturated drain current in a low voltage regime.

2.2 N-type Dual-Gate OTFT for Threshold Voltage Control

2.2.1 Introduction

Polymer OTFTs have attracted much attention for their potential use in flexible, low-cost electronic circuits [35-37]. In order to improve the electrical properties of the polymer OTFTs such as the on-current and the subthreshold swing, dual gate configurations of the polymer OTFTs have been proposed [38-41]. Among them, p-type polymer OTFTs have been quite extensively studied while n-type polymer OTFTs required for complementary circuits are barely demonstrated due to lack of proper materials.

In this chapter, the bias voltage effect on the electrical properties of n-type polymer OTFTs with dual gate electrodes is investigated. Their electrical characteristics including the hysteresis, the mobility, and the threshold voltage were measured as a function of the sweeping voltage at one gate electrode under the condition that the other gate was floated or biased.

2.2.2 Fabrication of dual gate configuration

The cross-sectional view of our dual gate configuration of n-type polymer OTFTs is schematically shown in Fig. 2.7(a). A p-doped Si substrate and a layer of 300 nm-thick SiO_2 were used for the bottom gate electrode and an insulator, respectively. The Si/SiO_2 substrate was cleaned with acetone, isopropyl alcohol, methanol, and deionized water in series for ten minutes each. The cleaned Si/SiO_2 substrate was exposed to UV-ozone and immersed in the toluene solution with octadecyltrichlorosilane to form a self-assembled monolayer on the surface of SiO_2 for improving the charge transport. The source and drain electrodes were prepared using 50-nm-thick Au by thermal deposition. The channel length and width were 80 μm and 1 mm, respectively. Poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)} [P(NDI2OD-T2)], dissolved in dichloro-benzene in 1 wt.%, was used to form an organic semiconductor layer by spin-coating at 3000 rpm for 30 sec and subsequently baked at 110° C for overnight in a vacuum dry oven. In preparing a top gate insulator, poly(methyl methacrylate) (PMMA) dissolved in ethyl acetate in 8 wt.% was spin-coated at 3000 rpm for 30 sec and baked at 100° C for 1 hour. The thickness of the PMMA film was 1.8 μm. The top gate electrode of 50-nm-thick Al was thermally deposited. Electrical characteristics of our polymer OTFTs with

dual gate electrodes were measured at room temperature under ambient condition using a semiconductor analyzer (HP 4155A).

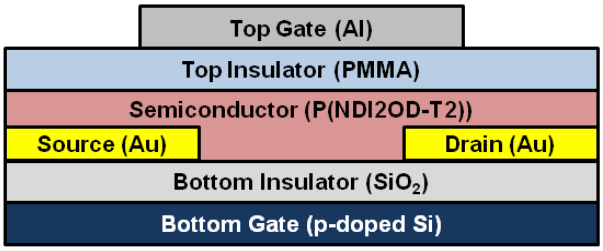

Figure 2. 7 A schematic cross-sectional view of the n-type polymer OTFT with dual gate electrodes.

2.2.3 Electrical characteristic of dual gate OTFT

It is fist examined how the bias voltage affects the hysteresis behaviors of n-type polymer OTFTs with dual gate electrodes. Figures 2.8(a) and (b) show the transfer characteristics as a function of the sweeping voltage at one gate electrode when the other gate was floated and vice versa, respectively. The hysteresis, which is defined as the difference (or the shift) of the threshold voltage between the forward sweeping (the gate voltage from 0 to 90 V) and the backward sweeping (the gate voltage from 90 to 0 V), was determined to be 24.6 V during sweeping the bottom gate voltage as shown in Fig. 2.8(a) while it was 20.2 V during sweeping the top gate voltage in Fig. 2.8(b). This large hysteresis results from the high trap density in the polymer semiconductor layer. In fact, the hysteresis originates from the change in the number of the trapped charges in the semiconductor layer during sweeping the gate voltage [42].

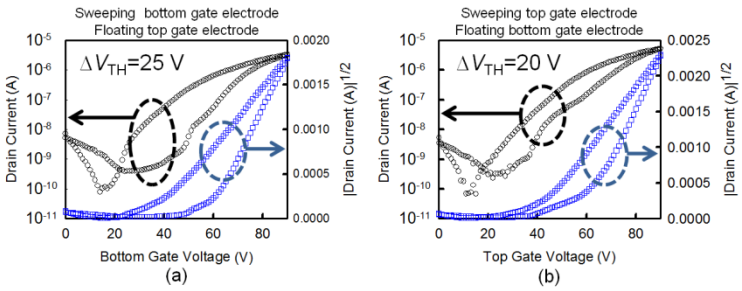

Figure 2. 8 The transfer characteristic curves (circles) and the square root of the drain current (squares) on sweeping the bottom gate voltage when the top gate is floated (a) and those on sweeping the top gate voltage when the bottom gate is floated (b).

The transfer characteristics of our n-type polymer OTFTs as a function of the sweeping voltage at one gate electrode is described under the condition that the other gate was biased and vice versa. As shown in Figs. 2. 9(a) and (b), the hysteresis was 15.5 V during sweeping the bottom gate voltage when the bias voltage was 80 V at the top gate electrode as shown in Fig. 2.9(a). For the case that the top gate and the bottom gate were interchanged, the hysteresis was found to be 0.5 V as shown in Fig. 2.8(b). This large difference of the hysteresis seen in Figs. 2.9(a) and (b) indicates that the trap density in the bottom channel is much higher than that in the top channel. Under the circumstance that the bottom gate voltage is swept for the bias voltage at the top gate electrode, only the number of the trapped charges in the bottom channel is changed while that in the top channel remains constant. This is also valid for the case that the top gate and the bottom gate are interchanged.

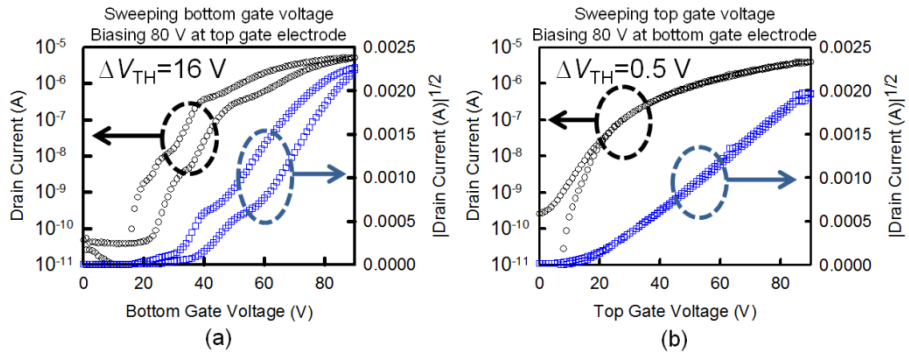

Figure 2. 9 The transfer characteristic curves (circles) and the square root of the drain current (squares) on sweeping the bottom gate voltage when the top gate is biased (a) and those on sweeping the top gate voltage when the bottom gate is biased (b) at V_D = 80 V.

2.2.4 Threshold voltage control of dual-gate OTFT

Let us discuss the effect of the magnitude of the bias voltage on the transfer characteristics of the n-type polymer OTFTs during sweeping the voltage at one gate electrode when the bias voltage is applied to the other gate electrode and vice versa. The transfer characteristic curves on sweeping the bottom gate voltage when the bias voltage at the top gate electrode was varied from 0 to 80 V are shown in Fig. 2.10(a). At the bias voltage of 0 V, no transfer characteristics were available. Above the bias voltage of 20 V, typical n-type transfer characteristic curves were observed. During sweeping the bottom gate voltage, the on-current increases from 46 nA to 5.1 μA at 90 V with increasing the bias voltage at the top gate electrode from 20 to 80 V as shown in Fig. 2.10(a). One interesting point is that the transfer characteristic curves are quite crooked and become shifted toward increasing the on-current with increasing the bias voltage at the top gate electrode. The capacitance of the bottom gate insulator is about six times larger than that of the top gate insulator. With increasing the bottom gate voltage, while the electrons in the bottom channel are accumulated, those in the top channel pre-accumulated by the top bias voltage become depleted. This is why the transfer curves were crooked

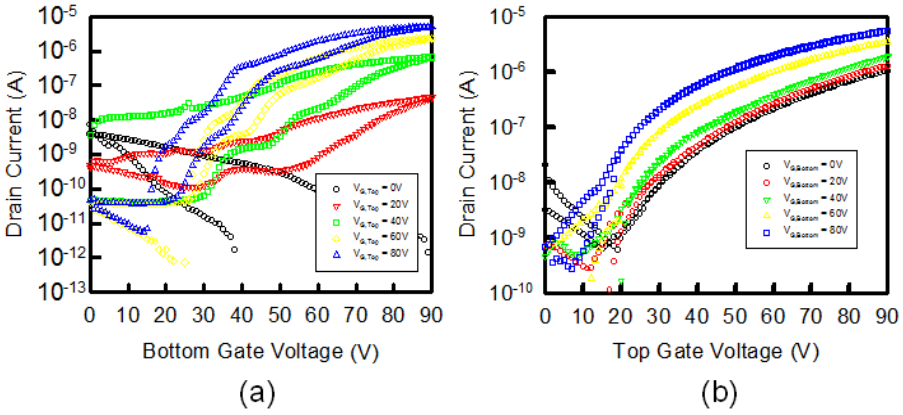

Figure 2. 10 The transfer characteristic curves on sweeping the bottom gate voltage when the bias voltage at the top gate electrode is varied (a) and those on sweeping the top gate voltage when the bias voltage at the bottom gate electrode is varied (b) at V_D = 50 V.

When the top gate electrode and the bottom gate electrode are interchanged, the on-current increases from 1.0 to 5.6 μA at 90 V with increasing the bias voltage at the bottom gate electrode from 0 to 80 V as shown in Fig. 2.10(b). Note that in this case, the hysteresis was negligible and no crooked behavior was observed in the entire range of the bias voltage we studied. Again, the transfer characteristic curves were shifted toward increasing the on-current with increasing the bias voltage.

The mobility and the threshold voltage in our p-type polymer OTFT are plotted as a function of the bias voltage at the bottom gate electrode in Fig. 2.11. The threshold voltage decreases with increasing the bias voltage at the bottom gate electrode. It was shifted from 38 to 19 V with increasing the bias

voltage from 0 to 80 V. In contrast to the p-type polymer OTFT with dual gate electrodes whose threshold voltage is positively shifted with increasing the negative bias voltage [41], the n-type polymer OTFT exhibits a negative shift of the threshold voltage with increasing the positive bias voltage since the electron is the majority carrier in the n-type semiconducting polymer. The mobility increases almost linearly from 0.017 to 0.082 cm^2/Vs with increasing the bottom gate voltage from 0 to 80 V. The behaviors of the threshold voltage in the presence of the bias voltage are attributed to the enhanced injection of mobile electrons from the source electrode to the n-type semiconducting polymer.

In dual-gate configuration, channels are formed in the top and bottom of the organic semiconducting layer. Thus, the total drain current is the sum of the top channel drain current ($I_{D,TOP}$) and the bottom channel drain current ($I_{D,BOT}$) as shown in Fig. 2.12. With increasing the bias voltage at bottom gate electrode, $I_{D,BOT}$ is increased. Therefore, the total drain current is increased, resulting in the increase of mobility. It is noted that the actual mobility of the top channel is not changed much and the charge flow at the bottom channel is included in the calculation of the mobility in the top gate sweeping and bottom gate biasing operation.

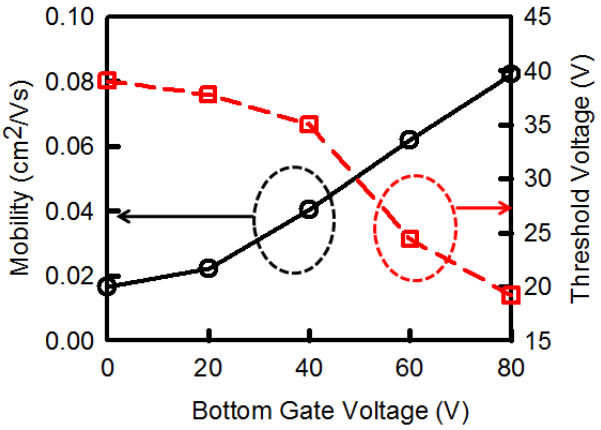

Figure 2. 11 The mobility and the threshold voltage in our n-type polymer OTFT with dual gate electrodes as a function of the bias voltage at the bottom gate electrode.

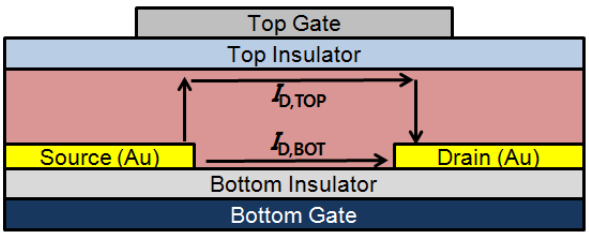

Figure 2. 12 Dual-channel formation in dual-gate OTFT.

2.2.5 Summary

It is demonstrated how the bias voltage affects the electrical characteristics of n-type polymer OTFTs with dual gate electrodes. The hysteresis is primarily governed by which gate electrode (bottom or top) is swept or biased. The hysteresis is negligible only when the top gate voltage is swept under the condition that the bottom gate electrode is biased. The dual gate configuration of the n-type polymer OTFT presented here will be useful for constructing a variety of organic integrated circuits.

Chapter 3. Organic Logic Elements

3.1 Introduction

Organic logic elements such as inverters, ring oscillators, and shift registers have attracted much attention due to their potential for low-cost and large-area electronic applications [43,44]. Particularly, a full-swing inverter is considered as one of the essential components needed for high-performance electronic circuits. For typical inorganic inverters, both an n-type OTFT and a p-type OTFT are generally integrated to guarantee a full-swing output. However, for organic inverters, p-type OTFTs are preferred since n-type organic semiconductor (OS) materials are rarely available and easily deteriorated under ambient environment in air and humidity [45]. Under these circumstances, two p-type OTFTs (one for a driving transistor and the other for a load transistor) [46-53] are commonly used for realizing an organic inverter as shown in Fig. 3.1(a). In this case, the requirements on an organic inverter for the high noise-margin and the full-swing operation are; i) the drain current of a load transistor should be saturated at zero gate-source voltage (V_{GS}) and ii) its magnitude should lie between the off-current of a driving transistor at V_{GS} = 0 and the on-current at V_{GS} = V_{DD} (the voltage supplied to the inverter) [54]. At a microscopic level, at V_{GS} = 0, no charges should exist in the interfacial region with an insulator for a driving transistor while positive charges (holes) should be accumulated in the p-type OS (p-OS)

layer for a load transistor as shown in Fig. 3.1(b). Besides the use of a dual-gate structure [46], a stacked architecture [47], two gate metals [48], or two organic semiconductors [49,50,51], different types of gate insulators including patterned electrets [52] or self-assembled monolayers (SAMs) [53] were previously employed for constructing a variety of organic inverters. Some of the existing approaches are relatively advantageous over others in view of the full-swing capability and the processing complexity. Therefore, it is very important to develop a simple and viable scheme of integrating two p-type OTFTs into a full-swing organic inverter with high noise-margin.

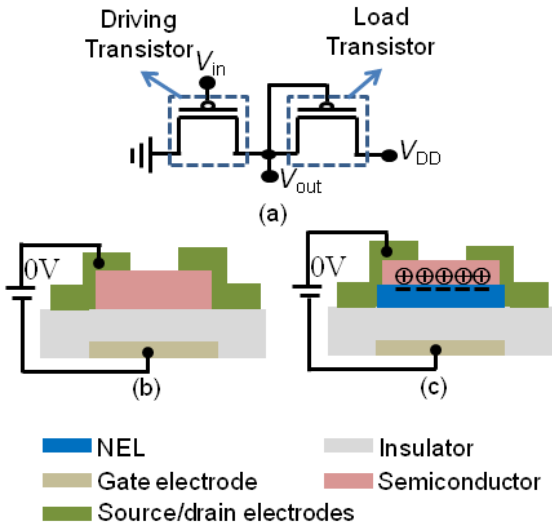

Figure 3. 1 . (a) The circuit diagram of a full-swing organic inverter consisting of two transistors with a same p-type semiconductor. V_{DD} is the supply voltage, V_{in} is the input voltage, and V_{out} is the output voltage. (b) Schematic illustration of a driving transistor (left) and a load transistor (right) where the accumulation of positive charges (holes) in the OS at VGS = 0 is shown.

In this chapter, the control mechanism for interfacial charges in an organic field-effect transistor (OTFT) by the introduction of a surface polarized layer (SPL) which produces a transverse dipolar field at the OS-interface is presented, and a high noise-margin full-swing organic inverter consisting of two p-type OTFTs on a single substrate is demonstrated. For the integration of two p-type OTFTs, the SPL is interfaced with the p-OS in the load transistor for the accumulation of holes by the transverse dipolar field (normal to the interface) at V_{GS} = 0. The SPL of a fluorinated polymer is selectively prepared on the top of a gate insulator. Due to the accumulated holes in the interfacial region, the drain current of the p-type OTFT becomes to saturate at V_{GS} = 0 and its magnitude lies between the on-current and off-current of a conventional OTFT with no SPL. This leads directly to the construction of a high-noise margin full-swing organic inverter where one OTFT without the SPL for a driving transistor and the other with the SPL for a load transistor are integrated in a single substrate.

3.2 Transfer-printing of SPL

3.2.1 Process of transfer-printing

The schematic diagrams showing the preparation of the SPL in the load transistor and the fabrication of a full-swing organic inverter on a single substrate are shown in Figs. 3.2(a) and (b). Glass substrates were cleaned with acetone, iso-propylalcohol, methanol, and deionized water in sequence. For a gate electrode, aluminum (Al) was thermally deposited on a cleaned glass substrate through a shadow mask. Two different polymers of poly(4-vinylnaphthalene) (PVN) [55] and polystyrene (PS) [56,57], known to yield high mobility and to reduce the hysteresis in the OTFTs, were used as gate insulators to systematically study the charge accumulation associated with the surface electric field of the SPL. Each of the PVN and PS, dissolved in toluene in 10 wt.%, was spin-coated on the top of the pre-patterned Al gate electrode, and cured at 90℃ for 30 min to remove residual toluene. The thickness of the PVN and that of the PS were 620 and 630 nm, respectively. The capacitance per unit area (C_i) for the PVN layer and that for the PS layer were 4.11 and 4.07 nF/cm^2, respectively. Two OTFTs for an organic inverter, a driving transistor and a load transistor, were interconnected to each other through a via hole produced using a solvent-drop method [58]. A fluorinated polymer (Novec^{TM} EGC-1700, 3M) possessing the surface dipoles was chosen for the SPL to produce a transverse electric field (normal to the OS interface)

in the load transistor. As shown in Fig. 3.2(a), the SPL pattern on an elastomeric stamp was transfer-printed onto the gate insulator (either the PVN or the PS) only in the load transistor without the application of heat and/or high pressure [58]. The thickness of the SPL was varied to be 50, 110, and 200 nm. The total C_i for the 50 nm-thick SPL on the PVN and that on the PS were measured as 3.94 and 3.76 nF/cm^2, respectively. A p-OS layer of pentacene was simultaneously deposited on both the bare gate insulator for a driving transistor and the SPL for a load transistor by thermal evaporation at the rate of 0.5 Å sec^{-1} under the pressure of about 10^{-6} Torr. The thickness of the pentacene layer was about 50 nm. As shown in Fig. 3.2(b), for the preparation of the source/drain electrodes and the interconnection between two transistors through a via hole structure, one-step thermal deposition of gold (Au) was carried out at the rate of 1.0 Å sec^{-1} under the pressure of about 10^{-6} Torr, producing the Au layer of 65 nm thick. The length and the width of the active channel were 50 μm and 1000 μm, respectively.

The measurements of the electrical properties of the fabricated OTFTs and organic inverters were carried out using a semiconductor parameter analyzer (HP4155A, Hewlett-Packard Co.) under ambient pressure at room temperature. The surface morphologies of both the polymeric insulators and the pentacene films were determined using an atomic scanning probe microscope (SPM) (SPA 400, Seiko Instruments Co., Ltd.).

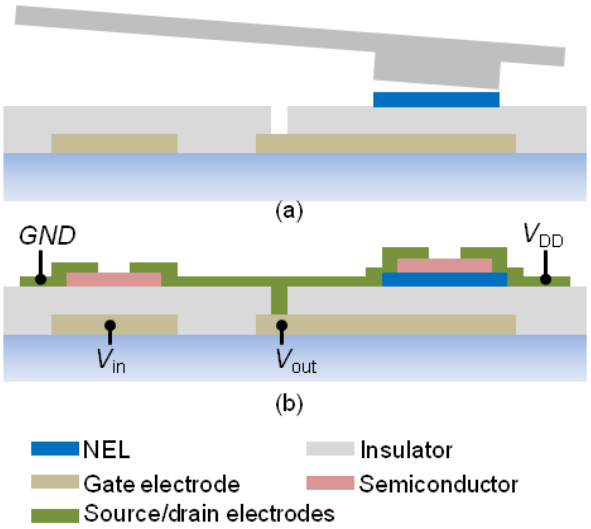

Figure 3. 2 (a) the preparation of the SPL in the load transistor by transfer-printing and (b) the fabrication of a full-swing organic inverter on a single substrate.

3.2.2 Morphological properties of SPL and pentacene films

The surface morphologies of two gate insulators, the PVN and the PS, and the patterned SPLs where the pentacene films are grown are examined. Figures 3.3(a) and (b) show the SPM images of the PVN and the PS, respectively. The surface roughness of the PVN and that of the PS were about 3.1 and 2.7 Å, respectively. The SPM images of the SPL on the PVN and the PS were shown in Figs. 3.3(c) and (d). The average roughness of the SPL on the PVN and that on the PS were 8.3 and 8.0 Å, respectively. The SPL patterns on the PVN and the PS observed with an optical microscope were shown in Figs. 3.3(e) and (f) where the SPL lines of 100 μm wide were produced by simple transfer-printing. In principle, the transfer-printing method is capable of producing high-resolution patterns of a few micrometers [58] but it often increases the surface roughness due to the direct contact with the substrate.

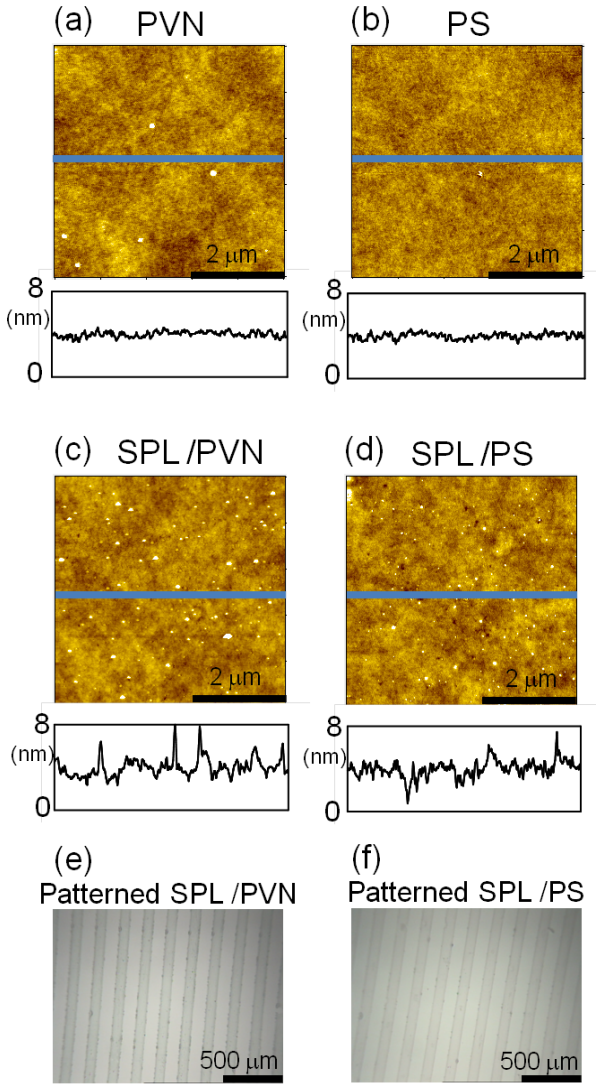

Fig. 3. 3 The surface morphologies of the gate insulators, (a) the PVN and (b) the PS, observed with a SPM. The surface morphologies of (c) the SPL on the PVN and (d) the SPL on the PS observed with a SPM. The transfer-printed SPL patterns on (e) the PVN and (f) the PS observed with an optical microscope.

3.3 Electrical Characteristics of SPL Capacitors and OTFTs

3.3.1 Turn-on voltage shift

The surface polarization properties of the SPL in contact with a p-type OS in the capacitance of a metal-insulator-semiconductor-metal (MISM) structure and the drain current in an OTFT are investigated to characterize the electrical stability and the reproducibility of the SPL. The bottom and top electrodes denoted by BE and TE were made of Al and Au, respectively. The p-type OS used was pentacene. Figures 3.4(a) and (b) show the capacitance in the MISM with the SPL thickness of about 110 nm and that of about 300 nm as a function of the applied voltage on sweeping, respectively. The capacitance during the cycling of the applied voltage up to ten times was shown in each inset. Essentially, no considerable hysteresis behavior of the capacitance was observed, suggesting that the surface polarization of the SPL is always reproducible irrespective of the SPL thickness. The capacitance approaches a minimum at the applied voltage above 6 V for the SPL of 110 nm and about 20 V for 300 nm, increases substantially at zero applied voltage, and saturates in the negative voltage regime as shown in Fig. 3.4(a) and (b). In contrast to typical dielectric materials such as PS [59] and poly(methylmethacrylate) [60], for the SPL we used, the minimum capacitance was obtained at a positive voltage due to a surface dipolar field which is known to exit a fluorine-

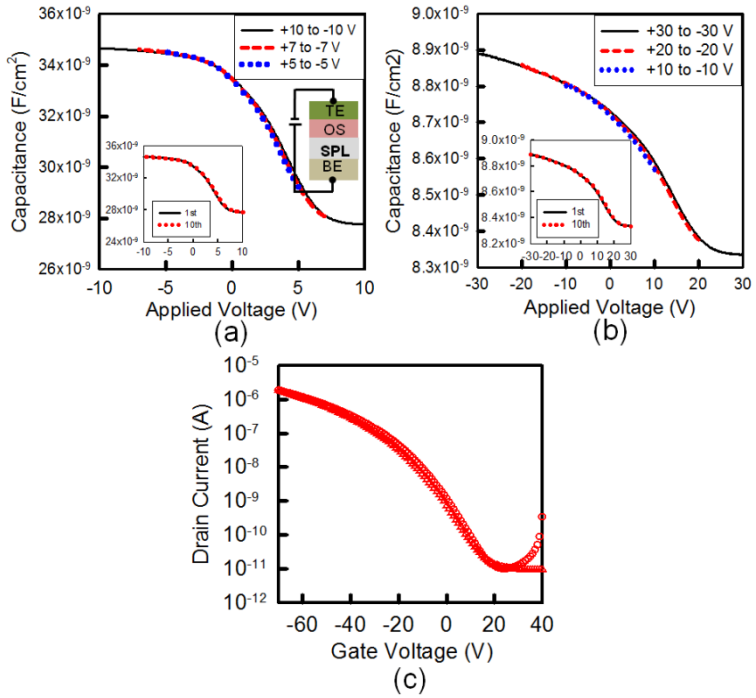

Figure 3. 4 (a) The capacitance in the MISM with the SPL of 110 nm thick as a function of the applied voltage on sweeping. Dotted (blue), dashed (red), and solid (black) lines represent the capacitance values measured at the applied voltage of 5 to – 5, 7 to – 7, and 10 to – 10 V, respectively. (b) The capacitance in the MISM with the SPL of 300 nm thick as a function of the applied voltage on sweeping. Dotted (blue), dashed (red), and solid (black) lines represent the capacitance values measured at the applied voltage of 10 to – 10, 20 to – 20, and 30 to – 30 V, respectively. Each inset shows the capacitance of the MISM after the first (black solid line) and tenth (red dotted line) cycles of the applied voltage. (c) The transfer characteristic curves of the OTFT with the SPL used as a gate insulator. Triangles and circles represent the transfer characteristic curves measured during the sweeping cycle of the gate voltage toward a positive direction and a negative direction at the drain-source voltage of – 50 V, respectively.

terminated which is known to exist at a fluorine-terminated surface in general [61-65]. The transfer characteristic curves of the OTFT with the SPL of 600 nm thick at the drain-source voltage of – 50 V during sweeping the gate voltage were shown in Fig. 3.4(c). Note that as in typical OTFTs [58,66,67], a rather thick (600 nm) SPL was used as an insulator for the OTFT to reduce the leakage current and a similar channel dimension was adopted. With the help of the intrinsic capacitance of 2.9 nF/cm^2 measured in a metal-insulator-metal structure, the mobility was calculated to be 0.04 Vs/cm^2. The drain current reaches a minimum at a relatively large positive value (about 20 V) of the V_{GS} and increases at zero voltage as in the capacitance of the MISM.

In understanding the charge accumulation in the OS layer due to the transverse dipolar field of the SPL placed on a gate dielectric, we determine the electrical properties of both a MISM structure without the SPL and that with the SPL. Figures 3.5(a) and (b) show the capacitance values measured in the MISMs with and without the SPL (50 nm thick) for the PVN case and those for the PS case, respectively. In both cases, the capacitance of the MISM without the SPL was found to have a nearly minimum at zero applied voltage and to increase with increasing the applied voltage toward the negative direction, implying that the charge accumulation depends solely on the applied electric field. In contrast, the minimum capacitance of the MISM with the SPL occurred at a large positive voltage (about 20 V) rather than zero voltage. Again, as in Fig. 3.4(a), this voltage shift originates from the transverse dipolar field generated from the SPL which is interfaced with the OS layer. Moreover, from the polarity-dependent capacitance and the

direction of the voltage shift, it is clear that the accumulated charges at the SPL-OS interface are holes and the SPL produces a transverse electric field toward the OS layer at the interface.

The transfer characteristic curves for two types of the OTFTs with and without the SPL (50 nm thick) at the drain-source voltage of – 50 V during the sweeping cycle of the gate voltage for the PVN case and those for the PS case are shown in Figs. 5(a) and (b),respectively. The subthreshold characteristics of our two transistors seem to be relatively poor but are still at a level comparable to previous works [13,16,24]. Such subthreshold characteristics will not limit the applicability of the SPL for the construction of a full-swing inverter although they will affect the switching speed and the noise-margin. The mobility of the OTFT with only the PVN and that with only the PS were about 0.4 and 0.3 Vs/cm^2, respectively. For two OTFTs with the SPL, the mobility of the OTFT was about 0.07 Vs/cm^2 for the PVN and 0.06 Vs/cm^2 for the PS. The decrease in the mobility was attributed to the increase in the surface roughness of the SPL as seen from Figs. 3.3(c) and (d). The subthreshold slope was found to be about 5 V/decade irrespective of the presence of the SPL in our OTFTs. It is known that the subthreshold slope is proportional to the thickness of the gate insulator [13] and typical OTFTs with the insulators of 600-1000 nm thick have the subthreshold slope in the range of 5 to 8 V/decade [13,24]. In analogy to the MISM case, the shift of V_{GS} for the minimum of the drain current in the OTFT with the SPL was observed due to the accumulation of the holes at the SPL-OS interface. More specifically, the turn-on voltage (V_{on}), defined as V_{GS} at which the drain current starts to

increase exponentially [19], is negative (– 2 V for the PVN and – 6 V for the PS) in the OTFT without the SPL while V_{on} in the OTFT with the SPL is positive (11 V for the PVN and 9 V for the PS). This means that in the p-type OTFT, the holes accumulated by the surface dipolar field from the SPL produces the charge flow in the drain at a positive value of V_{GS}.

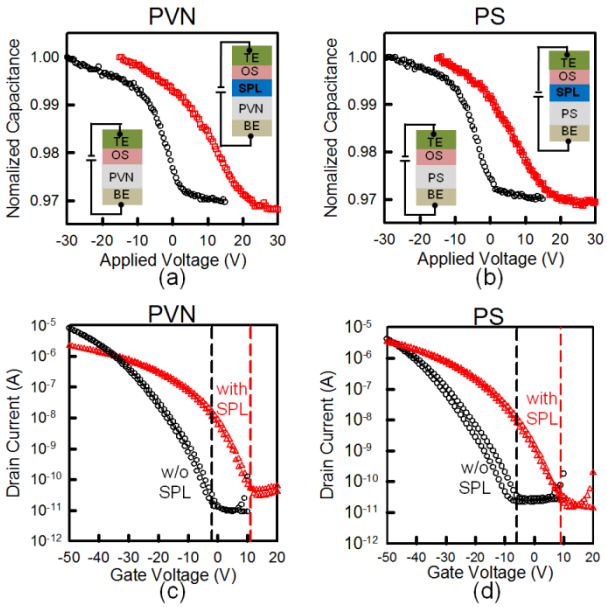

Figure 3. 5 The capacitance values measured in the MISMs with and without the SPL for (a) the PVN case and (b) for the PS case as a function of the applied voltage. Squares (red) and circles (black) represent the capacitance values in the MISMs with and without the SPL, respectively. The transfer characteristic curves of two types of the OTFTs with the SPL and without the SPL for (c) the PVN case and (d) the PS case during the sweeping cycle of the gate voltage. Triangles (red) and circles (black) represent the transfer characteristic curves of the OTFT with the SPL and those of the OTFT without the SPL at the gate voltage at V_{DS} = −50 V, respectively. The dotted and dash lines in the vertical direction indicate the turn-on voltage (V_{on}) of the OTFT with the SPL and that of the OTFT without the SPL, respectively.

3.3.2 Thickness independence of SPL

It is discussed how the accumulation of holes in the p-OS layer varies with the SPL thickness in terms of the drain current in the OTFT with the SPL. In fact, the magnitude of the transverse dipolar field generated from the SPL should be independent of the SPL thickness in the case that the dipoles exist only on the surface, not in the bulk, of the SPL. The SPL thickness was varied from 50 nm to 200 nm. The drain current at V_{GS} = 0 for the PVN case and that for the PS case are shown as a function of the SPL thickness in Figs. 3.6(a) and (b), respectively. Clearly, no dependence of the drain current on the SPL thickness was observed as discussed above. The saturated drain current at V_{GS} = 0 remains about 2 nA regardless of the SPL thickness. Note that a fluorine-terminated surface, in general, produces a dipolar field normal to the surface as in our case of the SPL. For a ferroelectric insulator, it may be interesting to examine how the permanent dipoles in the bulk affect the charge trapping and transport in the interfacial region.

Figures 3.6(c) and (d) show the output characteristic curves of the OTFTs with and without the SPL (50 nm thick) at V_{GS} = 0 for the PVN case and those for the PS case, respectively. In both cases, the drain current in the saturation regime was about 2 nA. Compared to the OTFT with no SPL in Figs. 4c and d, the saturated drain current of 2 nA was two orders of magnitude larger than the off-current (at V_{GS} = 0) and three orders of magnitude smaller than the on-current (at V_{GS} = − 50 V). As discussed earlier, this criterion of the drain current allows to construct a high noise-margin full-swing organic inverter

with two p-type OTFTs, one for a driving transistor (without the SPL) and the other for a load transistor (with the SPL).

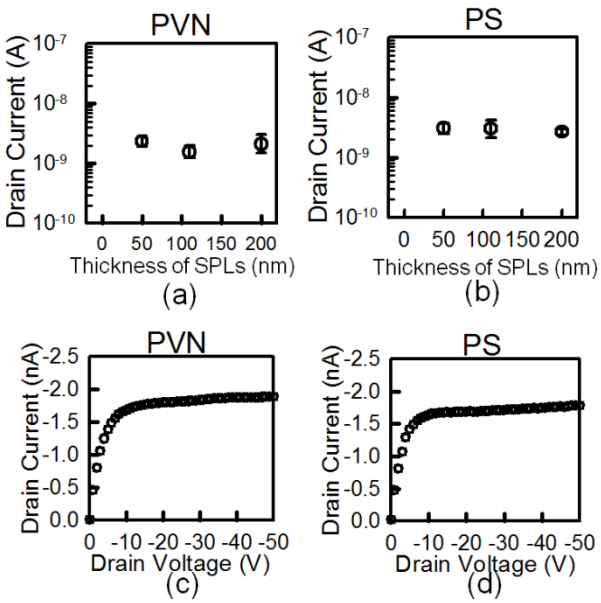

Figure 3. 6 The magnitudes of the drain current in the OTFTs with (a) the SPL/PVN and (b) the SPL/PS at V_{GS} = 0 for three different values of the SPL thickness. Each error bar represents the logarithmic standard deviation of five samples for given SPL thickness. The output characteristic curves of the OTFTs with (c) the SPL/PVN and (d) the SPL/PS at V_{GS} = 0.

3.4 Electrical Characteristics of SPL Capacitors and OTFTs

Based on the above results for the SPL in the MISM and the OTFT, we constructed two classes of organic inverters of pentacene shown in Fig. 1d; one is the PVN-based inverter and the other is the PS-based inverter. For a load transistor in each organic inverter, the SPL (50 nm thick) was introduced on the top of the corresponding gate insulator (the PVN or the PS) to produce a transverse dipolar field at the SPL-pentacene interface. All the OTFTs have the same dimensions of the channel length (50 μm) and the channel width (1000 μm). Figures 6a and b show the voltage transfer curves (VTCs) of the PVN-based organic inverter and those of the PS-based organic inverter measured as a function of the input voltage at three different values of V_{DD} = – 30, – 40, and – 50 V, respectively. Note that the two types of the inverters show the full-swing characteristics with no considerable hysteresis when the input voltage is swept from 0 to V_{DD} and from V_{DD} to 0. Regarding the scaling of the output voltage of an inverter, a reference driving OTFT with a relatively wide range of the operation voltage (below 10 V) is desirable. The noise margin at the high level and noise margin at the low level [47] are 13 and 34 V for the PVN inverter and 16.5 and 30 V for the PS inverter at V_{DD} = – 50 V. Those values are higher than 52 and 66 % of the maximum theoretical value (or the half of the V_{DD}) for the PVN inverter and the PS inverter, respectively. The rising and falling times of the inverter were found to be about 0.02 sec

and 0.8 sec, respectively. A rather slow speed is due to a relatively small value of the load current (about 2 nA). In fact, the falling time limits the switching speed of the inverter and thus, relatively large drain current of a load transistor at zero gate voltage is needed to improve the switching speed. Moreover, the reduction of the capacitance from the overlap between the gate electrode and the source/drain electrode is another factor to improve the speed without the loss of the noise-margin.

Figures 6c and d show the gain of the PVN-based inverter and that of the PS-based inverter, respectively. The maximum gain was about 27 for the PVN case and 17 for the PS case at $V_{DD} = -50$ V. In Table 1, both the ratio of the noise-margin to the maximum theoretical value (or the half of the V_{DD}) and the gain of a pentacene organic inverter in several approaches are summarized. It is clear that the concept of using the SPL leads to simple fabrication of an organic inverter based on only one type of the OS and allows high noise-margin together with high gain in full-swing operation.

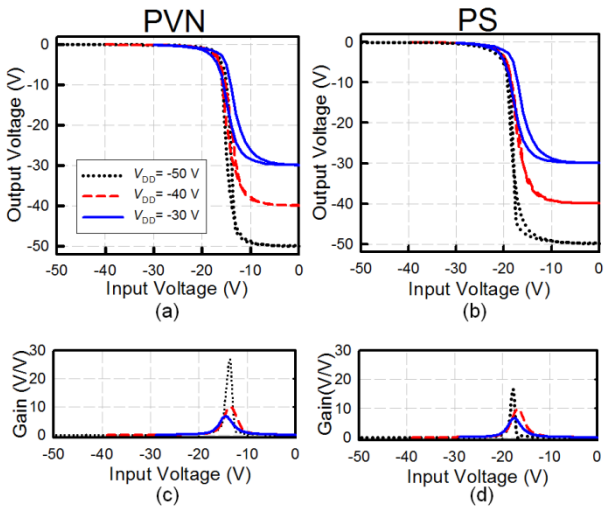

Figure 3. 7 The VTCs of (a) the PVN-based inverter and (b) the PS-based inverter as a function of the input voltage at three different values of V_{DD} = −30, −40, and −50 V. The solid (blue), dashed (red), and dotted (black) 43lines represent V_{DD} = −30, −40, and −50 V, respectively. Each set of the VTCs were obtained during sweeping the input voltage from V_{DD} to 0 and from 0 to V_{DD}. The gain of the PVN-based inverter and that of the PS-based inverter measured as a function of the input voltage are shown in (c) and (d), respectively.

Approaches	Ratio of noise margin to half of V_{DD} (%)	Gain (V/V)
Dual gate [46]	60	7
Stacked architecture [47]	66	13.4
Two gate metals [48]	20	6
Two semiconductors [51]	~0	22
Electrets [52]	25	7.2
SAMs [53]	12	2
This work: SPL on PVN	52	27
This work: SPL on PS	66	17

Table. 3. 1 The ratio of the noise-margin to the maximum theoretical value (the half of V_{DD}) and the gain of a pentacene organic inverter in several approaches.

3.5 Summary

The high noise-margin full-swing organic inverter consisting of only p-type OTFTs on a single substrate is demonstrated with the help of the SPL which controls effectively the accumulation of holes in the p-OS (pentacene) interfaced with the SPL. Note that the SPL of a fluorinated polymer possessing the surface dipoles is known to yield a dipolar field normal to the surface. Depending on the nature of the charge carriers (holes or electrons) and the type of the OS material (n-type or p-type) being used, the SPL needs to be properly tailored. Moreover, the magnitude of the surface polarization of the SPL is expected to significantly influence the voltage scalability of the inverter. In addition to the high electrical performance of a reference OTFT, an integration scheme of two OTFTs into an organic inverter configuration plays an essential role on the switching speed, the noise-margin, and the gain of the inverter. The concept of using the SPL together with the transfer-printing technique presented here provides a versatile platform to devise highly integrated organic electronic circuits for advanced electronic and optoelectronic systems.

Chapter 4. Nonvolatile Memory Cells

4.1 Introduction

Ferroelectric organic thin-film transistors (FeOTFTs) have received much attention due to their potential for the nonvolatile data storage at low cost and the design flexibility [68,69]. For more complex functional applications, the FeOTFTs should be combined with conventional paraelectric OTFTs (POTFTs). For example, ferroelectric memory array was realized by integrating the FeOTFTs with the POTFTs [70,71]. One of the crucial challenges for the realization of these ferroelectric circuits is to fabricate both the FeOTFTs and the POTFTs in a single substrate. For the integration of the FeOTFTs and the POTFTs, patterning a ferroelectric polymer, which is the general gate insulator for the FeOTFTs, is needed. During the photolithography which is the conventional patterning technique for the device integration, the ferroelectric polymer is damaged by solvents such as acetone. Thus, for the realization of the more functional application of the FeOTFTs, the difficulty in integration of the FeOTFTs and the POTFTs should be overcome.

In this chapter, the FeOTFTs and the POTFTs are integrated by transfer-printing of the paraelectric buffer layer (PBL) on the ferroelectric layer. The PBL eliminates the hysteresis of the ferroelectric layer. Using this technique,

ferroelectric memory array and voltage-readable ferroelectric multistate memory cell is demonstrated.

4.1.1 Array of ferroelectric memory

Ferroelectric memory array based on OTFTs has attracted a great deal of attentions since they provide the non-volatility together with the fabrication compatibility for low cost and flexible electronics such as identification tags and memory embedded sensor sheets [70,71]. One of the crucial challenges for the realization of the ferroelectric memory array is to prevent crosstalk between ferroelectric memory cells [72]. In order to avoid crosstalk in the ferroelectric memory array, combining one ferroelectric memory OTFT with one selection OTFT was introduced as shown in Fig. 4.1(a) [70,72]. In this case, it is necessary that the ferroelectric memory OTFT should exhibit high memory on-off current ratio and the selection OTFT should show high switching on-off current ratio. For those requirements, both ferroelectric and paraelectric insulators need to be integrated. However, patterning of the ferroelectric polymer is difficult since the ferroelectric polymer is damaged by solvents such as acetone during photolithography. Recently, in order to avoid the patterning process, the ferroelectric OTFTs and paraelectric OTFTs was vertically stacked and placed respectively on different floors as shown in Fig. 4.1(b) [70]. However, the formation of the stacked structure requires processing complexity. Therefore, it is very important to develop a simple and viable scheme of integrating two types of OTFTs into a single organic memory cell.

In the **Chap.** 4.2 to 4.4, ferroelectric nonvolatile memory array is demonstrated, which is realized by the paraelectric/ ferroelectric bilayer

structure in ferroelectric OTFTs as shown in Fig. 4.1(c). To laterally integrate ferroelectric memory OTFTs and paraelectric OTFTs in a single substrate, the PBL is selectively placed on the ferroelectric dielectric. The PBL on the ferroelectric dielectric plays an essential role in screening the ferroelectric dipole field and reducing the surface roughness of insulators. It is found that owing to the PBL, the memory on-off current ratio is decreased and switching on-off current ratio is increased in the selection OTFTs. This directly leads to the construction of ferroelectric memory array without crosstalk between memory cells in writing and reading operation.

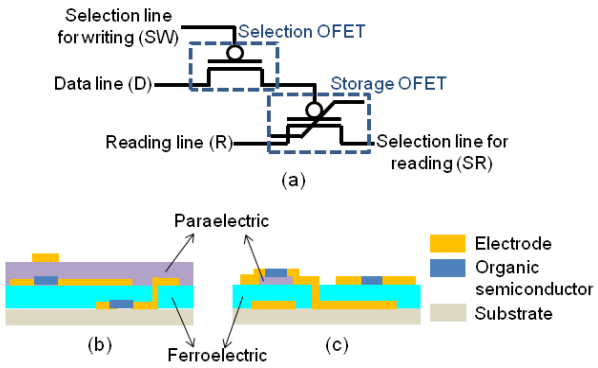

Figure 4. 1 (a) Circuit diagram of ferroelectric memory cell consisting of a selection OTFT and a storage OTFT. (b) The schematic diagram of the stacked structure memory cell reported in Ref. 70. (c) The schematic diagram of the memory cell with the bilayer structure.

4.1.2 Multi-level voltage readable memory

The underlying principle of the FeOTFT memory comes mainly from the ferroelectric nature of a gate insulator wherein the dipolar strength depends on the magnitude of the programming voltage (V_P) above the coercive voltage (V_C) [68,73]. Here, V_P represents the applied voltage at a gate electrode to program the nonvolatile memory state. As shown in Figs. 4.2(a) and (c), one of two alignment directions (toward either the organic semiconductor or the gate) of the dipole moments exists in the ferroelectric insulator depending on the polarity of $V_P > V_C$. As a result, two memory states corresponding to the two dipolar directions in the FeOTFT enable to construct data storage devices with nonvolatile binary memory [73]. Recently, in order to store more data than a single bit per a memory cell, the FeOTFT capable of storing multi-level information has been studied [74,75]. For the FeOTFT with the multi-level storage capability, the intermediate states between two dipolar alignment states, as shown in Fig. 4.2(b), have been researched for the FeOFET with the three memory states [74] or four memory states [75]..

In most of the FeOTFTs including multi-level FeOTFTs, the stored information is read as a magnitude of the drain current [68-75] due to the inherent current output nature of the FeOTFTs. However, for certain microelectronic applications such as voltage divider circuits or driving circuits for liquid crystal display or electrophoretic display, the voltage output is preferred to the current output. Therefore, for the more microelectronic

applications of the ferroelectric memory, the voltage readability is required together with the multi-level storage capability.

In the **Chap.** 4.5 and 4.6, the voltage-readable nonvolatile memory cell with the ferroelectric multistates is demonstrated in an organic inverter configuration. The ferroelectric intermediate states of the ferroelectric layer are programmed with the magnitude of V_P. It was found that such multlevel current output of the FeOTFT is converted into the multilevel voltage output of an inverter consisting of a driving paraelectric OTFT (DPT) and the load FeOTFT (LFT) as shown in Fig. 4. 2(d).

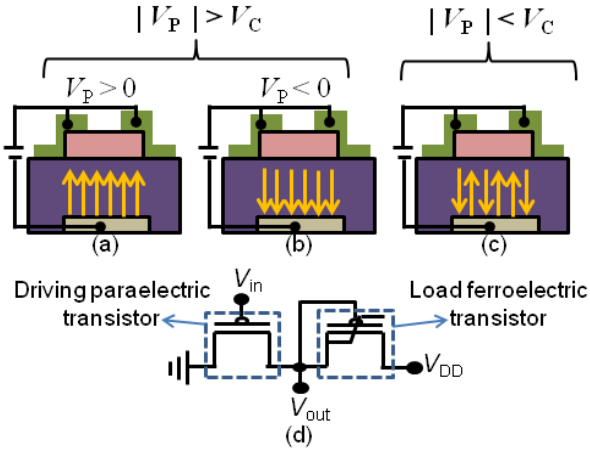

Figure 4. 2 Schematic illustrations of the alignment of the dipole moments in the ferroelectric layer in OTFTs at (a) | V_P | > V_C and V_P > 0, (b) | V_P | > V_C and V_P < 0, and (c) | V_P | < V_C. The yellow arrows represent the direction of the dipole moments in the ferroelectric layer. (d) The circuit diagram of a unipolar inverter with a zero gate load ferroelectric transistor. V_{DD} is the supply voltage, V_{in} is the input voltage, and V_{out} is the output voltage.

4.2 Fabrication of Ferroelectric Memory Circuit

4.2.1 Process of fabrication

Glass substrates were cleaned with acetone, iso-propylalcohol, methanol and deionized water in sequence. For a gate electrode, aluminum (Al) was thermally deposited on a cleaned glass substrate through a shadow mask. For a ferroelectric gate insulator, poly(vinylidene fluoride) copolymer with trifluoroethylene (75/25 mol%) copolymer [P(VDF-TrFE)], dissolved in cyclopentanone in 10 wt %, was spin-coated on the substrate and cured at 140 ℃ for 2 h to promote the ferroelectric β-phase of the P(VDF-TrFE) film. The thickness of the P(VDF-TrFE) film were measured as 630-650 nm. Two OTFTs for a memory cell, a FeOTFT and a POTFT, were interconnected to each other through a via hole produced using a solvent-drop method [76,77]. A fluorinated polymer (NovecTM EGC-1700, 3M) was chosen for the PBL due to its paraelectricity and compatibility to transfer-printing. As shown in Fig. 4.3(a), for the POTFT, the PBL pattern on an elastomeric stamp was transfer-printed onto the ferroelectric gate insulator without the application of heat and/or high pressure [76,77]. The thickness of the PBL (t) was varied to be 30, 50, 110 and 200 nm. A p-type organic semiconductor of pentacene was simultaneously deposited on both the bare gate insulator and the PBL for a selection OTFT by thermal evaporation at the rate of 0.5 Å sec^{-1} under the pressure of about 10^{-6} Torr. The thickness of the pentacene layer was about 50

nm. For the preparation of the source/drain electrodes, thermal deposition of gold (Au) was carried out at the rate of 1.0 Å sec^{-1} under the pressure of about 10^{-6} Torr, producing the Au layer of 65 nm thick. For the ferroelectric inverter, V_P is applied before connecting two OTFTs. The length and the width of the active channel were 50-150 μm and 1000 μm, respectively. The schematic views of the ferroelectric memory cell and the voltage-readable ferroelectric memory inverter cell are shown in Fig. 4.3 (b) and (c), respectively.

The measurement of the electrical properties of the memory circuits was carried out using a semiconductor parameter analyzer (HP4155A, Hewlett-Packard Co.) under ambient pressure at room temperature. The surface morphologies of both the polymeric insulators and the pentacene films were determined using an atomic force microscope (AFM) (SPA 400, Seiko Instruments Co., Ltd.).

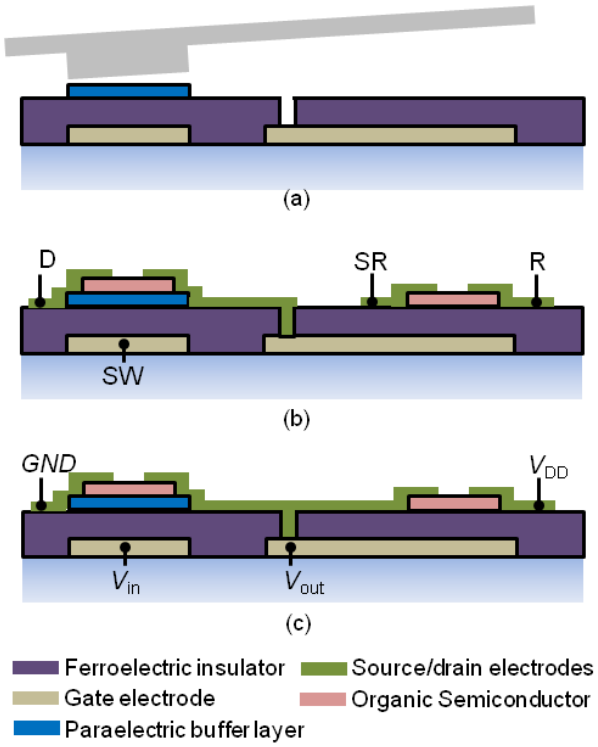

Figure 4. 3 (a) Transfer printing of the pattern of the PBL on the ferroelectric insulator (b) Schematic cross-sectional view of a ferroelectric memory cell with a selection OTFT and a memory OTFT. (c) Schematic cross-sectional view of a inverter-type ferroelectric memory with a zero gate LFT and a DPT.

4.2.2 Morphological properties of PBL

It is described how thickness of the PBL affects the morphological properties of ferroelectric gate insulators. The AFM images and the corresponding morphological profiles of the bare P(VDF-TrFE) and bilayer structures with P(VDF-TrFE) having 30, 50, and 200 nm-thick PBL are shown in Figs. 4.4(a), (b), (c) and (d), respectively. The root-mean-square (rms) roughness of the bare P(VDF-TrFE) was found to be 23.9 nm. Since the 30 nm-thick-PBL is not able to follow the high roughness of the P(VDF-TrFE), the partially transfer-printed PBL is observed as shown in Fig. 4.4(b). As shown in Figs. 4.4(c) and (d), in the case of the thickness above 30 nm, the PBL is fully transferred on the P(VDF-TrFE) and the morphology of the P(VDF-TrFE) with the PBL above 50 nm is smoother surface profile. Therefore, the PBL above 30 nm provide uniform and smooth surface of the insulators.

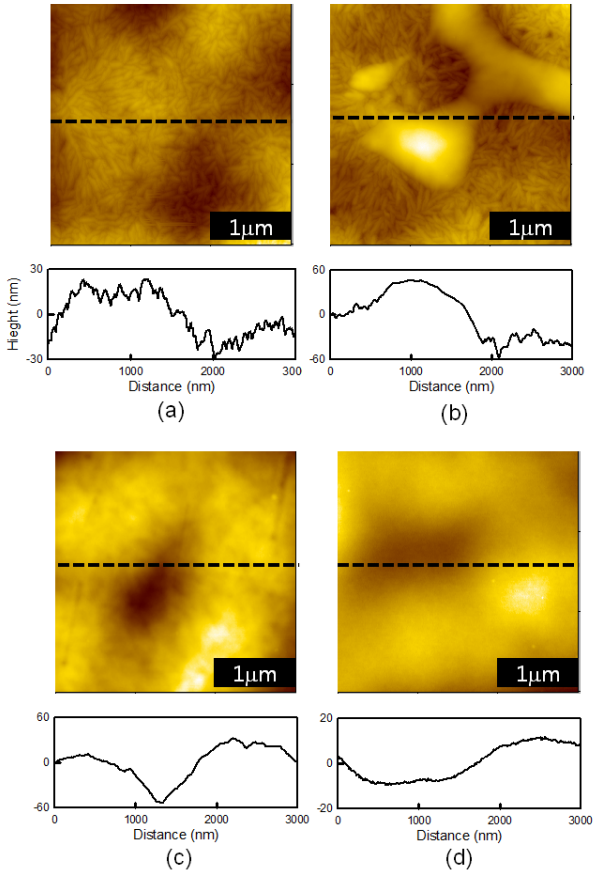

Figure 4. 4 The AFM images and the morphological profiles of the bilayer insulators with no PBL (a) and with *d* of 30 (b), 50 (c), and 200 nm (d).

4.3 Effect of PBL on Ferroelectric OTFTs

Figure 4.5(a) shows the transfer curves of five OTFTs with no PBL and with 30, 50, 110, and 200 nm-thick-PBL at V_D = −5 V. The gate voltage (V_G) was swept forward from 60 V to –60 V and backward from 60 V to –60 V. In Fig. 4.5(b), the drain current at V_G = 0 V in the forward sweep ($I_{D,0}$) and backward sweep ($I_{D,1}$) and its ratio ($I_{D,1}/I_{D,0}$) are shown as a function of the thickness of the PBL. Note that $I_{D,0}$ and $I_{D,1}$ will be used as a reading current for the state "0" and "1" of the memory cell, respectively.

In the ferroelectric OTFTs, the ferroelectric dipoles are aligned from bottom to top at the high negative gate voltage, and aligned from top to bottom at high positive gate voltage. The electric field of the remnant polarization of the bottom-to-top aligned ferroelectric layer allows holes to be accumulated at V_G = 0 V.

In the bilayer structure which is composed of lower ferroelectric layer and upper paraelectric layer, the electric field of the ferroelectric dipoles are screened by the paraelectric layer, which was reported in the metal-ferroelectric layer-paraelectric layer-metal capacitor structure [78]. Similarly, in the OTFTs with the PBL and ferroelectric bilayer structure, the charges induced by the electric field of the ferroelectric dipoles in the semiconductor at V_G = 0 V in the backward sweep is,

$$Q_{\text{semi}} = \frac{1}{1 + \left(\frac{C_{\text{ferro}}}{C_{\text{PBL}}}\right)} P \qquad (4.1)$$

Here, C_{ferro} is the intrinsic capacitance of the ferroelectric layer, C_{PBL} is the intrinsic capacitance of the paraelectric layer, and P is the remnant polarization at V_G = 0 V. The equation for the drain current at V_G = 0 V, which is modified from Ohm's law is

$$I_D = \frac{W}{L}\mu V_D Q_{semi} \qquad (4.2)$$

From eq. 4.1, 4.2, and $C_{PBL} = t\varepsilon_0^{-1}\varepsilon_r^{-1}$,

$$I_D \cong \frac{W}{L}\mu V_D \frac{1}{1+\left(\frac{C_{ferro}}{\varepsilon_0\varepsilon_r}\right)t} P \qquad (4.3)$$

Here, ε_0 is the dielectric constant, ε_r is the relative dielectric constant of the paraelectric layer, and t is the thickness of the paraelectric layer. With increasing t, I_D is decreased in Eq. 4.3 which is similarly shown in Fig. 4.5(b).

In contrast, at V_G = 0 V in the forward sweep, the drain current is dominantly affected by the gate leakage current due to the negligible drain-source current. Since, with increasing t, the gate leakage current decreases, $I_{D,0}$ decreases as shown in Fig. 4.5(b). $I_{D,1}$ decreases more rapidly than $I_{D,0}$ with increasing t, therefore, the memory on-off ratio ($I_{D,1}/I_{D,0}$) is decreased when increasing t. This is similar to the previous work for the high-k dielectric application [79].

In Fig. 4.5(c), the transfer curves of the same five OTFTs at a V_D = – 60 V are shown. The maximum drain current, minimum drain current, and their ratio in backward sweep of the transfer curves are presented as on-current, off-current, and on-off ratio, respectively, in Fig. 4.5(d). For t = 0 nm (with no PBL), the on-current is 0.61 μA. With increasing t, the on-current increases,

reaches a maximum value of 3.1 μA at t = 50 nm, and then decreases as low as 0.46 μA at d = 200 nm, as shown in Fig. 4.5(d). In the case where t < 50 nm, the PBL is not able to cover the whole area of the ferroelectric layer as shown in Fig. 4.4(b). Since the morphology of the PBL is smoother than that of P(VDF-TrFE) as shown in Fig. 4.4(a) and (c), the on-current increases with increasing the PBL-covered area. On the other hand, in the case where t > 50 nm, the on-current decreases due to the reduced capacitance of the bilayer insulator. The off-current monotonically decreases with increasing t, since the gate leakage current which is the major origin of the off-current decreases. The resultant on-off ratio shows maximum value of 2.6 $\times 10^4$ at t = 50 nm. Therefore, for the selection OTFT, the PBL thickness is chosen as 50 nm.

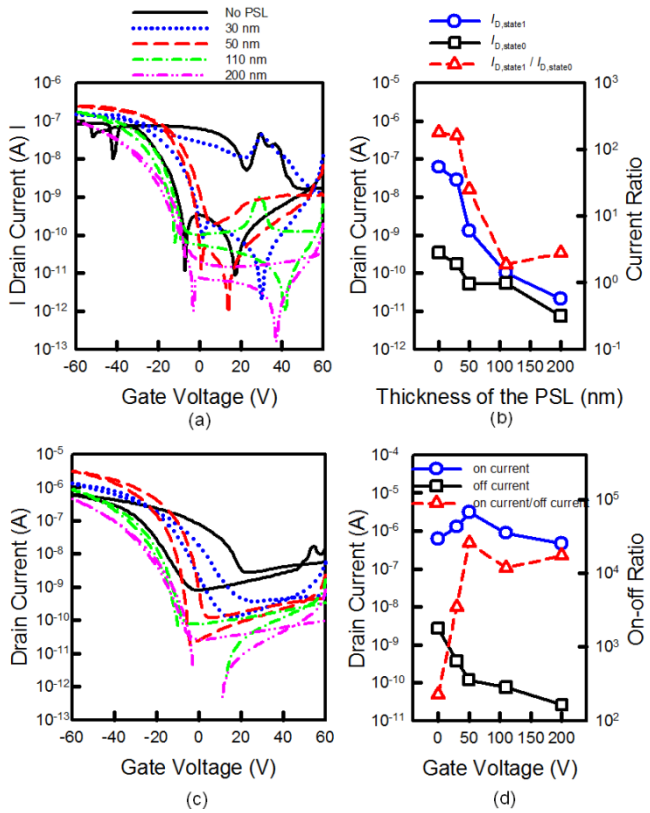

Figure 4. 5 (a) The transfer curves of OTFTs with no PBL and with various PBLs as a function of the gate voltage at V_D = − 5 V. (b) $I_{D,1}$, $I_{D,1}$, and current ratio of $I_{D,1}$ and $I_{D,0}$ as a function of the PBL thickness. Blue circles (blue solid line), black squares (black solid line), and red triangles (red dashed line) represent $I_{D,1}$, $I_{D,0}$, and $I_{D,1}$ / $I_{D,0}$. (c) The transfer curves of OTFTs with no PBL and with various PBLs as a function of the gate voltage at V_D = − 60 V. (d) On-current, off-current, and on-off ratio as a function of the PBL thickness. Blue circles (blue solid line), black squares (black solid line), and red triangles (red dashed line) represent on-current, off-current, and on-off ratio. Here, in (a) and (c), black solid curve, blue dotted curve, red dashed curve, green dash-dotted curve, and pink dash-dot-dotted curve represent no PBL case and 30, 50, 110, and 220 nm PBL cases, respectively.

4.4 Ferroelectric Memory Array

Based on the above results for the PBL in the OTFTs, we developed ferroelectric memory array with 2 x 2 matrix cells which consist of a storage OTFT and a selection OTFT. For a selection OTFT, the PBL (50 nm thick) was introduced on the top of the ferroelectric gate insulator to screen the electric field from ferroelectric dipole. The memory state where the ferroelectric dipoles are aligned from bottom to top is the state "1" which result in high reading current and the state "0" is the case for the reverse aligned dipoles causing low reading current. Based on the transfer curves in Fig. 4.5(c), the applied voltage at the data line for the state "1" and "0" is – 40 and + 40 V, respectively, and the applied voltage at the selection line for on- and off-operation of the selection OTFTs is – 60 and + 60 V. As shown in Fig. 4.6(a) and (b), the data are able to be written in each memory cell without the electrical interference between memory cells since the selection OTFTs suppress the current flow from data lines toward gate electrode of the memory OTFTs in the non-selected cells. In the reading operation, the applied voltage of the selection line for reading and for non-reading is –5 and 0 V, respectively. The reading current is 2.2 nA for the cell (0,0) and 45 nA for the cell (0,1) in the first row and 48 nA for the cell (1,0) and 1.5 nA for the cell (1,1) in the second row, as shown in Fig. 4.6(c) and (d). Therefore, the data are successfully read as written in writing operation.

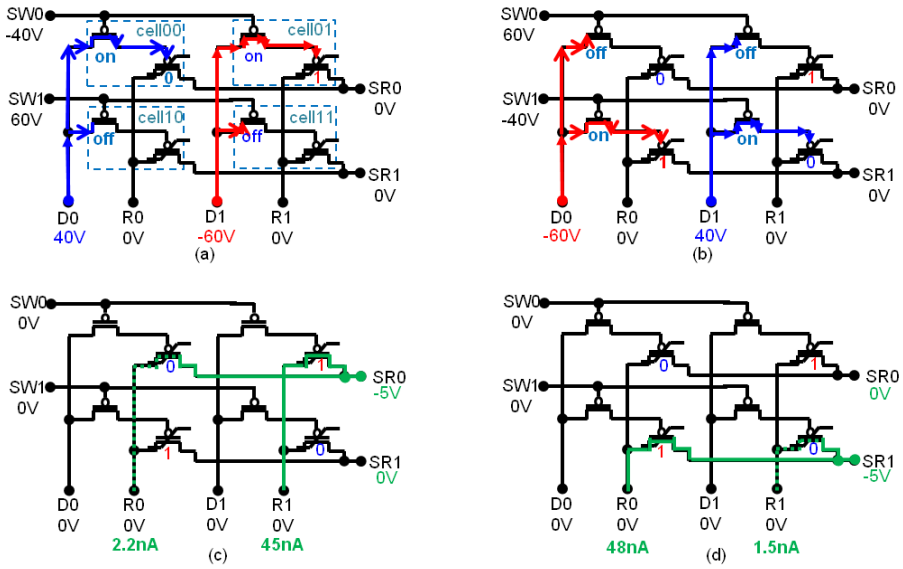

Figure 4. 6 Circuit diagrams of the writing/reading operation. Applied voltage for each line and resultant state of memory cell are presented. Red and blue color lines represent the negative data voltage path for state "1" and the positive data voltage path for state "0", respectively. Green lines represent the reading current path. (a) Writing "01" in the first row. (b) Writing "10" in the second row. (c) Reading the first row. (d) Reading the second row.

4.5 Intermediate States of Ferroelectric OTFT

It is described how the intermediate states of the ferroelectric insulator are programmed by the magnitude of V_P in terms of output current (I_{OUT}) of the FeOTFT. In Fig. 4.7(a), the transfer characteristic curve of the FeOTFT is shown. Compared to the sweeping range of V_G, the small drain voltage (–5 V) is applied to minimize the effect of V_D on the polarization of the ferroelectric insulator [74,75]. At V_G = 0 V, two memory states of ferroelectric layer corresponding the dipolar alignment states shown in Fig. 4.2(a) and (c) are observed through two values of I_D.

In order to program the intermediate memory states as shown in Fig. 4.2(b), the voltage was applied at the gate and drain electrodes as shown in Fig. 4.7(b). First, V_G of 60 V is applied for the erasing time (t_E) of 100 ms to fully erase the pre-programmed memory state. Note that at least t_E of 10 ms is required to fully reverse the ferroelectric dipoles in the FeOTFT [73]. After erasing the memory state of the ferroelectric insulator, V_P is applied at the gate electrode for the programming time (t_P) of 640 μs or 1280 μs to program the memory states. To read the memory state, I_D is measured as I_{OUT} at V_D = –5 V and V_G = 0 V for the reading time (t_R) of 640 μs.

Before programming the memory state, the dipole moments of the ferroelectric insulator were aligned as shown in Fig. 4.2(a) by the strong electric field from the gate electrode to the semiconductor. After programming the memory state under the condition that $|V_P| < V_C$ and $V_P < 0$, the dipole

moments are partially reversed as shown in Fig. 4.2(b) by the top-to-bottom electric field since the remnant polarization of the ferroelectric layer are affected by the magnitude of the applied voltage [80]. At $|V_P|$ near V_C, most of the dipoles are reversed by the strong top-to-bottom electric field. These reversed dipole moments attract holes in the organic semiconductor, which directly contribute to I_{OUT}.

Corresponding the above predicted states of the dipolar alignment of the ferroelectric layer, the magnitude of the measured I_{OUT} begins to gently increase near $V_P = -30$ V, rapidly enlarges near $V_P = -45$ V, and finally saturates beyond $V_P = -45$ V with increasing V_P toward the negative direction when $t_P = 1280$ μs as shown in Fig. 4.7(c). V_P at which the I_D begins to saturate is defined as the saturated programming voltage (V_{SP}). Here, V_{SP} is determined as –45 V whose magnitude is the similar value of V_C (46 V) calculated with the thickness of our ferroelectric layer from the measured coercive electric field of 74 MV/m in metal-ferroelectric insulator-metal structure [81].

In the intermediate states where $|V_P| < V_{SP}$ and $V_P < 0$, the behavior of I_{OUT} is consistent with the inverse first order approximation as shown in Fig. 4.7(d). That is, $I_{OUT} - I_{OUT0} = A_C(V_P - V_{SP})^{-1}$ where I_{OUT0} denotes a background value and A_C represents a characteristic constant. In fact, I_{OUT0} corresponds to the off-current including the channel off-current and the gate leakage current [82]. Fitting the experimental data to the above form of I_{OUT}, we have $A_C = 2.5 \times 10^{-8}$ W and $I_{OUT0} = 1.4 \times 10^{-9}$ A.

Figure 4.7(e) shows the retention property of intermediate states in terms of I_{OUT} at five different values of V_P = −10, −30, −35, −40, and −50 V. The ferroelectric intermediate memory states at V_P = −10, −30, −35, and −40 V is as stable as the retention property of the fully aligned state at V_P = −50 V. Therefore, the distinguishable values of I_{OUT} can be used as the multistate current-readable output for the nonvolatile memory, and the programmed FeOTFTs can be used as a DPT in a zero load inverter.

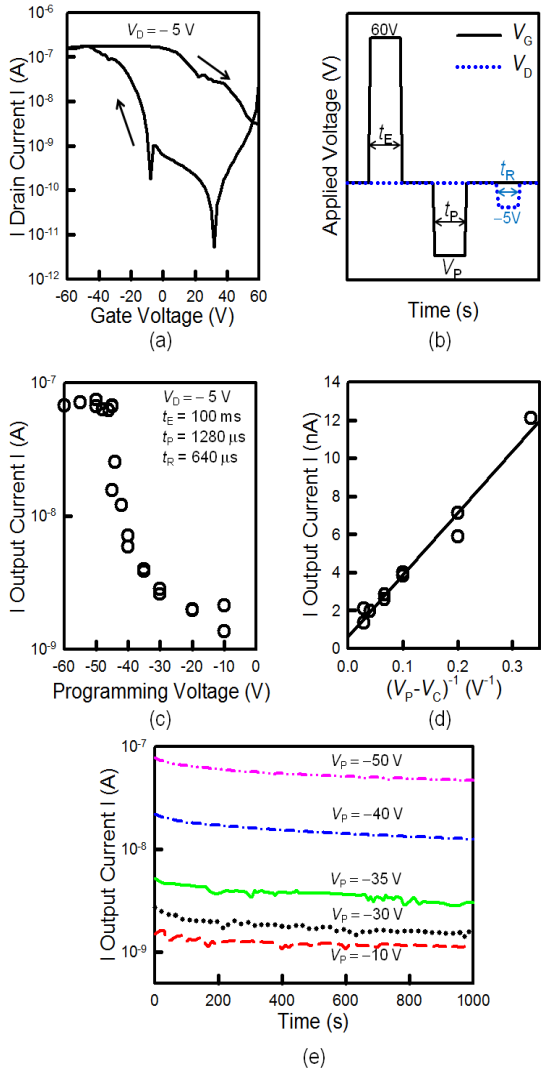

Figure 4.7 (a) The transfer characteristic curves of the FeOTFT at V_D = –5 V. (b) The timing diagram of the gate voltage and drain voltage. (c) I_{OUT} at V_D = –5 V as a function of V_P for t_P = 1280 µs. (d) I_{OUT} as a function of $(V_{SP} - V_{SP0})^{-1}$. (e) Output current as a function of the retention time.

4.6 Voltage-Readable Multistate Ferroelectric Memory

In order to convert the multistate current-readable output into the multistate voltage-readable output, a zero gate load inverter [83] with a DPT and an LFT was chosen as shown in Fig. 4.2(d) due to its simplicity and large range of voltage output. For a DPT, the PBL (50 nm thick) was introduced on the top of the ferroelectric gate insulator to eliminate the memory effect of the ferroelectric layer. In order to minimize the deterioration of the ferroelectric intermediate states of the FeOFET and to allow the enough current modulation of the DPT, the supplied voltage (V_{DD}) of the inverter is chosen as –15 V. The inset of Fig. 5(a) shows the voltage transfer curves of the inverter at four different values of V_P = –10, –30, –35, and –40 V, respectively. With increasing V_P to negative direction, I_{OUT} increases, resulting in the shift of the voltage transfer curves to more negative direction as shown in Fig. 4.8(a). In Fig. 4.8(b), the values of V_{out} at V_{BIAS} = –2 V are shown as a function of V_P. In order to obtain the enough voltage margins between output values, V_{BIAS} is determined as –2 V. The magnitude of V_{out} at V_{BIAS} = –2 V is increased when increasing V_P to negative direction. It is shown in Fig. 4.8(c) that the clearly distinguishable voltage outputs of the zero gate load inverter programmed at V_P = –10, –30, –35, and –40 V are retained. It is clear that the voltage-

readable nonvolatile memory cell with four memory states operates stable in the inverter configuration consisting of the LFT and the DPT.

This zero-gate load inverter-type memory cell is read-only-memory due to the connection between source and gate of the LFT as shown in Fig. 4.2(d). In order to realize ferroelectric multistate RAM, each cell should have selection OTFT as shown in Fig. 4.6. In this case, ferroelectric intermediate states can be programmed at each memory cell by the magnitude of data voltage. This multistate RAM could have noise problem. To solve this noise problem, leakage current in overlap area should be reduced, since memory array has numerous overlap areas. In the output state, load DPT can be inserted for voltage-readable output, which can be connected to the input of the amplification circuit. These approaches solve the noise problem.

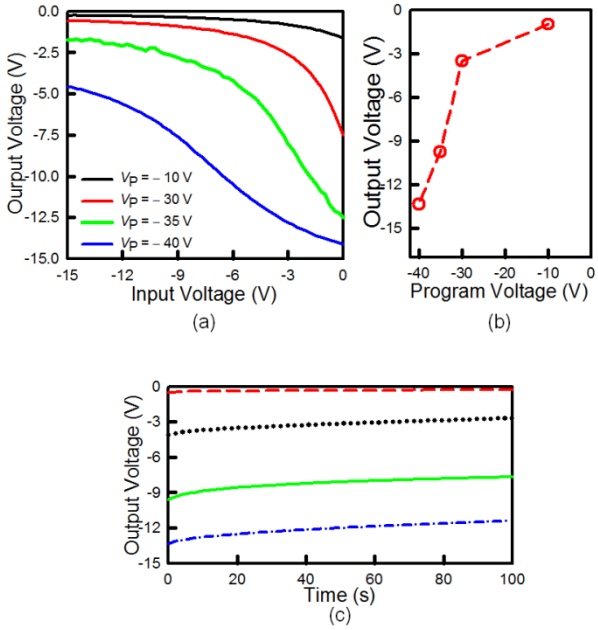

Figure 4. 8 (a) The voltage transfer curves of the ferroelectric inverter at four different values of V_P = –10, –30, –35, and –40 V. (d) V_{out} at V_{BIAS} = –2 V as a function of V_P. (c) $-V_{out}$ at V_{BIAS} = –2 V as a function of retention time at four different values of V_P = –10 (red dashed line), –30 (black dotted line), –35 (green solid line), and –40 V (blue dash-dotted line).

4.7 Summary

It is demonstrated how the PBL/ferroelectric bilayer structure affects the hysteresis of the FeOTFT. The role of the paraelectric screening layer (PBL) on the ferroelectric layer is to screen the electric field of the ferroelectric dipole and to reduce the roughness of insulator. It was found that the selective formation of the PBL on the ferroelectric insulator enables to laterally integrate both ferroelectric memory OTFTs and paraelectric OTFTs in a single substrate. Through this integration technique, ferroelectric memory array and voltage-readable inverter memory cell are demonstrated. This work is expected to provide a scientific basis for developing low-cost nonvolatile memory circuit.

Chapter 5. Conclusion

In this thesis, the advanced device architectures for the fabrication of the electronic functional blocks as well as the enhancement of the performance of the single OTFT are presented. The new patterning technology for the fabrication of the new device architecture is also demonstrated. Furthermore, it is presented how the interface between the gate insulator and the organic semiconductor affects the electrical properties of the OTFTs. Also, device physics for the proposed organic devices are presented.

In Chap. 1, the general overview of the organic electronics is introduced. The operation principles of an OTFT and ferroelectric OTFT are presented. It is demonstrated how the parameters of such devices affect the device performance. Furthermore, the operational principles and device parameters of the organic circuit such as an organic inverter is presented.

In Chap. 2, it is presented how device architectures have an influence on the performance of the single OTFT. First, in order to obtain saturated high drain current at low voltage, the chevron gate configuration is designed and fabricated. The chevron gate architecture gives short channel and very thin insulator. The large drain current is driven by the short channel and saturation behavior of the drain current is obtained by the very thin self-grown AlO_X. Furthermore, the short channel effect and current modulation is physically analyzed. Next, for the high performance OTFTs with the n-type polymer semiconductor, the dual-gate architecture is introduced. It is presented how

the driving method for top and bottom gate electrodes affects the electrical properties of the devices such as hysteresis, threshold voltage, and mobility. The dual-gate architecture allows the hysteresis free, low threshold voltage, and high mobility by the biasing the counter gate electrode.

In Chap. 3, a high noise-margin full-swing organic unipolar inverter consisting of only p-type OFETs on a single substrate is demonstrated. The V_{on} of the OFETs with the SPL is more positive than the V_{on} of the OFETs without the SPL. It is found that the SPL controls effectively the accumulation of holes in the p-type semiconductor due to the transverse dipolar field of the SPL of a fluorinated polymer. The accumulated interfacial holes at zero gate voltage provides the saturation behavior of the drain current and allows its magnitude to lie between the on-current and off-current of a conventional OTFT with no SPL, which directly leads the high noise-margin and the full-swing capability of an organic inverter.

In Chap. 4, organic circuits including ferroelectric OTFTs are presented. For the more practical use of the ferroelectric OTFTs, electronically functional cells are demonstrated by the introduction of the paraelectric /ferroelectric bilayer architectures. The ferroelectric OTFTs with the bilayer architecture operate similar to the conventional paraelectric OTFTs due to the screening effect of the electric field of the ferroelectric dipoles and reducing the roughness of the insulator. Based on this property of the ferroelectric OTFTs with the bilayer architecture, first, ferroelectric memory cell for the memory array is demonstrated. The normal ferroelectric OTFTs act as a memory OTFTs and the ferroelectric OTFTs with the bilayer architecture

operate as a selection OTFTs. Through integrating two OTFTs, ferroelectric nonvolatile memory array which is written and read without cross-talk are demonstrated. For the application of the complex circuits, voltage-readable memory cell with the ferroelectric multistates is also demonstrated. The intermediate states of the ferroelectric layer are programmed by the programming voltage. The multilevel output current of the programmed ferroelectric OTFTs is converted into the multilevel output voltage through combining the load ferroelectric organic thin-film transistor with the driving paraelectric organic thin-film transistor with bilayer structure.

In conclusion, through this thesis, it is presented that the advanced device architectures provide the realization of the functional circuits as well as the enhancement of the performance of the single device. Approaches of increasing the drain current and controlling the threshold voltage, introduced here, are expected to provide a basis for realizing many applications of the OTFTs. Moreover, the device physics and the integration technique for the organic inverter and ferroelectric circuit will provide a platform for the organic logic elements and nonvolatile memory cells.

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초 록

유기전자공학은 플렉시블 디스플레이나, RFID(Radio frequency identification tag), 센서 쉬트 (sensor sheet) 에 적합한 저가, 대면적, 유연성 전자소자를 제작할 수 있는 장정이 있어서 많은 관심을 끌고 있다. 특히 트랜지스터 고유의 드라이빙 특성과 스위칭 특성을 가지는 고성능 유기박막트랜지스터에 관한 많은 연구가 이루어지고 있다. 최근에는 유기박막트랜지스터의 상업화를 위하여 단일 소자에 관한 연구는 물론 단일 소자를 조합한 전자 기능 블록에 관한 연구가 이루어 지고 있다. 이러한 고성능 소자와 기능 블록의 구현을 위한 적합한 방법 중 하나가 새로운 소자의 구조를 적용하는 것이다.

본 논문에서는 단일 소자의 성능 향상과 전자 기능 블록의 구현이라는 관점에서 새로운 유기박막 트랜지스터의 구조를 제안하고 이러한 소자를 공정적인 측면과 물리적인 이해 관점에서 논의하였다. 특히 게이트 절연막과 유기 반도체 사이의 계면현상에서 오는 물리적인 현상에 관하여 논의 하였다. 이를 위하여 우선 유기전자공학에 대한 전반적인 소개를 하고 유기박막 트랜지스터의 작동 원리에 대해 기술하고, 어떠한 요소들이 단일 소자와 논리소자, 기억소자의 성능에 영향을 미치는 지를 논의 하였다. 특히 게이트

절연막과 채널 사이의 계면이 어떻게 소자의 성능에 영향을 미치는지를 중점적으로 논하였다.

단일 소자 수준에서 소자 구조가 성능에 어떠한 영향을 미치는 지 제시하였다. 저전압에서 포화된 고전류를 얻기 위한 chevron gate 구조를 제안하고 제작하였다. 이에 따르는 단채널 효과와 전류 변화에 대하여 논하였다. 또 n 형 고분자 반도체를 이중게이트 구조에 적용하여 문턱전압과 이동도에 어떠한 영향을 미치는 지를 알아보았다.

다음으로 서로 다른 성질을 가지는 두 개의 유기박막 트랜지스터를 조합하여 기능블럭으로 사용하기 위한 구조를 제안하였다. 우선 표면 극성층의 도입을 통하여 증식형 유기박막 트랜지스터와 공핍형 유기박막 트랜지스터를 조합한 단극성 반전기 회로를 제작하였다. 증식형 유기박막 트랜지스터를 위한 게이트 절연막 위에 표면이 극성을 띠는 고분자 층을 전사함으로써 간단하게 공핍형 유기박막 트랜지스터를 위한 게이트 절연막을 만들어 내었다. 같은 유기 반도체를 사용하더라도 상이한 성질의 계면이 나타나게 된다. 이로 인한 계면의 특성과 트랜지스터의 성능 변화가 분석되었다.

또한 상유전성 방지층을 도입함으로써 강유전성 유기박막 트랜지스터와 상유전성 유기박막 트랜지스터를 조합한 유기 회로를 제작하였다. 강유전성 게이트 절연막 위에 상유전성 층을

전사함으로써 부분적으로 강유전성 유전체의 성질을 사라지게 하여서 상유전성 유기박막 트랜지스터와 강유전성 유기박막 트랜지스터가 집적되게 하였다. 상유전성 방지층의 도입에 따른 성능 변화와 물리적인 분석이 이루어 졌고 혼선이 없는 비휘발성 메모리 어레이와 전압 출력을 가지는 비휘발성 메모리 셀이 제작되었다.

결론적으로 본 논문에서는 소자의 구조 변화가 단일 소자의 성능 향상과 기능블럭의 구현을 가능하게 함을 보였다. 이와 함께 각 소자의 성능에 대한 물리적인 분석과 함께 같은 반도체라도 어떠한 게이트 절연막의 사용에 따라서 다른 성질을 갖게 됨을 보였다. 본 연구에서 밝힌 새로운 소자의 구조는 논리 연산을 위한 회로와 비휘발성 메모리의 집적을 위한 연구에 기반을 제공할 수 있을 것으로 기대된다.

주요어: 유기박막 트랜지스터, 계면 작용, 유기 반전기, 강유전성 고분자, 비휘발성 메모리

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감사의 글

6 년 반의 석박사 통합과정을 마치며 학위를 받게 되었습니다. 학문적인 것을 넘어서 삶의 많은 것을 배울 수 있는 시간이었던 것 같습니다.

아름답게 창조된 자연의 질서를 탐구하고 그 원리를 조금씩이나마 이해하고 응용해 나갈 때 神妙莫測한 하나님의 창조 섭리에 경탄을 금할 수 없었습니다. 神의 인도하심을 따라서 한걸음씩 나아가며 그 길의 의미를 깨달아 나갈 때마다 감사로 마음이 가득 찹니다.

학위과정 동안 도움을 주신 많은 분들께 감사 드립니다.
무엇보다도 학문적으로 인격적으로 이끌어 주신 이신두 지도 교수님께 감사 드립니다. 학자의 본을 보여주신 그 가르침은 제 삶의 가장 큰 보배입니다. 바쁘신 시간을 내어 논문 심사를 지도해 주신 이병호 교수님, 박남규 교수님, 최종선 교수님, 배진혁 교수님께도 깊은 감사를 드립니다.

학위 기간 동안 함께 했던 연구실의 선후배 동기 분들께도 감사를 드립니다. 훌륭한 연구실 동료들과의 치열한 토론을 통하여 더욱 깊고 넓은 연구를 할 수 있었습니다.

지난 33 년간 저를 위해 늘 기도해주시고 위로해주신 부모님께 감사 드립니다. 묵묵히 저를 항상 믿어준 형과 형수님께도 감사 드립니다.

항상 자상함으로 귀하게 생각해주시는 장인 장모님께도 감사 드립니다. 그리고 많은 대화를 나누며 저를 위해 기도해준, 학문의 길을 시작하는 처남에게도 고맙다는 말을 전하고 싶습니다.

초등학교부터 학위를 마칠 때까지 지칠 때마다 함께 해준 친구들에게도 감사 드립니다. 10 여 년간 몸 담았던 청년부의 형제자매들과 교회 분들께도 감사 드립니다.

마지막으로 사랑하는 아내 영미에게 너무나 고맙다는 말을 전하고 싶습니다. 기쁘고 즐거운 날 뿐만 아니라 어렵고 힘든 날도 사랑과 배려로 함께 해주는 모습이 항상 큰 힘이 되었습니다. 이제 태어난 새 생명인 태준이와 아내를 위해 최선을 다하는 훌륭한 연구자로 더욱 정진하겠습니다.