A DISSERTATION FOR THE DEGREE OF DOCTOR OF PHYLOSOPHY

AlGaN/GaN Power Devices Employing RF-Sputtered Gate Insulator

RF-스퍼터링 게이트 절연막을 이용한 AlGaN/GaN 전력 소자

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Abstract

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This dissertation is intended as an investigation of AlGaN/GaN metal-oxide-semiconductors-high-electron-mobility transistors (MOS-HEMTs) employing RF-sputtered gate insulator to suppress leakage current and obtain high breakdown voltage. Also, material properties of RF-sputtered films and interface characteristics between GaN and gate insulator were studied. In addition, various device structures based on the MOS-HEMTs were proposed to improve devices performance and their electrical properties were verified.

AlGaN/GaN HEMTs have received a considerable amount of attention for high-power applications due to their wide bandgap properties, such as a high critical electric field, a high thermal conductivity, and a low intrinsic carrier concentration. In addition, an AlGaN/GaN heterostructure offers high-density and high-mobility two-dimensional electron gas (2DEG) by piezoelectric polarization between AlGaN barrier and GaN buffer layer, meaning that

AlGaN/GaN HEMTs exhibit a high breakdown voltage and a low on-resistance.

However, the surface leakage current by an electron trapping and trap-assisted tunneling at the Schottky/GaN interface are critical issues in the AlGaN/GaN heterostructure devices. Suppression of the leakage current and high breakdown voltage are indubitably important to achieve a low off-state power loss and high-conversion efficiency without device failure. The MOS is suitable structure for the high-voltage AlGaN/GaN HEMTs because the gate insulator suppresses the leakage current and effectively prevent the parasitic diodes operation from gate-source and gate-drain SBDs.

The RF-sputtered HfO_2 was studied for uses in the gate insulator of the AlGaN/GaN MOS-HEMTs and sputtering conditions such as sputtering power and working pressure were optimized. The electrical and materials properties of HfO_2 at the various sputtering conditions were verified by X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and Auger electron spectroscopy (AES). Also, the effects of post-deposition annealing (PDA) on the HfO_2 were investigated. The high breakdown voltage in the test pattern including 15 nm-thick HfO_2 on p-type Si substrate was increased from 42 to 78 V after PDA at 900 ^{o}C for 2 hours.

The AlGaN/GaN MOS-HEMT-on-Si using RF-sputtered HfO_2 gate insulator exhibited the high breakdown voltage of 1524 V, the low drain leakage current of 67 pA/mm at V_{DS}= 100 V and V_{GS}= –10 V, and high on/off current ratio of 2.37×10^{10} while the conventional HEMT had 470 V, 192 μA/mm, and 7.61×10^{3}, respectively. The improvement mechanism of breakdown voltage through HfO_2 gate insulator was studied by measuring various electrical characteristics. This was done with the separated two-factors including passivation effects and blocking capability of HfO_2 gate insulator. Both forward- and reverse-gate blocking characteristics of the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator were evaluated. In addition, suppression of

electron trapping due to surface passivation was verified by pulsed current-voltage (*I-V)* characteristics and capacitance-voltage (*C-V*) characteristics. Finally, interface traps density (D_{it}) was evaluated by terman's method and high-frequency *C-V* characteristics so that D_{it} of 6×10^{12} $cm^{-2}\cdot eV^{-1}$ at the energy level of 0.1 eV below conduction energy minimum.

Au-free fabrication is promising technologies for the CMOS-compatible process of the AlGaN/GaN devices. Also, it has an advantage in terms of the fabrication cost and large-wafer process. TaN was proposed to replace the gold-based electrodes in the AlGaN/GaN MOS-HEMTs-on-Si. The material and electrical properties were verified after PDA by XRD, scanning electron microscopy (SEM), and 4-point probe. Also, the sputtering conditions such as sputtering power and working pressure were optimized to obtain the low-resistance electrode and suppress sputtering damage to HfO_2 gate insulator. The TaN-gate AlGaN/GaN MOS-HEMTs with 15 nm-thick HfO_2 gate insulator showed high on/off current ratio of 4.56×10^{10} and high breakdown voltage of 1460 V at gate-drain distance of 10 μm. Also, the fully Au-free devices using TaN-gate and Ti/Al/TaN-source/drain showed on/off current ratio of 2.0×10^{9} without any considerable degradation.

The extended-gate structure was proposed to reduce specific on-resistance ($R_{on,sp}$) without any additional GaN epitaxial growth and lithography techniques by removing the redundant gate-source space in the AlGaN/GaN MOS-HEMTs-on-Si. The extended TaN-gate overlapped source with 15 nm-thick HfO_2 insulation. By using this structure, the $R_{on,sp}$ was successfully reduced from 2.91 to 2.28 $m\Omega\cdot cm^2$ in the device with 10 μm-long $L_{GD.}$ High-*k* characteristics and higher dielectric breakdown voltage of the HfO_2 gate insulator than $|V_{TH}|$ facilitated the stable on/off switching. This device also exhibited high breakdown voltage of 1410 V, high on/off current ratio of 4.97×10^{10}, and high figure-of-merit of 872 $MW\cdot cm^{-2}$.

A new method to increase the breakdown voltage trough RF-sputtered Ga_2O_3 and Al_2O_3 films without any termination structure was proposed. The sputtering power considering sputtering damage to the GaN surface was optimized to suppress the leakage current. An electron injection into the unintentionally formed deep traps in the amorphous β-Ga_2O_3 films extended depletion region under the gate and increased the breakdown voltage. The deep traps have a relatively long emission time so that the surface leakage current, which is originated from the shallow traps, would be suppressed. The AlGaN/GaN HEMT-on-SiC with 20 μm-long L_{GD} and Ga_2O_3 passivation sputtered at 50, 100, 150, and 200 W exhibited breakdown voltage of 1430, 890, 820, and 460 V, respectively while that of the unpassivated device was 520 V. Also, high breakdown voltage exceeding 2.7 *k*V at sputtering power of 50 W and 40 μm-long L_{GD} was obtained. In addition, Al_2O_3/Ga_2O_3 multiple stacks by RF-sputtering were employed to reduce the leakage current and shift threshold voltage positively in the AlGaN/GaN HEMTs-on-Si. The breakdown voltage in the device using the stacks was increased from 380 to 1104 V and drain leakage current was decreased from 1.8 μA/mm to 33 nA/mm by the electrons accumulation in the stacks. The threshold voltage was shifted from –2 to –1.4 V and this was shifted to 0.12 V after DC stress at V_{GS}= –10 V for 100 s.

Keywords: AlGaN, GaN, high-electron-mobility transistors (HEMT), MOS-HEMT, gate insulator, HfO_2

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Chapter 1

1. Introduction

1.1 Background

In recent years, power devices have received considerable attention arising from environmental consciousness and energy-saving issues. To realize future power system with high conversion efficiency, low power loss, and compact size, power devices require high breakdown voltage, low on-resistance, and thermal stability. Particularly in electric vehicle, high-performance devices are essential for efficient battery management and stable operation.

Power devices have been developed by Silicon technology and new structures such as trench gate, reduced surface field (RESURF), and

superjunction. Silicon has several advantages compared to other materials in terms of easy formation of insulation layer using oxidation methods, easy doping using ion implantation and drive-in process. However, Si technology for power devices has already approached its theoretical limitation, so that wide bandgap materials such as GaAs, GaN, and SiC have been considered as breakthrough [1]. Figure 1-1 shows the development of power devices since 1970s [2]. This time diagram indicates that wide bangap-based power devices have been required to obtain high-power density and high-conversion efficiency for the future power system.

In general, the critical electric field is proportional to the bandgap to a power of 2.5. Thus, wide bandgap materials-based devices enable thinner drift region and smaller area for same devices performance as Si-based devices as shown in Fig. 1-2 [3]. In addition, a low intrinsic carrier concentration and a low probability of band-to-band emission enable the efficient power conversion and high-temperature operation without bulky cooling system from electric system point of view. The theoretical properties of various semiconductor materials are summarized in Table 1-1 [3, 4, 5]. It is noted that GaN has high critical electric field, high electron mobility, and high saturation velocity compared with Si, GaAs, and SiC. Therefore, GaN is promising and suitable material for future high-power systems such as electric vehicle, hybrid vehicle, and fuel-cell vehicle.

Among the wide bandgap materials, SiC has been studied for a long time. Recently, SiC Schottky Barrier Diodes (SBDs) was commercialized. SiC-based metal-oxide-semiconductor field-effect-transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs) have been developed as well. However, the potential of SiC-based power devices has been still questionable because of high growth and fabrication cost. Diamond is expected to be next-generation power semiconductors material due to superior material properties. However,

diamond has the problems of impurity doping and deep-carrier activation energy. The difficult fabrication of diamond should be solved [6].

The figure of merits (FOMs) are commonly used to compare the materials-limitation. In 1965, Johnson derived the following FOM.

$$\text{Johnson's FOM} = \left(\frac{E_c V_{sat}}{\pi} \right)^2 \qquad (1.1)$$

E_c and V_{sat} are the critical field and the saturation velocity, respectively [7]. In the Johnson's FOM, the critical field and the saturation velocity limit the performance of typical devices. In 1982, Baliga derived the new FOM for power FETs,

$$\text{Baliga's FOM} = \varepsilon \cdot \mu \cdot E_G^3 \qquad (1.2)$$

, which was the FOM to minimize the conduction loss in power FETs [8]. The ε, μ, and E_G are permittivity, mobility, and energy gap of semiconductor materials, respectively. Baliga's FOM is based upon the assumption that the power dissipation of devices is originated from the only current flow through channel. The calculated values for Si, GaAs, SiC, and GaN are summarized in Fig. 1-3. It should be noted that GaN has the highest values among the other semiconductor materials in both Baliga's and Johnson's FOM so that GaN-based semiconductors are suitable for the future power system.

However, GaN has several obstacles to be applied for MOSFETs or IGBTs due to its material limitation. Above all, obtaining high-quality interface characteristics between GaN and gate insulator is very difficult. A low interface trap density is desired to modulate surface potential and form inversion channel. A few results in terms of the thermally grown Ga_2O_3 layer in the GaN

devices after high-temperature oxidation have been reported [9]. It is well known that high-temperature annealing may cause serious decomposition problems in the GaN devices so that interface characteristics are limited by N-vacancies [10]. For the reason, heterogenous gate insulator by various deposition methods such as chemical vapor deposition (CVD) [11] and atomic layer deposition (ALD) [12] has been developed for GaN MOSFETs. However, successful fabrication and operation have been demonstrated scarcely.

Another problem is the impurity doping for p-type GaN. Mg-based mixture are widely added during p-GaN growth. It is known that maximum hole-concentration is about 10^{19} cm^{-3} in p-GaN due to high activation energy and very low activation ratio about 1 %. The high resistive p-GaN causes a considerable voltage drop across PN or PiN junction and relatively high knee voltage. Furthermore, GaN exhibits a low hole mobility of 10 $cm^2/V{\cdot}s$ so that GaN-based bipolar devices are not desirable [3]. In addition, irreversible ion implantation damage by thermal annealing in GaN are more serious problem because GaN MOSFETs require multi-step ion implantation for V_{TH} control and formation of n- or p-type well.

For the reasons discussed above, modulation doping using heterojunction has been widely used for GaN FETs. The discontinuous conduction band across two-heterogenous materials offers highly conductive channel at their interface. That channel is called by two-dimensional electron gas (2DEG) [13]. The methods have been applied to various III-V devices such as GaAs, InP, and InSb-based high-electron-mobility transistors (HEMTs). III-Nitride heterojunction has unique polarization charges in the interface due to their wurtzite structure and lattice mismatch as shown in Fig. 1-4 [14]. The spontaneous and piezoelectric polarization in III-Nitride devices provide higher 2DEG density compared to other materials. Especially, AlGaN/GaN heterostructure has an advantage over other III-Nitride combination because

of high electron density in 2DEG and breakdown field. Figure 1-5 shows 2DEG channel formed by conduction band discontinuity and polarization in the AlGaN/GaN heterojunction system [15]. It is noted that the highly conductive channel at AlGaN/GaN interface and high breakdown field are suitable to achieve the low on-resistance and the low power loss.

The high Al composition in the AlGaN barrier results in large band discontinuity, improvement of carrier confinement, strong piezoelectric polarization, high sheet charge, and high breakdown field [5]. However, high Al composition restricts the critical thickness of AlGaN due to the larger lattice mismatch at the AlGaN/GaN interface than low Al composition. Thin AlGaN exhibits a low electron mobility and density in 2DEG channel. Moreover, the high Al composition increases the ohmic contact resistance. Thus, AlGaN barrier layer should be designed for its applications.

Lack of the native GaN substrate is a critical issue in the AlGaN/GaN HEMTs. Sapphire, SiC, and Si have been widely used for substrate. The mismatches in lattice and thermal coefficient between substrate and GaN strongly influence on the wafer quality and device performance. Large mismatch causes wafer bowing and dislocation, which is line trap from substrate/GaN interface. Mismatches of lattice and thermal coefficient between GaN and substrate are summarized in Table 1-2 [16]. Among the substrate materials, SiC has the smallest mismatch in terms of lattice and thermal coefficient with GaN so that the low dislocation density and high devices performance are expected. Currently, only a few companies have produced SiC substrate so that the price is usually higher than other materials. Also, the wafer size has been not over 6 inch until now. Sapphire has been studied to reduce growth cost. The low thermal conductivity and large mismatch in both lattice and thermal conductivity between Sapphire and GaN still impose constraints on wafer quality and devices performance. Moreover,

2 and 4 inch-sized Sapphire substrate still have been widely used for GaN growth until now.

Si substrate is very promising for the AlGaN/GaN HEMTs due to its low cost and large available wafer size. However, large lattice mismatch with GaN causes serious dislocation and wafer bowing problems so that growth technologies for transition layer should be developed. Recently, thick Si substrate over 1 mm has been used to suppress wafer bowing. Also, multiple layer of superlattice, which consists of AlGaN and AlGaN over 100 layers has been reported to relax the mechanical stress during the GaN growth.

Recently, based on the excellent material characteristics of GaN, high-performance GaN power devices have been demonstrated as shown in Fig. 1-6. 70 A-AlGaN/GaN hybrid MOS-HEMT using p-GaN buffer and multi-fingers structure has been demonstrated [17]. Moreover, Transphorm has released GaN-on-Si transistor which was qualified for the joint electron device engineering council (JEDEC) standard [18]. Also, IMEC has reported 8 inch Au-free AlGaN/GaN MOS-HEMT-on-Si using Cu-based electrodes [19].

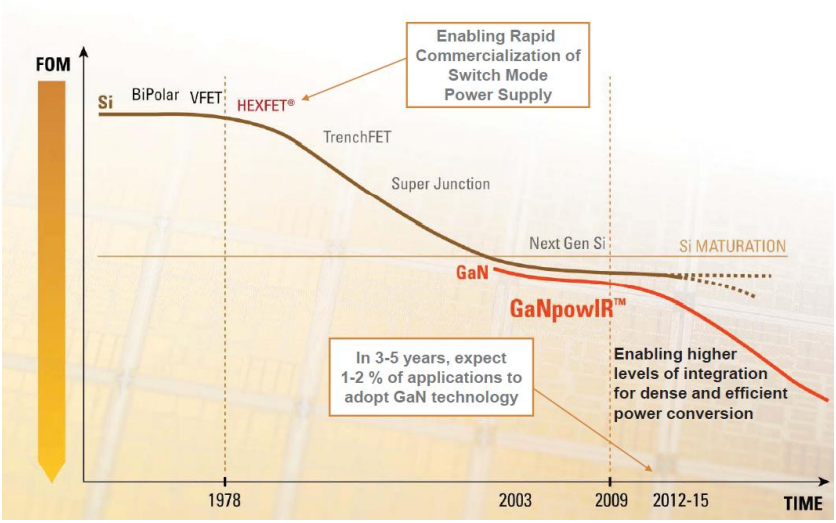
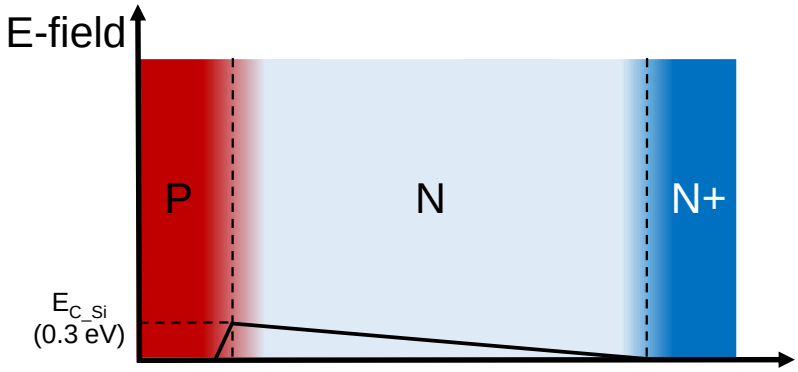


Figure 1-1: Silicon-limitation and potential of GaN power devices [2].



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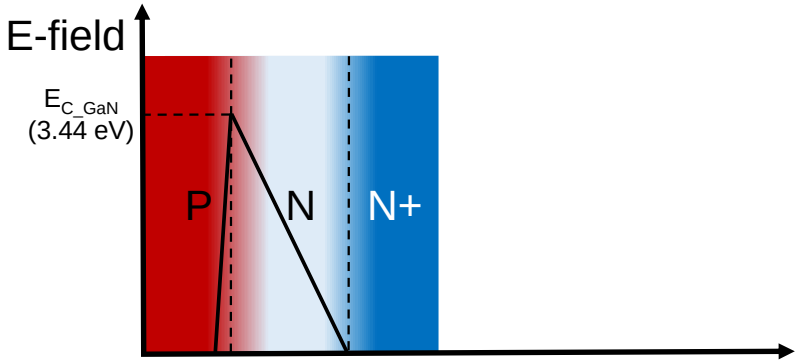


(b)

Figure 1-2: Electric field distribution when device's breakdown situation for (a) Si-PiN system (b) GaN-PiN system.

Table 1-1: Material properties of semiconductors [3, 4, 5].

		Si	GaAs	GaN	SiC		Diamond
					4H	6H	
Bandgap at 300 ^{o}C (eV)		1.12 Indirect	1.42 Indirect	3.44 Direct	3.25 Indirect	2.86 Indirect	5.46-5.60 Indirect
Bulk mobility at 300 K ($cm^2/V{\cdot}s$)	Electron	1400	8500	900	700	330-400	2200
	Hole	450	400	10	NA	75	1800
Saturation velocity (10^7 cm/s)		1	2	2.5	2	2	3
Critical field (10^6 V/cm)		0.3	0.4	3.5	3.2	2.4	7
Thermal conductivity (W/cm·K)		1.3	0.55	1.1	4	5	6-20

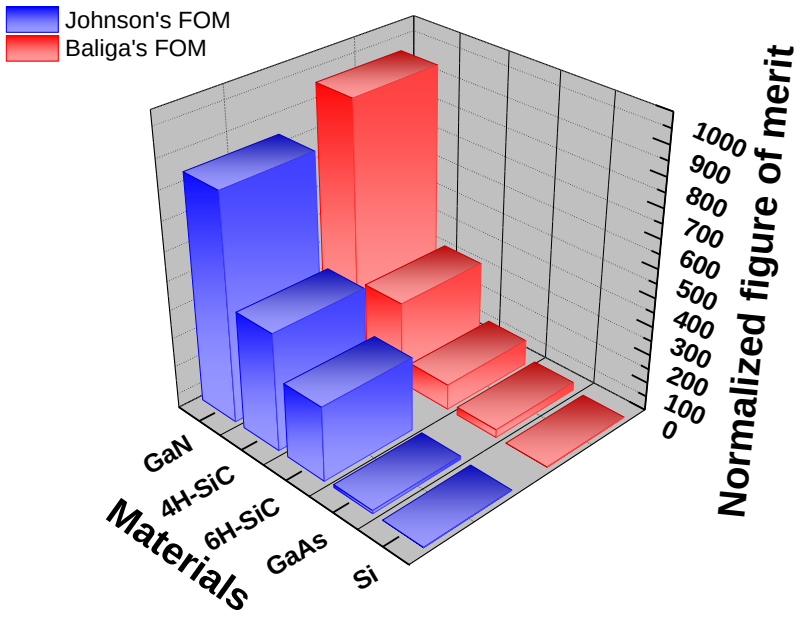
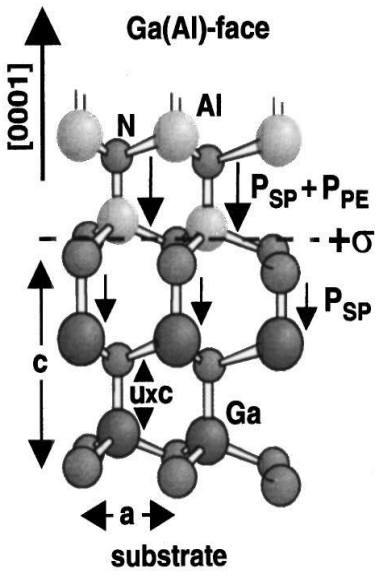


Figure 1-3: Baliga's and Johnson's figure of merit (FOM) for various semiconductors.



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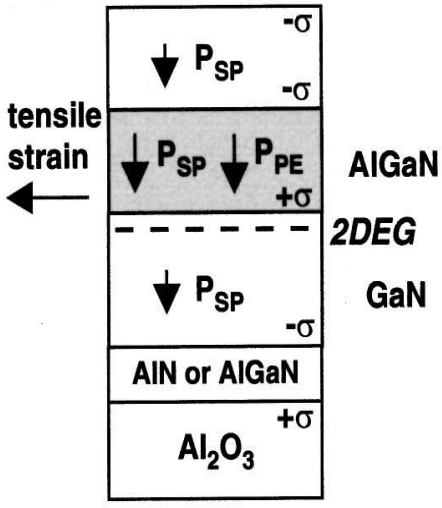
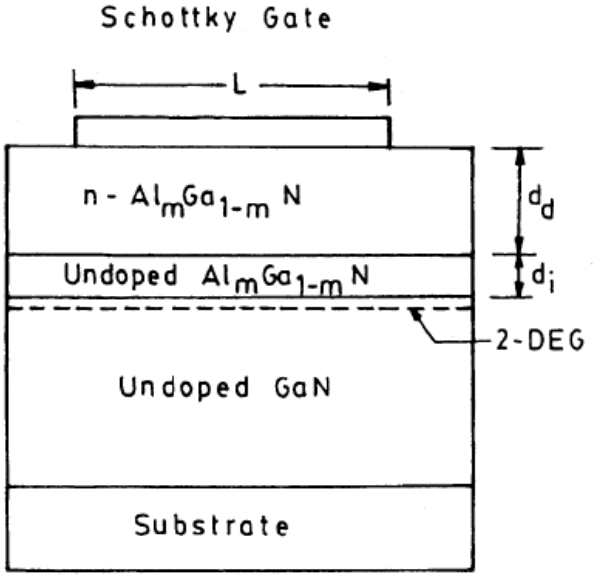


(b)

Figure 1-4: Ga (Al)-face AlGaN/GaN (a) crystal structure (b) polarization induced sheet charge, piezoelectric, and spontaneous polarization [14].



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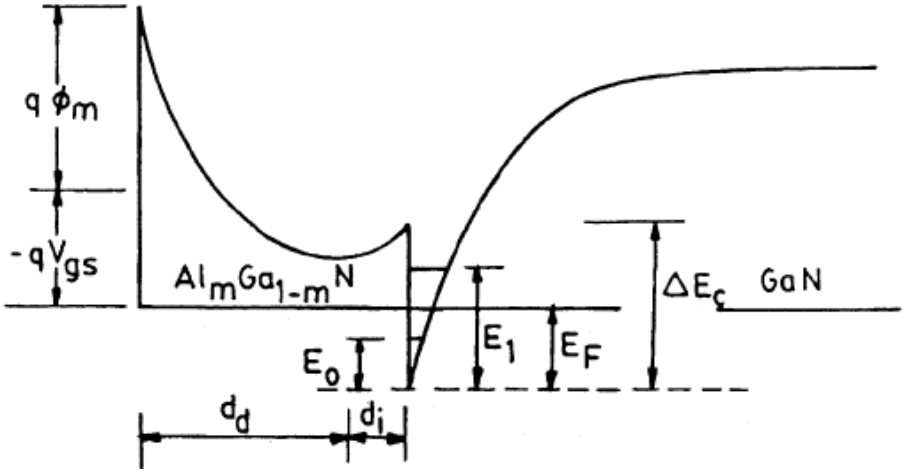
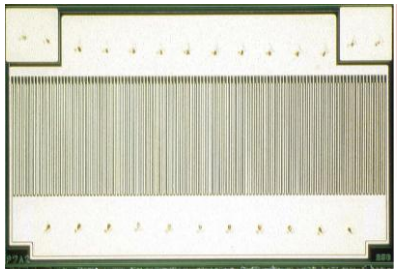


(b)

Figure 1-5: (a) Conventional structure of AlGaN/GaN HEMT (b) energy band diagram of AlGaN/GaN HEMT [15].

Table 1-2: Crystal and thermal properties of various substrates [16] .

	Lattice constant (Å)	Typical growth plane	Lattice mismatch with GaN	Thermal expansion coefficient
6H-SiC	a=3.081 c=5.7034	(0001)	3.51 %	a=4.2 c=4.68
Sapphire	a=4.765 c=12.982	(0001)	13.9 %	a=7.5 c=8.5
Si	A=5.431	(111)	–16.96 %	3.9



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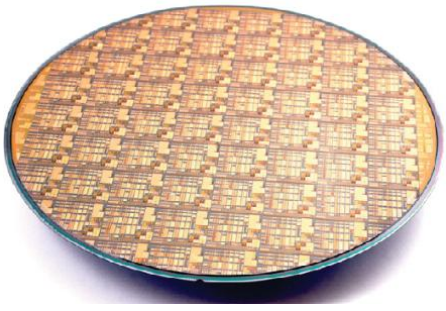
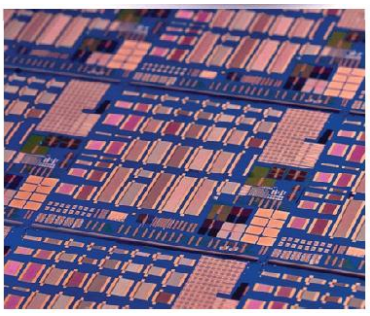




(c)

Figure 1-6: Demonstrated GaN power devices (a) multi-fingers AlGaN/GaN hybrid MOS-HEMT for high-current over 70 A (b) JEDEC-qualified 600 V-GaN-on-Si transistor (c) 8 inch GaN-on-Si MIS-HEMT device [17, 18, 19].

1.2 Dissertation organization

This purpose of this dissertation is to show new methods to achieve the high-performance AlGaN/GaN devices by using RF-sputtered films. RF-sputtered gate insulator and electrodes have been proposed and investigated for high breakdown voltage and low on-resistance. In addition, a new device design is proposed to increase FOM of the AlGaN/GaN power devices.

Chapter 2 describes the overview of AlGaN/GaN devices for power applications. The basic structure and fabrication process are introduced. Then, key issues which limit the electrical properties of the AlGaN/GaN devices are provided. Also, recent studies to improve device performance by using passivation, edge termination structures, and GaN buffer growth are reviewed.

Chapter 3 introduces high-quality HfO_2 gate insulator by RF-sputtering for the AlGaN/GaN MOS-HEMTs. Firstly, material and electrical properties of the RF-sputtered HfO_2 are characterized and the effects of crystallization by post-deposition annealing on HfO_2 insulator are followed. Secondly, various electrical properties of the AlGaN/GaN MOS-HEMTs are analyzed in order to verify the improvement mechanism of breakdown voltage. The reason to improve reverse characteristics is separated into two factors including surface passivation and blocking gate leakage current.

Chapter 4 provides a new Au-free fabrication for the AlGaN/GaN MOS-HEMTs using TaN-based electrodes. Material and electrical properties of the RF-sputtered TaN-electrodes are characterized after various post-deposition annealing are characterized. Also, I propose an extended TaN-gate structure, which overlaps source with HfO_2 insulation, for low on-resistance in the AlGaN/GaN MOS-HEMTs.

Chapter 5 focuses on methods to achieve high breakdown voltage of the AlGaN/GaN HEMTs by employing RF-sputtered Ga_2O_3-based films. The suppression of leakage current and breakdown voltage improvement by Ga_2O_3 and multiple Al_2O_3/Ga_2O_3 stacks are studied. Also, charge accumulation and shift of threshold voltage (V_{TH}) due to multiple Al_2O_3/Ga_2O_3 stacks are characterized.

Finally, Chapter 6 summarizes electrical and material characteristics of the devices proposed in this dissertation.

Chapter 2

2. Review of AlGaN/GaN Power Devices

2.1 Device Structure, Operation, and Fabrication

AlGaN/GaN high-electron-mobility transistors (HEMTs) have been demonstrated for high-power applications due to their superior material properties such as high critical electric field over 3 MV/cm, intrinsic carrier concentration (n_i) of 10^{-10} cm^{-3}, and high electron mobility over 1800 cm/V·s. Typical device structure and its operation of the AlGaN/GaN HEMTs are shown in Fig. 2-1. A transition layer is grown on heterogeneous substrate to reduce the mechanical stress arising from lattice and thermal mismatch between GaN buffer and substrate. An AlN spacer and an AlGaN barrier are grown to form

highly conductive channel which is located at the AlGaN/GaN hetero-interface. The AlGaN/GaN HEMTs have three terminals which are source, gate, and drain. These three-electrodes in the AlGaN/GaN HEMT are formed on the GaN surface.

Channel modulation of the AlGaN/GaN HEMTs is controlled by the Schottky-gate. In general, the AlGaN/GaN HEMTs have laterally asymmetry structure from gate to sustain high drain bias during off-state. The AlGaN/GaN HEMTs typically have negative V_{TH} due to the 2DEG channel. Figure 2-1 shows forward operation of the AlGaN/GaN HEMTs when $V_{GS}>V_{TH}$. Electrons flow from source to drain through 2DEG channel and highly conductive ohmic alloy. When $V_{GS}<V_{TH}$, the Schottky-gate makes the 2DEG channel depleted so that the electron is transferred from channel to GaN buffer. This depletion region under gate blocks the current flow through 2DEG channel. In theoretical situation, surface states can be ignored, the electric field concentration and breakdown occur at the gate edge by avalanche multiplication.

Here, I describe the fabrication procedure of the AlGaN/GaN MOS-HEMTs. This devices including MOS structure studied in this dissertation have various merits in respect of reverse blocking characteristics and electrical stability. The detail operation of the AlGaN/GaN MOS-HEMTs is taken up in the next chapter. Fabrication of the AlGaN/GaN MOS-HEMTs typically includes mesa isolation, drain/source formation, gate insulator deposition, gate formation, and pads opening. Additional processes can be added, for instance, second passivation and gate and/or drain field plates. The fabrication process of the conventional AlGaN/GaN MOS- HEMTs is shown in Fig. 2-2.

Firstly, etching process for device-to-device isolation and defining active region is performed. GaN cap/AlGaN barrier/AlN spacer should be eliminated by etching over total thickness of their stacks to cut off the 2DEG channel. GaN Buffer layer at an active region after mesa isolation sustains high drain voltage

so that its resistivity is very important. In order to improve resistive properties of GaN buffer layer, carbon (C) [20] and iron (Fe) [21, 22] doping has been widely used. These impurities are useful to compensate an unintentionally formed donor state. Inductively-coupled-plasma reactive ion etching (ICP-RIE) using Cl_2-based gas mixture is widely used for mesa isolation. Several researches have been reported regarding alternative isolation methods without etching such thermal oxidation [23] and ion implantation [24]. Photoresist residue is removed by sulfuric peroxide mixture (SPM) solution after etching process for mesa isolation.

Ti/Al-based multiple metal stacks are typically used for ohmic contact of source and drain [25, 26]. The mechanism of Ti/Al-based ohmic contact on n-GaN is as flow; after annealing process at the higher temperature than 800 ^{o}C, the reaction between Ti and nitrogen (N) in the AlGaN/GaN heterostructure forms TiN layer and nitrogen vacancies (V_N). The V_N acts as shallow donor state in GaN so that the Schottky barrier between GaN and ohmic metal is thinned after annealing. The pattern of ohmic contact is defined by the lift-off process. The recessed structure in the ohmic contact was also proposed to decrease the ohmic contact resistance [27]. Additional metals are commonly formed on the Ti/Al stacks to prevent Ti/Al from oxidation and preserve shape of the source/drain electrodes after high-temperature annealing. Thermal barrier layers such as Ni and Mo are widely formed on Ti/Al sequentially. Au has been considered as good top metal layer of the ohmic contact because of its very low resistance and thermal stability.

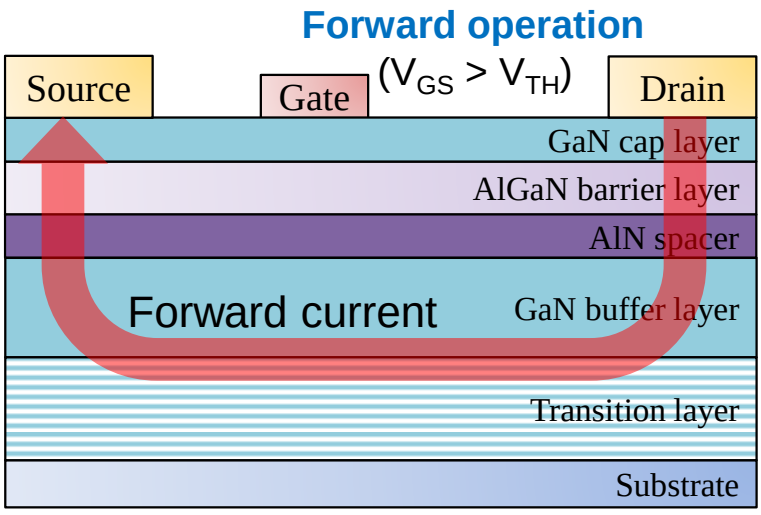
Gate insulator can be formed by various materials and deposition methods such as chemical vapor deposition (CVD), atomic layer deposition (ALD), and sputtering [28, 29, 11]. The dielectric properties such as dielectric constant and breakdown field of gate insulator should be considered to obtain desirable operation range and leakage current in the AlGaN/GaN MOS-HEMTs. Also, the deposition conditions should be optimized to obtain high-quality

interface characteristics between GaN and gate insulator. In this dissertation, RF-sputtering was used for gate insulator. Details of the AlGaN/GaN MOS-HEMTs are taken up in the next chapter.

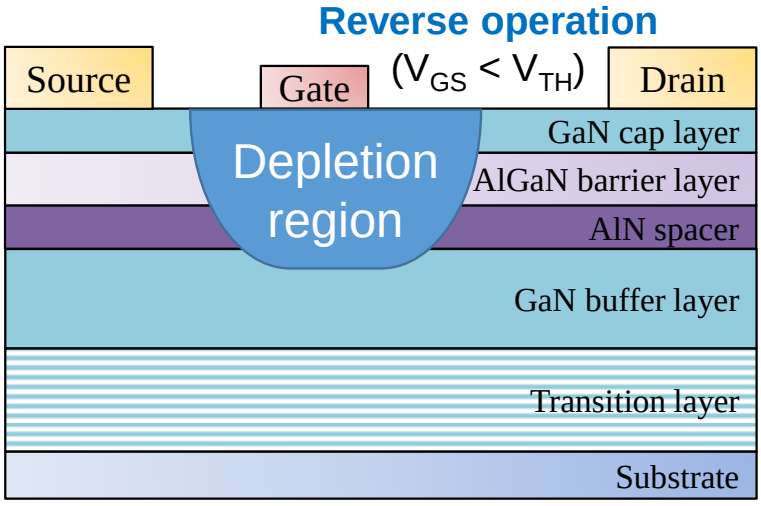
The Schottky-gate controls the AlGaN/GaN HEMTs by applying the voltage. The Schottky contact is fabricated by the sequence of native oxide etch, e-gun evaporation, and lift-off. The Schottky metal determines the Schottky barrier height (SBH) that equals the difference between metal work function and electron affinity of GaN (χ= 4.1 eV) as well as V_{TH}. The work function of Schottky contact on GaN is shown in Table 2-1 [30]. The high SBH is required in order to decrease the tunneling leakage current and increase breakdown voltage. The platinum (Pt) has the highest work function so that Pt-based Schottky contact is widely used for the AlGaN/GaN HEMTs. Ni has rather high work function as well as the good adhesion to the nitride and oxide materials.

Finally, etching process for source/drain opening is performed by conductive-coupled-plasma RIE (CCP-RIE) or ICP-RIE. Appropriate etchant should be used with considering gate insulator material. Thick Au layer on each electrode can be used for etching stopper during pad opening.

Post-gate annealing [30, 31], passivation [32, 33], and edge termination structure [34] can be optionally employed to improve reverse blocking characteristics after the standard fabrication process I described in above.



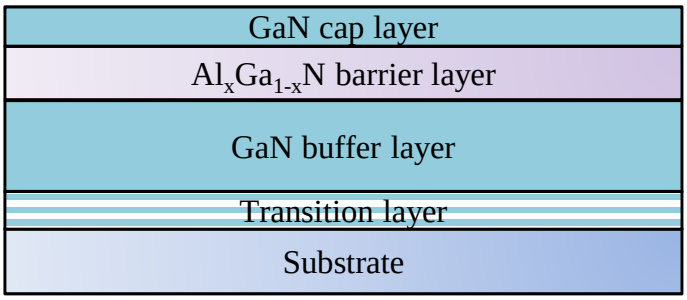
(a)



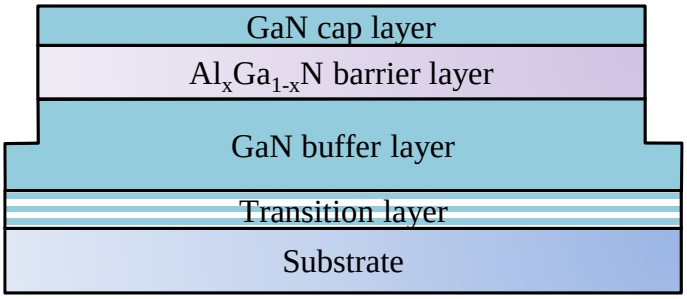
(b)

Figure 2-1: (a) Forward (b) reverse operation of AlGaN/GaN HEMTs.

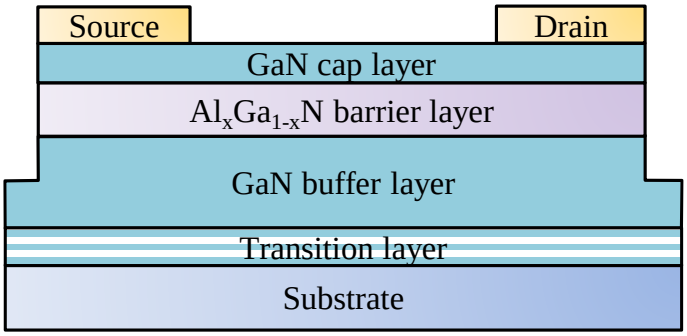
(a)


GaN cap layer
$Al_xGa_{1-x}N$ barrier layer
GaN buffer layer
Transition layer
Substrate

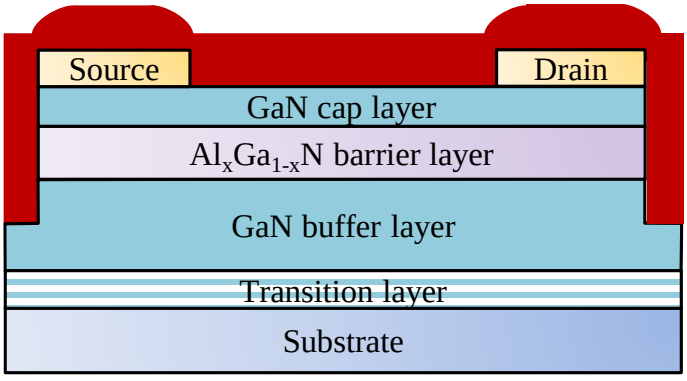
(b)


GaN cap layer
$Al_xGa_{1-x}N$ barrier layer
GaN buffer layer
Transition layer
Substrate

(c)


Source
Drain
GaN cap layer
$Al_xGa_{1-x}N$ barrier layer
GaN buffer layer
Transition layer
Substrate

(d)


Source
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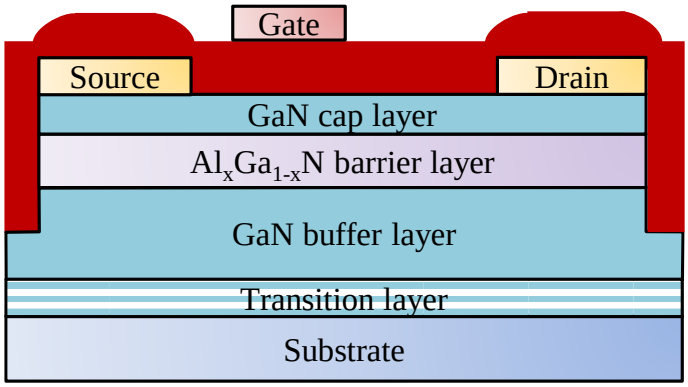
GaN cap layer
$Al_xGa_{1-x}N$ barrier layer
GaN buffer layer
Transition layer
Substrate

(e)



(f)

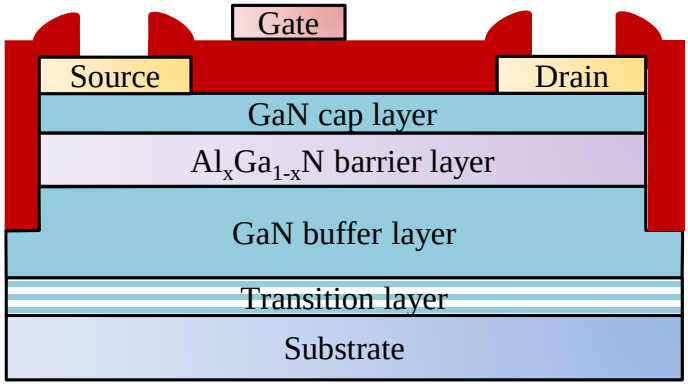


Figure 2-2: Fabrication processes of AlGaN/GaN MOS-HEMTs (a) starting material (b) mesa isolation (c) source/drain formation (d) gate insulator formation (e) gate formation (f) source/drain pads opening.

Table 2-1: Metal work function of Schottky contact on GaN [30].

	Work function (eV)
Pt	5.65
Ni	5.15
Pd	5.12
Au	5.10
Ir	5.46
Mo	4.60

2.2 Key Issues to Limit Electrical Properties

Although the AlGaN/GaN HEMTs have great material properties and they have been studied for a long time, the surface-states related problems in GaN epitaxial layer have still remained as critical issues for high breakdown voltage. Surface states cause current collapse [35], virtual gate effect [35], surface leakage current [36], premature breakdown [36], and radio-frequency (RF) dispersion [36, 37].

As I stated in chapter 1, lattice and thermal mismatches between GaN and substrate are dominant source for the surface states. Figure 2-3 shows cross-sectional transmission electron microscopy (TEM) image of GaN epitaxial layer [38]. As shown in this image, the dislocation, which is originated from substrate/GaN interface, can reach the surface. These surface states typically have shallow energy level within forbidden band. Shallow states offer free electrons which can contribute conductivity of the AlGaN/GaN HEMTs so that considerable leakage current occurs. The AlGaN/GaN HEMTs require plasma-based process for deposition of certain materials and etching as well as high-temperature process. These processes bring about degradation of GaN-surface morphology and deterioration of crystallinity. It is well known that GaN is irrecoverable material by annealing methods due to its decomposition problems. Atomic-forced measurement (AFM) images of GaN after Ar plasma treatment and/or thermal annealing are shown in Fig. 2-4 [10]. These AFM images indicate that GaN is sensitive to process conditions such as etching power and annealing temperature. The root-mean-square (RMS) is rather increased after thermal and/or plasma treatment.

There is one other factor that is important for origin of the surface states. The 2DEG channel results from the spontaneous and piezoelectric

polarization [39, 13]. The electrons are able to transfer from occupied surface states to empty conduction-band states at the AlGaN/GaN interface, creating 2DEG charge and leaving behind positive surface states [39]. The surface donor states have been reported as an actual origin of 2DEG charge. The surface donor states are located at 1.42 [39] or 1.65 eV [13] below the conduction-band edge of the $Al_{0.27}Ga_{0.73}N$ and $Al_{0.34}Ga_{0.66}N$ alloy, respectively.

The SBH lowering effect by surface states has been reported [40]. The surface states cause serious problem at gate/GaN interface increasing surface leakage current. The interface traps induce leakage current path by lowering SBH locally. The schematic band diagram of GaN/metal interface with Schottky contact is shown in Fig. 2-5. The AlGaN/GaN HEMTs have various surface leakage current paths including active-region current and isolation current as shown in Fig. 2-6. During off-states, negative gate bias may block channel leakage current through depletion region well so that suppression of surface leakage current would be more important to obtain high breakdown voltage.

The current paths during on-state are explained by Fig. 2-7. The AlGaN/GaN HEMTs have two kinds of inherent Schottky barrier diodes (SBDs) at gate-source and gate-drain regions. When $V_{GS}<V_F$ (knee voltage of gate-source or gate-drain SBD), the current flow from drain to source across 2DEG channel without any current dissipation into gate. When $V_{GS}>V_F$, however, considerably high gate leakage current occurs because of forward operation in the inherent SBDs. In case of the typical normally-on AlGaN/GaN HEMTs, the V_{GS} sweeping range is limited due to this gate leakage component. Thus, gate leakage current by SBDs operation should be suppressed to obtain high-current devices.

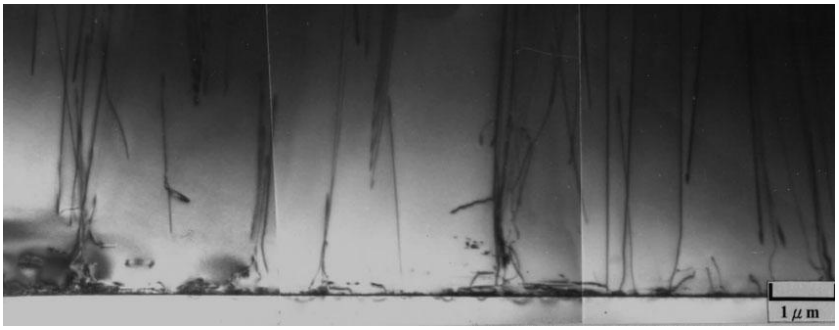


Figure 2-3: Cross-sectional TEM image of GaN epitaxial layer on sapphire [38].

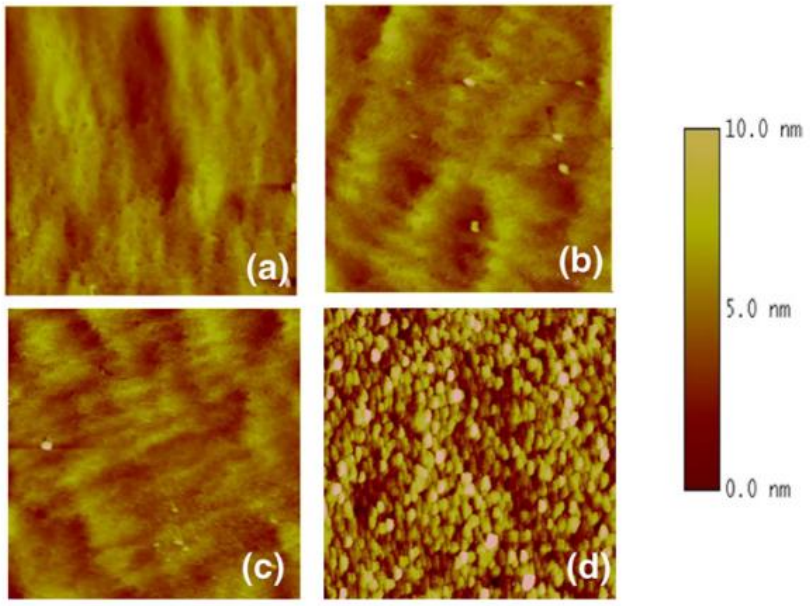


Figure 2-4: AFM images after different treatment (a) Control, (b) Ar plasma treatment, (c) Ar plasma + annealing (800 ^{o}C), and (d) Ar plasma + annealing(1000 ^{o}C) [10].

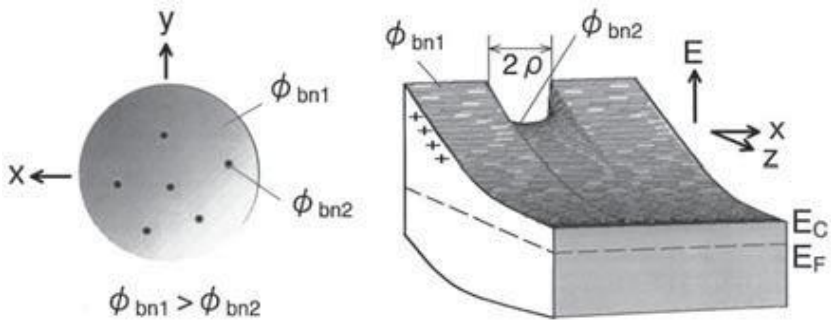


Figure 2-5: Schottky barrier height lowering by surface states [40].

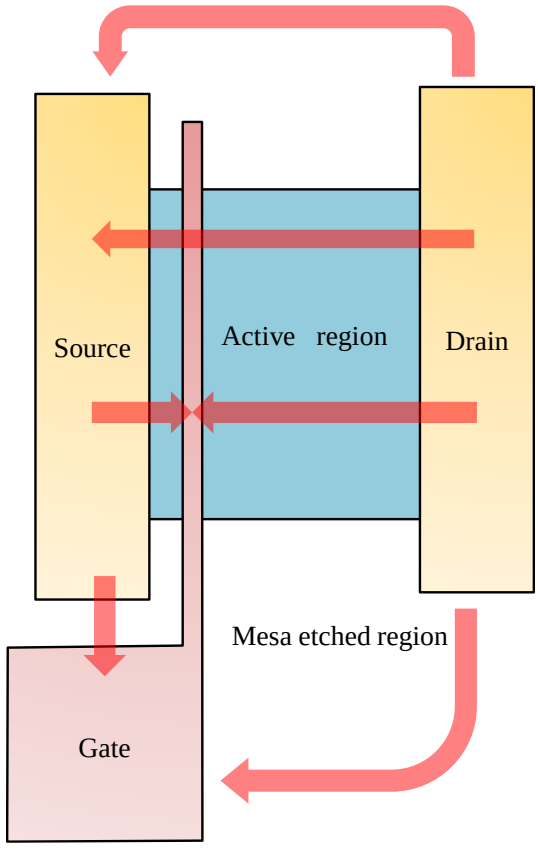
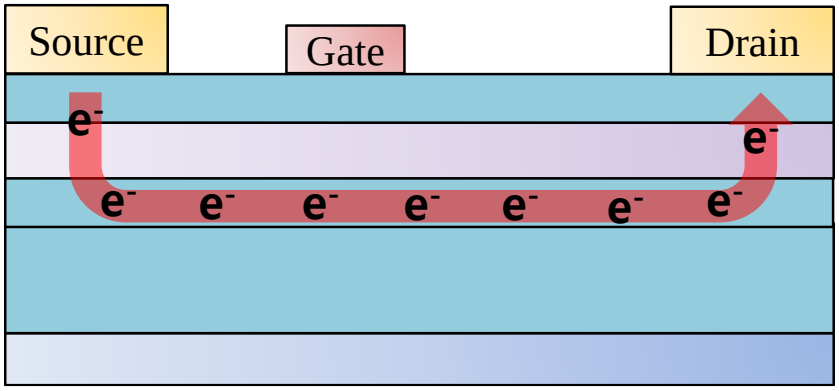
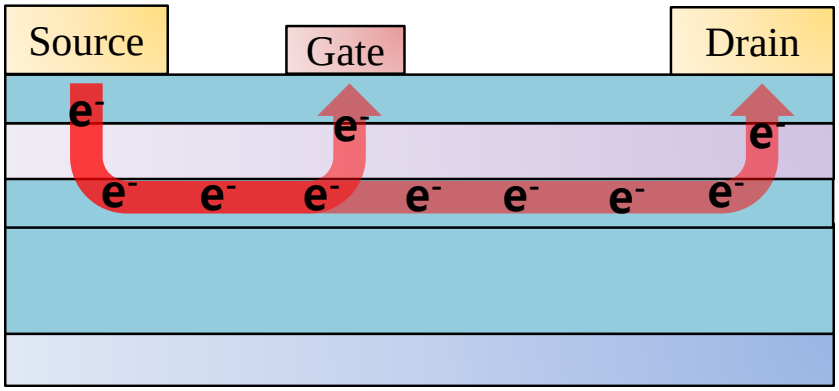


Figure 2-6: Surface leakage current paths in AlGaN/GaN HEMTs.



(a)



(b)

Figure 2-7: Electrons flow in AlGaN/GaN HEMTs at (a) $V_{GS}<V_F$ (b) $V_{GS}>V_F$.

2.3 Recent Technologies for High-Performance AlGaN/GaN Devices

2.3.1 Surface Passivation

Surface passivation has been widely used to suppress electron trapping from gate into surface states and increase breakdown voltage in the AlGaN/GaN HEMT [32, 33]. Also, passivation layer protects the devices from undesirable circumstance by humidity, electrostatic discharge, and physical damage. Although mechanism of surface passivation has been an object of study for a long time, there is a little controversy as to explain that. However, many groups have reported that blocking characteristics of the passivated AlGaN/GaN HEMTs were improved.

Y. Ohno, et al., described the improvement mechanism of breakdown voltage by surface passivation [41] as shown in Fig. 2-8. They explained virtual-gate effect as the mechanism by comparing two devices including the unpassivated HEMT and the passivated one. In case of the unpassivated HEMT, when high-drain voltage is applied, electron injection into the surface states occurs at the drain-sided gate edge so that effective gate would be lengthen. Then, the shorten gate-drain distance leads premature breakdown. This needs some assumption that reduction of potential across virtual gate is ignorable. However, the passivated AlGaN/GaN HEMT has no significant virtual-gate effects. It seems reasonable to conclude that surface passivation suppresses virtual-gate effects and increases breakdown voltage in the AlGaN/GaN HEMTs. Figure 2-9 and Fig. 2-10 show the increased breakdown voltage after

SiN_X passivation [42, 43]. These results match the schematic charge distribution in Fig. 2-8.

It has been reported that SiO_2 passivation using inductively-coupled-plasma chemical-vapor-deposition (ICP-CVD) improves the blocking characteristics of the AlGaN/GaN HEMTs and suppresses surface leakage current as shown in Fig. 2-11 [44]. Due to the effectively suppressed leakage current, they obtained high breakdown voltage exceeding 900 V without any edge termination structures. Besides passivation materials I mentioned, various materials such as benzocyclobutene (BCB) [45], Sc_2O_3, MgO [46], and polyimide [47] have been studied as passivation layer of the AlGaN/GaN HEMTs.

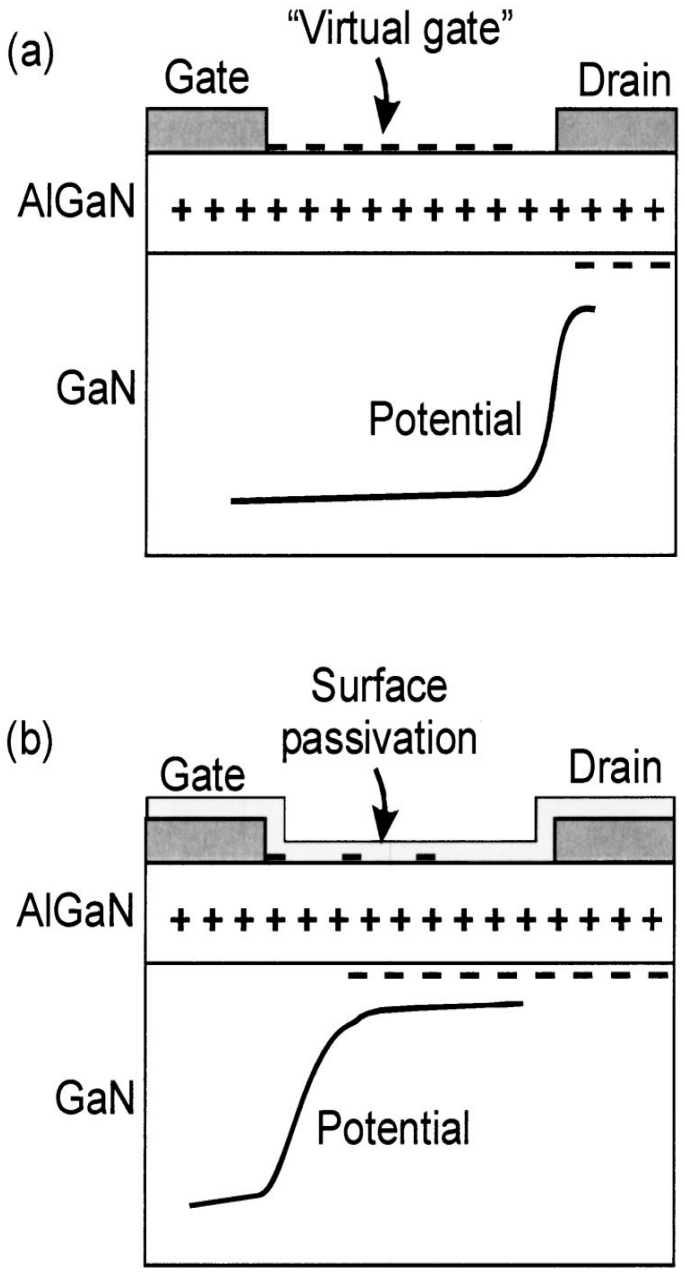


Figure 2-8: Schematics of charge distribution and potential profile between gate and drain (a) without and (b) with surface passivation [41].

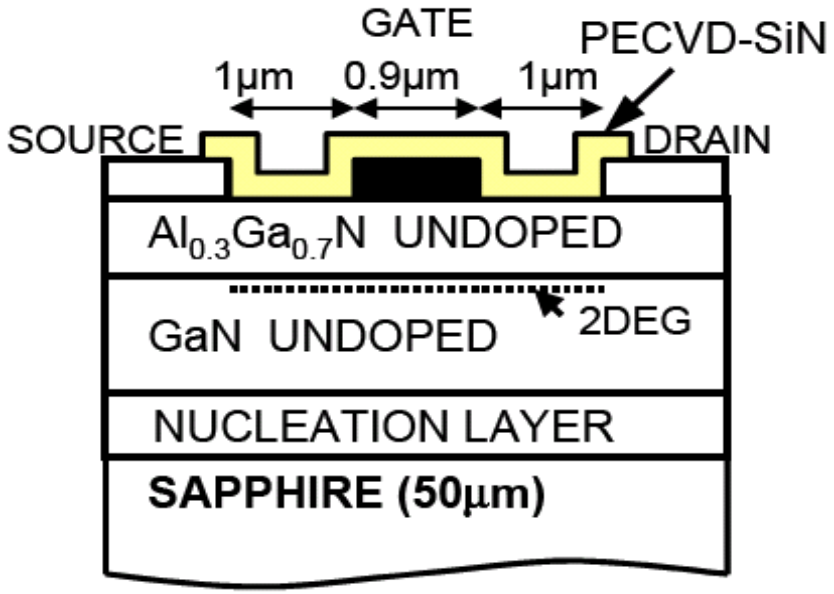


Figure 2-9: Schematic of SiN_X passivated AlGaN/GaN HEMT [42].

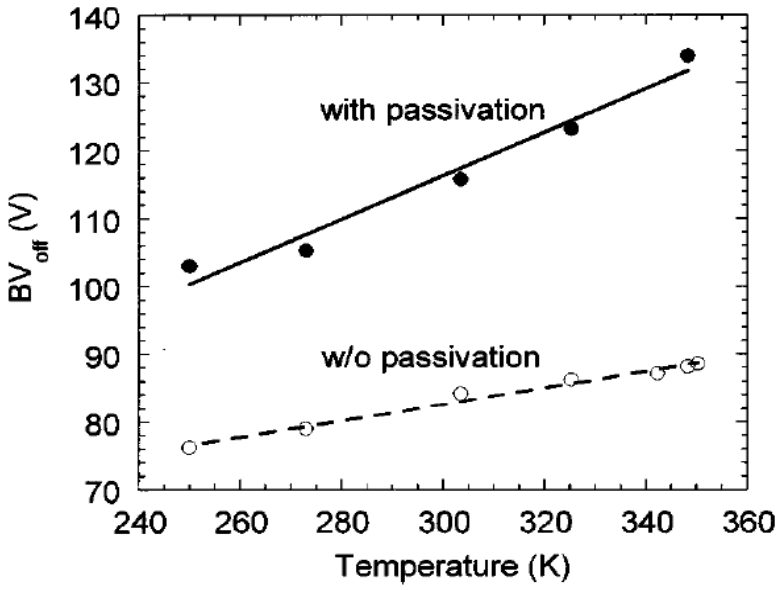
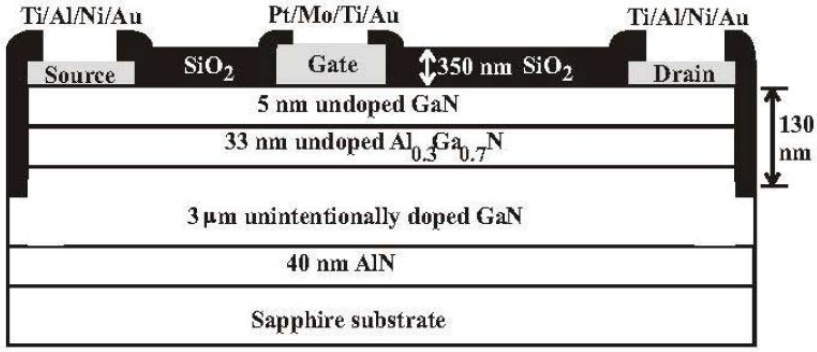
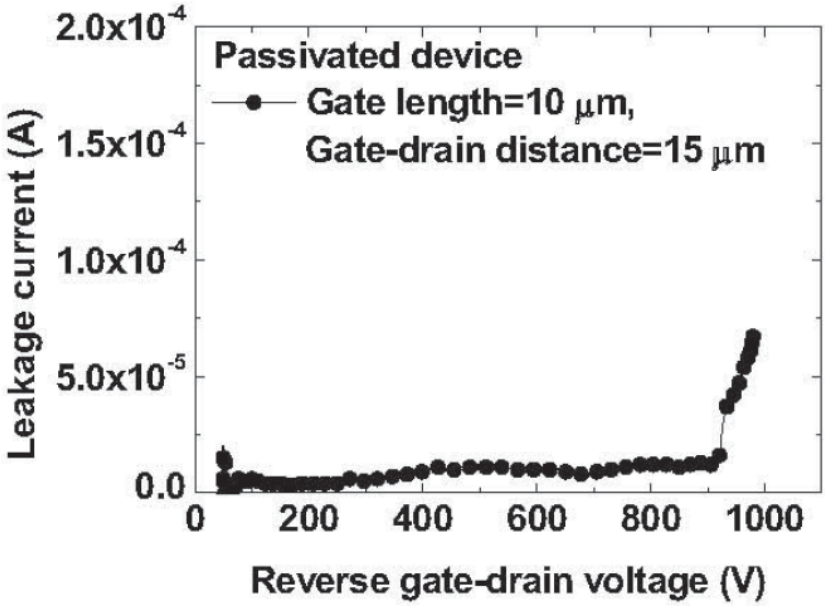


Figure 2-10: Increase of breakdown voltage after passivation [43].



(a)



(b)

Figure 2-11: AlGaN/GaN HEMT using SiO_2 passivation (a) Schematic (b) breakdown voltage characteristics [44].

2.3.2 Edge Termination Structure

The electric field concentration at the drain-sided gate edge is dominant reason for breakdown, electron trapping, and surface leakage current [48]. Therefore, various edge termination methods such as a floating metal and a field plate have been studied to divide the electric field concentration to additional point and reduce these maximum peak values. Figure 2-12 shows schematic of electric field distribution in the AlGaN/GaN HEMTs when gate field plate is used [49]. Gate field plate is typically formed on passivation layer between gate and drain by being connected to main gate. The thickness of passivation layer and field-plate length are important factors to decide electric field distribution between gate and drain. Electric field is divided into two regions including gate edge and field-plate edge. When two electric field peaks have identical value by controlling the thickness of passivation layer and gate field plate length, the AlGaN/GaN HEMTs have the highest breakdown voltage value.

It has reported that slant gate field plate is more useful to reduce maximum electric field peak [34]. Schematic structure of the AlGaN/GaN HEMT using slant gate field plate and the breakdown voltage characteristics are shown in Fig. 2-13. This structure enables gradual depletion region and planar electric field distribution between gate and drain so that they reported very high breakdown voltage over 1800 V by using slant gate field plate. In addition, similar method to obtain gradual depletion using multiple gate field plate was also reported as shown in Fig. 2-14 [34].

There is trade-off relationship between on-current and breakdown voltage because of the limited gate-drain distance. Even field plate structure are perfectly optimized, the shorter distance between gate and drain than

typically used drift region in vertical Si-devices has difficult in high-voltage operation. The AlGaN/GaN HEMT-on-SiC using drain field plate connected to back-side electrodes was reported to solve natural demerit of lateral devices by extending depletion region in semi-vertical direction as shown in Fig. 2-15 [50].

Recently, AlGaN/GaN HEMT using polarization junction to make drift region fully depleted was reported as shown in Fig. 2-16 [51]. Additional bias is applied to base electrode, which is connected to source, to extend the depletion region between gate and drain. The two dimensional hole gas (2DHG) controlled by base bias was used for depletion of 2DEG. It is well known that fully depleted region has excellent resistive characteristics so that it is suitable for sustaining high-drain voltage. In this research, they preciously controlled charge balance at the region between gate and drain by using polarization junction technology. The breakdown was increased by this technology from 130 to 830 V.

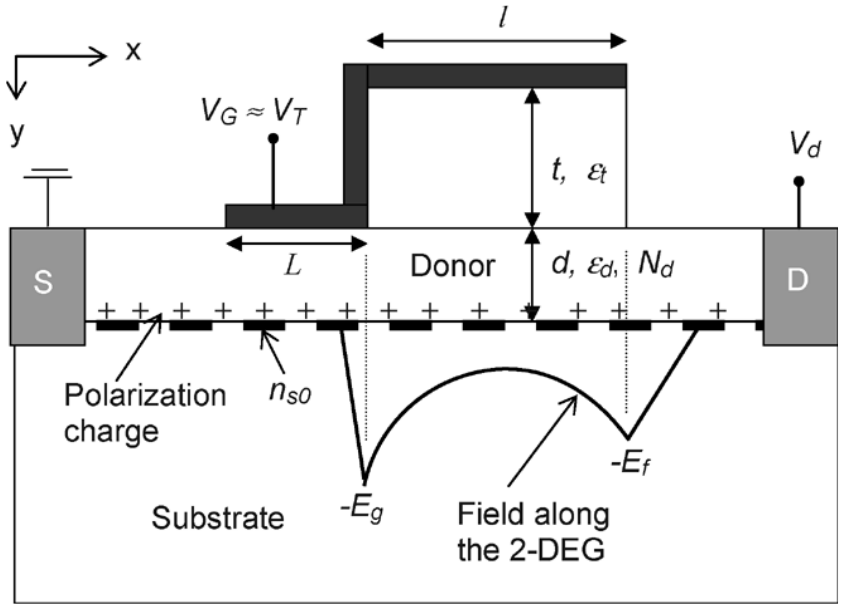
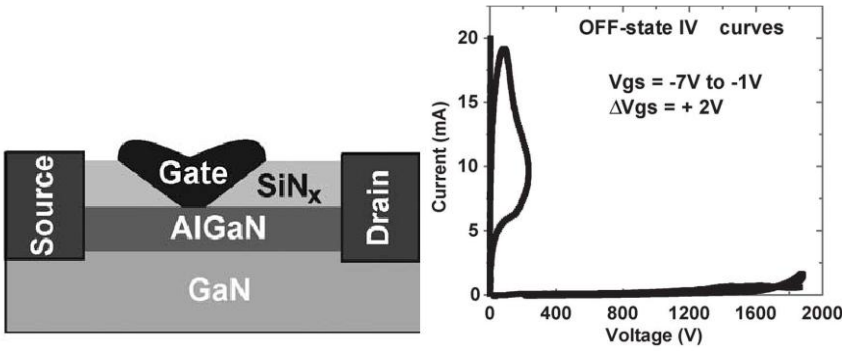
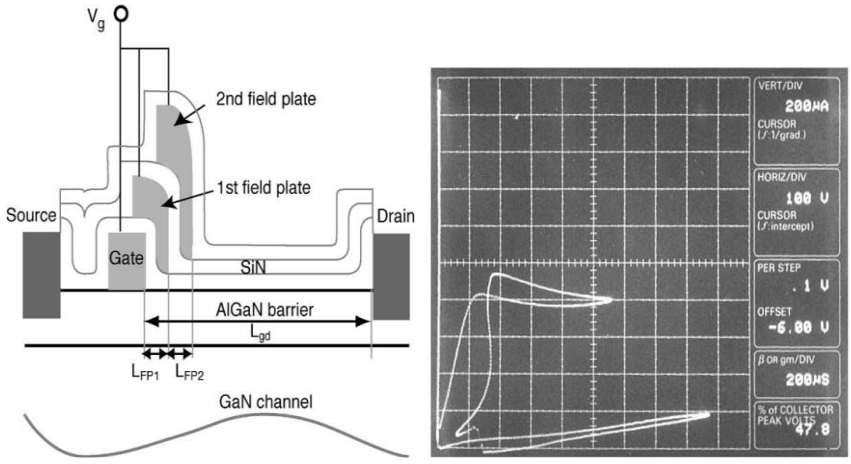


Figure 2-12: Schematic two-peak field distribution along the 2DEG in AlGaN/GaN HEMTs with gate filed plate [49].



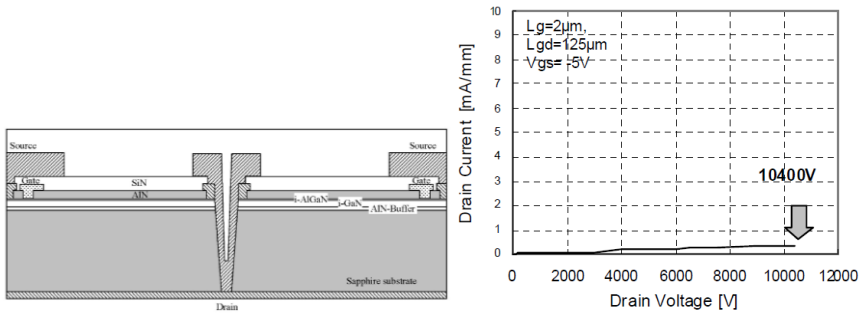
(a) (b)

Figure 2-13: AlGaN/GaN HEMT using slant field plate (a) Schematic (b) breakdown voltage characteristics [52].



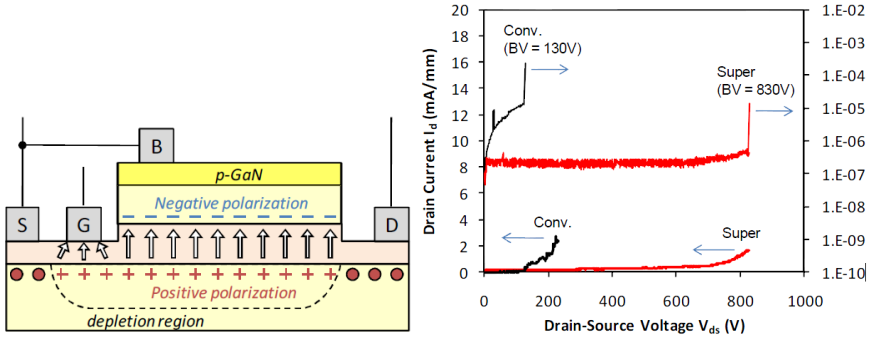
(a) (b)

Figure 2-14: AlGaN/GaN HEMT using multiple gate field plates (a) Schematic (b) breakdown voltage characteristics [34].



(a) (b)

Figure 2-15: AlGaN/GaN HEMT using poly-AlN passivation and drain field plate connected to back-side electrode (a) schematic (b) breakdown voltage characteristics [50].



(a) (b)

Figure 2-16: AlGaN/GaN HEMT using polarization junction (a) Schematic (b) breakdown voltage characteristics [51].

2.3.3 Buffer Growth Technologies

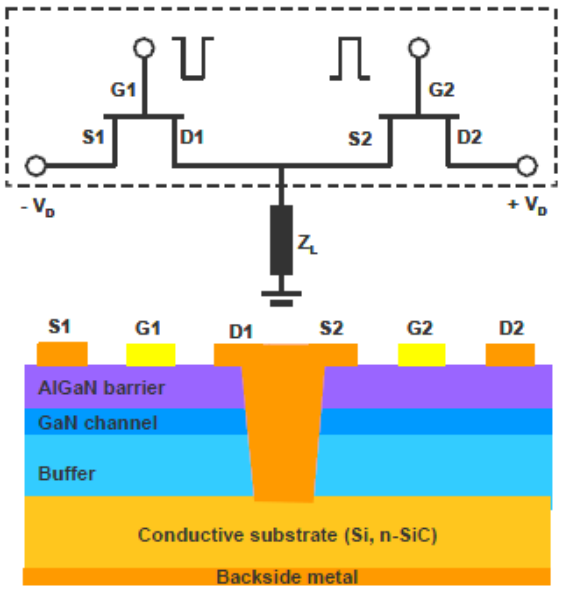
In the AlGaN/GaN HEMTs, GaN buffer layer has various roles such as contribution of highly conductive channel which is called 2DEG and sustention of breakdown voltage. In respect of reverse blocking of the AlGaN/GaN HEMTs, the resistive characteristics of GaN buffer layer are very important because this should sustain high drain voltage. Thus, leakage current trough buffer layer should be suppressed. Among the reported methods to improve resistivity of GaN buffer layer, carbon (c) doping has been aware of the most effective method by compensating shallow traps including nitrogen vacancies (V_N) in GaN buffer layer.

There is one other thing that is important for the AlGaN/GaN-on-Si substrate. It is well known that Si substrate is very promising for the AlGaN/GaN power devices due to its low cost and large available wafer size. However, large lattice mismatch between GaN and Si limits the thickness of GaN buffer layer. When high-drain voltage is applied, the depletion region is extended from gate to drain. At same time, a part of depletion region is extended in vertical direction. Sapphire and SiC substrates have good semi-insulating characteristics due to their wide bandgap properties so that there are no serious problems in GaN/substrate interface when depletion region reaches substrate at high-drain voltage situation. When Si substrate is used for GaN, however, depletion region reaches substrate and conduction through narrow bandgap-Si substrate can occur at high-drain voltage. Thus, sufficient distance between gate and Si-substrate is required. There is no doubt about the importance of thick GaN buffer growth technologies.

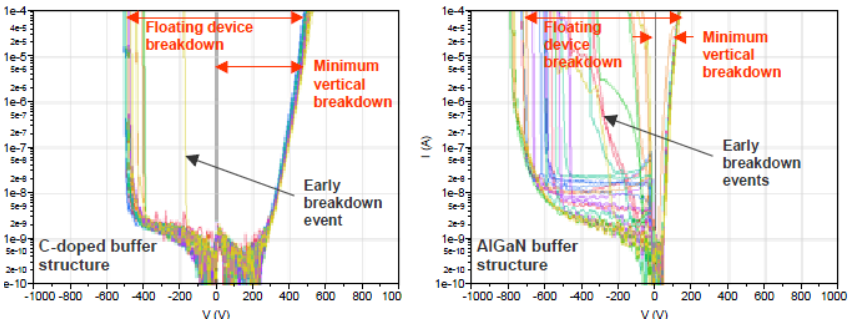
A study on vertical breakdown characteristics through Si substrate in the AlGaN/GaN HEMTs-on-Si was reported as shown in Fig. 2-17 [53]. It shows

schematic of measurement pattern for measuring vertical breakdown voltage. C-doped GaN and AlGaN buffer layers were used for comparison purpose. C-doped GaN buffer layer shows almost symmetry current-voltage characteristics between forward and reverse region. Forward and reverse breakdown voltages are around 400 V as shown in the AlGaN/GaN HEMT-on-Si using C-doped GaN buffer of Fig. 2-17 (b). When AlGaN buffer layer is used for the AlGaN/GaN HEMT-on-Si, however, the test pattern shows rectifying characteristics like diodes due to wider bandgap of AlGaN than upper GaN layer. The breakdown voltage of 800 V was obtained by AlGaN buffer layer because AlGaN buffer layer suppresses extension of depletion region in vertical direction during reverse blocking operation.

C-doping in GaN buffer layer is useful to improve resistance and blocking characteristics in vertical and lateral direction. Figure 2-18 (a) shows breakdown voltage improvement according to C-doping concentration [54]. Lateral breakdown voltage was increased as increasing C-doping concentration. Also, thick GaN buffer makes the distance between channel and substrate longer so that it prevents vertical conduction through substrate from the extension of depletion region in vertical direction. As shown in Fig. 2-18 (b), the breakdown voltage is increased when thick GaN buffer layer is used [54]. Also, high-voltage AlGaN/GaN HEMTs using p-GaN gate and AlGaN back barrier was reported as shown in Fig. 2-19. AlGaN back barrier suppresses electron overflow from channel to buffer layer so that they demonstrated high breakdown voltage over 900 V [55].

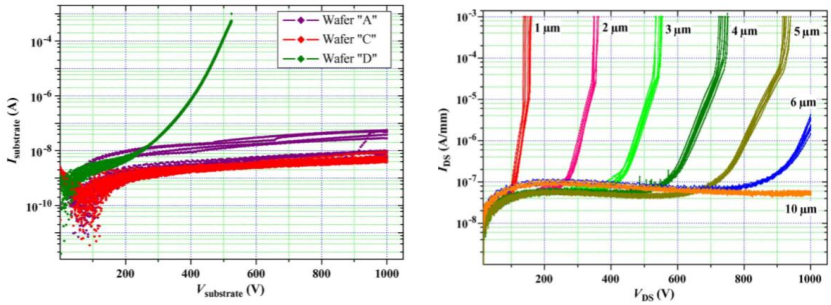


(a)



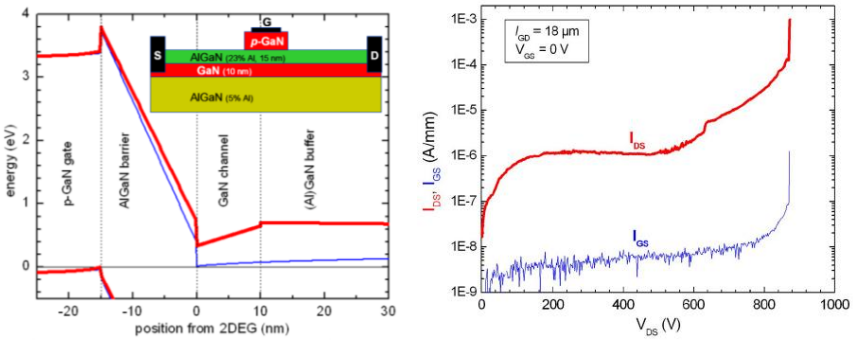
(b)

Figure 2-17: Test pattern for measurement of breakdown voltage through Si substrate in AlGaN/GaN HEMT-on-Si (a) Schematics (b) breakdown voltages of C-doped buffer and AlGaN buffer samples [53].



(a) (b)

Figure 2-18: Breakdown voltage variation according to (a) carbon concentration and (b) GaN buffer thickness [54].



(a) (b)

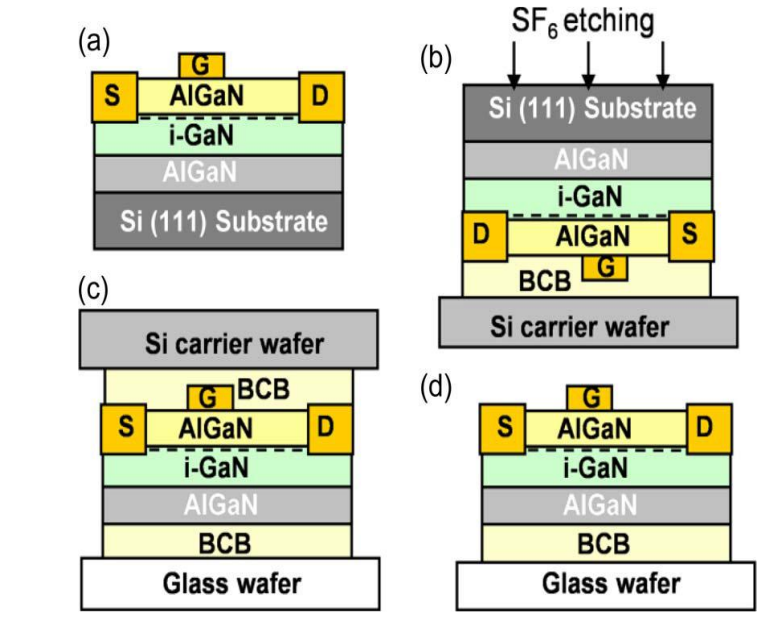
Figure 2-19: AlGaN/GaN HEMT using AlGaN back barrier (a) band diagram and schematic (b) breakdown voltage characteristics [55].

2.3.4 Substrate Transfer Technologies

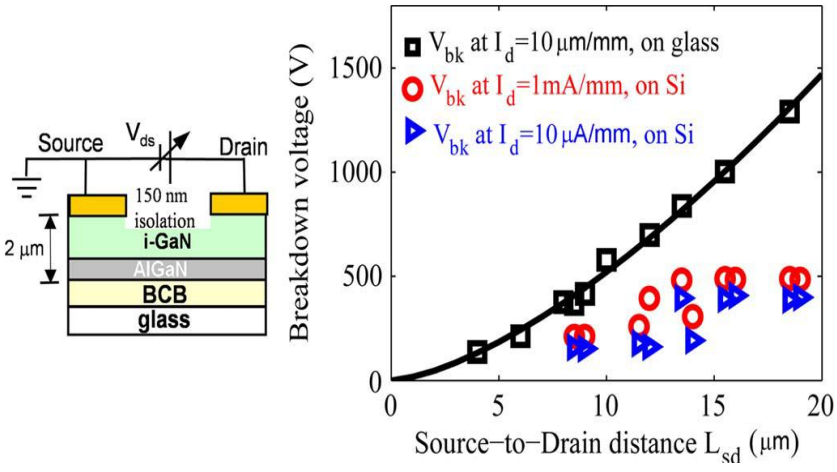
In the AlGaN/GaN HEMTs-on-Si, Si substrate causes a major drawback to obtain high breakdown voltage as described in above section. Thick GaN and AlGaN buffer layers have proven their worth to suppress vertical conduction through Si substrate. In this section, I introduce new methods to suppress conduction through substrate by removing Si substrate after fabrication process for the AlGaN/GaN HEMTs.

Bin Lu, et al., reported breakdown voltage improvement of the AlGaN/GaN HEMTs by using Si-substrate transfer technology [56]. The process procedure for substrate transfer and breakdown voltage improvement is shown in Fig. 2-20. The fabricated AlGaN/GaN HEMT was bonded with BCB-on-Si carrier substrate at front side. Then, original Si substrate was removed by SF_6-based etching. Next, alternative BCB-on-glass substrate was bonded with the AlGaN/GaN HEMT at back side. Finally, BCB-on-Si carrier substrate was detached from the AlGaN/GaN HEMT. Breakdown voltage of the AlGaN/GaN HEMT using substrate transfer is proportionally increased to source-drain distance by eliminating thoroughly conducting path through Si substrate.

Another method to suppress conduction through Si substrate at high drain voltage was reported [57]. The schematic and breakdown characteristics are shown in Fig. 2-21. Si substrate was locally eliminated by etching at the region between source and drain where vertical conduction through Si substrate occurs. This locally removing Si substrate may make depletion region extends to the drain-side when higher drain voltage is applied. It is likely that this result about breakdown voltage improvement is similar with the effects of semiconductor-on-insulator (SOI)-based devices.

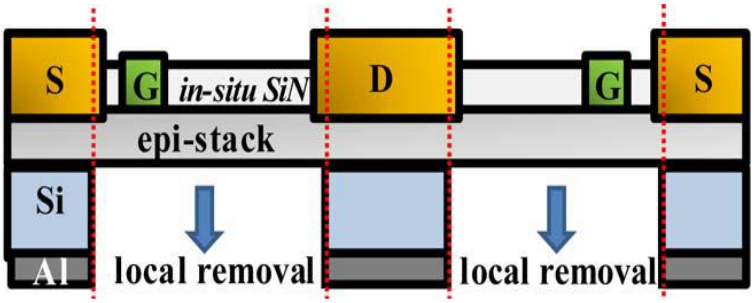


(a)

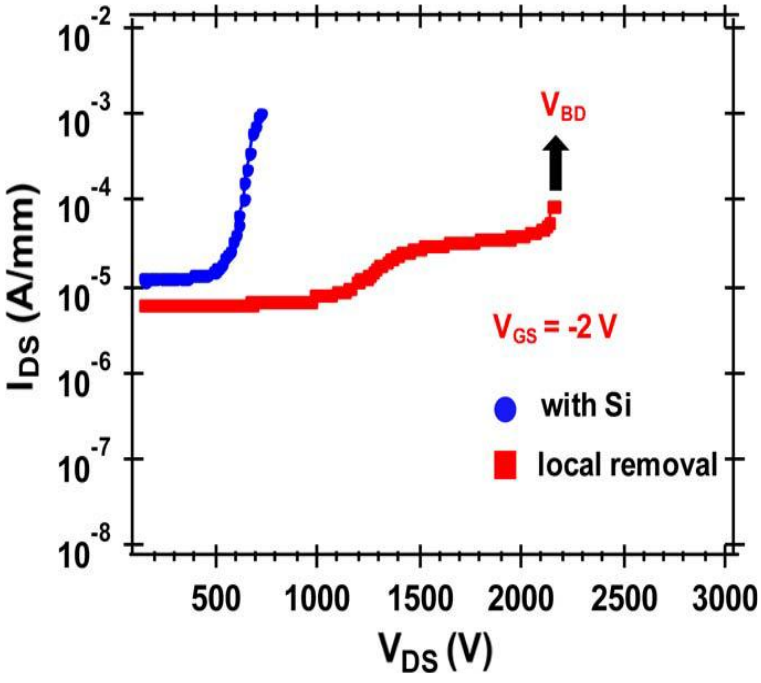


(b)

Figure 2-20: AlGaN/GaN HEMT adopting substrate transfer technique to glass wafer (a) transfer process (b) breakdown voltage characteristics [56].



(a)



(b)

Figure 2-21: AlGaN/GaN double-heterojunction FET (DHFET) using local substrate removal technique (a) Schematic (b) breakdown voltage [57].

Chapter 3

3. AlGaN/GaN MOS-HEMTs Employing HfO_2 Gate Insulator

3.1 Overview

Recently, AlGaN/GaN devices have gained considerable attention for high-power applications due to high critical electric field and high mobility two-dimensional electron gas (2DEG) channel at their hetero-interface [14, 58]. And, fabrication for the AlGaN/GaN devices is rather simple compared with Si-based power devices such as trench-gate metal-oxide-semiconductor field-effect transistors (MOSFETs), superjunction MOSFETs, and insulated-gate bipolar transistors (IGBTs) because the AlGaN/GaN devices don't require any high-cost thermal and ion implantation processes [59]. The fabrication cost of the GaN devices can be much lowered by developing the GaN growth technologies on large diameter-Si substrate.

In addition, good thermal stability of GaN enables lightweight power

system and provides excellent ruggedness under ultra-harsh environment. However, the surface states-related problems such as leakage current and current collapse should be suppressed because these cause the deterioration of breakdown voltage and switching loss as reviewed in section 2.2.

In this chapter, I propose high-quality HfO_2 gate insulator by RF-sputtering for the high-voltage AlGaN/GaN MOS-type high-electron-mobility transistors (HEMTs) for the first time. In the flowing section, the advantages of MOS structure in the AlGaN/GaN HEMTs during on and off states and device operation are explained. And, various methods and materials for gate insulator in the AlGaN/GaN MOS-HEMTs are introduced.

Section 3.3 shows RF-sputtering system used in the experiments of this dissertation. Sputtering guns with 4 target slots were established in the main chamber and sputtering of single target or multi-target was able to be performed for deposition of electrodes or insulator with variation of sputtering conditions such as sputtering power, working pressure, and substrate temperature. This multi-target system also enables in-situ deposition of electrodes/insulator.

Section 3.4 includes studies for characterization of the RF-sputtered HfO_2 gate insulator in material and electrical point of views. The sputtering conditions are optimized to obtain high-resistive HfO_2 insulator. Then, composition and dielectric breakdown characteristic of the HfO_2 sputtered at room temperature are evaluated. Also, post-deposition annealing under N_2, O_2, and H_2O ambient is investigated to improve dielectric breakdown characteristics of HfO_2 insulator.

Section 3.5 shows the electrical properties of the AlGaN/GaN MOS-HEMTs-on-Si using RF-sputtered HfO_2 gate insulator. First, the effects of sputtering power and working pressure on the surface leakage current is

discussed. It was found that high sputtering power affects damage to GaN surface. Secondly, the reverse blocking characteristics such as leakage current and breakdown voltage are evaluated. To verify improvement mechanism of breakdown voltage over 1.5 *k*V, I classify the reason for suppression of leakage current into two factors including surface passivation effects and blocking gate leakage current. And finally, reliability and interface characteristics of the AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator with various measuring conditions are investigated.

3.2 Advantages of AlGaN/GaN MOS-HEMTs

Leakage current of the AlGaN/GaN HEMTs should be suppressed for low stand-by power dissipation, high breakdown voltage, and high current density [60]. Various methods such as surface passivation [41, 43, 44, 61, 46], a field plate [52, 62, 50, 51, 49, 34], and impurity doping in buffer layer [54, 55] have been reported to improve device performance. A great deal of effort has been made on the high-performance AlGaN/GaN HEMTs. What seems to be lacking, however, is effective blocking of gate leakage current [63].

In case of the conventional AlGaN/GaN HEMTs without any gate insulator, the gate-source voltage (V_{GS}) is limited within negative sweeping range. When V_{GS} > knee voltage (V_F) of inherent gate-source or gate-drain Schottky barrier diodes (SBDs), the electron in 2DEG channel can be transferred to Schottky gate and forward current dissipation occurs [64, 65]. The problem increases when normally-off devices are used because of the narrow V_{GS} sweeping range above 0 V. Moreover, when negative drain-source voltage (V_{DS}) is applied, serious reverse conduction can lead to device failure [66]. Due to this reverse conduction problem, the conventional AlGaN/GaN HEMTs are not suitable for connection to opposite-phase device in complementary metal-oxide semiconductor (CMOS) and inverter system.

During off-state, the considerable surface leakage current and traps-assisted Schottky tunneling current occur as I have mentioned in section 2.2. The surface traps should be suppressed because these reduce Schottky barrier height (Φ_{BN}) and breakdown voltage [40]. The current path of the conventional AlGaN/GaN HEMTs during on and off state are shown in Fig. 3-1 (a) and (b). Figure 3-1 (c) indicates, the forward current dissipation by turn-on of the inherent SBDs during on-state can be blocked by gate insulator in the

AlGaN/GaN MOS-HEMTs. Gate insulator allows wide V_{GS} sweeping range up to highly positively value until dielectric breakdown. In the maximum current density point of view, the wide V_{GS} sweeping range is very important. Added to these, MOS structure is essential to realize normally-off AlGaN/GaN transistors. During off-state, the surface leakage current and tunneling leakage current through gate can be suppressed by gate insulator as shown in Fig. 3-1 (d). When the resistivity of GaN buffer layer is sufficiently high, the leakage current of the AlGaN/GaN MOS-HEMTs through GaN buffer layer can be ignored.

In the Si-based power devices, oxidation method is usually used for gate insulator formation [67]. It is well known that the interface traps can be decreased during this oxidation process so that 10^{10} $cm^{-2}{\cdot}eV^{-1}$-level interface trap density (D_{it}) can be easily obtained in the Si-devices [68]. Many research groups have made an effort to achieve high-quality Ga_2O_3 insulator for GaN MOS system as shown in Fig. 3-2 [9, 69, 70]. However, high-temperature oxidation process causes the decomposition of GaN and generates amount of nitrogen vacancies, which act as shallow traps at the GaN surface.

The plasma-enhanced chemical vapor deposition (PECVD) is widely used for gate insulator and passivation layer of the AlGaN/GaN devices [71, 72]. The plasma damage by using PECVD may degrade 2DEG which is only 30 nm below the surface. The 30 nm is the typical thickness of AlGaN barrier layer. It is noted that this plasma damage affects surface leakage current. Thus, low-damage inductively coupled plasma-chemical vapor deposition (ICP-CVD) and electron cyclotron resonance (ECR)-based methods are desirable for the AlGaN/GaN MOS-HEMTs [28, 29].

Figure 3-3 shows the AlGaN/GaN MIS-HEMT using ECR-sputtered SiN_X gate insulator [11]. The forward and reverse leakage current in the gate-source MIS diodes are dramatically decreased by gate insulator.

A very thin layer of SiO_2 or Si_3N_4 is required for the AlGaN/GaN MOS- or MIS-HEMTs to suppress negative shift of threshold voltage (V_{TH}) owing to their low-k characteristics [73, 74]. This thin gate insulator may cause hot carrier induced gate leakage current and narrow sweeping range of V_{GS}. In order to suppress the negative shift of V_{TH} and prevent device failure due to dielectric breakdown during the reverse blocking operation in the AlGaN/GaN MOS-HEMTs, high-k gate insulator materials such as Al_2O_3 [75, 76, 77, 78, 79], HfO_2 [25, 12], and ZrO_2 [80] are desired.

Among the various candidates for gate insulator, HfO_2 is the most suitable gate insulator material for the AlGaN/GaN MOS-HEMTs due to its high-k characteristics. High breakdown field is also useful to suppress negative shift of V_{TH} in the AlGaN/GaN MOS-HEMTs. Figure 3-4 shows high breakdown voltage and low leakage current of the AlGaN/GaN MOS-HEMT using atomic-layer deposition (ALD)-HfO_2 gate insulator. Another important point of HfO_2 insulator is that it has native fixed-charge while most insulator materials such as SiO_2 and Al_2O_3 generally contain positive fixed-charge [81]. This unique property of HfO_2 gate insulator is very helpful to obtain normally-off devices.

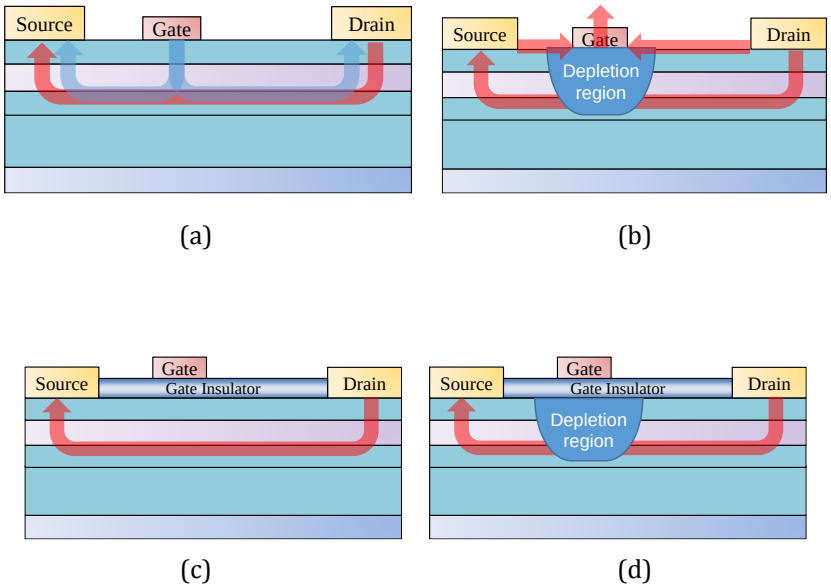


Figure 3-1: Device operation and possible current flow in (a) conventional HEMTs during on-state (b) conventional HEMTs during off-state (c) MOS-HEMTs during on-state (d) MOS-HEMTs during off-state.

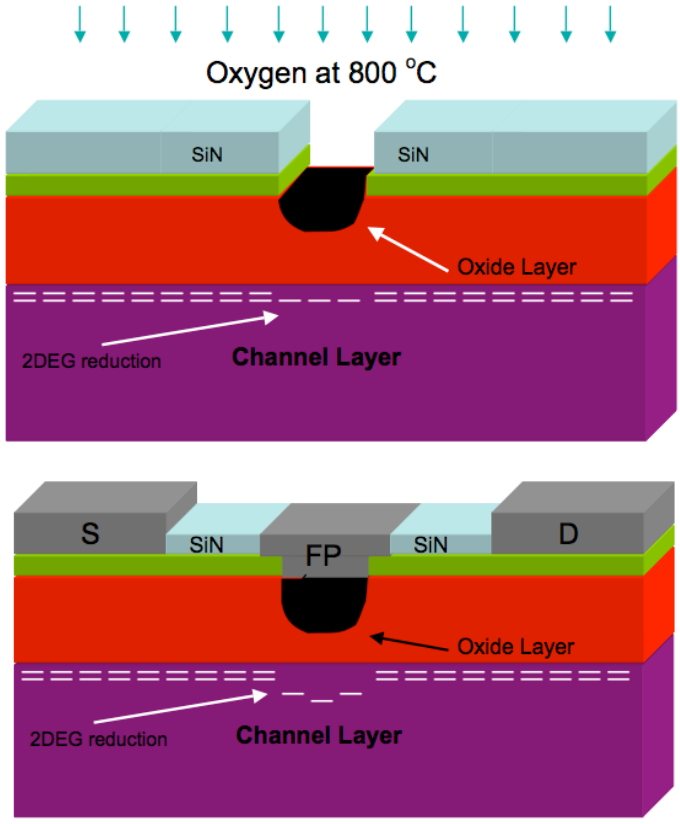
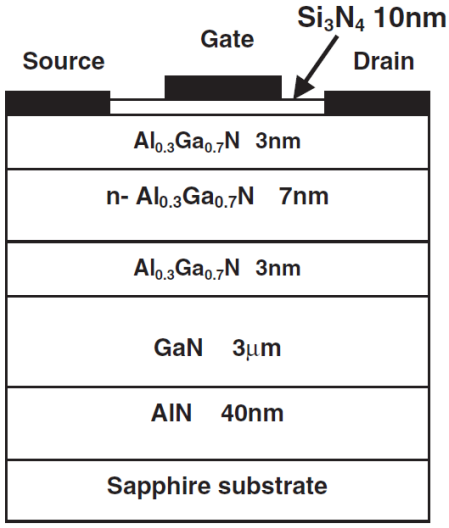
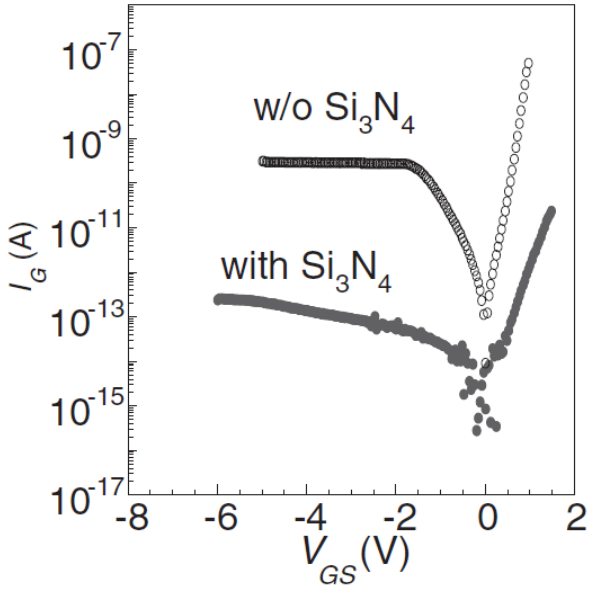


Figure 3-2: AlGaN/GaN MOS-HEMT using thermally grown oxide layer and gate field plate [9].

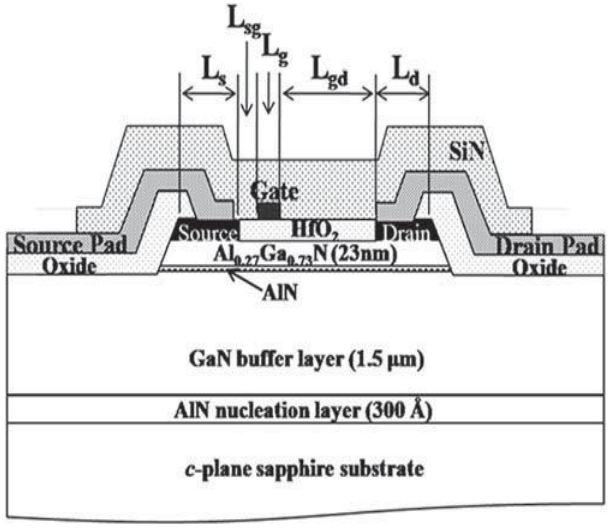


(a)

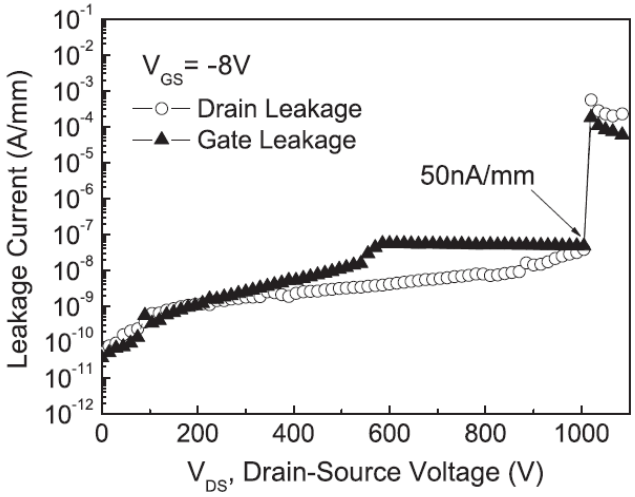


(b)

Figure 3-3: AlGaN/GaN MOS-HEMT using ECR sputtered Si_3N_4 gate insulator (a) device structure (b) gate-source diode characteristics [11].



(a)



(b)

Figure 3-4: AlGaN/GaN MOS-HEMT using ALD-HfO_2 gate insulator (a) device structure (b) breakdown voltage characteristics [12].

3.3 RF-Sputtering for Gate Insulator Formation

Gate insulator in the AlGaN/GaN MOS-HEMTs can be formed by various methods including CVD, ALD, and RF-sputtering as I stated above section. Among the deposition methods, RF-sputtering is very attractive method due to its controllability over deposition parameter [82]. It is well known that RF-sputtering methods exhibit high throughput due to its high deposition rate and availability of large-size process [83]. Also, a low-temperature and a low-cost process for gate insulator formation simplify fabrication process of the AlGaN/GaN MOS-HEMTs [84]. Also, sputtering has an advantage because the deposited films exhibit the same composition as the target material [85]. In addition, in-situ deposition of multiple layers and co-sputtering can be performed by using multi-targets and guns in a single chamber. Other films such as electrodes and semiconductor materials are also able to be deposited by the sputtering.

Figure 3-5 provides the detail description of the magnetron sputtering system used in this dissertation. This equipment consists of main-system controller and experimental chamber including main chamber and loadlock chamber. Two set of DC-power and two set of RF-power guns were embedded in the main chamber. These four set of guns allow for single sputtering, co-sputtering, and sequential sputtering. Various process gases such as Ar, H_2, O_2, and N_2 is supplied by mass flow controllers through gas lines. The DC- and RF-sputtering power up to 400 W is available. And substrate temperature can be controlled from room temperature to 600 ^{o}C by SiC heater. Target-to-the substrate distance is controllable from 117 to 134 mm and it is generally set to 134 mm during sputtering.

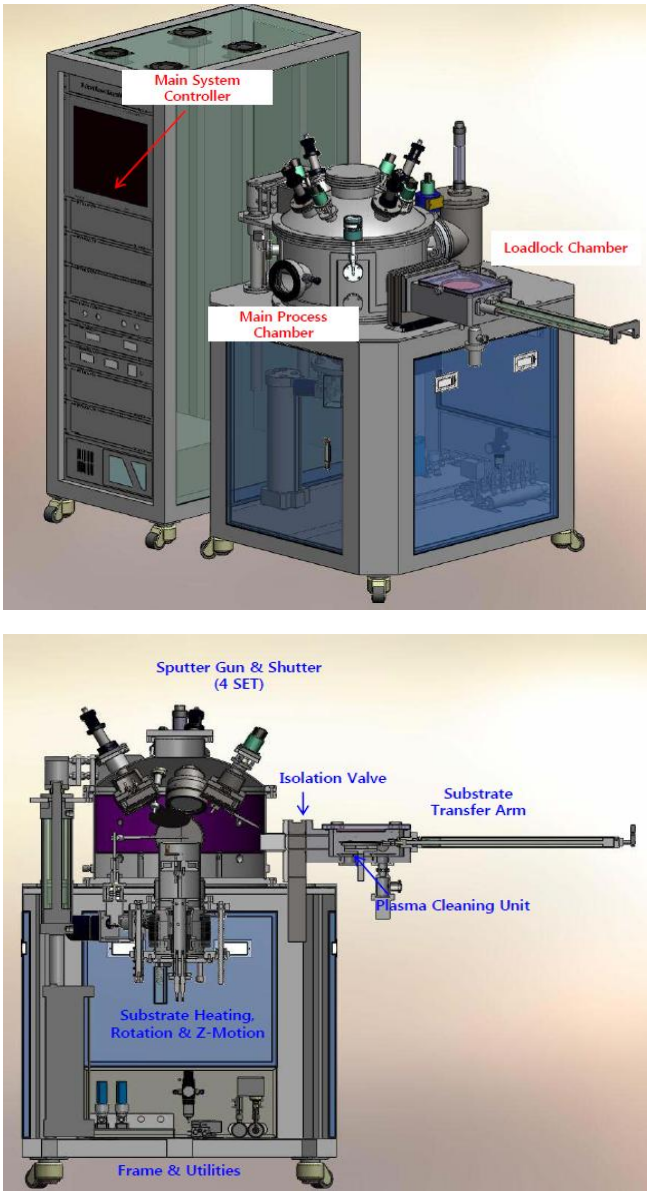


Figure 3-5: Configuration of magnetron sputtering system used for gate insulator and electrode in this dissertation.

3.4 Characterization of HfO_2 Gate Insulator

In this section, I investigate and evaluate the material and electrical properties of HfO_2 insulator sputtered at room temperature. This study would give an insight into understanding HfO_2 gate insulator by RF-sputtering for the AlGaN/GaN MOS-HEMTs. I describe optimization of sputtering conditions to obtain high dielectric breakdown voltage of HfO_2 insulator. In addition, the effects of post-deposition annealing (PDA) to increase sheet resistance and dielectric breakdown voltage are investigated. The mechanism of this effects will be discussed by measuring various material and electrical properties after PDA under N_2, O_2, and H_2O ambient. In this experiments, HfO_2 films was sputtered on p^+ Si and low-resistive p^{++} Si substrate.

3.4.1 Material and Electrical Properties of HfO_2

In order to optimize the HfO_2 sputtering conditions and obtain its accurate sputtering rate. I examined the thickness of HfO_2 insulator sputtered on p^+ Si (10~15 Ω·cm) substrate. HfO_2 insulator was sputtered with sputtering power variation from 50 to 300 W and sputtering time variation from 1200 to 10000 s at room temperature. Working pressure of 3 mTorr and Ar flow of 15 sccm were used for this analysis. Then, the thickness was measured by surface profiler (Alpha step) and atomic forced measurement (AFM) methods. It was found that sputtering rate and thickness of the RF-sputtered HfO_2 insulator exhibits good linearity according to sputtering power and sputtering time as shown in Fig. 3-6. This thickness controllability provides reliable and

repeatable fabrication for the AlGaN/GaN MOS-HEMTs. It is well known that V_{TH} is very sensitive to thickness of gate insulator in the voltage-controlled devices [86].

Figure 3-7 shows cross-sectional and surface scanning electron measurement (SEM) image of the RF-sputtered HfO_2 insulator-on-AlGaN/GaN heterostructure. It includes 3 nm-thick GaN cap/20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier/1 nm-thick AlN spacer/100 nm-thick i-GaN/3.9 μm–thick C-doped GaN buffer by grown metal-organic chemical vapor deposition (MOCVD) method. The 15 nm-thick HfO_2 insulator was obtained on the AlGaN/GaN heterostructure considering V_{GS} sweeping range and dielectric breakdown voltage. Working pressure of 3 mTorr, sputtering power of 50 W, and sputtering time of 20 min were used for HfO_2 formation. As shown in Fig. 3-7 (b), the RF-sputtered HfO_2 insulator shows visible grain-size, of which has diameter ranger from a few nm to a few tens nm. This visible grain is corresponding to spectral peaks in X-ray photoelectron spectroscopy (XPS) results in Fig. 3-8. The Hf 4f has two peaks centered at 16.48 and 18.16 eV. This peaks position has good agreement with the reported results by ICP-sputtering [87] and ALD [88]. And, those of O 1s are centered 529.69 and 531.49 eV. This spectral peaks are similar values reported previously [89]. Also RF-sputtered HfO_2 insulator doesn't have any problem in its composition even it was sputtered at room temperature as shown in Fig. 3-9. The oxygen/hafnium ratio of 1.75 was confirmed by Auger electron spectroscopy (AES) [90].

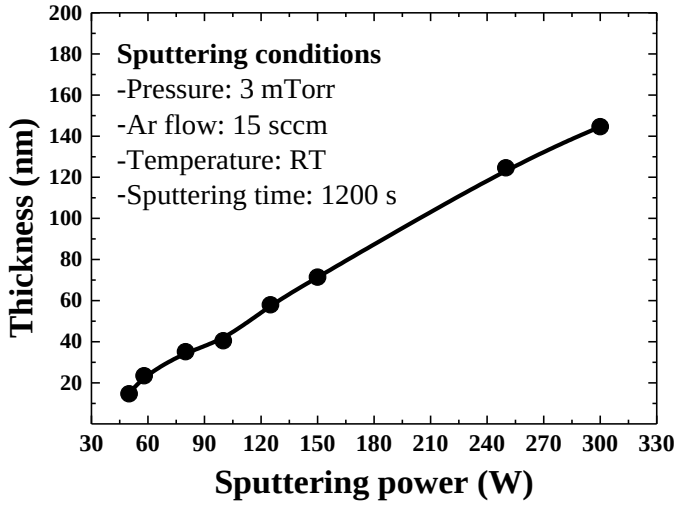
Figure 3-10 shows the X-ray diffraction (XRD) results of HfO_2 insulator sputtered at 3 and 10 mTorr. It was found that low working pressure induces better crystallinity compared to high working pressure. It is known that crystallinity of HfO_2 insulator strongly influence on the resistivity and dielectric breakdown characteristics [87, 91]. The HfO_2 at 3 mTorr showed

weak peaks of the (2 0 0) and (2 2 0) tetragonal phases at around 35° [92]. This indicates that the low-process pressure during the HfO_2 sputtering leads to the weak crystallization of HfO_2. The weakly crystallized properties of HfO_2 under low working pressure induce a low dielectric leakage current and high dielectric breakdown voltage. The most of important point is RF-sputtered HfO_2 insulator was formed at room temperature. Simple formation of high-quality gate insulator without any annealing or substrate heating provides various advantages for flexibility in fabrication procedure and considering thermal budget.

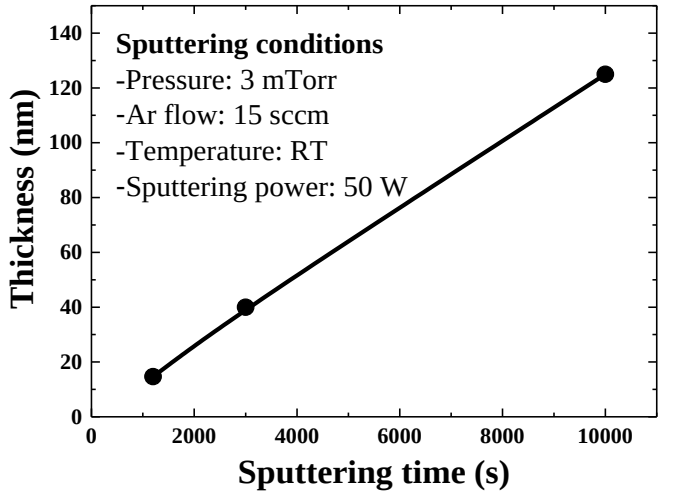
Figure 3-11 shows schematic structure of the test pattern to measure dielectric breakdown field of RF-sputtered HfO_2 insulator. Prior to HfO_2 insulator deposition, low resistance p^{++} Si (0.01 ~ 0.02 Ω·cm) substrate was prepared dipped into 4:1 sulfuric peroxide mixture (SPM) for 10 min and 30:1 buffered oxide etchant (BOE) for 30 s to remove organic-based contamination and native SiO_2 insulator on p^{++} Si substrate. The 18, 58, and 140 nm-thick HfO_2 films were deposited on p^{++} Si substrate by controlling sputtering time. Same sputtering conditions including sputtering power of 50 W, working pressure of 3 mTorr, and Ar flow of 15 sccm as that for above experiment were used. Then, wet etching using 6:1 BOE was performed to open HfO_2 insulator on p^{++} Si substrate. And finally, circular-type Al anode with 100 nm-long diameter was formed by e-gun evaporation and lift-off. The thickness of Al-anode was 100 nm.

The dielectric breakdown voltage was measured with sweeping anode voltage up to 100 V. The resistance of p^{++} Si substrate was ignored and the p^{++} Si substrate was grounded for this measurement. The dielectric breakdown in this pattern shows very small deviation range within device-to-device variation. Also, these values exhibit distinct linearity regarding thickness of HfO_2. The average dielectric breakdown voltages of the 18, 58, and 140 nm-

thick HfO_2 films are 10, 27, and 68 V, respectively. I obtained the normalized breakdown field of 5 MV/cm without any substrate heating and PDA. The high breakdown field of gate insulator would provide high current density and small shift of V_{TH} in the AlGaN/GaN MOS-HEMTs.

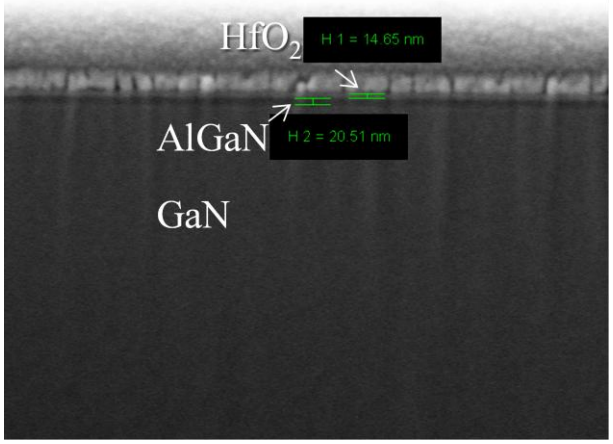


(a)

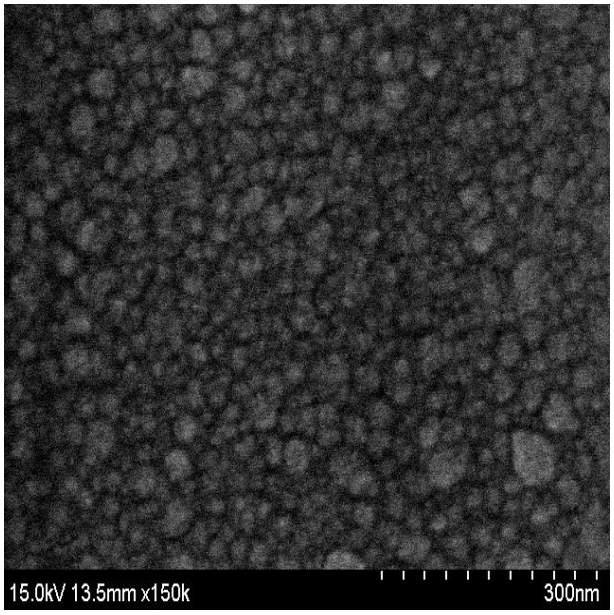


(b)

Figure 3-6: Thickness variation of RF-sputtered HfO_2 insulator according to (a) sputtering power (b) sputtering time.

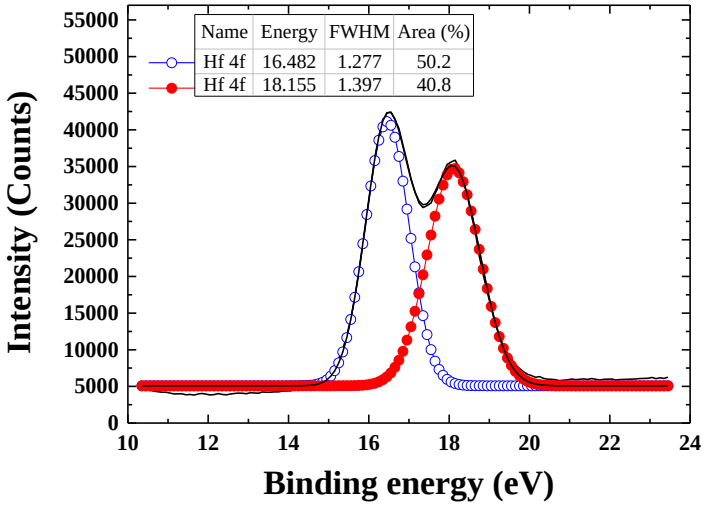


(a)

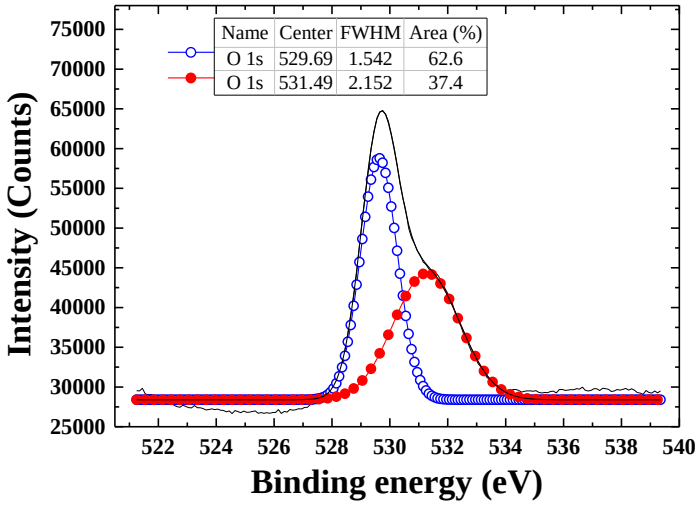


(b)

Figure 3-7: SEM images of RF-sputtered HfO_2 insulator (a) cross-sectional image (b) surface image.



(a)



(b)

Figure 3-8: XPS spectra deconvolution of RF-sputtered HfO_2 insulator (a) Hf 4f (b) O 1s.

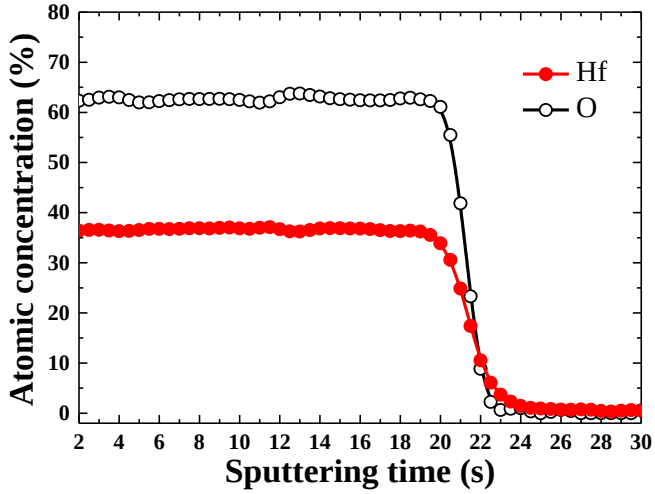


Figure 3-9: AES-depth profiles of RF-sputtered HfO_2 insulator.

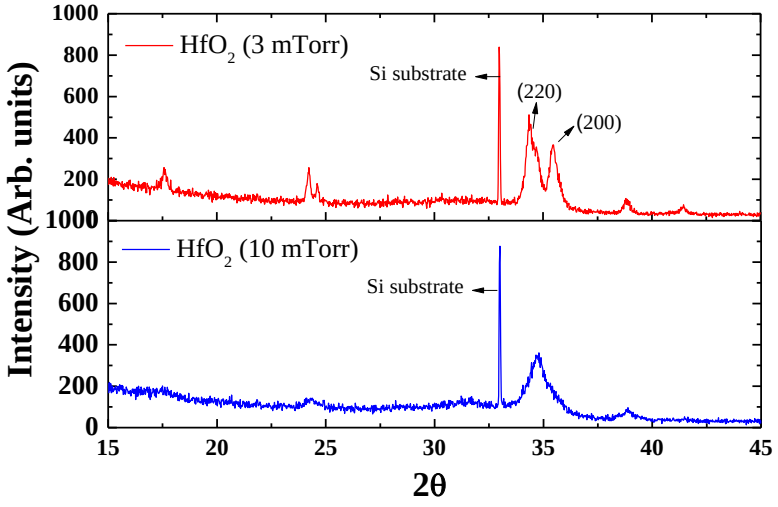
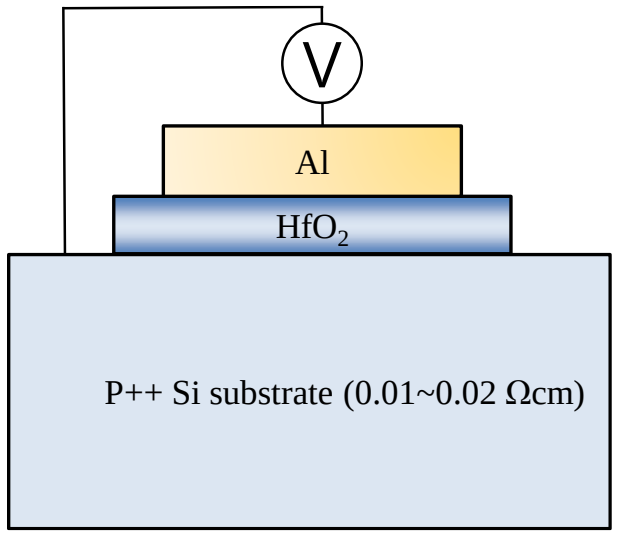
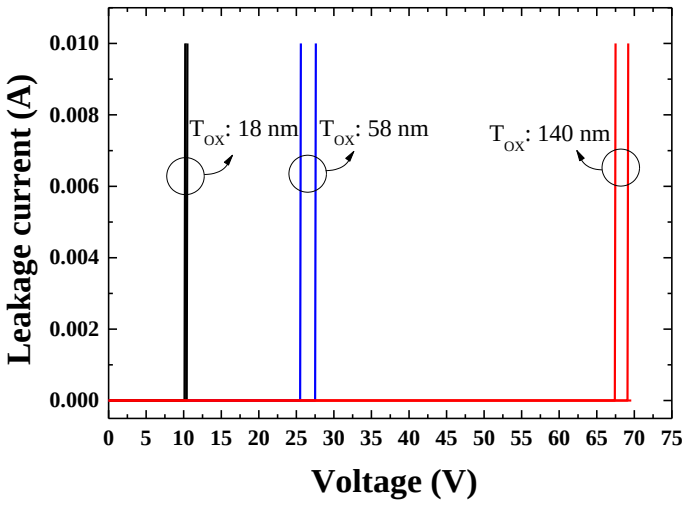


Figure 3-10: XRD results of HfO_2 insulator sputtered at 3 and 10 mTorr.



(a)



(b)

Figure 3-11: (a) Test patterns for measuring breakdown field of RF-sputtered HfO_2 insulator. MOS structure including Al-HfO_2-P^{++} Si was used (b) dielectric breakdown voltage characteristics of RF-sputtered HfO_2 in the test pattern.

3.4.2 Effects of post-deposition annealing on HfO_2 Insulator

The effect of PDA on RF-sputtered HfO_2 gate insulator is investigated in this section. PDA has important meaning, in two respects. Firstly, dielectric breakdown characteristics and crystallinity can be improved by PDA. As mentioned in previous section, the crystallinity of HfO_2 gate insulator strongly influences on blocking characteristics. At same time, thermal annealing provides small shift of V_{TH} because the thickness of HfO_2 gate insulator can be reduced due to improvement of dielectric breakdown voltage. Secondly, thermal stability of HfO_2 gate insulator can be tested by PDA. Excellent thermal stability of gate insulator provides flexibility in the fabrication sequence for the AlGaN/GaN MOS-HEMTs. This thermal stability of gate insulator is also important when post-gate annealing (PGA) to improve adhesion between gate and gate insulator [93], pre-passivation to suppress thermal damage to GaN surface [94], and PDA to improve interface trap density (D_{it}) [95] are considered. In addition, heat is produced by high-current operation [96]. The AlGaN/GaN power devices are desirable to be operated at high temperature to reduce the size of cooling system. Also, excellent thermal stability of gate insulator is necessary to achieve high-current devices.

The 100 nm-thick HfO_2 insulator was sputtered on p^+ (10~15 Ω·cm) Si substrate at room temperature. Sputtering power of 50 W, working pressure of 3 and 10 mTorr, and Ar flow of 15 sccm were used. These samples were annealed under O_2 ambient at 700 ^oC for 20 min and under H_2O ambient at 500 ^oC for 12 min, respectively. Figure 3-12 shows the XRD results of RF-sputtered HfO_2 insulator after PDA under O_2 and H_2O ambient. It was found that the crystallinity was improved with a few peaks around 27^o and 32^o at the

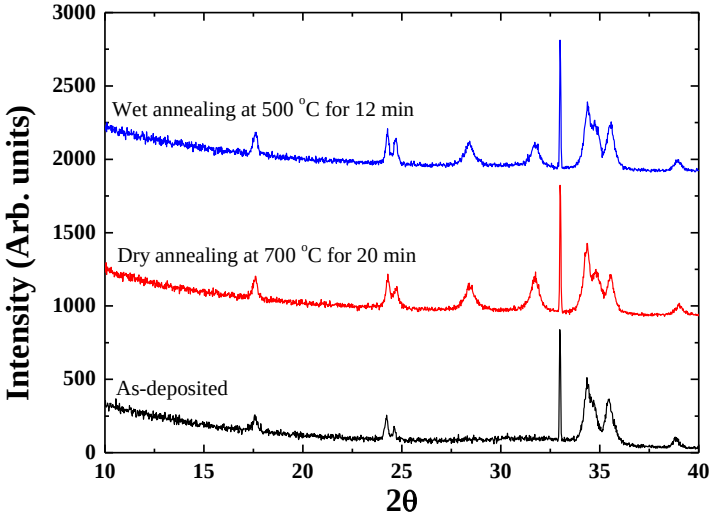
PDA sample using dry oxidation. HfO_2 sputtered at 3 mTorr exhibits better crystallinity compared to 10 mTorr. Also, those samples after PDA under H_2O ambient at 500 ^oC for 12 min show similar peaks location and magnitude as the dry oxidation samples. It means that wet oxidation for PDA is useful to decrease annealing temperature and reduce process time to crystallize RF-sputtered HfO_2 insulator.

Figure 3-13 shows the surface SEM images of the RF-sputtered HfO_2 insulator before and after PDA process with various temperature variation from 700 to 1000 ^oC for 2 hour under N_2 ambient. Same sputtering conditions and substrate as experiment above was used. The HfO_2 films after PDA at high temperature reveal a dense morphology and rough surface compared to those at low temperature. This change of the surface morphology results from poly-crystallization of RF-sputtered HfO_2 insulator by PDA process.

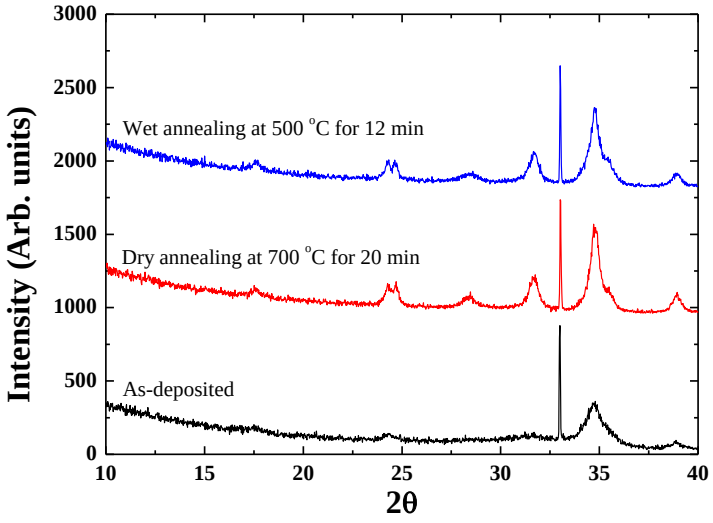
The XRD results of RF-sputtered HfO_2 insulator before and after PDA process are shown in Fig. 3-14. All PDA samples show the magnified peaks around 28.5^o, 31.8^o, and 34.8^o corresponding the peaks of poly-crystalline HfO_2. The highest values are shown in the sample with PDA at 900 ^oC. The lowered peak values in the sample after PDA at 1000 ^oC may be caused by decomposition of HfO_2 insulator. The measured sheet resistance value was also increased with PDA temperature up to 900 ^oC. The highest sheet resistance of 6×10^{12} Ω/□ was obtained at 900 ^oC while that without PDA had 1.5×10^{11} Ω·cm. However, the sheet resistance was decreased to 4×10^{12} Ω·cm after PDA at 1000 ^oC. This result is explained in view of decomposition caused by the high-temperature annealing.

Breakdown voltages before and after PDA process under N_2 ambient for 2 hours with various temperatures from 700 to 1000 ^oC were measured. Prior to HfO_2 formation, 30:1 BOE cleaning was carried out for 30 s. The 100 nm-thick HfO_2 was sputtered on p^+ Si substrate (10∼15 Ω·cm) at 50 W and 3 mTorr

with Ar flow of 15 sccm at room temperature. Ni/Au (30/150 nm) was formed on the HfO_2 insulator as anode electrode by e gun-evaporator and lift-off. Figure 3-16 shows the schematic structure of the test pattern to measure breakdown voltage. Anode voltage was swept from 0 to 100 V. The breakdown voltage of 55 V is not altered after PDA process at 700 ^oC while this is increased after PDA process at the temperature of 800 and 900 ^oC. It has good agreement with the result of sheet resistance as shown in Fig. 3-15. The highest value of 86 V was obtained at 900 ^oC. However, the breakdown voltage after PDA at 1000 ^oC shows large deviation in range from 19 to 77 V. It means that the sample after PDA at 1000 ^oC has unstable blocking characteristics due to its decomposition.



(a)



(b)

Figure 3-12: XRD results of HfO_2 insulator before and after dry and wet annealing. HfO_2 was sputtered at (a) 3 mTorr (b) 10 mTorr.

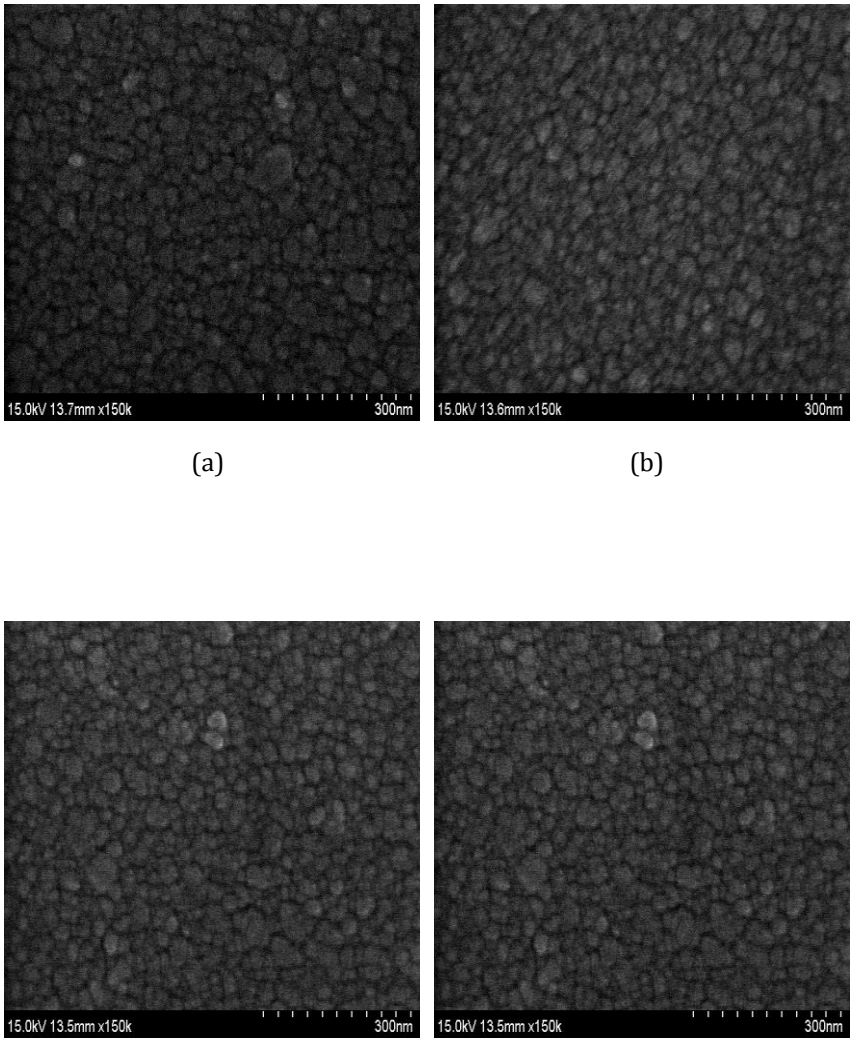


Figure 3-13: Surface SEM images after dry annealing under oxygen ambient for 2 hours at (a) 700 ^{o}C (b) 800 ^{o}C (c) 900 ^{o}C (d) 1000 ^{o}C.

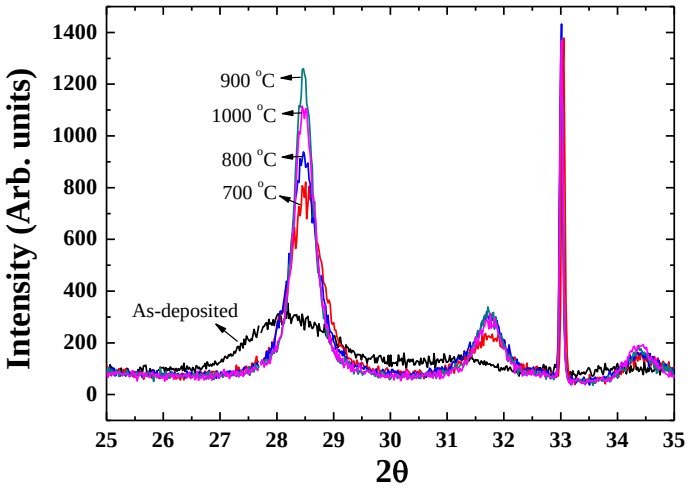


Figure 3-14: XRD results of RF-sputtered HfO_2 before and after dry oxidation for 2 hours at various temperatures.

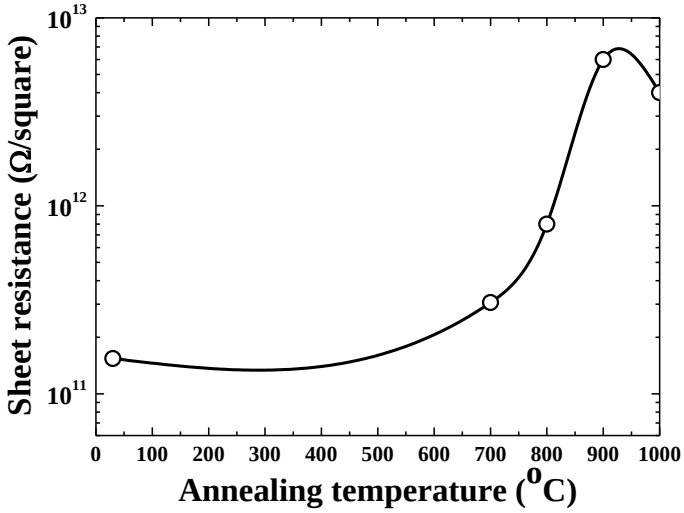
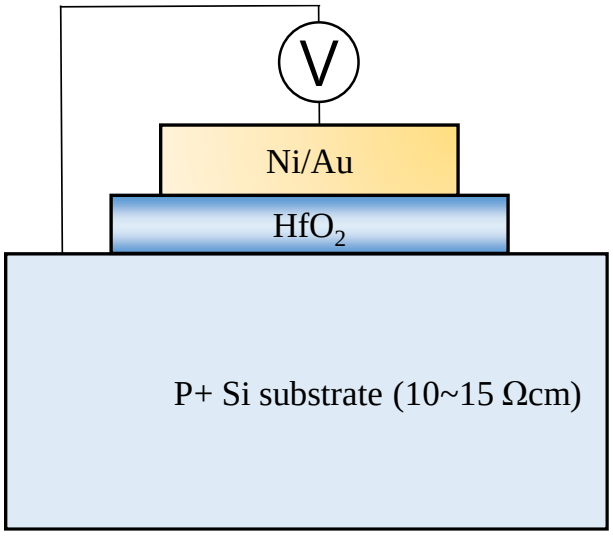
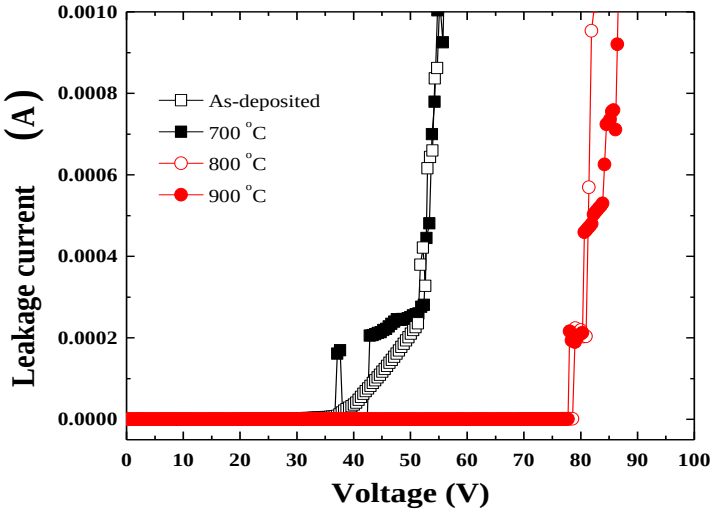


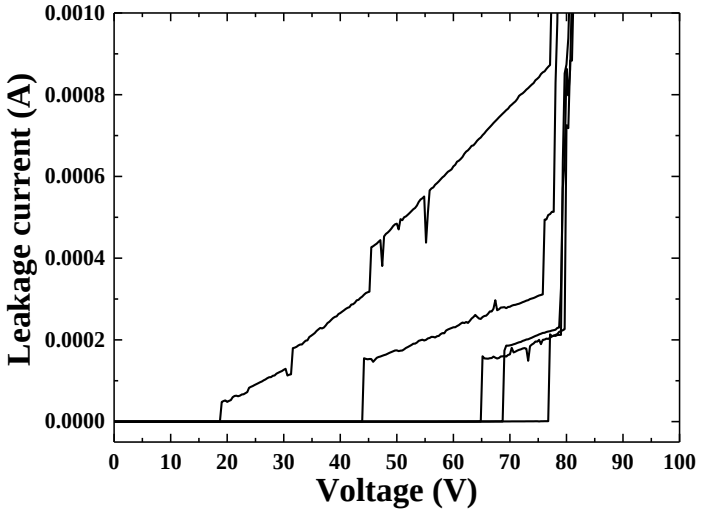
Figure 3-15: Sheet resistance of RF-sputtered HfO_2 insulator before and after dry oxidation for 2 hours at various temperatures.


V
Ni/Au
HfO2
P+ Si substrate (10~15 Ωcm)

(a)


Leakage current (A)
Voltage (V)
As-deposited
700 °C
800 °C
900 °C
0.0010
0.0008
0.0006
0.0004
0.0002
0.0000
0
10
20
30
40
50
60
70
80
90
100

(b)



(c)

Figure 3-16: (a) Test pattern for measuring breakdown field of RF-sputtered HfO_2 insulator. MOS structure including Ni/Au-HfO_2-P^+ Si was used. (b) breakdown voltage characteristics before and after PDA process with various temperatures including 700, 800, and 900 ^oC for 2 hours under N_2 ambient (c) breakdown voltage characteristics after PDA at 1000 ^oC for 2 hours under N_2 ambient.

3.5 Electrical Properties of AlGaN/GaN MOS-HEMTs Employing HfO_2 Gate Insulator

The AlGaN/GaN metal-oxide semiconductor high-electron-mobility transistors (MOS-HEMTs)-on-Si (111) substrate using RF-sputtered HfO_2 gate insulator was fabricated [97]. Schematic of the fabricated AlGaN/GaN MOS-HEMTs are shown in Fig. 3-17. The MOCVD-grown epitaxial layers consist of 3 nm-thick GaN cap/20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier/1 nm-thick AlN spacer/100 nm-thick i-GaN/3.9 μm-thick C-doped GaN buffer. The 270-deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) was deposited for source and drain by using e-gun evaporator and lift-off technique. This was annealed at 880 ^{o}C for 40 s to form ohmic contact. Prior to HfO_2 sputtering, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, the HfO_2 was sputtered at 3 and 10 mTorr with Ar flow of 15 sccm at room temperature. The 15 nm-thick HfO_2 was obtained at sputtering power of 50 W and sputtering time of 20 min. As described in previous section, 15 nm-thick HfO_2 is enough to sustain positive V_{GS} up to 5 V. And finally, the Ni/Au (30/150 nm) was formed for gate electrode by e-gun evaporator and lift-off. The gate length, gate–source distance, gate–drain distance, and gate width were 3, 3, 20, and 50 μm, respectively. The conventional AlGaN/GaN HEMT without any gate insulator was also fabricated for comparison purpose. The schematic structure of the fabricated AlGaN/GaN MOS-HEMT using HfO_2 gate insulator is shown in Fig. 3-17.

In the experiments using various sputtering powers from 50 to 300 W, sputtering damage to GaN surface was found as shown in Fig. 3-18. High

sputtering power can affects surface leakage current by generating shallow traps so that low sputtering power is desired to high breakdown voltage of the AlGaN/GaN MOS-HEMTs [98, 99, 100]. At sputtering power of 300 W, high drain leakage current of 99.1 μA/mm is shown at V_{GS}= –10 V and V_{DS}= 100 V while the devices using HfO_2 gate insulator sputtered at 50 W has drain leakage current of 67 pA/mm as shown in Fig. 3-18. These results are caused by sputtering damage at high sputtering power regardless of well-blocked gate leakage current. Thus, I fixed the sputtering power to 50 W to achieve high breakdown voltage of the AlGaN/GaN MOS-HEMTs in the following experiments.

In this section, electrical characteristics of the AlGaN/GaN MOS-HEMTs employing RF-sputtered HfO_2 gate insulator will be systematically discussed. Especially, I would focus on the mechanism of high breakdown voltage of the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator by measuring various electrical characteristics including reverse and forward characteristics, capacitance-voltage (*C*-*V*) characteristics, pulsed current-voltage (*I*-*V*) characteristics, and reliability characteristics.

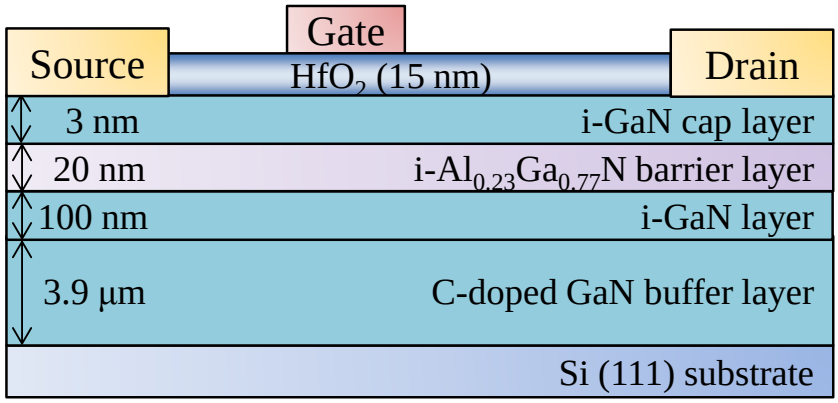


Figure 3-17: Cross-sectional view of fabricated AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator.

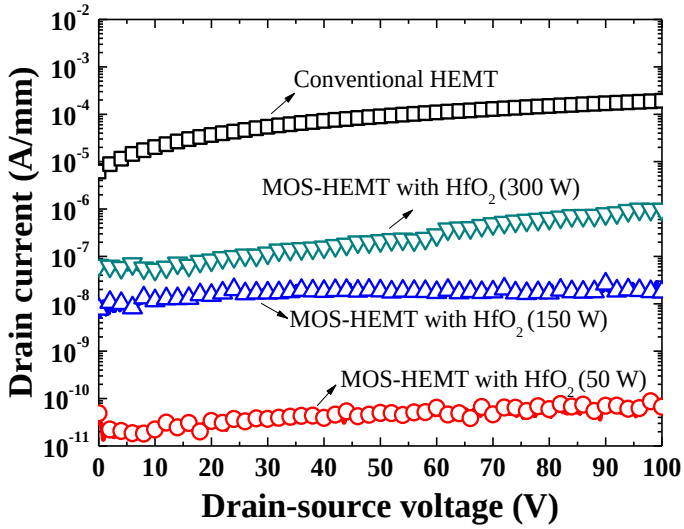


Figure 3-18: Drain leakage current of AlGaN/GaN HEMT and MOS-HEMTs using HfO_2 gate insulator sputtered at 50, 150, and 300 W.

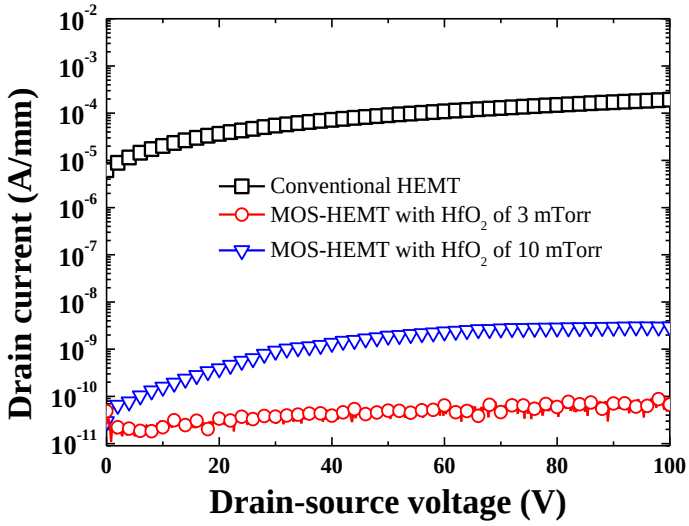
3.5.1 Reverse Blocking Characteristics

Drain and gate leakage current of the AlGaN/GaN HEMT and MOS-HEMTs using HfO_2 gate insulator sputtered at 3 and 10 mTorr are shown in Fig. 3-19. V_{DS} was swept from 0 to 100 V with V_{GS} of −10 V. Very low drain leakage current of 67 pA/mm at V_{DS} of 100 V for the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator sputtered at 3 mTorr was measured. Also, the device using HfO_2 gate insulator sputtered at 10 mTorr has drain leakage current of 3 nA/mm. It is explained that weakly crystallized HfO_2 insulator improves its blocking characteristics when it was sputtered at low working pressure. However, the conventional HEMT without any gate insulator has drain leakage current of 192 μA/mm. The gate leakage current at V_{DS} of 100 V and V_{GS} of −10 V is also decreased from −44.7 μA/mm to −67 pA/mm by HfO_2 gate insulator sputtered at 3 mTorr. The high drain and gate leakage current of the conventional AlGaN/GaN HEMT is originated from considerable number of surface states, such as dislocation from the GaN buffer/substrate interface and nitrogen vacancies (V_N), which are induced by plasma and thermal processes [101, 10].

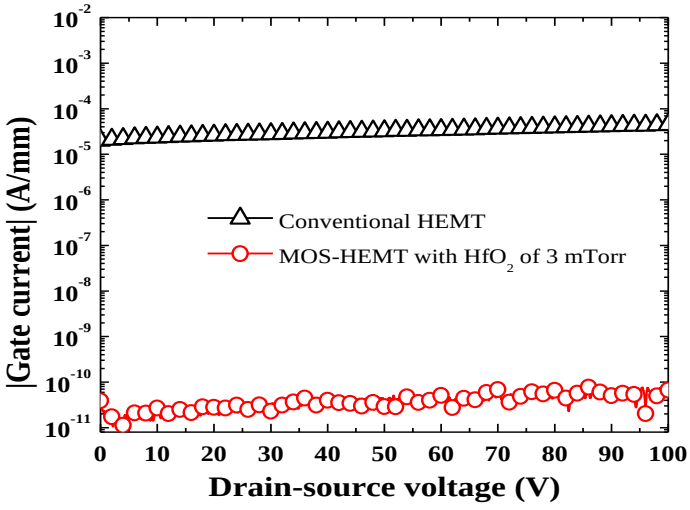
Figure 3-20 (a) shows the three-terminal breakdown voltage characteristics of the conventional HEMT and the MOS-HEMTs with HfO_2 gate insulator sputtered at 3 and 10 mTorr at V_{GS} of −10 V. It has been demonstrated that the breakdown voltage was measured at the drain leakage current of 1 mA/mm. The breakdown voltage of the MOS-HEMT with HfO_2 gate insulator sputtered at 3 mTorr is 1524 V while the device with HfO_2 sputtered at 10 mTorr has 1226 V. However, that of the conventional HEMT is 470 V. It means that low working pressure for HfO_2 sputtering is useful to improve breakdown voltage. As shown in Fig. 3-20 (b) the two-terminal breakdown voltage of the AlGaN/GaN MOS-HEMT are similar with the result

of three-terminal measurement. It means that breakdown in the AlGaN/GaN HEMTs or the MOS-HEMTs occurs at drain-sided gate edge due to electric field concentration and surface leakage current, that is to say the breakdown voltage of the AlGaN/GaN HEMTs is determined by electron runaway on the surface [102]. The injected electrons from gate into the surface states lead to surface leakage current in the conventional HEMTs and the MOS-HEMTs.

In order to investigate the mechanism of breakdown voltage improvement by HfO_2 gate insulator, I assumed the contribution to increase breakdown voltage can be divided into two factors. First factor is that from HfO_2 surface passivation effects and second one is that from blocking characteristics of gate leakage current by HfO_2 gate insulator. In the following section, I will describe the origin of leakage current in the AlGaN/GaN HEMT and represent systematical investigation of reverse blocking characteristics in the AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator.

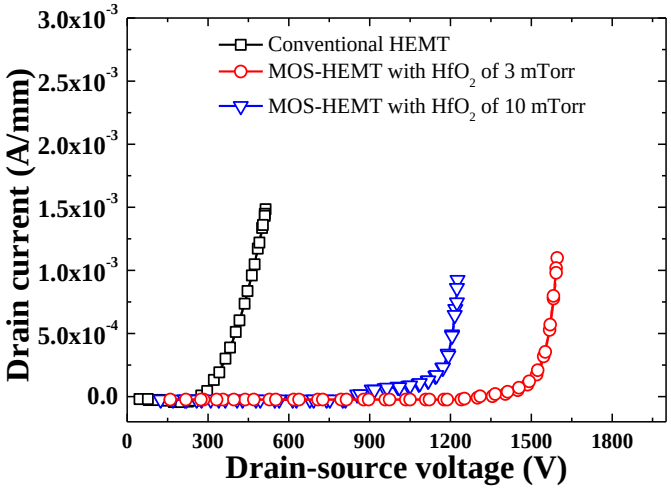


(a)

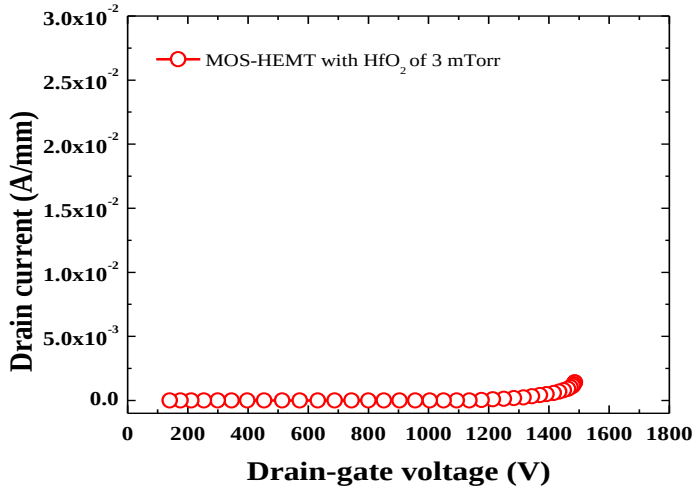


(b)

Figure 3-19: (a) Drain leakage current of AlGaN/GaN HEMT and MOS-HEMT with RF-sputtered HfO_2 at V_{GS}= –10 V (b) gate leakage current.



(a)



(b)

Figure 3-20: (a) Three-terminal breakdown voltage characteristics of AlGaN/GaN HEMT and MOS-HEMTs with HfO_2 sputtered at 3 and 10 mTorr (b) two-terminal breakdown voltage characteristics of AlGaN/GaN MOS-HEMT with HfO_2 of 3 mTorr.

3.5.2 Suppression of Surface Leakage Current

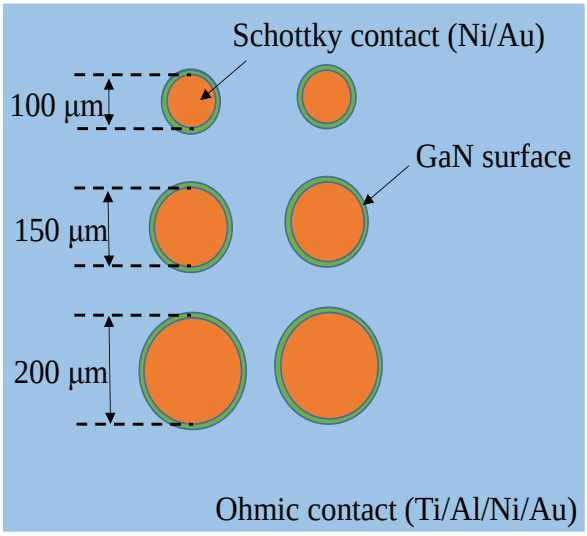
In order to investigate the origin of leakage current in the AlGaN/GaN heterostructure, I fabricated the circular-type AlGaN/GaN SBDs with three-different anode diameter. Top-view of the fabricated devices with anode diameter of 100, 150, and 200 μm are shown in Fig. 3-21 (a). 270 nm-deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) and Ni/Au (30/150) were used for anode and cathode, respectively. The anode-cathode distance was 3 μm. This sample was not passivated.

For an accurate analysis of leakage current path, the leakage current though GaN buffer layer should be evaluated. If the resistivity characteristics of GaN buffer layer is not enough to block leakage current, total leakage current would be affected by this component and the measured values should have square relationship with anode diameter due to the vertical leakage current [103]. On the other hand, if the leakage current is originated from only surface, the leakage current should be linearly increased with anode diameter.

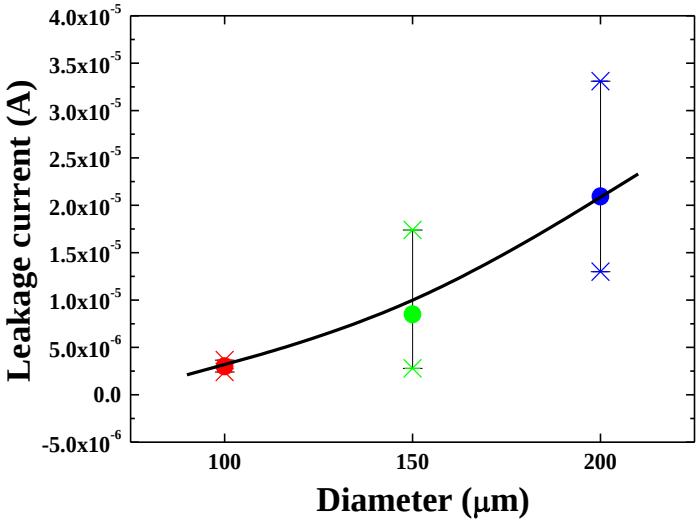
The cathode-anode voltage (V_{CA}) was swept from 0 to 100 V to measure leakage current of the circular AlGaN/GaN SBDs with three-different anode diameter. These samples show rather leakage current deviation so that I measured 20 devices for each anode diameter as shown in Fig. 3-21 (b). The larger deviation of leakage current was observed at longer anode diameter. The measurement results show that the average values of leakage current at V_{CA} of 100 V is increased proportionally to anode diameter as shown in Fig. 3-21 (c). It indicates that the surface leakage current is dominant in the epitaxial layer used in this experiment. As described in section 2.3.3, the carbon doping is useful to improve semi-insulating characteristics in GaN buffer layer. The carbon impurities act as shallow acceptor in GaN when Fermi level (E_F) is close

to the conduction band [104, 105]. Thus, carbon doping is very effective method to reduce buffer leakage current [20]. Thus, I concluded the vertical leakage current through buffer layer can be eliminated for investigation of leakage current in the following section.

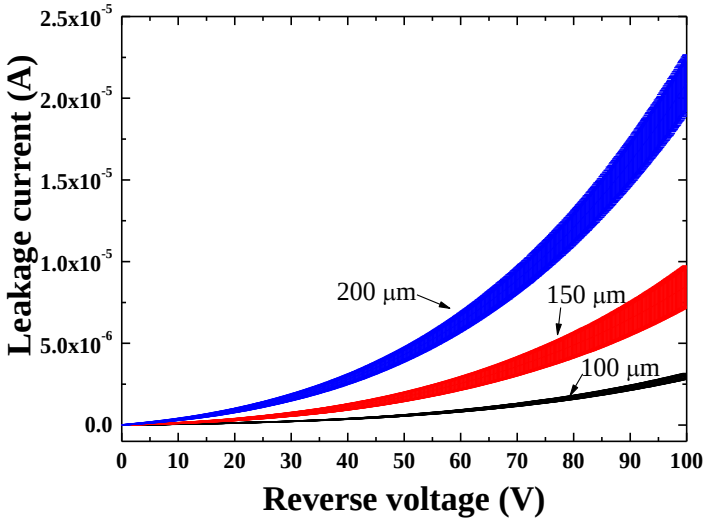
Based on above results, I investigated the passivation effects of RF-sputtered HfO_2 insulator on the AlGaN/GaN heterostructure. Mesa-isolated two ohmic pattern was fabricated as shown in Fig. 3-22. The 15 nm-thick HfO_2 passivation and the ohmic-to-ohmic distance of 20 μm were used. This structure doesn't include any Schottky contact so that blocking of gate leakage current can be excluded. At high drain voltage situation in the AlGaN/GaN MOS-HEMTs, this surface leakage current through isolation region is very important because there is no depletion region at an isolated region by mesa etching. The surface leakage current when 100 V is applied is considerably reduced from 87.7 μA mm to 81.7 pA/mm after 15 nm-thick HfO_2 passivation. It indicates that the RF-sputtered HfO_2 insulator is useful to improve the surface problems such as leakage current and electron trapping into the surface states by passivating the GaN surface. The HfO_2 may also suppress the damage introduced by mesa etching and thermal annealing. In addition, this result proves clearly that this suppression of surface leakage current by HfO_2 passivation is dominant mechanism of high breakdown voltage in the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator.


Schottky contact (Ni/Au)
100 μm
GaN surface
150 μm
200 μm
Ohmic contact (Ti/Al/Ni/Au)

(a)

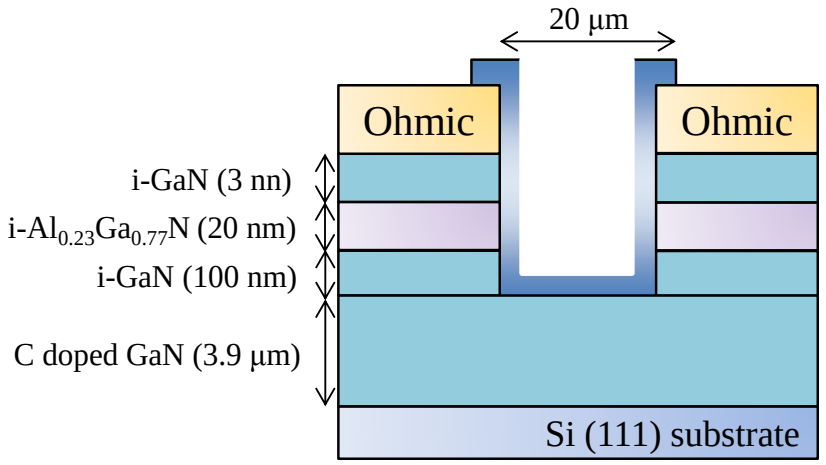

Leakage current (A)
4.0x10-5
3.5x10-5
3.0x10-5
2.5x10-5
2.0x10-5
1.5x10-5
1.0x10-5
5.0x10-6
0.0
-5.0x10-6
100
150
200
Diameter (μm)

(b)

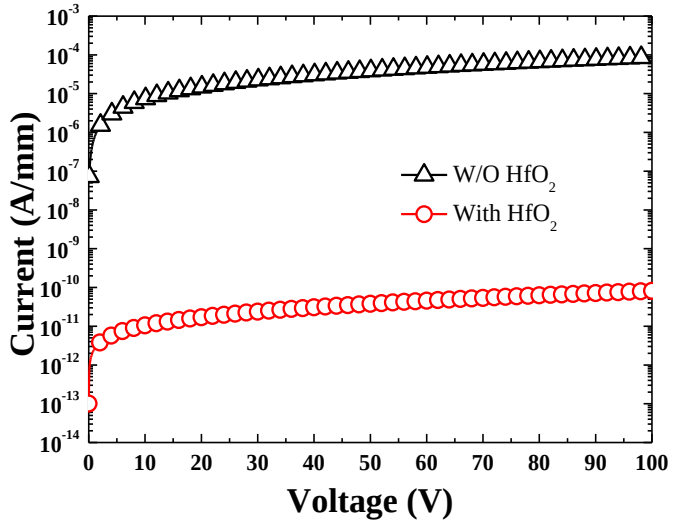


(c)

Figure 3-21: (a) Top view of the circular AlGaN/GaN SBDs for investigation into leakage current path. Three-different anode-diameters were used. (b) leakage current according to anode diameter (c) leakage current and its deviation.



(a)

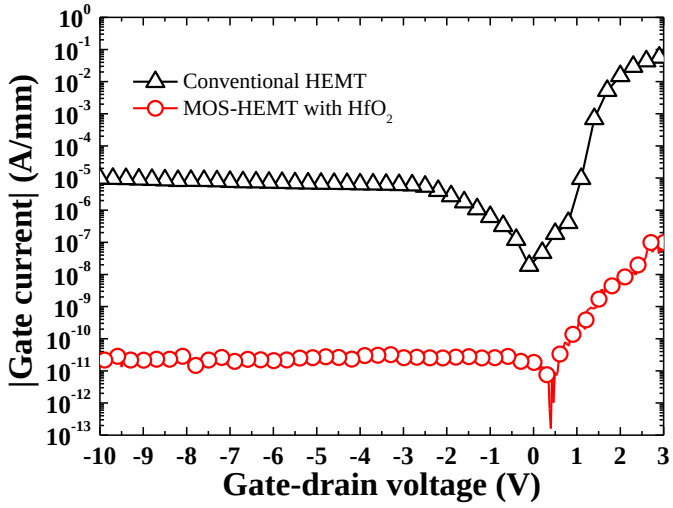


(b)

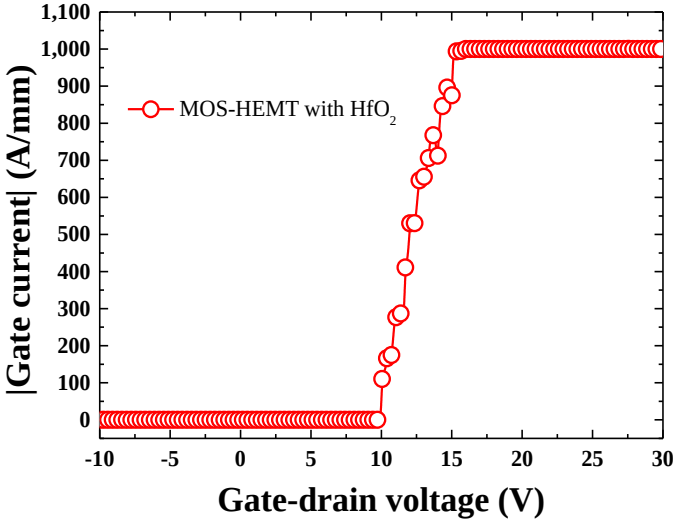
Figure 3-22: (a) Mesa-isolated two ohmic pattern to investigate the passivation effects of HfO_2 insulator on the AlGaN/GaN MOS-HEMTs (b) leakage current before and after HfO_2 passivation.

3.5.3 Blocking Forward and Reverse Gate Leakage Current

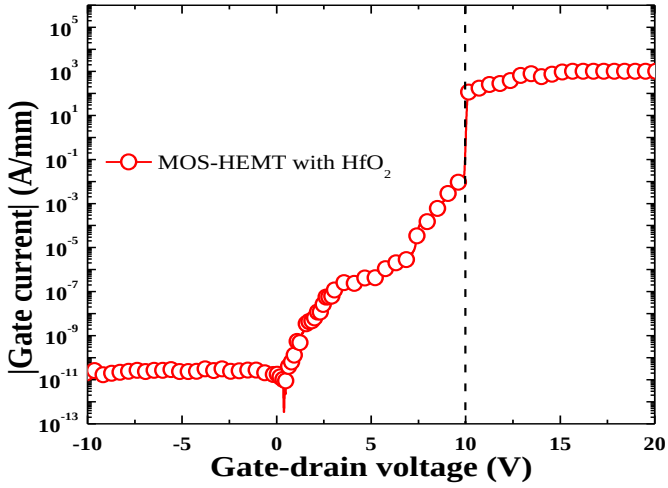
Figure 3-23 (a) shows gate–drain diode *I*–*V* characteristics of the conventional HEMT and the MOS-HEMT with HfO_2. This *I*-*V* measurement was performed to directly evaluate the blocking properties of gate leakage current by HfO_2 gate insulator. Blocking gate leakage current is important to obtain reliable and high-voltage devices. I swept the gate-drain voltage (V_{GD}) from –10 to 3 V. The 15 nm-thick HfO_2 gate insulator blocks the leakage current under both a positive and a negative bias. The forward leakage current of the MOS-HEMTs is 11 nA/mm when V_{GD}= 3 V, while this value for the conventional HEMT is 56 mA/mm. The reverse leakage current is also reduced by the HfO_2 gate insulator from −9.7 μA/mm for the conventional HEMT to −33 pA/mm for the MOS-HEMT with HfO_2 when V_{GD}= −10 V. Asymmetry *I*-*V* characteristics between forward and reverse region result from presence of depletion region underneath the gate at reverse bias. Thus, the higher serial resistivity under the reverse bias along MOS structure brought out the lower leakage current compared to that under forward bias. The MOS-HEMT with HfO_2 is capable of a positive gate bias of up to 10 V as shown in Fig. 3-23 (b) and (c). HfO_2 effectively blocks the forward gate leakage current by means of hot carrier-induced tunneling via the gate insulator. High forward-gate breakdown voltage meaning high-current capability is desired in the AlGaN/GaN MOS-HEMTs. Thicker gate insulator causes negative shift of V_{TH} so that high breakdown field of gate insulator is needed. The breakdown field over 6.7 MV/cm was achieved in this gate-drain MOS diodes. Even if the channel resistance should be considered, channel resistance doesn't affect the validity of breakdown field because electrons are accumulated at the HfO_2/GaN interface underneath the gate at the high gate-drain bias.


Conventional HEMT
MOS-HEMT with HfO2
|Gate current| (A/mm)
Gate-drain voltage (V)

(a)


MOS-HEMT with HfO2
|Gate current| (A/mm)
Gate-drain voltage (V)

(b)



(c)

Figure 3-23: (a) Gate-drain diode *I-V* characteristics of AlGaN/GaN HEMT and MOS-HEMT using RF-sputtered HfO_2 gate insulator (b) forward gate breakdown of AlGaN/GaN MOS-HEMT in linear scale (c) forward gate breakdown of AlGaN/GaN MOS-HEMT in log scale.

3.5.4 Switching Characteristics

Figure 3-24 shows the measured transfer characteristics of the fabricated devices when V_{DS} is 5 V. The on/off current ratio is determined at $I_{D,ON}$ when V_{GS}= 0 V and $I_{D,OFF}$ when V_{GS}= −10V. The on/off current ratio of the MOS-HEMT with HfO_2 gate insulator (2.37×10^{10}; $I_{D,OFF}$= 8.01 pA/mm and $I_{D,ON}$= 191 mA/mm) is dramatically improved compared to that of the conventional HEMT of 7.61×10^{3} ($I_{D,OFF}$= 23 μA/mm and $I_{D,ON}$= 175 mA/mm). The high on/off current ratio indicates that the HfO_2 successfully suppresses the gate leakage current as well as the isolation leakage current from drain to source. The V_{TH} values of the conventional HEMT and the MOS-HEMT with HfO_2 are −2.3 and −4.2 V, respectively. The maximum transconductance value is decreased from 91.6 to 80.7 mS/mm by HfO_2 gate insulator. MOS structure provides longer distance between gate and 2DEG channel as well as weak controllability over 2DEG channel compared to the conventional Schottky-gate. Thus, high-*k* gate insulator materials are desired to improve gate controllability over 2DEG channel. I also fabricated the AlGaN/GaN MOS-HEMT using a 15 nm-thick ICP-CVD-SiO_2 gate insulator and the same epitaxial structure as the proposed device using HfO_2 for comparing purpose. The MOS-HEMT using SiO_2 exhibits considerably low V_{TH} of −15.8 V due to the low-*k* characteristics of SiO_2. At the higher V_{GS} than 0 V, the transconductance is decreased by the electrons over-flown from 2DEG channel and AlGaN barrier accumulation phenomena.

In Fig. 3-25, the transfer characteristics were measured at V_{GS} range from −100 to 10 V to confirm stable switching characteristics of the AlGaN/GaN MOS-HEMT using HfO_2 gate insulator. The MOS-HEMT shows no significant increase of leakage current even highly negative V_{GS} is applied up to −100 V. The forward breakdown occurs at high V_{GS} of 9.2 V. It indicates that RF-sputtered HfO_2 gate insulator is suitable for the high applications.

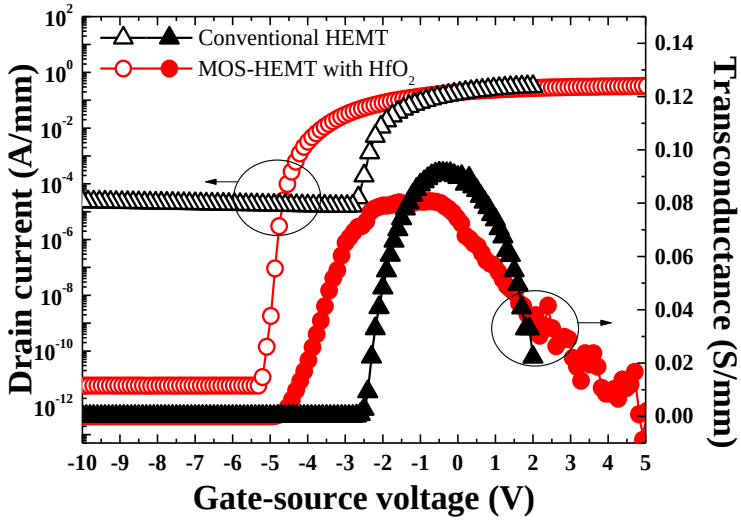


Figure 3-24: Transfer characteristics of AlGaN/GaN HEMT and MOS-HEMT with RF-sputtered HfO_2 at V_{DS} of 10 V.

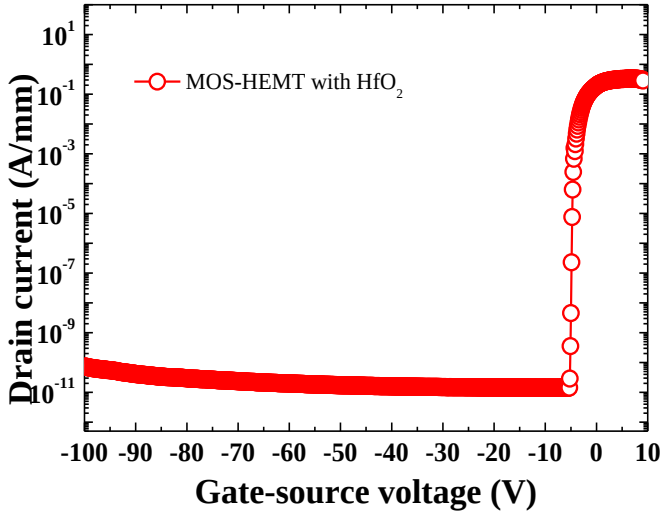
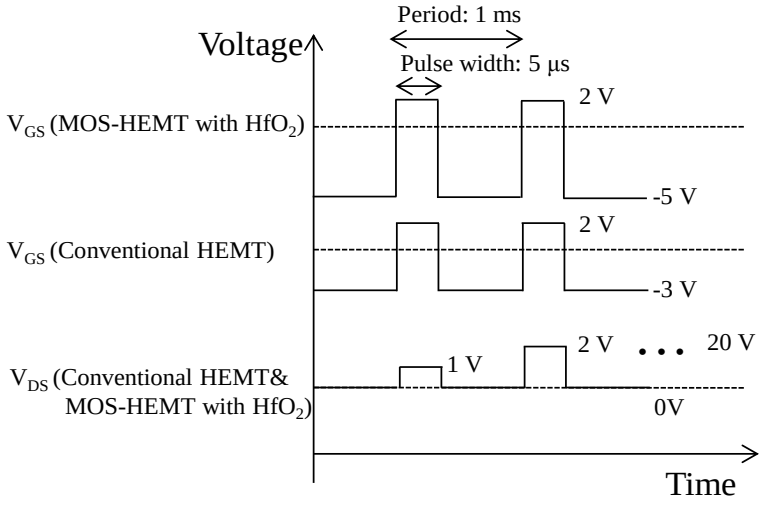


Figure 3-25: Transfer characteristics of AlGaN/GaN MOS-HEMT with RF-sputtered HfO_2 at V_{DS} of 10 V in the V_{GS} range from –100 to 10 V.

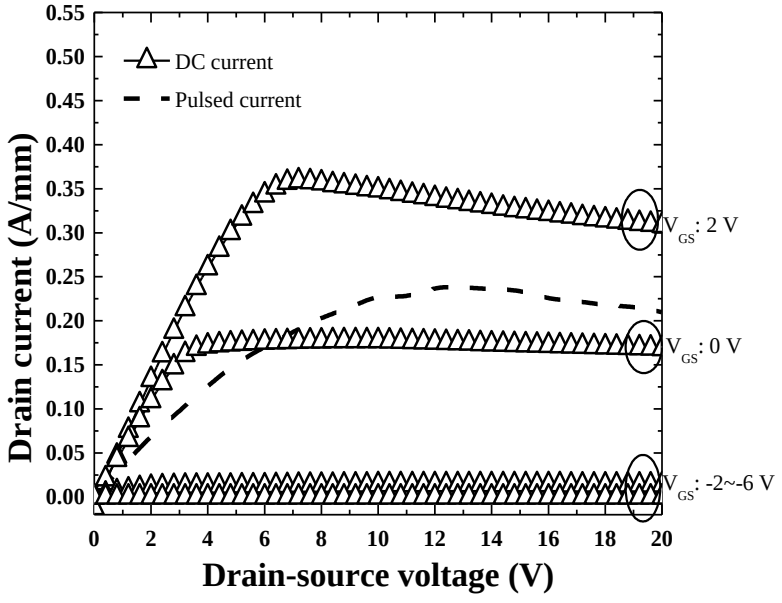
3.5.5 Pulsed *I-V* Characteristics

Figure 3-26 shows the DC and pulsed output I–V of the AlGaN/GaN HEMT and the MOS-HEMT with HfO_2 gate insulator. The V_{GS} for DC output *I–V* was swept from 2 to −6 V at −2 V increment. The pulsed *I–V* measurement conditions are presented in timing diagram of Fig. 3-26 (a). I used base V_{GS} of −3 V for the conventional HEMT and that of −5 V for the MOS-HEMT with HfO_2 due to the different V_{TH} values between the two devices. And, pulse width of 5 μs and period of 1 ms were used. The maximum DC drain current of the MOS-HEMT at V_{GS} of 2 V is 330 mA/mm and that of the conventional HEMT is 359 mA/mm. This decrement of drain current agrees well with the transconductance shown in section 3.5.4. Drain current degradation of the MOS-HEMT with HfO_2 under pulsed gate and drain bias was less than that of the conventional device, indicating that the HfO_2 gate insulator suppresses the surface trap effects or prevents a current collapse in the AlGaN/GaN MOS-HEMT. The measured $I_{D,pulse}/I_{D,DC}$ ratio at V_{GS} of 2 V is increased from 0.68 to 0.87.

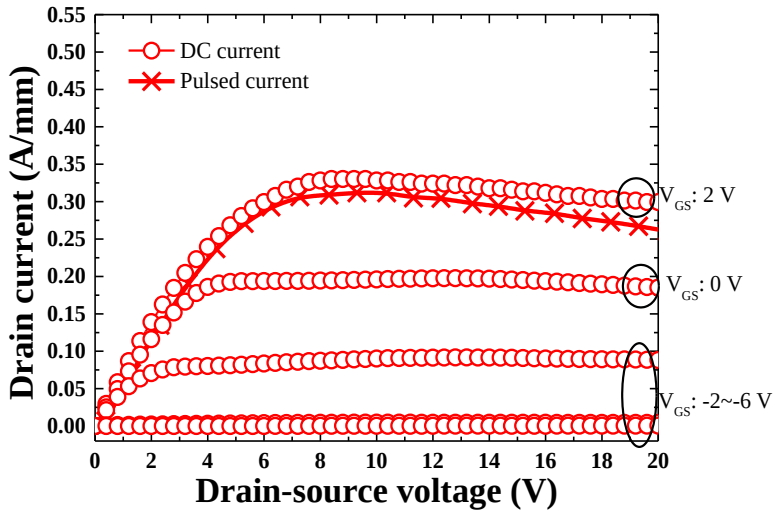
Pulsed output *I-V* measurement is useful for analysis of an electron trapping effects in the AlGaN/GaN heterostructure-based devices. Pulsed *I-V* measurement includes self-heating and the electron trapping effects depending on applied bias, pulse width, and period [106]. In this measurement, the thermal effects-related current reduction cannot be ignored because of a rather long pulse width of 5 μs. Decrease of pulsed drain current in the conventional AlGaN/GaN HEMT results from slow response of electrons to test signal due to trapping into surface shallow traps. The electrons trapping is suppressed by RF-sputtered HfO_2 gate insulator so that channel modulation of the MOS-HEMT with HfO_2 gate insulator may be faster than the conventional HEMT.


Period: 1 ms
Voltage
Pulse width: 5 μs
2 V
V_{GS} (MOS-HEMT with HfO_2)
-5 V
2 V
V_{GS} (Conventional HEMT)
-3 V
2 V
20 V
1 V
V_{DS} (Conventional HEMT&
MOS-HEMT with HfO_2)
0V
Time

(a)


DC current
Pulsed current
V_{GS}: 2 V
V_{GS}: 0 V
V_{GS}: -2~-6 V
Drain current (A/mm)
Drain-source voltage (V)
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
0
2
4
6
8
10
12
14
16
18
20

(b)



(c)

Figure 3-26: (a) Timing diagram for pulsed *I-V* measurement (b) DC and pulsed output *I-V* characteristics of the conventional AlGaN/GaN HEMT (c) DC and pulsed *I-V* characteristics of the AlGaN/GaN MOS-HEMT using RF-sputtered HfO_2 gate insulator.

3.5.6 Reliability of AlGaN/GaN MOS-HEMTs

The drain and gate leakage current were monitored with fixed bias condition to evaluate reliability characteristics of reverse blocking under negative DC stress. The V_{GS} of –10 V and V_{DS} of 100 V were applied for 100 s. The drain leakage current of the conventional HEMT and the MOS-HEMT using HfO_2 gate insulator are shown in Fig. 3-27. The drain leakage current of the conventional AlGaN/GaN HEMT is increased from 57.4 to 496 μA/mm after negative DC stress of 100 s. The injected electrons into the surface states during measurement increase the leakage current more.

However, drain leakage current of the AlGaN/GaN MOS-HEMTs with HfO_2 gate insulator are not altered after 100 s. Figure 3-28 shows the drain and gate leakage current of the AlGaN/GaN MOS-HEMT according to measuring time. Thus, all experimental results in section 3.5 reveal that RF-sputtered HfO_2 gate insulator provides stable blocking characteristics of the AlGaN/GaN MOS-HEMTs.

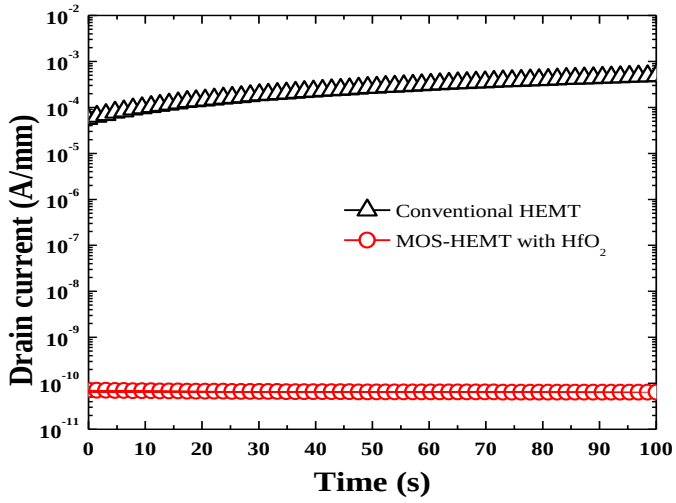


Figure 3-27: Monitored drain leakage current of conventional HEMT and MOS-HEMT with HfO_2 for 100 s.

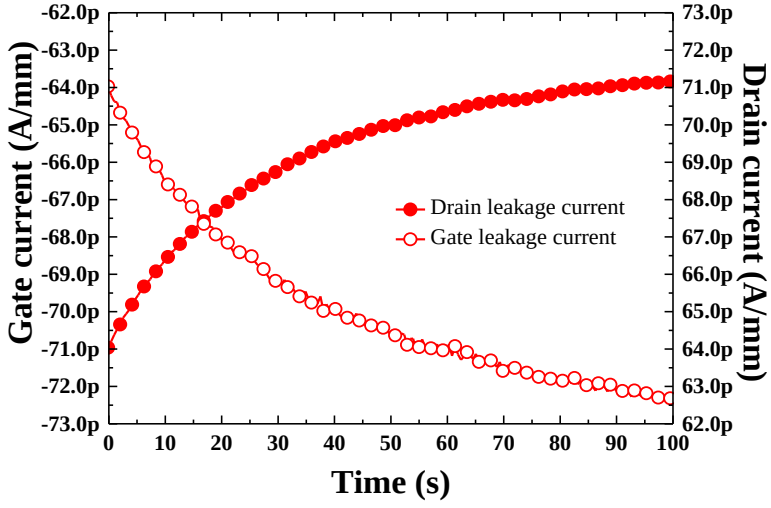


Figure 3-28: Monitored drain leakage current and gate leakage current of AlGaN/GaN MOS-HEMT with HfO_2 for 100 s.

3.5.7 Capacitance-Voltage Characteristics

Figure 3-29 shows capacitance-voltage (*C*-*V*) characteristics of the AlGaN/GaN MOS-HEMT using HfO_2 gate insulator sputtered at 3 mTorr and 50 W. I varied maximum gate-source bias with fixed frequency of 1 MHz to investigate response of electrons to HfO_2/GaN interface states. The capacitance curve with V_{GS} sweeping range from –10 to –0.5 V has a small hysteresis of 100 mV near V_{TH}. However, the capacitance curve with V_{GS} sweeping range from –10 to 5 V has a large hysteresis of 1.1 V corresponding acceptor-like traps at the HfO_2/GaN interface [107]. The electrons are accumulated at AlGaN barrier layer and capacitance increases with steep slope when gate bias is higher than 2.5 V.

Figure 3-30 shows the *C*-*V* characteristics with measuring frequencies of 1, 10, 100 kHz, and 1 MHz. At all frequency conditions, almost indentical hysteresis near V_{TH} is observed. However, the lower frequency causes the high capacitance value and the large hysteresis at positive V_{GS} range. This high capacitance values are originated from the electron capturing at the oxide/GaN interface [65]. This result indicates that the electron capturing at HfO_2/GaN interface states is a slow process which responds to the lower frequency than 1 MHz. The partial electrons which cannot be emitted during revese sweep is dominant reason for large hysteresis at positive V_{GS} range. The similar hysteresis values near V_{TH} in the AlGaN/GaN MOS-HEMT using RF-sputtered HfO_2 gate insulator provides stable operation at various frequencies.

Interface trap density (D_{it}) is extracted by terman's method using high frequency *C*-*V* characteristics to preciously evaluate interface quality between

HfO_2 gate insulator and the AlGaN/GaN heterostructure. Terman's method uses strech-out phenomenon caused by interface traps when the *C-V* characteristics are measured at high frequency. I summaried material parameters for the extraction of D_{it} in Table 3-1. The D_{it} can be extracted by comparing two curves between ideal C-ψ_S and experimental C-V_{GS} results as shown in Fig. 3-31. Ideal C-ψ_S was cacluated by below relationship [108].

$$C_T = [\frac{1}{C_{HfO2}} + \frac{1}{C_{it}+(\frac{1}{C_{AlGaN}}+\frac{1}{C_{2DEG}})^{-1}}]^{-1}] \qquad (3.1)$$

$$\text{where } C_{2DEG} = \frac{qN_{eff}}{KT}(1+e^{-\eta_{F,well}})^{-1} \text{ and } N_{eff} = \frac{m^*KT}{\pi\hbar^2}$$

N_{eff} and $\eta_{F,well}$ are effective conduction-band density-of-states and normalized Fermi energy relative to the conduction band in the quantum well, respectively. In this extraction method for D_{it}, I assumed AlGaN barrier as serial insulating layer with HfO_2 gate insulator. The material parameter used for this calculation is summaried in [109, 110, 111, 112]. After calculation of ideal C-ψ_S curve, I matched it with experimental result os C-V_{GS} curve. Then, I obtain $\partial V_{GS}/\partial\psi_S$ relationship from two curves. Finally D_{it} was extracted by following equation [113].

$$D_{it} = \frac{C_{HfO2}}{q}\left[\left(\frac{\partial\psi_S}{\partial V_{GS}}\right)^{-1} - 1\right] - \frac{C_{2DEG}}{q} \qquad (3.2)$$

By using this terman's method, I obtained D_{it} distribution as shown in Fig. 3-32. The extracted D_{it} value at 0.1 eV below the conduction band minimum is 6×10^{12} $cm^{-2}\cdot eV^{-1}$.

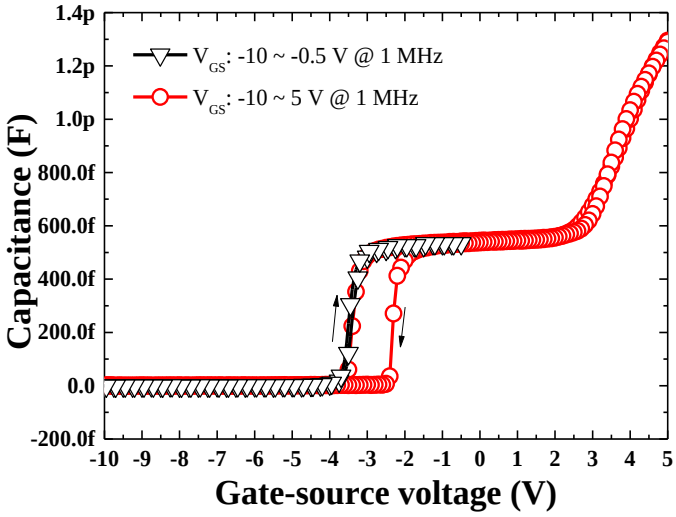


Figure 3-29: *C-V* characteristics of AlGaN/GaN MOS-HEMT with variation of maximum V_{GS} sweeping range.

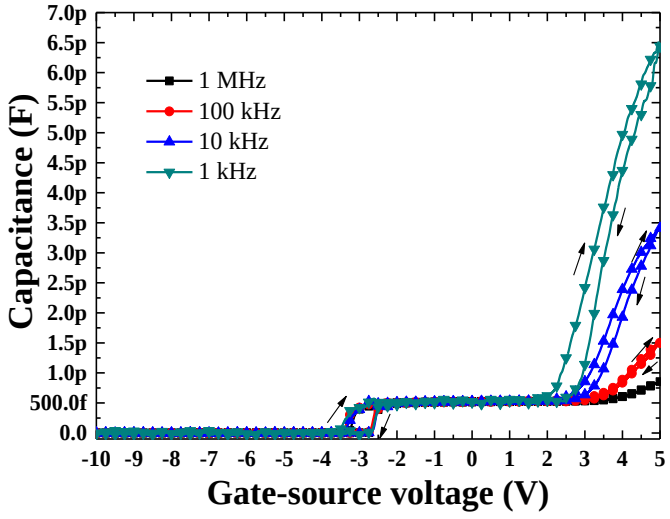


Figure 3-30: *C-V* characteristics of AlGaN/GaN MOS-HEMT with variation of measuring frequency.

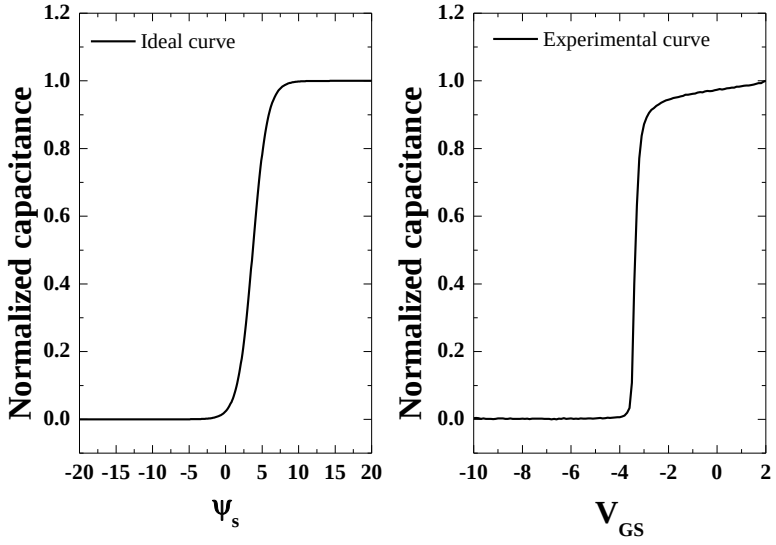


Figure 3-31: *C-V* characteristics for ideal and experimental results.

Table 3-1: Material parameter of AlGaN/GaN heterostructure for D_{it}-extraction [109, 110, 111, 112].

Parameter name	Unit	Numerical value
Bandgap at RT	eV	3.42 (GaN) 3.87 (AlGaN)
Effective mass of electron	m_n/m_e	0.22 (GaN) 0.22 (AlGaN)
Permittivity		9.5 (GaN) 9.38 (AlGaN) 11.89 (HfO_2)
Band offset	eV	0.312 (AlGaN/GaN)
T_{HfO2}	nm	15
T_{AlGaN}	nm	23

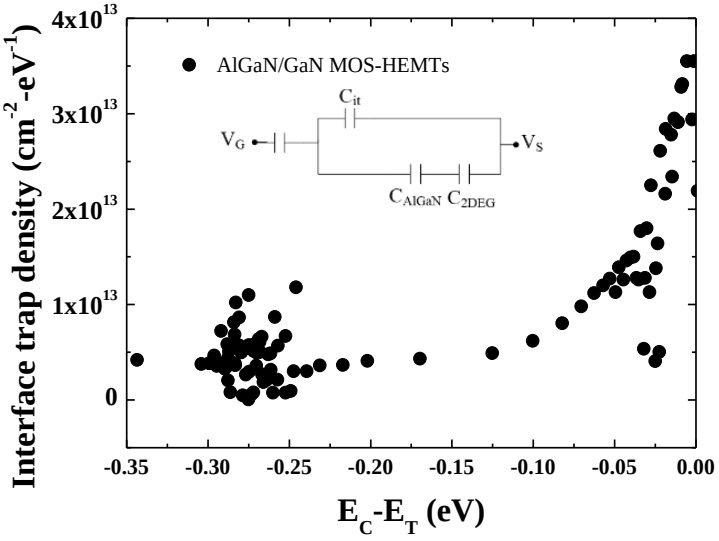


Figure 3-32: Extracted Interface trap density of AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator.

3.6 Summary

In this chapter, high-quality RF-sputtered HfO_2 gate insulator was proposed to obtain high on/off current ratio and high breakdown voltage in the AlGaN/GaN MOS-HEMTs-on-Si substrates. The material and electrical characteristics at various sputtering and post-deposition annealing process were studied. The AlGaN/GaN MOS-HEMT with RF-sputtered HfO_2 showed excellent blocking characteristics compared to the conventional AlGaN/GaN HEMT. I achieved the high breakdown voltage of 1524 V and high on/off current ratio of 2.37×10^{10}. These values for the conventional HEMT were 470 V and 7.6×10^{3}, respectively. Also, I evaluated the blocking characteristics and passivation effects of RF-sputtered HfO_2 on the AlGaN/GaN MOS-HEMTs by measuring various electrical properties. The MOS-HEMT with HfO_2 gate insulator showed gate leakage current of −67 pA/mm at V_{GS}= −10 V and V_{DS}= 100 V and drain leakage current was not considerably altered for 100 s. However, the conventional HEMT without any gate insulator had gate leakage current of −44.7 μA/mm and drain leakage current was increased from 57.5 to 496 μA/mm after 100 s. The sputtered HfO_2 showed weak crystallinity in XRD results. This indicates that HfO_2 is suitable for use as gate insulator of the high-voltage AlGaN/GaN MOS-HEMTs.

Chapter 4

4. TaN-Based Electrodes for Au-Free AlGaN/GaN MOS-HEMTs

4.1. Overview

Recently, AlGaN/GaN high-electron-mobility transistors (HEMTs) have proven their real worth as next-generation power devices due to the excellent material properties. With the successful growth of GaN-on-Si, despite the large lattice and thermal mismatch, GaN devices have been facing their commercialization in near future [114, 115]. As shown in chapter 1, several groups have released 600 V GaN power devices which are qualified joint electron for devices engineering council (JEDEC) standard.

Although GaN-on-Si device technologies enable reduction of fabrication

cost due to cheap and large-sized Si substrate, the cost-related problems have been still critical. Among the various fabrication steps, formation of electrodes including Au costs great expense to implement for the AlGaN/GaN HEMTs. It is well known that thick source and drain electrodes are necessary to reduce series resistance for high-current devices [116]. The collected electrons from drain suffer series resistance in omic metal even wire bonding using Al or Au is used to reduce current crowding. A few μm-thick source and drain were reported for high-current operation as shown in Fig. 4-1 [117]. I described the series resistance in each electrode of the AlGaN/GaN HEMTs for understanding importance of electrode thickness.

When Au-based electrodes are employed for the AlGaN/GaN HEMTs, another problem occurs in terms of compatibility with various fabrication equipments such as chemical vapor deposition (CVD) and etcher in the CMOS fabs. Au is not allowed in Si fabrication due to contamination issue. Therefore, the development of CMOS-compatible metals stack excluding Au in the GaN devices is a key issue to compete with Si-based power devices [118]. Also, Au-free technologies are very useful for fabless companies because they can use a foundry service for GaN devices.

In this chapter, I propose RF-sputtered TaN-based electrodes for the Au-free AlGaN/GaN MOS-HEMTs. TaN-sputtering conditions such as sputtering power and working pressure are optimized to be implemented into the AlGaN/GaN MOS-HEMTs. The effects of thermal annealing for ohmic contact formation on the electrical and material properties of RF-sputtered TaN films are studied. In the end of this chapter, I propose and investigate an extended TaN-gate structure in the AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator for low on-resistance. This devices have high figure-of-merit (FOM) of 872 MW·cm^{-2} and low specific on-resistance ($R_{on,sp}$) of 2.28 mΩ·cm^{-2} by the effectively reduced drain-source distance due to the extended TaN-gate structure and HfO_2 gate insulator.

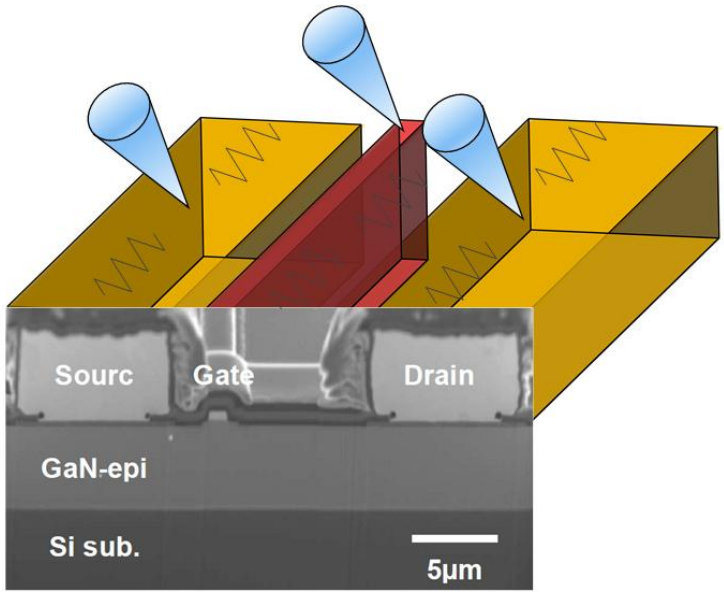


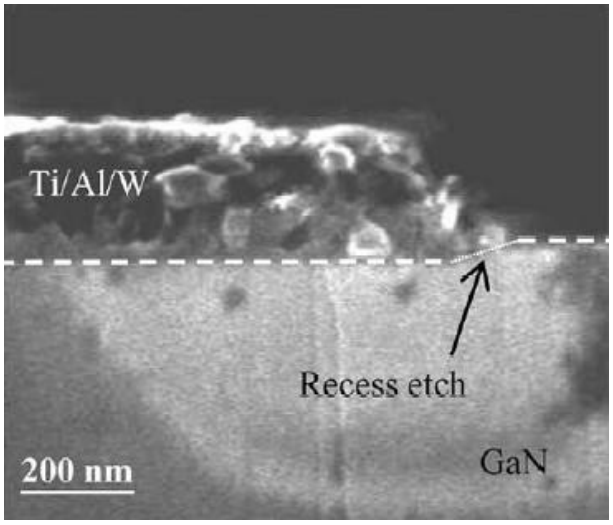
Figure 4-1: Cross-sectional SEM image of AlGaN/GaN HEMT for high-current operation [117].

4.2. Reported Technologies for Au-Free Fabrication

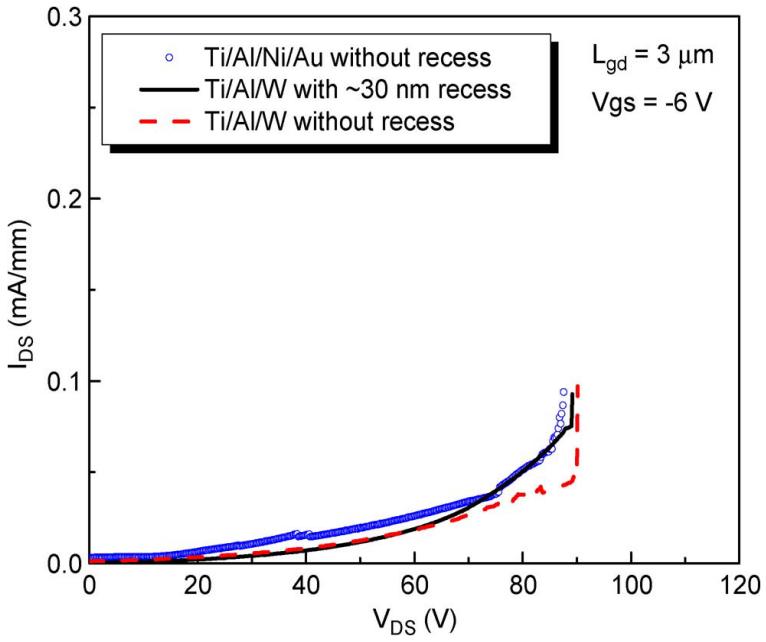
For development of the GaN power devices, various Au-free technologies have been studied for CMOS-compatible fabrication by a few groups. Among the alternative metals for Au-free fabrication, tungsten (W) has been firstly used for the AlGaN/GaN HEMTs [119]. W-based electrodes make high-temperature process possible after formation of metallic electrodes due to its excellent thermal blocking and stability characteristics. Based on these properties, gate-first process was reported using W-gate for the AlGaN/GaN MOS-HEMTs as shown in Fig. 4-2 [120]. However, considerably high resistivity of W is the biggest problem to be adopted to electrodes in the high-current AlGaN/GaN MOS-HEMTs. In addition, considerable heat is produced during W deposition by e-beam evaporation so that life-off process using negative photo resistor may be difficult.

Copper (Cu) has attracted considerable attention due to its low-material cost and low resistance [121]. Also, Cu has been widely used for interconnection metal in CMOS fabs. Recently, IMEC has demonstrated 8-inch AlGaN/GaN HEMT-on-Si substrate using Cu-based electrodes as shown in Fig. 4-3 [19]. This device using 60 mm-long gate exhibited maximum drain current of 6 A with normally-off operation. However, it is well known that Cu doesn't have suitable etchant due to non-volatile properties of the Cu-radical compound. Thus, Cu process requires chemical mechanical polishing (CMP) process for its patterning and planarization. In addition, Cu-diffusion into semiconductor material during high-temperature process is concerned about traps-related problems.

Tantalum nitride (TaN) is promising material for alternative electrode of Au due to its excellent material properties such as low resistance and highly thermal stability. TaN has been widely used for thermal barrier of Cu-gate in CMOS process [122]. Quite recently, TaN has been reported as gate electrode in the AlGaN/GaN MOS-HEMT using atomic-layer-deposition (ALD)-Al_2O_3 gate insulator [123] as shown in Fig. 4-4. The large work function of TaN (4.5~4.5 eV) has been established for gate electrodes materials [124].



(a)



(b)

Figure 4-2: Au-free AlGaN/GaN HEMT using recessed ohmic structure and Ti/Al/W electrode (a) cross-sectional SEM image (b) breakdown voltage characteristics [120].

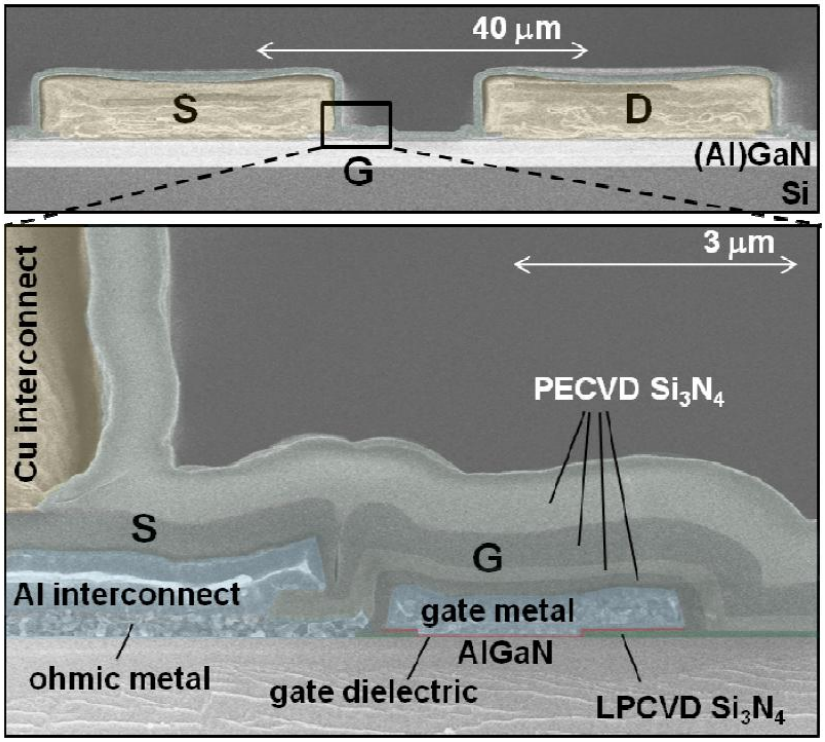
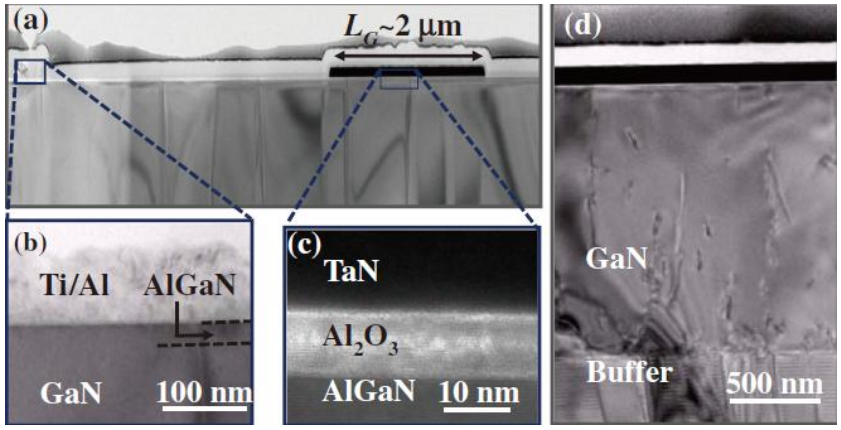
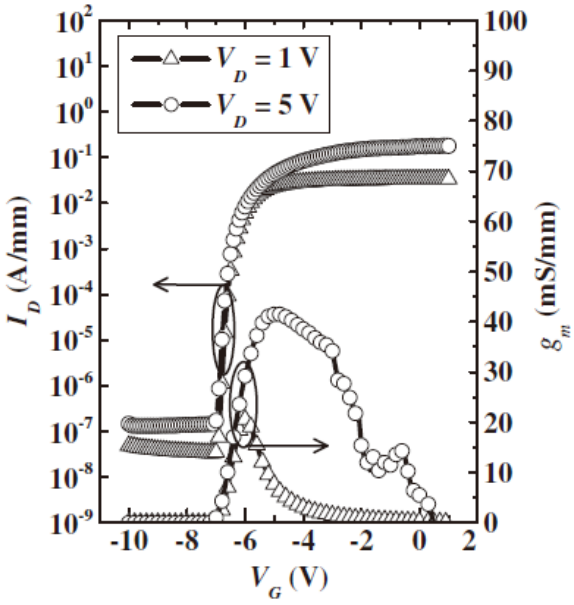


Figure 4-3: Cross-sectional SEM image of Au-free AlGaN/GaN transistor using Cu-based electrode [19].



(a)



(b)

Figure 4-4: AlGaN/GaN MOS-HEMT using ALD-Al_2O_3 gate insulator and TaN-gate (a) cross-sectional SEM image (b) Transfer characteristics [124].

4.3. Material Properties of RF-Sputtered TaN

In this section, the material properties of RF-sputtered TaN films with various working pressure are studied. Also, electrical characteristics of TaN films are evaluated to obtain low resistance. TaN was formed by RF-sputtering on p^+ Si substrate (10~15 Ω·cm) at room temperature. The working pressure was varied from 1 to 20 mTorr with sputtering power of 300 W, Ar flow of 20 sccm, and sputtering time of 3000 s. The sheet resistance of RF-sputtered TaN films was examined by 4-point probe.

Figure 4-5 shows thickness and sheet resistance of TaN sputtered at various working pressure. Thickness was measured by surface profiler (Alpha step). Sheet resistance of TaN films is reduced with decreasing working pressure. Low sheet resistance of 10.3 Ω/□ was achieved in the TaN film sputtered at working pressure of 1 mTorr. These results agree well with the resistance-variation of indium tin oxide (ITO) by sputtering method [125]. In this research, the resistance of ITO films was increased with increasing working pressure due to its phase shift.

Next, the resistance-variation of RF-sputtered TaN films after post-deposition annealing (PDA) is investigated. The effects of thermal annealing on electrical characteristics of TaN films should be verified because high-temperature annealing may affect contact resistance and on-resistance in the AlGaN/GaN devices. High-temperature annealing over 800 ^oC is required to form ohmic contact when Ti/Al-based metal stack is used. Locally formed TiN under source and drain by thermal annealing produces nitrogen vacancies which act as donor states. When Ti/Al/TaN-ohmic contact is used for source and drain, TaN should sustain high-annealing temperature. As shown in Fig. 4-6, sheet resistance of TaN sputtered at 1 mTorr is rather increased after PDA.

Sheet resistance of TaN films after PDA at the 980 ^{o}C is increased from 10.3 to 18.9 Ω/□. The 880 ^{o}C was used for Ti/Al/Ni/Au-ohmic contact of the conventional AlGaN/GaN HEMTs and the MOS-HEMTs used in the dissertation. The increase of sheet resistance is caused by shift of maximum-peak location from 34.7^{o} to 35.9^{o} as shown in Fig. 4-7. It means that hexagonal structure including TaN (110) and Ta_2N (002) bonding is shifted to cubic structure including TaN bonding (002), which is centered at 35.9^{o} after PDA. Surface scanning electron microscopy (SEM) image in Fig. 4-8 shows the increased morphology as well as dense surface after PDA. Tens of grain size of RF-sputtered TaN films after PDA at 980 ^{o}C was observed.

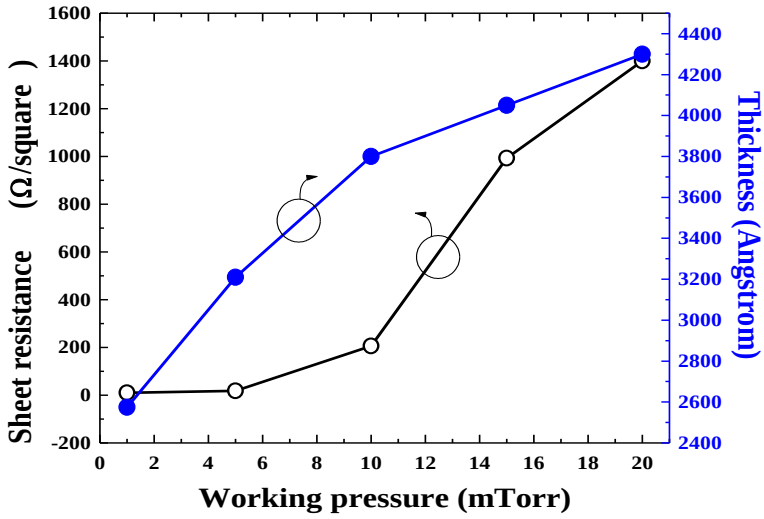


Figure 4-5: Sheet resistance and thickness of RF-sputtered TaN film according to working pressure.

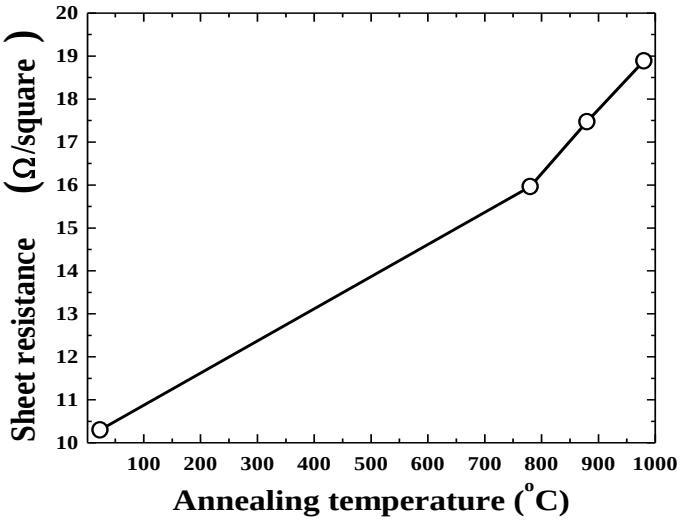


Figure 4-6: Sheet resistance of RF-sputtered TaN before and after PDA at various temperatures.

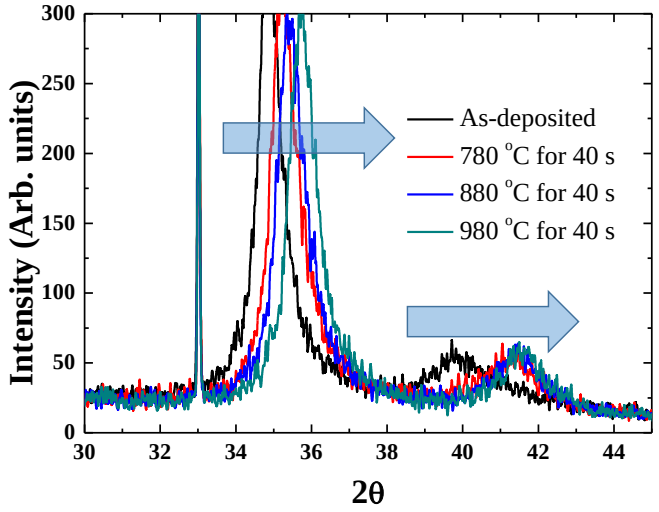
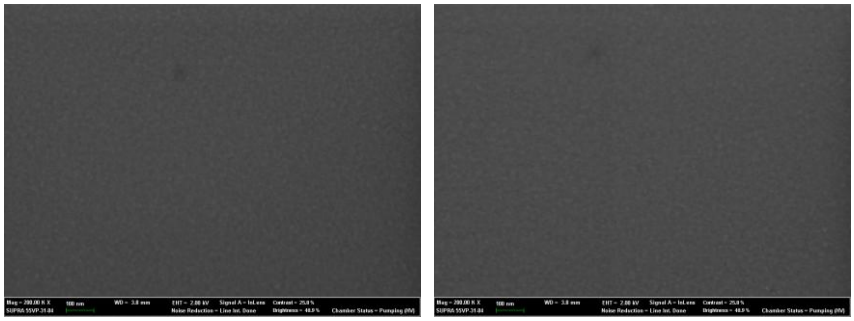
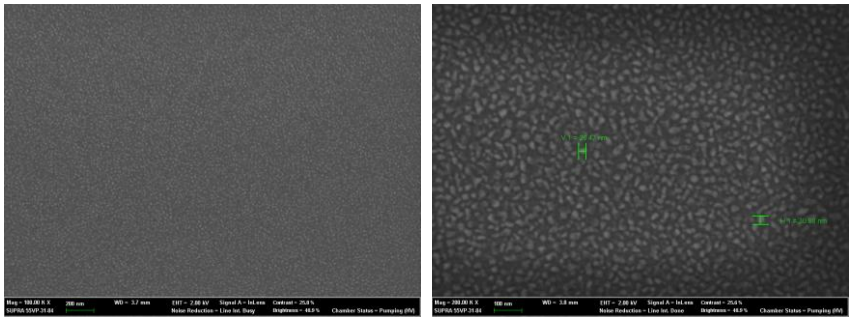


Figure 4-7: XRD results of RF-sputtered TaN before and after PDA at various temperatures.



(a) (b)



(c) (d)

Figure 4-8: Surface SEM image of RF-sputtered TaN films before and after PDA at various temperatures (a) as-deposited (b) annealing at 780 ^{o}C for 40 s (c) 880 ^{o}C for 40 s (d) 980 ^{o}C for 40 s

4.4. Electrical Properties of AlGaN/GaN MOS-HEMTs Employing TaN-Gate

In this section, electrical characteristics of the AlGaN/GaN MOS-HEMTs using RF-sputtered TaN-gate are studied to examine channel controllability by TaN-gate instead of Ni/Au-gate. Schematic cross-sectional view of the AlGaN/GaN MOS-HEMTs-on-Si (111) substrate using RF-sputtered TaN-gate is shown in Fig. 4-9. The MOCVD-grown epitaxial layers consist of 3 nm-thick GaN cap/20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier/1 nm-thick AlN spacer/100 nm-thick i-GaN/3.9 μm-thick C-doped GaN buffer. The 270-deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) was deposited for source/drain by using e-gun evaporator and lift-off. This was annealed at 880 ^{o}C for 40 s to form ohmic contact. Prior to HfO_2 sputtering, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, 15 nm-thick HfO_2 was sputtered at 3 mTorr and 50 W with Ar flow of 15 sccm at room temperature. And finally, 43 nm-thick TaN-gate was formed on HfO_2 gate insulator by RF-sputtering and lift-off technique. Ar flow of 15 sccm and working pressure of 1 mTorr were used for TaN sputtering without substrate heating. Sputtering power was varied from 50 to 350 W. The gate length, gate–source distance, gate–drain distance, and gate width were 3, 3, 10, and 50 μm, respectively.

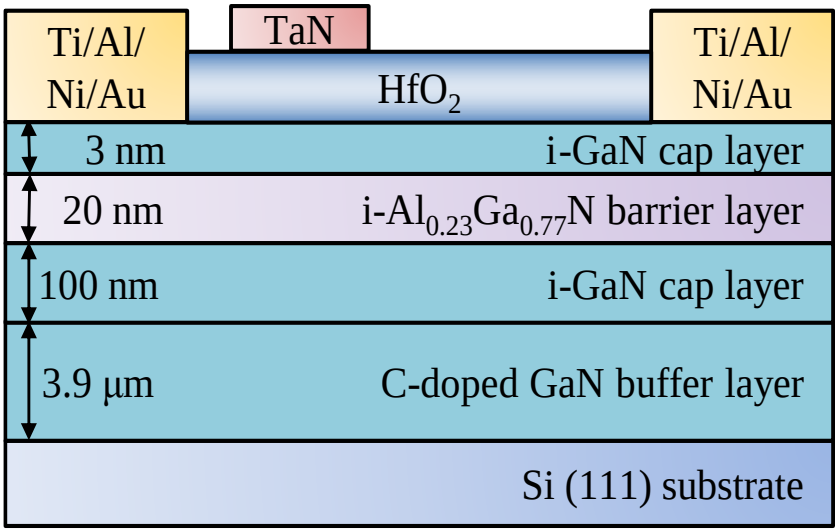


Figure 4-9: Cross-sectional view of fabricated AlGaN/GaN MOS-HEMTs using TaN-gate.

4.4.1 Switching Characteristics

Figure 4-10 shows transfer characteristics of the AlGaN/GaN HEMTs using Ni/Au-gate and TaN-gate, MOS-HEMT using TaN-gate at V_{DS} of 10 V. Sputtering power of 350 W was used for TaN-formation. V_{TH} was determined by constant current method at drain current of 1 mA/mm. The AlGaN/GaN HEMT using TaN-gate shows relatively high V_{TH} of –1.2 V compared to that using Ni/Au-gate (–2.4 V) due to low work-function of RF-sputtered TaN. As discussed in above results, the AlGaN/GaN HEMT using TaN-gate sputtered at 350 W shows high drain leakage current so that the device has low on/off current ratio of 5.23×10^2 when V_{GS}= 2 V and $I_{D,OFF}$ when V_{GS}= −8 V while that of the HEMT using Ni/Au-gate shows 2.1×10^4. The AlGaN/GaN MOS-HEMT using TaN-gate exhibits relatively high V_{TH} of –1.9 V due to sputtering damage to HfO_2 gate insulator and leakage current. Also, this MOS-HEMT has low on/off current ratio of 1.49×10^4 because of degradation of on-current by sputtering damage during TaN-gate formation.

As shown in Fig. 4-11, very high on/off current of 8.86×10^{10} was achieved in the AlGaN/GaN MOS-HEMT using TaN-gate and HfO_2 gate insulator with low sputtering power of 50 W. Thus, it is explained that low sputtering power is helpful to improve reverse blocking characteristics by suppressing sputtering damage to HfO_2 gate insulator. In addition, dissipation of forward current is suppressed by successfully blocked gate-drain and gate-source diodes current. These transfer characteristics of the MOS-HEMT using TaN-gate sputtered at low sputtering power reveals RF-sputtered TaN-gate is promising and suitable material as an alternative gate for the Au-free AlGaN/GaN devices.

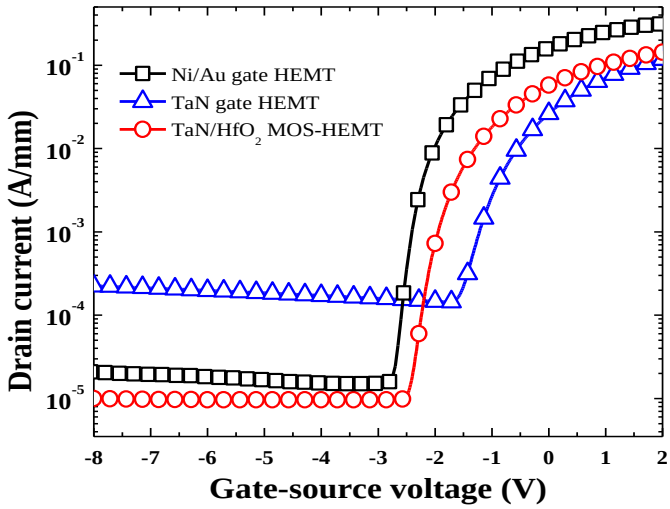
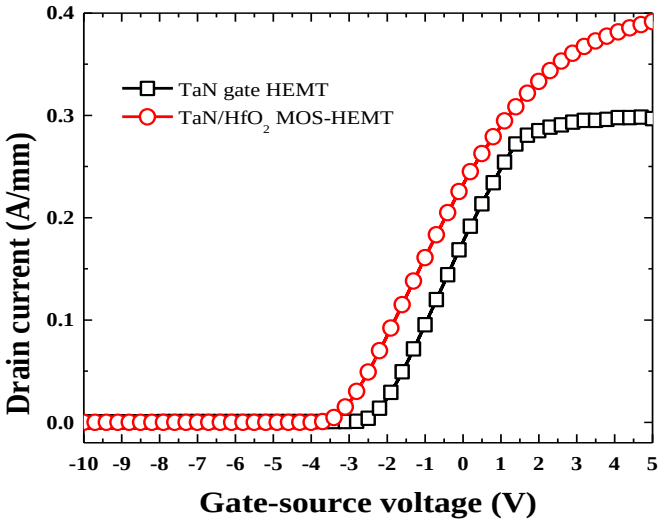
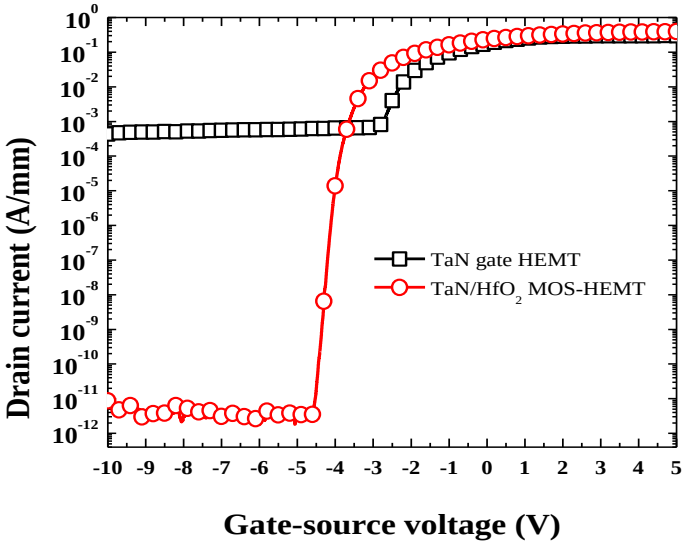


Figure 4-10: Transfer characteristics of AlGaN/GaN HEMT and MOS-HEMTs using TaN-gate sputtered at 350 W.



(a)



(b)

Figure 4-11: Transfer characteristics of AlGaN/GaN HEMT and MOS-HEMT using TaN-gate sputtered at 50 W (a) linear scale (b) log scale.

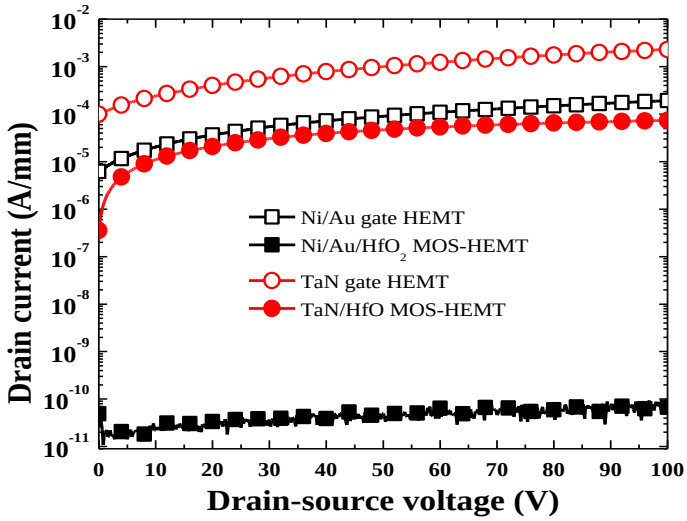
4.4.2 Reverse Blocking Characteristics

Here, reverse blocking characteristics of the AlGaN/GaN MOS-HEMTs using TaN-gate are discussed. Firstly, the effects of TaN-sputtering power on the electrical properties of the MOS-HEMTs are investigated. I compared four-different devices including the AlGaN/GaN HEMTs using Ni/Au-gate and TaN-gate, MOS-HEMTs using Ni/Au-gate and TaN-gate. The drain and gate leakage current at V_{GS} of –10 V are shown in Fig. 4-12. In this experiment, 43 nm-thick TaN was sputtered at high-sputtering power of 350 W. As I stated in chapter 3, leakage current of the AlGaN/GaN MOS-HEMT using Ni/Au-gate was dramatically decreased by HfO_2 gate insulator. The AlGaN/GaN HEMT using TaN-gate without any gate insulator shows relatively high drain leakage current of 2.29 mA/mm and gate leakage current of –2.37 mA/mm compared to the device using Ni/Au-gate at V_{DS} of 100 V. These results are explained by two factors. First one is low Schottky barrier height (Φ_{BN}) of TaN/GaN interface compared with that of Ni/GaN interface. Low Φ_{BN} causes higher probability of electron-transfer from gate to the GaN surface. Second one is considerable sputtering damage to HfO_2 gate insulator during TaN-gate formation with high-sputtering power of 350 W. Higher gate leakage current than drain leakage current reveals the HfO_2 gate insulator is physically broken by TaN-sputtering at high power.

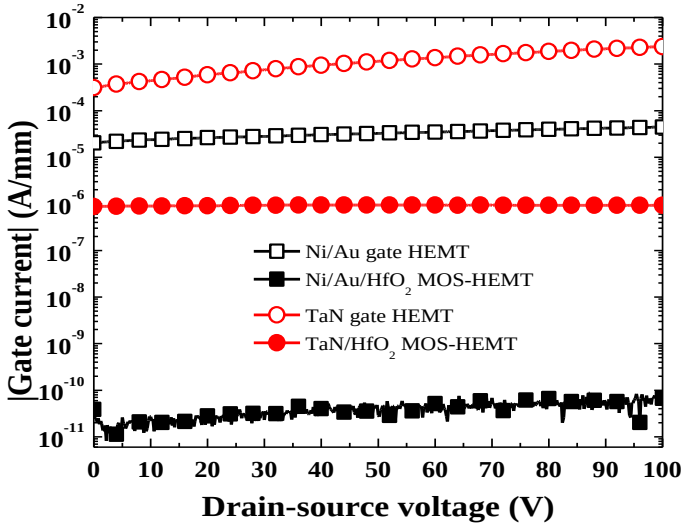
Figure 4-13 shows drain and gate leakage current of the AlGaN/GaN HEMTs using Ni/Au-gate and TaN-gate, MOS-HEMT using TaN-gate. TaN was sputtered at low sputtering power of 50 W considering damage to HfO_2 gate insulator. The AlGaN/GaN MOS-HEMT using TaN-gate sputtered at 50 W exhibits considerably low drain leakage current of 17.4 pA/mm and gate leakage current of –8.3 pA/mm at V_{GS} of –10 V and V_{DS} of 100 V. It means that

sputtering power during TaN-gate formation should be minimized to improve reverse blocking characteristics.

Breakdown voltage of the AlGaN/GaN HEMT and MOS-HEMT using TaN-gate sputtered at 50 W and 10 μm-long L_{GD} at V_{GS} of –4 V is shown in Fig. 4-14. It has been demonstrated that the breakdown voltage was measured at the drain leakage current of 1 mA/mm. High breakdown voltage of 1460 V was achieved by RF-sputtered HfO_2 gate insulator and low sputtering power of 50 W for TaN-gate formation in the AlGaN/GaN MOS-HEMT using TaN-gate while HEMT without gate insulator shows considerably low value of 120 V due to its leaky characteristics.

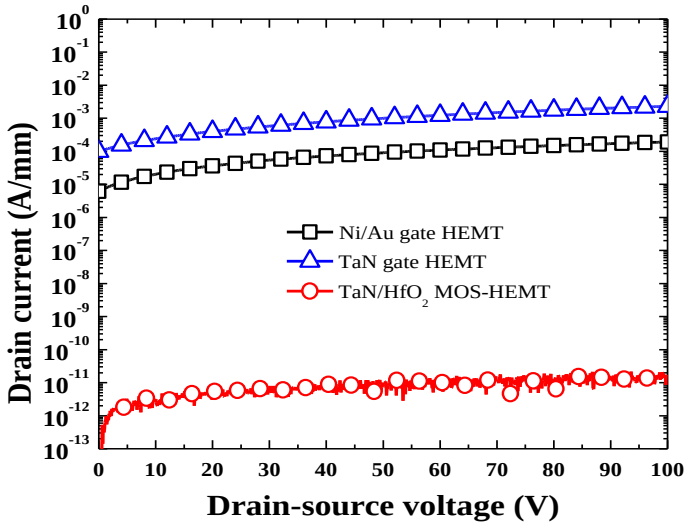


(a)

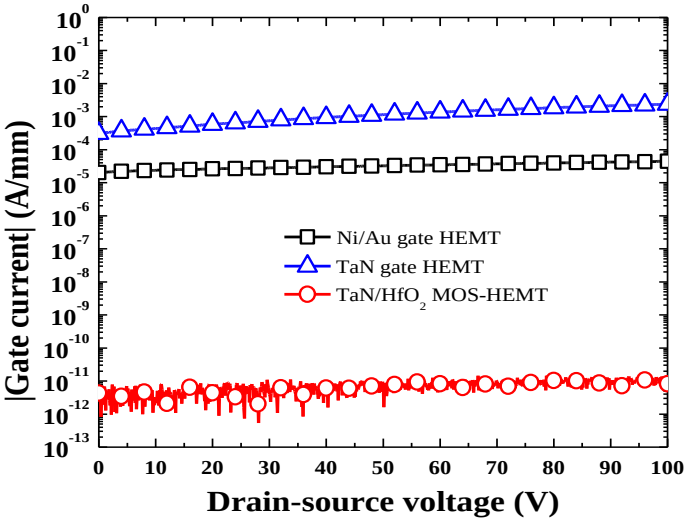


(b)

Figure 4-12: (a) Drain leakage current of AlGaN/GaN HEMTs and MOS-HEMT using Ni/Au- and TaN-gate sputtered at 350 W (b) gate leakage current.



(a)



(b)

Figure 4-13: (a) Drain leakage current of the AlGaN/GaN HEMTs and MOS-HEMT using Ni/Au- and TaN-gate sputtered at 50 W (b) gate leakage current.

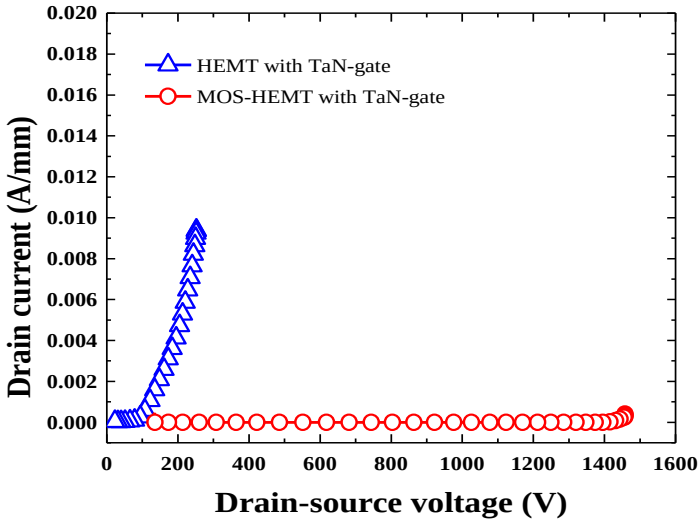


Figure 4-14: Breakdown voltage of AlGaN/GaN HEMT and MOS-HEMT using TaN-gate sputtered at 50 W.

4.5 Electrical Properties of AlGaN/GaN MOS-HEMTs Employing TaN-Gate and Ti/Al/TaN-Source/Drain

In this section, I describe electrical characteristics of the fully Au-free AlGaN/GaN MOS-HEMTs using TaN-based electrodes. Ti/Al/TaN (20/80/100 nm) and TaN (43 nm) were used for source/drain and gate, respectively. Schematic cross-sectional view of the AlGaN/GaN MOS-HEMTs-on-Si (111) substrate using RF-sputtered TaN-gate and Ti/Al/TaN-source/drain is shown in Fig. 4-15. The MOCVD-grown epitaxial layers consist of 3 nm-thick GaN cap/20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier/1 nm-thick AlN spacer/100 nm-thick i-GaN/3.9 μm-thick C-doped GaN buffer. The 270-deep mesa was formed for device-to-device isolation. Ti/Al (20/80 nm) was deposited by e-gun evaporator and 100 nm-thick TaN was sputtered at 350 W. Ar flow of 15 sccm and working pressure of 1 mTorr were used for TaN sputtering without substrate heating. This was annealed at various temperatures from 780 to 980 ^{o}C for 40 s to form ohmic contact. Prior to HfO_2 sputtering, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, 15 nm-thick HfO_2 was sputtered at 3 mTorr and 50 W with Ar flow of 15 sccm at room temperature. And finally, 43 nm-thick TaN-gate was formed on HfO_2 gate insulator by RF-sputtering with sputtering power of 50 W. Ar flow of 15 sccm and working pressure of 1 mTorr were used for TaN sputtering. The AlGaN/GaN MOS-HEMT using Ti/Al/Ni/Au-source/drain (20/80/20/100 nm) and Ni/Au-gate (30/150 nm) was fabricated for comparison purpose. Gate length, gate–source distance, gate–drain distance, and gate width were 3, 3, 10, and 50 μm, respectively.

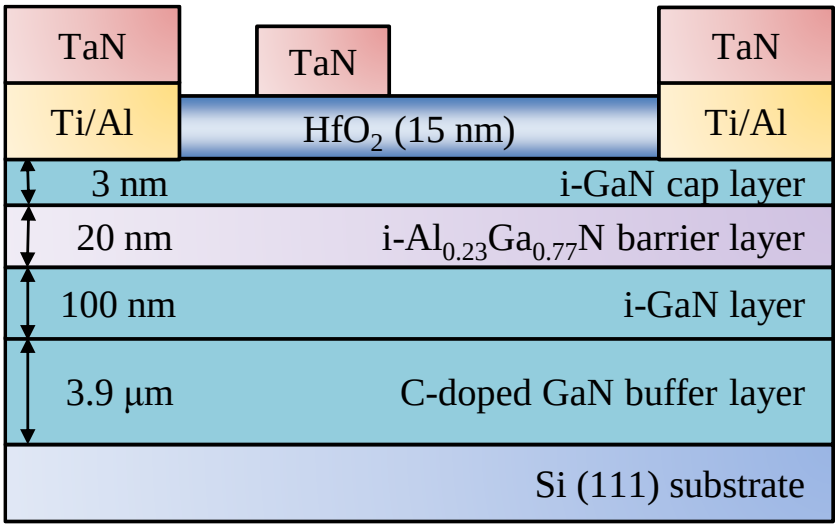


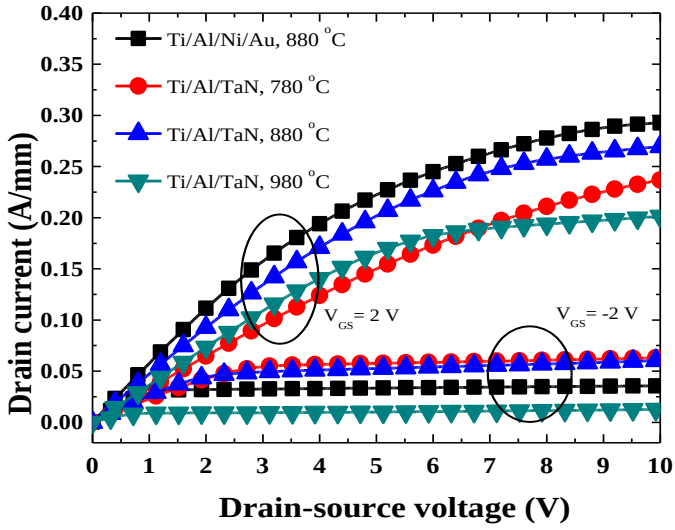
Figure 4-15: Cross-sectional view of fabricated AlGaN/GaN MOS-HEMTs using TaN-gate and Ti/Al/TaN-source/drain.

4.5.1. Switching Characteristics

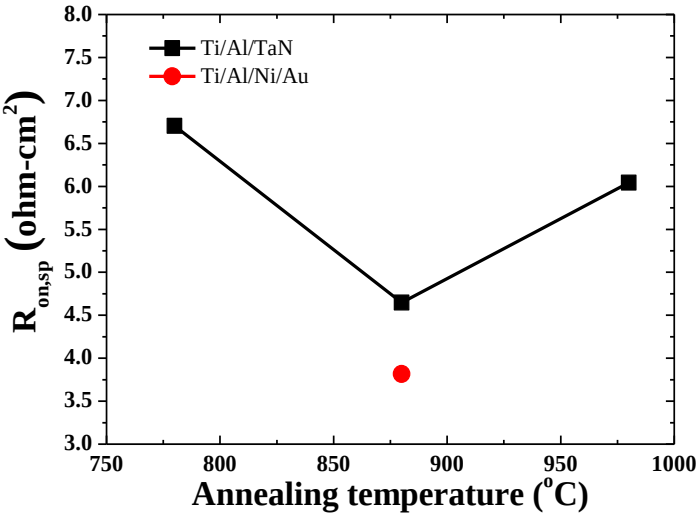
Figure 4-16 shows output *I-V* characteristics and specific on-resistance ($R_{on,sp}$) of the AlGaN/GaN MOS-HEMT using Ti/Al/Ni/Au-source/drain and Ni/Au-gate, the MOS-HEMTs using Ti/Al/TaN-source/drain with various annealing temperatures. Drain current of the devices using Ti/Al/TaN-source/drain are less than that using Ti/Al/Ni/Au-source/drain because of the relatively high resistivity of RF-sputtered TaN films compared to Au. The highest drain current of 270 mA/mm measured at V_{GS} of 2 V and V_{DS} of 10 V in the device annealed at 880 ^{o}C was obtained among the devices using various annealing temperatures while that with Ti/Al/Ni/Au-source/drain showed 293 mA/mm. The effects of thermal-annealing temperature on $R_{on,sp}$ of the AlGaN/GaN MOS-HEMTs using Ti/Al/TaN-source/drain can be divided into two tendencies. As shown in section 5.3, sheet resistance of RF-sputtered TaN films is increased with increasing PDA temperature due to their phase shift by annealing. Another contribution to $R_{on,sp}$ is that regarding contact resistance variation of ohmic contact according to annealing temperature. It is well known that enough annealing temperature is required to obtain low contact resistance in the AlGaN/GaN HEMTs. High annealing temperature provides sufficient nitrogen vacancy concentration under source/drain electrodes by forming TiN region. Arising from these two-tendencies for on-resistance of the AlGaN/GaN MOS-HEMTs using Ti/Al/TaN-source/drain, I conclude that annealing temperature of 880 ^{o}C is optimum point to obtain high-performance Au-free AlGaN/GaN MOS-HEMT using Ti/Al/TaN-source/drain.

In Fig. 4-17, transfer characteristics of the following devices; (1) AlGaN/GaN HEMT using Ni/Au-gate and Ti/Al/Ni/Au-source/drain, (2) MOS-HEMT using Ni/Au-gate and Ti/Al/Ni/Au-source/drain, (3) MOS-HEMT using

TaN-gate and Ti/Al/Ni/Au-source/drain, (4) MOS-HEMT using TaN-gate and Ti/Al/TaN-source/drain. Annealing was performed at 880 ^{o}C for 40 s under N_2 ambient for all devices. The device structures are summarized at inset table in Fig. 4-17. Transfer characteristics of the Au-free AlGaN/GaN MOS-HEMT using TaN-gate and Ti/Al/TaN-source/drain shows almost identical current values with that using Ti/Al/Ni/Au-source/drain. The MOS-HEMTs using TaN-gate show relatively high V_{TH} of –3.6 V compared to Ni/Au-gate devices due to the low work function of RF-sputtered TaN films compared to e-gun evaporated Ni.



(a)



(b)

Figure 4-16: Output *I-V* characteristics of AlGaN/GaN MOS-HEMTs using Ti/Al/Ni/Au- and Ti/Al/TaN-source/drain annealed at various temperatures.

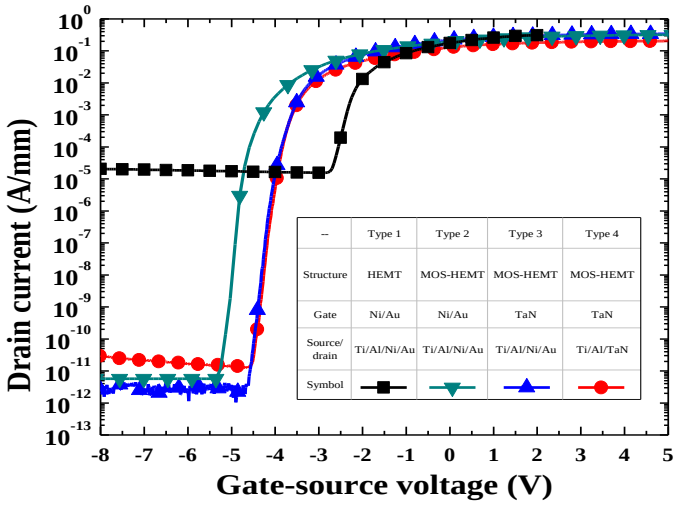
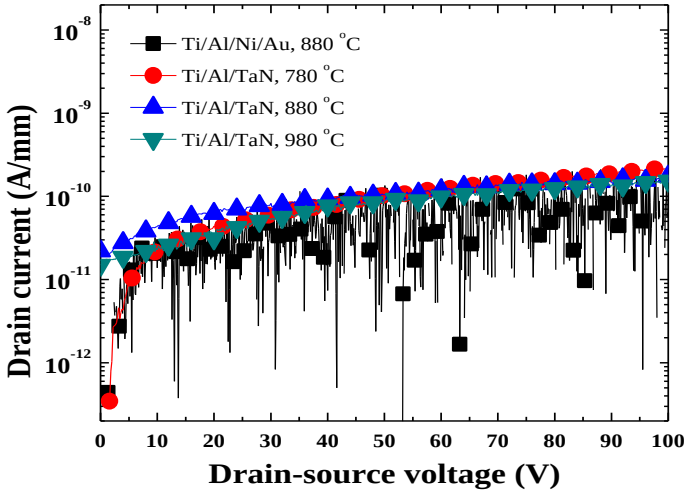


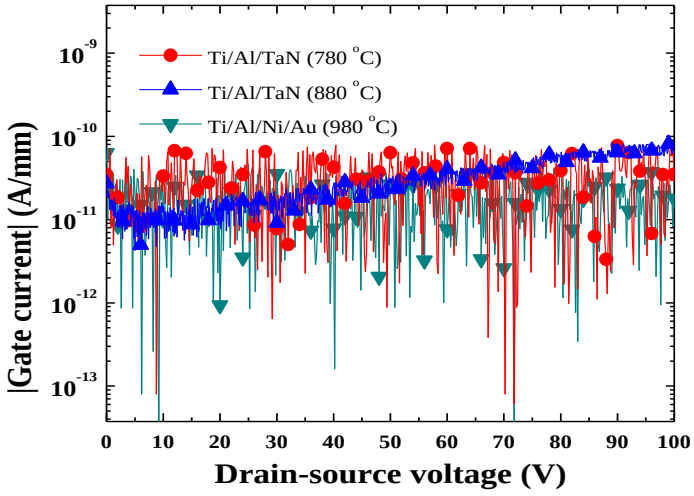
Figure 4-17: Transfer characteristics of AlGaN/GaN HEMT and MOS-HEMTs using Ti/Ai/Ni/Au- and Ti/Al/TaN-source/drain annealed at 880 ^{o}C.

4.5.2. Reverse Blocking Characteristics

Drain and gate leakage current of the Au-free AlGaN/GaN MOS-HEMTs using TaN-gate and Ti/Al/TaN-source/drain measured at V_{GS} of –10 V is shown in Fig. 4-18. The Au-free devices exhibit no significant degradation of reverse blocking characteristics compared to that using Ni/Au-gate and Ti/Al/Ni/Au-source/drain. Au-free MOS-HEMTs using Ti/Al/TaN-source/drain have hundreds level-drain and gate leakage current while that using Ti/Al/Ni/Au-source/drain exhibits tens-level leakage current. Also, considerable effects of annealing temperature on gate and drain leakage current are not shown.



(a)



(b)

Figure 4-18: (a) Drain leakage current of AlGaN/GaN MOS-HEMTs using Ti/Al/Ni/Au- and Ti/Al/TaN-source/drain annealed at various temperatures (b) gate leakage current.

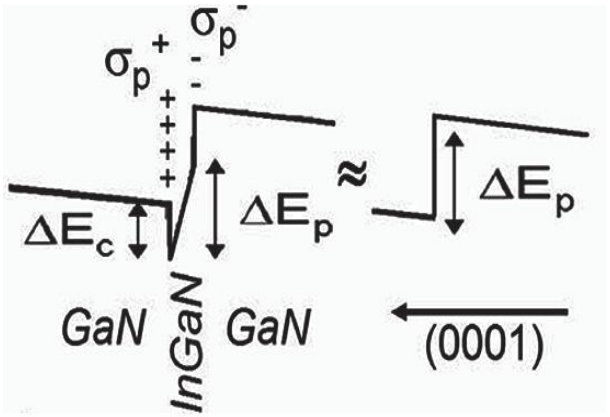
4.6. Electrical Properties of AlGaN/GaN MOS-HEMTs Employing Extended TaN-Gate Structure

I proposed and evaluated electrical properties of the Au-free AlGaN/GaN MOS-HEMTs using RF-sputtered TaN electrodes in above section. In this section, I propose new TaN-gate structure in the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator based on the results in section 5.5. The TaN-gate overlapped source with 15 nm-thick HfO_2 insulation. This extended gate structure reduces effective drain-source distance without any change of gate-drain distance by eliminating gate-source space. The $R_{on,sp}$ improvement by this new structure is investigated in this section.

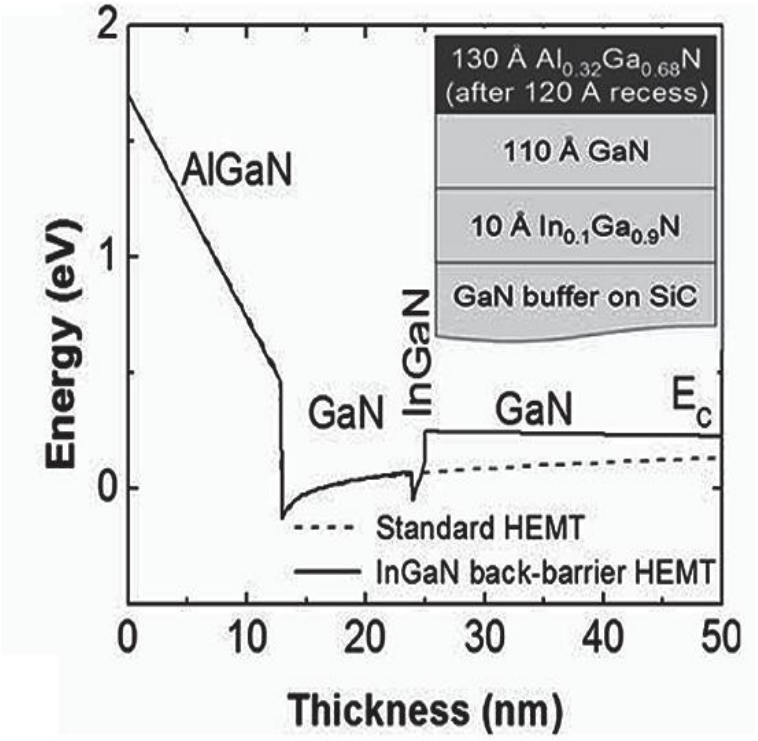
4.6.1. Reported Technologies for a Low On-Resistance

On-resistance is most important index to decide maximum current capability and switching speed in power devices. Most devices have trade-off relationship between on-resistance and breakdown voltage as described in chapter 1. Due to low on-resistance characteristics of the AlGaN/GaN heterostructure-based devices by piezoelectric polarization and two-dimensional electron gas (2DEG) channel, the AlGaN/GaN HEMTs have received considerable attention for next-generation power devices. To obtain more high-current density, many groups have investigated new technologies.

Almost the whole technologies reported previously have focused on GaN epitaxial growth [55, 126, 127]. InGaN-barrier insertion under thin GaN buffer layer increases electron carrier concentration and mobility in 2DEG channel [126]. InGaN-barrier improves carrier confirmation by additional quantum-well formation at the GaN/InGaN hetero-interface as shown in Fig. 4-19. Also, additional GaN back-barrier formed by InGaN insertion suppresses electron overflow from 2DEG channel to high-resistive GaN buffer region. Recently, AlGaN back-barrier has been also reported to improve carrier confirmation and increase breakdown voltage [55]. In addition, double heterostructure AlGaN/GaN HEMTs using AlN-forward barrier instead of AlGaN barrier was reported. Al mole-fraction in AlGaN barrier is dominant factor to decide piezoelectric polarization and sheet charge density. AlN front-barrier provides higher electron concentration than AlGaN by strong piezoelectric polarization and large conduction-band discontinuity between AlN front-barrier and GaN buffer layer (Fig. 4-20) [127].



(a)



(b)

Figure 4-19: (a) Effect of insertion of InGaN in GaN buffer layer (b) band diagram of the InGaN back-barrier [126].

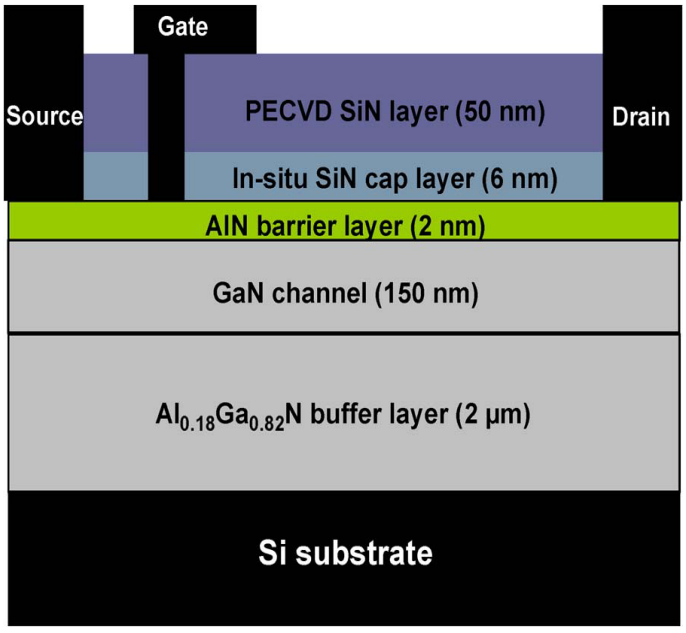


Figure 4-20: Schematic cross section of fabricated AlN/GaN/AlGaN DHFETs [127].

4.6.2. Device Structure and Requirement for Stable Operation

In this section, structure and operation mechanism of the proposed AlGaN/GaN MOS-HEMTs using extended TaN-gate structure are explained. Same fabrication procedure and epitaxial structure are used for the AlGaN/GaN MOS-HEMTs using extended TaN-gate as the experiment in above section. Schematic cross-sectional view of the AlGaN/GaN MOS-HEMTs-on-Si (111) substrate using extended TaN-gate is shown in Fig. 4-21 [128] . The MOCVD-grown epitaxial layers consist of 3 nm-thick GaN cap/20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier/1 nm-thick AlN spacer/100 nm-thick i-GaN/3.9 μm-thick C-doped GaN buffer. The 270-deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) was deposited for source/drain by using e-gun evaporator and lift-off. This was annealed at 880 ^{o}C for 40 s to form ohmic contact. Prior to HfO_2 sputtering, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, 15 nm-thick HfO_2 was sputtered at 3 mTorr and 50 W with Ar flow of 15 sccm at room temperature. And finally, 43 nm-thick TaN-gate was formed on HfO_2 gate insulator by RF-sputtering and lift-off technique. Ar flow of 15 sccm, working pressure of 1 mTorr, and sputtering power of 50 W were used for TaN sputtering without any substrate heating. The gate length, gate–drain distance, and gate width were 3, 10, and 50 μm, respectively. The 2 μm-long extended gate overlapped source with HfO_2 insulation so that gate-source space was eliminated by this structure.

For stable operation in this structure, high dielectric breakdown field is the most important. In case of the conventional AlGaN/GaN HEMTs, series resistance between gate insulator and depletion region sustain negative gate bias less than V_{TH} to be turned off while only gate insulator sustain positive

gate bias during on-state. In case of the proposed devices using extended gate structure, however, only gate insulator should sustain both positive and negative gate bias due to metal-oxide-metal (TaN-HfO_2-Ti/Al/Ni/Au) structure. Therefore, higher dielectric breakdown voltage of gate insulator than $|V_{TH}|$ is required. Thick gate insulator causes shift of V_{TH} in negative direction so that high dielectric breakdown field is needed. The relationship between thickness of gate insulator and V_{TH} as well as dielectric breakdown voltage is shown in Fig. 4-22.

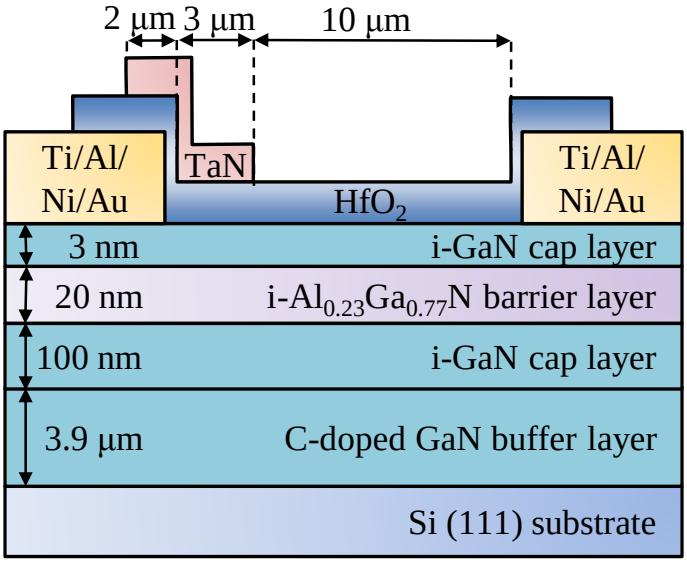


Figure 4-21: Schematic of AlGaN/GaN MOS-HEMT using extended TaN-gate structure [128].

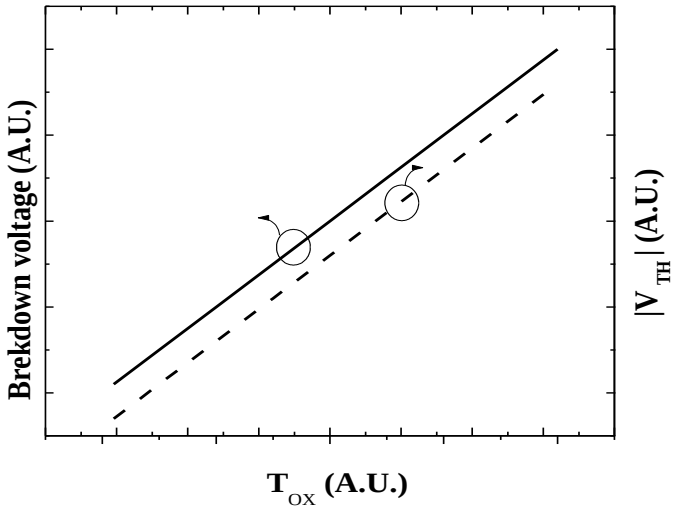
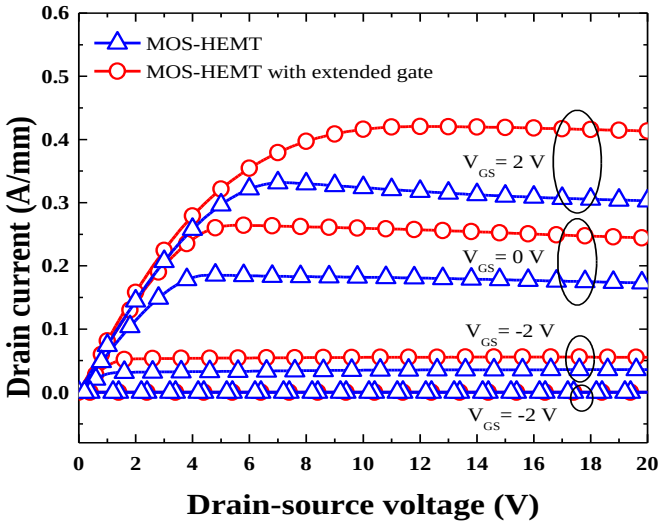


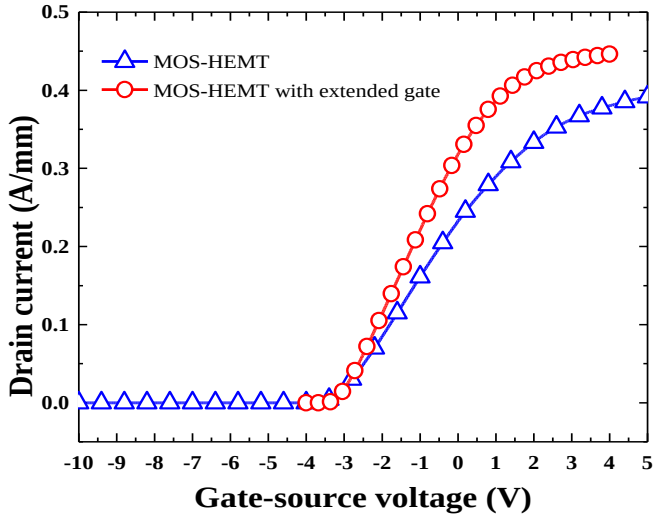
Figure 4-22: Thickness of gate insulator versus dielectric breakdown voltage and V_{TH}.

4.6.3. Forward characteristics

Output *I-V* and transfer characteristics of the conventional AlGaN/GaN MOS-HEMT and the device using extended gate structure are shown in Fig. 4-23. In output *I-V* characteristics, V_{GS} was swept from 2 to –6 V at –2 V increment. Maximum drain current of the AlGaN/GaN MOS-HEMTs using extended gate is 421 mA/mm at V_{GS} of 2 V while the conventional MOS-HEMT has 332 mA/mm because of the successfully eliminated gate-source space by the extended gate structure. This improvement of drain current leads reduction of on-resistance from 2.91 to 2.28 mΩ·cm^2. On-resistance was extracted at V_{GS} of 2 V and V_{DS} of 1 V. I assumed effective length of source and drain region, which act as current path, are 2.5 μm. As shown in Fig. 4-23(b), however, the proposed AlGaN/GaN MOS-HEMT using the extended gate structure has narrow V_{GS} sweeping range from –4 to 4 V due to MIM structure including source, HfO_2 gate insulator, and gate. When normally-off techniques such as recess gate and F^- ion implantation are used to this structure, the operation point would be moved to above V_{GS} of 0 V. Thus, sufficient reverse V_{GS} can be applied and this device using the extended gate can shows stable blocking characteristics. Increase of drain current by this proposed structure well matches with output *I-V* characteristics. As I showed in Fig. 4-24 and Fig. 4-25, $R_{on,sp}$ was proportionally increased to L_{GD}. The highest reduction rate of $R_{on,sp}$ by the extended gate structure was observed at L_{GD} of 10 μm. It is explained that L_{GS} space has great part in total L_{DS} at the short-L_{GD} devices compared to long-L_{GD} devices. Also, the highest reduction ratio of $R_{on,sp}$ was obtained at short-L_{GD} devices. Thus, I can say with fair certainty that this extended gate is advantageous for high-current AlGaN/GaN MOS-HEMTs with short L_{GD}.



(a)



(b)

Figure 4-23: Forward characteristics of AlGaN/GaN MOS-HEMTs with and without extended gate structure (a) output *I-V* (b) transfer characteristics.

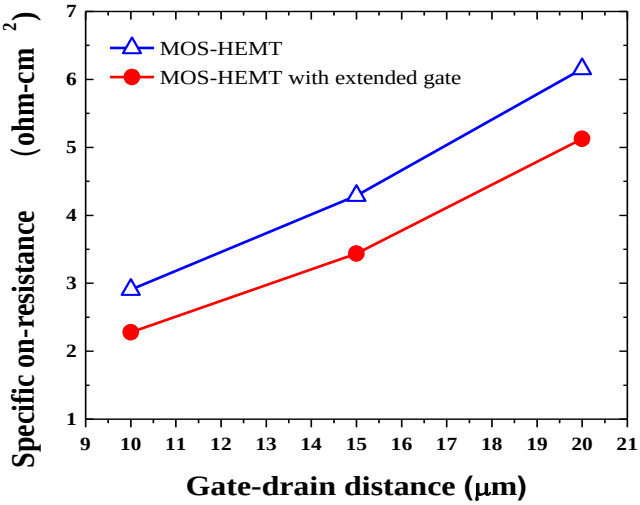


Figure 4-24: L_{GD} versus $R_{on,sp}$ of AlGaN/GaN MOS-HEMTs with and without extended gate.

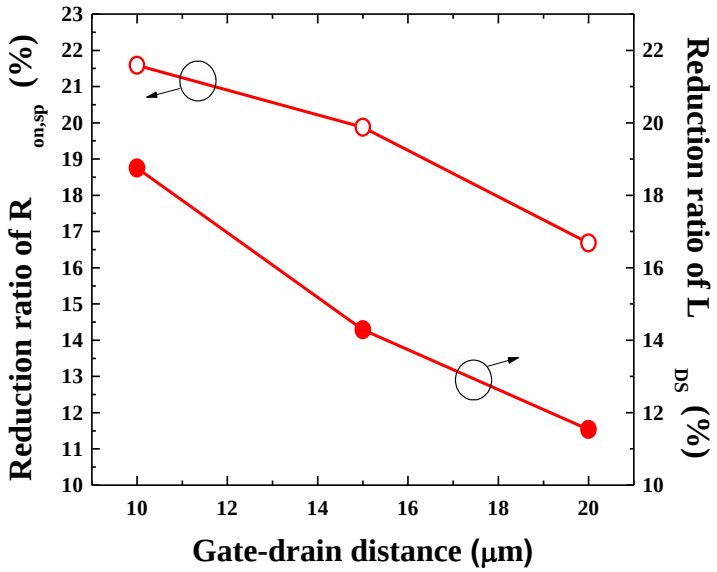
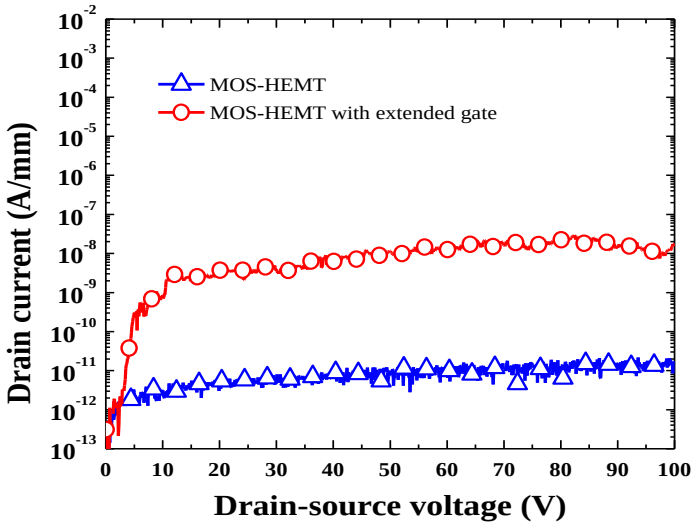


Figure 4-25: L_{GD} versus reduction ratio of $R_{on,sp}$ and L_{DS} in AlGaN/GaN MOS-HEMTs with and without extended gate.

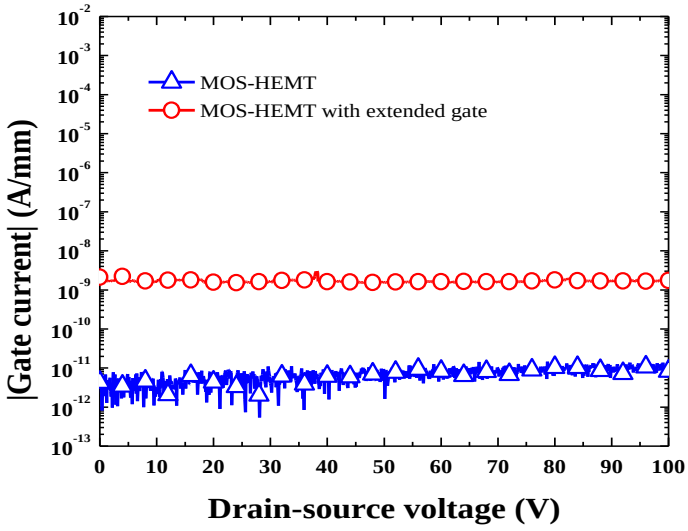
4.6.4. Reverse Blocking Characteristics

Figure 4-26 shows drain and gate leakage current of the AlGaN/GaN MOS-HEMTs with and without the extended gate structure. These were measured at V_{GS} of –4 V. As already shown in above experiment, the AlGaN/GaN MOS-HEMT with TaN-gate without the extended gate structure had very low drain leakage current of 17.4 pA/mm and gate leakage current of –8.3 pA/mm at V_{DS} of 10 V due to effectively blocked gate leakage current by HfO_2 gate insulator. However, the devices using the extended gate structure exhibits slightly high drain leakage current of 18.4 nA/mm and gate leakage current of –1.74 nA/mm arising from tunneling leakage component at the extended gate region through 15 nm –thick HfO_2 gate insulator.

Although a little leakage component at the extended gate region is observed, the breakdown voltage of the AlGaN/GaN MOS-HEMT using the extended gate has almost identical value with that of the conventional MOS-HEMT due to stable blocking characteristics by HfO_2 gate insulator. V_{GS} of –4 V was used for breakdown voltage measurement. Breakdown voltages of the AlGaN/GaN MOS-HEMTs with and without extended gate structure at 10 μm-long L_{GD} are 1460 and 1410 V, respectively. Thus, it is entirely fair to say that this extended TaN-gate provides innovate method to overcome the trade-off relationship between breakdown voltage and $R_{on,sp}$.



(a)



(b)

Figure 4-26: (a) Drain-leakage current of the AlGaN/GaN MOS-HEMTs with and without extended gate (b) gate-leakage current.

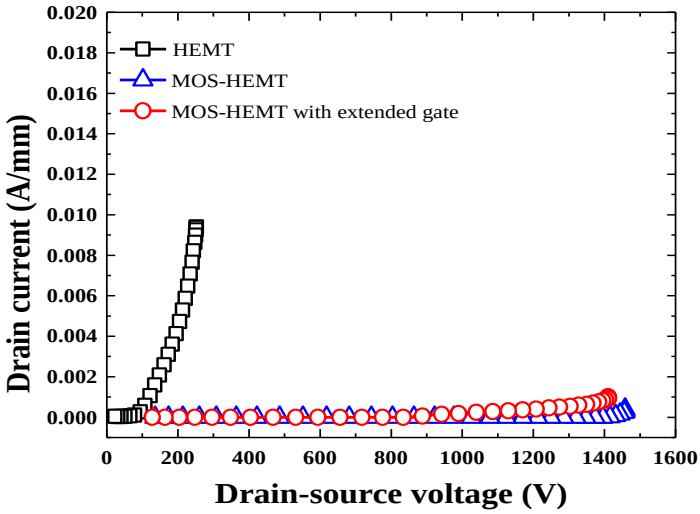


Figure 4-27: Breakdown voltage of the AlGaN/GaN HEMT and MOS-HEMTs with and without extended gate.

4.7. Summary

In this chapter, I proposed RF-sputtered TaN electrodes as gate and drain/source electrodes for the Au-free AlGaN/GaN MOS-HEMTs. TaN-sputtering conditions such as sputtering power and working pressure were optimized to be implemented into the AlGaN/GaN MOS-HEMTs. The effects of thermal annealing for ohmic contact formation on the electrical and material properties of RF-sputtered TaN films were studied. In addition, I proposed and investigated the extended TaN-gate structure in the AlGaN/GaN MOS-HEMTs using RF-sputtered HfO_2 gate insulator for low on-resistance. This devices had high figure-of-merit (FOM) of 872 $MW \cdot cm^{-2}$ and low specific on-resistance ($R_{on,sp}$) of 2.28 $m\Omega \cdot cm^{-2}$ by the effectively reduced drain-source distance in the AlGaN/GaN MOS-HEMT using the extended TaN-gate structure and HfO_2 gate insulator while the conventional MOS-HEMT had FOM of 734 $MW \cdot cm^{-2}$ and $R_{on,sp}$ of 2.91 $m\Omega \cdot cm^{-2}$. I summarized and compared the results including breakdown voltage and $R_{on,sp}$ with the reported data by other groups previously in Fig. 4-28.

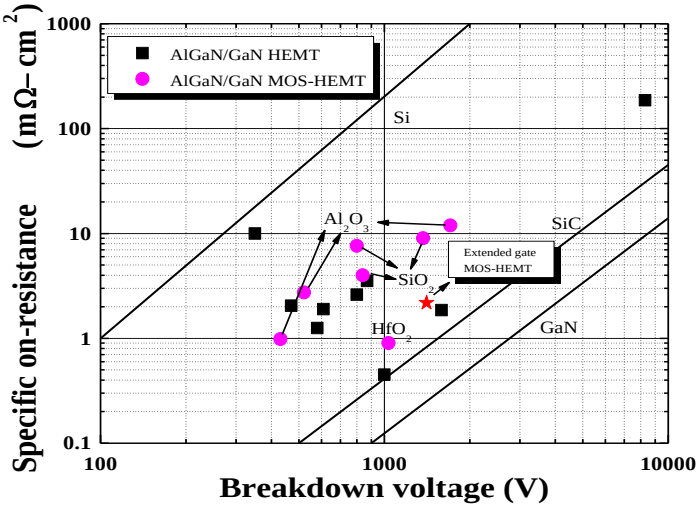


Figure 4-28: $R_{on,sp}$ versus breakdown voltage.

Chapter 5

5 High-Voltage Technologies Employing RF-Sputtered Ga_2O_3-Based Thin Films

5.1. Overview

Breakdown voltage is one of the most important requirement for power semiconductor devices in respect of safe-operation-area (SOA) and maximum delivering power into system or loads. Also, high-breakdown voltage devices have durability against abnormal current flow and electric shock. Although GaN has theoretically high critical electric field value and high figure-of-merits (FOMs) compared to other materials for power semiconductor devices, GaN power devices have not approached its material limitation because of

considerably amount of surface traps and thin GaN buffer layer. Lack of native substrate causes hardship to fabricate vertical GaN devices so that it is difficult to drive GaN devices effectively with lateral structures such as SBD, HEMT, and MESFET. Thus, research for high-voltage AlGaN/GaN HEMTs should be performed to overcome its material and structural demerits.

As I introduced in chapter 2, various technologies such as edge termination structures and GaN buffer growth have been reported for high breakdown voltage. In case of field plates, which are widely used for the AlGaN/GaN HEMTs, precious control of distance between main gate and field plates, each lengths and thickness of passivation layer should be done. If the dimension is not optimized, breakdown voltage can be decreased by field plate structure. Moreover, field plates require additional photolithography steps.

In this chapter, I propose a new technology for high breakdown voltage of the AlGaN/GaN HEMTs using RF-sputtered Ga_2O_3-based films. The AlGaN/GaN HEMTs are controlled by Schottky-type gate as shown in Fig. 5-1. When sufficiently high work-function metal is used for Schottky-gate, GaN/gate Schottky contact would have high Schottky barrier height (SBH). Then, thermionic field emission, which is dominant leakage current origin, is suppressed when doping concentration of GaN or AlGaN is relatively low. However, shallow traps, which act as donor states in GaN, provide low-activation energy to contribute leakage current [129]. As shown in Fig. 5-2, the injected electrons from gate into deep traps cannot contribute to leakage current due to thick Schottky barrier compared to that trough swallow traps [31]. Thus, formation of deep traps may be effective to increase breakdown voltage of the AlGaN/GaN HEMTs. It is well known that the AlGaN/GaN HEMTs have unintentionally doping effects, which are originated from SiC susceptor during high-temperature GaN growth and nitrogen vacancies (V_N) arising from dislocation and polarization charges. In this reason, post processes to form deep traps site and suppress shallow-trap effects is desirable.

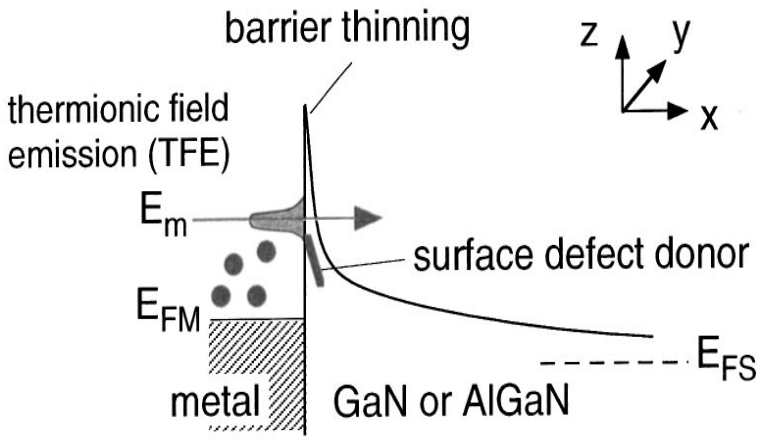


Figure 5-1: Leakage current mechanism in AlGaN/GaN Schottky interface [129].

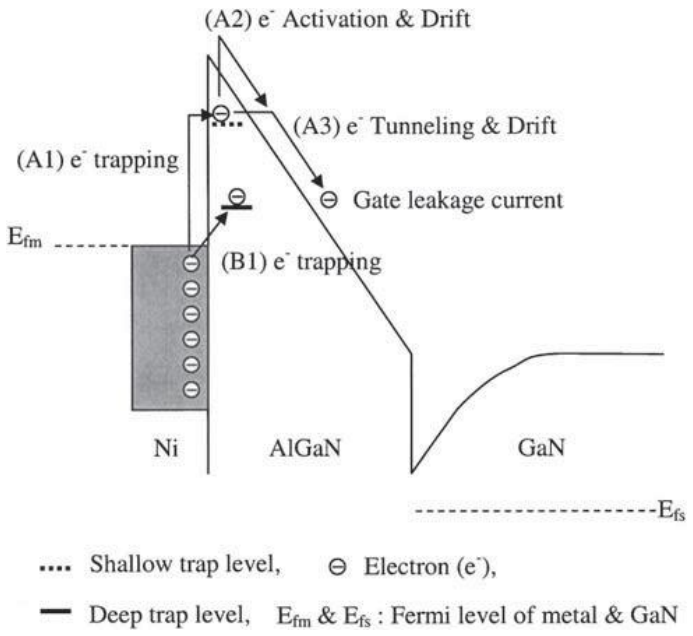


Figure 5-2: Electrons transfer from gate to 2DEG through shallow and deep trap sites [31].

5.2. Reported Deep Traps-Related Technologies in AlGaN/GaN Devices

Effects of deep traps on reverse blocking characteristics of the AlGaN/GaN HEMTs have been studied by a few groups. H. Kim, et al., reported the suppression of gate leakage current in the AlGaN/GaN HEMT after thermal annealing at nitrogen ambient for 20 min [31]. They revealed the suppression effects were originated from deep traps generated by thermal annealing. The existence of deep traps were found by pulsed *I-V* measurement and the exact activation energies for shallow traps and deep traps before and after thermal annealing were quantitatively extracted.

After their report, other methods to form deep traps in thee AlGaN/GaN HEMTs have been flown. O_2 plasma treatment was found that it is effective to form Ga-O bonds, which act as deep traps [130]. Gate leakage current was reduced by about 4 orders after O_2 plasma treatment at 40 W and 200 ^oC. Also, fluoride ion implantation into the AlGaN/GaN HEMT to form deep traps and suppress leakage current was reported as shown in Fig. 5-3 [131]. Gate leakage current was reduced by about 2 orders after CF_4 plasma treatment. F-related deep traps induced by CF_4 treatment screened electron trapping into shallow traps and reduced leakage current. They revealed the measured gate leakage current well matched with Frenkel pools emission through traps site in the AlGaN/GaN heterostructure.

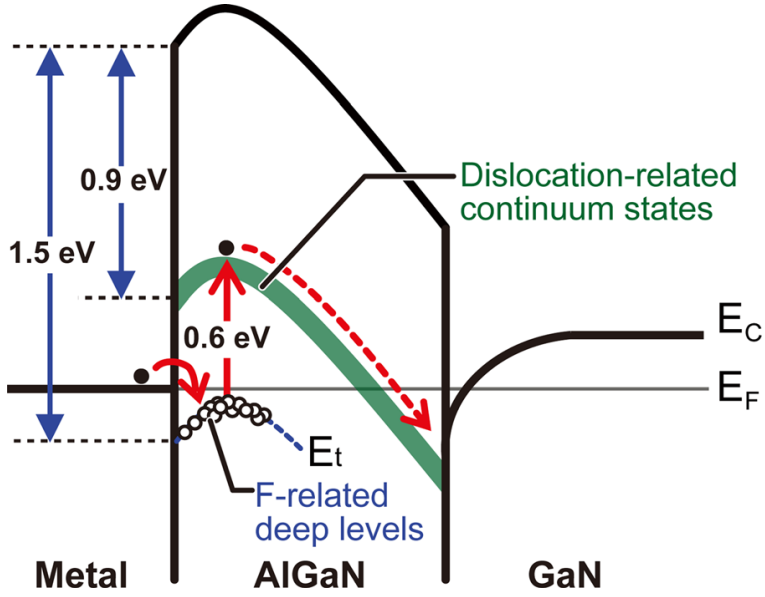


Figure 5-3: Energy band diagram of AlGaN/GaN Schottky interface for description of electron transfer through dislocation-related continuum states and F-related deep level [131].

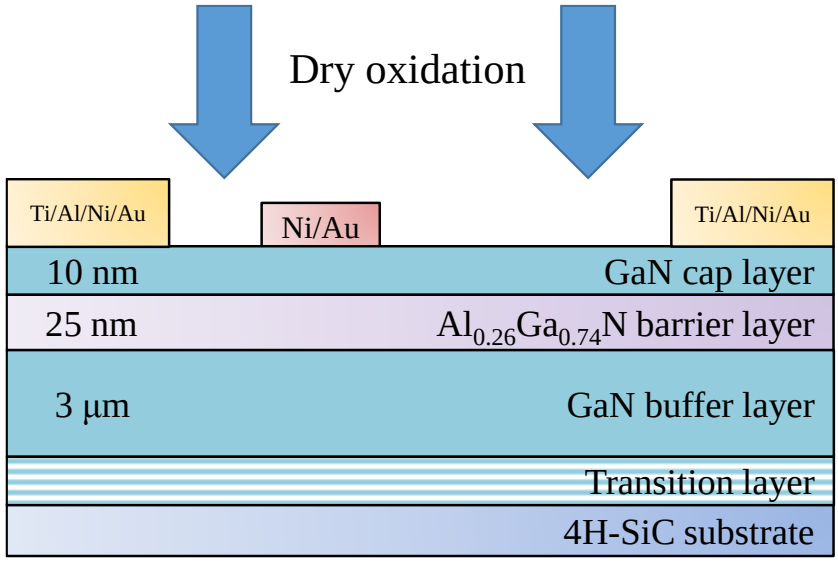
5.3. Post-Oxidation Process in AlGaN/GaN HEMTs

In this section, I propose effects of post-oxidation process in AlGaN/GaN HEMT to improve reverse blocking characteristics. The mechanism of breakdown voltage improvement was studied [132]. Schematic of the fabricated AlGaN/GaN MOS-HEMT-on-SiC substrate using dry oxidation is shown in Fig. 5-4. The MOCVD-grown epitaxial layers consist of 10 nm-thick GaN cap/25 nm-thick $Al_{0.26}Ga_{0.74}N$ barrier/3 μm-thick GaN buffer. The 270- deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) was deposited for source/drain by using e-gun evaporator and lift-off. This was annealed at 880 ^{o}C for 40 s to form ohmic contact. Prior to dry oxidation, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, this devices was annealed at 550 ^{o}C and O_2 ambient for 5 min. And finally, the Ni/Au (30/150 nm) was formed for gate electrode by e-gun evaporator and lift-off. The gate length, gate–source distance, gate–drain distance, and gate width were 3, 3, 20, and 50 μm, respectively.

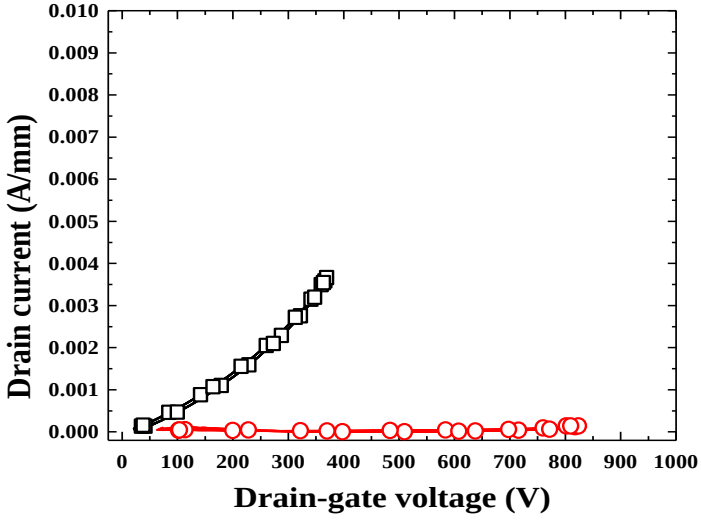
Breakdown voltage defined at drain leakage current of 1 mA/mm was increased from 180 to 830 V by dry oxidation. It was found that oxygen diffused into the AlGaN/GaN HEMTs and formed Ga-O and Al-O bonds after dry oxidation for 5 min at 550 ^{o}C as shown in secondary ion mass spectrometry (SIMS)-depth profile of Fig. 5-5. These SIMS profiles indicate that dry-oxidation is very useful to inject oxygen into GaN and form III-group oxide layer in the AlGaN/GaN HEMTs. What the results make clear at one is that breakdown voltage improvement is originated from Ga-O formation by dry oxidation.

Recently, a new method to increase breakdown voltage in the AlGaN/GaN HEMTs by wet oxidation at 500 ^{o}C for 5 min with N_2 carrier gas of 20 sccm before gate formation was reported [133]. Schematic structure and breakdown voltage are shown in Fig. 5-6. The breakdown voltage, which was determined at drain leakage current of 1 mA/mm, was dramatically increased from 470 to 1674 V by suppressing electron transfer from gate to 2DEG though shallow traps. Auger electron spectroscopy (AES)-depth-profile (Fig. 5-7) indicates that wet oxidation using H_2O enables much active penetration into the AlGaN/GaN heterostructure after wet oxidation. It is well known that H_2O has high probability of penetration than O_2 because of small molecule size so that more active reaction between GaN and oxygen occurs.

However, post-oxidation under O_2 and H_2O ambient causes degradation of forward current due to considerable high-temperature process. I compared output *I*-*V* characteristics of three devices in Fig. 5-8; the conventional HEMT, the O_2 annealed one, and the H_2O annealed one. As I described in chapter 2, GaN is sensitive to high-temperature annealing due to introduction of surface traps so that slightly decreased current was found in output *I*-*V* after O_2 and H_2O annealing. In case of H_2O annealing, considerable degradation of on-resistance was observed. It may be originated from slightly oxidized source/drain electrodes by water vapor. In order to form III-oxide bonding in the AlGaN/GaN heterostructure by annealing, no passivation layer or thermal blocking layer were used. Thus, although O_2 and H_2O annealing are effective method to increase breakdown voltage in the AlGaN/GaN devices, annealing temperature, time, and ambient should be optimized to prevent degradation of forward current from high-temperature process.

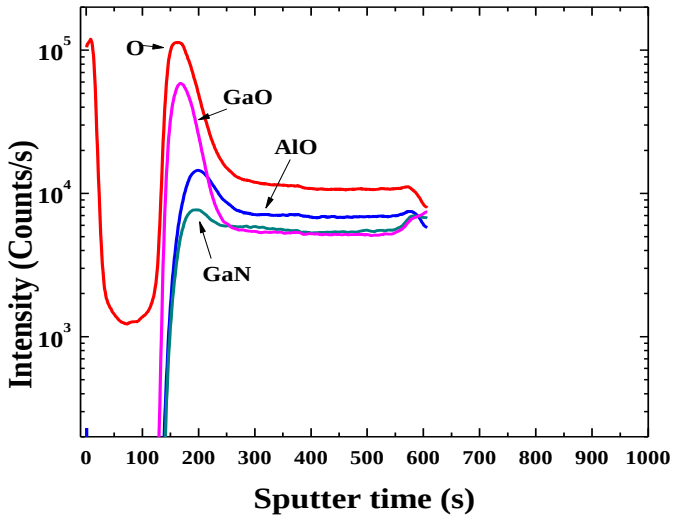


(a)

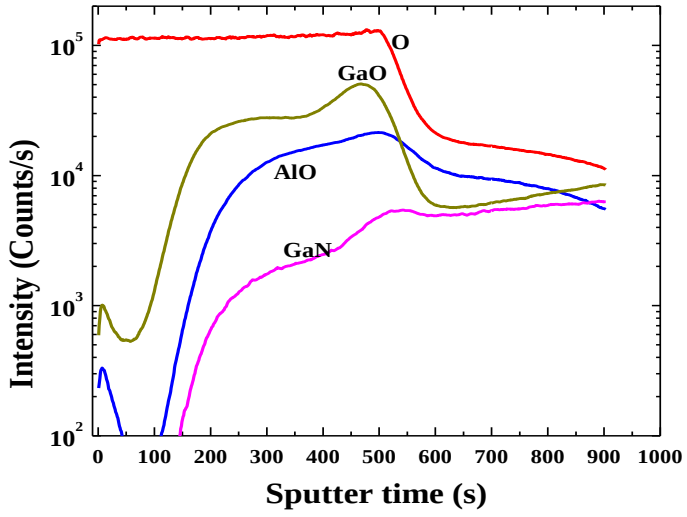


(b)

Figure 5-4: Dry oxidation before gate formation (a) schematic of the device (b) breakdown voltage of the devices with and without dry oxidation [132].

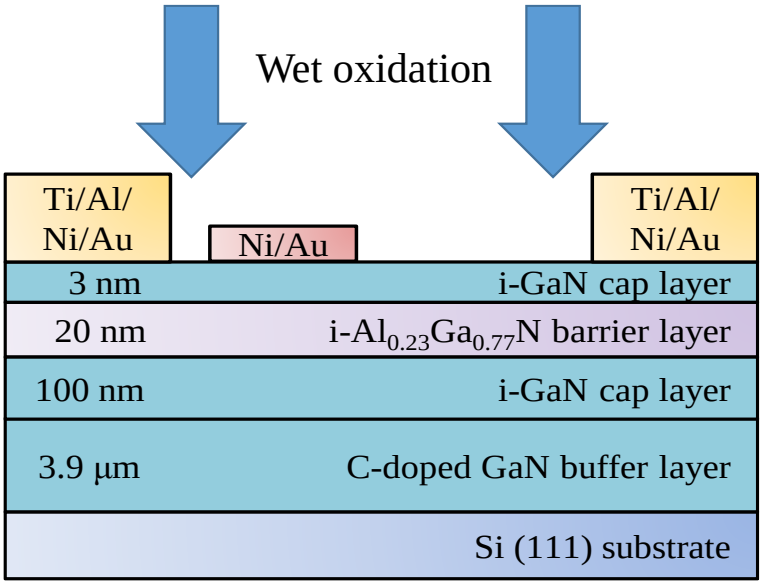


(a)

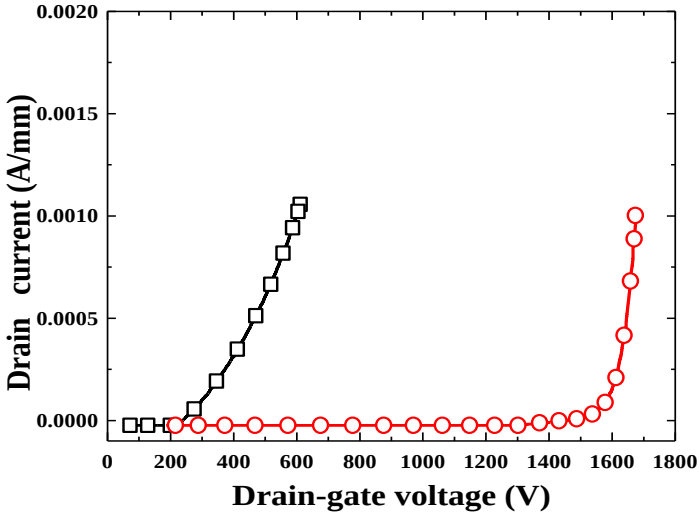


(b)

Figure 5-5: SIMS-depth profiles of AlGaN/GaN heterostructure (a) before and (b) after dry oxidation.



(a)



(b)

Figure 5-6: Wet oxidation before gate formation (a) schematic of the device (b) breakdown voltage of the devices with and without wet oxidation.

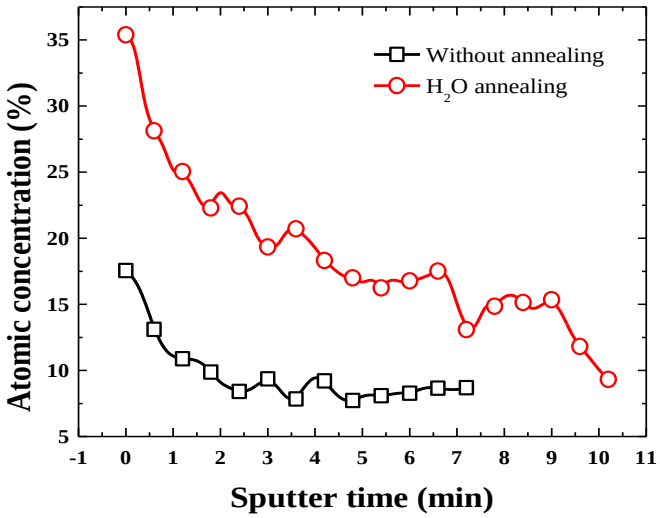


Figure 5-7: AES-depth profiles of AlGaN/GaN heterostructure before and after wet oxidation.

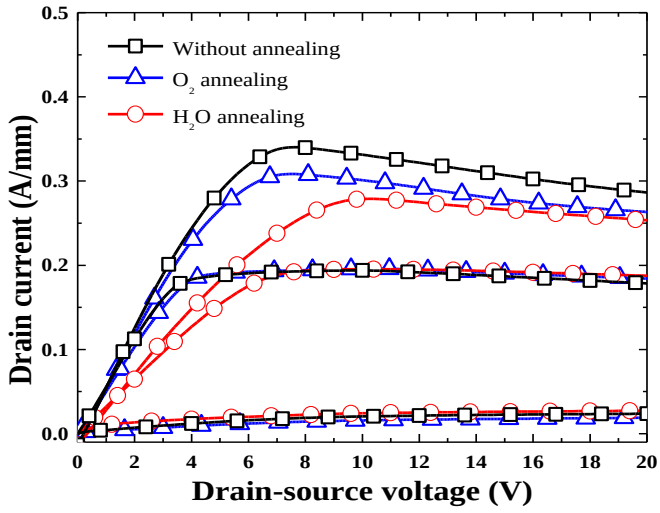


Figure 5-8: Output *I-V* characteristics of AlGaN/GaN HEMTs with and without dry and wet oxidation [133].

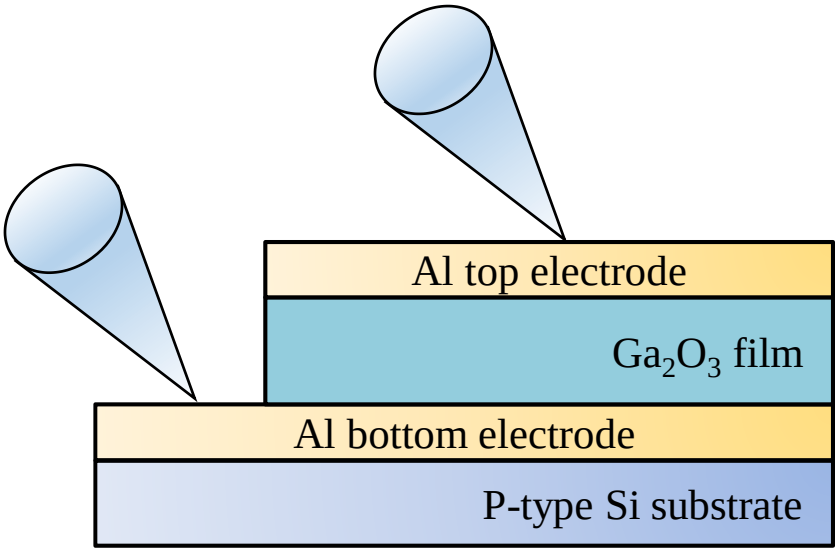
5.4. Material Properties of RF-Sputtered Ga_2O_3 Films

In order to confirm fundamental material properties of RF-sputtered Ga_2O_3 films, I fabricated test pattern using metal-oxide-metal (MIM) structure including Al-Ga_2O_3-Al on p^+ Si substrate as shown in Fig. 5-9. 100 nm-thick Al were used for top and bottom electrodes by e-gun evaporator and lift off. Ga_2O_3 was deposited with various thickness by RF-sputtering at room temperature. RF-power of 300 W, Ar flow of 15 sccm, and working pressure of 3 mTorr were used. As shown in Fig. 5-9 (b), RF-sputtered Ga_2O_3 shows good thickness controllability over sputtering power. The Ga_2O_3 sputtering rates for the powers of 50, 100, 150, and 200W were 0.19, 0.34, 0.6, and 0.83 Å/s, respectively.

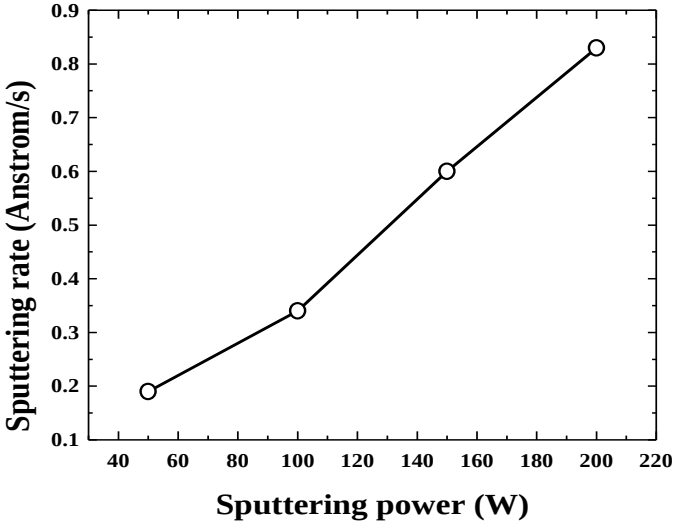
Room temperature process provides an advantage in respect of avoiding thermal degradation of the AlGaN/GaN HEMTs as a result after post-oxidation in section 5.3. Current-voltage (*I-V*) characteristics of the three-different sputtering power and thickness were measured to investigate electrical properties of RF-sputtered Ga_2O_3 films as shown in Fig. 5-9 (c). Leakage current through Ga_2O_3 film were divided by thickness. At high sputtering power of 150 W, unit leakage current is decreased but those breakdown voltage is not high below 1 V. At low sputtering power, Ga_2O_3 film shows slightly conductive properties. It may result from high sputtering conditions provides more dense films than low power. This experimental results show that RF-sputtered films are not suitable to form MOS structure in the AlGaN/GaN HEMTs.

RF-sputtered Ga_2O_3 films doesn't exhibit any crystallinity even substrate

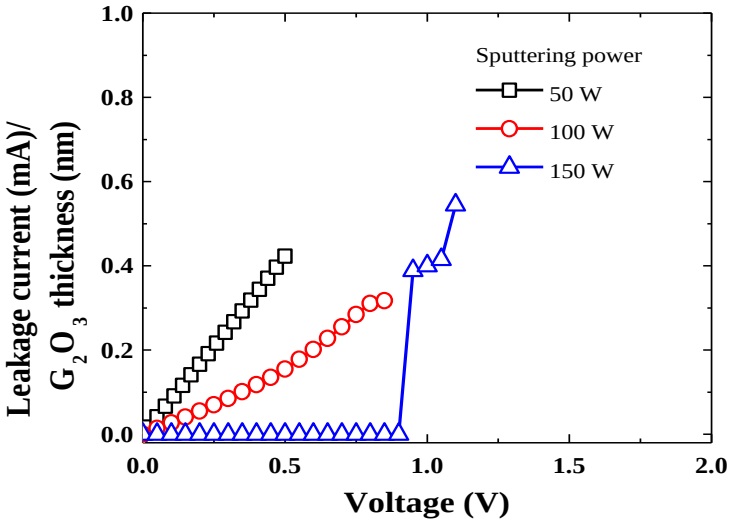
was heated up to 300 ^{o}C as shown in X-ray diffraction (XRD) results of Fig. 5-10. A peak at 54.6^{o} corresponding to β-Ga_2O_3 phase (3 1 2, –5 1 2) [134]. These results lead to the conclusion that RF-sputtered Ga_2O_3 has amorphous β-phase including various bonds. Also, peaks position of X-ray photoelectron spectroscopy (XPS) well agrees with Ga_2O_3 (Ga_{3d}: 20.2 eV, O_{1s}: 530.5 eV) as shown in Fig. 5-11.


Al top electrode
Ga_2O_3 film
Al bottom electrode
P-type Si substrate

(a)


Sputtering rate (Anstrom/s)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
40
60
80
100
120
140
160
180
200
220
Sputtering power (W)

(b)



(c)

Figure 5-9: (a) Test pattern for measuring vertical leakage current (b) sputtering rate of Ga_2O_3 films with power variation (c) leakage current of the RF-sputtered Ga_2O_3 films at various sputtering powers.

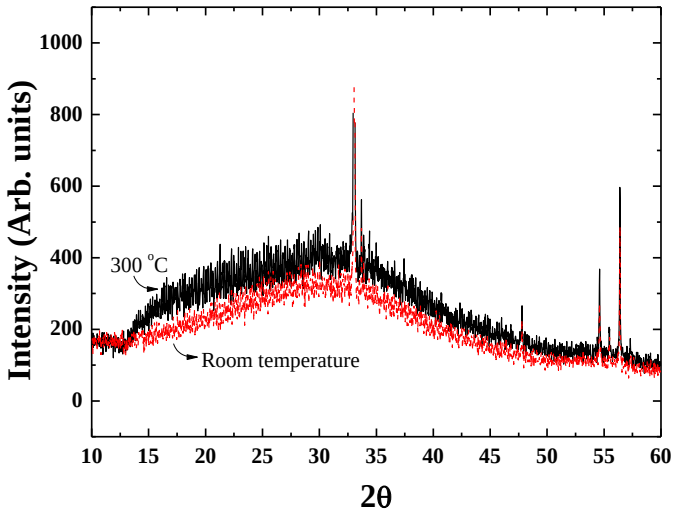


Figure 5-10: XRD results of Ga_2O_3 films sputtered at room temperature and 300 °C.

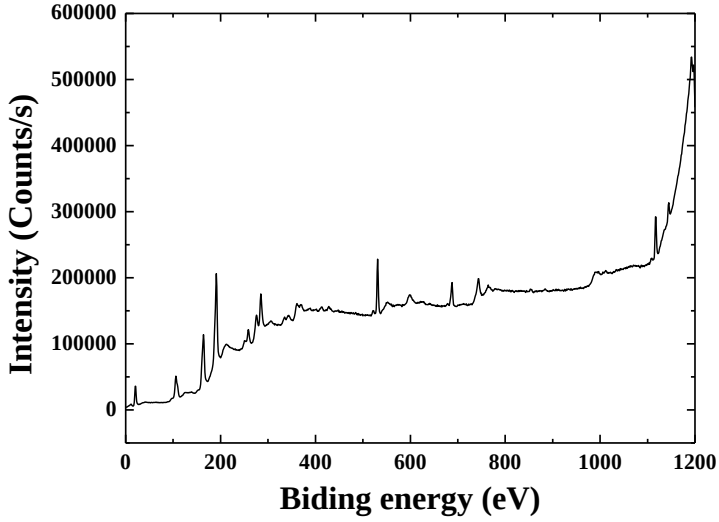


Figure 5-11: XPS results of RF-sputtered Ga_2O_3 film at room temperature.

5.5. Electrical Properties of AlGaN/GaN HEMTs Employing Ga_2O_3 Films

In this section, electrical characteristics of the AlGaN/GaN HEMTs-on-SiC substrate using RF-sputtered Ga_2O_3 films are proposed to increase breakdown voltage. Schematic cross-sectional view of the AlGaN/GaN MOS-HEMTs-on-SiC substrate using RF-sputtered Ga_2O_3 film is shown in Fig. 5-12 [135]. The MOCVD-grown epitaxial layers consist of 3 nm-thick GaN cap/30 nm-thick $Al_{0.26}Ga_{0.74}N$ barrier/3 μm-thick Fe-doped GaN buffer. The 270-deep mesa was formed for device-to-device isolation. Ti/Al/Ni/Au (20/80/20/100 nm) was deposited for source/drain by using e-gun evaporator and lift-off. This was annealed at 880 ^{o}C for 40 s to form ohmic contact. Prior to Ga_2O_3 sputtering, I dipped the device into 30:1 BOE for 30 s to remove native oxide. Then, 10 nm-thick Ga_2O_3 was sputtered at 3 mTorr with Ar flow of 15 sccm at room temperature. Sputtering power was varied from 50 to 200 W. And finally, Ni/Au (30/150) was formed on Ga_2O_3 film by e-gun evaporator and lift off technique. The gate length, gate–source distance, gate–drain distance, and gate width were 3, 3, 20, and 50 μm, respectively. An unpassivated AlGaN/GaN HEMT was also fabricated for comparison purpose.

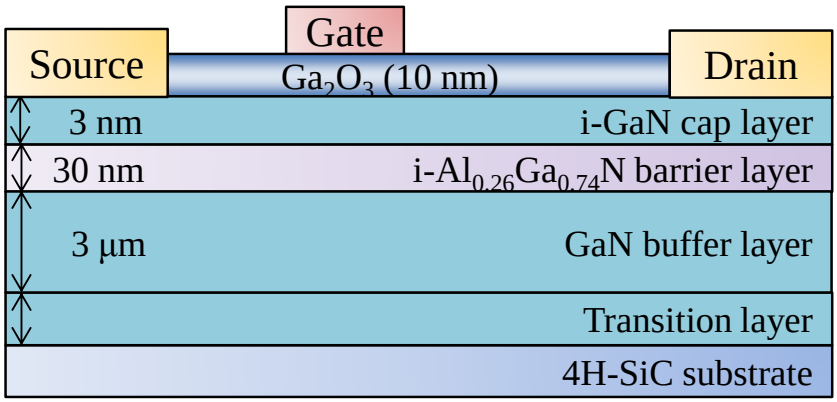


Figure 5-12: Schematic of AlGaN/GaN HEMT-on-SiC using RF-sputtered Ga_2O_3 films [135].

5.5.1. Reverse Blocking Characteristics

Figure 5-13 shows the drain and gate leakage currents of the Ga_2O_3-passivated AlGaN/GaN HEMTs and the unpassivated sample at various sputtering powers. The drain and gate leakage currents were measured at a V_{GS} of –10V and V_{DS} of 100 V. The drain leakage current of the Ga_2O_3-passivated HEMTs decreases with decreasing sputtering power. The Ga_2O_3-passivated HEMTs have drain leakage currents of 63 nA/mm, 237 nA/mm, 1.7 μA/mm, and 181 μA/mm when the devices are sputtered at 50, 100, 150, and 200 W, respectively, compared to 52 μA/mm for the unpassivated sample. The sputtered Ga_2O_3 exhibits an amorphous phase comprising various bonding and nonbonding states such as Ga and O vacancies [136, 137]. Under reverse blocking mode, the drain-sided gate edge in the AlGaN/GaN HEMTs exhibits a high electric field, so hot electrons at the gate/GaN interface cause the leakage current as well as breakdown. Electrons injected into deep traps such as Ga vacancies have a low probability of de-trapping [31] and these suppress the surface leakage current, and extend the depletion region between gate and drain.

However, a high sputtering power may have induced surface leakage current because of generation of V_N in the AlGaN/GaN HEMTs [98, 138, 139]. V_N are a surface leakage source and/or leakage current path by the trapping and de-trapping of electrons between shallow states and the conduction band of GaN [98]. A low sputtering power may decrease the density of V_N by reducing sputtering damage on the surface. Therefore, a low sputtering power possibly suppresses the surface leakage current of a device. The AlGaN/GaN HEMT sputtered at 200 W shows an increased leakage current compared with Ga_2O_3-passivated HEMTs sputtered at other low powers. The Ga_2O_3-passivated HEMTs exhibited leakage currents of –4.3 nA/mm, –45 nA/mm, –

128 nA/mm, and –24 μA/mm when sputtered at 50, 100, 150, and 200 W, respectively. In comparison, the unpassivated HEMT exhibited a leakage current of –2.5 μA/mm.

Figure 5-14 shows the Schottky barrier height (Φ_{BN}) and extracted ideality factor (n) at a V_{GD} of 0.5 V for the unpassivated device and the devices sputtered with Ga_2O_3 at various powers, based on gate-drain diode I–V characteristics by using following two equations [113].

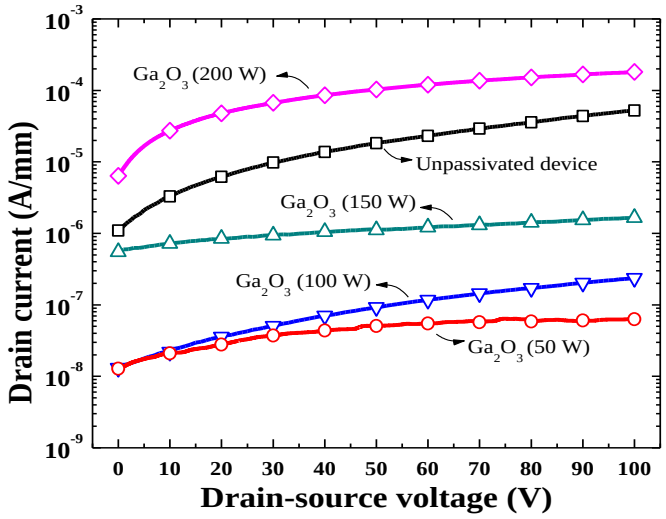
$$\mathrm{n} = \frac{qV}{KT\ln(\frac{J}{J_S})} \quad , \tag{5.1}$$

$$\Phi_{BN} = \frac{KT}{q}\ln(\frac{A^{**}T^2}{J_S}) \tag{5.2}$$

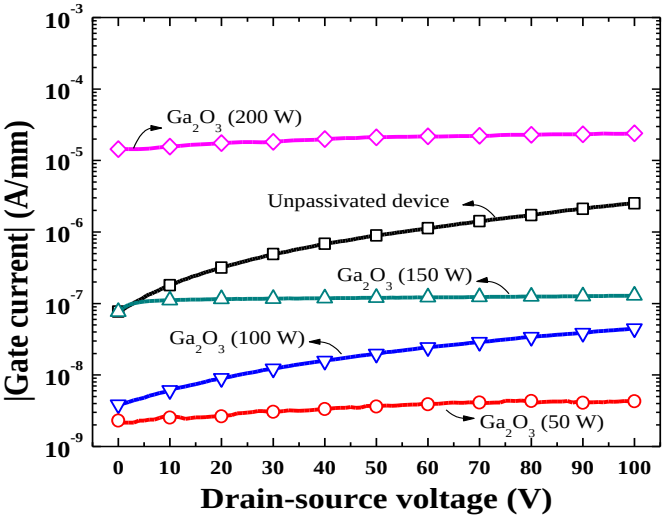
J_S is the saturation current density obtained by diode I–V characteristics at a V_{GD} of 0 V, A^{**} is the effective Richardson constant assuming 26.64 A/(cm·K)^2, and the temperature is 300 K. The Ga_2O_3-passivated HEMTs sputtered at low powers have higher Φ_{BN} values than the unpassivated sample because deep traps such as Ga vacancies in the Ga_2O_3 passivation layer may have captured electrons causing the conduction band of the gate-sided GaN cap to be lifted. The Ga_2O_3-passivated HEMTs had Φ_{BN} of 0.895, 0.841, 0.823, and 0.634 eV when sputtered at powers of 50, 100, 150, and 200 W, respectively. The unpassivated sample exhibited a Φ_{BN} of 0.715 eV. Damage to the AlGaN/GaN heterostructure by Ga_2O_3 sputtering at a high power may have caused a tunneling current via a thinned Schottky barrier and/or trap-assisted emission

Figure 5-15 shows the breakdown voltage values of the Ga_2O_3-passivated HEMTs for various sputtering powers. The breakdown voltage is defined at a drain leakage current of 1 mA/mm. Breakdown voltage increases with decreasing sputtering power. The Ga_2O_3-passivated HEMT sputtered at 50 W shows a high breakdown voltage of 1430 V, while that of the unpassivated

sample is 520 V. The devices sputtered at 100 and 150 W exhibit breakdown voltage values of 890 and 820 V, respectively. However, the Ga_2O_3-passivated HEMT sputtered at 200W shows a breakdown voltage of 460 V, relatively low compared with those of the unpassivated device and devices passivated at other sputtering powers, which is attributed to increased leakage current caused by sputtering damage. Also, the breakdown voltage values of the Ga_2O_3-passivated HEMTs linearly increase with L_{GD}, as shown in Fig. 5-15 (b). The injected electrons in the Ga_2O_3 passivation layer improve the extension of the depletion region between the gate and drain. The peak breakdown voltage of 2730 V was measured for a sputtering power of 50 W and L_{GD} of 40 μm, while the unpassivated device exhibited a breakdown voltage of less than 600 V.

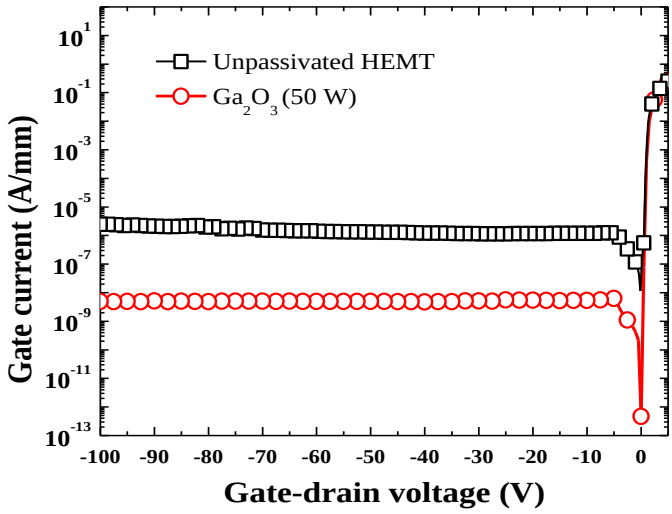


(a)

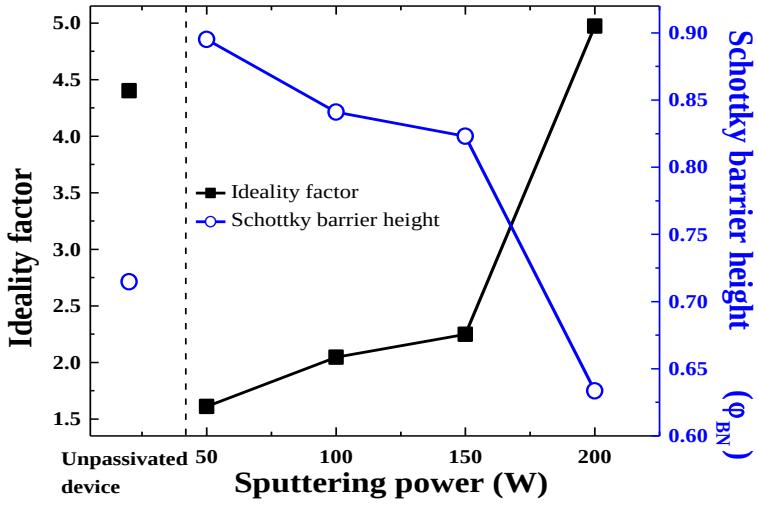


(b)

Figure 5-13: Leakage current of AlGaN/GaN HEMTs using Ga_2O_3 films sputtered at various powers (a) drain leakage current (b) gate leakage current.

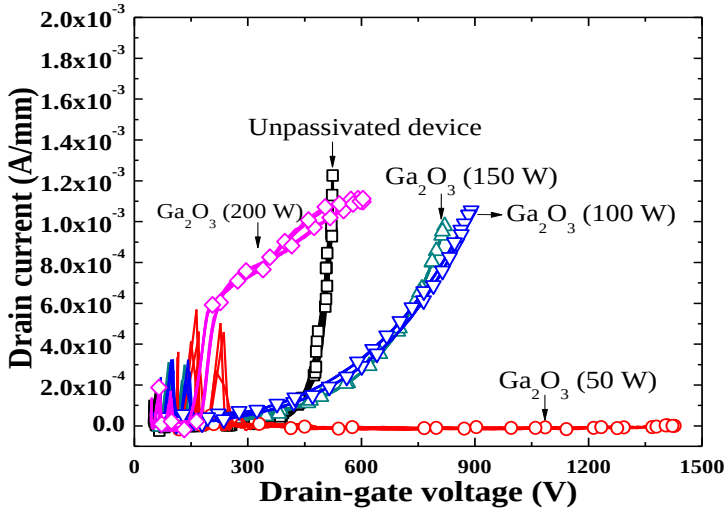


(a)

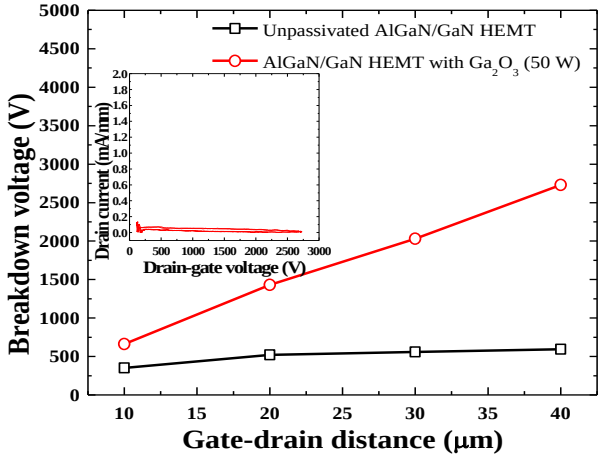


(b)

Figure 5-14: Gate-drain diode *I-V* of AlGaN/GaN HEMTs with and without Ga_2O_3 film sputtered at 50 W (b) ideality factor and Schottky barrier height.



(a)



(b)

Figure 5-15: Breakdown voltage characteristics of AlGaN/GaN HEMTs using Ga_2O_3 films sputtered at various powers (a) at 20 μm-long L_{GD} (b) breakdown voltage value with L_{GD} variation.

5.5.2. Switching Characteristics

Figure 5-16 shows output characteristics of the unpassivated and Ga_2O_3-passivated HEMTs. Output characteristics were measured while sweeping V_{GS} from 2 to –6 at –2 V increments. Transfer curves were measured at V_{DS} of 10 V. Drain currents of the Ga_2O_3-passivated HEMTs sputtered at 50, 100, and 150 W are not significantly different from the unpassivated sample. The drain currents of the unpassivated HEMT and Ga_2O_3-passivated HEMTs sputtered at 50, 100, and 150 W are about 375 mA/mm at V_{GS} of 0 V and V_{DS} of 20 V, while that of the Ga_2O_3-passivated HEMT sputtered at 200 W is 424 mA/mm because of considerable sputtering damage. The unpassivated HEMT and Ga_2O_3-passivated HEMTs sputtered at 50, 100, and 150 W exhibit a threshold voltage of –4.4 V, as shown by the transfer characteristics of Fig. 5-17. However, the threshold voltage of the Ga_2O_3-passivated HEMT sputtered at 200 W is decreased to –5.4 V because of a lowered Φ_{BN} caused by sputtering damage.

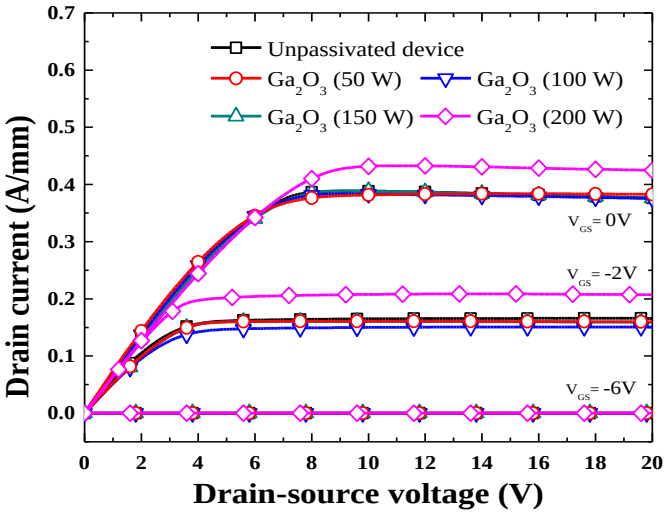


Figure 5-16: Output *I-V* characteristics of AlGaN/GaN HEMTs with and without Ga_2O_3 films sputtered at various powers.

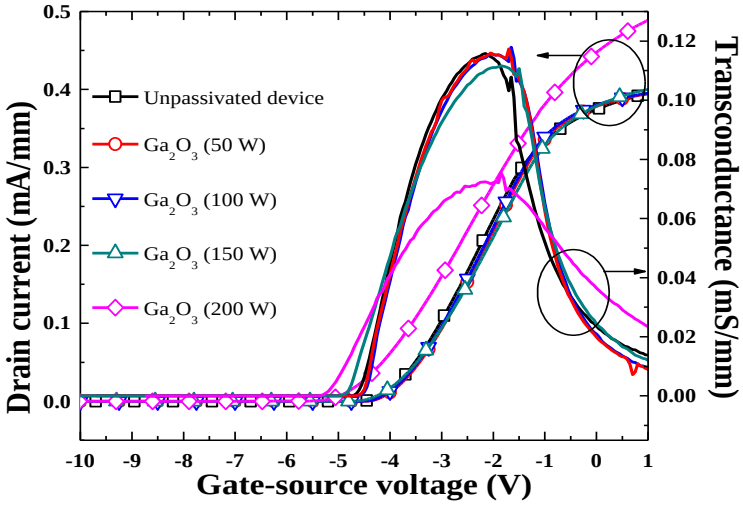
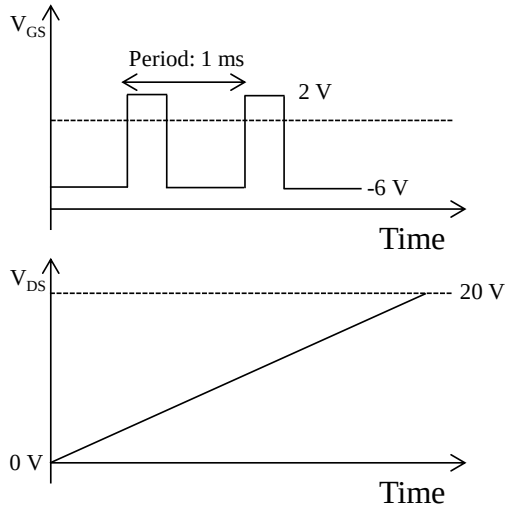


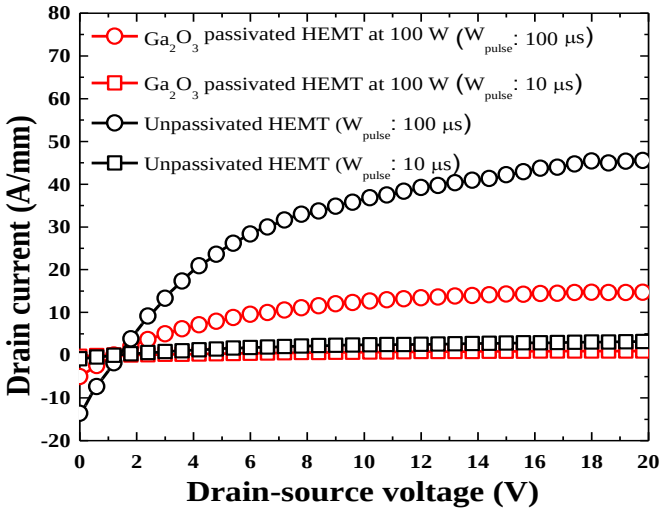
Figure 5-17: Transfer characteristics of AlGaN/GaN HEMTs with and without Ga_2O_3 films sputtered at various powers.

5.5.3. Pulsed *I-V* Characteristics

Figure 5-18 shows pulsed *I–V* characteristics of the unpassivated HEMT and the Ga_2O_3-passivated HEMT sputtered at 100 W, for verification of electron injection into deep traps and the extension of the depletion region. I swept static V_{DS} from 0 to 20 V with pulsed V_{GS} with the following conditions condition: pulse period of 1 ms, pulse widths of 100 and 10 μs, off-bias of –6 V, and on-bias of 2 V. The pulsed drain current of the unpassivated HEMT is about three times larger than that of the Ga_2O_3-passivated HEMT at a pulse width of 100 μs. This indicates that the Ga_2O_3-passivated HEMT has trapping levels deeper than the surface states in the unpassivated HEMT. Thus, it should be concluded, from what has been stated above, that RF-sputtered Ga_2O_3 films are effective to increase breakdown voltage and suppress leakage current in the AlGaN/GaN HEMTs by deep trap states in RF-sputtered Ga_2O_3 films.



(a)



(b)

Figure 5-18: Pulsed *I-V* characteristics of AlGaN/GaN HEMTs with and without Ga_2O_3 film sputtered at 100 W (a) measurement conditions (b) experimental results.

5.6. Electrical Properties of AlGaN/GaN HEMTs Multiple Al_2O_3/Ga_2O_3 Stack Structure

In this section, new multiple Al_2O_3/Ga_2O_3 stacks in the AlGaN/GaN HEMTs-on-Si substrate with under the gate in order to increase the breakdown voltage and V_{TH}. This multiple Al_2O_3/Ga_2O_3 stacks are useful to extend depletion region under gate due to effective injection of electron from gate into Ga_2O_3 layer sandwiched by Al_2O_3 blocking layer. Ga_2O_3 layer which is sandwiched by Al_2O_3 acts as charge accumulation center due to the unintentionally formed gallium Vacancies (V_{Ga}) [140]. The accumulated electrons in Ga_2O_3 layer under the reverse bias deplete the electrons in bulk and 2DEG so that breakdown voltage and V_{TH} are increased.

The cross-sectional view of the proposed device is shown in Fig. 5-19 [141]. A 3.8 μm-thick transition layer, 1.7 μm-thick unintentionally doped (UID) GaN buffer layer, a 20-nm-thick UID $Al_{0.23}Ga_{0.77}N$ barrier layer, and a 4 nm-thick UID GaN cap layer were grown on Si substrate in sequence by metal-organic chemical vapor deposition. The mesa isolation was performed by BCl_3 and Cl_2 based inductively coupled plasma-reactive ion etch to define active regions. Ohmic metal of Ti/Al/Ni/Au (20/80/20/100 nm) was formed by lift-off and annealed at 880 ^oC for 40 s under N_2 ambient. Prior to sputtering of the multiple Al_2O_3/Ga_2O_3 stacks, device was dipped in 30 : 1 buffered oxide etchant to remove native oxide. 10 nm-thick multiple Al_2O_3/Ga_2O_3 stacks were sputtered at room temperature under Ar ambient. The stacks with five layers consisted of 2 nm-thick Al_2O_3 and 2 nm-thick Ga_2O_3. I applied the low power of 50 W for suppressing sputtering damage on the surface. Finally, Schottky

contact of Ni/Au (30/150 nm) was formed by liftoff.

I also fabricated two conventional devices which had no passivation layer and only 10 nm-thick Al_2O_3 for comparison purpose. A gate width, a gate length, and a gate–drain distance were 50, 3, and 20 μm, respectively.

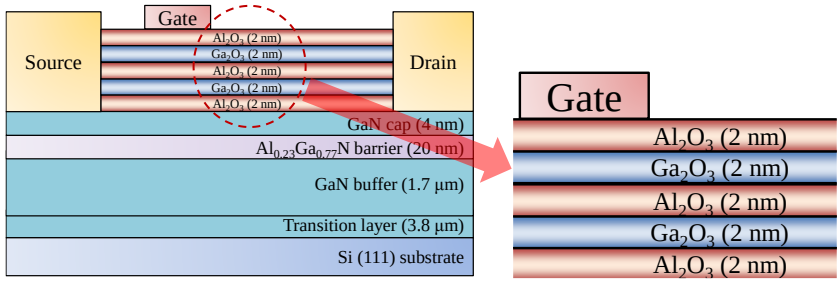


Figure 5-19: Schematic of AlGaN/GaN HEMT using multiple Al_2O_3/Ga_2O_3 stacks [141].

5.6.1. Reverse Blocking Characteristics

Figure 5-20 shows the drain leakage current of the devices. The drain leakage was measured at V_{GS} of –10 V and V_{DS} of 100 V. The drain leakage current of the unpassivated device and the device with only Al_2O_3 are 654 and 1.8 μA/mm while that of the proposed device with the multiple Al_2O_3/Ga_2O_3 stacks is 33 nA/mm. The electron trapping through shallow states on the surface can cause leakage current of the AlGaN/GaN HEMTs. The unpassivated device shows the high leakage current. The suppression of the leakage current due to Al_2O_3 indicates that the sputtered Al_2O_3 passivates the surface of GaN cap layer so that the electron trapping into surface states is suppressed. The accumulated electrons in Ga_2O_3 sandwiched by Al_2O_3 extend the depletion region so that the proposed device with the multiple Al_2O_3/Ga_2O_3 stacks shows the less leakage current than the other devices. It has reported that Ga_2O_3 layer which is sandwiched by Al_2O_3 acts as charge accumulation center.

Figure 5-21 shows the two-terminal breakdown voltages of the devices. The breakdown voltage is defined at the leakage current of 1 mA/mm. The unpassivated device shows the low breakdown voltage of 380 V. However, the breakdown voltage of the devices with only Al_2O_3 and the multiple Al_2O_3/Ga_2O_3 stacks achieve 1050 and 1104 V, respectively. Our experimental results show that the breakdown voltage of the fabricated devices with the longer gate–drain distance than 20 μm is limited to 1104 V. A small difference of the breakdown voltage between the proposed device with the multiple Al_2O_3/Ga_2O_3 stacks and the device with only Al_2O_3 is attributed to the breakdown at interface between transition layer and Si substrate [57].

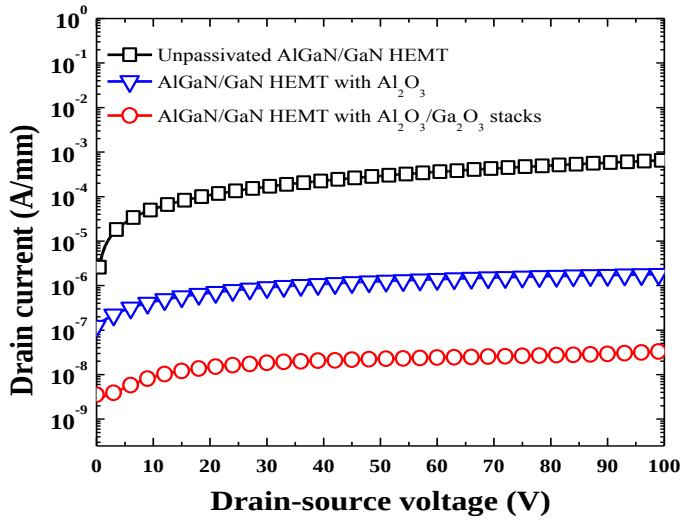


Figure 5-20: Drain leakage current of AlGaN/GaN HEMTs with and without Al_2O_3 and multiple Al_2O_3/Ga_2O_3 stacks.

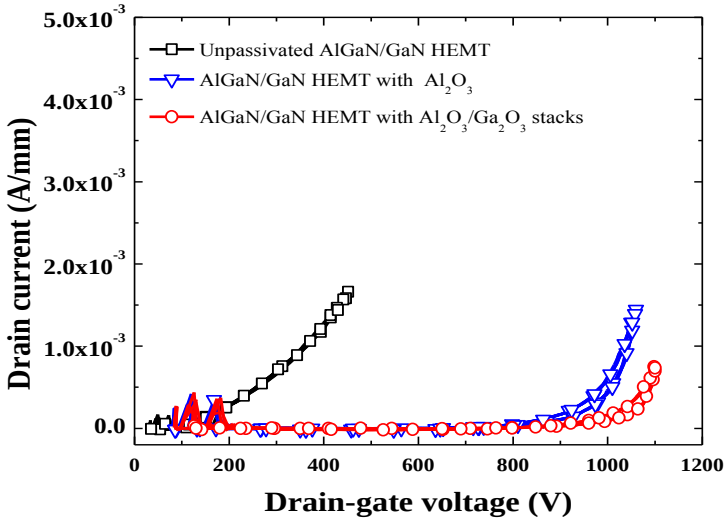


Figure 5-21: Breakdown voltage characteristics of AlGaN/GaN HEMTs with and without Al_2O_3 and multiple Al_2O_3/Ga_2O_3 stacks.

5.6.2. Switching Characteristics

Figure 5-22 shows the output characteristics of the devices. They are measured with sweeping V_{GS} from 2 to –4 V in –2 V increment. The proposed device with the multiple Al_2O_3/Ga_2O_3 stacks shows a high saturation current. The drain current of the devices with the multiple Al_2O_3/Ga_2O_3 stacks and only Al_2O_3, and the unpassivated device are 305, 221, and 224 mA/mm at V_{GS} of 2 V and V_{DS} of 20 V, respectively. The injected holes in Ga_2O_3 layer of the proposed device under the forward bias may accumulate more electrons in a quantum well of 2DEG than the unpassivated device with Ni/GaN Schottky contact. However, the sputtering damage on AlGaN/GaN heterostructure may degrade the slope of current–voltage (*I*–*V*) and the knee voltage. I fabricated the test pattern in order to verify the degradation of on-resistance in the HEMT with only Al_2O_3 and device with the multiple Al_2O_3/Ga_2O_3 stacks. The structure of test pattern and the *I*–*V* results before and after the sputtering the multiple Al_2O_3/Ga_2O_3 stacks are shown in Fig. 5-23. The degradation of current in test pattern may be caused by sputtering damage on the AlGaN/GaN heterostructure. Recently, the degradation of electron concentration and mobility by SiO_2 sputtering damage has been reported [98].

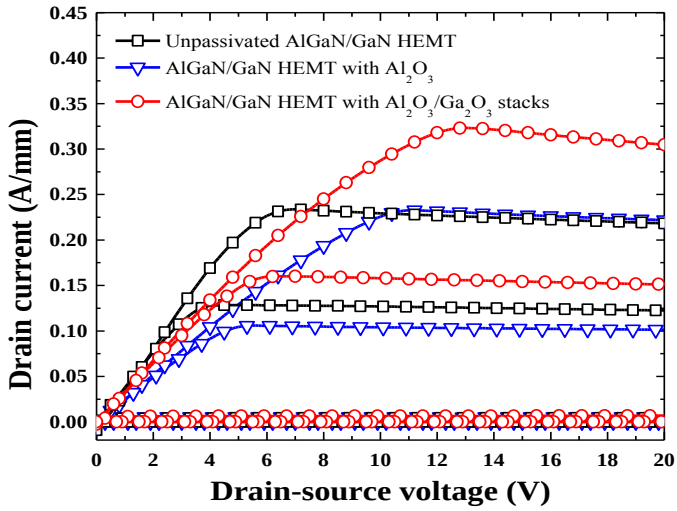
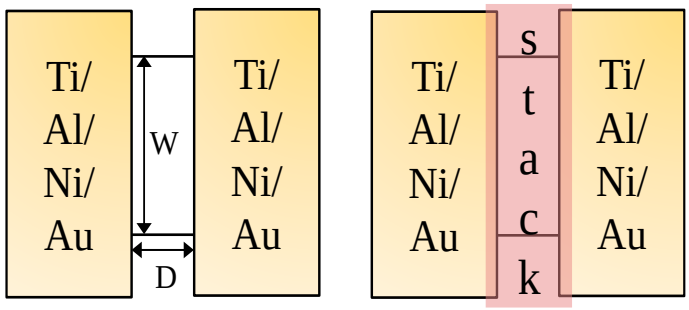
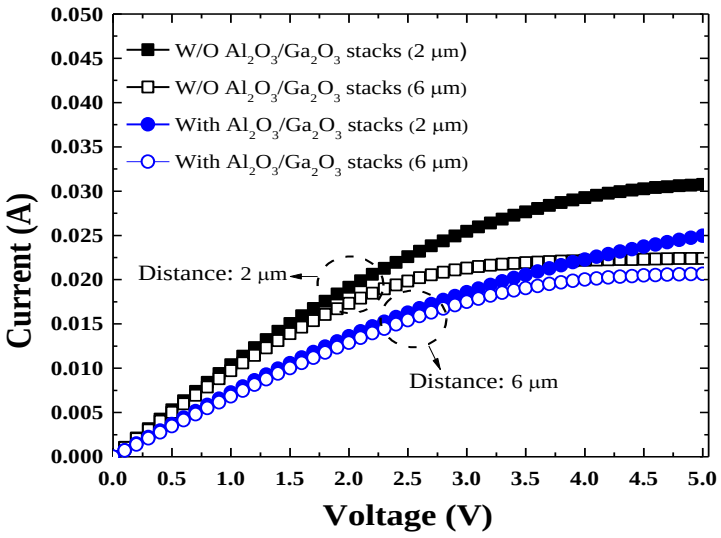


Figure 5-22: Output *I-V* characteristics of AlGaN/GaN HEMTs with and without Al_2O_3 and multiple Al_2O_3/Ga_2O_3 stacks.



W (width): 50 μm
D (distance): 2, 6 μm

(a)



(b)

Figure 5-23: Test pattern including two-ohmic pad (a) top-view of the pattern (b) *I-V* characteristics of test pattern with and without multiple Al_2O_3/Ga_2O_3 stacks.

5.6.3. Shift of Threshold Voltage and Hysteresis Phenomena

Figure 5-24 shows the transfer characteristics at V_{DS} of 5 V. The V_{TH} is determined at drain current of 1 mA/mm. The V_{TH} of the device with only Al_2O_3 is negatively shifted from –2 to –2.2 V because the distance from gate to 2DEG is increased. The V_{TH} of the proposed device with the multiple Al_2O_3/Ga_2O_3 stacks is –1.4 V because the injected electrons at reverse bias deplete the 2DEG. The decrease of drain current is caused by sputtering damage on the AlGaN/GaN heterostructure. Also electrons injection from gate into the multiple Al_2O_3/Ga_2O_3 stacks during the device operation contributes the decrease of drain current.

The charge accumulation of the proposed devices is investigated by capacitance–voltage (C–V) measurement as shown in Fig. 5-25. The capacitance between gate and drain was measured under both positive and negative directions at 1 MHz. The proposed device with the multiple Al_2O_3/Ga_2O_3 stacks achieves the higher on-state capacitance than the unpassivated one because the charges are accumulated in Ga_2O_3. The high on-state capacitance of the proposed device agrees well with the high saturation current. The proposed device with the multiple Al_2O_3/Ga_2O_3 stacks shows a large hysteresis. The large hysteresis induces the positive shift of V_{TH}, the suppression of leakage current, and the increase of saturation current. The injected charge density of 9.72×10^{14} $cm^2\cdot eV^{-1}$ is extracted by subthreshold characteristics in transfer curve and C–V characteristics [40].

Finally, I deposited 300 nm-thick SiO_2 layer on the proposed device with the multiple Al_2O_3/Ga_2O_3 stacks by using inductively coupled plasma-chemical vapor deposition (ICP-CVD). The negative DC stress makes the condition of

the electron accumulation in the stacks and the enhanced depletion. I measured the transfer characteristics of the proposed device with and without final SiO_2 layer before and after negative DC stress. Figure 5-26 shows the measured transfer characteristics before and after negative DC stress (V_{GS} of –10 V for 100 s). Two kinds of integration time ($T_{integration}$: 16.7 and 100.2 ms) were used for verifying the degradation of drain current during the measurement. In case of the device without SiO_2 passivation layer and DC negative stress, the drain current with $T_{integration}$ of 16.7 ms is higher than that with $T_{integration}$ of 100.2 ms. Degradation of drain current during the measurement is caused by charge injection into the surface traps [142]. The drain current is decreased and the V_{TH} is shifted from –1.4 to 0.12 V at $T_{integration}$ of 100.2 ms after DC negative stress.

In case of the proposed device with SiO_2 passivation layer on the multiple Al_2O_3/Ga_2O_3 stacks, the transfer characteristics are not significantly changed even longer stress time as shown in Fig. 5-27. The results before and after DC stress reveal that the improvement of breakdown voltage and V_{TH} in the proposed device is originated from charge accumulation in the multiple Al_2O_3/Ga_2O_3 stacks because the SiO_2 blocks the charge injection from gate into surface of the multiple Al_2O_3/Ga_2O_3 stacks.

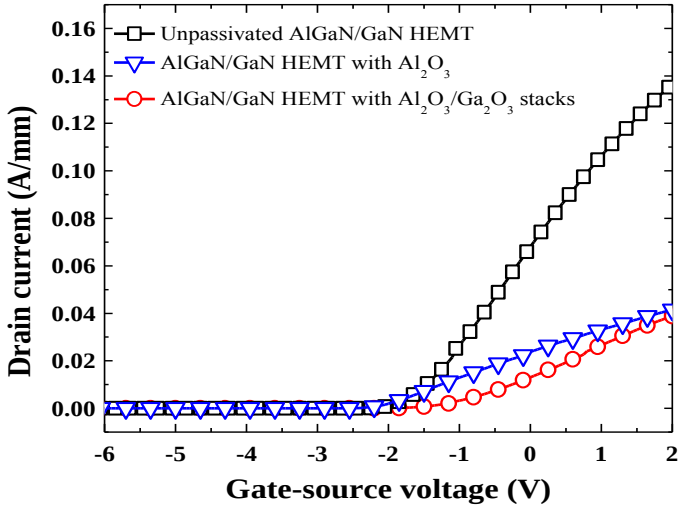


Figure 5-24: Transfer characteristics of AlGaN/GaN HEMTs with and without Al_2O_3 and multiple Al_2O_3/Ga_2O_3 stacks.

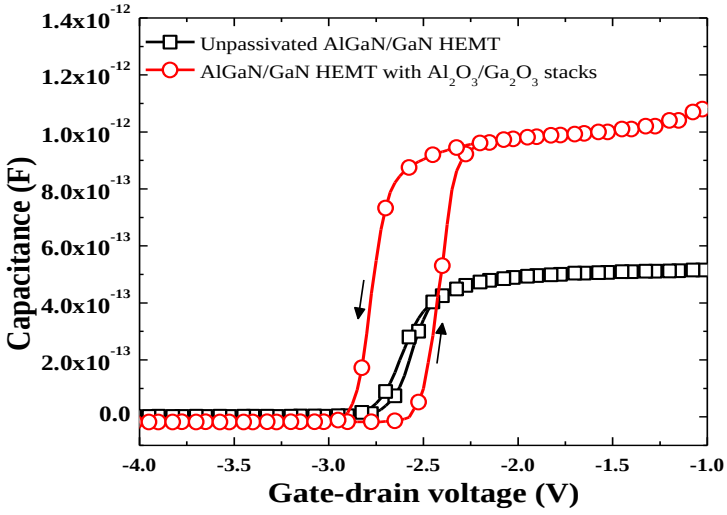


Figure 5-25: Capacitance-voltage characteristics of AlGaN/GaN HEMTs with and without multiple Al_2O_3/Ga_2O_3 stacks.

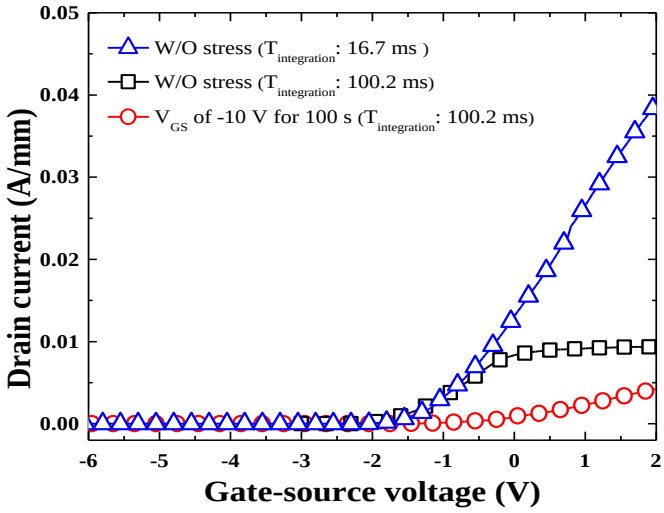


Figure 5-26: Transfer characteristics of AlGaN/GaN HEMTs with and without negative DC stress and different integration time.

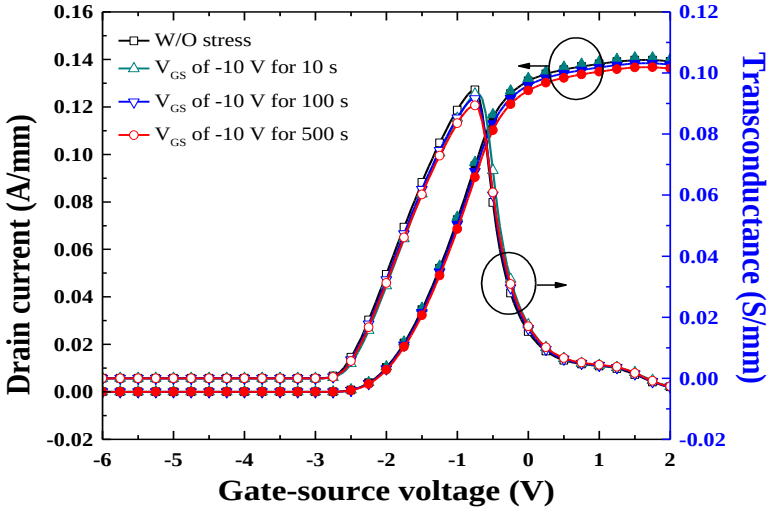


Figure 5-27: Transfer characteristics of AlGaN/GaN HEMTs using multiple Al_2O_3/Ga_2O_3 stacks and SiO_2 passivation with three-different DC stress conditions.

5.7. Summary

In this chapter, I proposed new method to increase breakdown voltage in AlGaN/GaN HEMT-on-SiC substrate using RF-sputtered Ga_2O_3-based thin film. Breakdown voltage was considerably increased because of electron injection from the gate into deep traps in the sputtered Ga_2O_3 passivation layer. The breakdown voltage of Ga_2O_3-passivated HEMTs with a L_{GD} of 20 μm and sputtered at 50, 100, 150, and 200 W were 1430, 890, 820, and 460 V, respectively, while that of an unpassivated sample was 520 V. Breakdown voltage increased with decreasing Ga_2O_3 sputtering power. In addition, breakdown voltage linearly increased with L_{GD} for the Ga_2O_3-passivated HEMTs because electrons injected into deep traps successfully extended the depletion region between the gate and drain. I achieved breakdown voltage of 2730 V using a sputtering power of 50 W and L_{GD} of 40 μm.

In the latter half, 10 nm-thick multiple Al_2O_3/Ga_2O_3 stacks was proposed to improve reverse blocking characteristics in AlGaN/GaN HEMT. The proposed device achieves the high breakdown voltage of 1104 V and V_{TH} of –1.4 V while those of the unpassivated one exhibits 380 and –2 V. The unintentionally formed Ga vacancies in the multiple Al_2O_3/Ga_2O_3 stacks act as accumulation center under gate. I have investigated the effects of charge injection into the multiple Al_2O_3/Ga_2O_3 stacks on the electrical properties of the AlGaN/GaN HEMTs by various measurements such as *C*–*V*, pulse *I*–*V*, and *I*–*V* with DC stress. The charge accumulation induced the improvement of leakage current and breakdown voltage. The suppression of current degradation by final SiO_2 deposition indicated that the charge accumulation in Ga_2O_3 layer is dominant mechanism of the breakdown improvement. The AlGaN/GaN HEMT with the multiple Al_2O_3/Ga_2O_3 stacks is suitable for a high-voltage operation and shows the possibility of normally-off operation.

Chapter 6

6 Conclusion

AlGaN/GaN HEMTs have received a considerable amount of attention for high-power applications due to their wide bandgap properties, such as a high critical electric field, a high thermal conductivity, and a low intrinsic carrier concentration. In addition, an AlGaN/GaN heterostructure offers high-density and high-mobility two-dimensional electron gas (2DEG) by piezoelectric polarization between AlGaN barrier and GaN buffer layer, meaning that AlGaN/GaN HEMTs exhibit a high breakdown voltage and a low on-resistance.

However, the surface leakage current by an electron trapping and trap-assisted tunneling at the Schottky/GaN interface are critical issues in the AlGaN/GaN heterostructure devices. Suppression of the leakage current and high breakdown voltage are indubitably important to achieve a low off-state power loss and high-conversion efficiency without device failure. The MOS is suitable structure for the high-voltage AlGaN/GaN HEMTs because the gate insulator suppresses the leakage current and effectively prevent the parasitic

diodes operation.

The RF-sputtered HfO_2 was studied for uses in the gate insulator of the AlGaN/GaN MOS-HEMTs and sputtering conditions such as sputtering power and working pressure were optimized. The electrical and materials properties of HfO_2 at the various sputtering conditions were verified by X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and Auger electron spectroscopy (AES). Also, the effects of post-deposition annealing (PDA) on the HfO_2 were investigated. The high breakdown voltage in the test pattern including 15 nm-thick HfO_2 on p-type Si substrate was increased from 42 to 78 V after PDA at 900 ^{o}C for 2 hours.

The AlGaN/GaN MOS-HEMT-on-Si using RF-sputtered HfO_2 gate insulator exhibited the high breakdown voltage of 1524 V, the low drain leakage current of 67 pA/mm at V_{DS}= 100 V and V_{GS}= −10 V, and high on/off current ratio of 2.37×10^{10} while the conventional HEMT had 470 V, 192 μA/mm, 7.61×10^{3}, respectively. The improvement mechanism of breakdown voltage through HfO_2 gate insulator was studied by measuring various electrical characteristics. This was done with the separated two-factors including passivation effects and blocking capability of HfO_2 gate insulator. Both forward- and reverse-gate blocking characteristics of the AlGaN/GaN MOS-HEMTs using HfO_2 gate insulator were evaluated. In addition, suppression of electron trapping due to surface passivation was verified by pulsed *I-V* characteristics and capacitance-voltage characteristics. Finally, interface traps density (D_{it}) was evaluated by terman's method and high-frequency capacitance-voltage characteristics so that D_{it} of 6×10^{12} $cm^{-2}\cdot eV^{-1}$ at the energy level of 0.1 eV below conduction energy minimum.

Au-free fabrication is promising technologies for the CMOS-compatible process of the AlGaN/GaN devices. Also, it has an advantage in terms of the fabrication cost and large-wafer process. TaN was proposed to replace the

gold-based electrodes in the AlGaN/GaN MOS-HEMTs-on-Si. The material and electrical properties were verified after PDA by XRD, scanning electron microscopy (SEM), and 4-point probe. Also, the sputtering conditions such as sputtering power and working pressure were optimized to obtain the low-resistance electrode and suppress sputtering damage to HfO_2 gate insulator. The TaN-gate AlGaN/GaN MOS-HEMTs with 15 nm-thick HfO_2 gate insulator showed high on/off current ratio of 4.56×10^{10} and high breakdown voltage of 1460 V at gate-drain distance of 10 μm. Also, the fully Au-free devices using TaN-gate and Ti/Al/TaN-source/drain showed on/off current ratio of 2.0×10^{9} without any considerable degradation.

The extended-gate structure was proposed to reduce specific on-resistance ($R_{on,sp}$) without any additional GaN epitaxial growth and lithography techniques by removing the redundant gate-source space in the AlGaN/GaN MOS-HEMTs-on-Si. The extended TaN-gate overlapped the source with 15 nm-thick HfO_2 insulation. By using this structure, the $R_{on,sp}$ was successfully reduced from 2.91 to 2.28 m$\Omega\cdot$cm^2 in the device with 10 μm-long $L_{GD.}$ High-k characteristics and higher dielectric breakdown voltage of the HfO_2 gate insulator than $|V_{TH}|$ facilitated the stable on/off switching. This device also exhibited high breakdown voltage of 1410 V, high on/off current ratio of 4.97×10^{10}, and high figure-of-merit of 872 MW$\cdot$cm^{-2}.

A new method to increase the breakdown voltage trough RF-sputtered Ga_2O_3 and Al_2O_3 films without any termination structure was proposed. The sputtering power considering sputtering damage to the GaN surface was optimized to suppress the leakage current. An electron injection into the unintentionally formed deep traps in the amorphous Ga_2O_3 films extended depletion region under the gate and increased the breakdown voltage. The deep traps have a relatively long emission time so that the surface leakage current, which originated from the shallow traps, would be suppressed. The

AlGaN/GaN HEMT-on-SiC with 20 μm-long L_{GD} and Ga_2O_3 passivation sputtered at 50, 100, 150, and 200 W exhibited breakdown voltage of 1430, 890, 820, and 460 V, respectively while that of the unpassivated device was 520 V. Also, high breakdown voltage exceeding 2.7 *k*V at sputtering power of 50 W and 40 μm-long L_{GD} was obtained. In addition, Al_2O_3/Ga_2O_3 multiple stacks by RF-sputtering were employed to reduce the leakage current and shift threshold voltage positively in the AlGaN/GaN HEMTs-on-Si. The breakdown voltage in the device using the stacks was increased from 380 to 1104 V and drain leakage current was decreased from 1.8 μA/mm to 33 nA/mm by the electrons accumulation in the stacks. The threshold voltage was shifted from –2 to –1.4 V and this was shifted to 0.12 V after DC stress at V_{GS}= –10 V for 100 s.

I summarized devices structure and electrical characteristics of the proposed devices in this dissertation in Table 6-1 and Table 6-2. This research is meaningful in devices structure aspect. I reported high-quality RF-sputtered HfO_2 gate insulator and a new method using RF-sputtered Ga_2O_3 films to improve breakdown voltage in AlGaN/GaN HEMTs for the first time. In addition, a new method using TaN-based electrodes for Au-free fabrication in AlGaN/GaN power devices. Taking advantages of the proposed methods to improve device performance, I proposed an extended gate structure using RF-sputtered HfO_2 gate insulator and TaN-gate. By this structure, the on-resistance was rather improved with high breakdown voltage.

Table 6-1: Summary of devices structure used in this dissertation.

	Epitaxial structure	Gate	Source/drain	Dimension ($L_G/L_{GS}/L_{GD}$)
A	i-GaN/i-$Al_{0.23}Ga_{0.77}N$/AlN /i-GaN/C-doped GaN (3/20/1/100 nm/3.9 μm)	Ni/Au (30/150 nm)	Ti/Al/Ni/Au (20/80/20/100 nm)	3/3/20 μm
B		TaN (43 nm)	Ti/Al/Ni/Au (20/80/20/100 nm)	3/3/10 μm
C		TaN (43 nm)	Ti/Al/TaN (20/80/100 nm)	3/3/10 μm
D		TaN (43 nm)	Ti/Al/Ni/Au (20/80/20/100 nm)	3/0/10 μm
E	i-GaN/i-$Al_{0.27}Ga_{0.73}N$ /Fe-doped GaN (3/30 nm/3 μm)	Ni/Au (30/150 nm)	Ti/Al/Ni/Au (20/80/20/100 nm)	3/3/20 μm
F	i-GaN/i-$Al_{0.27}Ga_{0.73}N$ /C-doped GaN (4/20 nm/1.7 μm)	Ni/Au (30/150 nm)	Ti/Al/Ni/Au (20/80/20/100 nm)	3/3/20 μm

A: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator (section 3.5)
B: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator and TaN-gate (section 4.4)
C: Au-free AlGaN/GaN-on-Si MOS-HEMT using HfO_2 gate insulator, TaN-gate, and Ti/Al/TaN-source/drain (section 4.5)
D: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator and extended TaN-gate (section 4.6)
E: AlGaN/GaN HEMT-on-SiC using Ga_2O_3 passivation (section 5.5)
F: AlGaN/GaN HEMT-on-Si using Al_2O_3/Ga_2O_3 stacks (section 5.6)

Table 6-2: Summary of electrical characteristics of the proposed devices used in this dissertation.

	Drain leakage current (V_{DS}=100 V)	On current (V_{GS}= 2 V, V_{DS}= 10 V)	Breakdown voltage
A	67 pA/mm (V_{GS}= –10 V)	299 mA/mm	1526 V
B	17 pA/mm (V_{GS}= –10 V)	333 mA/mm	1460 V
C	174 pA/mm (V_{GS}= –10 V)	269 mA/mm	-
D	18 nA/mm (V_{GS}= –4 V)	430 mA/mm	1410 V
E	64 nA/mm (V_{GS}= –10 V)	400 mA/mm	1428 V (20 μm) 2730 V (40 μm)
F	33 nA/mm (V_{GS}= –10 V)	39 mA/mm	1104 V

A: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator (section 3.5)
B: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator and TaN-gate (section 4.4)
C: Au-free AlGaN/GaN-on-Si MOS-HEMT using HfO_2 gate insulator, TaN-gate, and Ti/Al/TaN-source/drain (section 4.5)
D: AlGaN/GaN MOS-HEMT-on-Si using HfO_2 gate insulator and extended TaN-gate (section 4.6)
E: AlGaN/GaN HEMT-on-SiC using Ga_2O_3 passivation (section 5.5)
F: AlGaN/GaN HEMT-on-Si using Al_2O_3/Ga_2O_3 stacks (section 5.6)

Bibliography

[1] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductor for superior high-voltage power devices", in *Proc. Int. Symp. Power Semiconductor and ICs*, 1993.

[2] International Rectifier, "Commerciallization of GaN based Power Devices: An Introduction to GaNpowIR", 2010.

[3] J. L. Hudgins, G. S. Simin, E. Santi and M. A. Khan, "An assessment of wide bandgap semiconductor for power devices", *IEEE Trans. Power Electron.,* vol. 18, no. 3, pp. 907-914, 2003.

[4] B. S. Kang, F. Ren, Y. Irokawa, K. W. Baik, S. J. Pearton, C. -C. Pan, G. -T. Chen, J. -I. Chyi, H. -J. Ko and H. -Y. Lee, "Temperature dependent characteristics of bulk GaN Schottky rectifiers on free-standing GaN substrates", *J. Vac. Scie. Technol. B,* vol. 22, no. 2, pp. 710-714, 2004.

[5] S. Keller, Y. -F. Wu, G. Parish, N. Ziang, J. J. Xu, B. P. Keller, S. P. DenBaars and U. K. Mishra, "Gallium nitride based high power heterojunction field effect transistors: process development and present status at UCSB", *IEEE Trans. Electron Devices,* vol. 48, no. 3, pp. 552-559, 2001.

[6] K. Hirama, T. Koshiba, K. Yohara, H. Takayanagi, S. Yamaguchi, M. Satoh and H. Kawarada, "RF diamond MISFETs using surface accumulation layer", in *Proc. Int. Symp. Power Semiconductor Device and ICs*, 2006.

[7] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors", *RCA Rev,* vol. 26, pp. 163-177, 1965.

[8] B. J. Baliga, "Semiconductor for high-voltage, vertical channel field effect transistors", *J. Appl. Phys,* vol. 53, no. 3, pp. 1759-1764, 1985.

[9] A. Banerjee, S. Taking, D. MacFarlane, A. Dabiran and E. Wasige, "Development of enhancement mode AlGaN/GaN MOS-HEMTs using

localized gate-foot oxidation", in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, 2010.

[10] A. A. Syed and X. A. Cao, "Thermal and plasma damage in AlGaN Schottky diodes", *J. Phys. D: Appl. Phys.,* vol. 42, no. 19, pp. 195105, 2009.

[11] M. Ochiai, M. Akita, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, "AlGaN/GaN Heterostructure Metal-Insulator-Semiconductor High-Electron-Mobility Transistors with Si_3N_4 Gate Insulator", *Jpn. J. Appl. Phys,* vol. 42, no. 4B, pp. 2278-2280, 2003.

[12] J. Shi, L. F. Eastman, X. Xin and M. Pophristic, "High performance AlGaN/GaN power switch with HfO_2 insulation", *Appl. Phys. Lett.,* vol. 95, no. 4, p. 042103 , 2009.

[13] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck and U. K. Mishra, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy", *J. Appl. Phys.,* vol. 86, no. 8, pp. 4520-5426, 1999.

[14] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", *J. Appl. Phys,* vol. 85, no. 6, pp. 3222-3233, 1999.

[15] A. K. Rashmi, S. Haldar and R. S. Gupta, "An accurate charge control model for spontaneous and piezoelectric polarization dependent two-dimensional electron gas sheet charge density of lattice-mismatched AlGaN/GaN HEMTs", *Solid-State Electron*., vol. 46, no. 5, pp. 621-630, 2002.

[16] S. M. Hurrbard, Metalorganic vapor phase peitaxy (MOVPE) Growth and Characterization of III-Nitride Heterostructures for Application in Electronic Devices, Ph. D. Dissertation, Department of Electrical

Engineering, University of Michigan, 2005.

[17] H. Kambayashi, Y. Satoh, Y. Niiyama, T. Kokawa, M. Iwami, T. Nomura, S. Kato and T. Chow, "Enhancement-mode GaN hybrid MOS-HFETs on Si substrates with Over 70 A operation", in *Proc. Int. Symp. Power Semiconductor and ICs*, 2009.

[18] Transphorm, "http://powerelectronics.com/power-electronics-systems/apec-2013-new-product-introductions", 2013. [Online].

[19] B. De Jaeger, M. Van Hove, D. Wellekens, X. Kang, H. Liang, G. Mannaert, K. Geens and S. Decoutere, "Au-free CMOS-compatible AlGaN/GaN HEMT processing on 200 mm Si substrates", in *Proc. Int. Symp. Power Semiconductor and ICs*, 2012.

[20] C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. K. Mishra and J. S. Speck, "Effect of carbon doping on buffer leakage in AlGaN/GaN high electron mobility transistors", *J. Vac. Sci. Technol. B,* vol. 22, no. 3, pp. 1145-1149, 2004.

[21] S. Heikman, S. Keller, S. P. DenBaars and U. K. Mishra, "Growth of Fe doped semi-insulating GaN by metalorganic chemical vapor deposition", *Appl. Phys. Lett.,* vol. 81, no. 3, pp. 439-441, 2002.

[22] V. Desmaris, M. Rudzinski, N. Rorsman, P. R. Hageman, P. K. Larsen, H. Zirath, T. Rodle and H. F. F. Jos, "Comparison of the DC and Microwave Performance of AlGaN/GaN HEMTs Grown on SiC by MOCVD With Fe-Doped or Unintentionally Doped GaN Buffer Layers", *IEEE Trans. Electron Devices,* vol. 53, no. 9, pp. 2413-2417, 2006.

[23] F. Roccaforte, F. Giannazzo, F. Iucolano and V. R. C. Bongiorno, "Electrical behavior of AlGaN/GaN heterostuctures upon high-temperature selective oxidation", *J. Appl. Phys.,* vol. 106, no. 2, pp. 023703 , 2009.

[24] M. Werquin, N. Vellas, Y. Guhel, D. Ducatteau, B. Boudart, J. C. Pesant, Z. Bougrioua, M. Germain, J. C. D. Jaeger and C. Gaquiere, "First results of AlGaN/GaN HEMTs on sapphire substrate using an argon-ion implant-

isolation technology", *Microw. Opt. Technol. Lett. ,* vol. 46, no. 4, pp. 311-315, 2005.

[25] C. Liu, E. F. Chor and L. S. Tan, "Investigations of HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors", *Appl. Phys. Lett.,* vol. 88, no. 17, pp. 173504 , 2006.

[26] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K. J. Duxstad, E. E. Haller, Z.-F. Fan, S. N. Mohammad, W. Kim, A. E. Botchkarev and H. Morkoc, "Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for n-GaN", *Appl. Phys. Lett.,* Vols. 1556-1558, no. 11, pp. 69, 1996.

[27] T. Kikkawa, "Highly Reliable 250 W GaN High Electron Mobility Transistor Power Amplifier", *Jpn. J. Appl. Phys.,* vol. 44, no. 7A, pp. 4896-4901, 2005.

[28] S. Ashida, M. R. Shim and M. A. Lieberman, "Measurements of pulsed-power modulated argon plasmas in an inductively coupled plasma source", *J. Vac. Sci. Technol. A,* vol. 14, no. 2, pp. 391-397, 1996.

[29] M. Goto, H. Toyoda, M. Kitagawa, T. Hirao and H. Sugai, "Low Temperature Growth of Amorphous and Polycrystalline Silicon Films from a Modified Inductively Coupled Plasma", *Jpn. J. Appl. Phys,* vol. 36 , no. 6A, pp. 3714-3720, 1997.

[30] N. Miura, T. Nanjo, M. Suita, T. Oishi, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa and T. Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal", *Solid-State Electron.,* vol. 48, no. 5, pp. 689-695, 2004.

[31] H. Kim, J. Lee, D. Liu and W. Lu, "Gate current leakage and breakdown mechanism in unpassivated AlGaN/GaN high electron mobility transistors by post-gate annealing", *Appl. Phys. Lett.,* vol. 86, no. 14, pp. 143505, 2005.

[32] W. Lu, V. Kumar, R. Schwindt, E. Piner and I. Adesida, "A comparative study of surface passivation on AlGaN/GaN HEMTs", *Solid-State*

Electron., vol. 46, no. 9, pp. 1441-1444, 2002.

[33] A. P. Zhang, J. W. Johnson, F. Ren, J. Han, A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, J. M. Redwing, K. P. Lee and S. J. Pearton, "Lateral $Al_xGa_{1-x}N$ power rectifiers with 9.7 *k*V reverse breakdown voltage", *Appl. Phys. Lett.,* vol. 78, no. 6, pp. 823-825, 2001.

[34] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller and U. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates", *IEEE Electron Device Lett.,* vol. 25, no. 4, pp. 161-163, 2004.

[35] R. Vetury, N.-Q. Zhang, S. Keller and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs", *IEEE Trans. Electron Devices,* vol. 48, no. 3, pp. 560-566, 2001.

[36] B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy and L. F. Eastman, "effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs", *IEEE Electron Device Lett.,* vol. 21, no. 6, pp. 268-270, 2000.

[37] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs", *IEEE Trans. Electron Devices,* vol. 51, no. 10, pp. 1554-1561, 2004.

[38] S.-Y. Huang and J.-R. Yang, "A Transmission Electron Microscopy Observation of Dislocations in GaN Grown on (0001) Sapphire by Metal Organic Chemical Vapor Deposition", *Jpn. J. Appl. Phys.,* vol. 47, no. 10, pp. 7998-8002, 2008.

[39] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors", *Appl. Phys. Lett.,* vol. 77, no. 2, pp. 250-252, 2000.

[40] T. Sawada, N. Kimura, K. Imai, K. Suzuki and K. Tanahashi, "Interpretation of current transport properties at Ni/n-GaN Schottky interfaces", *J. Vac. Sci. Technol. B,* vol. 22, no. 4, pp. 2051-2088, 2004.

[41] Y. Ohno, T. Nakao, S. Kishimoto and K. Maezawa, "Effects of surface passivation on breakdown of AlGaN/GaN high-electron-mobility transistors", *Appl. Phis. Lett,* vol. 84, no. 12, pp. 2184-2186, 2004.

[42] Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara and M. Kuzuhara, "A 110-W AlGaN/GaN heterojunction FET on thinned sapphire substrate", in *Int. Electron Devices Meet. Tech. Dig.*, 2001.

[43] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo and Y. Sano, "Surface passivation effects on AlGaN/GaN high-electron-mobility transistors with SiO_2, Si_3N_4, and silicon oxynitride", *Appl. Phys. Lett.,* vol. 84, no. 4, pp. 613-615, 2004.

[44] M.-W. Ha, Y.-H. Choi, J. Lim, J.-H. Park, S.-S. Kim, C.-M. Yun and M.-K. Han, "Hot-Carrier-Stress-Induced Degradation of 1 *K*V AlGaN/GaN HEMTs by Employing SiO_2 Passivation", in *Proc. Int. Symp. Power Semiconductor Device and ICs*, 2007.

[45] W.-K. Wang, C.-H. Lin, P.-C. Lin, C.-K. Lin, F.-H. Huang, Y.-J. Chan, G.-T. Chen and J.-I. Chyi, "Low-*k* BCB passivation on AlGaN-GaN HEMT fabrication", *IEEE Electron Device Lett.,* vol. 25, no. 12, pp. 763-765, 2004.

[46] B. Luo, J. W. Johnson, J. Kim, R. M. Mehandru, F. Ren, B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier and J. Han, "Influence of MgO and Sc_2O_3 passivation on AlGaN/GaN high-electron-mobility transistors", *Appl. Phys. Lett.,* vol. 80, no. 9, pp. 1661-1663, 2002.

[47] M. Hampson, S.-C. Shen, R. Schwindt, R. Price, U. Chowdhury, M. Wong, T. G. Zhu and D. Yoo, "Polyimide passivated AlGaN-GaN HFETs with 7.65 W/mm at 18 GHz", *IEEE Electron Device Lett.,* vol. 25, no. 5, pp. 238-240, 2004.

[48] W. Frensley, "Power-limiting breakdown effects in GaAs MESFET's", *IEEE Trans. Electron Devices,* vol. 28, no. 8, pp. 962-970, 1981.

[49] S. Karmalkar, M. Shur, G. Simin and M. A. Khan, "Field-plate engineering

for HFETs", *IEEE Trans. Electron Devices,* vol. 52, no. 12, pp. 2534-2540, 2005.

[50] M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka and D. Ueda, " Recent advances in GaN transistors for future emerging applications", *phys. stat. sol. (a),* vol. 206, no. 6, pp. 1221-1227, 2009.

[51] A. Nakajima, M. Dhyani, E. M. S. Narayanan, Y. Sumida and H. Kawai, "GaN based Super HFETs over 700 V using the polarization junction concept", in *Proc. Int. Symp. Power Semiconductor and ICs*, 2011.

[52] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. DenBaars and U. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates", *IEEE Electron Device Lett.,* vol. 27, no. 9, pp. 713-715, 2006.

[53] J. Würfl, E. B. Treidel, F. Brunner, M. Cho, O. Hilt, A. Knauer, P. Kotara, O. Krueger, M. Weyers and R. Zhytnytska, "Device Breakdown and Dynamic effects in GaN Power Switching Devices: Dependencies on Material Properties and Device Design", *ECS Trans.,* vol. 50, no. 3, pp. 211-222, 2013.

[54] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl and G. Trankle, "AlGaN/GaN/GaN:C Back-Barrier HFETs With Breakdown Voltage of Over 1 *k*V and Low R_{on}-*A*", *IEEE Trans. Electron Devices,* vol. 57, no. 11, pp. 3050-3058, 2010.

[55] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel and J. Würfl, "Normally-off AlGaN/GaN HFET with p-type GaN gate and AlGaN buffer", in *Int. Conf. Integrated Power Electronics Systems*, 2010.

[56] B. Lu and T. Palacios, "High Breakdown (>1500 V) AlGaN/GaN HEMTs by Substrate-Transfer Technology", *IEEE Electron Device Lett.,* vol. 31, no. 9, pp. 951-953, 2010.

[57] P. Srivastava, J. Das, D. Visalli, M. Van Hove, P. E. Malinowski, D. Marcon, S. Lenci, K. Geens, K. Cheng, M. Leys, S. Decoutere, R. Mertens and G. Borghs, "Record Breakdown Voltage (2200 V) of GaN DHFETs on Si

With 2-*u*m Buffer Thickness by Local Substrate Removal", *IEEE Electron Device Lett.,* vol. 32, no. 1, pp. 30-32, 2011.

[58] T. Nomura, H. Kambayashi, M. Masuda, S. Ishii, N. Ikeda, J. Lee and S. Yoshida, "High Temperature Operation AlGaN/GaN HFET with a low on-state resistance, a high breakdown voltage and a fast switching capacity", in *Proc. Int. Symp. Power Semiconductor*, 2006.

[59] T. Uesugi, T and Kachi, "Which are the Future GaN Power Devices for Automotive Applications, Lateral Structures or Vertical Structures?", in *Int. Conf. Compound Semiconductor Manufacturing Technology*, 2011.

[60] Y.-H. Choi, J. L. Y.-S. K. O. S. M. K. and M.-K. Han, "High voltage AlGaN/GaN High-Electron-Mobility Transistors (HEMTs) employing oxygen annealing", in *Proc. Int. Symp. Power Semiconductor Device and ICs*, 2010.

[61] N. Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang and T. P. Ma, "Effects of surface traps on breakdown voltage and switching speed of GaN", in *Int. Electron Devices Meet. Tech. Dig.*, 2001.

[62] E. Bahat-Treidel, O. Hilt, F. Brunner, V. Sidorov, J. Würfl and G. Tränkle, "AlGaN/GaN/AlGaN DH-HEMTs Breakdown Voltage Enhancement Using Multiple Grating Field Plates (MGFPs)", *IEEE Trans. Electron Devices,* vol. 57, no. 6, pp. 1208-1216, 2010.

[63] J. W. P. Hsu, M. J. Manfra, R. J. Molnar, B. Heying and J. S. Speck, "Direct imaging of reverse-bias leakage through pure screw dislocations in GaN films grown by molecular beam epitaxy on GaN templates", *Appl. Phys. Lett.,* vol. 81, no. 1, pp. 79-81, 2002.

[64] C.-T. Lee, Y.-L. Chiou and C.-S. Lee, "AlGaN/GaN MOS-HEMTs With Gate ZnO Dielectric Layer", *IEEE Electron Device Lett.,* vol. 31, no. 11, pp. 1220-1223, 2010.

[65] S. Huang, S. Yang, J. Roberts and K. J. Chen, "Threshold Voltage Instability in Al_2O_3/GaN/AlGaN/GaN Metal–Insulator–Semiconductor High-Electron Mobility Transistors", *Jpn. J. Appl. Phys,* vol. 50, pp.

110202, 2011.

[66] C. Zhou, W. Chen, E. Piner and K. Chen, "Schottky-Ohmic Drain AlGaN/GaN Normally Off HEMT With Reverse Drain Blocking Capability", *IEEE Electron Device Lett.,* vol. 31, no. 7, pp. 668-670, 2010.

[67] B. Gil, "Chapter 1", in *Group III Nitride Semiconductor Compounds-Physics and Applications*, Clatendon Press Oxford, 1998.

[68] S. C. Vitkavage, E. A. Irene and H. Z. Massoud, "An Investigation of Si-SiO_2 Interface Charges in Thermal Oxidized (100), (110), (111), (511) Silicon", *J. Appl. Phys.,* vol. 68, no. 5262, pp. 1-31, 1990.

[69] C.-T. Lee, H.-Y. Lee and H.-W. Chen, "GaN MOS Device Using SiO_2-Ga_2O_3 Insulator Grown by Photoelectrochemical oxidation Method", *IEEE Electron Device Lett.,* vol. 24, no. 2, pp. 54-56, 2003.

[70] H.-Y. Liu, B.-Y. Chou, W.-C. Hsu and C.-S. Lee, "A Simple Gate-Dielectric Fabrication Process for AlGaN/GaN Metal–Oxide–Semiconductor High-Electron-Mobility Transistors", *IEEE Electron Device Lett.,* vol. 33, no. 7, pp. 997-999, 2012.

[71] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al_2O_3 as gate dielectric", *Appl. Phys. Lett.,* vol. 86, no. 6, pp. 063501, 2005.

[72] N. Pala, R. Gaska, S. Rumyantsev, M. Shur, M. Khan, X. Hu, G. Simin and J. Yang, "Low-frequency noise in AlGaN/GaN MOS-HFETs", *Electron. Lett.,* vol. 36, no. 3, pp. 268-270, 2000.

[73] V. Adivarahan, J. Yang, A. Koudymov, G. Simin and M. A. Khan, "Stable CW operation of field-plated GaN-AlGaN MOSHFETs at 19 W/mm", *IEEE Electron Device Lett.,* vol. 26, no. 8, pp. 535-537, 2005.

[74] M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo and K. Joshin, "An over 100 W n-GaN/n-AlGaN/GaN MIS-HEMT power amplifier for wireless base station applications", in *Int Electron Devices Meet. Tech.*

Dig, 2005.

[75] M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada and N. Hara, "Enhancement-Mode GaN MIS-HEMTs With n-GaN/i-AlN/n-GaN Triple Cap Layer and High-*k* Gate Dielectrics", *IEEE Electron Device Lett.,* vol. 31, no. 3, pp. 189-191, 2010.

[76] P. Kordos, D. Gregusova, R. Stoklas, K. CiCo and J. Novak, "Improved transport properties of Al_2O_3/AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistor", *Appl. Phys. Lett.,* vol. 90, no. 12, pp. 123513, 2007.

[77] Z. H. Liu, G.-I. Ng, S. Arulkumaran, Y. K. T. Maung and K. L. Teo, "High Microwave-Noise Performance of AlGaN/GaN MISHEMTs on Silicon With Al_2O_3 Gate Insulator Grown by ALD", *IEEE Electron Device Lett.,* vol. 31, no. 2, pp. 96-98, 2010.

[78] Z. Liu, G. Ng, S. Arulkumaran, Y. K. T. Maung, K. Teo, S. C. Foo and V. Sahmuganathan, "Improved Linearity for Low-Noise Applications in 0.25-*u*m GaN MISHEMTs Using ALD Al_2O_3 as Gate Dielectric", *IEEE Electron Device Lett.,* vol. 31, no. 8, pp. 803-805, 2010.

[79] J. J. Freedsman, S. L. S. T. Kubo and T. Egawa, "Suppression of Gate Leakage and Enhancement of Breakdown Voltage Using Thermally Oxidized Al Layer as Gate Dielectric for AlGaN/GaN Metal–Oxide–Semiconductor High-Electron-Mobility Transistors", *Jpn. J. Appl. Phys.,* vol. 50, no. 4, pp. 04DF03, 2011.

[80] K. Balachander, S. Arulkumaran, H. Ishikawa, K. Baskar and T. Egawa, "Studies on electron beam evaporated ZrO_2/AlGaN/GaN metal–oxide–semiconductor high-electron-mobility transistors", *phys. stat. sol. (a),* vol. 202, no. 2, pp. R16-R18, 2005.

[81] S. Sugiura, S. Kishimoto, T. Mizutani, M. Kuroda, T. Ueda and T. Tanaka, "Normally-off AlGaN/GaN MOSHFETs with HfO_2 gate oxide", *Phys. phys. stat. sol. (c),* vol. 5, no. 6, pp. 1610-1642, 1923-1925.

[82] L. J. Meng and M. D. Santos, "Direct current reactive magnetron

sputtered zinc oxide thin films-the effect of the sputtering pressure", *Thin Solid Films,* vol. 250, no. 1-2, pp. 26-32, 1994.

[83] U. Schürmann, H. Takele, V. Zaporojtchenko and F. Faupel, "Optical and electrical properties of polymer metal nanocomposites prepared by magnetron co-sputtering", *Thin Solid Films,* vol. 515, no. 2, pp. 801-804, 2006.

[84] J. Niinisto, M. Putkonen, L. Niinisto, S. L. Stoll, K. Kukli, T. Sajavaara, M. Ritala and M. Leskela, "Controlled growth of HfO_2 thin films by atomic layer deposition from cyclopentadienyl-type precursor and water", *J. Mater. Chem.,* vol. 15, no. 23, pp. 2271-2275, 2005.

[85] D. A. Sanchez, "TUTORIAL ON SPUTTER DEPOSITION", *MATERION ADVANCED CHEMICALS-COATING MATERIALS NEWS,* pp. 1-6, 2 21 2011.

[86] M. Eickelkamp, D. Fahle, J. Lindner, M. Heuken, C. Lautensack, H. Kalisch, R. H. Jansen and A. Vescan, "Impact of gate dielectric thickness on the electrical properties of AlGaN/GaN MISHFETs on Si(111) substrate", *phys. stat. sol. (a),* vol. 207, no. 6, pp. 1342-1344, 2010.

[87] W. J. Choi, E. J. Lee, K. S. Yoon, J. Y. Yang, J. H. Lee, C. O. Kim and J. P. Hong, "Annealing Effects of HfO_2 Gate Thin Films Formed by Inductively Coupled Sputtering Technique at Room Temperature", *J. Korean Phys. Soc.,* vol. 45, no. 96, pp. S716-S719, 2004.

[88] S. Kim, S. Woo, H. Kim, I. Kim, k. Lee, W. Jeong, Y. Park and H. Jeon, "Atomic Layer Deposition of HfO_2 Thin Films on Ultrathin SiO_2 Fomred by Remote Plasma Oxidation", *J. Korean Phys. Soc.,* vol. 52, no. 4, pp. 1103-1108, 2008.

[89] T. L. Duan, H. Y. Yu, L. Wu, Z. R. Wang, Y. L. Foo and J. S. Pan, "Investigation of HfO_2 high-*k* dielectrics electronic structure on SiO_2/Si substrate by x-ray photoelectron spectroscopy", *Appl. Phys. Lett.,* vol. 99, no. 1, pp. 012902, 2011.

[90] S.-W. Do, Y.-H. Lee and J.-S. Lee, "Study of the Characteristics of HfO_2/Hf

Films Prepared by Atomic Layer Deposition on Silicon", *J. Korean Phys. Soc.,* vol. 50, no. 3, pp. 666-669, 2007.

[91] H. Kim, P. C. McIntyre and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition", *Appl. Phys. Lett.,* vol. 82, no. 1, pp. 106-108, 2003.

[92] P. Tirmali, A. G. Khairnar, B. N. Joshi and A. Mahajan, "Structural and electrical characteristics of RF-sputtered HfO_2 high-*k* based MOS capacitors", *Solid-State Electron.,* vol. 62, no. 1, pp. 44-47, 2011.

[93] Y. Cai, Y. Zhou, K. M. Lau and K. Chen, "Control of Threshold Voltage of AlGaN/GaN HEMTs by Fluoride-Based Plasma Treatment: From Depletion Mode to Enhancement Mode", *IEEE Trans. Electron Devices,* vol. 53, no. 9, pp. 2207-2215, 2006.

[94] M. Lee, Y. Ryoo, J. -G. Lee, H. -Y. Cha and K. Seo, "Prepassivated AlGaN/GaN HEMTs with improved edge acuity in annealed ohmic contacts", *Electron. Lett.,* vol. 47, no. 12, pp. 725-726, 2011.

[95] W. Huang, T. Khan and T. P. Chow, "Comparison of MOS Capacitors on n- and p-Type GaN", *J. Electron. Mater.,* vol. 35, no. 4, pp. 726-732, 2006.

[96] A. Wang, M. J. Tadjer and F. Calle, "Simulation of thermal management in AlGaN/GaN HEMTs with integrated diamond heat spreaders", *Semicond. Sci. Technol,* vol. 28, no. 5, pp. 055010, 2013.

[97] O. Seok, W. Ahn, M.-K. Han and M.-W. Ha, "High on/off current ratio AlGaN/GaN MOS-HEMTs employing RF-sputtered HfO_2 gate insulator", *Semicond. Sci. Technol.,* vol. 28, no. 2, pp. 025001, 2013.

[98] L. Pang and K. Kim, "Bimodal gate-dielectric deposition for improved performance of AlGaN/GaN metal–oxide–semiconductor high-electron-mobility transistors", *J. Phys. D: Appl. Phys.,* vol. 45, no. 4, pp. 045105, 2012 .

[99] F. A. Khanz, V. Kumar and I. Adesida, "Inductively Coupled Plasma-Induced Damage in AlGaN/GaN HEMTs", *Electrochem. Solid-State Lett.,*

vol. 5, no. 2, pp. G8-G9, 2002.

[100] W. D. Hu, X. S. Chen, Z. J. Quan, X. M. Zhang and Y. Huang, "Simulation and optimization of GaN-based metal-oxide-semiconductor high-electron-mobility-transistor using field-dependent drift velocity model", *J. Appl. Phys.,* vol. 102, no. 3, pp. 034502, 2007.

[101] S. Binari, P. Klein and T. Kazior, "Trapping effects in GaN and SiC microwave FETs", *Proceedings of the IEEE,* vol. 90, no. 6, pp. 1048-1058, 2002.

[102] W. S. Tan, P. A. Houston, P. J. Parbrook, D. A. Wood, G. Hill and C. R. Whitehouse, "Gate leakage effects and breakdown voltage in metalorganic vapor phase epitaxy AlGaN/GaN heterostructure field-effect transistors", *Appl. Phys. Lett.,* vol. 80, no. 17, pp. 3207, 2002.

[103] F. Ren, A. Zhang, G. Dang, X. Cao, H. Cho, S. Pearton, J.-I. Chyi, C.-M. Lee and C.-C. Chuo, "Surface and bulk leakage currents in high breakdown GaN rectifiers", *Solid-State Electron.,* vol. 44, no. 1, pp. 619-622, 4 2004.

[104] A. F. Wright, "Substitutional and interstitial carbon in wurtzite GaN", *J. Appl. Phys,* vol. 92, no. 5, pp. 2575-2585, 2002.

[105] C. H. Seager, A. F. Wright, J. Yu and W. Gotz, "Role of carbon in GaN", *J. Appl. Phys.,* vol. 92, no. 11, pp. 6553-6560, 2002.

[106] C. P. Baylis, II and L. P. Dunleavy, "Understanding pulsed *IV* measurement", in *Int. Conf. Electron Devices for Microwave and Optoelectronic Applications*, 2003.

[107] C. Mizue, Y. Hori, M. Miczek and T. Hashizume, "Capacitance–Voltage Characteristics of Al_2O_3/AlGaN/GaN Structures and State Density Distribution at Al_2O_3/AlGaN Interface", *Jpn. J. Appl. Phys,* vol. 50, pp. 021001, 2011.

[108] D. A. Deen and J. G. Champlain, "High frequency capacitance-voltage technique for the extraction of interface trap density of the heterojunction capacitor: Terman's method revised", *Appl. Phys. Lett.,*

vol. 99, no. 5, pp. 053501-1-503501-3, 2011.

[109] M. Miczek, C. Mizue, T. Hashizume and B. Adamowicz, "Effects of interface states and temperature on the *C-V* behavior of metal/insulator/AlGaN/GaN heterostructure capacitors", *J. Appl. Phys.,* vol. 103, no. 10, pp. 104510-1-104510-11, 2008.

[110] V. Bermudez, C. I. Wu and A. Kahn, "AlN films on GaN: Sources of error in the photoemission measurement of electron affinity", *J. Appl. Phys.,* vol. 89, no. 3, pp. 1991, 2001.

[111] J. I. Pankove and H. Schade, "Photoemission from GaN", *Appl. Phys. Lett,* vol. 25, no. 1, pp. 53-55, 1974.

[112] I. Vurgaftman and J. R. Meyer, "Band parameters for nitrogen-containing semiconductors", *J. Appl. Phys.,* vol. 94, no. 6, pp. 3675-3676, 2003.

[113] S. M. Sze, Physics of Semiconductor Device, 2nd ed., New York: Wiley, 1981.

[114] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications", *IEEE Electron Device Lett.,* vol. 10, no. 10, pp. 455-457, 1989.

[115] P. Hower, S. Pendharkar and T. Efland, "Current status and future trends in silicon power devices", in *Int. Electron Devices Meet. Tech. Dig.*, 13.1.1-13.1.4, 2010.

[116] M. Ogasawara, S. Kodama, H. Tokuda and M. Kuzuhara, "Effects of ohmic metal thickness on drain current capability of AlGaN/GaN HEMTs", in *Int. Conf. Future of Electron Devices*, 2012.

[117] Y. Uemoto, T. Ueda, T. Tanaka and D. Ueda, "Recent advanced of high AlGaN/GaN power HFETs", in *SPIE 7216, Gallium Nitride Materials and Devices IV*, 2009.

[118] C.-J. Youn and K.-Y. Kang, "Low-Resistance Ohmic Contacts to AlGaN/GaN Heterostructure Using Si/Ti/Al/Cu/Au Multilayer Metal

Scheme", *Jpn. J. Appl. Phys.,* vol. 39, no. 7A, pp. 3955-3956, 2000.

[119] H.-S. Lee, D. S. Lee and T. Palacios, "AlGaN/GaN High-Electron-Mobility Transistors Fabricated Through a Au-Free Technology", *IEEE Electron Device Lett.,* vol. 32, no. 5, pp. 623-625, 2011.

[120] O. Saadat, J. Chung, E. Piner and T. Palacios, "Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications", *IEEE Electron Device Lett.,* vol. 30, no. 12, pp. 1254-1256, 2009.

[121] H.-C. Chiu, C.-W. Lin, H.-L. Kao, G.-Y. Lee, J.-I. Chyi, H.-W. Chuang, K.-J. Chang and Y.-T. Gau, "A gold-free fully copper metalized AlGaN/GaN power HEMTs on Si substrate", *Microelectron. Reliab.,* vol. 52, no. 11, pp. 2556-2560, 2012.

[122] T. Oku, E. Kawakami, M. Uekubo, K. Takahiro, S. Yamaguchi and M. Murakami, "Diffusion barrier property of TaN between Si and Cu", *Appl. Surf. Sci.,* vol. 99, no. 4, pp. 265-272, 1996.

[123] X. Liu, C. Zhan, K. W. Chan, W. Liu, L. S. Tan, K. J. Chen and Y.-C. Yeo, "AlGaN/GaN-on-Silicon Metal–Oxide–Semiconductor High-Electron-Mobility Transistor with Breakdown Voltage of 800 V and On-State Resistance of 3 mohm-cm^2 Using a Complementary Metal–Oxide–Semiconductor Compatible Gold-Free Process", *Appl. Phys. Express,* vol. 5, no. 6, pp. 066501-1-066501-4, 2012.

[124] C. S. Kang, H.-J. Cho, Y. H. Kim, R. Choi, K. Onishi, A. Shahriar and J. C. Lee, "Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications", *J. Vac. Sci. Technol. B,* vol. 21, no. 5, pp. 2026-2028, 2003.

[125] M. Chuang, "ITO Films Prepared by Long-throw Magnetron Sputtering without Oxygen Partial Pressure", *J. Mater. Sci. Technol.,* vol. 26, no. 7, pp. 577-583, 2010.

[126] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. DenBaars and U. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers", *IEEE Electron Device Lett.,* vol. 27, no. 1, pp. 13-15,

2006.

[127] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain and G. Borghs, "Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate", *IEEE Electron Device Lett.,* vol. 31, no. 2, pp. 111-113, 2010.

[128] O. Seok, W. Ahn, M.-K. Han and M.-W. Ha, "High-breakdown voltage and low on-resistance AlGaN/GaN on Si MOS-HEMTs employing an extended TaN gate on HfO_2 gate insulator", *Electron. Lett.,* vol. 49, no. 6, pp. 245-247, 2013.

[129] T. Hashizume, J. Kotani and H. Hasegawa, "Leakage mechanism in GaN and AlGaN Schottky interfaces", *Appl. Phys. Lett.,* vol. 84, no. 24, pp. 4884-4886, 2004.

[130] S. K. Hong, K. H. Shim and J. Yang, "Reduced gate leakage current in AlGaN/GaN HEMT by oxygen passivation of AlGaN surface", *Electron. Lett.,* vol. 44, no. 18, pp. 1091-1092, 2008.

[131] W. J. Ha, S. Chhajed, S. J. Oh, S. Hwang, J. K. Kim, J.-H. Lee and K.-S. Kim, "Analysis of the reverse leakage current in AlGaN/GaN Schottky barrier diodes treated with fluorine plasma", *Appl. Phys. Lett.,* vol. 100, no. 13, pp. 132104, 2012.

[132] O. Seok, Y.-S. Kim, J. Lim and M.-K. Han, "Effect of oxygen annealing temperature on AlGaN/GaN HEMTs", in *Proc. Int. Symp. Power Semiconductor and ICs*, 2011.

[133] W. Ahn, O. Seok, S. M. Song, M.-K. Han and M.-W. Ha, "High-performance AlGaN/GaN High-electron-mobility transistors employing H_2O annealing", *J. Cryst. Growth,* 2013.

[134] G.-S. Park, W.-B. Choi, J.-M. Kim, Y. C. Choi, Y. H. Lee and C.-B. Lim, "Structural investigation of gallium oxide (β-Ga_2O_3) nanowires grown by arc-discharge", *J. Cryst. Growth,* vol. 220, no. 4, pp. 494-500, 2000.

[135] O. Seok, W. Ahn, M.-K. Han and M.-W. Ha, "Effect of Ga_2O_3 sputtering power on breakdown voltage of AlGaN/GaN high-electron-mobility

transistors", *J. Vac. Sci. Technol. B,* vol. 31, no. 1, pp. 011203, 2013.

[136] L.-C. Tien, W.-T. Chen and C.-H. Ho, "Enhanced Photocatalytic Activity in β-Ga_2O_3 Nanobelts", *J. Am. Ceram. Soc.,* vol. 94, no. 9, pp. 3117-3122, 2011.

[137] U. Rambabu, N. R. Munirathnam, T. L. Prakash, B. Vengalrao and S. Buddhudu, "Synthesis and characterization of morphologically different high purity gallium oxide nanopowders", *J. Mater. Sci.,* vol. 42, no. 22, pp. 9262-9266, 2007.

[138] S. J. Chang, C. H. Lan, J. D. Hwang, Y. C. Cheng, W. J. Lin, J. C. Lin and H. Z. Chen, "Sputtered Indium-Tin-Oxide on p-GaN", *J. Electrochem. Soc.,* vol. 155, no. 2, pp. H140-H143, 2008.

[139] M. Ye, Z. Liu, P. Ding, S. Hung and K. Ahmed, "Study of metal gate deposition by magnetron sputtering", *J. Vac. Sci. Technol. B,* vol. 24, no. 5, pp. 2214-2219, 2006.

[140] O. Fathallaha, M. Gassoumia, B. Grimberta, C. Gaquièrea and H. Maarefa, "Parasitic effects and traps in AlGaN/GaN HEMT on sapphire substrate", *Eur. Phys. J. Appl. Phys.,* vol. 51, no. 01, pp. 10304-10308, 2010.

[141] O. Seok, W. Ahn, M.-K. Han and M.-W. Ha, "New AlGaN/GaN High Electron Mobility Transistors Employing Charge Accumulation in Multiple Al_2O_3/Ga_2O_3 Stacks", *Jpn. J. Appl. Phys.,* vol. 51, pp. 101001, 2012.

[142] J. Joh and J. d. Alamo, "A Current-Transient Methodology for Trap Analysis for GaN High Electron Mobility Transistors", *IEEE Trans. Electron Devices,* vol. 58, no. 1, pp. 132-140, 2011.

초 록

본 논문에서는 AlGaN/GaN 전력소자의 누설전류와 항복전압 특성의 개선을 위한 방법으로 RF-스퍼터링 게이트 절연막을 제안하였다. 또한, RF-스퍼터링에 의해 증착된 박막의 재료적, 전기적 특성과 함께 절연막/GaN의 계면 특성을 분석하였다. 그리고, 소자의 전기적 특성을 향상시키기 위한 새로운 구조를 제안하고, 제작과 분석을 통해 검증하였다.

최근, AlGaN/GaN HEMTs는 높은 임계전계와 높은 열전도도, 낮은 진성캐리어 농도 특성과 함께 활발하게 연구가 진행되고 있다. 또한, AlGaN/GaN 이종접합은 높은 전자 이동도와 농도를 갖는 2DEG 채널층을 형성하여 Si 소자 대비 매우 낮은 온-저항을 보인다. 따라서, AlGaN/GaN HEMTs는 차세대 전력반도체로 적합하다고 할 수 있다.

하지만, AlGaN/GaN 이종접합에서의 전자트래핑과 쇼트키/GaN 계면에서의 전자 터널링은 표면 누설전류를 유발하여 여전히 해결되어야 될 문제점으로 남아있다. 누설전류의 억제와 항복전압의 증가는 오프 상태의 전력손실과 높은 전력변환 효율을 위해 매우 중요하다. MOS 구조는 게이트 절연막이 효과적으로 표면 누설전류를 억제하고, AlGaN/GaN HEMTs의 게이트-소스, 게이트-드레인의 기생 다이오드의 동작을 억제하는데 유용하다.

RF-스퍼터링 HfO_2를 AlGaN/GaN MOS-HEMTs의 게이트 절연막으로의 적용을 제안하였으며, 압력과 스퍼터링 전력 등의 스퍼터링 조건을 최적화함으로써 우수한 절연특성을 확보하였다. 또한,

다양한 스퍼터링 조건에서 증착된 HfO_2 게이트 절연막의 재료적, 전기적 특성의 분석을 위해, XRD, XPS, AES 측정을 하였다. 그리고, 후처리 열공정의 효과도 함께 분석하였다. p-type Si 기판 위에 증착된 15 nm 두께의 HfO_2는 900 °C에서 2시간의 어닐링 이후 항복전압은 42 V에서 78 V로 증가함을 확인하였다.

RF-스퍼터링에 의한 HfO_2를 적용한 AlGaN/GaN MOS-HEMTs-on-Si은 1524 V의 높은 항복전압과 함께 V_{DS}= 100 V, V_{GS}= -10 V 기준에서 67 pA/mm의 낮은 드레인 누설전류, 2.37×10^{10}의 높은 온/오프 전류비를 보였다. 반면에, 게이트 절연막이 없는 AlGaN/GaN HEMTs의 경우 470 V의 항복전압과 192 μA/mm의 드레인 누설전류, 7.61×10^{3}의 온/오프 전류비를 보였다. HfO_2 게이트 절연막을 적용한 AlGaN/GaN MOS-HEMTs 소자에서의 항복전압 증가 매커니즘을 분석하기 위하여 다양한 전기적 특성을 분석하였다. 항복전압 증가의 원인을 표면 패시베이션 효과와 게이트 누설전류의 차단 특성의 두 가지 효과로 나누어서 분석하였다. 게이트-드레인 MOS 다이오드에서 순방향과 역방향 차단 특성 모두 크게 향상되었고, 펄스 I-V와 C-V 특성을 통해 평가된 전자 트래핑 현상 또한 효과적으로 억제되었음을 확인하였다. 마지막으로, 고주파 C-V 특성을 사용하는 Terman 방법으로 계면전하밀도 (D_{it})를 추출하였다. 전도대로부터 0.1 eV 아래에서 6×10^{12} $cm^{-2}\cdot eV^{-1}$ 의 양호한 수준의 계면전하밀도 값을 확보하였다.

골드-프리 공정의 AlGaN/GaN 소자와 CMOS 공정의 호환성을 위해서 매우 유망한 기술이다. 골드-프리 공정은 CMOS 공정과 함께 공정 단가를 획기적으로 줄일 수 있으므로 미래 전력반도체 산업에서 더욱 중요성이 부각될 것이다. 본 논문에서는 AlGaN/GaN MOS-

HEMTs-on-Si에서 골드 기반의 전극을 대체하기 위한 목적으로 TaN을 제안하였다. 재료적, 전기적 특성의 분석을 위해서 후처리 열공정 전과 후의 XRD, SEM, 4 point probe를 통한 분석을 하였다. 또한, 낮은 전극 저항과, 하부층인 AlGaN/GaN 이종접합구조의 스퍼터링 데미지를 줄이기 위해서 스퍼터링 파워와 압력 등을 최적화하였다. TaN 게이트를 Ni/Au 대신 적용한 AlGaN/GaN MOS-HEMTs는 10 μm의 게이트-드레인 거리에서 4.56×10^{10}의 높은 온/오프 전류비와 1460 V의 항복전압을 보였으며, 게이트와 함께 Ti/Al/TaN을 소스와 드레인을 적용한 소자는 2.0×10^{10} 의 온/오프 전류비를 보였다.

다음으로는 별도의 GaN 성장기술과 사진공정 없이 AlGaN/GaN MOS-HMETs-on-Si의 온-저항($R_{on,sp}$)을 감소시키기 위한 방법으로 게이트-소스 간격을 제거된 연장된 게이트 구조를 제안하였다. 이 구조는 TaN 게이트의 일부분이 소스 상단에 겹친 구조로 HfO_2 게이트 절연막으로 절연된다. 따라서 드레인-소스 간격의 감소와 함께 온-저항이 2.91 m$\Omega\cdot$cm^{2}에서 2.28 m$\Omega\cdot$cm^{2}로 크게 감소하였다. 게이트 절연막의 높은 유전상수와 AlGaN/GaN MOS-HEMTs의 문턱전압의 절대값 이상의 절연막 항복전압은 안정적인 온/오프 동작을 위해서 필수적인 요소이다. 따라서, 연장된 TaN 게이트 구조를 통해 4.97×10^{10}의 높은 온/오프 전류비와 872 MW$\cdot$cm^{-2}의 성능지수, 1410 V의 높은 항복전압을 보였다.

마지막으로, 별도의 마감구조의 적용 없이 높은 항복전압의 구현을 위한 방법으로 RF-스퍼터링 방식을 통한 Ga_2O_3과 Al_2O_3 박막의 적용을 제안하였다. GaN 표면으로의 스퍼터링 데미지와 AlGaN/GaN HEMTs에서의 표면 누설전류를 억제하기 위하여 스퍼터링 조건을

최적화하였다. 비정질 Ga_2O_3 내부의 깊은 에너지를 갖는 트랩으로의 전자의 트래핑을 활용함으로써 게이트 하단의 공핍층을 효과적으로 확장시킴에 따라 항복전압이 크게 증가하였다. 깊은 에너지를 갖는 트랩은 상대적으로 긴 전자의 방출 시간을 보이므로, 얕은 에너지 준위로 인한 표면 누설전류가 효과적으로 억제될 수 있다. 제작된 AlGaN/GaN HEMTs-on-SiC에서 Ga_2O_3 패시베이션을 50, 100, 150, 그리고 200 W에서 진행하였을 경우 항복전압은 각각 1430, 890, 820, 그리고 460 V로 측정되었다. 반면에 패시베이션을 하지 않은 기본 소자의 경우 520 V로 상대적으로 낮은 항복전압이 측정되었다. 그리고 50 W에서 Ga_2O_3 패시베이션을 진행한 AlGaN/GaN HEMTs 소자는 40 μm의 게이트-드레인 간격에서 2.7 kV의 높은 항복전압이 측정되었다. 또한, 더욱 효과적인 누설전류의 억제와 문턱전압의 양의 방향으로의 이동을 위한 구조로서, RF-스퍼터링에 의한 Al_2O_3/Ga_2O_3 다층구조를 적용한 AlGaN/GaN HEMTs를 제안하였다. Al_2O_3/Ga_2O_3 다층구조를 통해서 AlGaN/GaN HEMTs의 항복전압이 380 V에서 1104 V로 증가하였으며 드레인 누설전류는 1.8 μA/mm에서 33 nA/mm로 감소하였다. 또한 문턱전압은 −2 V에서 −1.4 V로 증가하였고 V_{GS}= −10 V를 100초동안 DC 스트레스 이후 문턱전압이 0.12 V로 이동함을 것을 확인하였다.

주요어: AlGaN, GaN, 고-전자-이동도 트랜지스터 (HEMT), 게이트 절연막, HfO_2, 골드-프리 공정, 온-저항, 항복전압

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