



공학박사 학위논문

Improvement of Low Temperature Solution-processed Oxide Thin Film Transistors by O₂ plasma, UV radiation and Biased-H₂O annealing

O₂ 플라즈마, 자외선 조사, Biased-H₂O 어닐링을 통한 저온 용액공정을 이용한 산화물 박막트랜지스터의 특성 향상에 대한 연구

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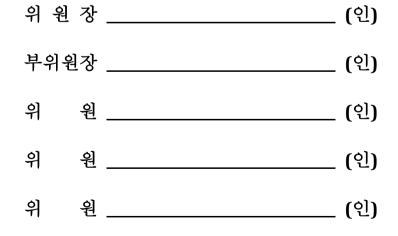
Improvement of Low Temperature Solution-processed Oxide Thin Film Transistors by O₂ plasma, UV radiation and Biased-H₂O annealing

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> 서울대학교 대학원 전기·컴퓨터 공학부 이 정 수

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논문제목: Improvement of Low Temperature Solution-processed Oxide Thin Film Transistors by O₂ plasma, UV radiation and Biased-H₂O annealing

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Abstract

Improvement of Low Temperature Solution-processed Oxide Thin Film Transistors by O₂ plasma, UV radiation and Biased-H₂O annealing

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Solution-processed oxide thin film transistors (TFTs) with zinc-tin-oxide (ZTO) and indium-gallium-zinc-oxide (IGZO) have attracted considerable attention for the driving elements of active matrix display, instead of Si-based TFTs and organic TFTs, because of high mobility, visible light transparency, flexibility, wide range of materials, and controllability of electrical properties by atomic composition. Solution-processed oxide TFTs show superior performance for active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) display backplanes, compared with solution-processed oxide TFTs are compatible with large area due to good uniformity and high throughput, so that could be a method for achieving low cost fabrication contrary to vacuum processes.

Among various ZnO-based oxide semiconductors, ZTO TFTs employing tin (Sn) material maybe promising candidates for achieving low cost processes because Sn is a quite low cost material compared with widely used indium (In).

Solution-processed ZTO TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic for additional cost reduction and application extension to a flexible display. For solution-processed ZTO TFTs fabrication with these flexible substrates, low temperature processes are necessary because these substrates are easily damaged at high annealing temperatures. At low annealing temperature, however, solution-processed ZTO TFTs have poor performance such as low on-current, high threshold voltage and low mobility, so a rather high annealing temperature exceeding 500 °C is required in solutionprocessed ZTO TFTs. To improve the device characteristics of solution-processed oxide TFTs even at low annealing temperature on an active layer, a study of the effects of annealing temperature on the electrical characteristics of solutionprocessed oxide TFTs and the efforts to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature on active layer are desired. There were some efforts to investigate the effects of annealing temperature on solution-processed oxide TFTs, but the electrical and chemical mechanisms of annealing temperature on solution-processed oxide TFTs have been scarcely studied.

The purpose of this thesis is to fabricate oxide TFTs employing solution-process for an oxide semiconductor active layer with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability, and to improve the electrical characteristics of low temperature solution-processed oxide TFTs for low cost, stable, and flexible active matrix display backplane.

The effects of annealing temperature on the bonding structure of ZTO active layer in solution-processed ZTO TFTs were investigated and the chemical formation equation of the ZTO active layer with regard to the annealing temperature was established.

To improve the electrical characteristics of low temperature solution-processed oxide TFTs according to the investigation of effects of annealing temperature in regard of the chemical formation of ZTO active layer, O₂ plasma treatment, UV radiation treatment, and the biased-H₂O annealing were proposed to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature. Moreover, the effects on electrical and chemical characteristics of solution-processed oxide TFTs with proposed methods were investigated in detail. These proposed methods to improve the electrical characteristics of low temperature solution-processed oxide TFTs would be suitable for the low cost, stable, and flexible active matrix display backplane.

Keywords: Oxide thin film transistor, Solution-process, Annealing temperature, O_2 plasma, Ultra-Violet radiation, Biased-H₂O annealing

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Contents

Abstracti
Contentsiv
List of Tablesvii
List of Figuresix
Chapter 1 Introduction1
1.1 Recent flat panel display technology2
1.2 Device parameter extraction
1.3 Dissertation organization14
Chapter 2 Review of solution-processed oxide TFTs16
2.1 Overview of oxide TFTs17
2.2 Advantages of solution-process
2.3 Solution-processed oxide TFTs
Chapter 3 Optimization of the fabrication process of
solution-processed oxide TFTs
3.1 Overview
3.2 Structure of solution-processed oxide TFTs
3.3 Stirring time on solution-processed oxide TFTs
3.4 Active layer thickness on solution-processed oxide TFTs
3.5 Effects of passivation on solution-processed oxide TFTs60

3.6 Electrical characteristics of solution-processed oxide TFTs63
3.6.1 Transfer characteristics63
3.6.2 Reliability characteristics
Chapter 4 Effects of Annealing Temperature on Solution-
processed oxide TFTs75
4.1 Motivation
4.2 Fabrication of solution-processed ZTO TFTs with various
annealing temperature
4.3 Electrical characteristics with the increase in annealing
temperature
4.4 Dechlorination on threshold voltage with the increase in
annealing temperature
4.5 Dechlorination and crystallization on saturation mobility with
the increase in annealing temperature
4.6 Reliability characteristics with the increase in annealing
temperature
4.7 Chemical formation equations with the increase in annealing
temperature
4.8 Conclusion
Chapter 5 Improvement of low temperature solution-
processed oxide TFTs100
5.1 Improvement of low temperature solution-processed oxide
TFTs employing O_2 plasma treatment 101
5.1.1 Motivation 101
5.1.2 Fabrication of solution-processed ZTO TFTs employing O_2 plasma

treatment 104
5.1.3 Electrical characteristics with O_2 plasma treatment
5.1.4 Preferential dissociation of Cl on threshold voltage by O_2 plasma
treatment 111
5.1.5 Increase of electron concentration on saturation mobility by O_2
plasma treatment 116
5.1.6 Reliability characteristics with O_2 plasma treatment 119
5.1.7 Conclusion 122
5.2 Improvement of low temperature solution-processed oxide
TFTs employing Ultra-Violet radiation treatment
5.2.1 Motivation 123
5.2.2 Fabrication of solution-processed ZTO TFTs employing UV
radiation treatment
5.2.3 Electrical characteristics with UV radiation treatment
5.2.4 Effects of UV radiation treatment on oxide active layer
semiconductors
5.2.5 Generation of hydroxide(-OH) bonding by UV radiation treatment
on oxide active layer semiconductors
5.2.6 Conclusion
5.3 Improvement of low temperature solution-processed oxide
TFTs employing biaed-H ₂ O annealing
5.3.1 Motivation
5.3.2 Effects of various annealing condition
5.3.3 Effects of H_2O wet annealing according to the annealing
temperature
5.3.4 Proposed biased- H_2O annealing to improve low temperature
solution-processed oxide TFTs154
5.3.5 Conclusion 161
Chapter 6 Summary162
Bibliography171
초 록191

List of Tables

Table 2-1. Comparison of TFTs with various active layers 22
Table 2-2. Comparison of various solution-processed semiconductor TFTs 32
Table 2-3. The electrical characteristics of solution-processed ZTO TFTs with
various annealing temperature34
Table 3-1. The property of solute as zinc chloride (ZnCl ₂) and Tin (II) chloride
(SnCl ₂) powders and solvent as Acetonitrile (CH ₃ CN) for the synthesis of
solution of ZTO
Table 3-2. Thickness of spin-coated ZTO active layer before and after RTA 500 °C
annealing according to the variation of rpm and time of spin-coating 58
Table 3-3. Materials including the thickness and processes for each layer of
solution-processed ZTO TFTs on Si-wafer substrate65
Table 4-1. Electrical characteristics of solution-processed ZTO TFTs with the
annealing temperature of 300 - 500 °C with W / L = 100 / 10 μm and V_{DS} =
10 V
Table 5-1. Electrical characteristics of solution-processed ZTO TFTs with an
annealing temperature of 350 °C by employing O_2 plasma treatment of
100 W and 300 W with W / L = 100 / 10 μm and V_{DS} = 10 V 110
Table 5-2. Electrical characteristics of solution-processed ZTO TFTs with an
annealing temperature of 350 $^{\circ}$ C employing UV radiation treatment for 30
min and 1 hour with W / L = 3000 / 500 μm and V_{DS} = 10 V

Table 5-3. Electrical characteristics of solution-processed IGZO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30

min and 1 hour with W / L = 3000 / 500 μ m and V_{DS} = 10 V 132

- Table 6-1. Summary of improved electrical characteristics of solution-processedZTO TFTs with various annealing condition170

List of Figures

Figure 1-1. Desired development of display and active matrix TFT backplane
technology9
Figure 1-2. Evolution of display technology10
Figure 1-3. Desired development of active matrix TFT backplanes to achieve high
performance of AMLCD and/or AMOLED11
Figure 2-1. Schematic orbital structure of the conduction-band minimum in
crystalline and amorphous phase in (a) covalent bond as Si and (b) ionic
bond as oxide semiconductor
Figure 2-2. Progress of oxide TFT technology (Ref. Displaybank)
Figure 2-3. The advantages of oxide semiconductors compared with a-Si and
poly-Si
Figure 2-4. Transparent and flexible displays
Figure 2-5. The deposition types of solution-process as (a) spin-coating, (b) dip-
coating, and (c) ink-jet printing28
Figure 2-6. The comparison of solution-processible semiconductor materials 29
Figure 2-7. Transfer characteristics of solution-processed ZTO TFTs with various
Figure 2-7. Transfer characteristics of solution-processed ZTO TFTs with various annealing temperature
annealing temperature
annealing temperature
annealing temperature

Figure 3-3. Cross-sectional view of ZTO active layer, SiO_2 gate insulator, and Si
wafer substrate
Figure 3-4. Plane view of the patterned solution-processed ZTO TFTs with ZTO
active layer and IZO source/drain electrodes45
Figure 3-5. Sequence of the fabrication process of solution-processed ZTO TFTs
on Si-wafer substrate
Figure 3-6. Transfer characteristics of solution-processed ZTO TFTs according to
various stirring time of ZTO solution with an annealing temperature of
500 °C with W / L = 100 / 10 μm and V_{DS} = 10 V
Figure 3-7. Thermogavimetry analysis (TGA) and differential thermal analysis
(DTA) results of ZTO solution with the increase in temperature according
to various stirring time of ZTO solution52
Figure 3-8. Transmittance of ZTO active layer on bare glass with the increase in
temperature according to various stirring time of ZTO solution53
Figure 3-9. Transfer characteristics of solution-processed ZTO TFTs with stirring
time of 15 and 30 min, and their post-annealed results at 200 $^{\circ}\mathrm{C}$ for 120
min
Figure 3-10. Transfer characteristics of solution-processed ZTO TFTs with
stirring time of 30 min according to various post-annealing time at 200 $^\circ\mathrm{C}$
Figure 3-11. Transfer characteristics of solution-processed ZTO TFTs according
to multi-coating with an annealing temperature of 500 °C with W / L =
100 / 10 μm and V_{DS} = 10 V
Figure 3-12. Stability for time of transfer characteristics of solution-processed

ZTO TFTs (a) without passivation and (b) with PMMA passivation with an

- Figure 3-13. Transfer characteristics of solution-processed ZTO TFTs with an annealing temperature of 500 °C with V_{DS} = 10 V (a) according to various channel width (W) and length (L) and (b) normalized curves with W/L.66

Figure 4-3. Threshold voltage and electron concentration of solution-processed
ZTO TFTs with the annealing temperature of 200 - 500 $^\circ$ C85

- Figure 4-8. (a) Diffraction patterns below 450 °C and (b) diffraction pattern and dark field images above 450 °C of ZTO active layer obtained by TEM92

Figure 5-1. Plasma treatment effects on (a) the transfer characteristics and (b)
carrier density and hall mobility of sputtered oxide TFTs in previous work
Figure 5-2. Inverted staggered structure of low temperature solution-processed
ZTO TFTs employing O_2 plasma treatment105
Figure 5-3. Cross-sectional view of ZTO active film, SiO_2 gate insulator, and Si
wafer substrate
Figure 5-4. Sequence of the fabrication process of low temperature solution-
processed ZTO TFTs employing O_2 plasma treatment 107
Figure 5-5. Transfer characteristics of solution-processed ZTO TFTs with an
annealing temperature of 350 °C by employing O_2 plasma treatment of
100 W and 300 W with W / L = 100 / 10 μm and V_DS = 10 V 109
Figure 5-6. Threshold voltage and electron concentration of solution-processed
ZTO TFTs with an annealing temperature of 350 °C according to O_2 plasma
power
Figure 5-7. Atomic concentration of ZTO films in AES annealed at 350 $^{\circ}\mathrm{C}$
according to O_2 plasma power for (a) Cl atoms and (b) O atoms114
Figure 5-8. Atomic concentration of ZTO films in AES annealed at 350 °C
according to O_2 plasma power for C atom 115
Figure 5-9. Cl atomic concentration and saturation mobility of solution-
processed ZTO TFTs with an annealing temperature of 350 °C according
to O_2 plasma power
Figure 5-10. ZTO active layer with amorphous phase regardless of O_2 plasma
power with (a) XRD results and (b) TEM images

Figure 5-11. Reliability characteristics of solution-processed ZTO TFTs with the
positive gate bias-stress of 10 V for 3600 sec as transfer curve (a) without
O_2 plasma treatment, (b) employing O_2 plasma treatment of 300 W 120 $$
Figure 5-12. Threshold voltage shift without O_2 plasma treatment and with O_2
plasma treatment of 300 W 121
Figure 5-13. UV exposure measurement on sputtered oxide TFTs in previous
work
Figure 5-14. Inverted staggered structure of low temperature solution-processed
oxide TFTs employing UV radiation treatment128
Figure 5-15. Sequence of the fabrication process of low temperature solution-
processed oxide TFTs employing UV radiation treatment
Figure 5-16. Transfer characteristics of solution-processed ZTO TFTs with an
annealing temperature of 350 °C employing UV radiation treatment for 30 $$
min and 1 hour with W / L = 3000 / 500 μm and V_{DS} = 10 V
Figure 5-17. Transfer characteristics of solution-processed IGZO TFTs with an
annealing temperature of 350 °C employing UV radiation treatment for 30 $$
min and 1 hour with W / L = 3000 / 500 μm and V_{DS} = 10 V 132
Figure 5-18. Atomic concentration of solution-processed (a) ZTO and (b) IGZO
active layers with UV radiation treatment by XPS 134
Figure 5-19. XPS spectra of 0 1s core level of solution-processed 135
Figure 5-20. [O(hydroxide)] / [O(total)] of (a) ZTO and (b) IGZO active layers
with UV radiation treatment136
Figure 5-21. Schematic diagram of generation of hydroxide (-OH) bonding by UV
radiation treatment on oxide active layer semiconductors

Figure 5-24. Transfer characteristics of solution-processed ZTO TFTs with various annealing condition with W / L = 100 / 10 μ m and V_{DS} = 10 V.. 147

- Figure 6-2. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing O₂ plasma treatment 166

Figure	6-3. Chemical	diagram	of metal-	oxide form	nation fro	om precur	sors v	vith	the
	increase in an	nealing te	emperatu	re employ	ing UV ra	diation		1	.67

Figure 6-4. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing biased-H₂O annealing 168

Figure	6-5.	Diagram	of	improvement	of	low	temperature	solution-processed	ł
	oxide	e TFTs)

Chapter 1 Introduction

Recently, high performance, large size, low cost, transparent and flexible active matrix displays have attracted considerable attention in the emerging electronic device industry. Solution-processed oxide thin film transistors (TFTs) are promising candidates for next generation high performance, large size, low cost, transparent and flexible display backplane due to high mobility, good uniformity, high throughput and visible light transparency. The only issue of solution-processed oxide TFTs is the fabrication temperature, so that the efforts to achieve high device characteristics of solution-processed zinc-tin-oxide (ZTO) TFTs even at low annealing temperature on active layer are desired.

1.1 Recent flat panel display technology

Display technology has been desired to achieve high resolution, no motion blur, large size, cost reduction, transparency and flexibility. As a result, to keep pace with the development of display technology, the TFT backplane technology for active matrix display has been also developed as device minimizing, high mobility, good uniformity, non-vacuum process, large band-gap materials and low temperature process as demonstrated in Figure 1-1.

In development of display technology, flat panel displays (FPDs) have been remarkably encompassed a growing number of electronic visual display technologies with replacing the cathode ray tubes (CRTs) in display industries in the last decade as shown in Figure 1-2 [1]. FPDs are far lighter, thinner, usually less than 10 centimeters (3.9 in) thick, and more power efficient than traditional cathode ray tubes (CRTs) which was a dominant display for decades. They have many advantages such as the light and thin display, high-resolution images, and low-power consumption with low voltage driving so that they have been prevailed in many display applications such as monitor, television, and specifically modern portable devices as laptops, mobile phones, digital cameras, and camcorders.

FPDs could be divided by various types of materials and method to display into liquid crystal display (LCD), organic light emitting diode (OLED), plasma display panel (PDP), and field emission display (FED) [2-6].

Among various FPDs, LCDs have been used in most display technologies because they are thin, light-weight, bright and cost-effective due to the low-temperature process on glass substrates. LCDs are common in a wide range of applications including computer monitors, televisions, instrument panels, aircraft cockpit displays, signage, watches, calculators, and cellular phones. [7]. LCDs have been emerged by large size TVs and monitors over 40 inch so that they enlarge their portion over PDPs and projection TVs in home display applications [8]. Moreover, its low electrical power consumption enables it to be used in batterypowered electronic equipment so that they could be employed for diverse portable applications.

Although LCD display is the most widely commercialized FPD, it is relatively slow response time (~several msec), and narrow viewing angle. OLED technology could be another candidate for the alternative to LCD with regard to TFT backplane. In 1987, *C. W. Tang* and *S. A. VanSlyke* reported luminescence from an organic material [9-11]. Small molecules were deposited to form a layered structure in a vacuum and the layered structure is sandwiched between an anode and cathode. A high electric field at low voltage could be achieved by the thin (< 1 μ m) organic material. Therefore, a light from thin film organic materials could be produced at low voltage. OLED displays exhibit superb electro-optical properties such as a fast response (~ several µsec) to the image addressing and a wide viewing angle due to self-emissive characteristics. New organic materials and new configurations of devices to improve efficiency and stability of OLED displays have been investigated by many research groups [12-15]. Thus, OLED displays have the potential for new technology compared with the LCDs.

The development of both active matrix LCDs (AMLCDs) and active matrix OLED (AMOLED) for high resolution and full-color display has been fulfilled by the development of TFT backplanes [16]. The active matrix display employing the TFT as a pixel switch has enhanced the capability of high quality image processing, so that the importance of LCDs in commercial fields increases. The electro-optical performance of AMOLED is very sensitive to the characteristics of

TFT. A small variation of the OLED current in the each pixel may cause a critical problem because the OLED luminance is emitted by the current driving. Each TFT pixel in AMOLED panel requires a constant current source with a desired image data during the whole emission time. Therefore, TFT with high electrical capability as well as reliability is key issue for achieving high performance active matrix display.

In terms of the active matrix backplane TFTs to achieve high performance of AMLCD and/or AMOLED, the TFTs need to have been developed as the aspect of material as well as fabrication process as demonstrated in Figure 1-3.

In material development of TFTs for the active matrix backplanes, TFTs have been investigated with the issues of semiconductor, gate dielectric, electrode, and passivation materials. Especially, semiconductor materials have been mostly investigated to achieve high performance TFTs of active matrix display.

Hydrogenated amorphous silicon thin film transistors (a-Si TFTs) have been widely used for AMLCDs due to their productivity on a large area glass substrates by low temperature process below 300 °C [17]. The a-Si TFT can represent the gray scale by switching the voltage data and charging the capacitors of each pixel element. However, the low field effect mobility (~ 0.5 cm²/V·sec) is the critical limitation for achievement of the high resolution display in AMLCD, results in the poor current driving characteristics of a-Si TFT [18]. Moreover, a-Si TFT should meet adequate requirements for current-driving device in AMOLED, which luminance emitting is closely related with electrical capability of TFT.

The a-Si technology is considered to be applied for large area AMOLED displays due to its low fabrication cost and excellent uniformity as widely used in AMLCDs. However, a long-term device degradation would be the fatal problem for adequate requirements of AMOLED, so that the degradation of the a-Si:H TFT should be compensated by the pixel circuit and the new driving scheme should be investigated to suppress the degradation of a-Si TFTs itself. This would require a rather complicated compensation circuit compared with the poly-Si TFT based pixel design. However, to fabricate the compensation circuit in every pixel is limited by the dimension of a-Si:H TFT components and other signal lines of the circuit.

Polycrystalline silicon (poly-Si) film as an active layer could be employed to solve the problem of low carrier mobility of a-Si TFTs [19, 20]. Poly-Si TFTs have attracted considerable attentions due to its high electron mobility ($30 \sim 500$ cm²/V·sec) and current driving capability [21, 22]. Generally, Poly-Si film is fabricated by recrystallization of the a-Si:H film deposited at low temperature below 400 °C. The superior electrical characteristics of poly-Si TFT allows a fast switching required for high-resolution image with reduced device size compared with a-Si TFT. In addition, poly-Si TFTs enable the ability to implement the complementary metal-oxide-semiconductor (CMOS) process and to integrate the peripheral driver circuits and pixel switching devices simultaneously on a glass substrate for so-called 'System-on-Glass (SOG)' recently [23, 24].

Excimer laser annealing (ELA) technologies have been extensively investigated to fabricated high mobility poly-Si thin film on a large area glass substrate for a reliable current driving in AMOLED. The low temperature (< 400 °C) crystallization of a-Si film on a glass can be obtained by ELA without any thermal damage to the glass [25].

Although the low temperature poly-Si (LTPS) technology could achieve high electrical performances, the uniformity should be improved caused by grainboundaries induced by the fluctuation of ELA energy. In poly-Si film, the grain boundaries are inherently incorporated by a lot of disconnected or mismatched silicon bonds which make a high density of trap states [26]. The random distribution of grain boundaries would cause the non-uniformity of the field effect mobility and the threshold voltage of the poly-Si TFT. The anomalous large off-state leakage current is also attributed to the enhanced electron-hole pair generation in the grain boundary near the drain junction [27]. Additionally, the hot-carriers induced by the high drain field accelerate the kink current, resulting in the deterioration of reliability [28]. Therefore, the I_{OLED} compensation pixel circuits, which can compensate the non-uniform characteristics of poly-Si TFTs, are required for the uniform luminance in the display panel [29, 30]. Furthermore, the LTPS technology requires high fabrication cost of poly-Si TFTs due to the additional process steps than a-Si TFT, reducing the process yield [31].

Therefore, the advanced technology are desired to achieve the high performance active matrix display, instead of conventional TFT devices, which poor reliability and low electrical capability of a-Si TFT and severe non-uniformity and complicated fabrication process of LTPS TFT.

nc-Si TFTs, which has small grains of crystalline silicon within the amorphous phase, may be promising devices to fabricate various flat displays, due to a superior performance and stability compared with a-Si and organic TFTs because of the uniformity of crystalline grains formed during the deposition and a rather simple process and good uniformity compared with a poly-Si TFT [32]. Although it currently cannot attain the mobility that poly-Si can, it has the advantage for both AMLCD and AMOLED applications over poly-Si that it is easier to fabricate, as it can be deposited using conventional low temperature a-Si deposition techniques, such as plasma enhanced chemical vapor deposition (PECVD), as opposed to laser annealing or high temperature CVD processes, in the case of poly-Si. Another candidate for advanced TFT would be amorphous oxide (a-oxide) semiconductor TFT for next generation display of AMLCD and/or AMOLED. a-oxide TFTs have attracted considerable attention with a high mobility of > 10 cm²/V·sec even in the amorphous phase for an good alternative to a-Si TFTs [33]. The high mobility in the a-oxide material is attributed to the electron transport by the conduction band, whose features are completely different from those of the covalent semiconductors [34]. In addition, oxide semiconductor materials have an amorphous phase, which shows uniform electrical properties even with a large-size display [35-37]. Therefore, high resolution, such as ultra-high definition (UD : 3840×2160), a high frame rate (> 240 Hz), and large size display (more than 70 inches) could be achieved by the high electrical performance of a-oxide TFTs [38-40].

Transparency with the visible light of oxide semiconductors could be another advantage of the oxide TFTs over the silicon-based TFTs. Zinc oxide based semiconductor, such as indium-gallium-zinc-oxide, exhibits large optical band gap (> 2.8 eV) compared to silicon-based semiconductor [41, 42]. Due to large band gap characteristics, the oxide semiconductor exhibits low leakage current.

In fabrication process development of semiconductor materials of TFTs for the active matrix backplanes, the deposition method of semiconductor materials could be divided into vacuum process and non-vacuum process. Non-vacuum solution-processes such as spin-coating, dip-coating, and ink-jet printing could achieve low-cost fabrication because vacuum-deposition processes, such as rf magnetron sputtering and pulsed laser deposition, require a high manufacturing cost. Solution-processes are also suitable for large-area, high-throughput, and direct patterning [43, 44].

Therefore, the solution-processed oxide TFTs are employed in this study to

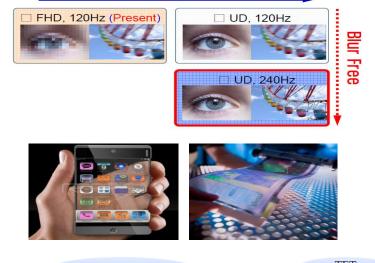
achieve low-cost fabrication as well as high mobility and high throughput for active matrix display.

For additional cost reduction and application extension to a flexible display, the solution-processed oxide TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic. These substrates are easily damaged at high annealing temperatures, so low-temperature processes are essential for solution-processed oxide TFTs fabrication with flexible substrates. However, a high annealing temperature on an active layer exceeding 500 °C is required to obtain high device performance such as low threshold voltage and high mobility in solution-processed oxide TFTs from previous reports [45-49]. To improve the device characteristics of solution-processed oxide TFTs even at low annealing temperature on an active layer, a study of the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs and the efforts to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature on active layer are desired. There were some efforts to investigate the effects of annealing temperature on solution-processed oxide TFTs, but the electrical and chemical mechanisms of annealing temperature on solution-processed oxide TFTs have been scarcely studied [50, 51].

The purpose of this thesis is to fabricate oxide TFTs employing solution-process for an oxide semiconductor active layer with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage and mobility, and to improve the electrical characteristics of low temperature solution-processed oxide TFTs for active matrix display.



High Resolution



	Display			TFT Backplane
High Resolution	FHD		UD $(4K \times 2K)$	Device minimizing
Motion Blur Free	120 Hz		240 Hz	High mobility
Large Size	40 "		82 "	Good uniformity
Cost Reduction	High-thro	oughput p	Non-vacuum	
Transparency	Visible li	ight transp	Large band-gap materials	
Flexibility	Flex	ible subst	Low temperature process	

Figure 1-1. Desired development of display and active matrix TFT backplane technology



Figure 1-2. Evolution of display technology

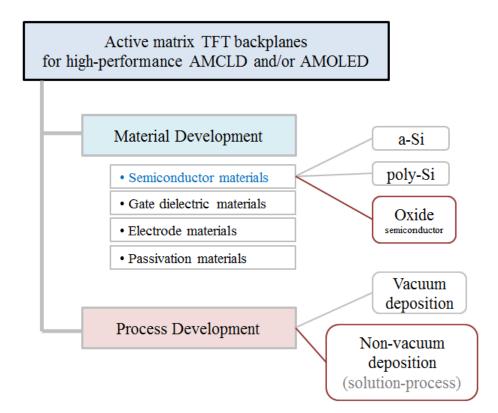


Figure 1-3. Desired development of active matrix TFT backplanes to achieve high performance of AMLCD and/or AMOLED

1.2 Device parameter extraction

In this section, the methods for preparing solution of oxide semiconductor precursors and device parameters extraction in this thesis are introduced.

The solution of oxide semiconductor is prepared with measuring by its weight. The solute, that is precursor, is measured by weight to confirm its molar ratio with a quantity of 3 ml as following equation.

$$FW [g/mol] \times 3 ml \times M [mol/L] = W [g]$$

(FW : Formula weight [g/mol], M : Molarity(Molar ratio) [mol/L], W : weight [g]) The solvent is also measured by weight to be matched with a quantity of 3 ml as following equation.

> d [g/ml] × 3 ml = W [g] (d : density [g/ml], W : weight [g])

Basically, the measurement was carried out in the dark state and at room temperature. The device parameter originated by from the conventional MOS field effect transistor (MOSFET) is adopted in TFT analysis.

I-V relationship of a TFT can be derived by Ohm' law,

$$I_{DS} = \frac{W}{L} \mu_{lin} C_{ox} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$
(1)

where μ_{lin} , μ_{sat} , C_{ox} and V_{TH} are the field effect mobility for the linear region and the saturation region, gate insulator capacitor per unit area and the threshold voltage, respectively. W and L are channel width and length of the TFT, respectively.

(1) is the standard linear regime equation. When $V_D=V_G-V_{TH}$, the channel becomes pinch-off, which means no longer potential difference between the gate

and the drain terminal, leading the drain region depletion of free carrier. By substituting ' $V_D=V_G-V_{TH}$ ' into (1) yields,

$$I_{DS} = \frac{W}{2L} \mu_{sat} C_{ox} (V_{GS} - V_{TH})^2$$
(2)

The saturation mobility (μ_{sat}) in the saturation region can be extracted from (2) with unit of cm²/V·sec.

The V_{TH} was defined by the gate voltage, which induced a drain current of 'L/W \times 10 nA \times V_{DS}'.

The subthreshold swing (S slope) describes how effectively the device switches between on and off state, with unit of V/dec or mV/dec.

$$S = \frac{dV_{GS}}{dlogI_{DS}}$$
(4)

1.3 Dissertation organization

The purpose of this thesis is to fabricate oxide TFTs employing solution-process for an oxide semiconductor active layer with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability, and to improve the electrical characteristics of low temperature solution-processed oxide TFTs for inexpensive and flexible active matrix display.

Chapter 2 gives a brief introduction to the solution-processed oxide TFTs. The advantages of oxide TFTs and solution-process are reviewed, and accordingly the merits and the only issue, that is the fabrication temperature, of solution-processed oxide TFTs are also reviewed.

Chapter 3 indicates the optimization of the fabrication process of oxide TFTs employing solution-process for an oxide semiconductor active layer with various condition of the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation to investigate the effects of fabrication process condition on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability.

Chapter 4 focuses on the investigation of the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability. The effects of annealing temperature on the bonding structure of ZTO active layer in solution-processed ZTO TFTs were investigated and the chemical formation equation of the ZTO active layer with regard to the annealing temperature was established.

Chapter 5 concentrates on the methods to improve the electrical characteristics of low temperature solution-processed oxide TFTs according to the investigation

of effects of annealing temperature. In regard of the chemical formation of ZTO active layer according to the annealing temperature, O₂ plasma treatment, UV radiation treatment, and the biased-H₂O annealing were proposed to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature. Moreover, the effects on electrical and chemical characteristics of solution-processed oxide TFTs with proposed methods were investigated in detail.

Finally, the investigation of the effects of annealing temperature on solutionprocessed oxide TFTs and the proposed methods to improve the electrical characteristics of low temperature solution-processed oxide TFTs for the low cost, stable, and flexible active matrix display backplane were summarized in chapter 6.

Chapter 2 Review of solution-processed oxide TFTs

Solution-processed oxide TFTs are promising candidates for advanced high performance, large size, low cost, and flexible active matrix display backplane due to high mobility, visible light transparency, and good uniformity. Furthermore, solution-process could be a method for achieving low cost fabrication contrary to vacuum processes and suitable for large area and high throughput. The only issue of solution-processed oxide TFTs is the fabrication temperature, so that the efforts to improve electrical characteristics of solutionprocessed ZTO TFTs such as threshold voltage, saturation mobility, and reliability even at low annealing temperature on active layer are desired.

2.1 Overview of oxide TFTs

Oxide semiconductors with polycrystalline phase, such as ZnO, In₂O₃, SnO₂, and ITO, have been introduced for the application of transparent conductive oxides (TCOs) for solar cells and conductive transparent electrodes because of high conductivity and wide-bandgap. Furthermore, oxide semiconductor TFTs (oxide TFTs) have been intensively studied as promising alternatives to conventional a-Si TFTs by a requirement for high-resolution, large size and high frame rate operation, from early 2000s.

Oxide TFT employing ZnO using radio frequency (RF) magnetron sputtering or pulsed laser deposition (PLD) was reported by various groups since early 2000s. Hoffman et al. fabricated ZnO TFT employing ion beam sputtering, and mobility of 2.5 cm²/V-s with a drain current on-to-off ratio >10⁵ were obtained.[52] Elvira et al. developed fully transparent ZnO TFTs, with a room temperature process, exhibiting high mobility near 20 cm²/V·sec [53].

Higher electrical conductivity $(10^{-2} \Omega^{-1} \text{ cm to } 10^3 \Omega^{-1} \text{ cm}^1)$ of oxide semiconductor is attributed to the existence of native defects, such as oxygen vacancies, cation interstitials, and substitutional/interstitial hydrogen, that act as shallow donors [54]. Because of these donors, the TCOs have a high carrier concentration of 10^{18} cm⁻³ to 10^{21} cm⁻³.

However, polycrystalline oxide TFTs have its own drawback, which is the formation of grain boundary, causing non-uniform TFT performance at different locations. Another problem is the difficulty of fabrication, which originates from the low chemical durability of pure ZnO against acidic etchants. They also require relatively high gate voltages to turn-on as enhancement mode.

Oxide TFTs with amorphous phase were firstly reported in 2004, Nomura et al. with a new class of a-oxide semiconductors based on IGZO deposited at room temperature, and demonstrated high performance transistors ($\mu \approx 8.3 \text{ cm}^2/\text{V} \cdot \text{sec}$) [55, 56]. Despite the amorphous state, the origin of the high mobility was attributed to the electronic orbital structure of the material.

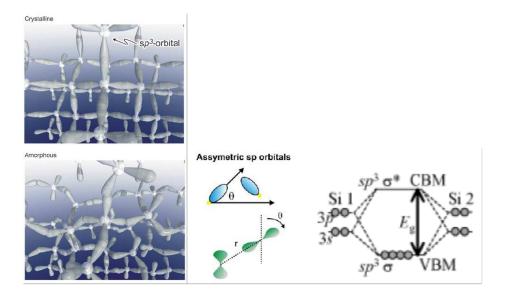
Figure 2-1 shows schematic orbital structure of the conduction-band minimum for the carrier transport paths in crystalline and amorphous phase in covalent bond as Si and also ionic bond as oxide semiconductor. Covalent semiconductors have carrier transport paths composed of strongly directive sp³ orbitals, so structural randomness greatly degrades the magnitude of bond overlap and carrier mobility [57]. However, a-oxide semiconductors are composed of posttransition-metal cations which exhibit isotropic properties, where the overlap of the In 5s orbitals is mainly formed and the contribution of oxygen 2p orbitals is small. Direct overlap between neighboring metal s orbitals is rather large, and is not significantly affected even in a distorted amorphous structure [58]. Therefore, a-oxide semiconductor is insensitive to structural deformation, so that could exhibits high mobility even in an amorphous phase.

While Si material undergoes a significant reduction in mobility from 1000 (single crystal) to 1 (amorphous) cm²/V·sec, a-oxide semiconductor is not degraded in mobility even in amorphous phase so that a promising material for switching or driving elements in future high resolution and large size display.

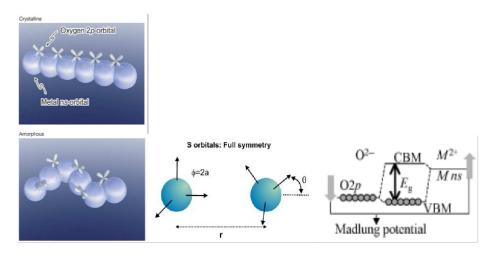
The development of oxide TFTs technology has been emerged drastically in the last decade by a number of advantages of oxide semiconductors as demonstrated in Figure 2-2 of the prototypes AMLCD or AMOLED employing oxide TFTs.

The progress of oxide TFTs could be achieved by their many advantages such as high mobility, good uniformity, low cost process, transparency, and flexibility, compared with conventional ones. Comparison of TFTs with various active layers was described in Table 2-1. Although currently widely used a-Si TFTs show a good uniformity, their low mobility is not suitable for high resolution and high speed driving devices. Poly-Si TFTs have high mobility and good reliability, but their bad uniformity would be the issue for large size display panel. nc-Si TFTs show no particular advantages compared with a-Si and poly-Si TFTs, so that they seems not to be good candidates for state-of-the-art display needs. However, oxide TFTs show better mobility and reliability than that of a-Si TFTs and better uniformity than that of poly-Si TFTs as demonstrated in Figure 2-3, so that oxide TFTs have attracted considerable attention for high resolution, high speed driving, and large size display. Moreover, a number of research groups such as Hosono have investigated the effective improvement of electrical characteristics of ZnO-based oxide semiconductors by adding indium, gallium, or tin, to be applied to advanced display technologies [59-61]. Especially, indiumgallium-zinc-oxide (IGZO), indium-zinc-oxide (IZO), and zinc-tin-oxide (ZTO) have been reported in the last decade and recently hafnium-indium-zinc-oxide (HIZO) and aluminum-zinc-oxide (AZO) have been investigated vigorously [62-67].

Furthermore, the oxide TFTs have merits of high transparency due to their widbandgap as well as flexibility due to their stability against bending stress. Therefore, oxide TFTs may be the promising candidate for the active matrix backplanes to the next generation transparent and flexible display as shown in Figure 2-4 [68, 69].



(a)



(b)

Figure 2-1. Schematic orbital structure of the conduction-band minimum in crystalline and amorphous phase in (a) covalent bond as Si and (b) ionic bond as oxide semiconductor



Figure 2-2. Progress of oxide TFT technology (Ref. Displaybank)

	a-Si TFTs	Poly-Si TFTs	nc-Si TFTs	Oxide TFTs
Mobility (cm²/V·sec)	0.4~0.8	30~400	0.5~250	5~100
Uniformity	Good	Medium	Good	Good
Reliablility	Bad	Good	Good	Good
Cost	Low	High	Medium	Low
Yield	High	Low	Medium	High

Table 2-1. Comparison of TFTs with various active layers

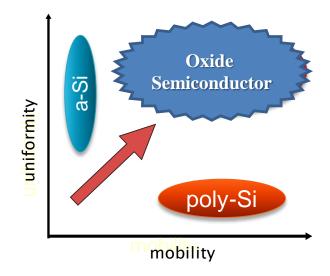


Figure 2-3. The advantages of oxide semiconductors compared with a-Si and

poly-Si



Figure 2-4. Transparent and flexible displays

2.2 Advantages of solution-process

The deposition method of semiconductor materials for the active matrix backplane TFTs could be divided into vacuum process and non-vacuum process. Deposition methods based on non-vacuum solution-processes such as spincoating, dip-coating, and ink-jet printing require no pumping down time and are not limited by the size of the vacuum chamber. Therefore, they are compatible with low production cost for manufacturing devices and large-area thin film fabrication, while vacuum processes such as rf magnetron sputtering and pulsed laser deposition require a high manufacturing cost and have poor uniformity. Solution-processes are also suitable for high-throughput and direct patterning, so that they have attracted considerable attention for low cost, large size, and high-throughput display fabrication method [70, 71].

Solution-processes are the simple deposition method with the solution from the solute of precursors or nano-particle and the solvent on the substrate, afterward apply the annealing process to the solution for solid thin film.

There are two representative synthesis method of solution, employing the solute of precursors or nano-particle. The solution could be synthesized from precursors, a compound that participates in the chemical reaction that produces another compound, or nano-particle, semiconductor materials as themselves which approach to the nano-scale [72-75].

Lower fabrication temperature could be achieved employing nano-particle than precursors, but the thin film deposited by nano-particle has grain boundary, because nano-particle thin film is the bonding combination of semiconductor paricles, which causes mobility degradation [76]. On the other hand, the thin film deposited by precursors has fine amorphous film quality in spite of higher fabrication temperature.

Various deposition types of solution-processes are described in Figure 2-5. Spincoating is a procedure used to deposit uniform thin films to flat substrates and usually a small amount of coating material is applied on the center of the substrate, then rotate at high speed in order to spread the coating material uniformly by centrifugal force [77]. Dip-coating is a method of depositing thin films by immersing the substrate in the solution of the coating material at a constant speed. Ink-jet printing is a deposition type by propelling droplets of ink onto substrate in order to make the pattern formation [78-80].

Si, organic semiconductors, and oxide semiconductors have been vigorously investigated in solution-processes among various semiconductor materials. Figure 2-6 shows the comparison of solution-processible semiconductor materials [81-85]. The solution types of all semiconductors, Si, organic, and oxide, could be precursors or nano-particle. Solution-processed Si has merits of the mature fabrication industry and the feasibility material for both p-type and ntype, but also has demerits of oxidation of Si and process complexity in case of laser application. Solution-processed organic semiconductors could be fabricated with low process temperature and have suitability for transparency, flexibility, and mechanical stability, but their relatively low electrical performance is issue. Solution-processed oxide semiconductors have advantages of high electrical performance, transparency, flexibility, wide range of materials, controllability of electrical properties by atomic composition, but also have disadvantages of high process temperature and improving reliability [86].

Among these various semiconductor materials, solution-processed oxide semiconductors have superior electrical and chemical characteristics, so that may be the promising candidate for the next generation active matrix backplane TFTs to high-resolution, high frame rate operation, large size, transparent, and flexible display [87].

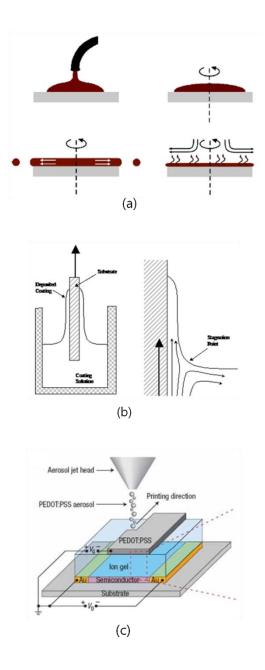


Figure 2-5. The deposition types of solution-process as (a) spin-coating, (b) dipcoating, and (c) ink-jet printing

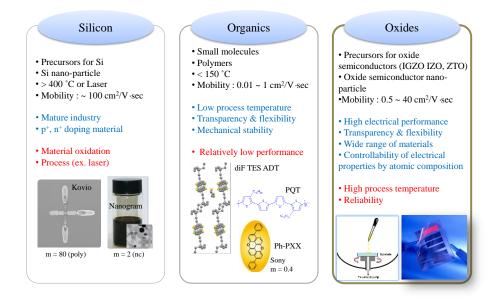


Figure 2-6. The comparison of solution-processible semiconductor materials

2.3 Solution-processed oxide TFTs

Solution-processed oxide TFTs with zinc-tin-oxide (ZTO) and indium-galliumzinc-oxide (IGZO) have attracted considerable attention for the driving elements of active matrix display, instead of Si-based TFTs and organic TFTs, because of high mobility, visible light transparency, flexibility, wide range of materials, and controllability of electrical properties by atomic composition [88-91]. Table 2-2 describes the comparison of various solution-processed semiconductor TFTs. Solution-processed oxide TFTs show superior performance for AMLCD and AMOLED display backplanes, compared with solution-processed Si and organic TFTs which have a number of issues. Furthermore, solution-processed oxide TFTs are compatible with large area due to good uniformity and high throughput, so that could be a method for achieving low cost fabrication contrary to vacuum processes.

Among various ZnO-based oxide semiconductors, ZTO TFTs employing tin (Sn) material maybe promising candidates for achieving low cost processes because Sn is a quite low cost material compared with widely used indium (In) [92-95]. Therefore, ZTO TFTs employing Sn maybe promising candidates for achieving low cost processes.

Solution-processed ZTO TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic for additional cost reduction and application extension to a flexible display. For solution-processed ZTO TFTs fabrication with these flexible substrates, low temperature processes are necessary because these substrates are easily damaged at high annealing temperatures. At low annealing temperature, however, solution-processed ZTO TFTs have poor performance such as low on-current, high threshold voltage and low mobility, so a rather high annealing temperature exceeding 500 °C is required in solutionprocessed ZTO TFTs as investigated in the transfer characteristics of Figure 2-7 and the electrical characteristics of Table 2-3 of solution-processed ZTO TFTs with various annealing temperature [96, 97]. To improve the device characteristics of solution-processed oxide TFTs even at low annealing temperature on an active layer, a study of the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs and the efforts to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature on active layer are desired. There were some efforts to investigate the effects of annealing temperature on solution-processed oxide TFTs as shown in Figure 2-8, but the electrical and chemical mechanisms of annealing temperature on solution-processed oxide TFTs have been scarcely studied [98, 99].

The purpose of this thesis is to fabricate oxide TFTs employing solution-process for an oxide semiconductor active layer with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability, and to improve the electrical characteristics of low temperature solution-processed oxide TFTs for active matrix display.

31

Solution-processed	Poly-Si TFTs	Organic TFTs	Oxide TFTs
Туре	Precursor Nano-particle	Small Molecule Polymer	Precursor Nano-particle
Process Temp.	>400 °C or Laser	<150 °C	400~600 °C 200~300 °C
Mobility	108	0.01 ~ 1	0.5~44
Reliability	0	×	Δ
Transparency	×	0	0
Display Mode	LCD/OLED	EPD, Flexible	LCD/OLED
Issue	Air stability of ink Toxic precursor High temp. or Laser Crystalline phase	Low mobility Bias stability	High temp.

Table 2-2. Comparison of various solution-processed semiconductor TFTs

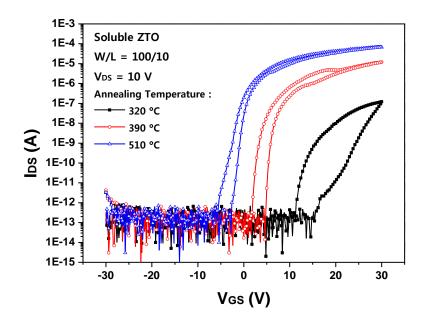


Figure 2-7. Transfer characteristics of solution-processed ZTO TFTs with various annealing temperature

Annealing temperature	Vth (V)	I _{on} /I _{off} [10 ^x]	µsat (cm²/V·sec)	S.S (V/decade)
320 °C	28.43	5	0.02	2.57
390 °C	6.68	7	0.36	0.63
510 °C	-0.48	8	2.09	0.34

Table 2-3. The electrical characteristics of solution-processed ZTO TFTs with various annealing temperature

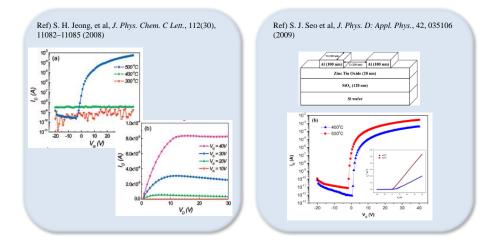


Figure 2-8. Previous report to investigate the effect of annealing temperature on solution-processed ZTO TFTs

Chapter 3 Optimization of the fabrication process of solution-processed oxide TFTs

3.1 Overview

Solution-processed oxide TFTs with ZTO and IGZO have attracted considerable attention for the driving elements of active matrix display, instead of Si-based TFTs and organic TFTs, because of high mobility, visible light transparency, flexibility, wide range of materials, and controllability of electrical properties by atomic composition. Furthermore, solution-processed oxide TFTs are compatible with large area due to good uniformity and high throughput, so that could be a method for achieving low cost fabrication contrary to vacuum processes.

Among various ZnO-based oxide semiconductors, ZTO TFTs employing Sn material maybe promising candidates for achieving low cost processes because Sn is a quite low cost material compared with widely used In. Therefore, ZTO TFTs employing Sn maybe promising candidates for achieving low cost processes.

To optimize the fabrication process of solution-processed ZTO TFTs for high and stable electrical characteristics, a number of issues should be investigated in regards of the TFT structure, the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation, and so on [100-104].

The purpose of this chapter is to optimize the fabrication process of ZTO TFTs employing solution-process for an oxide semiconductor active layer with various condition of the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation to investigate the effects of fabrication process condition on the electrical characteristics of solution-processed ZTO TFTs such as threshold voltage, saturation mobility, and reliability.

3.2 Structure of solution-processed oxide TFTs

There are four major typical classes of TFT devices: (a) staggered top gate, (b) staggered bottom gate (SBG), (c) coplanar top gate, and (d) coplanar bottom gate, as shown in Figure 3-1.

Staggered structure means that source / drain and gate are placed on the opposite sides if the channel layer, whereas they locates on the same side in coplanar structure. The inverted staggered structure is most widely used in the oxide TFTs, since it is the most commonly used among the commercial TFTs in the active matrix display [105]. Thus, for the achievement of conventional a-Si TFT compatible process, the inverted staggered structure is considered most appropriate one.

For the conventional TFTs, the inverted staggered bottom gated structure of a-Si TFT was most widely used in the industry since it maximizes the advantage of sequential deposition of gate insulator, channel layer and doped layer. However, for poly-Si TFT, which require additional ion doping and activation process, top gate coplanar structure has been preferentially selected [106-108].

The inverted staggered structure is most widely used in the oxide TFTs, since it is the most commonly used among the commercial TFTs in the active matrix display [109, 110]. Thus, for the achievement of conventional a-Si TFT compatible process, the inverted staggered structure is considered most appropriate one.

In this thesis, solution-processed ZTO TFTs were fabricated with inverted staggered structure on the silicon wafer substrates as shown in Figure 3-2. Heavily boron doped p-type silicon wafer substrate and thermal oxidized silicon dioxide (SiO₂) were used as the gate and gate insulator, respectively [111].

The precursor-based solution of ZTO for active layer was prepared with zinc chloride ($ZnCl_2$) and Tin (II) chloride ($SnCl_2$) powders in Acetonitrile (CH_3CN) at equal molar ratios of 0.07 M. The formula weight of $ZnCl_2$ is 136.3, so that the weight of $ZnCl_2$ would be 0.029 g with a quantity of 3 ml of solvent by the follwing equation, explained in chapter 1.2 above.

$$FW[g/mol] \times 3 ml \times M [mol/L] = W [g]$$

(FW : Formula weight [g/mol], M : Molarity(Molar ratio) [mol/L], W : weight [g])

The formula weight of $SnCl_2$ is 189.6, so that the weight of $SnCl_2$ would be 0.04 g with a quantity of 3 ml of solvent by the same equation

The density of solvent CH₃CN is 0.782, so that the weight was matched as 2.346 g with a quantity of 3 ml as following equation, explained in chapter 1.2 above. The property of solute as zinc chloride (ZnCl₂) and Tin (II) chloride (SnCl₂) powders and solvent as Acetonitrile (CH₃CN) for the synthesis of solution of ZTO is demonstrated in Table 2-1.

d [g/ml] × 3 ml = W [g] (d : density [g/ml], W : weight [g])

The mixed precursor-based solution of ZTO was stirred at room temperature to promote the dissolving process and deposited by spin-coating with 500 rpm for 6 sec and sequentially 4000 rpm for 30 sec. The deposited ZTO active layer was soft-baked at 200 °C for 10 min with the slow increase and slow decrease in

temperature to solidify the ZTO active layer without pore. To avoid the fringing effect and a large leakage current, the soft-baked ZTO active layer was patterned by the photolithography employing wet-etching process with diluted HF. The photoresist (PR) GXR 601 for photolithography was spin-coated with 500rpm for 6sec and sequentially 3000rpm for 20sec, and soft-baked at 100 °C for 2 min. The exposure was performed employing MA-6 with the wavelength of 365 nm for 9 sec and developed in DPD200 for 40 sec. After hard-baking at 100 °C for 2 min, ZTO active layer was wet-etched in diluted HF as 500 : 1 with deionized water (DI water). The PR was stripped in acetone for 10 sec.

The pattened ZTO active layer were annealed at 500 °C for 10 min by rapid thermal annealing (RTA) process. The cross-sectional view of ZTO active layer, SiO_2 gate insulator, and Si wafer substrate is shown as Figure 3-3 by transmission electron microscopy (TEM).

After the patterned ZTO active layer were formed on the SiO₂, indium zinc oxide (IZO) film was deposited by dc sputtering with the thickness of 1000 Å and then defined by a lift-off process of PMMA (Poly(methyl methacrylate)) / PR double layer to yield source and drain electrodes. The plane view of the patterned solution-processed ZTO TFTs with ZTO active layer and IZO source/drain electrodes is demonstrated in Figure 3-4 by microscope.

Finally a PMMA layer was employed for passivation with the thickness of 2000 Å by spin-coating to protect the active layer from moisture in the air.

The sequence of the fabrication process of solution-processed ZTO TFTs on Siwafer substrate is summarized in Figure 3-5.

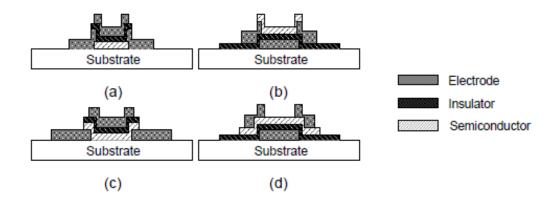


Figure 3-1. Typical structure of TFT : (a) top gate co-planar, (b)bottom gate coplanar, (c) top gate staggered, and (d) bottom gate staggered

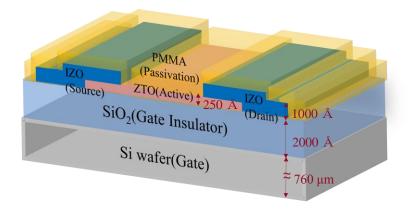


Figure 3-2. Inverted staggered structure of solution-processed ZTO TFTs

Table 3-1. The property of solute as zinc chloride (ZnCl₂) and Tin (II) chloride (SnCl₂) powders and solvent as Acetonitrile (CH₃CN) for the synthesis of solution of ZTO

ZTO	Zn	Sn	
Solute	Zinc chloride, ZnCl ₂	Tin chloride, SnCl ₂	
Solute	(FW=136.3, d=2.907)	(FW=189.6, d=3.95)	
Column	ile, CH₃CN		
Solvent	(d=0.782)		

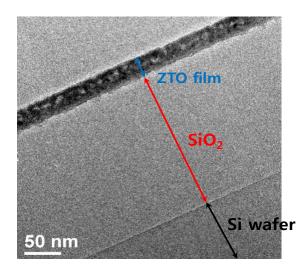


Figure 3-3. Cross-sectional view of ZTO active layer, SiO $_{\rm 2}$ gate insulator, and Si wafer substrate

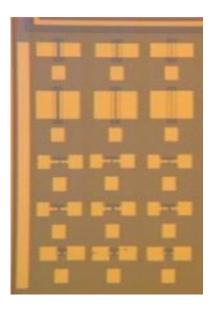


Figure 3-4. Plane view of the patterned solution-processed ZTO TFTs with ZTO active layer and IZO source/drain electrodes

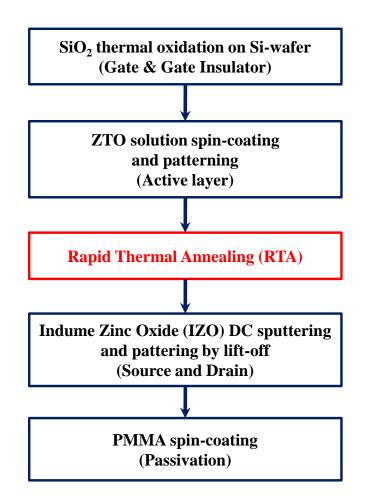


Figure 3-5. Sequence of the fabrication process of solution-processed ZTO TFTs

on Si-wafer substrate

3.3 Stirring time on solution-processed oxide TFTs

To optimize the fabrication process of solution-processed ZTO TFTs for high and stable electrical characteristics, a number of issues should be investigated in regards of the TFT structure, the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation, and so on.

In this section, the stirring time of ZTO semiconductor solution was varied to investigate to effect of stirring time on the electrical, optical, and chemical characteristics of solution-processed ZTO TFTs and to optimize the fabrication process of ZTO TFTs employing solution-process for an oxide semiconductor active layer for high and stable electrical characteristics [112].

The precursor-based solution of ZTO for active layer was prepared with zinc chloride (ZnCl₂) and Tin (II) chloride (SnCl₂) powders in Acetonitrile (CH₃CN) at equal molar ratios and stirred at room temperature to promote the dissolving process with various stirring time of 15, 30, 60, and 90 min.

Figure 3-6 shows the transfer characteristics of solution-processed ZTO TFTs according to various stirring time of ZTO solution with an annealing temperature of 500 ° with W / L = 100 / 10 μ m and V_{DS} = 10 V. When the stirring time of ZTO solution was decreased from 90 min to 15 min, the transfer characteristic of solution-processed ZTO TFTs was improved as the threshold voltage was increased to 0 V and the subthreshold swing (S.S) was decreased. The improvement of the transfer characteristics of solution-processed ZTO TFTs according to the decrease in stirring time was caused by the decrease in the halide residues such as Cl which was included in precursors. The decrease in the halide residues such as Cl could be investigated with thermogavimetry analysis (TGA), differential thermal analysis (DTA), and transmittance [113, 114].

The thermogavimetry analysis (TGA) and differential thermal analysis (DTA) results of ZTO solution with the increase in temperature according to various stirring time of ZTO solution was demonstrated in Figure 3-7. TGA is a method of thermal analysis in which changes in physical and chemical properties of materials, such as weight loss, are measured as a function of increasing temperature (with constant heating rate). Differential thermal analysis (or DTA) is a thermoanalytic technique, in which the material under study and an inert reference are made to undergo identical thermal cycles, while recording any temperature difference between sample and reference [115]. In Figure 3-7 (a) of TGA results, the ZTO solution underwent the evaporation of solvent, the pyrolysis, and the solidification of ZTO active layer with the increase in temperature. The ZTO solution with the stirring time of 15 min was first pyrolyzed at lowest temperature [116]. In Figure 3-7 (b) of DTA results, the ZTO solution underwent endothermic reaction which means the melting of ZTO precursors and exothermic reaction which means the solidification of ZTO solution. The ZTO solution with the stirring time of 15 min was first stablized at lowest temperature. The TGA and DTA results of ZTO solution show that the increase of precipitate such as halide residues according to the increase of stirring time retards the decomposition of ZTO precursors.

The transmittance of spin-coated ZTO active layer on bare glass with the increase in temperature according to various stirring time of ZTO solution was demonstrated in Figure 3-8. When the stirring time of ZTO solution decreased from 90 min to 15 min, the transmittance of ZTO active layer was increased up to 97 % at the wavelength of 500 nm. The improvement of transmittance of ZTO active layer would be caused by the decrease of precipitate such as halide residues when the stirring time decreased [117].

Therefore, the threshold voltage and subthreshold swing of solution-processed

ZTO TFTs were improved with the decrease in stirring time of ZTO solution due to the decrease of precipitate, investigated in the TGA, DTA, and transmittance results.

Figure 3-9 demonstrates the transfer characteristics of solution-processed ZTO TFTs with stirring time of 15 and 30 min, and their post-annealed results at 200 °C for 120 min. When compared the transfer characteristic with stirring time of 15 and that of 30 min and/or compared the post-annealed transfer characteristic with stirring time of 15 and that of 30 min, it is observed again that the threshold voltage, subthreshold swing, and on-current of solutionprocessed ZTO TFTs were improved with the decrease in stirring time of ZTO solution due to the decrease of precipitate, and the precipitate would not be removed by the post-annealing. The improvement of post-annealed transfer characteristics would be mainly due to the elimination of residues from PR and PMMA, and/or the moisture in the air, which are absorbed to the ZTO active layer during the fabrication process after the ZTO active layer was annealed, because the temperature of post-annealing is remarkably lower than that of ZTO active layer annealing temperature. However, when compared the transfer characteristic with stirring time of 15 and the post-annealed transfer characteristic with stirring time of 30 min, the precipitate during stirring of ZTO solution could be also eliminated during post-annealing because the latter has better electrical characteristics.

Figure 3-10 demonstrates the transfer characteristics of solution-processed ZTO TFTs with stirring time of 30 min according to various post-annealing time. The transfer characteristics of solution-processed ZTO TFTs were improved with the increase in post-annealing time because of the elimination of residues from PR and PMMA, the moisture in the air, and/or the precipitate during stirring of ZTO solution.

Therefore, the optimized stirring time of ZTO semiconductor solution for the least precipitate during stirring would be 15 min to achieve high and stable electrical characteristics of solution-processed ZTO TFTs, and the precipitate during stirring of ZTO solution could be eliminated by employing post-annealing treatment.

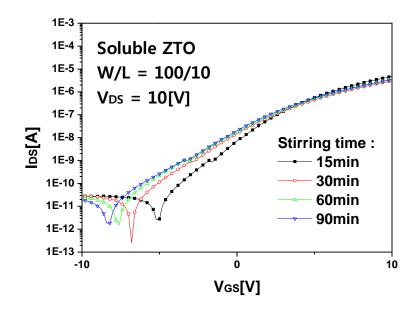
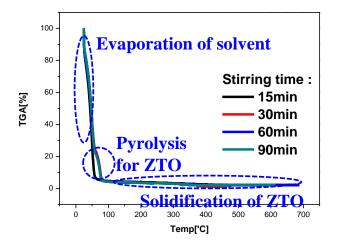
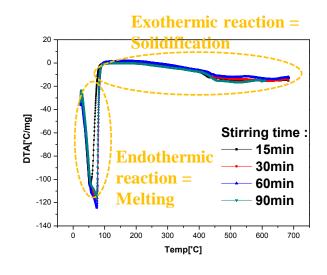


Figure 3-6. Transfer characteristics of solution-processed ZTO TFTs according to various stirring time of ZTO solution with an annealing temperature of 500 °C with W / L = 100 / 10 μ m and V_{DS} = 10 V



(a)



(b)

Figure 3-7. Thermogavimetry analysis (TGA) and differential thermal analysis (DTA) results of ZTO solution with the increase in temperature according to various stirring time of ZTO solution

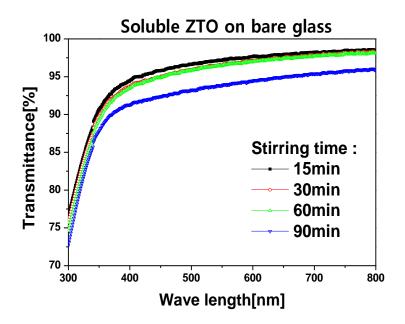


Figure 3-8. Transmittance of ZTO active layer on bare glass with the increase in temperature according to various stirring time of ZTO solution

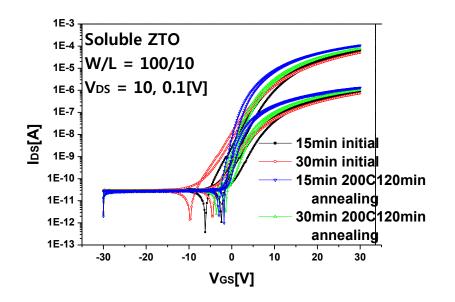


Figure 3-9. Transfer characteristics of solution-processed ZTO TFTs with stirring time of 15 and 30 min, and their post-annealed results at 200 °C for 120 min

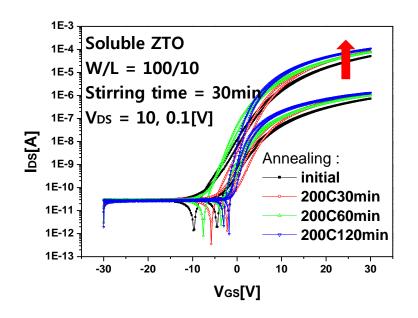


Figure 3-10. Transfer characteristics of solution-processed ZTO TFTs with stirring time of 30 min according to various post-annealing time at 200 $^{\circ}\mathrm{C}$

3.4 Active layer thickness on solution-processed oxide TFTs

To optimize the fabrication process of solution-processed ZTO TFTs for high and stable electrical characteristics, a number of issues should be investigated in regards of the TFT structure, the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation, and so on.

In previous report, the oxide TFTs has good electrical characteristics in regard of reliability as the active layer thickness increased [118]. Therefore, in this section, the ZTO active layer thickness was tried to be varied to investigate to effect of ZTO active layer thickness on the electrical characteristics of solution-processed ZTO TFTs and to optimize the fabrication process of ZTO TFTs employing solution-process for an oxide semiconductor active layer for high and stable electrical characteristics.

The rpm and time of ZTO active layer spin-coating were varied to control the thickness of deposited ZTO active layer. The thickness of spin-coated ZTO active layer before and after RTA 500 °C annealing according to the variation of rpm and time of spin-coating are shown in Table 3-2. When ZTO active layer was spin-coated with 4000 rpm for 30 sec, the initial thickness was 400 Å by measuring with alpha stepper. When the rpm and time increased as 5000 rpm and 60 sec, the initial thickness of ZTO active layer was decreased to 350 Å. When the rpm and time decreased as 3000 rpm and 20 sec, the initial thickness of ZTO active layer was 400 Å, not increased so that 400 Å is the maximum thickness of ZTO active layer deposited by spin-coating with 1 time. Moreover, the thickness of ZTO active layer after RTA 500 °C annealing was 250 Å regardless of the spin-coating condition, so that the thickness of ZTO active layer

could not be controlled by spin-coating condition.

To increase the thickness of ZTO active layer, multi-coating process was performed. The transfer characteristics of solution-processed ZTO TFTs according to multi-coating with an annealing temperature of 500 °C with W / L = 100 / 10 μ m and V_{DS} = 10 V are shown in Figure 3-11. The transfer characteristics of solution-processed ZTO TFTs were degraded with the increase of the number of multi-coating time. The increase in off-current as (1) shows the creation of states at the interface of active layer and the decrease in on-current as (2) shows the quality degradation of front channel of first-coated active layer by repeated annealing process in Figure 3-11. Therefore, the multi-coating process of ZTO active layer could not be adopted to control the thickness of ZTO active layer [119].

Therefore, the optimized thickness of ZTO active layer would be 400 Å by 1 time spin-coating to achieve high and stable electrical characteristics of solution-processed ZTO TFTs.

* Alpha stepper							
	Initial	(RTA)	After annealing				
4000 rpm / 30 sec	400 Å	\rightarrow	250 Å				
5000 rpm / 60 sec	350 Å	\rightarrow	250 Å				
3000 rpm / 20 sec	400 Å	\rightarrow	250 Å				

Table 3-2. Thickness of spin-coated ZTO active layer before and after RTA 500 °C annealing according to the variation of rpm and time of spin-coating

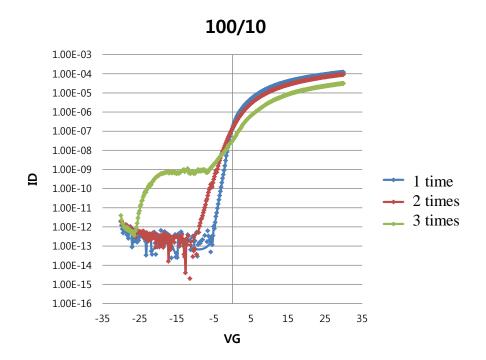


Figure 3-11. Transfer characteristics of solution-processed ZTO TFTs according to multi-coating with an annealing temperature of 500 °C with W / L = 100 / 10 $$\mu m$$ and V_{DS} = 10 V

3.5 Effects of passivation on solution-processed oxide TFTs

To optimize the fabrication process of solution-processed ZTO TFTs for high and stable electrical characteristics, a number of issues should be investigated in regards of the TFT structure, the stirring time of oxide semiconductor solution, the active layer thickness, the effects of passivation, and so on.

Especially, the passivation against the ambient atmosphere is desired to be investigated in-depthly for stable electrical characteristics because oxide semiconductors are reported to be sensitive to the ambient atmosphere and active matrix backplane TFTs for switching devices of LCD and current driving devices of OLED are exposed to the ambient atmosphere such as light, oxygen, and the moisture.

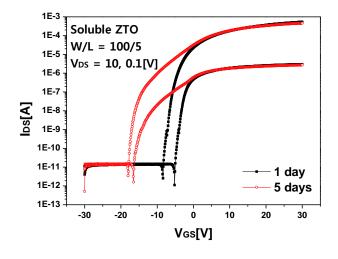
The electrical characteristics of oxide TFTs are affected by the ambient atmosphere because oxygen and the moisture could vary the electrical characteristics of back channel which is the surface of the oxide semiconductors to be adjacent to ambient atmosphere in recent reports [120, 121]. Therefore, the passivation for back channel of oxide semiconductors against the ambient atmosphere would improve the stability of solution-processed oxide TFTs.

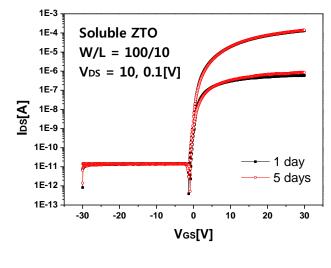
The vacuum process passivation is widely used as SiO_x and Al_2O employing plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) [122-124]. However, theses vacuum process passivation cause the damage to solution-processed oxide semiconductors due to physical bombardment by plasma or atoms. Moreover, vacuum process passivation is hard to achieve large size process due to the limitation of vacuum chamber size and poor uniformity. Therefore, solution-processed passivation is employed for the compatibility with low production cost for manufacturing devices, large-area thin film fabrication, and all solution-process fabrication.

In this section, the effects of passivation on the electrical characteristics of solution-processed ZTO TFTs were investigated. Widely used PMMA layer was employed for passivation at final fabrication process with the thickness of 2000 Å by spin-coating to protect the ZTO active layer from moisture in the air.

The stability for time of transfer characteristics of solution-processed ZTO TFTs according to the existence of passivation with an annealing temperature of 500 °C with $V_{DS} = 10$ V was demonstrated in Figure 3-12. The transfer characteristic of solution-processed ZTO TFTs without passivation was not stable with large negative shift due to the absorption of moisture in the air to ZTO active layer in 5 days at atmosphere condition as Figure 3-12 (a). On the other hand, the transfer characteristic of solution-processed ZTO TFTs with passivation was remarkably stable without shift due to the protection effects of PMMA passivation from the absorption of moisture in the air to ZTO active layer in 5 days at atmosphere condition as Figure 3-12 (b).

Therefore, the PMMA passivation would be desired to achieve high and stable electrical characteristics of solution-processed ZTO TFTs.





(b)

Figure 3-12. Stability for time of transfer characteristics of solution-processed ZTO TFTs (a) without passivation and (b) with PMMA passivation with an annealing temperature of 500 °C with V_{DS} = 10 V

3.6 Electrical characteristics of solution-processed oxide TFTs

3.6.1 Transfer characteristics

In regard of the optimized fabrication process above, solution-processed ZTO TFTs were fabricated with inverted staggered structure on the silicon wafer substrates as shown in Figure 3-2. Heavily boron doped p-type silicon wafer substrate and thermal oxidized silicon dioxide (SiO₂) with the thickness of 2000 Å were used as the gate and gate insulator, respectively.

The precursor-based solution of ZTO for active layer was prepared with zinc chloride ($ZnCl_2$) and Tin (II) chloride ($SnCl_2$) powders in Acetonitrile (CH_3CN) at equal molar ratios of 0.07 M.

The mixed precursor-based solution of ZTO was stirred for 15 min at room temperature to promote the dissolving process and deposited by spin-coating with 500 rpm for 6 sec and sequentially 4000 rpm for 30 sec. The deposited ZTO active layer was soft-baked at 200 °C for 10 min with the slow increase and slow decrease in temperature to solidify the ZTO active layer without pore. To avoid the fringing effect and a large leakage current, the soft-baked ZTO active layer was patterned by the photolithography employing wet-etching process with diluted HF.

The pattened ZTO active layer were annealed at 500 °C for 10 min by rapid thermal annealing (RTA) process.

After the patterned ZTO active layer were formed on the SiO₂, indium zinc oxide (IZO) film was deposited by dc sputtering with the thickness of 1000 \AA and then defined by a lift-off process to yield source and drain electrodes.

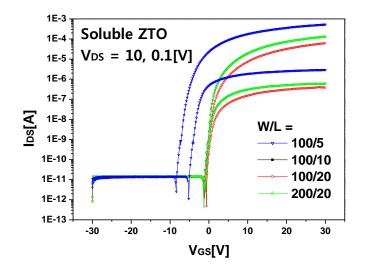
Finally a PMMA layer was employed for passivation with the thickness of 2000 Å by spin-coating to protect the active layer from moisture in the air.

The materials including the thickness and processes are summarized for each layer of solution-processed ZTO TFTs on Si-wafer substrate in Table 3-3.

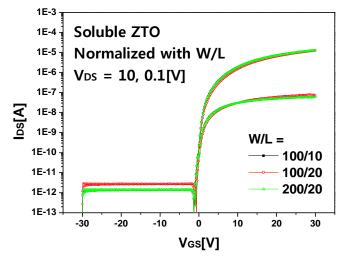
The transfer characteristics of solution-processed ZTO TFTs with an annealing temperature of 500 °C with $V_{DS} = 10$ V according to various channel width (W) and length (L) and normalized curves with W/L are shown in Figure 3-13 (a) and (b), respectively. The fabricated solution-processed ZTO TFT showed high performance of electrical characteristics such as on/off current ratio of 10⁷, threshold voltage of 0 V, saturation mobility of 3.5 cm²/V·sec, subthreshold swing of 0.125 V/dec, and a small hysteresis. The output characteristics of solution-processed ZTO TFTs with an annealing temperature of 500 °C with V_{DS} = 10 V of channel width of 100 μ m and length of (a) 5 μ m and (b) 10 μ m. The solution-processed ZTO TFTs with W/L of 100/5 showed the short channel effect in terms of the negative shift of transfer characteristic and no-saturated output characteristic.

Table 3-3. Materials including the thickness and processes for each layer ofsolution-processed ZTO TFTs on Si-wafer substrate

Layer	Material	Process
Gate	Si (760 µm)	Wafer
Gate Insulator	SiO ₂ (2000 Å)	Thermal Oxidation
Active layer	ZTO (250 Å)	Spin-coating
Source / Drain	IZO (1000 Å)	DC Sputtering
Passivation	PMMA (2000 Å)	Spin-coating

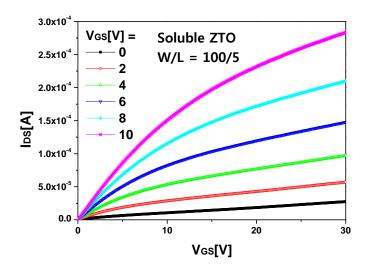


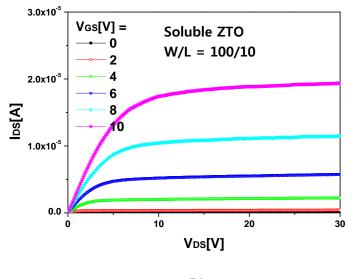
(a)



(b)

Figure 3-13. Transfer characteristics of solution-processed ZTO TFTs with an annealing temperature of 500 °C with $V_{DS} = 10$ V (a) according to various channel width (W) and length (L) and (b) normalized curves with W/L





(b)

Figure 3-14. Output characteristics of solution-processed ZTO TFTs with an annealing temperature of 500 °C with V_{DS} = 10 V of channel width of 100 µm and length of (a) 5 µm and (b) 10 µm

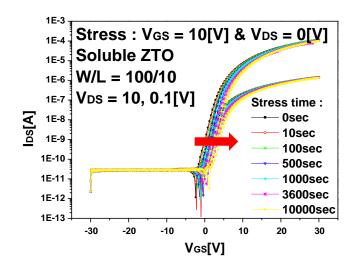
3.6.2 Reliability characteristics

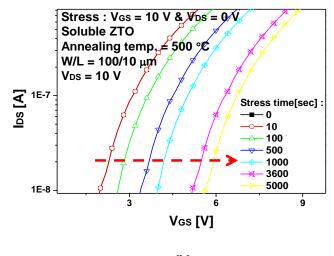
The fabricated solution-processed ZTO TFTs with $W/L = 100/10 \mu m$ were biasstressed by positive and negative gate bias to investigate the reliability characteristics. Figure 3-15 demonstrates the reliability characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C under positive gate bias-stress of 10 V for 5000 sec. Figure 3-16 demonstrates the reliability characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C under negative gate-bias stress of - 10 V for 5000 sec. The transfer curve shifted positively and negatively with parallel almost without change of slope with positive gate-bias stress and negative gate bias-stress, respectively. Therefore, this parallel shift of reliability characteristics demonstrates that the electrons are trapped or de-trapped rather than trap states are created by gate-bias stress.

Threshold voltage (Vth) shifts of solution-processed ZTO TFTs under positive gate-bias stress and negative gate-bias stress are shown in Figure 3-17. When positive gate-bias stress of 10 V was applied to solution-processed ZTO TFTs for 5000 sec, Vth was increased from 2.80 V to 5.34 V. On the other hand, when negative gate-bias stress of -10 V was applied for 5000 sec, Vth was decreased from 3.80 V to 1.34 V.

The recovery characteristics and effect of post-annealing for the gate-bias -stress are also investigated. The transfer curves under positive gate-bias stress of 10 V for 10000 sec, that of recovered characteristics after 1 week recovery under ambient condition, and that of post-annealed characteristics with 200 °C for 1 hour of solution-processed ZTO TFTs with annealing temperature of 500 °C are shown in Figure 3-18. The increased Vth under positive gate-bias stress was almost recovered after 1 week. Moreover, the post-annealing caused Vth slightly decreased. The transfer curves under negative gate-bias stress of - 10 V for 10000 sec, that of recovered characteristics after 1 week recovery under ambient condition, and that of post-annealed characteristics with 200 °C for 1 hour of solution-processed ZTO TFTs with annealing temperature of 500 °C are shown in Figure 3-19 (a). The decreased Vth by negative gate-bias stress was recovered to the positive shift after 1 week. Moreover, the post-annealing caused Vth slightly decreased. Figure 3-19 (b) shows that the decreased Vth by negative gate bias-stress for 10000 sec was almost recovered in about 2 hours. These fast recoveries could be explained that the electrons trapped under gate-bias stress would be located at shallow trap states.

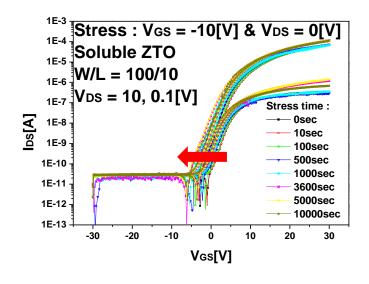
Furthermore, after enough recovery after 1 week, the Vth was slightly increased compared with the initial Vth, under both positive and negative gate-bias stress. Moreover, post-annealing causes Vth slightly decreased under both positive and negative gate-bias stress. These are explained that the oxidation under ambient condition causes oxygen vacancies decreased, so that the decrease in electron concentration result in the increase in Vth within recovery, and the post-annealing causes the evaporation of oxygen, so that the increase in electron concentration result in the decrease in Vth.



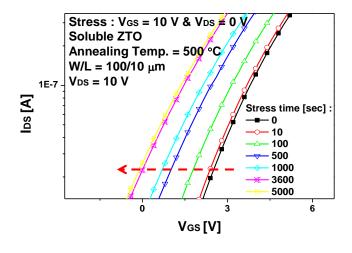


(b)

Figure 3-15. Reliability characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C under (a) positive gate-bias stress of 10 V for 5000 sec and (b) that of enlarged curve



(a)



(b)

Figure 3-16. Reliability characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C under (a) negative gate-bias stress of - 10 V for 5000 sec and (b) that of enlarged curve

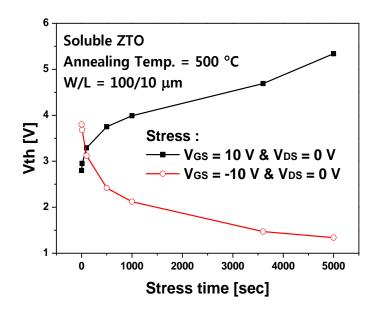


Figure 3-17. Threshold voltage (Vth) shift of solution-processed ZTO TFTs with annealing temperature of 500 °C under positive gate-bias stress and negative gate-bias stress

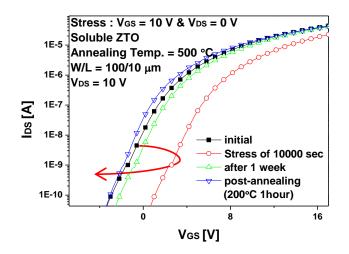
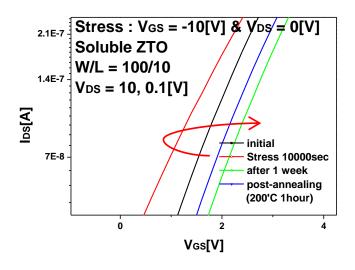
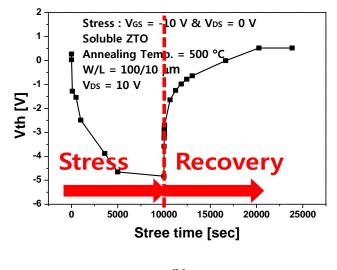


Figure 3-18. Reliability under positive gate-bias stress, recovery under ambient condition, and post-annealed characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C





(b)

Figure 3-19. Reliability under negative gate-bias stress, recovery under ambient condition, and post-annealed characteristics of solution-processed ZTO TFTs with annealing temperature of 500 °C as (a) transfer curve and (b) Vth shift

Chapter 4 Effects of Annealing Temperature on Solutionprocessed oxide TFTs

4.1 Motivation

Solution-processed oxide TFTs with ZTO and IGZO have attracted considerable attention for the driving elements of active matrix display for AMLCD and AMOLED, instead of Si-based TFTs and organic TFTs, because of high mobility, visible light transparency, flexibility, wide range of materials, and controllability of electrical properties by atomic composition [125-127]. Furthermore, solution-processed oxide TFTs are compatible with large area due to good uniformity and high throughput, so that could be a method for achieving low cost fabrication contrary to vacuum processes [128, 129].

Among various ZnO-based oxide semiconductors, ZTO TFTs employing Sn material maybe promising candidates for achieving low cost processes because Sn is a quite low cost material compared with widely used In [128]. Therefore, ZTO TFTs employing Sn maybe promising candidates for achieving low cost processes.

Solution-processed ZTO TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic for additional cost reduction and application extension to a flexible display. For solution-processed ZTO TFTs fabrication with these flexible substrates, low temperature processes are necessary because these substrates are easily damaged at high annealing temperatures. At low annealing temperature, however, solution-processed ZTO TFTs have poor performance such as low on-current, high threshold voltage and low mobility, so a rather high annealing temperature exceeding 500 °C is required in solution-processed ZTO TFTs [130, 131]. To improve the device characteristics of solution-processed oxide TFTs even at low annealing temperature on an active layer, a study of the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs and the efforts to achieve high

device characteristics of solution-processed oxide TFTs even at low annealing temperature on active layer are desired. There were some efforts to investigate the effects of annealing temperature on solution-processed oxide TFTs, but the electrical and chemical mechanisms of annealing temperature on solutionprocessed oxide TFTs have been scarcely studied.

In this chapter, oxide TFTs were fabricated employing solution-process for an oxide semiconductor active layer with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability.

4.2 Fabrication of solution-processed ZTO TFTs with various annealing temperature

Solution-processed ZTO TFTs with inverted staggered structure were fabricated on silicon wafer substrates to observe the effect of annealing temperature effectively, as shown in Figure 4-1. Heavily boron-doped p-type silicon wafer substrates and thermally oxidized silicon dioxide (SiO₂) of 2,000 Å were used as the gate and gate insulator, respectively [132].

The precursor-based solution of ZTO for the active layer was prepared with 0.07 M of zinc chloride (ZnCl₂) and 0.07 M of tin (II) chloride (SnCl₂) powders in acetonitrile (CH₃CN) of 3 mL at equal molar ratios. The mixed solution was stirred at room temperature for 15 min to promote the dissolving process. The ZTO active layer was deposited by spin-coating and isolated by the wet-etching process using diluted HF, and the ZTO active layers were annealed at 300 - 500 °C for 10 min by RTA under ambient condition.

After the ZTO active layers were formed on the SiO₂, an IZO film was deposited by dc sputtering and then defined by a lift-off process to yield source and drain electrodes. Finally, a PMMA layer was employed for passivation to protect the active layer from water, oxygen, and hydrogen in the air from the ambient atmosphere.

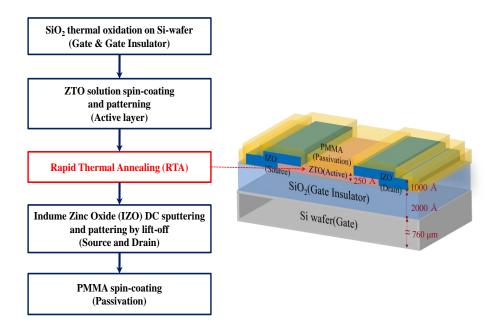


Figure 4-1. (a) Sequence of fabrication process and (b) structure of solutionprocessed ZTO TFTs

4.3 Electrical characteristics with the increase in annealing temperature

The drain current-gate voltage transfer characteristics of solution-processed ZTO TFTs with a length (L) of 10 μ m and width (W) of 100 μ m in the dark at room temperature are investigated as shown in Figure 4-2. The electrical characteristics of solution-processed ZTO TFTs with the annealing temperature from 300 to 500 °C are summarized in Table 4-1. When the annealing temperature increased from 300 to 500 °C, the on-current was gradually increased, while the off-current was scarcely altered, so that the on/off current ratio was increased. And the threshold voltages in particular were drastically decreased in the negative direction.

The threshold voltage of solution-processed ZTO TFTs decreased gradually from 16.89 to - 0.23 V with the increase in annealing temperature from 300 to 500 °C. The threshold voltages were derived by employing the widely used "constant current method" from the measured transfer characteristics in Figure 4-2 at a drain-source current of 100 nA with forward swing. Furthermore, because the transfer characteristics of a solution-processed ZTO TFTs are usually slightly changed with each measurement, the threshold voltages of Table 4-1 are the averaged values of many measurements and are expressed with the error bars. The saturation mobility of solution-processed ZTO TFTs increased from 0.18 to 4.75 cm²/V·sec with the increase in annealing temperature from 300 to 500 °C.

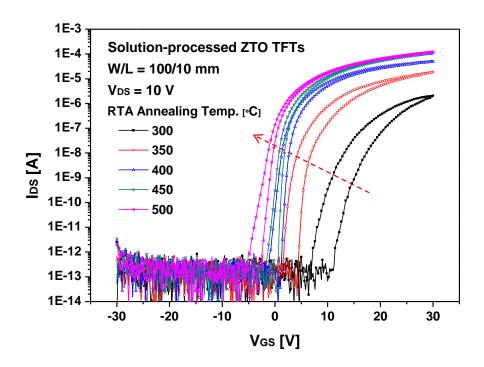


Figure 4-2. Transfer characteristics of solution-processed ZTO TFTs with the annealing temperature of 300 - 500 °C with W / L = 100 / 10 μ m and V_{DS} = 10 V

Annealing Temperature [°C]	I_{on}/I_{off}	$Vth (* V_{DS} = 10 V)$ [V]	μ _{sat} [cm²/Vsec]
300	106	16.89	0.18
350	107	6.55	0.91
400	4×10^{7}	2.38	1.47
450	8 × 10 ⁷	1.59	2.23
500	10 ⁸	-0.23	4.75

Table 4-1. Electrical characteristics of solution-processed ZTO TFTs with the annealing temperature of 300 - 500 °C with W / L = 100 / 10 μm and V_{DS} = 10 V

4.4 Dechlorination on threshold voltage with the increase in annealing temperature

In recent reports on sputter-processed oxide TFTs, the variation of threshold voltage has been analyzed by the change of electron concentration. The decrease in threshold voltage in solution-processed ZTO TFTs can be understood similarly to the increase in electron concentration of the ZTO active layer.

Hall measurement result confirmed that when the annealing temperature increased from 200 to 500 °C, the electron concentration of the ZTO active layer increased from 1.9 \times 10¹⁶ to 5.6 \times 10¹⁷, and accordingly, the threshold voltage decreased, as shown in Figure 4-3.

The increase in electron concentration of the ZTO active layer with annealing temperature could be explained by the removal of impurities such as C and/or Cl, which come from precursors such as ZnCl₂ and SnCl₂ or CH₃CN [133]. This reduction of impurities could be supported by the densification of the ZTO active layer after annealing. The thickness of the ZTO active layer was decreased from 420 to 300 Å when the annealing temperature increased from 300 to 500 °C, as measured by transmission electron microscopy (TEM), as shown in Figure 4-4. The rutherford backscattering spectrometry (RBS) result also demonstrates the decrease in Cl atomic concentration from 14.39 to 3.83 % in the ZTO active layer when the annealing temperature increased from 300 to 500 °C, as shown in Figure 4-5. In contrast to the decrease in Cl atomic concentration, C atomic concentration was scarcely altered regardless of annealing temperature and was maintained at a considerably small quantity of about 2.7 %. This shows that C impurities were sufficiently removed under 300 °C, so the removal of Cl would be dominant to the electrical characteristics of the ZTO active layer. On the other

hand, O atomic concentration increased from 36.24 to 47.19 % corresponding to the decrease in Cl atomic concentration, so consequently, Zn and Sn atoms would be more tightly bound to O atoms when the annealing temperature increased. These findings could be confirmed with Raman spectroscopy result whih shows the decrease in binding energy of the ZTO active layer from OH-Cl bonding of hydrogen bond to Zn-O and Sn-O bonding of ionic bond with the increase in annealing temperature [134]. Furthermore, when the binding energy of oxygen decreases, the energy level of oxygen vacancies becomes close to the conduction energy minimum level so that oxygen vacancies working as donors generate electrons more easily, and consequently the electron concentration of the ZTO active layer increases as. Modeling of dechlorination of ZTO active layer with the increase in annealing temperature is demonstrated in Figure 4-6. This increase in electron concentration is not a matter of the quantities of oxygen vacancies as many reports have mentioned because metal-oxide bondings are not sufficiently formed yet at low annealing temperature.

Therefore, the decrease in Cl atomic concentration with annealing temperature resulted in the increase in electron concentration of the ZTO active layer, and accordingly the threshold voltage of ZTO TFTs decreased with the increase of annealing temperature from $300 \,^{\circ}$ C to $500 \,^{\circ}$ C.

84

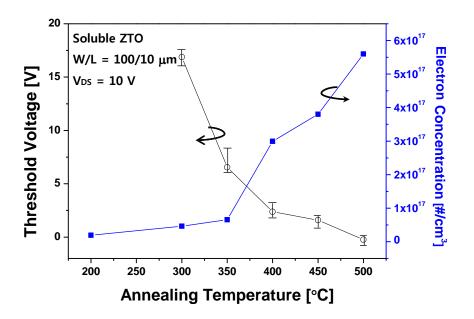


Figure 4-3. Threshold voltage and electron concentration of solution-processed ZTO TFTs with the annealing temperature of 200 - 500 $^\circ C$

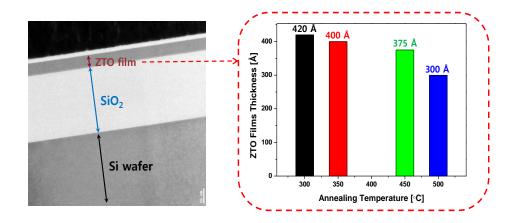


Figure 4-4. Cross-sectional image of ZTO active layer on SiO_2 gate insulator and wafer obtained by TEM and thickness of the ZTO active layer

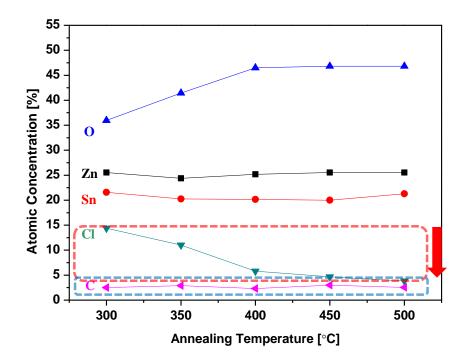
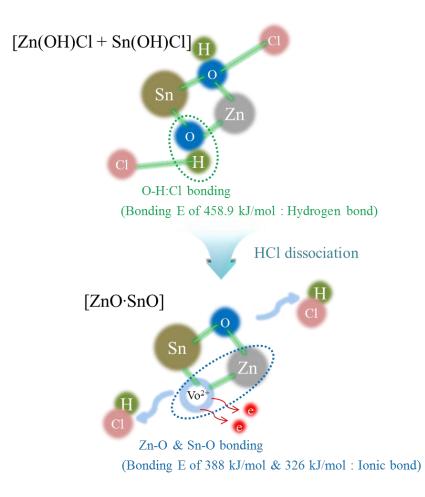
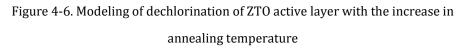


Figure 4-5. Atomic concentration of O, Cl, Zn, Sn, and C atoms of ZTO active layer with the annealing temperature obtained by RBS analysis





4.5 Dechlorination and crystallization on saturation mobility with the increase in annealing temperature

The saturation mobility of solution-processed ZTO TFTs increased from 0.18 to 4.75 cm²/V·sec with the increase in annealing temperature from 300 to 500 °C, and this result is also strongly related to the Cl atomic concentration as well as the microstructure of the ZTO active layer with annealing temperature, as shown in Figure 4-7.

In Region I, below an annealing temperature of 450 °C in Figure 4-7, the saturation mobility of ZTO TFTs was improved when the annealing temperature increased because halide residues such as Cl compounds in the ZTO active layer were decomposed, as confirmed by the RBS results in Figure 4-5. Halide residues in the ZTO active layer could be considered as trap states, so they could act as obstacles for electron accumulation and transportation of electrons in the conduction band, and they consequently reduce mobility. Figure 4-8 (a) shows a TEM diffraction pattern image of the ZTO active layer below 450 °C, and the ZTO active layer is amorphous in this region.

In Region II, above an annealing temperature of 450 °C in Figure 4-7, the saturation mobility of ZTO TFTs was drastically improved, compared with Region I, because the ZTO active layer was nano-crystallized in this region when the annealing temperature increased. Figure 4-8 (b) shows a TEM diffraction pattern and dark field images of the crystallized ZTO active layer, of which the crystalline grains are about 1 - 2 nm, and the grain size was gradually increased above 450 °C. Nano-crystallization above the annealing temperature of 450 °C reduced the amount of trap states of the interface between the ZTO active layer

and the SiO₂ gate insulator compared with those of the amorphous phase. Therefore, nano-crystallization as well as the decomposition of halide residues of the ZTO active layer improved the saturation mobility of solution-processed ZTO TFTs drastically because it decreased the amount of the defects of trap states in this region [135].

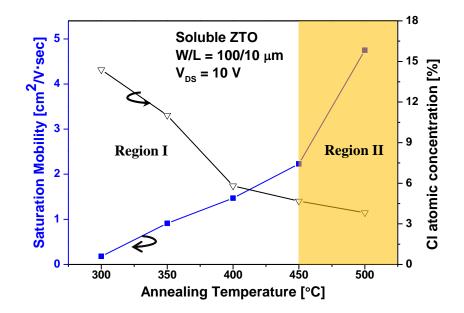
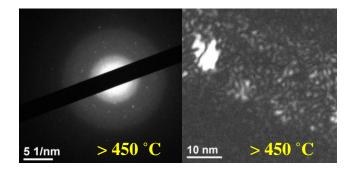


Figure 4-7. Saturation mobility of solution-processed ZTO TFTs and Cl atomic concentration with the annealing temperature





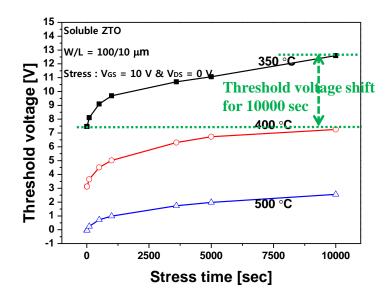
(b)

Figure 4-8. (a) Diffraction patterns below 450 °C and (b) diffraction pattern and dark field images above 450 °C of ZTO active layer obtained by TEM

4.6 Reliability characteristics with the increase in annealing temperature

The reliability characteristics according to annealing temperature for the active layer of solution-processed ZTO TFTs are demonstrated in Figure 4-9. With positive gate bias stress of 10 V during 10,000 s, the threshold voltage of ZTO TFTs increased from 7.5 to 12.84 V with an annealing temperature of 350 °C and from - 0.3 to 2.3 V with an annealing temperature of 500 °C, as shown in Figure 4-9 (a), with parallel shift without change of slope. In particular, the amount of threshold voltage shift for 10,000 s with various annealing temperatures is demonstrated in Figure 4-9 (b), showing that the threshold voltage shift for 10,000 s decreased from 5.34 V with an annealing temperature of 350 °C to 2.6 V with an annealing temperature of 500 °C.

The decrease in the threshold voltage shift for 10,000 s could also be explained with the decrease in Cl concentration and nano-crystallization of the ZTO active layer with the increase in annealing temperature from 300 to 500 °C. The reduction of halide residues such as Cl acting as trap states makes the number of trapped electrons at the ZTO active layer decreases and the nano-crystallization above the annealing temperature of 450 °C also makes the number of trapped electrons decreases at the trap states of the interface between the ZTO active layer and the SiO₂ gate insulator, so eventually the threshold voltage shift for 10,000 s decreases.



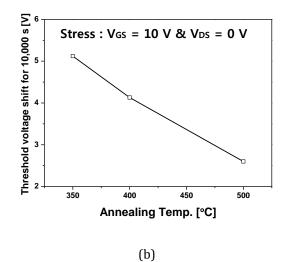


Figure 4-9. (a) Threshold voltage shift with positive gate bias stress and (b) threshold voltage shift for 10,000 s of solution-processed ZTO TFTs with the annealing temperature

4.7 Chemical formation equations with the increase in annealing temperature

According to the above analyses, which indicate that the Cl atomic concentration decreases and the ZTO active layer are nano-crystallized with increasing annealing temperature, the details of chemical formation equations could be established with the chemical characteristics of spin-coated ZTO solution with the annealing temperature using thermogavimetry analysis (TGA) and differential thermal analysis (DTA). The TGA and DTA curves of Fig. 9 could be divided into three regions.

An endothermic reaction in Region ① below 200 °C represents the evaporation of residual solvent and hydroxylation of metal chloride compounds with H_2O coming from air, and it can be expressed by equation (4-1). In this region, $ZnCl_2$ and $SnCl_2$ were transformed to Zn(OH)Cl and Sn(OH)Cl, respectively, so that Cl atomic concentration decreased with the increase in annealing temperature, but a considerable amount of Cl still remained below 200 °C. Therefore, Figure 4-5 shows a high Cl atomic concentration at low annealing temperature, and it is well-matched with the low carrier concentration of the ZTO active layer at 200 °C, as the Hall measurement result in Figure 4-3 showed.

$$ZnCl_2 + SnCl_2 + 2H_2O \rightarrow Zn(OH)Cl + Sn(OH)Cl + 2HCl(\uparrow)$$
(4-1)

Two exothermic reactions, occurred at 230 - 320 °C and 320 - 450 °C in Region ②, indicate the dehydroxylation of Sn(OH)Cl and Zn(OH)Cl with regard to the melting point of Sn of 232 °C and Zn of 420 °C, respectively. The dehydroxylated Sn(OH)Cl and Zn(OH)Cl would form the alloy of ZnO·SnO (ZTO), and this can be expressed by equation (4-2). Therefore, Cl atoms are gradually evaporated with HCl in this region, and the decrease in Cl atomic concentration in the RBS results of Figure 4-5 with the increase in annealing temperature could be well understood. As a result, the electron concentration of the ZTO active layer increases and the threshold voltage of solution-processed ZTO TFTs decreases gradually, as shown in Figure 4-3, and the saturation mobility increases gradually, as shown in Figure 4-7, with the increase in annealing temperature from 300 to 500 °C owing to the decrease in Cl atomic concentration in this region.

12Zn(OH)Cl + 12Sn(OH)Cl

$$\rightarrow 4\text{ZnO} \cdot \text{SnO} + \text{Zn}_2\text{OCl}_2 + \text{Sn}_2\text{OCl}_2 + 6\text{Zn}(\text{OH})\text{Cl} + 6\text{SnO} + 14\text{HCl}(\uparrow) + 2\text{H}_2\text{O}(\uparrow)$$

$$\rightarrow \text{ZnO} \cdot \text{SnO} + \text{HCl}(\uparrow) + \text{H}_2\text{O}(\uparrow) \qquad (4-2)$$

Another exothermic reaction in Region ③ above 450 °C is associated with the crystallization of the solution-processed ZTO active layer. This could be further supporting data for the nano-crystallization of the solution-processed ZTO active layer with regard to the TEM results and the dramatic increase in saturation mobility of solution-processed ZTO TFTs above 450 °C, as shown in Figure 4-7.

Therefore, the chemical mechanism of solution-processed ZTO active layer according to the increase in annealing temperature could be investigated as the formation of the metal-oxide thin film from metal-halide thin film with H_2O in the air by dechlorination process as demonstrated in Figure 4-11.

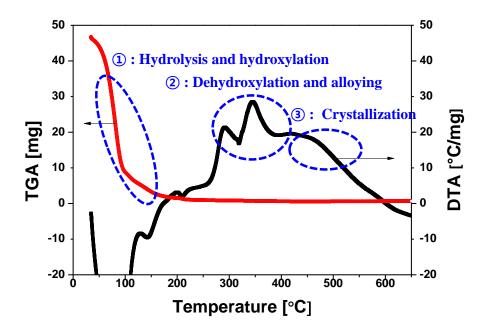


Figure 4-10. TGA and DTA results of ZTO solution with the annealing temperature

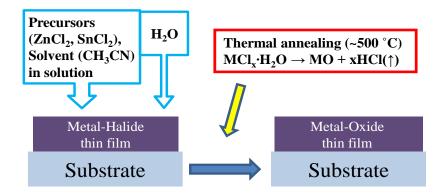


Figure 4-11. Chemical mechanism of solution-processed ZTO active layer according to the increase in annealing temperature as the formation of the metal-oxide thin film from metal-halide thin film with H₂O in the air by dechlorination process

4.8 Conclusion

In summary, the solution-processed ZTO TFTs with various annealing temperatures were fabricated, and the electrical characteristics of ZTO TFTs were improved with the increase in annealing temperature. The threshold voltage of solution-processed ZTO TFTs decreased from 16.89 to - 0.23 V with the increase in annealing temperature from 300 to 500 °C owing to the increase in electron concentration in the active layer. Hall measurement showed that the electron concentration increased because the oxygen vacancies generate electrons more easily as the binding energy of ZTO active layer decreased with the removal of Cl. The saturation mobility of solution-processed ZTO TFTs increased gradually from 0.18 to 4.75 cm²/V·sec with the increase in annealing temperature from 300 to 500 °C because of the decomposition of halide residues such as Cl and nano-crystallization. In regard of the reliability characteristics with increasing annealing temperature of solution-processed ZTO TFTs with a positive gate bias stress of 10 V, the threshold voltage shift for 10,000 s decreased from 5.34 to 2.6 V when the annealing temperature increases from 350 to 500 °C because of the reduction of trap states by the decrease in Cl and nano-crystallization.

The effects of annealing temperature on the active layer of solution-processed ZTO TFTs were successfully investigated and the chemical formation equation of the ZTO active layer with regard to the annealing temperature was established. Chapter 5 Improvement of low temperature solutionprocessed oxide TFTs

5.1 Improvement of low temperature solutionprocessed oxide TFTs employing O₂ plasma treatment

5.1.1 Motivation

The solution-processed oxide TFTs with ZTO and IGZO have attracted considerable attention for the driving elements of active matrix display because of high mobility, visible light transparency, and good uniformity. Furthermore, solution-process has suitability for large area and high throughput and could be a method for achieving low cost fabrication contrary to vacuum processes.

Among various ZnO-based oxide semiconductors, ZTO TFTs employing Sn material maybe promising candidates for achieving low cost processes because Sn is a quite low cost material compared with widely used In. Therefore, ZTO TFTs employing Sn maybe promising candidates for achieving low cost processes.

Solution-processed ZTO TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic for additional cost reduction and application extension to a flexible display. For solution-processed ZTO TFTs fabrication with these flexible substrates, low temperature processes are necessary because these substrates are easily damaged at high annealing temperatures. At low annealing temperature, however, solution-processed ZTO TFTs have poor performance such as low on-current, high threshold voltage and low mobility, so a rather high annealing temperature exceeding 500 °C is required in solution-processed ZTO TFTs. Therefore, the efforts to achieve high device characteristics of solution-processed ZTO TFTs even at low annealing temperature on active

layer are desired.

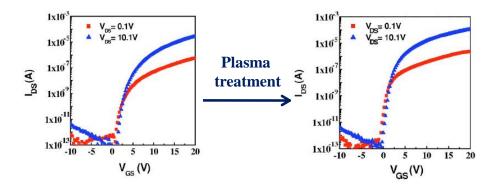
The solution-processed oxide TFTs has low conductance and low mobility with low annealing temperature because of its high concentration of halide residues such as Cl as observed in chapter 4.

Several previous papers showed that the plasma treatment could give rise to the energetic ion bombardment and result in physical momentum transfer and consequently preferential dissociation of light atom such as oxygen in sputtered oxide TFTs [136, 137]. Accordingly, oxygen vacancies would be increased so that ultimately the net electron concentration and hall mobility could be increased as shown in Figure 5-1 of previous work.

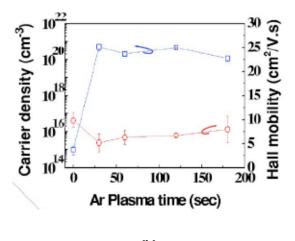
These plasma treatment effects of energetic ion bombardment could be applied to improve the electrical characteristics of low temperature solution-processed oxide TFTs by preferential dissociation on halide residues.

In this section, the electrical characteristics such as threshold voltage, saturation mobility, and reliability of solution-processed ZTO TFTs could be considerably improved by employing O_2 plasma treatment even at an low annealing temperature of 350 °C and to investigate the effects of O_2 plasma treatment on low temperature (350 °C) solution-processed ZTO TFTs.

102







(b)

Figure 5-1. Plasma treatment effects on (a) the transfer characteristics and (b) carrier density and hall mobility of sputtered oxide TFTs in previous work

5.1.2 Fabrication of solution-processed ZTO TFTs employing O₂ plasma treatment

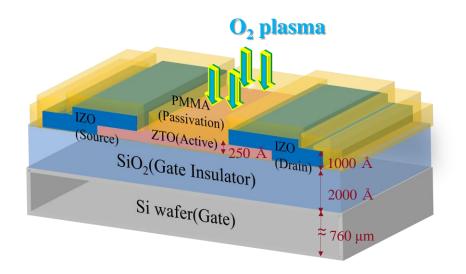
The solution-processed ZTO TFTs employing O₂ plasma treatment with inverted staggered structure were fabricated on the silicon wafer substrates as shown in Figure 5-2. Heavily boron doped p-type silicon wafer substrate and thermal oxidized silicon dioxide (SiO₂) were used as the gate and gate insulator, respectively. The cross-sectional view of ZTO active film, SiO₂ gate insulator, and Si wafer substrate is shown as Figure 5-3 by transmission electron microscopy (TEM).

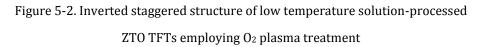
The precursor-based solution of ZTO for active layer was prepared with Zinc chloride (ZnCl₂) and Tin (II) chloride (SnCl₂) powders in acetonitrile (CH₃CN) at equal molar ratios. The ZTO film was deposited by spin-coating and isolated by the wet-etching process using diluted HF. And the ZTO films were annealed at 350 °C for 10 min by RTA process.

After the ZTO films were formed on the SiO₂, O₂ plasma treatment was performed with flow rate of 30 ml/min and plasma powers of 100 W and 300 W for 10 min on ZTO active layer by plasma asher in order to improve the characteristics of solution-processed ZTO TFT without any substrate heating.

The IZO film was deposited by dc sputtering and then defined by a lift-off process to yield source and drain electrodes. Finally, a PMMA layer was employed for passivation to protect the active layer from the ambient atmosphere.

The sequence of the fabrication process of solution-processed ZTO TFTs employing O_2 plasma treatment on Si-wafer substrate is summarized in Figure 5-4.





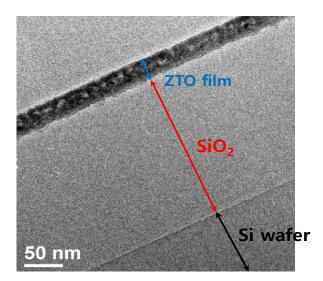


Figure 5-3. Cross-sectional view of ZTO active film, SiO_2 gate insulator, and Si wafer substrate

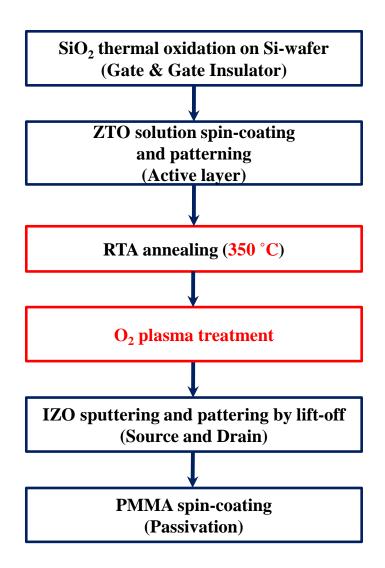


Figure 5-4. Sequence of the fabrication process of low temperature solutionprocessed ZTO TFTs employing O₂ plasma treatment

5.1.3 Electrical characteristics with O₂ plasma treatment

The drain current-gate voltage transfer characteristics of 350 °C low temperature solution-processed ZTO TFTs with a length (L) of 10 μ m and width (W) of 100 μ m in the dark at room temperature are investigated as shown in Figure 5-5 and the electrical characteristics are summarized in Table 5-1. When O₂ plasma power increases to 300 W, the on-currents was increased, while off-currents are not varied considerably. Especially the threshold voltages decreased drastically to the negative direction from 25 V to 10.74 V with the increase in O₂ plasma power. The saturation mobility of 350 °C low temperature solution-processed ZTO TFTs was increased from 0.09 cm²/V·sec to 0.58 cm²/V·sec when the O₂ plasma power was increased to 300 W. The subthreshold swing of 350 °C low temperature solution-processed ZTO TFTs was decreased from 1.65 V/dec to 1.20 V/dec when the O₂ plasma power was increased to 300 W.

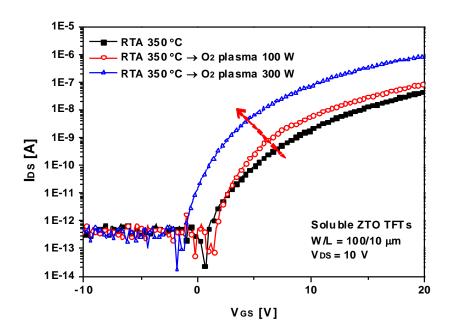


Figure 5-5. Transfer characteristics of solution-processed ZTO TFTs with an annealing temperature of 350 °C by employing O_2 plasma treatment of 100 W and 300 W with W / L = 100 / 10 μ m and V_{DS} = 10 V

Table 5-1. Electrical characteristics of solution-processed ZTO TFTs with an annealing temperature of 350 °C by employing O_2 plasma treatment of 100 W and 300 W with W / L = 100 / 10 μ m and V_{DS} = 10 V

	V _{th} [V]	I_{on}/I_{off}	µ _{sat} [cm²/V·sec]	S.S [V/decade]
No Plasma	> 25	4.5	0.09	1.65
O ₂ plasma 100 W	20.28	5	0.12	1.39
O ₂ plasma 300 W	10.74	6	0.58	1.20

5.1.4 Preferential dissociation of Cl on threshold voltage by O₂ plasma treatment

The threshold voltage of 350 °C low temperature solution-processed ZTO TFTs decreased gradually from 25 V to 10.74 V with the increase in O_2 plasma power to 300 W. It has been already reported in recent reports on sputter-processed oxide TFTs that the variation of threshold voltage has been analyzed by the change of electron concentration. The decrease in threshold voltage of solution-processed ZTO TFTs could be similarly understood as being caused by the increase in electron concentration of the ZTO active layer. Hall measurement result confirmed that when O_2 plasma power increases to 300 W, the electron concentration of ZTO films increased from 6.5 × 10¹⁶ to 4.1 × 10¹⁷, and accordingly, the threshold voltage decreased as shown in Figure 5-6.

The increase in electron concentration of ZTO active layer due to O_2 plasma could be explained by the decrease in Cl atomic concentration. O_2 plasma treatment causes preferential dissociation of weak halide-related bonding such as Cl bonding and simultaneous composition of O-related bonding of ZTO active layer by ion bombardment of energetic O_2 plasma with promoting the reaction of chemical formation as equation (5-1) as previous investigation in chapter 4 [138].

$$Zn(OH)Cl + Sn(OH)Cl \rightarrow ZnO \cdot SnO + 2HCl (\uparrow)$$
(5-1)

Figure 5-7 (a) and (b) demonstrate Auger Electron Spectroscopy (AES) results of the changes of Cl and O atomic concentration, respectively, according to O_2

plasma. In ZTO active layer region of Figure 5-7 (a) and (b), Cl atomic concentration decreased gradually from 11.1 % to 8.2 % and 0 atomic concentration rather increased from 51.7 % to 53.8 % at 100 Å depth of ZTO layers, when O_2 plasma power increased to 300 W. The decrease in Cl atoms and increase in 0 atoms cause Zn and Sn atoms would be bound to 0 atom when O_2 plasma is applied. These cause the decrease in binding energy of ZTO active layer from OH-Cl bonding to Zn-O and Sn-O bonding with the increase in O_2 plasma power. Further, when binding energy decreases, the oxygen vacancies generate electrons more easily, and consequently the electron concentration of ZTO active layer increases. In the interface region with SiO₂ gate insulator of Figure 5-7 (a) and (b), Cl and O atomic concentration were scarcely affected by O_2 plasma treatment.

 H_2 plasma treatment was also performed on ZTO active layer with a plasma power of 300 W as shown in Figure 5-7 (a) and (b). On the contrary to the effect of O_2 plasma treatment, the atomic concentration of ZTO active layer with H_2 plasma treatment were scarcely altered from that of ZTO active layer without plama treatment. Ion bombardment by plasma treatment could be occurred effectively with O_2 atoms than H_2 atoms because O_2 has a larger mocular weight than that of H_2 . Therefore, O_2 plasma treatment is suitable to improve the electrical characteristics of 350 °C low temperature solution-processed ZTO TFTs by ion bombardment.

The change of C atomic concentration according by AES is also demonstrated in Figure 5-8. C atomic concentration was maintained at a considerably small quantity of about $1 \sim 2$ % except for the abnormal peak by contamination of surface, and was scarcely altered regardless of O₂ plasma treatment. This shows that C impurities were sufficiently removed under 300 °C, so the removal of Cl would be dominant to the electrical characteristics of the ZTO active layer.

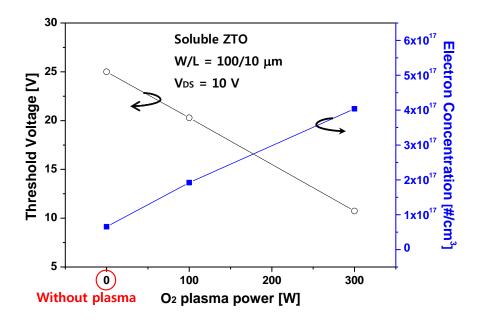
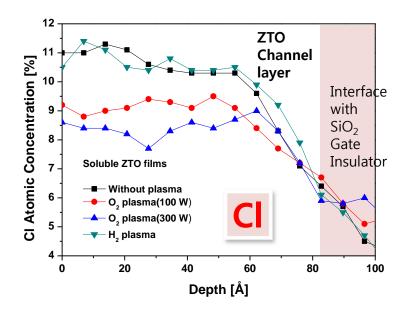
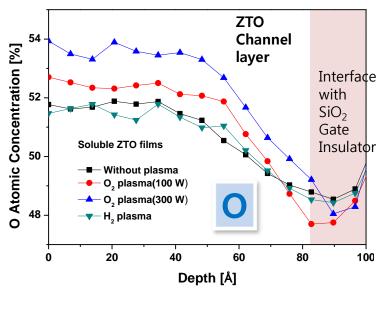


Figure 5-6. Threshold voltage and electron concentration of solution-processed ZTO TFTs with an annealing temperature of 350 °C according to O_2 plasma power





(b)

Figure 5-7. Atomic concentration of ZTO films in AES annealed at 350 °C according to O_2 plasma power for (a) Cl atoms and (b) O atoms

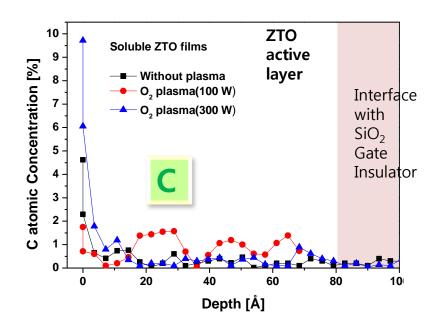


Figure 5-8. Atomic concentration of ZTO films in AES annealed at 350 $^{\circ}\text{C}$ according to O_2 plasma power for C atom

5.1.5 Increase of electron concentration on saturation mobility by O₂ plasma treatment

The saturation mobility of 350 °C low temperature solution-processed ZTO TFTs was increased from 0.09 cm²/V·sec to 0.58 cm²/V·sec when the O₂ plasma power was increased to 300 W as demonstrated in Figure 5-9 with Cl atomic concentration. The increase in saturation mobility could be caused by the crystallization and/or the dissociation of halide residues, but O₂ plasma treatment didn't cause the crystallization of ZTO active layer with amorphous phase regardless of O₂ plasma power as Figure 5-10 (a) and (b), with x-ray diffraction (XRD) results and TEM images respectively.

O₂ plasma treatment causes the preferential dissociation of halide residues such as Cl bonding of ZTO films, resulting in the increase in electron concentration [139]. The increase in electron concentration could increase the saturation mobility because the hall mobility is proportional to the carrier concentration in oxide semiconductors. Moreover, the halide residues such as Cl atoms in ZTO films are considered as trap states acting as obstacles for electron accumulation and transportation of electron in the conduction band, and consequently reducing the mobility. Therefore, the reduction of halide residues such as Cl atoms with O₂ plasma treatment, which is confirmed in AES results of Figure 5-7 above, and demonstrated again in Figure 5-9, could increase the saturation mobility of solution-processed ZTO TFTs.

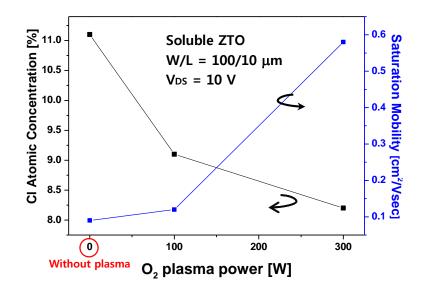
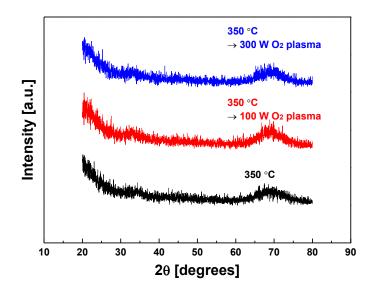
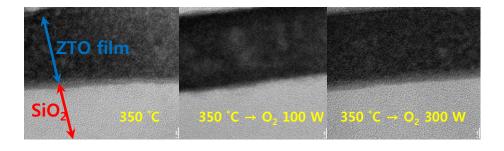


Figure 5-9. Cl atomic concentration and saturation mobility of solutionprocessed ZTO TFTs with an annealing temperature of 350 °C according to O_2 plasma power



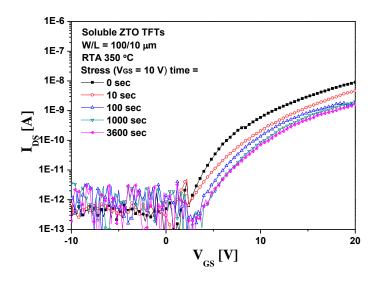


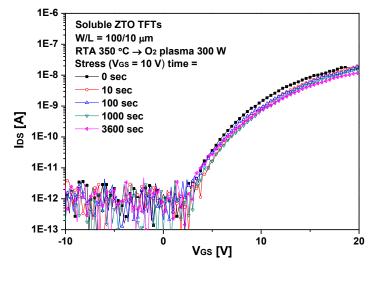
(b)

Figure 5-10. ZTO active layer with amorphous phase regardless of O₂ plasma power with (a) XRD results and (b) TEM images

5.1.6 Reliability characteristics with O₂ plasma treatment

The electrical reliability characteristics such as threshold voltage shift of 350 °C low temperature solution-processed ZTO TFTs were also investigated with the positive gate bias-stress of 10 V for 3600 sec as shown in Figure 5-11. The threshold voltage of 350 °C low temperature solution-processed ZTO TFTs was shifted positively by positive gate bias-stress with parallel almost without change of slope, regardless of O₂ plasma treatment. The threshold voltage shift for positive gate bias-stress of solution-processed ZTO TFTs without plasma treatment was 5.34 V as Figure 5-11 (a), but decreased to 3.23 V with an O₂ plasma power of 300 W as Figure 5-11 (b). Therefore, the improvement in reliability could be observed by O₂ plasma treatment as demonstrated in Figure 5-12. It is another supporting data that O₂ plasma treatment reduces the halide residues such as Cl acting as trap states.





(b)

Figure 5-11. Reliability characteristics of solution-processed ZTO TFTs with the positive gate bias-stress of 10 V for 3600 sec as transfer curve (a) without O_2 plasma treatment, (b) employing O_2 plasma treatment of 300 W

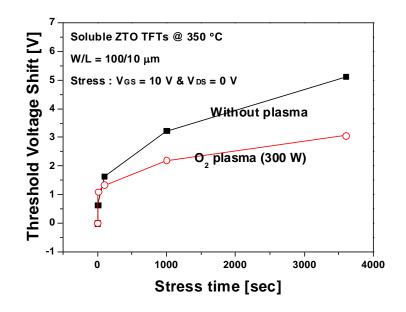


Figure 5-12. Threshold voltage shift without O_2 plasma treatment and with O_2 plasma treatment of 300 W

5.1.7 Conclusion

In conclusion, the low temperature solution-processed ZTO TFTs with an annealing temperature of 350 °C on ZTO active layer, which is considerably lower than widely used 500 °C were fabricated employing O_2 plasma treatment on ZTO active layer to improve the electrical characteristics of solution-processed ZTO TFTs.

 O_2 plasma treatment causes preferential dissociation of weak halide-related bonding such as Cl bonding by ion bombardment. After O_2 plasma treatment, the threshold voltage decreased from 25 V to 10.74 V with an O_2 plasma power of 300 W because of the increase in electron concentration from 6.5×10^{16} to 4.1×10^{17} due to the reduction of Cl bonding and simultaneous composition of Orelated bonding by ion bombardment. Moreover, the saturation mobility was increased from 0.09 cm²/V·sec to 0.58 cm²/V·sec with an O_2 plasma power of 300 W because of the increase in electron concentration and reduction of halide residues such as Cl atoms as trap states.

The electrical reliability characteristic such as threshold voltage shift of 350 °C low temperature solution-processed ZTO TFTs for positive gate bias-stress was improved from 5.34 V to 3.23 V with an O_2 plasma power of 300 W because O_2 plasma reduced the halide residues such as Cl acting as trap states.

Therefore, the electrical characteristics of 350 °C low temperature solutionprocessed ZTO TFTs to decrease threshold voltage and enhance mobility and reliability were successfully improved by employing O2 plasma treatment, and this proposed treatment are suitable for the low cost, stable, and flexible display backplane.

5.2 Improvement of low temperature solutionprocessed oxide TFTs employing Ultra-Violet radiation treatment

5.2.1 Motivation

For a flexible display, the solution-processed oxide TFTs need to be fabricated on cheap and flexible substrates such as glass and plastic. These substrates are easily damaged at high annealing temperatures, so low temperature processes are essential for solution-processed oxide TFTs fabrication. Therefore, the annealing temperature should be decreased less than 350 °C in solution-processed oxide TFTs for flexible substrates such as plastic. However, a high annealing temperature on an active layer exceeding 500 °C is required in order to obtain high device performance such as low threshold voltage and high mobility in solution-processed oxide TFTs. Annealing temperature should be decreased, but low conductivity and low mobility of low temperature Solution-processed oxide TFTs would be the issues.

Figure 5-13 shows the previous paper that ultra-violet (UV) radiation measurement in sputtered oxide TFTs [140]. UV light is electromagnetic radiation with a wavelength shorter than that of visible light, but longer than X-rays, that is, in the range between 400 nm and 10 nm, corresponding to photon energies from 3 eV to 124 eV. UV exposure could give rise to the generation of electron-hole pair and consequently result in the increase of conductivity of ZnO films. These UV treatment effect could be applied to improve the electrical characteristics of low temperature solution-processed oxide TFTs by increasing the conductivity of oxide semiconductor films.

In this section, the electrical characteristics of solution-processed oxide TFTs could be considerably improved by employing UV radiation treatment on the active layer of oxide TFTs. UV treatment increased electron concentration of ZTO and IGZO active layer because electrons were generated with increasing -OH bonding by UV in oxide semiconductors. The threshold voltage decreased and mobility increased by UV treatment due to the increase of electron concentration at low annealing temperature of 350 °C in solution-processed oxide TFTs. The proposed UV treatment could decrease annealing temperature, so that may be suitable for flexible substrates.

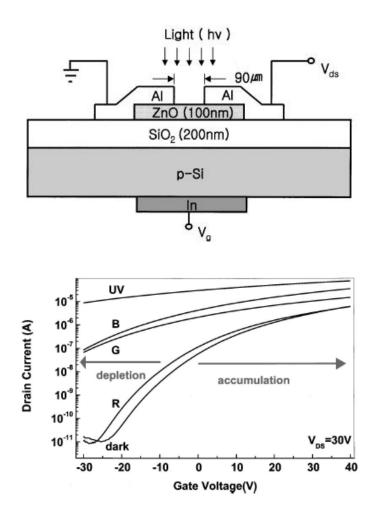


Figure 5-13. UV exposure measurement on sputtered oxide TFTs in previous

work

5.2.2 Fabrication of solution-processed ZTO TFTs employing UV radiation treatment

The solution-processed ZTO and IGZO TFTs with annealing temperature of 350 °C on active layer were fabricated. ZTO and IGZO TFTs with inverted staggered structure were fabricated on glass substrates as Figure 5-14. Sputtered Mo layer was used as the gate and gate insulator was deposited with widely used 300 nm thick silicon dioxide (SiO₂) using plasma-enhanced chemical vapor deposition (PECVD).

The precursor-based solution of ZTO for active layer was prepared by dissolving 0.07 M of Tin (II) chloride (SnCl₂, FW of 189.6, Aldrich) and 0.07 M of Zinc chloride (ZnCl₂, FW of 136.3, Aldrich) powders in Acetonitrile (CH₃CN) of 3mL. The mixed ZTO solution was stirred at room temperature for 15 min to promote the dissolving process. The precursor-based solution of IGZO for active layer was prepared by dissolving 0.085 M of In nitrate hydrate (In(NO₃)₃·xH₂O, FW of 390.91, Aldrich), 0.0125 M of Ga nitrate hydrate (Ga(NO₃)₃·xH₂O, FW of 255.74, Aldrich) and 0.0275 M of Zn acetate dihydrate (Zn(C₂H₃O₂)₂·2H₂O, FW of 219.5, Aldrich) powders in 2-methoxyethanol (C₃H₈O₂) of 3mL. The mixed IGZO solution was stirred at 75 °C for 2 h to promote the dissolving process.

After spin-coating, ZTO and IGZO active layers were annealed at 350 °C for 10 min by RTA process and cooled down to the room temperature. The thicknesses of ZTO and IGZO films decreased from 400 Å to 250 Å during annealing due to the solvent and halide residue were evaporated.

UV was radiated by employing low pressure mercury lamp with wavelength of 184.9 nm and 253.7 nm without any substrate heating. UV treatment was varied with time in order to investigate the effects of UV on the electrical characteristics

of solution-processed oxide TFT.

Finally, 300 nm thick indium tin oxide (ITO) film as source and drain electrodes was deposited by dc sputtering with shadow mask.

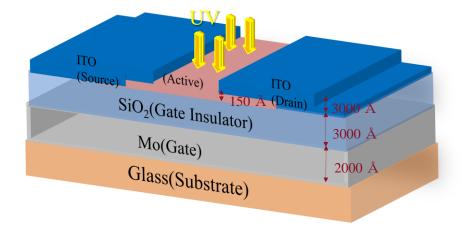


Figure 5-14. Inverted staggered structure of low temperature solution-processed oxide TFTs employing UV radiation treatment

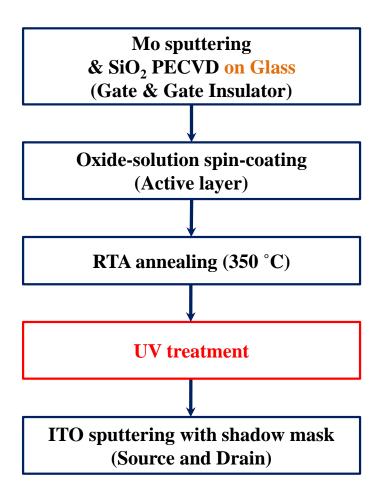


Figure 5-15. Sequence of the fabrication process of low temperature solutionprocessed oxide TFTs employing UV radiation treatment

5.2.3 Electrical characteristics with UV radiation treatment

The transfer characteristics of solution-processed ZTO and IGZO TFTs with an annealing temperature of 350 °C employing UV radiation treatment were investigated.

The transfer characteristics and electrical characteristics of solution-processed ZTO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \mu m$ and V_{DS} = 10 V are demonstrated in Figure 5-16 and Table 5-2, respectively. The on/off current ratio of solution-processed ZTO TFTs was increased and threshold voltage decreased from 25 V (without UV treatment) to 12.32 V (with 1 h UV treatment) with UV treatment. Saturation mobility of solution-processed ZTO TFTs increased from $0.01 \text{ cm}^2/\text{V}\cdot\text{sec}$ (without UV treatment) to $0.30 \text{ cm}^2/\text{V}\cdot\text{sec}$ (with 1 h UV treatment) h UV treatment) with UV treatment.

The transfer characteristics and electrical characteristics of solution-processed IGZO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \mu$ m and V_{DS} = 10 V are demonstrated in Figure 5-17 and Table 5-3, respectively. The on/off current ratio of solution-processed IGZO TFTs was increased and threshold voltage decreased from 1.02 V (without UV treatment) to -5.09 V (with 1 h UV treatment) with UV treatment. Saturation mobility of solution-processed IGZO TFTs increased from $0.31 \text{ cm}^2/\text{V}\cdot\text{sec}$ (without UV treatment) to $2.96 \text{ cm}^2/\text{V}\cdot\text{sec}$ (with 1 h UV treatment) h UV treatment) with UV treatment.

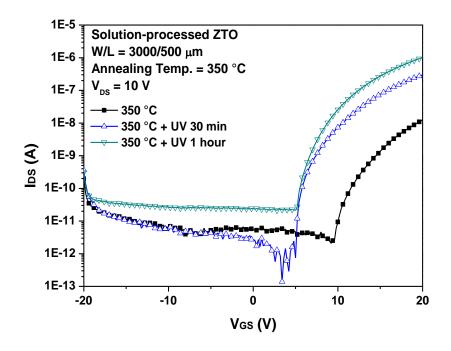


Figure 5-16. Transfer characteristics of solution-processed ZTO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \ \mu m$ and V_{DS} = $10 \ V$

Table 5-2. Electrical characteristics of solution-processed ZTO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \mu m$ and $V_{DS} = 10 V$

	I_{on}/I_{off} [10 ^x]	V _{th} [V]	µ _{sat} [cm²/V⋅sec]
Without UV	3	> 25	0.01
UV 30 min	4	15.80	0.09
UV 1 hour	5	12.32	0.30

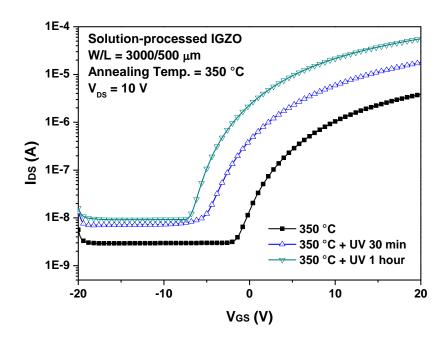


Figure 5-17. Transfer characteristics of solution-processed IGZO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \ \mu m$ and $V_{DS} = 10 \ V$

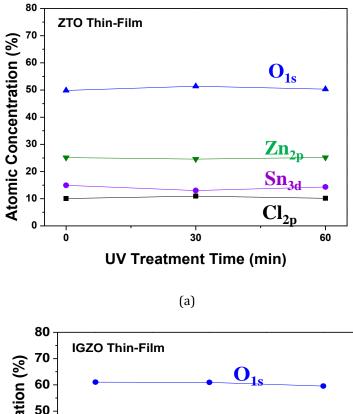
Table 5-3. Electrical characteristics of solution-processed IGZO TFTs with an annealing temperature of 350 °C employing UV radiation treatment for 30 min and 1 hour with W / L = $3000 / 500 \ \mu m$ and V_{DS} = $10 \ V$

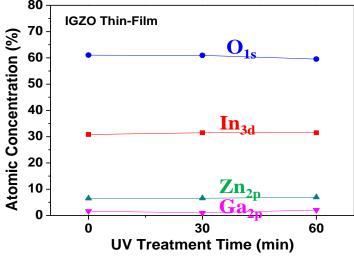
	I _{on} /I _{off} [10 ^x]	V _{th} [V]	µ _{sat} [cm²/V·sec]
Without UV	3	1.02	0.31
UV 30 min	3.5	- 2.45	1.03
UV 1 hour	4	- 5.09	2.96

5.2.4 Effects of UV radiation treatment on oxide active layer semiconductors

The X-ray photoelectron spectroscopy (XPS) was employed to observe the effects of UV radiation treatment on the quantification such as atomic concentrations and chemical state information such as bonding status of solution-processed oxide semiconductors.

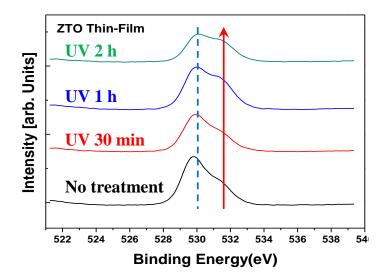
The XPS results in Figure 5-18 demonstrated that atomic concentrations of ZTO active layer and IGZO active layer were not considerably varied regardless of UV radiation treatment time. On the other hand, XPS spectra of O 1s core level in Figure 5-19 showed that -OH bonding was increased with the increase in UV treatment time in both of solution-processed ZTO and IGZO active layers. In Figure 5-19, the dashed line represents O^{2-} ions surrounded by metal atoms in Zn-O bonding (529.8 eV ± 0.2), and the solid line represents -OH bonding (531.6 eV ± 0.2). The proportion of hydroxide in total oxygen was increased in both of solution-processed ZTO and IGZO active 5-20 and Table 5-4.



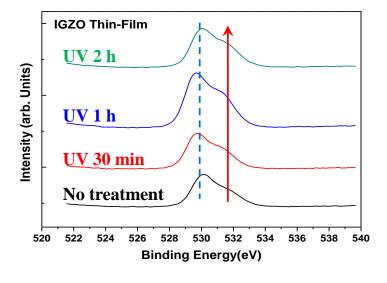


(b)

Figure 5-18. Atomic concentration of solution-processed (a) ZTO and (b) IGZO active layers with UV radiation treatment by XPS



(a)



(b)

Figure 5-19. XPS spectra of O 1s core level of solution-processed (a) ZTO and (b) IGZO active layers with UV radiation treatment

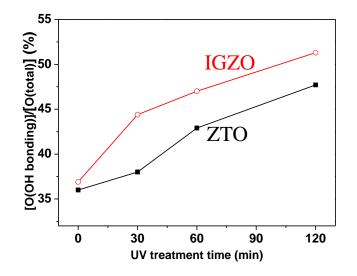


Figure 5-20. [O(hydroxide)] / [O(total)] of (a) ZTO and (b) IGZO active layers with UV radiation treatment

Table 5-4. [O(hydroxide)] / [O(total)] of (a) ZTO and (b) IGZO active layers with UV radiation treatment

The proportion of OH bonding				
	ZTO	IGZO		
350 °C	36 %	36.9 %		
350 °C + UV 2 hour	47.7 %	51.3 %		

5.2.5 Generation of hydroxide(-OH) bonding by UV radiation treatment on oxide active layer semiconductors

The proportion of hydroxide (-OH) in total oxygen was increased with the increase in UV radiation treatment time in both of solution-processed ZTO and IGZO active layers as shown in Figure 5-20.

When short wavelength of UV was exposed on or ZTO or IGZO active layers, the conduction band electrons and valence band holes were generated at oxide semiconductors like following equation (5-2).

$$ZTO \text{ or } IGZO + hv \rightarrow e^- + h^+$$
(5-2)

And the generated holes accelerate the bonding of moisture-sensitive ZTO or IGZO with H₂O from the air by the strong oxidizing power of holes, like following equation (5-3). Then, the hydroxide(-OH) bonding in oxide semiconductors are formed with preventing the recombination of the electron and the hole, so that finally the electrons would be increased.

$$h^{+} + H_2 O \rightarrow -OH + H^{+}$$
 (5-3)

This chemical mechanism of generation of hydroxide(-OH) bonding by UV radiation treatment on oxide active layer semiconductors is demonstrated as a schematic diagram in Figure 5-21 and this a similar mechanism with a photocatalytic process of UV on ZnO or TiO₂.

The threshold voltage of solution-processed ZTO and IGZO TFTs decreased with the increase in UV treatment time as shown in Figure 5-16 and Figure 5-17 because the electron concentration of ZTO and IGZO active layers increased. In recent reports of sputter-processed oxide TFTs, the variation of threshold voltage has been analyzed by the change of electron concentration. The decrease in threshold voltage in solution-processed oxide TFTs can be understood similarly with the increase in electron concentration of the ZTO and IGZO active layers. UV radiation treatment increased the electron concentration of ZTO and IGZO active layers because the electrons were generated with increasing -OH bonding by UV radiation in oxide semiconductors, so that the threshold voltage decreased. Moreover, there was a report that the hall mobility is proportional to the carrier concentration in oxide semiconductors by Hosono.

The increase of electron concentration of solution-processed ZTO and IGZO active layers according to UV radiation treatment could be confirmed by hall measurement method. When UV treatment time increased to 2 hour, the electron concentration of ZTO and IGZO active layer increased as shown in Figure 5-22 and Table 5-5.

Therefore, the threshold voltage decreased and the saturation mobility increased by UV radiation treatment due to the increase of electron concentration at low annealing temperature of 350 °C in solution-processed oxide TFTs.

138

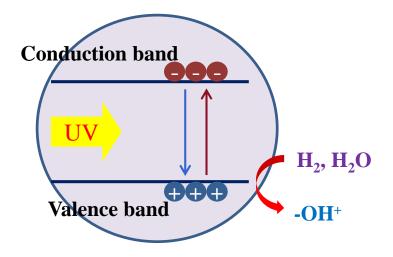


Figure 5-21. Schematic diagram of generation of hydroxide (-OH) bonding by UV radiation treatment on oxide active layer semiconductors

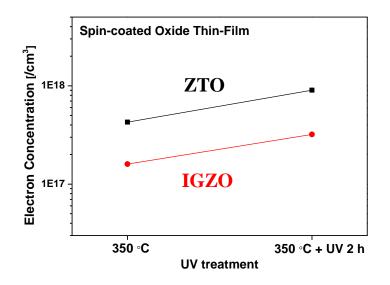


Figure 5-22. Electron concentration of solution-processed ZTO and IGZO active layers according to UV radiation treatment by Hall measurement

Table 5-5. Electron concentration of solution-processed ZTO and IGZO active
layers according to UV radiation treatment by Hall measurement

	ZTO	IGZO
350 °C	4.27E17	1.6E17
350 °C +	9.01E17	3.2E17
UV 2 hour		

5.2.6 Conclusion

In conclusion, the solution-processed ZTO and IGZO TFTs were fabricated with an annealing temperature of 350 °C employing UV radiation treatment. The electrical characteristics of solution-processed oxide TFTs would be considerably improved by employing UV radiation treatment on the active layer of oxide TFTs. UV treatment increased electron concentration of ZTO and IGZO active layer because electrons were generated with increasing -OH bonding by UV in oxide semiconductors. The threshold voltage decreased and the saturation mobility increased by UV treatment due to the increase of electron concentration at low annealing temperature of 350 °C in solution-processed oxide TFTs.

Threshold voltage of solution-processed ZTO TFTs decreased from 25 V (without UV treatment) to 12.32 V (with 1 h UV treatment) with UV treatment. Saturation mobility of solution-processed ZTO TFTs increased from 0.01 cm²/V·sec (without UV treatment) to 0.30 cm²/V·sec (with 1 h UV treatment) with UV treatment. Threshold voltage of solution-processed IGZO TFTs decreased from 1.02 V (without UV treatment) to -5.09 V (with 1 h UV treatment) with UV treatment. Saturation mobility of solution-processed IGZO TFTs increased from 0.31 cm²/V·sec (without UV treatment) to 2.96 cm²/V·sec (with 1 h UV treatment) with UV treatment.

These experiment results showed that the low annealing temperature solutionprocessed oxide TFTs employing UV treatment may be suitable for flexible display backplane such as glass or plastic substrate which is easily damaged at high annealing temperatures.

5.3 Improvement of low temperature solutionprocessed oxide TFTs employing biaed-H₂O annealing

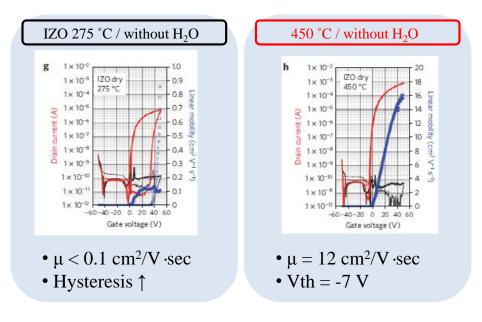
5.3.1 Motivation

In regard of the established chemical formation equations of ZTO active layer accordint to the annealing temperature in chapter 4, the removal of residues of the low temperature solution-processed oxide TFTs is the a dominant factor to achieve high device characteristics even at low annealing temperature [141, 142]. Furthermore, the residues from precursors such as halide residues as Cl could be evaporated by combining with H_2O in the ambient atmosphere.

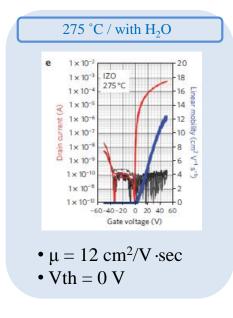
Therefore, the provide of H_2O in the annealing process would be the most effective method to improve the electrical characteristics of low temperature solution-processed oxide TFTs. There were some previous research in regard of the improvement of solution-processed oxide TFTs employing H_2O wet annealing as shown in Figure 5-23, but the effects of H_2O wet annealing according to the annealing temperature were scarcely investigated [143].

In this section, the effects of various annealing condition were investigated to verify the role of H_2O in the ambient atmosphere at the annealing process. Moreover, the low temperature solution-processed oxide TFTs were fabricated employing H_2O wet annealing to provide H_2O at the annealing process, so that the electrical characteristics of low temperature solution-processed oxide TFTs were considerably improved by employing H_2O wet annealing and the effects of H_2O wet annealing according to the annealing temperature were investigated [144]. Furthermore, the biased- H_2O annealing was proposed to promote the

composition of H_2O with the oxide active layer semiconductors at the annealing process of low temperature solution-processed oxide TFTs.



(a)



(b)

Figure 5-23. Improvement of solution-processed oxide TFTs employing H_2O wet

annealing

5.3.2 Effects of various annealing condition

The solution-processed ZTO TFTs with various annealing condition with inverted staggered structure were fabricated on the silicon wafer substrates. Heavily boron doped p-type silicon wafer substrate and thermal oxidized silicon dioxide (SiO₂) were used as the gate and gate insulator, respectively.

The precursor-based solution of ZTO for active layer was prepared with Zinc chloride (ZnCl₂) and Tin (II) chloride (SnCl₂) powders in acetonitrile (CH₃CN) at equal molar ratios of 0.07 M. The ZTO film was deposited by spin-coating and isolated by the wet-etching process using diluted HF.

The ZTO active layers were annealed at 300 °C under ambient condition and at 350 °C under N_2 , O_2 , and ambient condition for 10 min by RTA process.

The IZO film was deposited by dc sputtering and then defined by a lift-off process to yield source and drain electrodes. Finally, a PMMA layer was employed for passivation to protect the active layer from the ambient atmosphere.

The transfer characteristics and electrical characteristics of solution-processed ZTO TFTs with various annealing condition were demonstrated in Figure 5-24 and Table 5-6, respectively. The electrical characteristic at 350 °C under ambient condition was improved from that of 300 °C under ambient condition by the effects of annealing temperautre. However, the electrical characteristic at 350 °C under N_2 condition was degraded and more degraded at 350 °C under N_2 condition.

Under O_2 annealing condition, the composition from the precursors of ZnCl₂ and SnCl₂ to the metal-oxide bonding of ZnO·SnO occurs in a difficult way because the bonding energy of O_2 is stronger than that of H₂O. Furthermore, the composition from the precursors of ZnCl₂ and SnCl₂ to the metal-oxide bonding

of ZnO SnO is scarcely occurred under $N_{\rm 2}$ annealing condition, so that the electrical characteristic would be degraded.

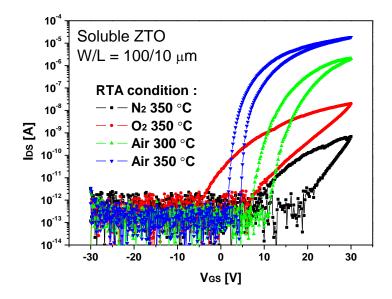


Figure 5-24. Transfer characteristics of solution-processed ZTO TFTs with various annealing condition with W / L = 100 / 10 μm and V_{DS} = 10 V

Table 5-6. Electrical characteristics of solution-processed ZTO TFTs with various annealing condition with W / L = 100 / 10 μm and V_{DS} = 10 V

$(*V_{DS}=10\ V)$	Vth (V)	Ion/Ioff	Hysteresis (V)	μ_{sat}	S.S.
N ₂ 350 °C	-	10 ³	-	0.01	3.14
O ₂ 350 °C	-	104	-	0.1	3.25
Air 300 °C	16.89	106	4.07	0.18	1.35
Air 350 °C	6.55	107	2.94	0.56	1.02

5.3.3 Effects of H₂O wet annealing according to the annealing temperature

The solution-processed ZTO TFTs were fabricated with 350 °C of annealing temperature on ZTO active layer which is quite lower temperature than required temperature of 500 °C to make the characteristics of TFT be sufficient for industrial devices. ZTO TFTs with inverted staggered structure were fabricated on wafer substrates as Figure 5-25. About 760 μ m heavily boron doped p-type silicon wafer substrate was used as the gate and gate insulator was fabricated with Silicon dioxide (SiO₂) of 2000 Å using thermal oxidation.

The precursor-based solution of ZTO for active layer was prepared by dissolving 0.07 M of Tin (II) chloride (SnCl₂, fomular weight (FW) of 189.6, Aldrich) and 0.07 M of Zinc chloride (ZnCl₂, FW of 136.3, Aldrich) powders in Acetonitrile (CH₃CN) of 3mL at equal molar ratio. The mixed solution was stirred at room temperature for 15 min to promote the dissolving process.

The ZTO active layer thicknesses were about 400 Å from the spin-coating process with 500 rpm for 5 sec and 4000 rpm for 30 sec and soft annealing of 200 °C for 10 min to solidify ZTO film was followed immediately.

After spin-coating, ZTO active layers were annealed at 350 °C for 10 min by RTA process under H_2O wet annealing condition with various flow rate of 5 slm, 10 slm, and 15 slm and cooled down to room temperature. The final thicknesses of ZTO active layers all became about 250 Å by evaporation process during annealing.

Indium tin oxide (ITO) film was deposited by dc sputtering with 1000 Å with shadow mask to yield source and drain electrodes. Finally, a PMMA layer was employed for the passivation to protect active layer from the ambient atmosphere.

Transfer characteristics of solution-processed ZTO TFTs according to H_2O flow rate are shown in Figure 5-26. The electrical characteristics such as on/off current ratio (Ion/Ioff), threshold voltage (Vth), saturation mobility, hysteresis, and subthreshold swing (S.S) of solution-processed ZTO TFT were improved with the increase of H_2O flow rate to 10 slm as shown in Table 5-7 and Figure 5-27. On the other hand, the solution-processed ZTO TFTs with H_2O 15 slm showed poor performance with high off-current characteristics, large subthreshold swing, and even low on-current.

The effects of H_2O flow rate could be explained with the role of H_2O when the annealing temperature increased. The chemical formation equations could be established according to the increase of annealing temperature to 350 °C with regard to H_2O employing as investigated in chapter 4.

The evaporation of residual solvent and hydroxylation of metal chloride compounds occur with H₂O coming from ambient atmosphere below 200 °C, as expressed by equation (4-1). In this region, ZnCl₂ and SnCl₂ were transformed to Zn(OH)Cl and Sn(OH)Cl so that H₂O is needed to reduce Cl atomic concentration according to the increase of annealing temperature. Therefore, the electrical characteristics of solution-processed ZTO TFTs were improved with the increase of H₂O flow rate to 10 slm because H₂O would promote the deformation of Zn-Cl and Sn-Cl bonding of ZTO active layer [145].

The dehydroxylated Sn(OH)Cl and Zn(OH)Cl would form the alloy of ZnO·SnO (ZTO) until 350 °C, as expressed by equation (4-2). In this region, Zn(OH)Cl and Sn(OH)Cl were transformed to ZnO·SnO so that H_2O is evaporated according to the increase of annealing temperature. The chemical bonding of ZTO active layer from OH-Cl bonding to Zn-O and Sn-O bonding with the increase in annealing

temperature result in the increase in electron concentration. The increase in electron concentration could increase the saturation mobility because the hall mobility is proportional to the carrier concentration in oxide semiconductors. The electrical characteristics of solution-processed ZTO TFTs were degraded with H₂O flow rate of 15 slm because the excessive H₂O would disturb the change of bonding of ZTO active layer from Zn(OH)Cl and Sn(OH)Cl to ZnO·SnO with H₂O evaporation in this region.

Therefore, H_2O would be essential below 200 °C while should be removed above 200 °C to promote the composition of ZnO·SnO in solution-processed ZTO TFTs with regard to the investigation of effects of H_2O wet annealing according to the annealing temperature.

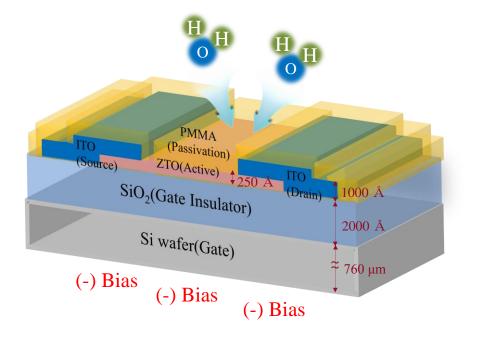


Figure 5-25. Inverted staggered structure of low temperature solution-processed oxide TFTs employing H_2O wet annealing

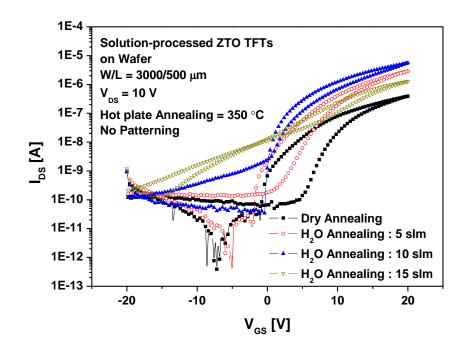


Figure 5-26. Transfer characteristic of solution-processed ZTO TFTs with 350 °C of H_2O wet annealing temperature according to H_2O flow rate

Annealing Condition	I_{on}/I_{off}	$Vth (* V_{DS} = 10 V) [V]$	μ _{sat} [cm²/Vsec]	Hysteresis [V]	S.S [V/dec]
Dry	5×10^{3}	11.05	0.42	4.64	2.94
$H_2O: 5 slm$	104	4.91	0.81	3.52	1.58
H ₂ O : 10 slm	10 ⁵	2.87	1.51	0.84	1.12
H ₂ O : 15 slm	-	-	-	-	-

Table 5-7. Electrical characteristics of solution-processed ZTO TFTs with 350 $^{\circ}$ C of annealing temperature according to H₂O flow rate

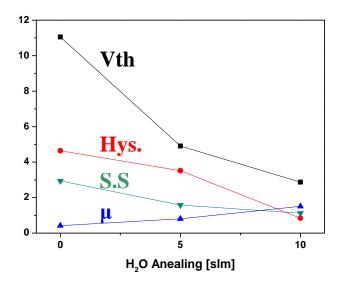


Figure 5-27. Electrical characteristics of solution-processed ZTO TFTs with $350\ ^\circ C$ of annealing temperature according to H_2O flow rate

5.3.4 Proposed biased-H₂O annealing to improve low temperature solution-processed oxide TFTs

 H_2O would be essential below 200 °C while should be removed above 200 °C to promote the composition of ZnO·SnO in solution-processed ZTO TFTs with regard to the investigation of effects of H_2O wet annealing according to the annealing temperature. To promote the composition of H_2O with the oxide active layer semiconductors at the annealing process, the negative-bias stress could be employed with H_2O wet annealing on the fabrication of low temperature solution-processed oxide TFTs because H_2O has slightly positive polarity.

The solution-processed ZTO TFTs with various H_2O annealing condition on active layer with inverted staggered structure were fabricated on the silicon wafer substrates as Figure 5-28. The various H_2O annealing condition were demonstrated in a schematic diagram with regard to the annealing temperature as Figure 5-29, with 500 °C and 300 °C dry (ambient) annealing temperature as the reference samples, 300 °C H_2O (15 slm) wet annealing, 300 °C partial H_2O (15 slm) wet annealing (only H_2O wet annealing below 200 °C), and biased- H_2O annealing. The biased- H_2O annealing condition was performed below 90 °C and could be divided with humidity (50, 70, and 90 %) and negative-bias (-10, -20 V).

The transfer characteristics and electrical characteristics of solution-processed ZTO TFTs with various H_2O wet annealing condition including biased- H_2O annealing are demonstrated in Figure 5-30 and Table 5-8, respectively. The 300 °C dry (ambient) annealing device showed poor electrical characteristic due to the residues by low annealing temperature. The 300 °C H_2O (15 slm) wet annealing device showed better electrical characteristic than that of 300 °C dry (ambient) annealing device due to the promotion of H_2O from ZnCl₂ and SnCl₂ to Zn(OH)Cl and Sn(OH)Cl, but showed high off-current due to the metastable

intermediates as Zn(OH)Cl and Sn(OH)Cl which could not be decomposed above 200 °C because of the provide of H₂O. The 300 °C partial H₂O (15 slm) wet annealing (only H₂O wet annealing below 200 °C) device showed better electrical characteristic than that of 300 °C H₂O (15 slm) wet annealing device due to the decomposition of metastable intermediates above 200 °C, but showed still high off-current due to the residues of metastable intermediates.

The biased-H₂O annealing device with -10 V and 50 % showed better electrical characteristic than that of 300 °C partial H₂O (15 slm) wet annealing device due to the promotion of composition of H₂O with the oxide active layer semiconductors by the negative-bias stress below 90 °C, but showed quite high off-current due to the adsorption of H₂O at the back channel of ZTO active layer as demonstrated in Figure 5-31 (a). The biased-H₂O annealing device with -20 V and 50 % showed better electrical characteristic than that of biased-H₂O annealing device with -10 V and 50 % device due to the adsorption of H₂O into the front channel of ZTO active layer by high negative-bias stress as demonstrated in Figure 5-31 (b). The biased-H₂O annealing device with humidity of 70 or 90 % showed high conductivity characteristic due to the excessive H₂O causing high electron concentration on the ZTO active layer.

Therefore, the proposed The biased-H₂O annealing device with -20 V and 50 % showed high performance solution-processed ZTO TFTs as saturation mobility of $2.19 \text{ cm}^2/\text{V}$ -sec, compared with the 500 °C dry (ambient) annealing device.

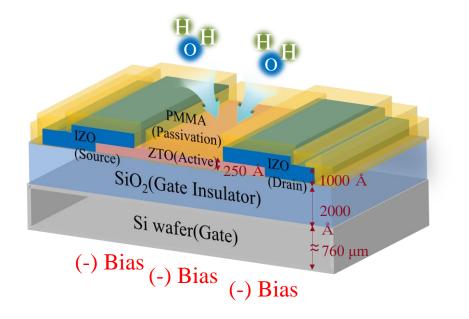


Figure 5-28. Inverted staggered structure of low temperature solution-processed oxide TFTs employing biased-H $_2$ O annealing

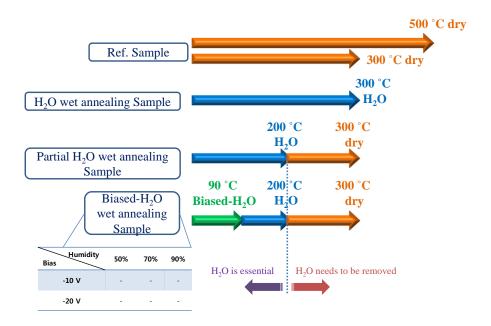


Figure 5-29. Schematic diagram of various $H_2 O$ annealing condition with regard to the annealing temperature

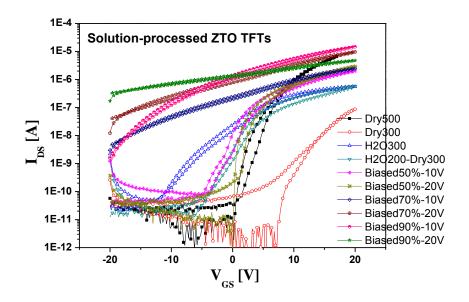
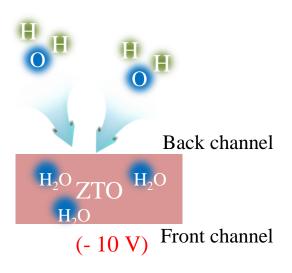


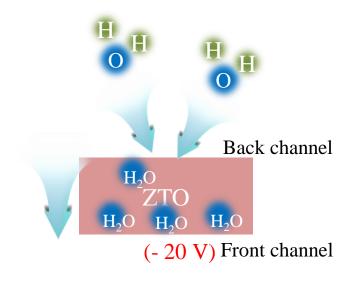
Figure 5-30. Transfer characteristic of solution-processed ZTO TFTs with various H_2O wet annealing condition including biased- H_2O annealing

Annealing Condition	I_{on}/I_{off}	$Vth (* V_{DS} = 10 V)$ [V]	μ _{sat} [cm²/Vsec]
Dry 500 °C	8 × 10 ⁵	5.80	2.45
Dry 300 °C	1 × 10 ⁴	~ 20	0.2
H ₂ O 300 °C	7 × 10 ⁴	4.51	1.03
H ₂ O 200 °C → Dry 300 °C	7 × 10 ⁴	6.22	1.04
Biased-H ₂ O (50% / -10V)	3 × 10 ⁴	3.29	2.12
Biased-H ₂ O (50% / -20V)	4×10^5	3.49	2.19

Table 5-8. Electrical characteristic of solution-processed ZTO TFTs with various H_2O wet annealing condition including biased- H_2O annealing



(a)



(b)

Figure 5-31. Schematic diagram of the adsorption of H_2O on ZTO active layer by the biased- H_2O annealing with (a) -10 V and (b) -20 V

5.3.5 Conclusion

In conclusion, the low temperature solution-processed ZTO TFTs with an annealing temperature of 300 °C on ZTO active layer, which is considerably lower than widely used 500 °C were fabricated employing biased-H₂O annealing on ZTO active layer to improve the electrical characteristics of solution-processed ZTO TFTs.

The biased-H₂O annealing with -20 V and 50 % causes the promotion of adsorption of H₂O into the front channel of ZTO active layer by high negativebias stress, the composition from $ZnCl_2$ and $SnCl_2$ to Zn(OH)Cl and Sn(OH)Cl below 200 °C, and the decomposition of metastable intermediates above 200 °C.

Therefore, the electrical characteristics of 300 °C low temperature solutionprocessed ZTO TFTs were successfully improved by employing proposed biased- H_2O annealing, and this proposed method are suitable for the low cost, stable, and flexible display backplane.

Chapter 6 Summary

In this thesis, oxide TFTs employing solution-process for an oxide semiconductor active layer were fabricated with various annealing temperatures to investigate the effects of annealing temperature on the electrical characteristics of solution-processed oxide TFTs such as threshold voltage, saturation mobility, and reliability. The electrical characteristics of ZTO TFTs were improved with the increase in annealing temperature owing to the increase in electron concentration in the active layer because the oxygen vacancies generate electrons more easily as the binding energy of ZTO active layer decreased with the removal of Cl, moreover the decomposition of halide residues such as Cl and nano-crystallization causing the reduction of trap states. The chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature is demonstrated in Figure 6-1.

According to the investigation of effects of annealing temperature on the

162

electrical characteristics of solution-processed oxide TFTs, the electrical characteristics of low temperature solution-processed oxide TFTs were improved to achieve high device characteristics of solution-processed oxide TFTs even at low annealing temperature by various proposed methods because solution-processed oxide TFTs need to be fabricated on inexpensive and flexible substrates such as glass and plastic which are easily damaged at high annealing temperatures for additional cost reduction and application extension to a flexible display.

Firstly, O_2 plasma treatment was employed to improve the electrical characteristics of low temperature solution-processed ZTO TFTs with an annealing temperature of 350 °C, which is considerably lower than widely used 500 °C. O_2 plasma treatment causes preferential dissociation of weak halide-related bonding such as Cl bonding by ion bombardment. The chemical diagram of accelerated metal-oxide formation from precursors with the increase in annealing temperature employing O_2 plasma treatment is demonstrated in Figure 6-2. After O_2 plasma treatment, the threshold voltage decreased because of the increase in electron concentration due to the reduction of Cl bonding and simultaneous composition of O-related bonding by ion bombardment. Moreover, the saturation mobility was increased because of the increase in electron concentration and reduction of halide residues such as Cl atoms as trap states. The electrical reliability characteristic such as threshold voltage shift was improved because O_2 plasma reduced the halide residues such as Cl acting as trap states.

Secondly, UV radiation treatment was employed to improve the electrical characteristics of low temperature solution-processed ZTO and IGZO TFTs with an annealing temperature of 350 °C. UV treatment increased electron concentration of ZTO and IGZO active layer because electrons were generated

with increasing -OH bonding by UV in oxide semiconductors. The chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing UV radiation is demonstrated in Figure 6-3. The threshold voltage decreased and the saturation mobility increased by UV treatment due to the increase of electron concentration at low annealing temperature of 350 °C in solution-processed oxide TFTs.

Thirdly, the biased-H₂O annealing was employed to improve the electrical characteristics of low temperature solution-processed ZTO TFTs with an annealing temperature of 300 °C. The biased-H₂O annealing with -20 V and 50 % causes the promotion of adsorption of H₂O into the front channel of ZTO active layer by high negative-bias stress, the composition from ZnCl₂ and SnCl₂ to Zn(OH)Cl and Sn(OH)Cl below 200 °C, and the decomposition of metastable intermediates above 200 °C. The chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing biased-H₂O annealing is demonstrated in Figure 6-4.

Therefore, the electrical characteristics of low temperature solution-processed oxide TFTs were successfully improved by various proposed methods as the diagram shown in Figure 6-5. And the improved electrical characteristics of solution-processed ZTO TFTs with various annealing condition were summarized in Table 6-1. These proposed methods to improve the electrical characteristics of low temperature solution-processed oxide TFTs would be suitable for the low cost, stable, and flexible active matrix display backplane.

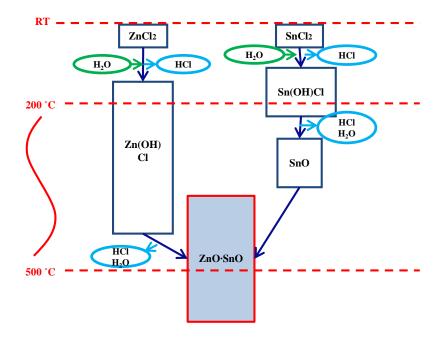


Figure 6-1. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature

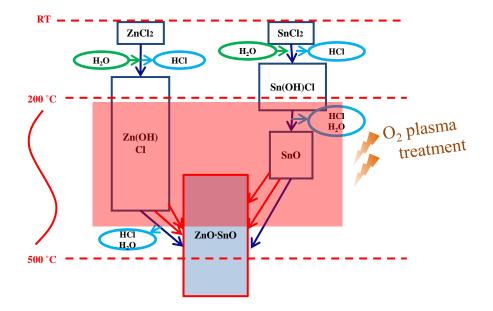


Figure 6-2. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing O_2 plasma treatment

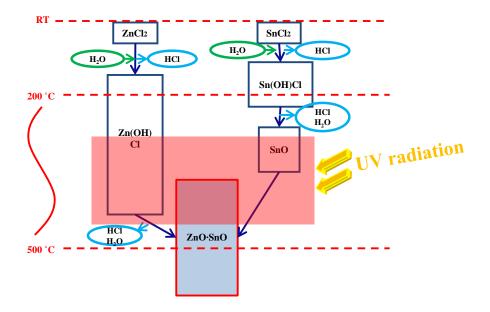


Figure 6-3. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing UV radiation

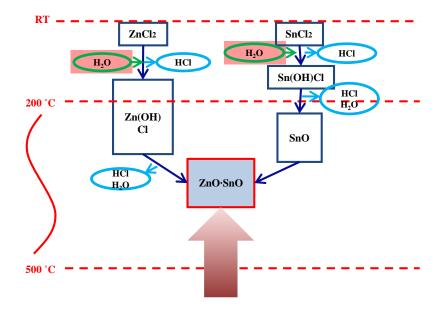


Figure 6-4. Chemical diagram of metal-oxide formation from precursors with the increase in annealing temperature employing biased-H₂O annealing

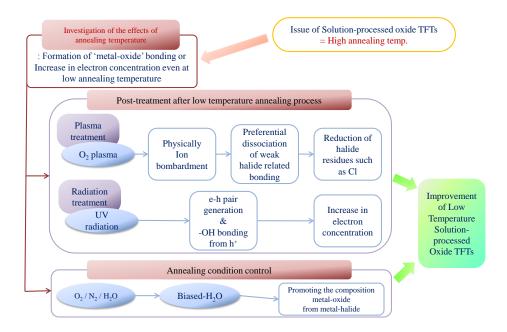


Figure 6-5. Diagram of improvement of low temperature solution-processed

oxide TFTs

Annealing Condition	I_{on}/I_{off}	Vth (* $V_{DS} = 10 \text{ V}$) [V]	$\begin{array}{c} \mu_{sat} \\ [cm^2/V \cdot sec] \end{array}$	S.S [V/dec]
Dry (500 °C)	8×10^{5}	5.80	2.45	1.26
Dry (300 °C)	1×10^{4}	~ 20	0.2	2.32
O ₂ 300 W (350 °C)	106	10.74	0.58	1.20
UV 1 hour (350 °C)	105	12.32	0.30	1.18
Biased-H ₂ O (50% / -20V) (300 °C)	4×10^{5}	3.49	2.19	1.04

Table 6-1. Summary of improved electrical characteristics of solution-processedZTO TFTs with various annealing condition

Bibliography

[1] T. SUNATA, T. YUKAWA, K. MIYAKE, Y. MATSUSHITA, Y. MURAKAMI, Y. UGAI, J. TAMAMURA and S. AOKI, "A large-area high-resolution active-matrix color LCD addressed by a-Si TFT's," Electron Devices, IEEE Transactions on, vol. 33, pp. 1212-1217, 1986.

[2] L. F. WEBER, "Measurement of wall charge and capacitance variation for a single cell in the AC plasma display panel," Electron Devices, IEEE Transactions on, vol. 24, pp. 864-869, 1977.

[3] A. Dodabalapur, "Organic light emitting diodes," Solid State Communications, vol. 102, pp. 259-267, 1997.

[4] W. B. Choi, D. S. Chung, J. H. Kang, H. Y. Kim, Y. W. Jin, I. T. Han, Y. H. Lee, J. E. Jung, N. S. Lee, G. S. Park, and J. M. Kim, "Fully sealed, high-brightness carbonnanotube field-emission display," Applied Physics Letters, vol. 75, pp. 3129-3131, 1999.

[5] H. Meiling, J. Westendorp, J. Hautala, Z. Saleh and C. Malone, "Influence of the deposition rate of the a-Si: H channel on the field-effect mobility of TFTs deposited in a VHF glow discharge," in MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, 1994, pp. 65-65.

[6] C.-y. Chen and J. Kanicki, "High field-effect-mobility a-Si: H TFT based on high deposition-rate PECVD materials," Electron Device Letters, IEEE, vol. 17, pp. 437-439, 1996.

[7] K. SERA, F. OKUMURA, H. UCHIDA, S. ITOH, S. KANEKO and K. HOTTA, "Highperformance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," Electron Devices, IEEE Transactions on, vol. 36, pp. 2868-2872, 1989. [8] K. Shimizu, O. Sugiura and M. Matsumura, "High-mobility poly-Si thin-film transistors fabricated by a novel excimer laser crystallization method," Electron Devices, IEEE Transactions on, vol. 40, pp. 112-117, 1993.

[9] T. Sameshima, S. Usui and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," Electron Device Letters, IEEE, vol. 7, pp. 276-278, 1986.

[10] H. J. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," Applied Physics Letters, vol. 68, pp. 1513-1515, 1996.

[11] C. W. Tang and S. A. VanSlyke, "Organic electroluminescent diodes," Applied Physics Letters, vol. 51, pp. 913-915, 1987.

[12] T. Tohma, "Recent progress in development of organic electroluminescent display devices," in SID CONF REC INT DISPLAY RES CONF. pp. F 1-F 4. 1997, 1997.

[13] M. T. Bernius, M. Inbasekaran, J. O'Brien and W. Wu, "Progress with lightemitting polymers," Advanced Materials, vol. 12, pp. 1737-1750, 2000.

[14] M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, W. Howard and O. Prache, "Polysilicon VGA active matrix OLED displays-technology and performance," in Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International, 1998, pp. 871-874.

[15] M. Stewart, R. S. Howell, L. Pires and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," Electron Devices, IEEE Transactions on, vol. 48, pp. 845-851, 2001.

[16] T. Shimoda, M. Kimura, S. Seki, H. Kobayashi, S. Kanbe, S. Miyashita, R. Friend,J. Burroughes, C. Towns and I. Millard, "Technology for active matrix light

emitting polymer displays," in Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International, 1999, pp. 107-110.

[17] A. Nathan, G. R. Chaji and S. J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," Display Technology, Journal of, vol. 1, pp. 267-277, 2005.

[18] J.-H. Lee, J.-H. Kim and M.-K. Han, "A new a-Si:H TFT pixel circuit compensating the threshold voltage shift of a-Si:H TFT and OLED for active matrix OLED," Electron Device Letters, IEEE, vol. 26, pp. 897-899, 2005.

[19] K. Shih-Chin, Z. Hsiao-Wen, H. Jung-Jie and K. Bo-Cheng, "Self-Heating Effect on Bias-Stressed Reliability for Low-Temperature a-Si:H TFT on Flexible Substrate," Electron Devices, IEEE Transactions on, vol. 57, pp. 588-593, 2010.

[20] Y. Juhn-Suk, J. Sang-Hoon, K. Yong-Chul, B. Seung-Chan, K. Jong-Moo, C. Nack-Bong, Y. Soo-Young, K. Chang-Dong, H. Yong-Kee and C. In-Jae, "Highly Flexible AM-OLED Display With Integrated Gate Driver Using Amorphous Silicon TFT on Ultrathin Metal Foil," Display Technology, Journal of, vol. 6, pp. 565-570, 2010.

[21] N. Young, I. French, M. Trainor, D. Murley, D. McCulloch and R. Wilks, "LTPS for AMLCD on glass and polymer substrates," in Proceedings of the sixth international display workshop, 1999, pp. 219-222.

[22] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Roomtemperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," Nature, vol. 432, pp. 488-492, 2004.

[23] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J.-S. Park, J. K. Jeong, Y.-G. Mo and H. D. Kim, "High mobility bottom gate InGaZnO thin film transistors with SiOx etch stopper," Applied Physics Letters, vol. 90, p. 212114, 2007.

[24] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," Japanese Journal of Applied Physics, vol. 45, p. 4303, 2006.

[25] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering," Applied Physics Letters, vol. 89, p. 112123, 2006.

[26] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo and H. D. Kim, "High performance thin film transistors with cosputtered amorphous indium gallium zinc oxide channel," Applied Physics Letters, vol. 91, p. 113505, 2007.

[27] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee, and J. M. Kim, "Bottom-Gate Gallium Indium Zinc Oxide Thin-Film Transistor Array for High-Resolution AMOLED Display," Electron Device Letters, IEEE, vol. 29, pp. 1309-1311, 2008.

[28] H. S. Shin, B. D. Ahn, K. H. Kim, J.-S. Park and H. J. Kim, "The effect of thermal annealing sequence on amorphous InGaZnO thin film transistor with a plasma-treated source-drain structure," Thin Solid Films, vol. 517, pp. 6349-6352, 2009.

[29] T. Kamiya, K. Nomura, M. Hirano and H. Hosono, "Electronic structure of oxygen deficient amorphous oxide semiconductor a-InGaZnO4–x: Optical analyses and first-principle calculations," physica status solidi (c), vol. 5, pp. 3098-3100, 2008.

[30] H. Seo, Y.-J. Cho, J. Kim, S. M.bobade, K.-Y. Park, J. Lee and D.-K. Choi, "Permanent optical doping of amorphous metal oxide semiconductors by deep ultraviolet irradiation at room temperature," Applied Physics Letters, vol. 96, p. 222101, 2010.

[31] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," Applied Physics Letters, vol. 92,

p. 033502, 2008.

[32] J. Lee, J.-S. Park, Y. S. Pyo, D. B. Lee, E. H. Kim, D. Stryakhilev, T. W. Kim, D. U. Jin and Y.-G. Mo, "The influence of the gate dielectrics on threshold voltage instability in amorphous indium-gallium-zinc oxide thin film transistors," Applied Physics Letters, vol. 95, p. 123502, 2009.

[33] J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang and H.-I. Kwon, "Comparative study of electrical instabilities in top-gate InGaZnO thin film transistors with Al2O3 and Al2O3/SiNx gate dielectrics," Applied Physics Letters, vol. 94, p. 222112, 2009.

[34] C.-T. Tsai, T.-C. Chang, S.-C. Chen, I. Lo, S.-W. Tsao, M.-C. Hung, J.-J. Chang, C.-Y. Wu and C.-Y. Huang, "Influence of positive bias stress on N2O plasma improved InGaZnO thin film transistor," Applied Physics Letters, vol. 96, p. 242105, 2010.

[35] Y.-K. Moon, S. Lee, W.-S. Kim, B.-W. Kang, C.-O. Jeong, D.-H. Lee and J.-W. Park, "Improvement in the bias stability of amorphous indium gallium zinc oxide thinfilm transistors using an O2 plasma-treated insulator," Applied Physics Letters, vol. 95, p. 013507, 2009.

[36] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," Applied Physics Letters, vol. 62, pp. 1286-1288, 1993.

[37] M. J. Powell, C. v. Berkel and J. R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," Applied Physics Letters, vol. 54, pp. 1323-1325, 1989.

[38] W. B. Jackson, J. M. Marshall and M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," Physical Review B, vol. 39, p. 1164, 1989.

[39] M. J. Powell, C. v. Berkel, I. D. French and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," Applied Physics Letters, vol. 51, pp. 1242-1244, 1987.

[40] K. Hoshino, D. Hong, H. Q. Chiang and J. F. Wager, "Constant-Voltage-Bias Stress Testing of a-IGZO Thin-Film Transistors," Electron Devices, IEEE Transactions on, vol. 56, pp. 1365-1370, 2009.

[41] M. Fujii, H. Yano, T. Hatayama, Y. Uraoka, T. Fuyuki, J. S. Jung and J. Y. Kwon, "Thermal Analysis of Degradation in Ga2O3–In2O3–ZnO Thin-Film Transistors," Japanese Journal of Applied Physics, vol. 47, pp. 6236-6240, 2008.

[42] C. In-Tak and et al., "Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses," Semiconductor Science and Technology, vol. 24, p. 015013, 2009.

[43] J.-M. Lee, I.-T. Cho, J.-H. Lee and H.-I. Kwon, "Bias-stress-induced stretchedexponential time dependence of threshold voltage shift in InGaZnO thin film transistors," Applied Physics Letters, vol. 93, p. 093504, 2008.

[44] K. Nomura, T. Kamiya, M. Hirano and H. Hosono, "Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors," Applied Physics Letters, vol. 95, p. 013502, 2009.

[45] K. Nomura, T. Kamiya, Y. Kikuchi, M. Hirano and H. Hosono, "Comprehensive studies on the stabilities of a-In-Ga-Zn-O based thin film transistor by constant current stress," Thin Solid Films, vol. 518, pp. 3012-3016, 2010.

[46] M. D. H. Chowdhury, P. Migliorato and J. Jang, "Time-temperature dependence of positive gate bias stress and recovery in amorphous indium-gallium-zinc-oxide thin-film-transistors," Applied Physics Letters, vol. 98, p. 153511, 2011.

[47] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya and H. Hosono, "Trap densities in amorphous-InGaZnO4 thin-film transistors," Applied Physics Letters, vol. 92, p. 133512, 2008.

[48] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins and I. Ferreira, "Gate-bias stress in amorphous oxide semiconductors thin-film transistors," Applied Physics Letters, vol. 95, p. 063502, 2009.

[49] C. Geng-Wei, C. Ting-Chang, J. Jhe-Ciou, T. Tsung-Ming, S. Yong-En, C. Kuan-Chang, T. Ya-Hsiang, J. Fu-Yen and H. Ya-Chi, "Abnormal Subthreshold Leakage Current at High Temperature in InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 33, pp. 540-542, 2012.

[50] T.-C. Chen, T.-C. Chang, C.-T. Tsai, T.-Y. Hsieh, S.-C. Chen, C.-S. Lin, M.-C. Hung, C.-H. Tu, J.-J. Chang and P.-L. Chen, "Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress," Applied Physics Letters, vol. 97, p. 112104, 2010.

[51] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo and S. Lee, "The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors," Applied Physics Letters, vol. 95, p. 232106, 2009.

[52] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. K. Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee and H. Y. Chu, "Light Effects on the Bias Stability of Transparent ZnO Thin Film Transistors " ETRI Journal, vol. 31, p. 62, 2009.

[53] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U.-I. Chung and J.-H. Lee, "Instability in threshold voltage and subthreshold behavior in Hf--In--Zn--O thin film transistors induced by bias-and light-stress," Applied Physics Letters, vol. 97, p. 113504, 2010.

[54] J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-Y. Kwon, K.-B. Chung, J.-S. Park, B. Koo and S. Lee, "The impact of SiN[sub x] gate insulators on amorphous indium-gallium-zinc oxide thin film transistors under bias-temperature-illumination stress," Applied Physics Letters, vol. 96, p. 193506, 2010.

[55] D. W. Kwon, J. H. Kim, J. S. Chang, S. W. Kim, M.-C. Sun, G. Kim, H. W. Kim, J. C. Park, I. Song, C. J. Kim, U. I. Jung, and B.-G. Park, "Charge injection from gate electrode by simultaneous stress of optical and electrical biases in HfInZnO amorphous oxide thin film transistor," Applied Physics Letters, vol. 97, p. 193504, 2010.

[56] J.-Y. Kwon, J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-S. Park, R. Choi, J. K. Jeong, B. Koo, and S. Y. Lee, "The impact of gate dielectric materials on the light-induced bias instability in Hf–In–Zn–O thin film transistor," Applied Physics Letters, vol. 97, p. 183503, 2010.

[57] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang and S.-H. K. Park, "Photonaccelerated negative bias instability involving subgap states creation in amorphous In–Ga–Zn–O thin film transistor," Applied Physics Letters, vol. 97, p. 183502, 2010.

[58] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon, W. Choi, M. K. Ryu, and S. Y. Lee, "The influence of SiO[sub x] and SiN[sub x] passivation on the negative bias stability of Hf–In–Zn–O thin film transistors under illumination," Applied Physics Letters, vol. 96, p. 262109, 2010.

[59] B. Ryu, H.-K. Noh, E.-A. Choi and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," Applied Physics Letters, vol. 97, p. 022108, 2010.

[60] S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang and J. K. Jeong,
"Improvement in the photon-induced bias stability of Al–Sn–Zn–In–O thin film transistors by adopting AlO[sub x] passivation layer," Applied Physics Letters, vol. 96, p. 213511, 2010.

[61] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, Y. G. Mo and J. K. Jeong, "Comprehensive studies of the degradation mechanism in amorphous InGaZnO transistors by the negative bias illumination stress," Microelectronic Engineering, vol. 88, pp. 1412-1416, 2011.

[62] B. Kim, E. Chong, D. Hyung Kim, Y. Woo Jeon, D. Hwan Kim and S. Yeol Lee, "Origin of threshold voltage shift by interfacial trap density in amorphous InGaZnO thin film transistor under temperature induced stress," Applied Physics Letters, vol. 99, p. 062108, 2011.

[63] J. H. Kim, U. K. Kim, Y. J. Chung, J. S. Jung, S. H. Ra, H. S. Jung, C. S. Hwang, J. K. Jeong and S. Y. Lee, "The effects of device geometry on the negative bias temperature instability of Hf-In-Zn-O thin film transistors under light illumination," Applied Physics Letters, vol. 98, p. 023507, 2011.

[64] S. Kim, S. Kim, C. Kim, J. Park, I. Song, S. Jeon, S.-E. Ahn, J.-S. Park and J. K. Jeong, "The influence of visible light on the gate bias instability of In–Ga–Zn–O thin film transistors," Solid-State Electronics, vol. 62, pp. 77-81, 2011.

[65] K. Nomura, T. Kamiya and H. Hosono, "Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects," Applied Physics Letters, vol. 99, p. 053505, 2011.

[66] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang and S.-H. K. Park, "Transition of dominant instability mechanism depending on negative gate bias under illumination in amorphous In-Ga-Zn-O thin film transistor," Applied Physics Letters, vol. 98, p. 033504, 2011.

[67] S. Yang, K. Hwan Ji, U. Ki Kim, C. Seong Hwang, S.-H. Ko Park, C.-S. Hwang, J. Jang and J. Kyeong Jeong, "Suppression in the negative bias illumination instability of Zn-Sn-O transistor using oxygen plasma treatment," Applied Physics Letters, vol. 99, p. 102103, 2011.

[68] S. Y. Lee, S. J. Kim, Y. W. Lee, W. G. Lee, K. S. Yoon, J. Y. Kwon and M. K. Han, "The Effect of the Photo-Induced Carriers on the Reliability of Oxide TFTs Under Various Intensities of Light," Electron Device Letters, IEEE, vol. 33, pp. 218-220, 2012.

[69] T. Y. Luo, M. Laughery, G. A. Brown, H. N. Al-Shareef, V. H. C. Watt, A. Karamcheti, M. D. Jackson and H. R. Huff, "Effect of H2 content on reliability of ultrathin in-situ steam generated (ISSG) SiO2," Electron Device Letters, IEEE, vol. 21, pp. 430-432, 2000.

[70] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules," Applied Physics Letters, vol. 90, p. 192101, 2007.

[71] J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," Applied Physics Letters, vol. 93, p. 123508, 2008.

[72] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan and L. M. Irving,"Stable ZnO thin film transistors by fast open air atomic layer deposition,"Applied Physics Letters, vol. 92, p. 192101, 2008.

[73] J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," Applied Physics Letters, vol. 92, p. 072104, 2008.

[74] P.-T. Liu, Y.-T. Chou and L.-F. Teng, "Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress," Applied Physics Letters, vol. 95, p. 233504, 2009.

[75] S.-Y. Sung, J. H. Choi, U. B. Han, K. C. Lee, J.-H. Lee, J.-J. Kim, W. Lim, S. J. Pearton, D. P. Norton and Y.-W. Heo, "Effects of ambient atmosphere on the transfer characteristics and gate-bias stress stability of amorphous indium-gallium-zinc oxide thin-film transistors," Applied Physics Letters, vol. 96, p. 102107, 2010.

[76] W.-F. Chung, T.-C. Chang, H.-W. Li, C.-W. Chen, Y.-C. Chen, S.-C. Chen, T.-Y. Tseng and Y.-H. Tai, "Influence of H2O Dipole on Subthreshold Swing of Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors," Electrochemical and Solid-State Letters, vol. 14, pp. H114-H116, 2011.

[77] C.-S. Fuh, S. M. Sze, P.-T. Liu, L.-F. Teng and Y.-T. Chou, "Role of environmental and annealing conditions on the passivation-free in-Ga–Zn–O TFT," Thin Solid Films, vol. 520, pp. 1489-1494, 2011.

[78] S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-C. Chen, C.-T. Tsai, M.-C. Hung, C.-H. Tu, C.-H. Chen, J.-J. Chang and W.-L. Liau, "Effects of Ambient Atmosphere on Electrical Characteristics of Al2O3 Passivated InGaZnO Thin Film Transistors during Positive-Bias-Temperature-Stress Operation," Electrochemical and Solid-State Letters, vol. 14, pp. H177-H179, 2011.

[79] D. L. Staebler and C. R. Wronski, "Optically induced conductivity changes in discharge-produced hydrogenated amorphous silicon," Journal of Applied Physics, vol. 51, pp. 3262-3268, 1980.

[80] M. Stutzmann, W. B. Jackson and C. C. Tsai, "Light-induced metastable defects in hydrogenated amorphous silicon: A systematic study," Physical Review B, vol. 32, pp. 23-47, 1985.

[81] S.-H. Choi and M.-K. Han, "Effect of Deposition Temperature of SiOx Passivation Layer on the Electrical Performance of a-IGZO TFTs," Electron Device Letters, IEEE, vol. 33, pp. 396-398, 2012.

[82] S.-H. Choi, J.-H. Jang, J.-J. Kim and M.-K. Han, "Low-Temperature Organic (CYTOP) Passivation for Improvement of Electric Characteristics and Reliability in IGZO TFTs," Electron Device Letters, IEEE, vol. 33, pp. 381-383, 2012.

[83] W. B. Jackson, R. Hoffman, B. Yeh, T. Emery, T. Koch, C. McConica and O. Kwon,
"Metastability in multicomponent oxide transistors," physica status solidi (a), vol.
207, pp. 695-699, 2010.

[84] J. S. Jung, K.-H. Lee, K. S. Son, J. S. Park, T. S. Kim, J. H. Seo, J.-H. Jeon, M.-P. Hong, J.-Y. Kwon, B. Koo, and S. Lee, "The Effect of Passivation Layers on the Negative Bias Instability of Ga-In-Zn-O Thin Film Transistors under Illumination," Electrochemical and Solid-State Letters, vol. 13, pp. H376-H378, 2010.

[85] S.-I. Kim, S. W. Kim, C. J. Kim and J.-S. Park, "The Impact of Passivation Layers on the Negative Bias Temperature Illumination Instability of Ha-In-Zn-O TFT," Journal of The Electrochemical Society, vol. 158, pp. H115-H118, 2011.

[86] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon, W. Choi, M. K. Ryu, and S. Y. Lee, "The influence of SiOx and SiNx passivation on the negative bias stability of Hf--In--Zn--O thin film transistors under illumination," Applied Physics Letters, vol. 96, p. 262109, 2010.

[87] L. Shou-En, Y. Ming-Jiue, L. Chang-Yu, H. Geng-Tai, C. Chun-Cheng, L. Chih-Ming, L. Chrong-Jung, K. Ya-Chin and Y. Yung-Hui, "Influence of Passivation Layers on Characteristics of a-InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 32, pp. 161-163, 2011. [88] B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, L. Ke, C. Jian-Zhang, S. Wagner, J. C. Sturm, K. Rajan and M. Hack, "Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays With Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic," Electron Device Letters, IEEE, vol. 29, pp. 63-66, 2008.

[89] G. Fortunato, A. Pecora, L. Maiolo, M. Cuscuna, D. Simeone, A. Minotti and L. Mariucci, "Excimer Laser Annealing for Low-Temperature Polysilicon Thin Film Transistor Fabrication on Plastic Substrates," in Advanced Thermal Processing of Semiconductors, 2007. RTP 2007. 15th International Conference on, 2007, pp. 301-305.

[90] J.-S. Park, T.-W. Kim, D. Stryakhilev, J.-S. Lee, S.-G. An, Y.-S. Pyo, D.-B. Lee, Y. G. Mo, D.-U. Jin and H. K. Chung, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," Applied Physics Letters, vol. 95, p. 013503, 2009.

[91] N. Munzenrieder, K. H. Cherenack and G. Troster, "The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs," Electron Devices, IEEE Transactions on, vol. 58, pp. 2041-2048, 2011.

[92] S. Yang, J. Y. Bak, S.-M. Yoon, M. K. Ryu, H. Oh, C.-S. Hwang, G. H. Kim, S.-H. K. Park and J. Jang, "Low-Temperature Processed Flexible In-Ga-Zn-O Thin-Film Transistors Exhibiting High Electrical Performance," Electron Device Letters, IEEE, vol. 32, pp. 1692-1694, 2011.

[93] G. Fortunato, A. Pecora and L. Maiolo, "Polysilicon thin-film transistors on polymer substrates," Materials Science in Semiconductor Processing, 2012.

[94] N. D. Young, M. J. Trainor, S. Y. Yoon, D. J. McCulloch, R. W. Wilks, A. Pearson, S. Godfrey, P. W. Green, S. Roosendaal and E. Hallworth, "Low Temperature Poly-Si

on Flexible Polymer Substrates for Active Matrix Displays and Other Applications," in Materials Research Society Symposium - Proceedings, 2003, pp. 17-28.

[95] S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur and J. Jang, "Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate," Journal of The Electrochemical Society, vol. 151, pp. G167-G170, 2004.

[96] F. Templier, B. Aventurier, P. Demars, J.-L. Botrel and P. Martin, "Fabrication of high performance low temperature poly-silicon backplanes on metal foil for flexible active-matrix organic light emission diode displays," Thin Solid Films, vol. 515, pp. 7428-7432, 2007.

[97] A. Jong-Hyun, K. Hoon-Sik, L. Keon Jae, Z. Zhengtao, E. Menard, R. G. Nuzzo and J. A. Rogers, "High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates," Electron Device Letters, IEEE, vol. 27, pp. 460-462, 2006.

[98] S. D. Theiss and S. Wagner, "Amorphous silicon thin-film transistors on steel foil substrates," Electron Device Letters, IEEE, vol. 17, pp. 578-580, 1996.

[99] S. Maikap, C. Y. Yu, S. R. Jan, M. H. Lee and C. W. Liu, "Mechanically strained strained-Si NMOSFETs," Electron Device Letters, IEEE, vol. 25, pp. 40-42, 2004.

[100] Y. J. Yang, W. S. Ho, C. F. Huang, S. T. Chang and C. W. Liu, "Electron mobility enhancement in strained-germanium n-channel metal-oxide-semiconductor field-effect transistors," Applied Physics Letters, vol. 91, p. 102103, 2007.

[101] T. Afentakis, M. Hatalis, A. T. Voutsas and J. Hartzell, "Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils," Electron Devices, IEEE Transactions on, vol. 53, pp. 815-822, 2006. [102] P.-C. Kuo, A. Jamshidi-Roudbari and M. Hatalis, "Effect of mechanical strain on mobility of polycrystalline silicon thin-film transistors fabricated on stainless steel foil," Applied Physics Letters, vol. 91, p. 243507, 2007.

[103] I.-H. Peng, P.-T. Liu and T.-B. Wu, "Effect of bias stress on mechanically strained low temperature polycrystalline silicon thin film transistor on stainless steel substrate," Applied Physics Letters, vol. 95, p. 041909, 2009.

[104] S. Nai-Chao, W. Shui-Jinn, H. Chin-Chuan, C. Yu-Han, H. Hao-Yuan, C. Chen-Kuo and A. Chin, "Low-Voltage-Driven Flexible InGaZnO Thin-Film Transistor With Small Subthreshold Swing," Electron Device Letters, IEEE, vol. 31, pp. 680-682, 2010.

[105] M. J. Gadre and T. L. Alford, "Highest transmittance and high-mobility amorphous indium gallium zinc oxide films on flexible substrate by roomtemperature deposition and post-deposition anneals," Applied Physics Letters, vol. 99, p. 051901, 2011.

[106] D. H. Lee, K. Nomura, T. Kamiya and H. Hosono, "Diffusion-Limited a-IGZO/Pt Schottky Junction Fabricated at 200 °C on a Flexible Substrate," Electron Device Letters, IEEE, vol. 32, pp. 1695-1697, 2011.

[107] E. Fortunato, P. Barquinha and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," Advanced Materials, vol. 24, pp. 2945-2986, 2012.

[108] S. Lee, S. Park, S. Kim, Y. Jeon, K. Jeon, J.-H. Park, J. Park, I. Song, C. J. Kim, Y. Park, D. M. Kim, and D. H. Kim, "Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors by Using Multifrequency Capacitance-Voltage Characteristics," Electron Device Letters, IEEE, vol. 31, pp. 231-233, 2010.

[109] W. J. Lee, B. Ryu and K. J. Chang, "Electronic structure of oxygen vacancy in crystalline InGaO3(ZnO)m," Physica B: Condensed Matter, vol. 404, pp. 4794-4796, 2009.

[110] K. Nomura, T. Kamiya, H. Yanagi, E. Ikenaga, K. Yang, K. Kobayashi, M. Hirano and H. Hosono, "Subgap states in transparent amorphous oxide semiconductor, In–Ga–Zn–O, observed by bulk sensitive x-ray photoelectron spectroscopy," Applied Physics Letters, vol. 92, p. 202117, 2008.

[111] T. Y. Hsieh, T. C. Chang, T. C. Chen, M. Y. Tsai, Y. T. Chen, F. Y. Jian, Y. C. Chung,
H. C. Ting and C. Y. Chen, "Investigating the Drain-Bias-Induced Degradation Behavior Under Light Illumination for InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 33, pp. 1000-1002, 2012.

[112] B. Kim, C.-I. Ryoo, S.-J. Kim, J.-U. Bae, H.-S. Seo, C.-D. Kim and M.-K. Han, "New Depletion-Mode IGZO TFT Shift Register," Electron Device Letters, IEEE, vol. 32, pp. 158-160, 2011.

[113] S.-H. K. Park, C.-S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J.-I. Lee, K. Lee, M. S. Oh and S. Im, "Transparent and Photo-stable ZnO Thin-film Transistors to Drive an Active Matrix Organic-Light- Emitting-Diode Display Panel," Advanced Materials, vol. 21, pp. 678-682, 2009.

[114] S.-H. Kuk, S.-Y. Lee, S.-J. Kim, B. Kim, S.-J. Park, J.-Y. Kwon and M.-K. Han, "Light-Induced Hysteresis of In-Ga-Zn-O Thin-Film Transistors With Various Temperatures," Electron Device Letters, IEEE, vol. 33, pp. 1279-1281, 2012.

[115] J.-S. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim and C.-J. Kim, "Control of threshold voltage in ZnO-based oxide thin film transistors," Applied Physics Letters, vol. 93, p. 033513, 2008.

[116] G. Zaccanti and P. Bruscaglioni, "Deviation from the Lambert-Beer Law in

the Transmittance of a Light Beam Through Diffusing Media: Experimental Results," Journal of Modern Optics, vol. 35, pp. 229-242, 1988.

[117] A. Janotti and C. G. V. d. Walle, "Oxygen vacancies in ZnO," Applied Physics Letters, vol. 87, p. 122102, 2005.

[118] S.-J. Kim, S.-Y. Lee, Y. W. Lee, S.-H. Kuk, J.-Y. Kwon and M.-K. Han, "Effect of Charge Trapping/Detrapping on Threshold Voltage Shift of IGZO TFTs under AC Bias Stress," Electrochemical and Solid-State Letters, vol. 15, pp. H108-H110, 2012.

[119] J. H. Kim, U. K. Kim, Y. J. Chung and C. S. Hwang, "Correlation of the change in transfer characteristics with the interfacial trap densities of amorphous In– Ga–Zn–O thin film transistors under light illumination," Applied Physics Letters, vol. 98, p. 232102, 2011.

[120] A. Janotti and C. G. Van de Walle, "Native point defects in ZnO," Physical Review B, vol. 76, p. 165202, 2007.

[121] S. J. Clark, J. Robertson, S. Lany and A. Zunger, "Intrinsic defects in ZnO calculated by screened exchange and hybrid density functionals," Physical Review B, vol. 81, p. 115311, 2010.

[122] C. G. Van de Walle, "Hydrogen as a Cause of Doping in Zinc Oxide," Physical Review Letters, vol. 85, pp. 1012-1015, 2000.

[123] S. Kohiki, M. Nishitani, T. Wada and T. Hirao, "Enhanced conductivity of zinc oxide thin films by ion implantation of hydrogen atoms," Applied Physics Letters, vol. 64, pp. 2876-2878, 1994.

[124] Y.-B. Park and S.-W. Rhee, "Effect of hydrogen plasma precleaning on the removal of interfacial amorphous layer in the chemical vapor deposition of microcrystalline silicon films on silicon oxide surface," Applied Physics Letters, vol. 68, pp. 2219-2221, 1996.

[125] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Goncalves, A. J. S. Marques, R. F. P. Martins, and L. M. N. Pereira, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature", Appl. Phys. Lett., Vol.85, No.13, pp.2541-2543, 2004.

[126] H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, and D. A. Keszler, "High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer", Appl. Phys. Lett., Vol.86, No.1, pp.013503, 2005.

[127] S. J. Seo, C. G. Choi, Y. H. Hwang, and B. S. Bae, "High performance solution-processed amorphous zinc tin oxide thin film transistor", J. Phys. D: Appl. Phys., Vol.42, pp.035106, 2009.

[127] Y. J. Chang, D. H. Lee, G. S. Herman, and C. H. Chang, "High-Performance, Spin-Coated Zinc Tin Oxide Thin-Film Transistors ", Electrochem. Solid-State Lett., Vol.10, No.5, pp.H135-H138, 2007.

[129] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors", Appl. Phys. Lett., Vol.93, pp.123508, 2008.

[130] A. Suresh and J. E. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors", Appl. Phys. Lett., Vol.92, pp.033502, 2008.

[131] P. Gorrn, P. Holzer, T. Riedl, W. Kowalsky, J. Wang, T. Weimann, P. Hinze, and S. Kipp, "Stability of transparent zinc tin oxide transistors under bias stress", Appl. Phys. Lett., Vol.90, pp.063502, 2007.

[132] Y. J. Kim, J. S. Lee, Y. U. Lee, and M. K. Han, "High Performance Solution-Processed ZTO Thin-Film Transistor with Spin-Coated ITO Source/Drain Electrodes", International TFT Conference(ITC)'10, pp.22-25, 2010.

[133] A. Janotti and C. G. Van de Walle, "Oxygen vacancies in ZnO", Appl. Phys.Lett., Vol.87, pp.122102, 2005.

[134] M. Lubecka, A. Wegrzyn, and D. Sendorek, "Influence of oxygen vacancy concentration on electrical resistivity in EuO1-x", Thin Solid Films, Vol.131, pp.15-20, 1985.

[135] T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Combinatorial approach to TFTs using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In-Ga-Zn-O system", Appl. Phys. Lett., Vol.90, pp.242114, 2007.

 K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono,
 "Amorphous Oxide Semiconductors for High-Performance Flexible Thin-Film Transistors", Jpn. J. Appl. Phys., Vol.45, No.5B, pp.4303-4308, 2006.

[137] J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, and C. J. Kim, "Control of threshold voltage in ZnO-based oxide thin film transistors", Appl. Phys. Lett., Vol.93, pp.033513, 2008.

[138] J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, and S. I. Kim, "Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by Ar plasma treatment", Appl. Phys. Lett., Vol.90, pp.262106, 2007.

[139] S. H. Jeong, Y. M. Jeong, and J. H. Moon, "Solution-processed Zinc Tin Oxide Semiconductor for Thin-Film Transistors", J. Phys. Chem. C Lett., Vol.112, No.30, pp.11082–11085, 2008.

 Y. H. Yang, S. S. Yang, and K. S. Chou, "Characteristics Enhancement of Solution-Processed In-Ga-Zn Oxide Thin-Film Transistors by Laser Annealing", IEEE Elec. Dev. Lett., Vol.31, No.9, pp.969-971, 2010. [141] G. H. Kim, H. S. Shin, B. D. Ahn, K. H. Kim, W. J. Park, and H. J. Kim, "Formation Mechanism of Solution-Processed Nanocrystalline InGaZnO Thin Film as Active Channel Layer in Thin-Film Transistor ", J. Electrochem. Soc., Vol.156, No.1, pp.H7-H9, 2009.

[142] D. H. Lee, Y. J. Chang, G. S. Herman, and C. H. Chang, "A General Route to Printable High-Mobility Transparent Amorphous Oxide Semiconductors", Adv. Mater., Vol.19, No.6, pp.843-847, 2007.

[143] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard, and H. Sirringhaus, " Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process", Nature Mater., Vol.10, pp.45, 2011.

[144] J. S. Lee, Y. J. Kim, Y. U. Lee, Y. H. Kim, J. Y. Kwon, and M. K. Han, "Effects of Annealing Temperature on Electrical Characteristics of Solution-Processed Zinc Tin Oxide Thin-Film Transistors", Jpn. J. Appl. Phys., Vol.51, pp.061101, 2012.

[145] Y. H. Kim, J. S. Heo, T. H. Kim, S. J. Park, M. H. Yoon, J. W. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, and S. K. Park, "Flexible metal-oxide devices made by room-temperature photochemical activation of sol-gel films", Nature, Vol.489, pp. 128, 2012.

초 록

Zinc tin oxide (ZTO)나 indium gallium zinc oxide (IGZO)를 이용한 용액공정형 산화물 박막 트랜지스터는 고이동도, 빛 투명성, 플렉서블 적합성, 물질의 광범위함, 분자 구성비에 의한 전기적 특성 조절 용이성 등의 장점 때문에 실리콘 기반의 박막 트랜지스터와 유기물 박막 트랜지스터를 대체하며 능동 매트릭스형 디스플레이의 구동 소자로서 상당한 주목을 받고 있다. 용액공정형 산화물 박막 트랜지스터는 능동 매트릭스형 액정표시장치와 능동 매트릭스형 유기발광다이오드 디스플레이 백플레인으로서 많은 문제점을 가지고 있는 실리콘 기반의 박막 트랜지스터와 유기물 박막 트랜지스터와 비교하여 우수한 특성을 보여주고 있다. 더욱이, 용액공정형 산화물 박막 트랜지스터는 우수한 균일성과 고처리량 덕분에 대면적 공정에 적합하다.

ZnO 기반의 산화물 반도체 중에서, Sn 물질을 이용한 ZTO 박막 트랜지스터는 Sn이 널리 사용되고 있는 In 보다 상당히 저가의 물질이기 때문에 저가 공정을 확립하는데 유망한 소자이다.

추가적인 가격 절감과 플렉서블 디스플레이로의 응용성 확장을 위해서 용액공정형 ZTO 박막 트랜지스터는 저렴하고 플렉서블한 기판에 제작되어야 한다. 플렉서블한 기판은 고온에서 쉽게 손상되기 때문에 플렉서블한 기판에 용액공정형 ZTO 박막 트랜지스터가 제작되기 위해서는 저온 공정이 요구된다. 그러나, 저온에서 제작된 용액공정형 ZTO 박막 트랜지스터는 낮은 on-currnet, 높은 문턱 접압, 낮은 이동도 등의 열등한

191

특성을 가지므로, 우수한 특성의 용액공정형 ZTO 박막 트랜지스터를 제작하기 위해서는 500도 이상의 고온 공정이 필요하다. 저온에서 제작된 용액공정형 산화물 박막 트랜지스터의 소자 특성을 향상시키기 위해서는, 용액공정형 산화물 박막 트랜지스터에 대한 어닐링 온도의 영향성과 더불어 저온 공정에서 제작되더라도 우수한 소자 특성을 가지도록 하는 연구가 요구된다. 기존에 용액공정형 산화물 박막 트랜지스터에 대한 어닐링 온도의 영향상을 분석하려는 시도가 있었지만, 용액공정형 산화물 박막 트랜지스터에 대한 어닐링 온도 영향성의 전기적, 화학적 메커니즘은 거의 연구되지 않았다.

이 논문의 목적은 용액공정을 이용하여 다양한 어닐링 온도에서 산화물 박막 트랜지스터를 제작하여 문턱 전압, 포화 이동도, 신뢰성 등의 용액공정형 산화물 박막 트랜지스터의 전기적 특성에 대한 어닐링 온도의 영향성을 분석하고, 제안된 O₂ 플라즈마, 자외선 조사, Biased-H₂O 어닐링 등의 방법을 통하여 능동 매트릭스형 디스플레이를 위한 저온 용액공정 산화물 박막 트랜지스터의 전기적 특성을 향상시키는 것이다.

주요어: 산화물 박막트랜지스터, 용액공정, 어닐링 온도, O₂ 플라즈마, 자외선 조사, Biased-H₂O 어닐링

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