Ph.D. Dissertation

Silicon-rim-reinforced Silicon Nitride Micro-scanner and Wafer-level Vacuum Packaging

실리콘 테두리로 강화된 실리콘 질화막 초소형 스캐너 및 웨이퍼 단위 진공 패키징

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Abstract

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This dissertation presents a novel method to achieve large dynamic range as well as large radius-of-coverture (ROC) of silicon nitride (SiN) microscanner. Optically flat mirror plate in conjunction with a large tilt angle and low driving voltage in SiN microscanner was obtained through the use of a silicon rim and wafer-level vacuum packaging. The silicon rim, attached to the edge of the SiN film, increases the flatness of the mirror plate and enables a vertical comb to be assembled. The vertical comb provides the SiN scanner with a large tilt angle. In addition, vacuum packaging offers low driving voltage of proposed SiN scanner. This work proposed and demonstrated the design and the fabrication process for implementing the silicon-rim-reinforced SiN microscanner. Diameter of mirror plate was 1 mm. 20-100 μm-width silicon rim was tested to investigate optimized width of silicon rim. Thickness of silicon rim and torsional spring was 50 μm. Vertical combs were 10 μm in width, 100 μm in length, and 25 μm in thickness, respectively. Conventional

silicon mirror plate with 50-μm-thick mirror plate was fabricated to compare the performance with silicon nitride scanner. All of them were designed to be same resonant frequency of 15 kHz by different spring width. Mechanical and optical properties were measured, and ROC of more than 300 mm (minimum value required) and driving voltage of 40 % decrease from silicon mirror plate were shown. Moreover, large dynamic range of 32 ° was measured. This was more than 6 times of that of the previous work, and the best result thus far.

This paper not only demonstrated SiN microscanner with large dynamic range, but also achieved the modulation of vacuum-packaged SiN microscanner in wafer-level. Vacuum packaging offers additional shrinkage of the driving voltage owing to the low energy loss due to the viscous flow of the gas molecules. Furthermore, it protects the SiN scanner from the environment and secures the reliability of the performance of the device. This paper proposed and successfully demonstrated the wafer-level vacuum packaging of silicon-rim-reinforced SiN microscanner. Two kinds of fabrication techniques were proposed. Firstly, wafer-level vacuum packaging using glass cap with deep cavity and vertical through-via was proposed. High vacuum level of 1.3 Torr, 1/700 of atmosphere, was demonstrated. Dynamic range was 32° at 85 V_{rms} at a resonant frequency of 14.82 kHz. In addition, he silicon nitride microscanner packaging with silicon through-via substrate has proposed, and led to better production yields and simplicity of back-end process including the wiring and PCB attachment. The through-wafer interconnection (TWIn)

substrate was adapted to offer advanced packaging process. Fabrication method for deep cavity of TWIn substrate was investigated and optimized for optical transparency of cavity in order to prevent from optical signal distortion. Optical verification of cavity suggests its feasibility as optical window for microscanner. SiN scanner packaging using proposed TWIn substrate is demonstrated. Vacuum level of 3.0 Torr and tilt angle of 18 ° at 53.5 V_{rms} have been measured..

The proposed novel SiN scanner has demonstrated superior properties of dynamic range of six times or more of that of reported works and driving voltage of 41% decrease from conventional silicon microscanner. This work contributes to the significant improvement of SiN microscanner, and opens the door to a high resolution microscanner with a low driving voltage.

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Chapter 1

Introduction

This chapter deals with the background of the creation of a silicon nitride thin-film microscanner and gives the objectives of this dissertation. A review of the literature on thin-film microscanners which overcome the limitations of the conventional silicon microscanner is given as well. Among thin-film microscanners, the silicon nitride scanner preferred due to its superior optical and mechanical properties is introduced, and issues which should be overcome in future studies are noted. A novel concept for resolving current issues is briefly introduced. Finally, research objectives and the organization of the dissertation are included.

1.1 Research background

1.1.1 Microscanner and applications using MEMS technology

Micro-electro-mechanical systems (MEMS) led to the fabrication of three-dimensional structures using integrated-circuit fabrication technology [1-6] through the 1960s to the 1990s. MEMS has been successfully adopted to create a micro-pressure sensor [7-11], and it was applied in the area of blood vessel pressure sensing and in industrial control systems in the 1990s.

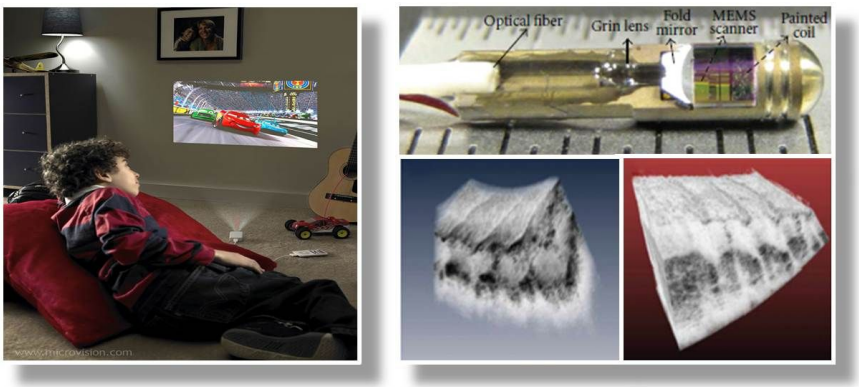
Numerous studies about ink-jet printing [12-15], accelerometers [16-21] and bio-sensors [22-24] were then conducted, followed by the creation of a variety of commercial equipment. Novel micro/nano devices have been realized using MEMS technology.

Specifically, MEMS technology has led to innovations in displays, optical sensors, and in the optical communication industry. Digital displays were realized, and TEXAS Instruments Co. achieved commercialization. Large display projectors and digital cinema film followed [25, 26].

1.1.2 Electrostatic-actuated microscanner and its limitations

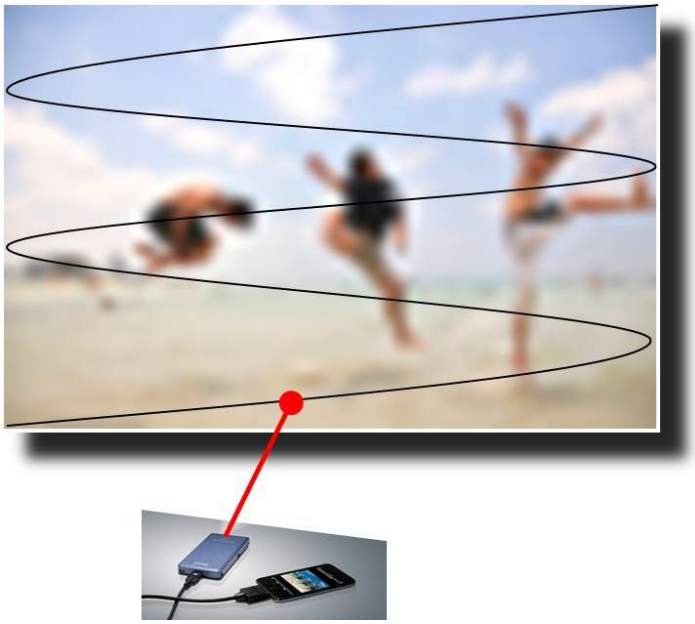
In the display market, microscanners are utilized in high-end applications such as heads-up displays, hand-held projectors, and in endoscopy (Figure 1.1). In recent years, the demand for microscanners for high-resolution displays has increased in keeping with the level of demand in the display market. A high-resolution display requires a high-speed and/or a high-resonant-frequency microscanner. Figure 1.2 illustrates the relationship between a high resolution and a high resonant frequency of a scanner. With the same frame rate, it is fairly straightforward to understand that a higher horizontal frequency scans more lines, thus enabling a higher resolution.

(a)



(b) (c)

Figure 1.1. Applications of microscanners in the display market: (a) heads-up display, (b) hand-held projector, and (c) endoscopy



(a)

(b)

Figure 1.2. Comparison of scanned images using (a) a low-speed scanner and (b) high-speed scanner

Typically, an electrostatic actuated microscanner consists of a mirror plate and a couple of torsional springs (Figure 1.3). In this case, the resonant frequency f_o of the microscanner can be denoted as follows:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{I}} \tag{1}$$

where k is spring constant and I is moment of inertia [27].

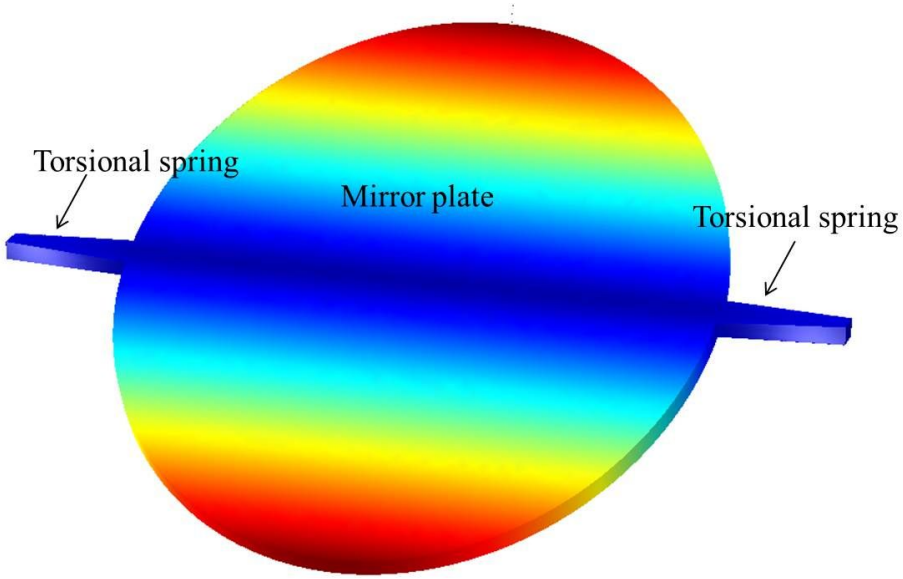


Figure 1.3. Configuration of a typical electrostatic-actuated microscanner

The conventional means of achieving a high resonant frequency is to increase the spring constant k. This method has been preferred because a high k is simply achieved by increasing the spring width or decreasing the spring

length. However, a higher spring constant requires greater force to deform the spring, which is directly related to the issue of a high driving voltage.

Another method is to decrease I in equation (1). Because the spring constant does not change, a higher resonant frequency can be realized without the cost of a higher driving voltage. A lower I requires a lightweight mirror plate. Specifically, a mirror plate consisting of a thin film several micrometers thick drastically decreases the moment of inertia. Therefore, various studies have been conducted on microscanners with a thin-film mirror plate.

1.2 Literature review: thin-film mirror plate micromirror

Among the various thin film materials, poly-silicon and silicon nitride thin film are widely used because an optically flat mirror plate of thin film requires residual stress. A comparison of reported thin film-based micromirrors is given in Table 1.1.

Table 1.1. Comparison of Thin Film-Based Micromirrors

Flattening method	Film thickness (μm)	ROC (mm)	Dynamic Range (˚)	f_o (kHz)	Actuator	Ref.
Poly-silicon thin film microscanner						
Curvature compensation	3.5	111	-	-	Vertical comb	[28]
SCS-rib	1.5	173	-	3	Lateral comb	[29]
SCS-rib	1	1260	-	24.1	Vertical comb	[30]
Poly-Si rib	2	150	11.2	1.8	Vertical comb	[31]
Silicon nitride thin film microscanner						
SiN-rib	1.5	60	8	0.4	Parallel plate	[32]
SiN-rib	2.5	1220	-	-	Parallel plate	[33]
SiN folded frame	2.5	179	5.5	17.7	Parallel plate	[34]

1.2.1 Poly-silicon thin-film micromirror

Poly-silicon thin film has an optically smooth surface created by low-pressure chemical vapor deposition (LPCVD). Moreover, it can be easily manufactured through the commonly used silicon-based fabrication process. Therefore, many papers about poly-silicon thin-film microscanners have been reported. However, the residual tensile stress bends the poly-silicon thin film and deteriorates the flatness of the mirror plate. Cao et al. [28] devised a simple compensation scheme to achieve a flat mirror plate. With the deposition of a thin dielectric layer of silicon dioxide, a 3.5 μm-thick mirror plate with a radius-of-curvature (ROC) of 111 mm was fabricated. However, it required precise control of the LPCVD process and had issues related to the repeatability of the process. Moreover, the ROC of the mirror plate was not sufficient for use in a microscanner (ROC>300 mm). Nee et al. [29] reported that a single-crystal silicon rib on the edge of the poly-silicon mirror plate ensured a flat mirror surface. However, the ROC of 36 mm was small. Moreover, because the supporting rib and the mirror plate were made of the same material, i.e., silicon, complicated surface micromachining was required so that the thin mirror plate was not damaged during the manufacturing of the silicon supporting rib. Nee et al. [30] suggested a thicker and wider supporting rib to achieve a large ROC (1260 mm). In order to assemble the vertical comb actuator, fusion bonding between the top and bottom silicon layer as well as chemical mechanical polishing was performed. Although a high resonant

frequency of 24.1 kHz and a flat mirror plate were realized, a complicated surface and bulk micromachining were needed to retain the thin poly-silicon mirror during the fabrication of the vertical comb actuator and the supporting rib.

Because a single-crystal rib requires complicated bulk micromachining such as bonding and a CMP process, Wu et al. [31] proposed a poly-silicon rib underneath the thin mirror plate. The poly-silicon rib could be fabricated through surface micromachining, and it offered a flat mirror plate without the need for bonding or CMP. Although this method led to an optical tilt angle of 11.2 ° at a low voltage (50 V) at a high resonant frequency 1.8 kHz, the reported ROC of 150 mm was not sufficient. Moreover, complicated surface micromachining was necessary in order to release the microscanner from the silicon substrate via silicon wet etching without damage to the scanner.

1.2.2 Silicon nitride thin-film micromirror

Although poly-silicon thin-film scanners have the benefit of compatibility with the conventional silicon-based fabrication process, a complicated process is typically required to release the microscanner without damaging the thin film. In contrast, silicon nitride thin film can be selectively etched onto silicon by reactive ion etching. Therefore, a micromirror made of silicon nitride does not require complicated processes to protect the mirror plate during the release process. However, residual stress remains an issue to be resolved to

achieve a flat mirror plate. Similar to the poly-silicon micromirror, reinforcement of silicon nitride film has been shown to be a promising method to overcome residual stress. Lutzenberger et al. [32] proposed a silicon nitride rib to reinforce a thin-film mirror plate. Because their microscanner was composed of silicon nitride, a complicated release process was not needed. However, the optical tilt angle was only 8 ° at 51 V, and resonant frequency of 400 Hz was low. These values resulted from the low driving force and the limited dynamic range of the parallel plate actuator. Moreover, because marks made by the silicon nitride rib underneath the silicon nitride film appeared on the surface, this area could not be used as a reflective surface. Therefore, the optical surface was only 400 μm with a microscanner diameter of 1 mm. The 60 mm ROC of the optical surface was not sufficient for use as a reflective surface either. In order to overcome the issue of a small ROC, other researchers proposed a periodic silicon nitride rib underneath the mirror plate [33]. Although the periodic reinforcing rib increased the ROC to 1220 mm, rib marks appeared on the optical surface, severely deteriorating its optical smoothness.

Lin et al. [34] reported a reinforcement method for silicon nitride thin film without rib marks using a folded silicon nitride frame on the edge of the mirror plate. The folded frame reinforced the flatness of the silicon nitride thin film and achieved a ROC of 179 mm. They demonstrated an optical tilt angle of 5.5 ° at 33 V_{rms} at a high resonant frequency of 17.7 kHz as well.

However, the ROC was less than 300 mm and the dynamic range of 5.5 ° was not sufficient for high resolutions. The small dynamic range was caused by the limitation of the dynamic range of the parallel plate actuator.

1.3 Research motivation

The display market requires high-speed microscanners for use in high-resolution displays. In order to achieve a high-speed microscanner, a scanner with a higher resonant frequency is needed. Rather than increasing the spring constant, decreasing the weight of the mirror plate is considered as a promising means of circumventing the high driving voltage issue. A thin-film mirror plate effectively decreases the mirror plate mass. Poly-silicon thin-film microscanners have been reported by a variety of researchers in an effort to realize a thin-film mirror plate. However, the fixed etch rate of the poly-silicon to the silicon substrate complicated the manufacturing process as part of the required steps to avoid damage to the mirror plate during the fabrication of the actuators and the release of the microscanner. In contrast, a silicon nitride microscanner has the benefits of a selective etch rate of the silicon nitride to the silicon substrate and a simple subsequent fabrication process. However, reported papers have dealt only with acquiring a flat mirror plate considering the tensile stress on the silicon nitride film. Although these studies achieved large ROC values, the dynamic ranges were typically less than 10 ° and the product of the optical tilt angle θ_{opt} and the mirror diameter D was less than 4 °·mm. Considering that VGA displays require a $\theta_{opt} \cdot D$ product of more than 30 °·mm, these results were not sufficient for a high-resolution display. Therefore, silicon nitride thin-film scanners require additional

research to realize a large dynamic range and a large $\theta_{opt} \cdot D$ product that exceeds 30 $^{\circ}$·mm while securing flatness with an ROC value of more than 300 mm at the same time.

1.4 Research overview of silicon-rim-reinforced silicon nitride scanners with a vertical comb actuator

This research presents a novel method to achieve a large dynamic range as well as a large ROC in a silicon nitride thin-film micromirror. Moreover, wafer-level packaging process is given to decrease driving voltages and protect devices from external environment. Reported studies typically show a low dynamic range when the mirror plate and the ribs are made of the same material, i.e., silicon nitride. Therefore, the overall thickness of the mirror plate was thin such that a parallel plate actuator was essential, leading to a limited dynamic range caused by the pull-in effect as well. The current study proposes a single-crystal silicon rim on the edge of the mirror plate instead of a silicon nitride rib. This silicon rim minimizes the deformation of the thin-film mirror plate and offers a large ROC. Moreover, a vertical comb actuator was assembled onto the silicon rim. This actuator leads to large dynamic range compared to a parallel plate actuator. Moreover, low driving voltage was achieved using wafer-level packaging compared to reported studies.

The silicon nitride of the mirror plate is deposited to thickness of 1 μm using LPCVD, showing good optically smoothness ($<\lambda/10$). The silicon rim and vertical comb actuator are defined by the deep-reactive ion etching (DRIE) of the single-crystal silicon substrate. The width of the silicon rim ranges in size from 20 μm to 100 μm. The vertical combs with a thickness of 25 μm and a

length of 100 μm were attached to the rim, resulting in a large dynamic range of the silicon nitride thin-film microscanner. Wafer-level packaging was accomplished using two different method, glass cap packaging and TWIn substrate packaging. Vacuum level less than 3 Torr offered high quality factor which resulted in large tilt angle in low driving voltage.

1.4.1 Silicon-rim-reinforced silicon nitride microscanner

A silicon-rim-reinforced silicon nitride scanner was fabricated and the feasibility of large ROC and large dynamic range was investigated (Figure 1.4). The silicon rim was successfully fabricated, and it stiffened the silicon nitride thin film. Vertical combs were attached to the silicon rim with a thickness of 25 μm. A 20-100 μm-width silicon rim was tested to determine its optimal width. A conventional silicon mirror plate was fabricated to compare the performance with that of a silicon nitride scanner. All samples were designed to have the same resonant frequency of 15 kHz with different spring widths. The mechanical and optical properties were measured, and a ROC of more than 300 mm and a driving voltage showing a 40% decrease relative to that of a silicon mirror plate were demonstrated. A large dynamic range of 32° was measured using a vacuum chamber at an ambient pressure of 1.2 mm Torr.

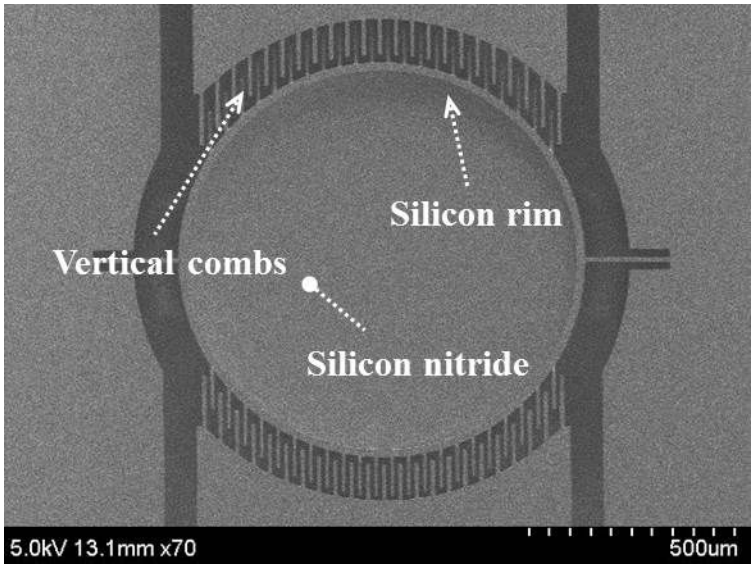


Figure 1.4. Silicon nitride microscanner reinforced using a silicon rim

1.4.2 Wafer-vacuum-packaging using a glass cap

This modularized vacuum-level-actuated silicon nitride scanner was fabricated on a single chip by vacuum packaging (Figure 1.5). Vacuum packaging enabled the vertical-comb-actuated silicon nitride microscanner to have a maximum tilt angle at a low driving voltage. Vacuum packaging was achieved by bonding a glass cover with a deep cavity onto the top and bottom sides of the scanner. On the bottom glass wafer, through-vias were formed to supply driving voltage to the silicon nitride scanner. An optimized process for the deep cavity on the glass wafer was investigated, resulting in a pit-free glass wafer with a 250-μm-deep cavity. A large dynamic range of more than 30 ° was confirmed in a single chip. Packaging reliability was investigated using a thermal cycling test, a die shear strength test, and vacuum-level

uncertainty measurements over time.

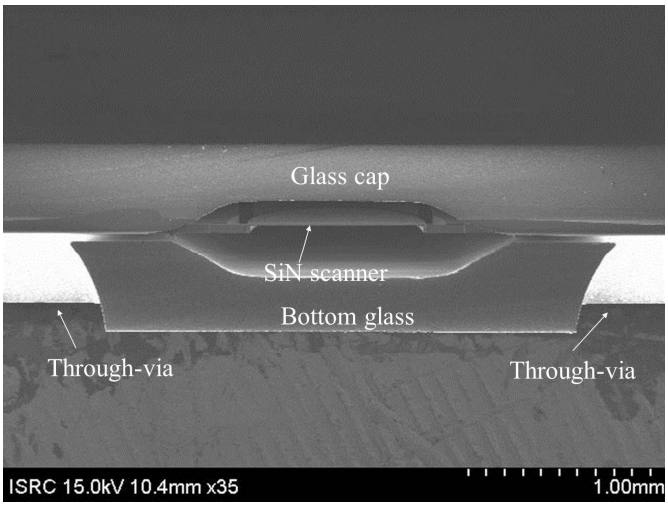


Figure 1.5. Cross-section of the vacuum-packaged microscanner

1.4.3 Wafer-level vacuum packaging using a TWIn substrate

Wafer-level vacuum packaging of silicon nitride microscanners using TWIn substrate showed improved fabrication of the through-vias, leading to better production yields and a simpler back-end process, including the wiring and PCB attachment. A through-wafer interconnection (TWIn) substrate was adapted, offering an advanced packaging process. The TWIn substrate was composed of a silicon through-via and reflowed glass. The silicon through-via was fabricated by the anisotropic etching of silicon, offering the benefits of minimized through-via dimensions and a simple back-end process. The reflowed glass isolated the silicon vias and served as an optical signal conduit due to its transparency. Specifically, the fabrication method for a deep cavity

on the TWIn substrate was investigated and optimized for optical transparency of the cavity in order to prevent distortion of the optical signal. The vacuum level and dynamic range of the third-generation microscanner were measured as well.

1.5 Research objectives and dissertation organization

This research focuses on an advanced silicon nitride thin-film microscanner. A silicon nitride microscanner has the benefit of a low driving voltage at the high resonant frequency required to achieve a high-resolution display. Earlier studies accomplished a flat thin-film mirror plate made of silicon nitride using an impressive method involving silicon nitride ribs and a folded frame. However, the small dynamic range limited by the parallel plate actuator has been an issue that prevents the use of high-resolution displays. The objective of this research is to propose and demonstrate a novel method to achieve a large dynamic range as well as sufficient flatness of the thin film. The study proposes a single-crystal rim assembled with a vertical comb actuator for a large dynamic range and a large ROC. Moreover, a wafer-level vacuum package process is proposed to achieve a low driving voltage of less than 100 V_{rms} for the maximum dynamic range in a single chip. Chapter 2 discusses the details of design and numerical analysis of proposed SiN scanner and wafer-level vacuum packaging. The maximum dynamic range was confirmed using a vacuum chamber. Chapter 3 shows fabrication process and results of silicon rim reinforced SiN scanner and the modularization of the vacuum-packaged silicon nitride scanner. Chapter 4 deals with characterization of SiN scanner and demonstrates a large dynamic range, large ROC and low driving voltage. The vacuum level and packaging reliability are investigated. The vacuum

packaging of silicon nitride microscanner using the glass cap and the TWIn substrate is described. Finally, the conclusion gives a brief discussion about future works as well as a summary of this research.

1.6 Contributions

This research focuses on a silicon nitride thin-film microscanner with optically flatness as well as a large dynamic range. A novel idea of a single-crystal silicon rim assembled with a vertical comb actuator was proposed and the optical and mechanical properties were verified.

The proposed novel SiN scanner demonstrates superior properties of its dynamic range that are at least fourfold of those in earlier works as well as a driving voltage showing a 41% decrease relative to that of a conventional silicon microscanner. This work contributes to the significant improvement of SiN microscanners and opens the door to a high-resolution microscanner with a low driving voltage. Moreover, the study contributes not only to the advancement of silicon nitride scanners but also to the advancement of the fabrication technology related to deep-cavity glass wafers and optically transparent TWIn substrates.

As for the fabrication techniques, a novel wet-etching mask for deep cavities in glass wafers including borosilicate glass and fused silica has been proposed and implemented to realize wafer-level vacuum packaging of microscanner. In addition, fabrication techniques for the silicon through-via substrate with deep cavity have been developed. Simple fabrication for an optically smooth surface of dry-etched silicon during fabrication of silicon through-via substrate has been proposed. Moreover, the reflow process of glass has been

optimized for the optically transparent window of the cavity of silicon through-via substrate. Furthermore, three-stack anodic bonding using conductive aluminum foil as the ion moving path has been demonstrated to achieve the packaging of microscanner. Simple fabrication of the silicon rim and the SiN mirror plate using SiN as an etching stop layer has been proposed as well.

In this paper, a novel concept of a silicon rim to meet flatness requirements as well as a large dynamic range was proposed in silicon nitride microscanner. It demonstrated a large dynamic deformation at a low voltage compared with a conventional silicon scanner. Moreover, this paper proposed a wafer-level vacuum packaging process for the silicon nitride scanner with a glass cap or a TWIn substrate. The optical effectiveness of the glass cap and the TWIn substrate with deep cavities has been demonstrated of packaged SiN scanner. Moreover, reliability of vacuum packaging for the proposed fabrication process has been proved.

Chapter 2

Design and numerical analysis of SiN scanner and wafer-level vacuum packaging

This chapter deals with proposal and numerical analysis of silicon-rim-reinforced silicon nitride microscanner with vertical comb actuator and its wafer-level vacuum packaging. Silicon rim assembled by vertical comb actuator is introduced in order to resolve the limited dynamic range of existing silicon nitride scanner while confirming large radius-of-curvature. Wafer-level packaging is mentioned so as to decrease driving voltage and protect microscanner from external environment. Behavior of proposed SiN scanner and characteristics of packaged scanner is numerically analyzed. Optical and mechanical properties are mentioned and verify feasibility of large dynamic range and large ROC.

2.1 Introduction

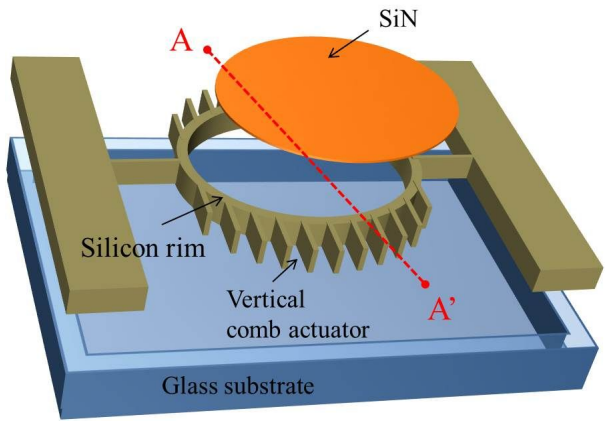
Reported silicon nitride thin film microscanners achieved flat mirror plate successfully. However, small dynamic range due to limited movement of parallel plate actuator has been issue to be resolved. The chapter presents a

novel means of achieving a large dynamic range as well as a large ROC in a silicon nitride thin-film micromirror. A single-crystal silicon rim on the edge of the mirror plate is proposed for the reinforcement of the SiN mirror plate used here. The silicon rim minimizes the deformation of the thin-film mirror plate and offers a large ROC. Moreover, a vertical comb actuator can be assembled onto the silicon rim, giving the device a large dynamic range. Furthermore, the proposed wafer-level packaging process protects the microscanner from the environment, secures the reliability of the performance of the device and improves the scanner efficiency by increasing the quality factor. These approaches open the door for optical scanning with a high resolution and a low driving voltage together with high performance reliability.

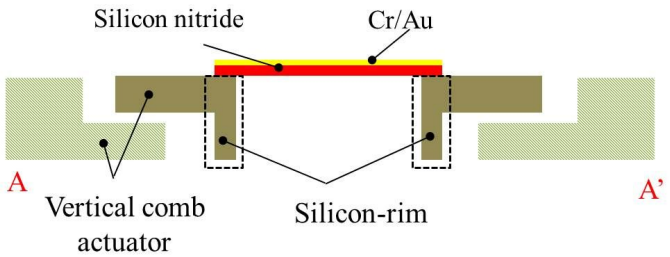
2.2 Design

2.2.1 Silicon-rim-reinforced SiN scanner

We propose a silicon rim in conjunction with a vertical comb actuator for dual purposes, i.e., the realization of a flat silicon nitride mirror plate and a large dynamic range. Figure 2.1 illustrates a schematic of the proposed one-degree-of-freedom silicon nitride scanner. The microscanner consists of a SiN thin-film mirror plate, a silicon rim and a vertical comb actuator.



(a)



(b)

Figure 2.1. Illustration of (a) schematic of proposed silicon nitride scanner, and (b) cross section along AA'

The SiN thin-film mirror plate has a thickness of 1 μm and a diameter of 1 mm, respectively. SiN was deposited by low-pressure chemical vapor deposition (LPCVD) for an optically smooth surface. The large of 1 mm offers a large aperture in the microscanner and increases the resolution. The tensile stress of the SiN prevents the bumpy deformation of the thin-film mirror plate. Gold with a chrome adhesion layer is coated onto the silicon nitride film as a reflective surface. The thickness of the gold and the chrome was thin (10 nm of chrome and 40 nm of gold) so as not to affect the flatness of the mirror plate due to the residual stress caused by the gold and chrome.

The silicon rim is attached underneath the silicon nitride thin film. Deep-reactive-ion etching (DRIE) of the single-crystal silicon substrate fabricated the silicon rim. The non-residual stress and mechanical stiffness of the single-crystal silicon stiffened the silicon nitride mirror plate. The thickness of the silicon rim was designed to be 50 μm considering the mechanical stiffness and thickness of the vertical combs. The width of the silicon rim ranged from 20 μm to 100 μm. Optimized sizes of the radius-of-curvature (ROC) and the driving voltage were investigated.

Vertical combs were assembled onto the edges of the silicon rim. Moving and fixed combs were fabricated in the silicon rim and fixed electrodes, respectively. The combs were 25 μm thick, 10 μm wide and 100 μm long. The gap between the straightforward fixed comb and the moving comb was 10 μm,

and there were 22 moving combs per side. Compared with a parallel plate actuator, the vertical comb actuator has large electrical force and no pull-in phenomenon. Therefore, it offers a large dynamic range and a low driving voltage.

Two torsional springs enable the microscanner to tilt along its torsional axis. The springs consist of single-crystal silicon. The length and thickness are 210 μm and 50 μm, respectively. The width varies according to the width of the silicon rim in order to achieve a resonant frequency of 15 kHz.

Three types of SiN scanner were designed with different widths of the silicon rim and the corresponding spring width to achieve the same resonant frequency of 15 kHz. In addition, a silicon mirror plate with a thickness of 50 μm was used to fabricate a conventional silicon microscanner as a control. The spring width in this case was 19.6 μm in order to maintain 15 kHz, as in the silicon nitride scanner.

The sizes of the designed scanner are summarized in Table 2.1 and 2.2 as follows.

Table 2.1. Dimensional size of the SiN Scanner

Microscanner	Die size	10 mm × 6 mm
Mirror plate	Diameter	1 mm
	Thickness	1 μm
Silicon rim	Width	20~100 μm
	Thickness	50 μm
Vertical comb	Width	10 μm
	Thickness	25 μm
	Length	100 μm
	Gap	10 μm
Spring	Width	12~19.8 μm
	Thickness	50 μm
	Length	210 μm

Table 2.2 Dimensional size of each type of SiN scanner

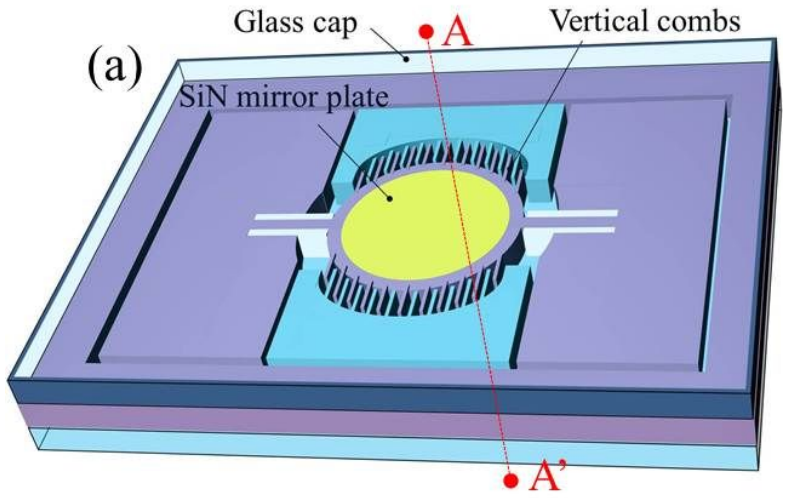
Type	**Si**	**Rim20**	**Rim50**	**Rim100**
Rim width	-	20 μm	50 μm	100 μm
Silicon thickness	50 μm			
f_o	15 kHz			
Silicon width	19.8 μm	12 μm	14.4 μm	16.8 μm

2.2.2 Wafer-level vacuum packaging

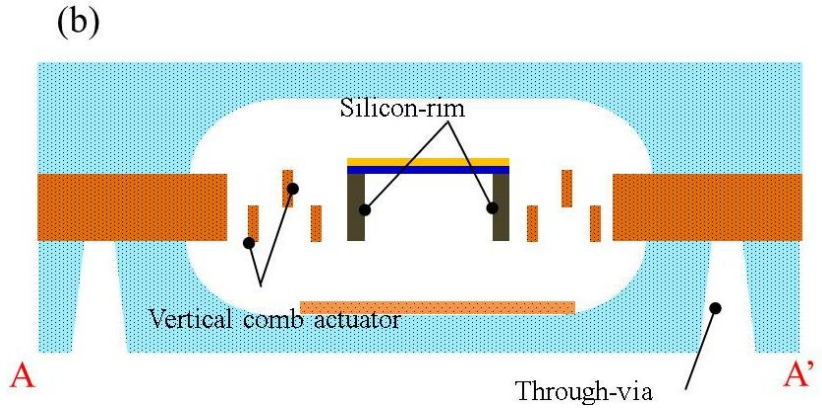
2.2.2.1 Packaging using glass cap

The SiN scanner is composed of a thin film mirror plate, a silicon rim, and vertical combs (Figure 2.2). A mirror plate with a diameter of 1 mm is made from1 μm-thick silicon nitride, giving it an extremely low weight. The reflectivity of the mirror plate stems from its use of Cr/Au (10nm/60 nm) metal. The flatness of the SiN mirror plate is ensured by a 50 μm-thick silicon rim attached to the underside of the mirror plate. The silicon rim has a width of 20 μm to minimize the effect of the silicon rim on the total mass of the mirror plate. The silicon rim offers the flatness of the mirror plate and provides the platform for the vertical combs to be assembled. The vertical comb actuator does not undergo the pull-in effect resulting in limited tilt angle. Therefore, an optical tilt angle of more than 180° can be obtained in principle. A flat mirror plate and a large tilt angle in a SiN scanner can be realized with a silicon rim and a vertical comb actuator.

Vacuum packaging of the SiN scanner was accomplished by means of the anodic bonding of the top and bottom glass under a vacuum condition. Vacuum packaging enhances the performance and reliability of the scanner by giving it a high quality factor (Q factor) and protecting it from the external environment. A 210-μm-deep cavity is formed in either glass to provide an actuation space for the movement of the scanner. The driving signal is supplied to the packaged scanner using a through-via in the bottom glass.



(a)



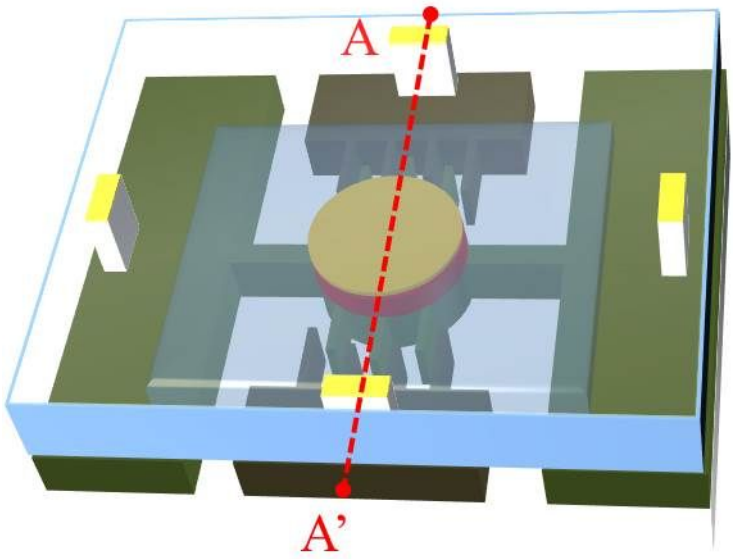
(b)

Figure 2.2. Schematic of the design of packaging using glass cap: (a) Overall design and (b) cross-section along AA'

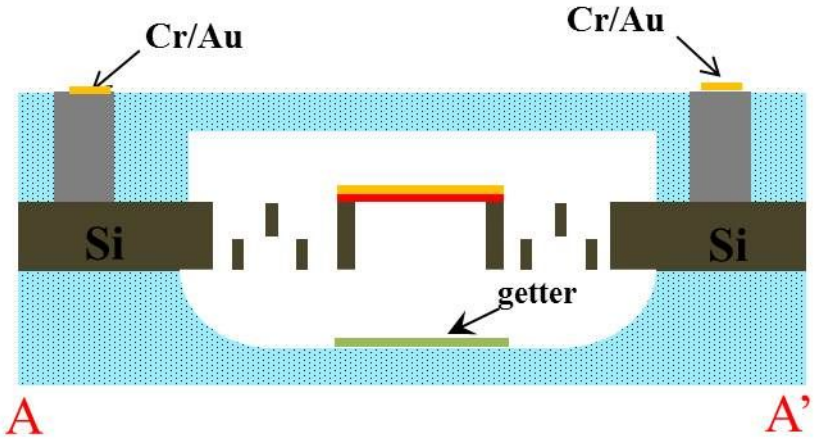
2.2.2.1 Packaging using TWIn substrate

Figure 2.3 shows design of vacuum packaging of SiN scanner with TWIn substrate. Device comprises of TWIn substrate, device layer, and bottom glass. TWIn substrate on the top side provides optical window of the packaging and electric interconnection into packaged microscanner. Deep cavity is formed to offer the space of scanner actuation. SiN scanner reinforced by silicon rim is fabricated in the device layer. Bottom glass provides deep cavity and packaged SiN scanner on the bottom side.

Figure 2.4 shows a schematic view of silicon through-via substrate with a deep glass cavity. The substrate is composed of silicon through-via, reflowed glass and deep cavity. The silicon through-via serves to transmit electric signals inside packaging when the substrate is used as a cover of the vacuum packaging. In order to obtain sufficient conductivity, a silicon with low resistivity (0.001 ~ 0.003Ω · cm) is used. Silicon via has benefits of no void inside the via. Silicon via is perfectly isolated by reflowed glass. Similar coefficient of thermal expansion prevents generation of crack during eutectic bonding in high temperature The reflowed glass allows optical signal to be transmitted as well. The deep cavity secures a space for acuation of the optical devices.



(a)



(b)

Figure 2.3. Schematic of packaged SiN scanner using TWIn susbtrate: (a) Overall design and (b) cross-section along AA'

The silicon through-via is 1 mm × 0.7 mm. Thickness of the TWIn substrate is 250 μm. The cavity is 2.4 mm long, 2.0 mm wide, and 0.15 mm thick, respectively. The deep glass cavity of 150 μm enables micro-devices to have large dynamic deformation. Wide window of glass cap is designed for the laser beam not to be distorted through the glass. SiN scanner and bottom glass wafer are same with previously mentioned design. Packaged SiN scanner can be simply wired on the top side as shown in Figure 2.5.

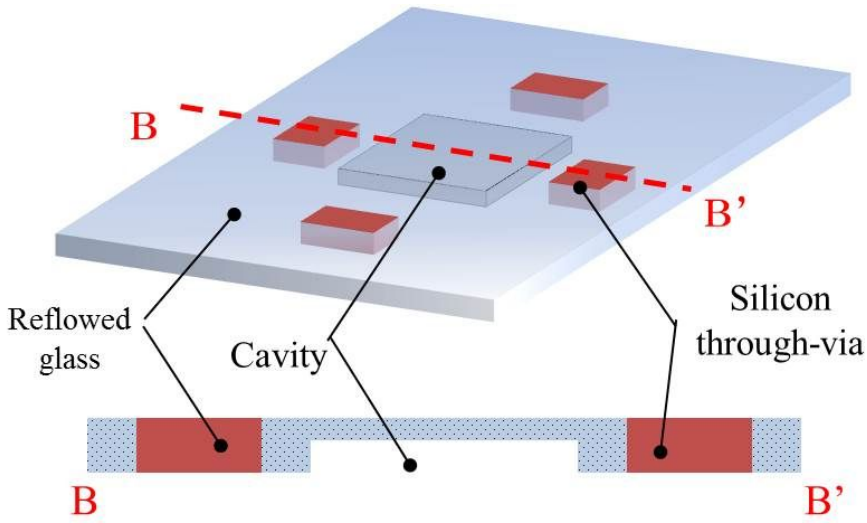


Figure 2.4. Schematic design of TWIn substrate with deep cavity: (a) Overall design and (b) cross-section along BB'

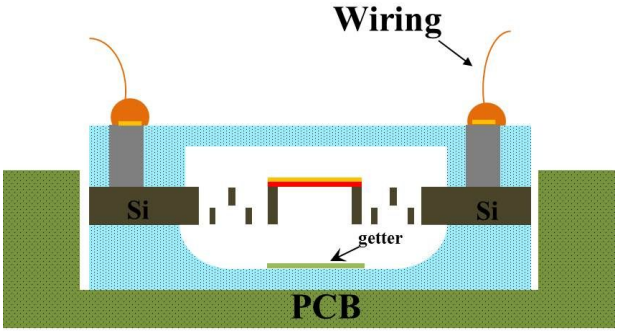


Figure 2.5. Attachment of packaged SiN scanner to PCB and wiring

2.3 Numerical analysis of silicon nitride microscanner

2.3.1 Dynamic characteristics

The microscanner tilts along two torsional springs. Therefore, the resonant frequency in the torsional mode is related to the spring constant. It can be expressed as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{c}{I}} \tag{2.1}$$

where c is the spring constant of the two torsional springs and I is the moment of inertia of the microscanner. The spring constant is a function of the dimensional size of the spring via the following equation [27]:

$$c = 2\frac{kGt_s w_s^3}{l_s} \quad (w_s<t_s) \tag{2.2}$$

Here, $G=E/(2(1+v))$. In addition, G denotes the shear modulus of the silicon, E is the Young's modulus, v is the Poisson ratio, k denotes the cross-section shape-dependent factor, l_s is the spring length, t_s represents the spring thickness, and w_s is the spring width. In the single-crystal silicon, E and v were determined to be 168 GPa and 0.28, respectively. The value of k is

expressed as follows [27]:

$$k = \frac{1}{3}\left(1 - \frac{192}{\pi^5}\left(\frac{w_s}{t_s}\right) \times \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n^5} tanh\left(\frac{n\pi t_s}{2w_s}\right)\right) \quad (2.3)$$

Meanwhile, the moment of inertial I is composed of the terms from the mirror plate and the moving combs via the following equation:

$$I = I_{mirror} + I_{combs} \quad (2.4)$$

Here, I_{mirror} denotes the moment of inertia of the silicon nitride mirror plate and I_{combs} is the moment of inertia of the moving combs. In addition, the mirror plate consists of SiN thin film and a silicon rim. Therefore, the calculation of I_{mirror} should be divided into calculations of its components. Calculation of the moment of inertia of the silicon rim $I_{silicon\text{-}rim}$ is straightforward, as follows:

$$I_{silicon-rim} = \int r^2 dm = \int_0^{2\pi} (r sin\emptyset)^2 \cdot (\rho_{si} t_{si} dA)$$

$$= 4\rho_{si} t \int_0^{\pi/2} r^3 sin^2\emptyset d\emptyset dr = \frac{\pi}{4}\rho_{si} t_{si}\left({R_{out}}^2 - {R_{in}}^2\right) \quad (2.5)$$

Here, ρ_{si} is density of silicon (2330 kg/m^3). Other parameters are displayed in as shown in Figure 2.6.

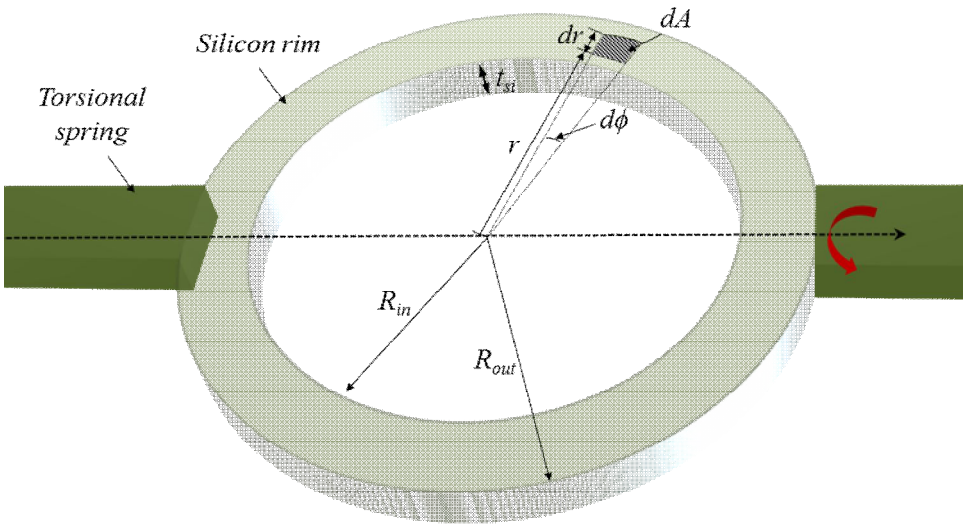


Figure 2.6. Illustration of the silicon rim of the SiN scanner for the numerical analysis

The moment of inertia of the SiN film I_{SiN} is expressed in equation (2.6) by extension from (2.5):

$$I_{SiN} = \frac{\pi}{4} \rho_{SiN} t_{SiN} {R_{out}}^2 \tag{2.6}$$

In this equation, ρ_{SiN} is the density of silicon nitride, 3440 kg/m^3, and t_{SiN} is the thickness of the SiN thin film. I_{mirror} is simply the sum of $I_{silicon\text{-}rim}$ and I_{SiN}. The moment of inertia of the moving combs, I_{combs}, can be calculated as follows:

$$I_{comb} = \sum_{i=1}^{N} \frac{1}{3} \rho_{si} t_c w_c \left({R_{i1}}^3 - {R_{i.0}}^3 \right) \tag{2.7}$$

Here, t_c is the thickness of the combs, w_c is the width of the combs, and N is the number of moving combs per side of the mirror plate, i.e., 22. $R_{i.1}$ is the distance between the rotational axis and the edge of the i_{th} comb and $R_{i.0}$ is between the rotational axis and the edge of the fixed comb corresponding to the i_{th} moving comb. Based on the calculated value of I, the resonant frequency in torsional mode can be extracted. This is summarized in Table 2.3. A computer simulation using a finite element method (FEM) was performed as well. Figure 2.7 shows simulation result of Rim20. The correspondence between the calculation results to the simulated values demonstrated the effectiveness of the numerical analysis.

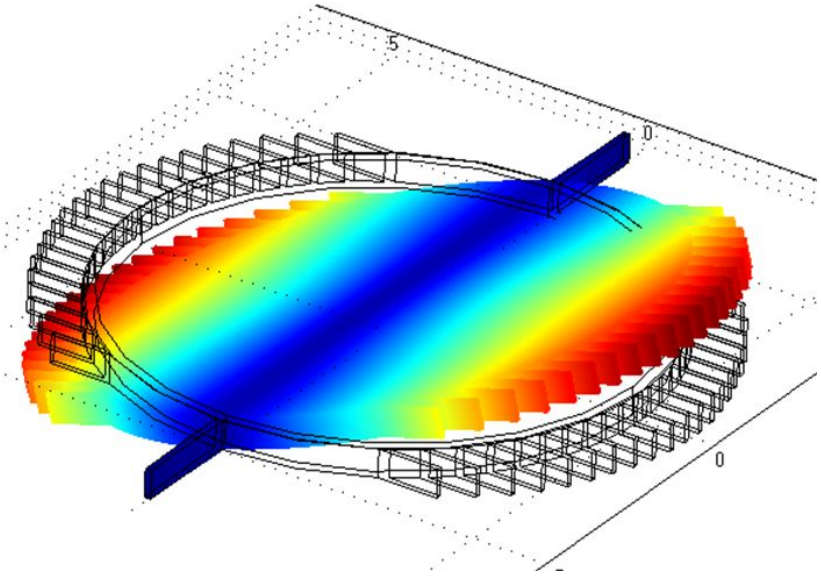


Figure 2.7 FEM simulation result

Table 2.3 Numerical analysis and simulation results

Type	**Si**	**Rim20**	**Rim50**	**Rim100**
Rim width (μm)	-	20	50	100
Calculation (kHz)	15.006	15.001	14.994	15.002
FEM simulation (kHz)	14.994	14.997	14.985	14.995

2.3.2 Static characteristics

The static characteristics are analyzed by calculating the tilt angle according to the DC driving voltage. The mechanical torque T_m generated by the tilted mirror plate to the mechanical tilt angle θ_{mech} is expressed by equation (2.8),

$$T_m = c\theta_{mech} \tag{2.8}$$

The electrical torque T_e resulting from the vertical comb actuator is derived from the variation of the coenergy stored in the capacitor which is composed of the moving comb and the fixed comb, as shown in the following equation:

$$T_e = \frac{\partial W_{coenergy}}{\partial \theta_{mech}} = \frac{\partial}{\partial \theta_{mech}}\left(\frac{1}{2}C(\theta_{mech})V^2\right) \tag{2.9}$$

In this equation, V and $C(\theta_{mech})$ are the applied voltage and the capacitance between the moving and fixed combs, respectively. Because the overlapped area between the moving and fixed combs varies as the mirror plate rotates along the tilt axis, the capacitance is a function of the tilt angle θ_{mech} via the following equation:

$$C(\theta_{mech}) = \frac{\varepsilon_0 A}{g} = \frac{\varepsilon_0}{g} \cdot 2 \sum_{i=1}^{N} \left({R_{i.1}}^2 - {R_{i.0}}^2 \right) \theta_{mech} \qquad (2.10)$$

Here, N is number of moving combs in a side of mirror plate, 22, $R_{i.1}$ is distance between rotational axis and edge of i^{th} comb and $R_{i.0}$ is between rotational axis and edge of corresponding fixed comb to i^{th} moving comb.

The mechanical tilt angle according to the applied voltage is the equilibrium condition of the electric and mechanical torque, as follows:

$$T_e = T_m \qquad (2.11)$$

Therefore, the tilt angle is derived by the following equation (2.12):

$$\theta_{mech} = \frac{1}{c} \cdot \frac{\varepsilon_0}{g} \cdot 2 \sum_{i=1}^{N} \left({R_{i1}}^2 - {R_{i.0}}^2 \right) \qquad (2.12)$$

Based on the derived equation (2.12), we plotted the tilt angle according to the driving voltage in order to compare each type. Figure 2.8 shows the calculated results

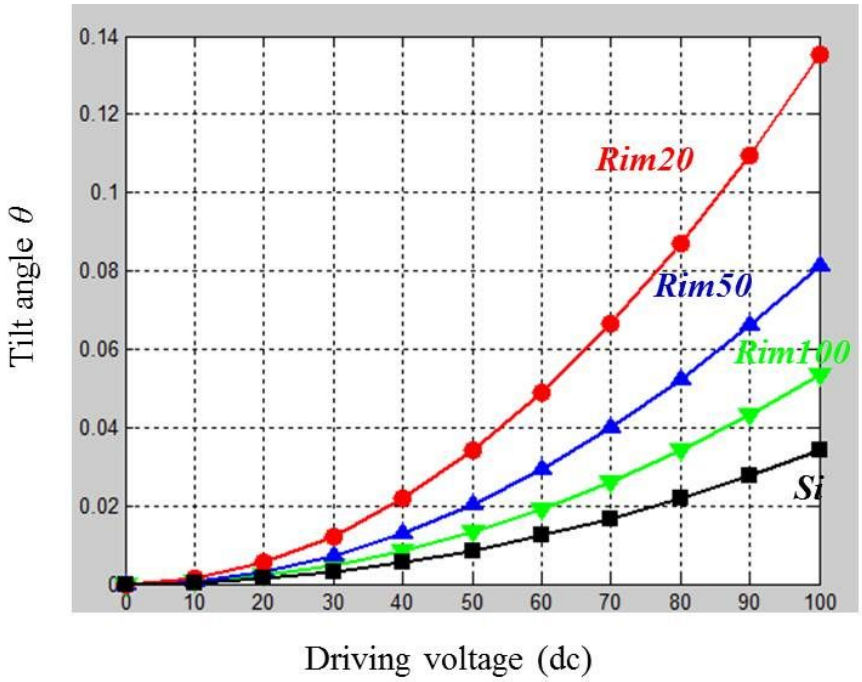


Figure 2.8. Calculated curves of the tilt angle according to the driving voltage

Although all types have the same resonant frequency, the driving voltage of Rim20 showed a decrease of approximately 52% from the conventional silicon scanner. In terms of the tilt angle, Rim20 was approximately fourfold larger than the reference at the same driving voltage, as summarized in Table 2.4.

Table 2.4. Summarized calculation results of tilt angle

Type	Si	Rim20	Rim50	Rim100
Rim width (d)	-	20 μm	50 μm	100μm
Silicon width	19.8 μm	12 μm	14.4 μm	16.8 μm
f_o	15 kHz			
Tilt angle @ 100 V_{dc}	0.035˚	0.138˚	0.083˚	0.054˚

These calculation results demonstrate the benefit of the proposed silicon nitride scanner compared to a conventional silicon scanner. In addition, Rim20 shows the most effective performance in terms of the ROC and dynamic characteristics.

2.3.3 Quality factor in vacuum condition

We numerically analyze quality factor (Q factor) of silicon nitride scanner in vacuum condition. Quality factor is ratio of stored energy to energy loss of oscillating product. Therefore, low driving voltage of scanner can be achieved by high Q factor because more electric energy supplied by voltage source transfers to oscillating microscanner with low loss of energy.

There are many types of energy loss categorized by its causes, i.e. thermoelastic damping loss, support loss, surface loss, and friction loss. Quality factor caused by each loss is denoted by Q_{TED}, Q_{sup}, Q_{surf}, and Q_{fric},

respectively. Total Q factor is expressed as following [35]:

$$\frac{1}{Q_{total}} = \frac{1}{Q_{TED}} + \frac{1}{Q_{sup}} + \frac{1}{Q_{surf}} + \frac{1}{Q_{fric}} \tag{2.13}$$

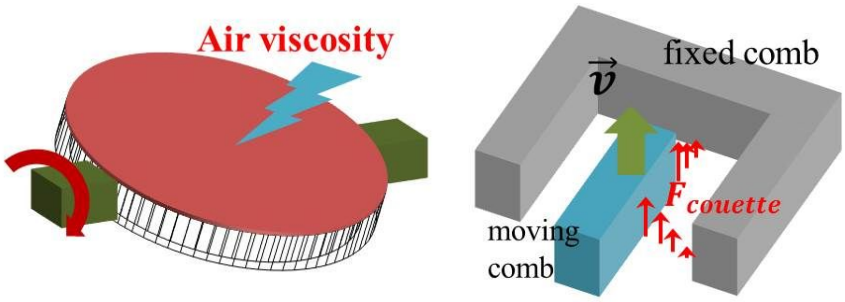
Q_{TED} is caused by heat conduction due to temperature gradients in strained and expanded region of oscillation body. Q_{sup} comes from elastic energy propagation into the surrounding support structure. Q_{surf} is generated by dissipation of acoustic wave due to crystallographic defects and surface effects. A variety of studies analyzed numerically these factors in recent years. However, reasonable model for accurate values of each factor has not been achieved yet. Moreover, these factors are minor compared to Q_{fric} in low vacuum level. Therefore, we analyzed Q_{fric} in this section.

Q_{fric} is caused by friction of gas molecules to each other and structure. As ambient pressure decreases from atmosphere, density of gas molecules shrink, loss from viscosity of gas molecules decrease and quality factor enhances. Chu et al. proposed numerical model of Q_{fric} in microscanner [36]. We applied this model to our silicon nitride scanner and achieved numerical analysis.

2.3.3.1 Q factor in low vacuum level

In low vacuum level (10^3~10^5 Pa) [37], mean free path of gas molecules is small than typical dimension of structure. Therefore, viscosity of gas

molecules is dominant factor causing fraction loss. Energy loss from viscosity occurs in mirror plate and gap between moving and fixed comb, which is denoted by L_{plate} and L_{comb}, respectively (Figure 2.9(a)). We analyze these losses in the following.



(a) (b)

Figure 2.9. Energy loss due to viscous flow of gas molecule in (a) mirror plate and (b) combs in low vacuum level

2.3.3.1.1 Loss in mirror plate

The energy loss due to viscosity of gas molecules is express as following [38]:

$$L_{vis} = 2A\left(\frac{\omega\rho\eta}{2}\right)^{1/2}\langle\overline{v^2}\rangle \tag{2.14}$$

where A is damped area, and ρ is air density (=1.1839P/P_0 kg/m^3 at room temperature, P_0 is atmosphere), and η is dynamic viscosity of air

($18.714\times 10^{-6}\, N\cdot s\cdot m^{-2}$), and v is the velocity of an oscillating object. In order to calculate mean square of v, we expressed v with terms in Figure 2.10.

$$\mathrm{H} = H_0\sin(2\pi ft) \cong y\theta_0\sin(2\pi ft) \tag{2.15}$$

$$\mathrm{v(t)} = \frac{dH}{dt} = 2\pi f\theta_0 y\cos(2\pi ft) \tag{2.16}$$

Because $y = R\sin\phi$, $v(t)$ can be expressed as following:

$$\mathrm{v(t)} = 2\pi f\,\theta_0 R\sin\phi\cos(2\pi ft) \tag{2.17}$$

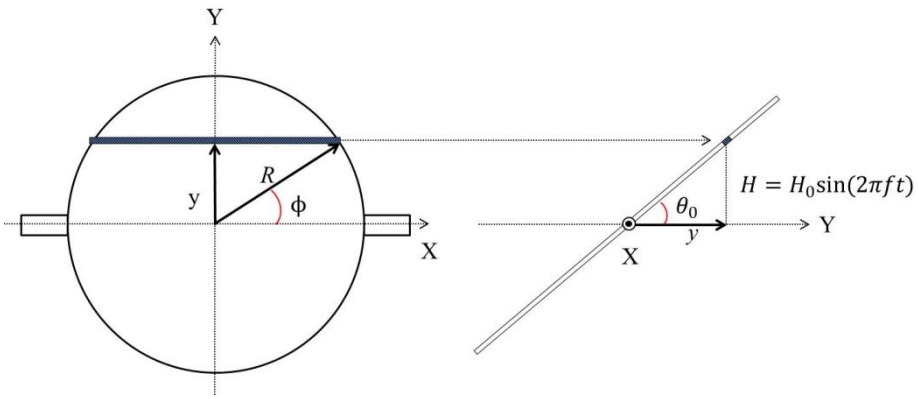


Figure 2.10. Illustration of microscanner for calculation of energy loss in mirror plate

Therefore, loss in mirror plate is calculated neglecting loss in side wall of mirror plate as following:

$$L_{plate} = 2\left(\frac{\omega\rho\eta}{2}\right)^{\frac{1}{2}}\cdot 2\int_0^T\int_0^R 2\sqrt{R^2-y^2}\,dy v^2(t)dt$$

$$= \pi^3 f R^4 {\theta_0}^2 \left(\frac{\omega\rho\eta}{2}\right)^{\frac{1}{2}} \quad (2.18)$$

where T is period time of oscillating object.

2.3.3.1.2 Loss in comb fingers

Energy loss in comb fingers is led by slide film damping between fixed and moving combs. Viscous flow of gas molecules in adjacent combs can be assumed as Coutte flow as Figure 2.9(b). Forced by Coutte flow can be express as following [39]:

$$\vec{F}_{Cout} = -\eta_{eff}\frac{2h\Delta l}{g}\vec{v} \quad (2.19)$$

where $h\triangle l$ is interaction area between combs and g is gap of combs and η_{eff} is effective dynamic viscosity of air ($=\eta/(1+9.658K_n^{1.159})$ [40]). K_n is Knudsen number denoted as following equation:

$$K_n = \frac{K_B T}{\sqrt{2}\pi\sigma^2 pL} \quad (2.20)$$

where K_B is Boltzman's constant (1.38×10-23 kg·m^2/s^2·K), T is is absolute temperature or thermodynamic temperature (300K at room temperature), σ is

particle shell diameter (1.42×10^{-9} m in N_2 molecule), P is ambient pressure, and L is representative physical length scale (25 μm in our model).

Loss in comb fingers, L_{comb}, can be calculated as following:

$$L_{comb} = \int P \cdot v dt = \sum_{i=1}^{N} \int_{o}^{T} \vec{F}_{Cout.i} \cdot \vec{v_i} dt \tag{2.21}$$

$$= \frac{4\pi^2 h_c {\theta_0}^2 \eta_{eff}}{3g} \sum_{i=1}^{N} \left\{ (l_{o.i} + l_c)^3 - {l_{o.i}}^3 \right\} \tag{2.22}$$

where N is the number of combs and h_c is height of comb fingers. $l_{o.i}$ is distance of outer edge of i_{th} fixed comb from rotational axis, and l_c is interaction length between two combs (100 μm).

Because Q_{fric} is ratio of stored energy to energy loss, it can be expressed as following

$$Q_{fric} = \frac{2\pi E_{st}}{L_{plate} + L_{comb}} \tag{2.23}$$

where stored energy $E_{st} = \frac{1}{2} I [\theta]^2_{max} = \frac{1}{2} I {\theta_0}^2 \omega^2$

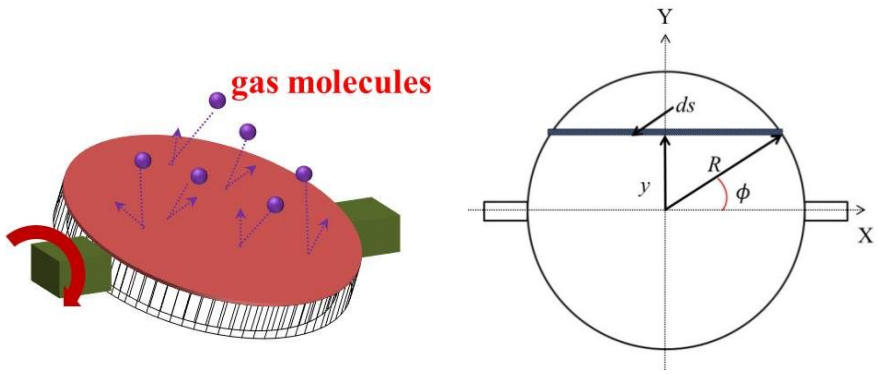
Therefore, Q_{fric} can be calculated as following:

$$Q_{fric} = \frac{4fI}{R^4 \left(\frac{\omega \rho \eta}{2}\right)^{1/2} + \frac{4h\eta_{eff}}{3\pi g} \sum_{i=1}^{N} \left\{ (l_{0.i} + l_c)^3 - {l_{0.i}}^3 \right\}} \tag{2.24}$$

2.3.3.2 Q factor in high vacuum level

In high vacuum level (<1000 Pa [37]), mean free path is larger than typical dimension of structure. Therefore, friction loss by collision of gas molecules to moving structure becomes dominant factor. There are two types of friction loss, i.e. loss in mirror plate and loss in comb fingers. Loss in mirror plate and comb fingers is generated by difference pressure between front and back side of moving structure resulting in damping torque of T_{plate} and T_{comb}, respectively.

2.3.3.2.1 Damping torque in mirror plate



(a) (b)

Figure 2.11. Illustration of SiN mirror plate for calculation of damping torque

When the device moves, pressure difference $\triangle P$ generates between front and back side, and can be expressed as following equation [37, 41]:

$$\Delta P(y) = \frac{Py\dot{\theta}}{c}\left[(2-\sigma_n)\cdot\left(\frac{2}{\sqrt{\pi}}+1\right)+\sigma_n\sqrt{\frac{\pi T_W}{T_i}}\right] \quad (2.25)$$

where P is ambient pressure, $\dot{\theta}$ is angular velocity of moving structure, c is thermal velocity of the gas molecules ($c = \sqrt{2K_BT_i/m}$, m: mass of gas molecule($7 \times 10^{-3}/6.02 \times 10^{-23}$ kg for N_2 gas molecule), σ_n is normal accommodation coefficient, σ_t is tangential accommodation coefficient, T_i is ambient temperature, T_w is wall temperature, and K_B is Boltzman's coefficient. Based on Figure 2.11, torque due to pressure difference can be calculated in condition of isothermal system (T_i=T_w) and full momentum accommodation ($\sigma_n = \sigma_t = 1$) neglecting difference pressure generated on sidewall of mirror plate as following:

$$T_{plate} = \int r\cdot dF = \int y\cdot ds = 2\int_0^R y\cdot\left[\Delta P(y)\times 2\sqrt{R^2-y^2}\right]dy$$

$$= \left(\frac{m}{2K_BT_i}\right)^{1/2}\dot{\theta}\frac{\sqrt{\pi}R^4P}{4}\left(2+\sqrt{\pi}+\pi\right) \quad (2.26)$$

2.3.3.2.2 Damping torque in comb fingers

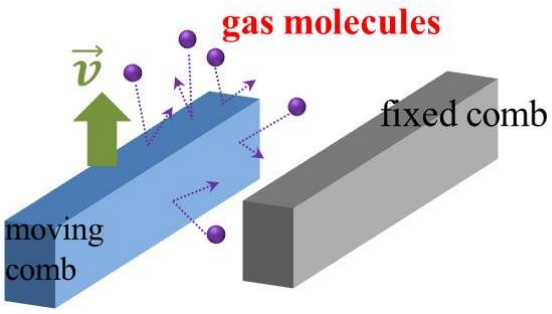


Figure 2.12. Illustration of comb fingers for calculation of damping torque

Pressure difference in moving combs generates shear stress and causes damping torque T_{comb} (Figure 2.12). Shear stress along front edge (τ_{fe}) and side edge (τ_{se}) in i_{th} moving comb is expressed as following equation [37]:

$$\tau_{fe.i} = \frac{\sigma_t P (l_{o.i}+l_c)\dot{\theta}}{c\sqrt{\pi}} \tag{2.27}$$

$$\tau_{se.i} = \frac{\sigma_t P y\dot{\theta}}{c\sqrt{\pi}} \tag{2.28}$$

Therefore, damping torque T_{comb} generated by pressure difference can be calculated as following:

$$T_{comb} = \sum_{i=1}^{N} w_c \cdot h_c \cdot (l_{o.i} + l_c)\tau_{fe.i} + 2h \sum_{i=1}^{N} \int_{l_{o.i}}^{l_{o.i}+l_c} \tau_{se.i} \cdot y dy$$

$$= \frac{h_c \sigma_t p \dot{\theta}}{c\sqrt{\pi}} \sum_{i=1}^{N} \left\{ w_c (l_{o.i} + l_c)^2 + \frac{2}{3} \left[(l_{o.i} + l_c)^3 - l_{o.i}{}^3 \right] \right\} \quad (2.29)$$

where w_c is width of comb finguer, and h_c is height of comb fingers.

Based on calculation results, Q_{fric} can be simply extracted using following equation:

$$T_{total} = T_{plate} + T_{comb} = G \cdot \dot{\theta} \quad (2.30)$$

$$Q_{fric} = \frac{wI}{G} \quad (2.31)$$

where I is momentum of inertia of scanner ($1.6236 \times 10\text{-}15$ kg·m^2) in this work.

2.3.3.3 Results

We calculated Q factor according to ambient pressure using analytical model analyzed in previous section. Figure 2.13 shows calculation result.

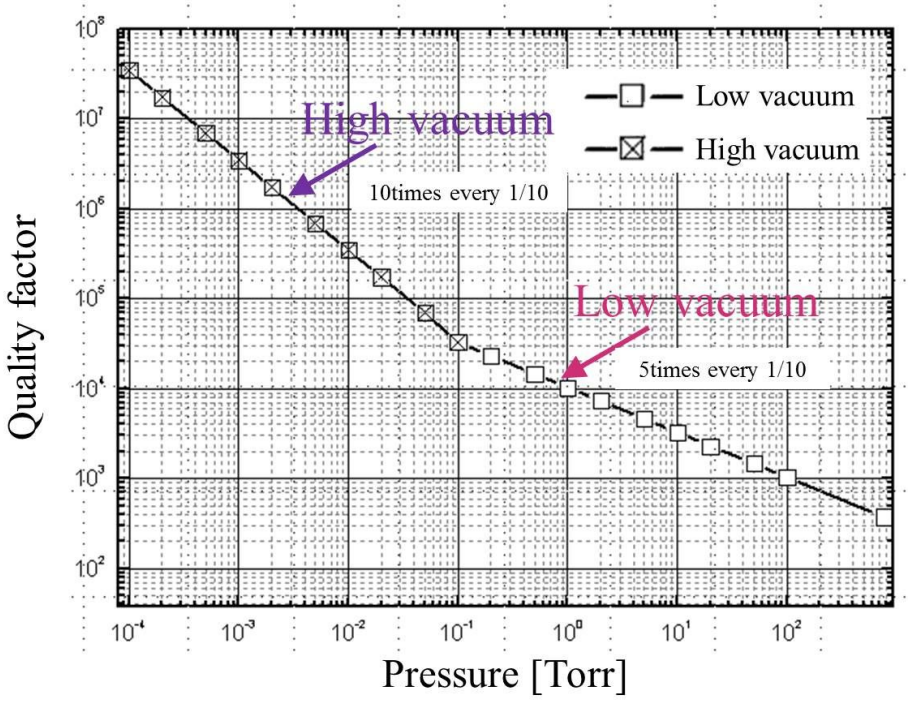


Figure 2.13. Calculated Q factor according to ambient pressure based on numerical analyzed model.

2.4 Conclusion

We proposed a silicon-rim-reinforced silicon nitride scanner with a vertical comb to achieve a large dynamic range while also ensuring the flatness of the silicon nitride microscanner. Moreover, wafer-level vacuum packaging was introduced in order to decrease driving voltage additionally. Numerical analysis of spring constant and moment of inertia was shown. Calculated resonant frequency which corresponded with FEM simulation verified effectiveness of numerical analysis. Moreover, FEM simulation showed large ROC of more than 800 mm of silicon-rim-reinforced SiN scanner. In addition, calculation results of optical tilt angle showed proposed SiN scanner reduced driving voltage to 51% in maximum compared with conventional silicon scanner. Behavior of SiN scanner in vacuum condition was successfully analyzed by calculation of quality factor according to ambient pressure.

Chapter 3

Fabrication of SiN scanner and vacuum packaging

This chapter contains fabrication process and fabrication results of SiN scanner wafer-level vacuum packaging dealt in previous chapter. SiN mirror plate can be formed easily due to etching selectivity to silicon. SiN thin film takes role as mirror plate as well as etching stop layer. Vacuum packaging enable the microscanner to be tilted maximum angle in low driving voltage. Wafer-level process of vacuum packaging provides batch fabrication resulted in low manufacturing cost. Fabrication process of vacuum packaged microscanner using a glass cap and a Through-Wafer Interconnection (TWIn) substrate are mentioned.

3.1 Introduction

In previous chapter, we proposed and numerically demonstrated silicon nitride scanner with silicon rim and wafer-level packaging for low driving voltage in high frequency. Dynamic and static characteristics were analyzed. This chapter proposes fabrication process of proposed SiN scanner and wafer-

level vacuum packaging. Section 3.2 deals with fabrication process and results of silicon-rim-reinforced SiN scanner with vertical comb actuator. Section 3.3 shows packaging technique using the glass cap. Section 3.4 deals with wafer-level vacuum packaging with TWIn substrate. Conclusion is dealt in Section 3.5.

3.2 SiN scanner with silicon rim and vertical comb

This section deals with fabrication process for realizing proposed silicon nitride scanner. The abbreviated schematic of process is illustrated in Figure 3.1. Detail techniques and issues are described in following sub-section.

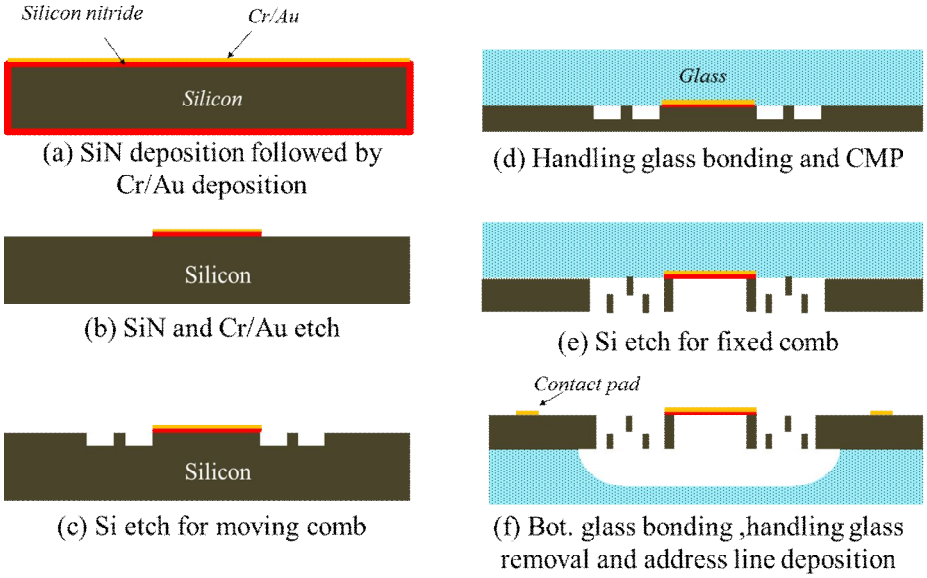


Figure 3.1. Fabrication process of silicon-rim-reinforced SiN scanner

3.2.1 Silicon nitride mirror plate and vertical comb actuator

Fabrication started with deposition of silicon nitride film on single-crystal silicon wafer. LPCVD deposited optically smooth film. Extra high residual stress several deteriorated flatness of thin film, low stress silicon nitride film

was required. High temperature LPCVD at 825℃ produced low stress silicon nitride film of 30 MPa. Ambient pressure was 180 mTorr and gas flow rate of dichlorosilane and ammonia was 51 and 8.5 sccm, respectively. Sputtering of chrome (Cr) and gold(Au) then followed as reflective surface. In order to minimize effect of residual stress of this layer to thin film flatness, thickness was thin to 10 nm of Cr and 40 nm of Au.

Standard photolithography patterned circular mirror plate using positive photoresist AZ4330. Cr/Au film and silicon nitride film were etched with etching mask of photoresist. SPM cleaning for stripping the photoresist was then followed by photolithography for patterning AZ4330 into moving comb configuration. Silicon was anisotropically dry-etched to depth of 25 μm. After removal of photoresist by SPM cleaning, borosilicate glass was anodically bonded to the silicon wafer. Borosilicate glass was used as handing layer in order to manipulate 50 μm-thick silicon layer after chemical-mechanical polishing (CMP). After bonding step, silicon wafer was leveled to thickness of 50 μm for defining thickness of silicon rim and springs.

Double etch-masking layer fabricated vertical comb actuator and silicon rim on silicon device layer. Cr coated to thickness of 30 nm, and was followed by photolithography and wet etching for pattering it into torsional spring, silicon rim and fixed combs. SPM cleaning was then followed by photolithography for moving combs using AZ4330. After thermal curing, silicon was dry-etched to depth of 50 μm and microscanner was released. Removal of photoresist by

AZ700 stripper was followed by additional dry etching of silicon to 25 μm depth. This etching defined thickness of moving combs. Cr etch mask was removed by wet-etching.

3.2.2 Deep-cavity-integrated bottom glass

Bottom glass took a roll as not only supporting substrate but also providing movement space of microscanner. Therefore, deep cavity of more than 200 μm was required for mechanical tilt angle of more than 20°. The wet etching has been widely used for the fabrication of deep cavity due to high etch rate, smoothness of etched surface, and simple fabrication. However, deep etching requires longer etching times, which leads to the generation of pits on a glass wafer due to HF diffusion through the etch mask. A variety of studies have been published to prevent HF diffusion and ensure long-etching times of glass wafers. Table 3.1 summaries reported studies on wet etching techniques.

Table 3.1. Wet etching techniques of glass wafer

Etch mask		Mask thickness	Max. depth or time	HF %	Ref.
Photoresist	Microposit	2 μm	50 μm	49 wt%	[42]
	ProTEK PSA	n/a	>15 hr	49 wt%	[43]
Silicon	Single crystal silicon	500 μm	Unlimited	49 wt%	[44]
	Polishied poly-Si + SU-8	1.5 μm + 50 μm	320 μm	48 wt%	[42]
	Amorphous Si + SiC + AZ7220	n/a	> 170 min	49 wt%	[45]
Molybden	Molybden + SPR220-7	n/a	3.5 hr	25 wt%	[46]
Cr/Au	Cr/Au+AZ7220	1 μm + 2 μm	85 min	49 wt%	[47]
	Cr/Au/Cr/Au + SPR220-7	0.92 μm + 20 μm	>38 min	49 wt%	[48]

A variety of studies have been published to prevent HF diffusion and ensure long-etching times of glass wafers. A variety of materials for etching masks have been investigated as well. A photoresist (PR) is a commonly used material in the wet etching process. However, HF easily penetrates into and peels off a PR, which results in an etching depth of 50 μm or less [42]. Nagarah et al. [43] reported a HF-resistant photosensitive resist as mask, and successfully wet-etched fused silica for 15 hr in 49 wt% HF. This was cheapest and simplest technique for deep wet-etching of glass to date. However, the undercut was severe and an alkali-protective resist was not

easily removed in acetone. Silicon is also widely used in etching masks for glass wafers due to the inert characteristic when used with HF. Corman et al. [44] obtained depths of 500 μm or more on the borosilicate glass in 49 wt% HF using single-crystal-silicon. Good mask was kept without pits after glass wet etching. However, many processing steps including anodic bonding, chemical-mechanical polishing, and KOH etching were needed. Moreover, this technique was not available to fused silica which cannot be anodically bonded to silicon due to lack of movable sodium ions. Bien et al. [42] reported polished polysilicon in combination with a SU-8 photoresist and etched an aluminosilicate glass wafer up to 320 μm deep. Iliescu et al. [49] also reported that the annealing of PECVD amorphous silicon reduced the residual stress and obtained a maximum etching depth of 300 μm with a 2-μm thick photoresist in a Pyrex glass wafer. These methods successfully demonstrated deep wet-etching of glass wafer by blocking generation of pits caused by surface spike on polysilicon and breakages of amorphous silicon due to residual stress. Compared to technique using anodically bonded single-crystal silicon, these techniques required simple process and were able to be applied to fused silica which was not anodically bondable to silicon. However, the maximum etching time of less than 40 min in 49 wt% HF was not sufficient. In addition, many process steps such as the polishing and the annealing at 400 ˚C were still required. A new material, molybdenum, was also introduced by Ceyssens et al. [46]. Molybdenum (Mo) can be simply

deposited by evaporator and patterned using etchants. Mo mask in combination with SPR220-7 achieved etch depth of 1.2 mm without pinholes in borosilicate glass. However, the maximum etching time was only 3.5 hr at a low concentration of 25 wt% HF, which was not sufficient to etch fused silica deeply.

Cr/Au is also a commonly used masking material due to the inert property of gold when in contact with HF. However, because Cr/Au is hydrophilic, HF can easily penetrate it and attack the surface of the glass wafer [50]. Micro-creep generated after the Cr/Au deposition process also causes pits on the glass surface [47]. Many techniques have been reported in an effort to resolve these factors and increase the etching depth. Nagarah et al. [43] used the alkali-protective resist on Cr/Au mask for the purpose of blocking penetration of HF solution. Although pits were not occurred for 3 hr in 49 wt% HF, the alkali-protective resist was difficult to be removed in acetone. Iliescu et al. [47] increased the thickness of gold to 1 μm using three successive depositions in order to remove micro-creep on Cr/Au masks. However, a 1-μm thick Cr/Au film with an A7220 PR resisted 49 wt% HF only for approximately 85 min. The complicated and expensive process also limits the usefulness of this technique. Although Bu et al. [48] reported that a 0.92-μm thick Cr/Au/Cr/Au layer with a 20-μm thick photoresist resisted for 38 min in 49 wt% HF without pits, the fabrication process is complicated for the masking metal to be deposited and patterned. In addition, the etching time was

not sufficient.

This research demonstrates 430-nm thick Cr/Au film in combination with a commonly used positive photoresist, 5.2-μm thick AZ4330, resists 49 wt% HF for 20 hr or more during the glass wet etching process. The AZ4330 photoresist is widely used as a wet and dry etch mask [51], a electroplating mold [52], and as a lift-off sacrificial layer [53].

We hypothesized that HF diffusion was the dominant reason, and the hydrophobicity of the dehydrated PR could prevent outcomes effectively. Through the thermal curing at a high temperature, dehydration and cross-linking arose and the hydrophilicity of the PR decreased significantly [54, 55]. Instead of thick Au film, the cured PR was expected to prevent the creation of pits effectively.

In order to demonstrate this hypothesis, we experimented with glass etching using Cr/Au film with cured AZ4330. The borosilicate glass wafer was cleaned via a standard process (SPM cleaning, H_2SO_4/H_2O=4/1). Cr/Au film was deposited on the top side of the glass wafer in the sputter device (Figure 3.2(a)). Standard photolithography was used to pattern the AZ4330 into a circle window 300 μm in diameter (Figure 3.2 (b)). After the thermal curing of the AZ4330, the Cr/Au film was etched. This was followed with the wet etching of the glass wafer in 49 wt% HF for 60 min at room temperature (Figure 3.2 (c)). The photoresist was then removed by SPM cleaning for 10 min. Finally, Cr/Au was stripped by means of wet etching (Figure 3.2 (d)).

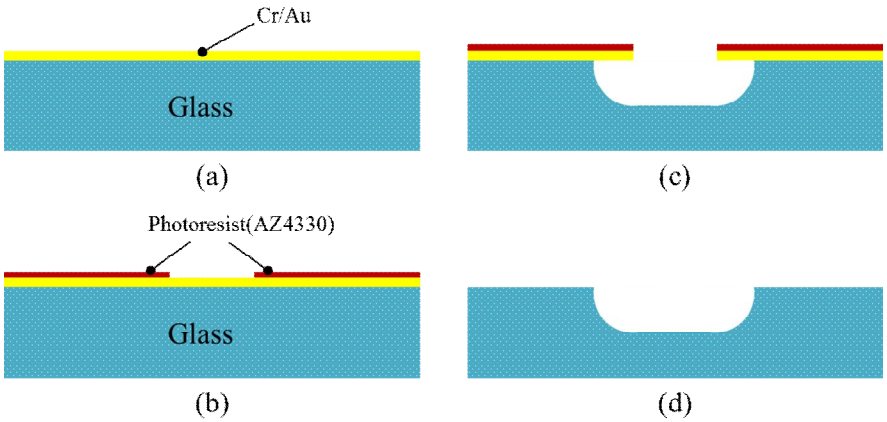
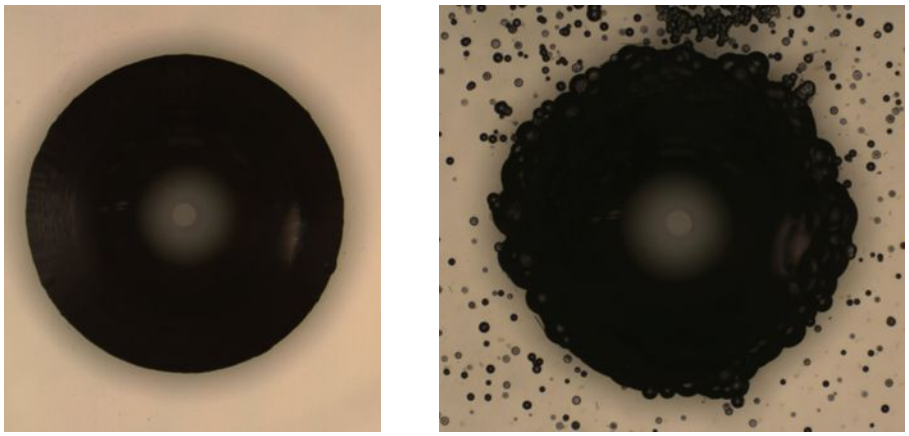


Figure 3.2. Micromachining procedure of the experiment.

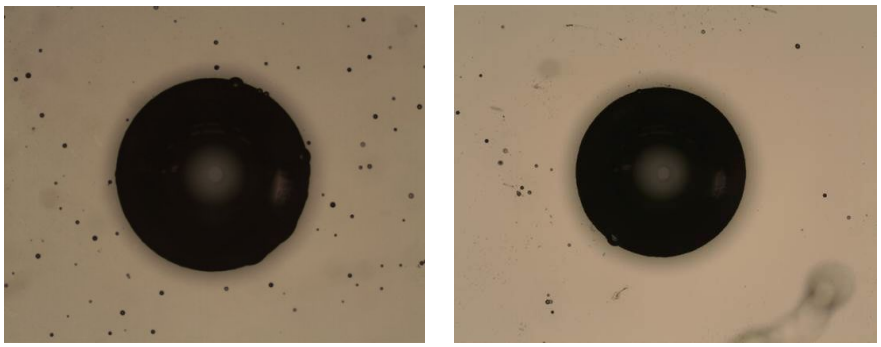
The fabrication results showed that no pits created on the glass wafer and that the circle window was not distorted at all (Figure 3.3(a)). However, in the case of glass wet etching without the PR removed by an acetone solution before being dipped into HF, several pits were generated and the circle window was severely distorted (Figure 3.3(b)). These results demonstrated that the PR blocked the diffusion of HF through the Cr/Au mask and prevented the development of pits. The etching depths of the glass wafers with and without the PR were 388.3 μm and 390.6 μm, respectively. The surface roughness values of the etched cavity with and without the PR were 94.4 and 98.6 Å, respectively. These results showed that the generation of pits did not affect the etching rate or the surface roughness.



(a) (b)

Figure 3.3. Fabrication results of wet etching of the borosilicate glass wafer (a) with the cured AZ4330 plus Cr/Au mask, and (b) with only Cr/Au mask.

We also verified the effect of the thermal curing process against HF diffusion and the creation of pits. Figure 3.4(a) shows the experimental result without the curing process of the PR. Although the number of pits was significantly decreased, many pits were generated on the glass wafer. These findings indicated that curing of the PR caused dehydration and decreased the HF penetrability of the PR. The dehydration of the PR is addressed in the next section. Interestingly, when the PR was cured after Cr/Au wet etching, pits were also created, although the number of pits was lower than that on a glass wafer with uncured PR (Figure 3.4(b)). This showed that the generation of pits was also caused by the diffusion of hydrophilic Cr/Au etchants through the PR and that the cured PR prevented the diffusion of not only the HF solution but also the Cr/Au etchants.



(a) (b)

Figure 3.4. The effect of curing of the PR: Fabrication results of glass wet etching (a) without curing, and (b) with curing only after Cr/Au etching.

The number of pits per square millimeter is shown in Figure 3.5. The averages were 114.7, 14.8, and 5.9 for Cr/Au only, uncured PR, and cured PR cases after Cr/Au etching, respectively. These findings indicate that 95.1% of the pits were generated from HF diffusion through Cr/Au mask, while 4.9% were generated from pinholes on the Cr/Au mask formed by the diffusion of Cr/Au etchants during the Cr/Au wet etching process. In addition, of the created pits, 87.7% were blocked by uncured AZ4330; the rest (12.3 %) were blocked by the curing process.

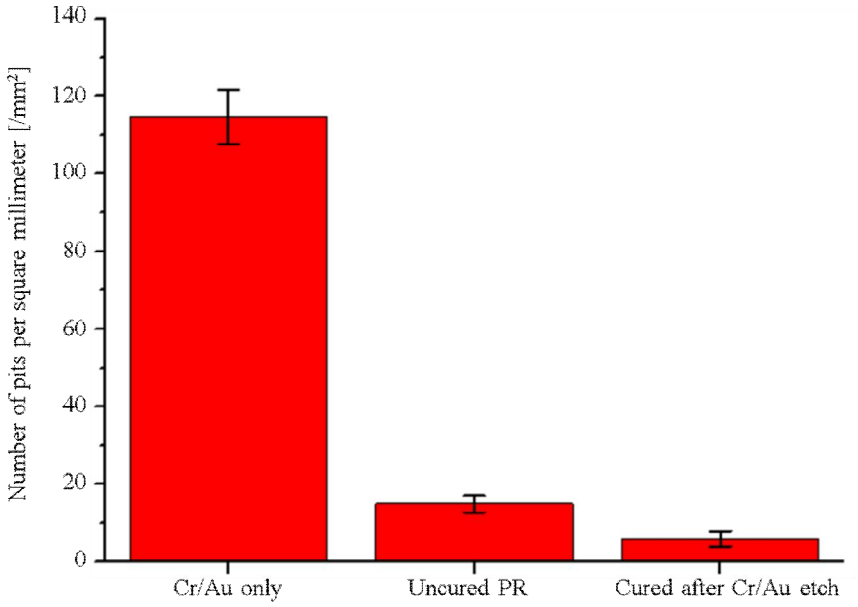


Figure 3.5. Number of pits per square millimeter according to different etching masks.

The effect of the curing process on the properties of the PR was analyzed and optimization was done. Factors that may affect the curing of the PR were the curing time, the temperature, and the thickness of the PR. We investigated the effect of each factor in our optimization of the curing process.

Previous results showed PR cured at 110℃ for 20 min effectively prevents the diffusion of HF solution and Cr/Au etchants and consequently blocks the generation of pits on a glass wafer. Firstly, we investigate that how much the curing time at 110℃ affects the PR and the creation of pits. Figure 3.6 shows the number of pits per square millimeter according to the curing time in 49 wt% HF. As the curing time increased, the number of pits decreased

exponentially. Compared to uncured PR, 5 min of curing time removed 36% of the pits, 10 min removed 77%, and 15min removed 86%. No pits were found when the curing time exceeded 20 min.

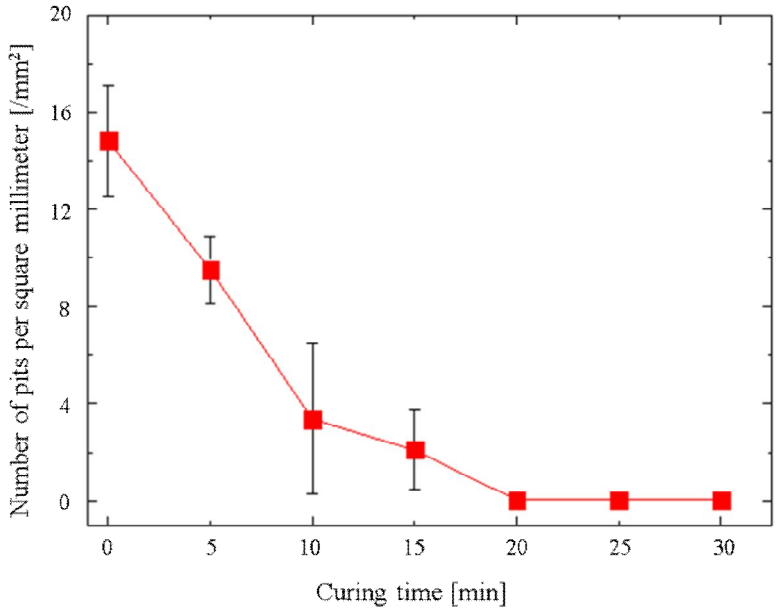


Figure 3.6. The number of generated pits in different curing time at 110 ˚C.

These results suggest that the curing process transformed the property of the PR from hydrophilic to hydrophobic, and blocked the diffusion of the hydrophilic HF solution and the Cr/Au etchants. Baking of the PR at a high temperature was reported to trigger the cross-linking of the carboxyl group, cause dehydration, and increase the hydrophobicity of the PR dramatically [54, 55]. The hydrophobic cured PR appeared to block the diffusion of HF and of the Cr and Au etchants effectively.

To verify the increase in the hydrophobicity of the PR, we measured the amount of hydroxides of the PR using a Raman spectrometer. Figure 3.7 shows the Raman intensity at a wavenumber range of 100 to 3500 cm^{-1} according to the increase in the curing time. As the curing time increased, the intensity in range of the hydroxide (3000-3500 cm^{-1}) decreased. These findings suggest that the hydrophobicity increased due to the removal of the hydroxide with the increase of the curing time. In addition, a recognizable decrease in the intensity of the curing time at more than 20 min was not found, implying that the hydrophobicity did not meaningfully change when the curing time was 20 min or more. These results are in agreement with the experiment results in which the number of pits at a curing time of 20 min was identical to that at 25 min and at 30 min.

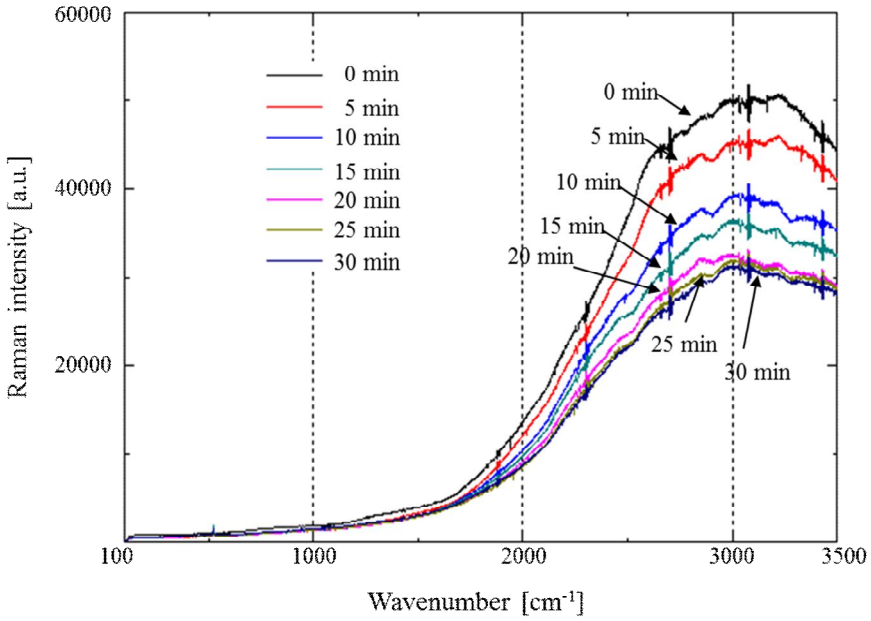


Figure 3.7. Raman intensity of the cured PR in baking time of 0- 30 min.

One interesting finding was that the intensity of another wavenumber range also decreased with an increase of the curing time. This may have occurred because the hydroxyl group existed in the form of various compound with carbon in the PR such as the carboxylic acid, and because the dehydration led to a decrease of the intensity in the other ranges, resulting in broad spectral lines.

We investigated the effect of the curing temperature on the hydrophobicity of the PR. Curing temperatures of 70, 90, 110, 130 and 150℃ for 20 min were used to bake the PR. Then, the etching of a Cr/Au mask and a glass wafer followed. Figure 3.8 shows the measurement results. The average number of pits at 70℃ was 15.3 /mm^3, which is similar to the result with uncured PR

(14.8 /mm^3). Pits were decreased at 90℃ and were not found at 110℃ or more. These findings indicate that the curing process at 110℃ for 20 min was sufficient to remove the pits.

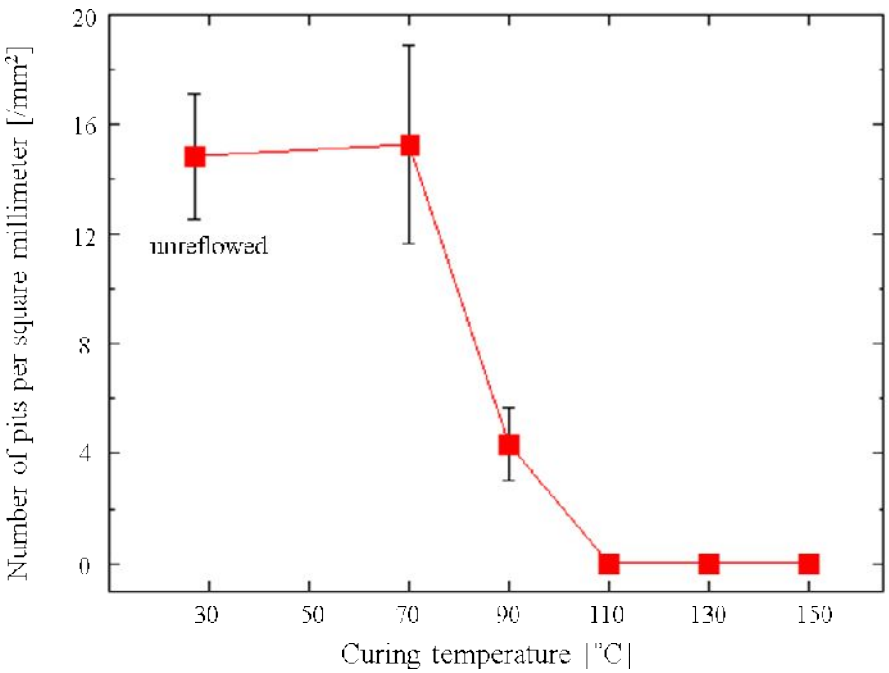


Figure 3.8. Number of pits according to the curing temperature for 20 min.

We used a Raman spectrometer to investigate the dehydration of the PR as the temperature increases. The measurement results (Figure 3.9) showed that the hydroxide was reduced as the temperature increased. Interestingly, the Raman intensity of the PR cured at 130℃ was lower than that of 110℃ and similar to that of 150℃ despite the fact that the number of pits remained the same. These finding suggest that although the hydrophobicity of the PR cured

at 110℃ was less than that at 130℃ and 150℃, it was enough to block the diffusion of the solutions, including HF and the Cr/Au etchant.

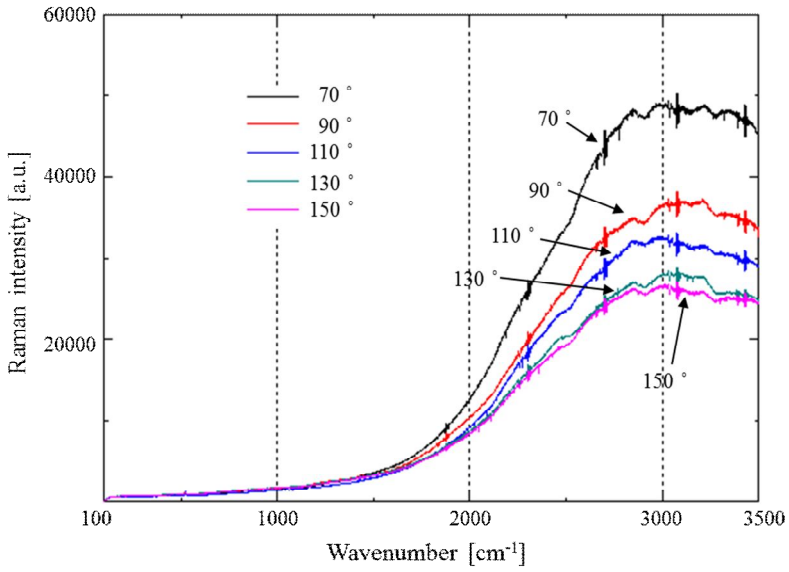


Figure 3.9. Raman spectrum of the cured PR in curing temperature of 70-150 ˚C for 20 min.

We also considered the thickness of the PR as a possible factor behind the creation of the pits, and we investigated this with different PR thicknesses. The thickness was controlled by the rotational speed during the coating of the PR. The PR was coated at speeds of 4000, 3000, 2000, and 1000 rpm, and the thickness of the PR was 3.0, 3.5 5.2, and 7.1 μm, respectively. Standard photolithography then followed with a curing process at 110℃ for 20 min. After Cr/Au wet etching, the glass wafer was etched in 49 wt% HF for 60 min.

The number of pits in each case is illustrated in Figure 3.10. At a thickness of 3.5 μm or less, pits were generated despite of the curing of the PR. This suggests that the surface of the cured PR was not the main barrier preventing solution diffusion and that the thickness of the dehydrated PR was an influential factor.

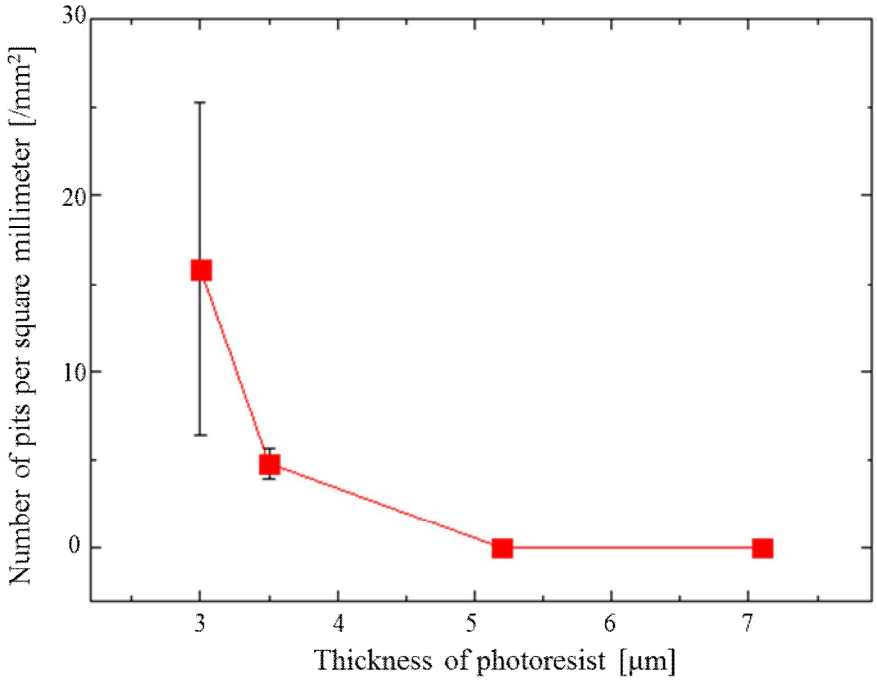


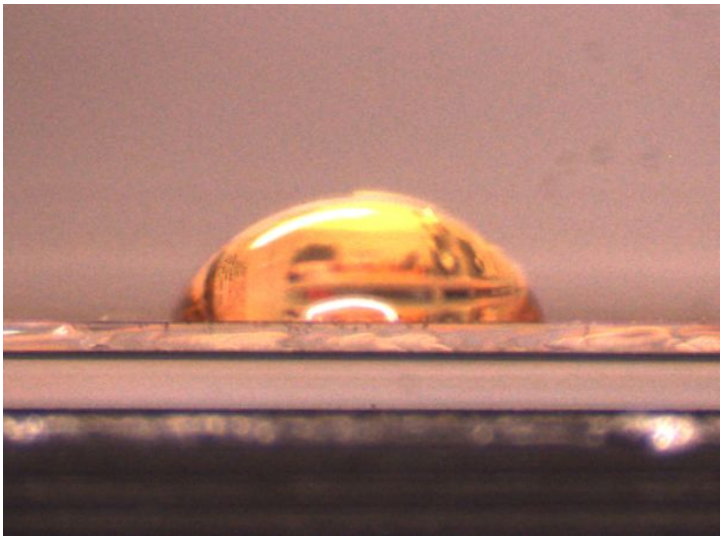
Figure 3.10. Number of pits according to thickness of photoresist in wet etching of borosilicate glass for 60 min using 49 wt% HF

d. Fabrication of deep cavity

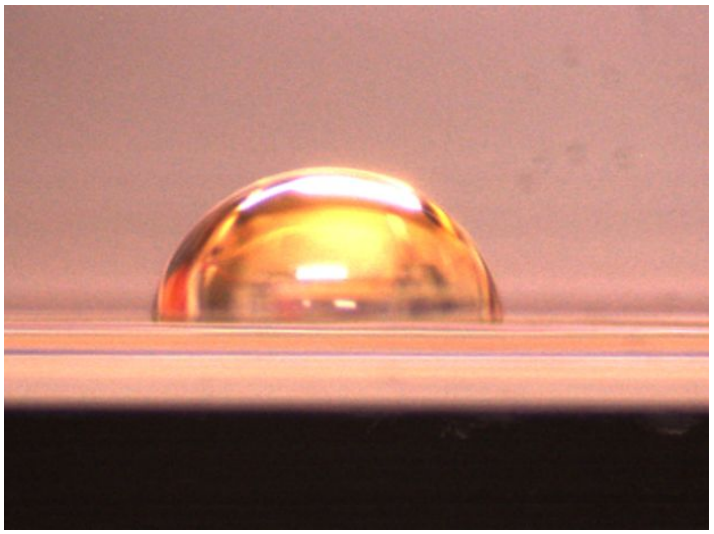
We investigated the effects of the curing time, curing temperature, and thickness of the PR. Considering the minimum process time, a low

deterioration of etching masks, and a thin thickness of the PR, we designated a curing process with the parameters of 130℃, 20 min, and a 5.2-μm thick PR layer as the optimized conditions for the fabrication of a diffusion barrier against the HF solution and Cr/Au etchants. Although the curing process at higher temperature for longer time was expected to dehydrate the PR more, it can cause the deterioration of Cr/Au mask by the diffusion of Au into Cr [56].

Curing process with the parameters of 130℃, 20 min, and a 5.2-μm thick PR layer was expected to dehydrate AZ4330 and prevent diffusion of HF and Cr/Au etchants. In order to verify the dehydration and hydrophobicity of AZ4330, we measured contact angle (CA) before and after curing process using sessile drop method with droplet of 4 μl. Figure 3.11 shows measurement results. Contact angle increased from 66 ° to 85 °, and demonstrated that AZ4330 was dehydrated by curing process.



(a)



(b)

Figure 3.11. Contact angle (a) before (66 ˚) and (b) after (85 ˚) curing process of AZ4330 which was coated on Cr/Au film

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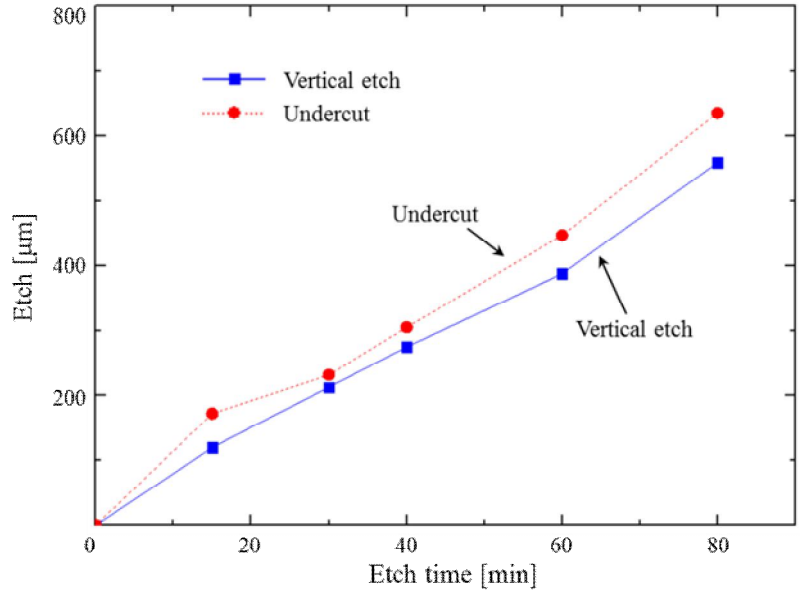
Investigation of effect of thickness of AZ4330 and curing process on wet etching was performed. However those terms may not be all of possible

factors. Because AZ4330 has been a reliable material for etching mask in our research group, AZ4330 was used as protective photoresist in this work. However, because there was a variety of useful positive, further investigation was needed. In addition, thickness of Cr/Au mask can be factors which affect occurrence of pits. We found that wet etching using Cr/Au mask of 20 nm/200 nm thickness generated pits in 49 wt% HF for 60 min of etching time even with optimized curing process. This result suggested that thickness of metal film can be meaningful factor. Investigation on these factors may be dealt in ongoing work.

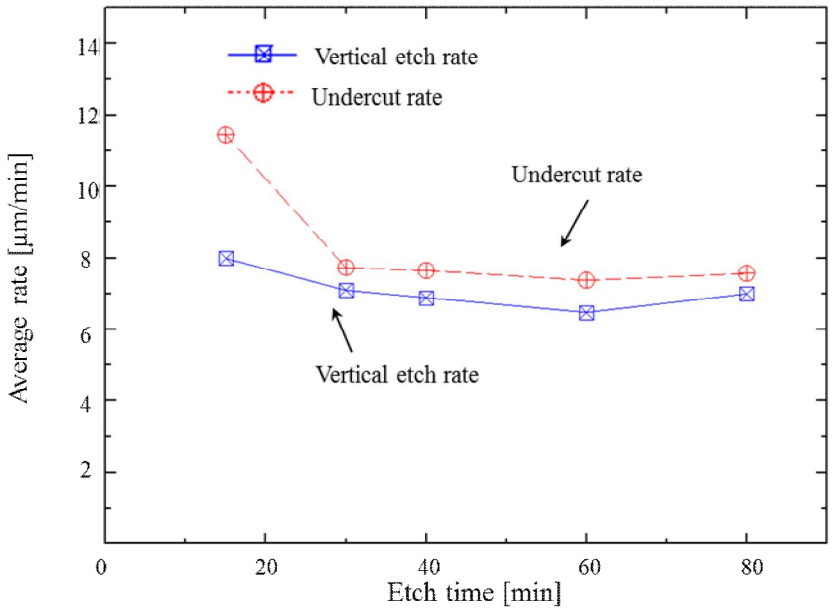
Meanwhile, although experiment results showed that curing process of AZ4330 with Cr/Au eliminated generation of pits in wet etching for 60 min in 49 wt% HF, hydrophobicity of photoresist may not be the main reason of pits removal. It was possible that cured resist reflowed into micro cracks on Au surface because Iliescu et al. [47] demonstrated that micro-creep generated during deposition can cause pits. This argument was persuasive based on the fact that AZ4330 alone was peeled off from glass surface and cannot withstand 49 wt% HF. However, cured resist on Cr/Au mask remained without any deterioration during wet etching of borosilicate glass for 80 min and fused silica for 20 hr in 49 wt% HF. This demonstrated that peeling-off of resist in HF solution when being used alone was not due to deterioration by chemical reaction with HF solution but due to poor adhesion to glass surface which was wet etched by penetrated HF molecules. Moreover, experiment

results showed that curing process of photoresist of less than 5.2 μm thickness failed to eliminate generation of pits. In addition, thin Cr/Au mask of 20/200 nm thickness also failed to prevent occurrence of pit. Strong effect of thickness of resist and Cr/Au mask on pit generation implied that cured photoresist not only reflowed into microcreeps but also blocked a large amount of HF molecules to penetrate the resist and that HF molecules penetrated the resist was perfectly blocked by Cr/Au mask.

We measured the etch depth and undercut of a borosilicate glass wafer with the optimized process. Figure 3.12 shows the etch depth and etch rate in the vertical and lateral directions according to the etch time. The vertical etch rate was slightly reduced from 8.0 μm/min at 15 min to 7.0 μm/min at 80 min. These findings can be explained as stemming from the presence of insoluble particles such as Al_2O_3 in the borosilicate glass wafer, as created from the 1.36 wt% Al atoms of the borosilicate wafer [57, 58]. For the same reason, the undercut rate also slightly decreased from 7.7 μm/min at 30 min to 7.4 μm/min at 80 min.



(a)



(b)

Figure 3.12. (a) Etch depth and undercut, and (b) etch rate of lateral and vertical direction.

The undercut rate was interestingly very high during the first 15 min, at 11.6 μm/min. In order to investigate its effect, we measured the side wall of the cavity (Figure 3.13). A high undercut rate produced a tapered side wall at the edge of the cavity in the initial time (Figure 3.13(a)). The tapered side wall remained during the further etching of the cavity and caused a discontinuous contour of the side wall in the deep cavity (Figures 3.13(b) and (c)). This was caused by the poor adhesion of the Cr/Au film to the borosilicate glass wafer, which led to the delamination of the Cr/Au mask at the etched edge [23]. The rough edge of the circle window proved the delamination of the Cr/Au mask (Figure 3.13(d)). The tapered side wall due to the poor adhesion and subsequent delamination of the Cr/Au mask may be possible to eliminate by the annealing of the glass wafer, a low-stress Cr/Au mask under e-beam deposition, or Cr/Au annealing [56, 59].

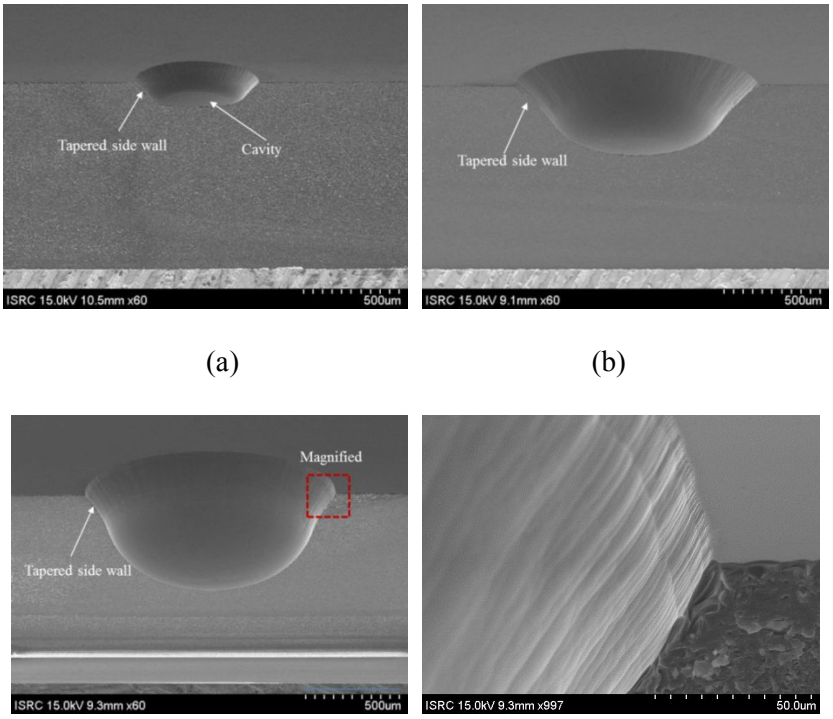


Figure 3.13. Cross-section of a wet-etched borosilicate glass wafer etched for (a) 15 min, (b) 40 min, and (c) 60 min at 49 wt% HF; (d) magnified image of the red squared area of (c).

In order to confirm the maximum etch time with the proposed etch mask in 49 wt% HF, we etched 525-μm thick fused silica. The etch rate of fused silica was reported to be approximately 1.0 μm/min in even highly concentrated HF (49 wt%). Therefore, several hours were required to fabricate the deep cavity of the fused silica, and the etch masks should resist during this time. We demonstrated maximum etching time of the proposed curing process of the PR in combination of the Cr/Au. Figure 3.14 shows the experiment results.

The results in Figures 3.14(a) and (b) showed that 525-μm-thick fused silica was penetrated after approximately 10 hr and that no pits were formed. Pits did not develop even after etch time of 20 hr (Figures 3.14(c)-(d)). These findings imply that the proposed process can be applied to most types of applications requiring a wet-etched deep cavity or through-via on a borosilicate glass wafer or fused silica, as the etch time of 20 hr at 49 wt% HF corresponded to approximate etch depth of 1.2 mm on fused silica. For the same reason, we did not confirm the maximum etch time of the proposed process. To the best of our knowledge, this is the best existing result.

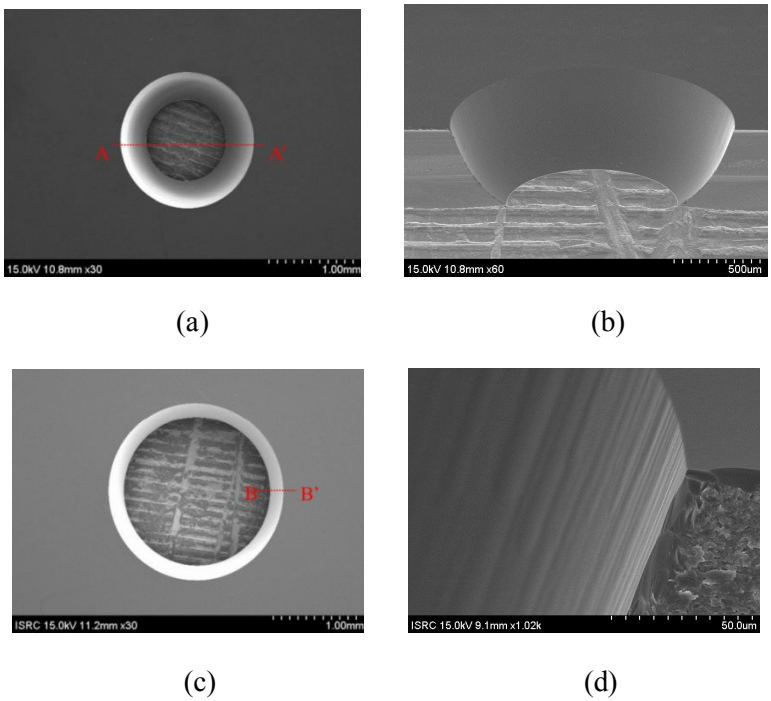


Figure 3.14. SEM images of (a) wet-etched fused silica at HF 49wt% for 10 hr, (b) cross section along AA' of (a), (c) wet-etched fused silica for 20 hr, and (d) cross section along BB' of (c).

Based on previous results, we fabricated bottom glass wafer with 250 μm-deep cavity. Fabrication process was same with Figure 3.2 except glass etching time of 30 min.

3.2.3 Anodic bonding and removal of handling glass

Silicon nitride scanner was anodically bonded to bottom glass wafer in vacuum condition. Bonding process was done with bonding force of 600 N, temperature of 350℃, voltage of 800 V, and vacuum level of less than 6×10^{-4} Torr. After bonding to bottom glass, handling glass was removed for releasing microscanner. HF solution wet etched handing glass. In order to protect bottom glass wafer during this step, bare silicon wafer attached to bottom side using adhesive layer of thick photoresist AZ4620. AZ4620 also covered edge of wafer using dropping pipettes in order to protect it from HF solution. Curing at 150℃ for 10 min was then followed by wet etching for 80 min in 49wt% HF solution. After rinsing in deionized (DI) water for 20 min, wafer was dipped into IPA (Isopropyl alcohol) solution and heated on hot plate.

3.2.4 Fabrication results

Figure 3.15 shows fabrication results of each types. Silicon rim and vertical comb actuator were successfully fabricated.

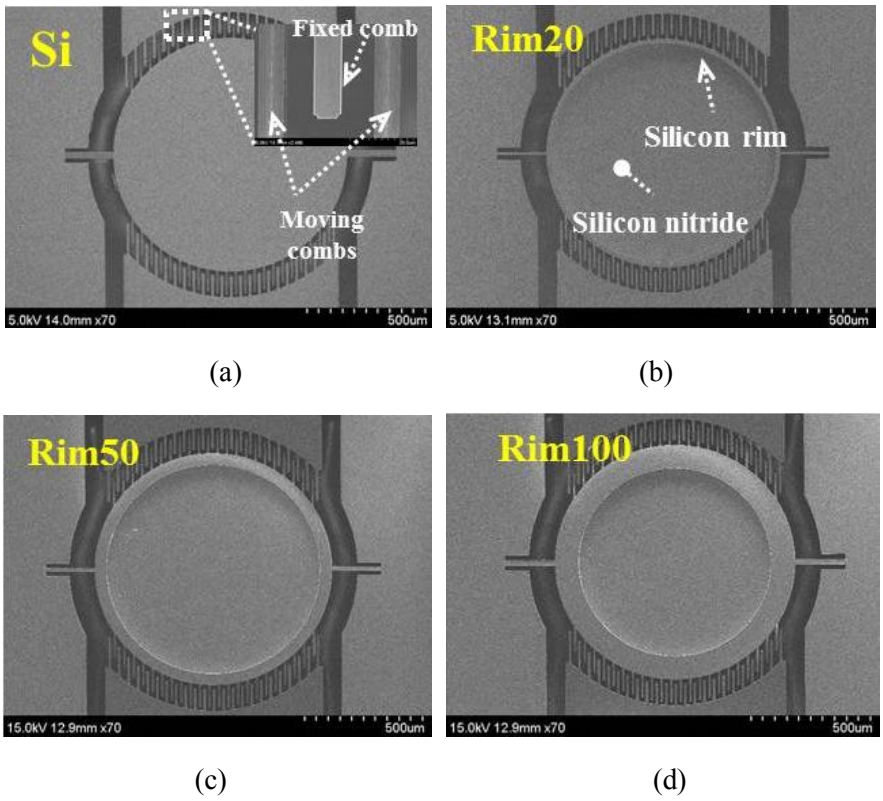


Figure 3.15. SEM images of fabricated SiN scanner of type of (a) Si, (b) Rim20, (c) Rim50, and (d) Rim100

Fabricated dimensions were measured and summarized in Following Table 3.2. Fabricated dimensions were less than 5% error from design values.

Table 3.2. Measured dimensional size of fabricated SiN scanner

Type		Si	Rim20	Rim50	Rim100
Spring width	Design	19.8 μm	12.0 μm	14.4 μm	16.8 μm
	Measured	19.3 μm	11.6 μm	14.0 μm	16.3 μm
Spring length	Design	205 μm			
	Measured	209.4 μm	208 μm	209.1 μm	209.2 μm
Silicon-rim width	Design	-	20 μm	50 μm	100 μm
	Measured	-	18 μm	49.2 μm	98.1 μm
Thickness	Design	50 μm			
	Measured	49 μm			

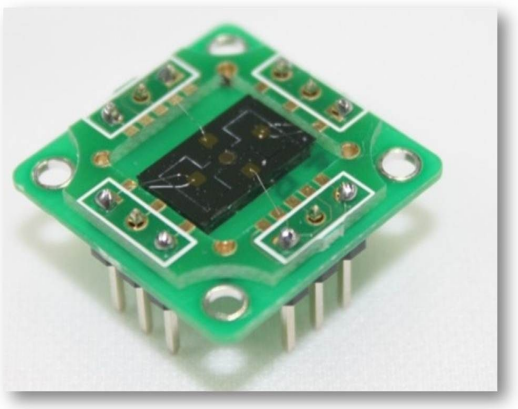


Figure 3.16. Silicon nitride scanner wire-bonded to printed circuit board (PCB)

3.3 Wafer-level vacuum packaging with glass cap

3.3.1 Overall process

Fabrication process is shown in Figure 3.17. Difference from process of non-packaged silicon nitride scanner is that glass wafer integrated with through-via is bonded on bottom side and silver paste is applied for signal path and adhesive material. Firstly, silicon nitride is deposited using LPCVD (Figure 3.17(a)). After Cr/Au deposition by thermal deposition, standard photolithography patterned circle for mirror plate (Figure 3.17(b)). Cr/Au and silicon nitride are etched using resist mask. Moving combs are then formed through photolithography and silicon dry etching (Figure 3.17(c)). After glass wafer with deep cavity is anodically bonded, silicon device layer is leveled to thickness of 50 μm (Figure 3.17(d)). Scanner is released by silicon dry etching (Figure 3.17(e)). Vacuum packaging is realized by anodic bonding of glass bottom wafer in vacuum condition (Figure 3.17(f)). Finally, single chip diced from wafer is attached to PCB using silver paste (Figure 3.17(g)). Process is done in wafer-level.

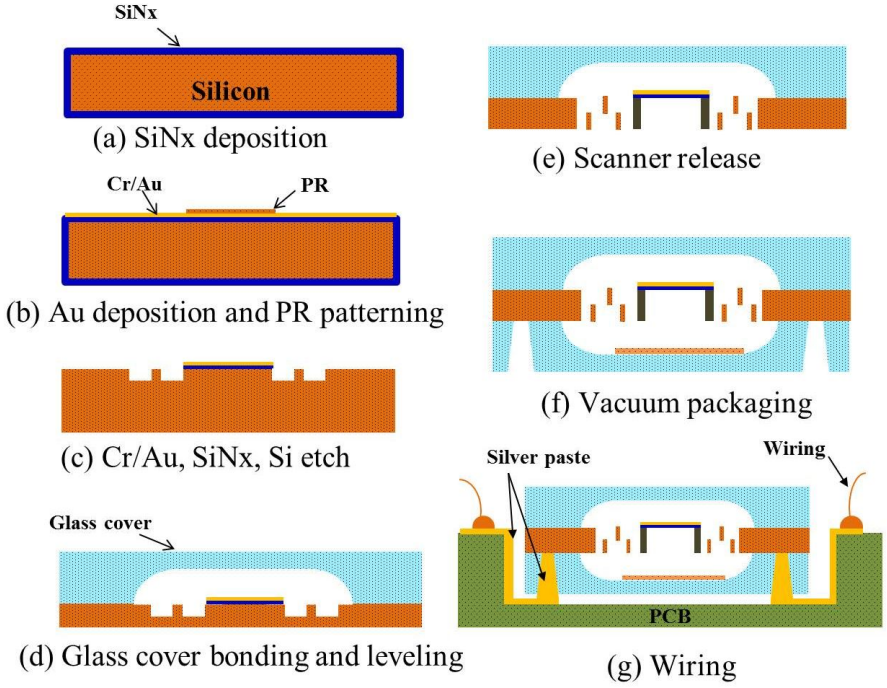


Figure 3.17. Fabrication process of wafer-level vacuum packaging of silicon nitride scanner

3.3.2 Top and bottom glass

Fabrication process of glass cap is identical to the process of bottom glass in previous section. The borosilicate glass wafer was cleaned via a standard process (SPM cleaning, H_2SO_4/H_2O=4/1). Cr/Au film was deposited on the top side of the glass wafer in the sputter device. Standard photolithography was used to pattern the AZ4330 into a circle window 300 μm in diameter. After the thermal curing of the AZ4330, the Cr/Au film was etched. This was followed with the wet etching of the glass wafer in 49 wt% HF for 30 min at

room temperature. The photoresist was then removed by SPM cleaning for 10 min. Finally, Cr/Au was stripped by means of wet etching (Figure 2.6(d)).

As for the bottom glass wafer, fabrication results of wafer are shown in Figure 3.18. Same with top glass wafer, deep cavity of more than 190 μm was required in bottom glass wafer as well. Moreover, through-via was needed to be assembled for supplying driving signals for packaged SiN scanner. Moreover, Ti getter should be placed in the surface of cavity in order to enhance vacuum level by trapping outgases inside the packaging. Figure 3.18 shows successful fabrication of deep cavity, through-vias and Ti getter. Cavity and through-via was formed by glass wet-etching and sand blasting, respectively. Ti getter was deposited with shadow mask using sputter machine.

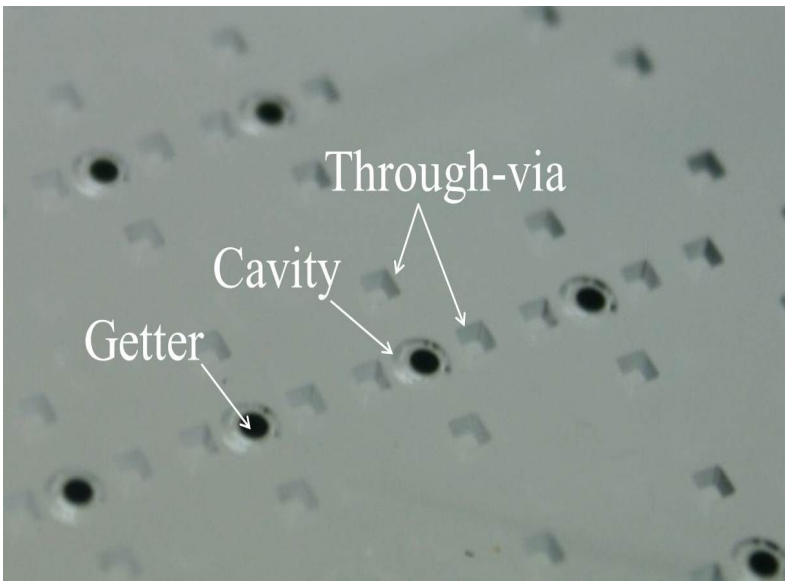
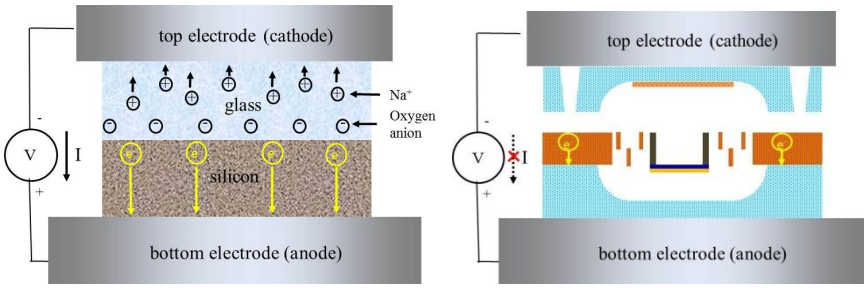


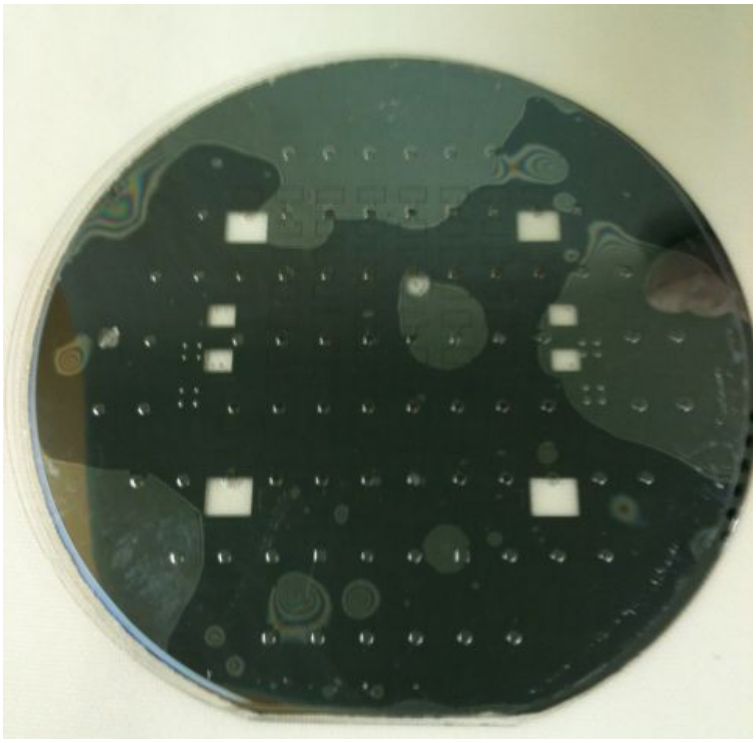
Figure 3.18. Photograph of fabricated bottom glass wafer integrated with deep cavity, through via and Ti getter.

3.3.3 Triple-stack anodic bonding

Silicon nitride scanner was anodically bonded to bottom glass wafer in vacuum condition. Bonding process was done with bonding force of 600 N, temperature of 350℃, voltage of 800 V, and vacuum level of less than 6×10^{-4} Torr. An issue should be resolved was that electrical path was not formed because anode and cathode were contact to the glass wafer of nonconductive material (Figure 3.19(a)-(b)). Therefore, electron did not transfer to cathode, and bonding was not achieved. Figure 3.19(c) showed a lot of voids occurred during anodic bonding. Possible solution was making electrical path from backside of scanner wafer to front side using a frit of aluminum foil (Figure 3.20(a)). Foil was attached at two points on edge of scanner wafer (Figure 3.20(b)). Figure 3.20(c) shows successful bonding without generation of voids.

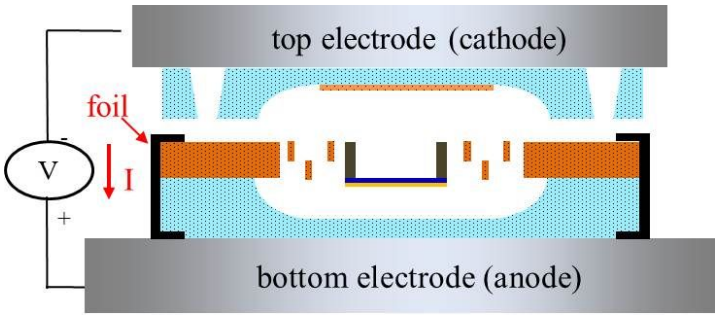


(a) (b)

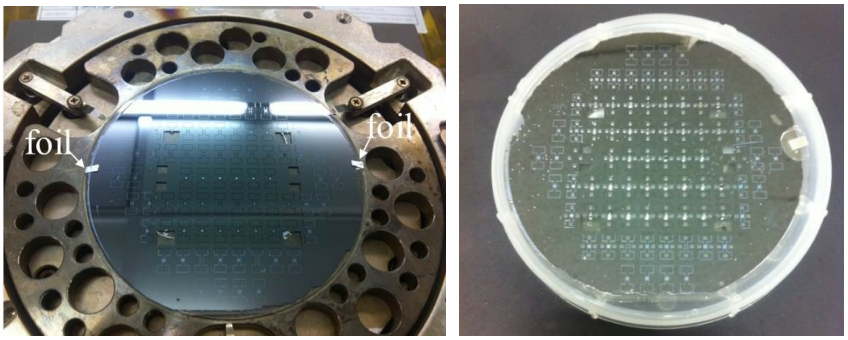


(c)

Figure 3.19. Moving path of anodic bonding in (a) double stack and (b) triple stack, and voids in triple-stack bonding without using of foil



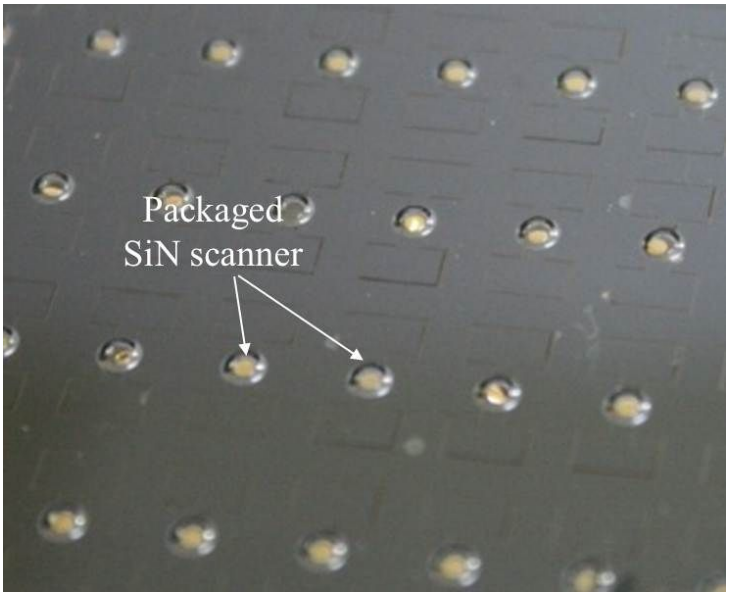
(a)



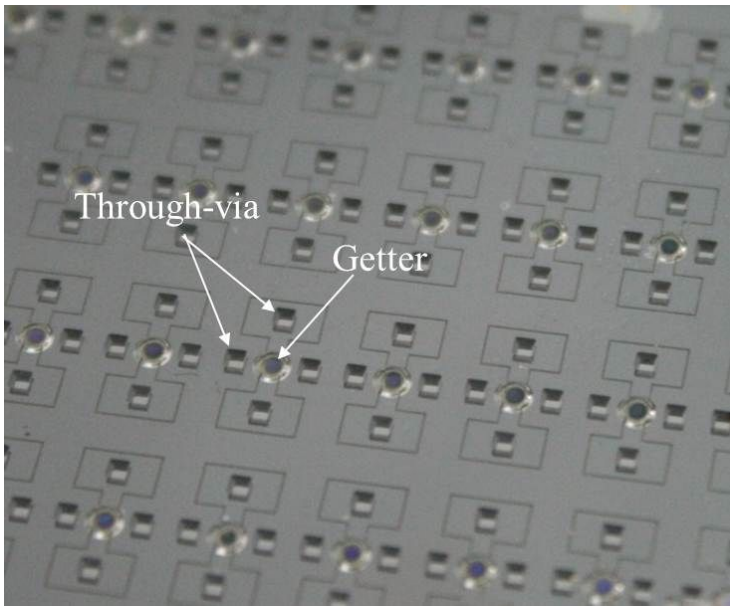
(b) (c)

Figure 3.20. (a) Electron moving path in anodic bonding with foil, and photographs of (b) anodic bonding chuck with foil and (c) anodic bonding result

After bonding to bottom glass, wafer was diced into single chips using dicing saw. Figure 3.21 shows successful packaging of SiN scanner using glass cap and bottom glass.



(a)



(b)

Figure 3.21. Photographs of wafer-level-vacuum-packaged SiN scanner (a) in top view and (b) bottom view.

3.3.4 Fabrication results

SiN scanner with silicon rim and vertical comb was successfully fabricated as shown in Figure 3.22(a) and (b). Vacuum packaging of SiN scanner is demonstrated in Figure 3.22(c). SiN scanner vacuum-packaged in wafer-level was separated into single module using dicing saw.

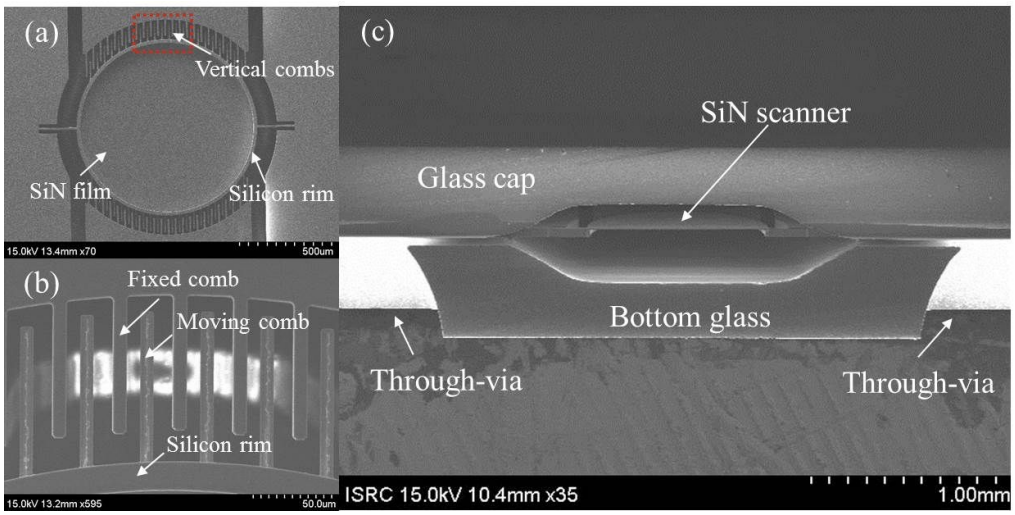


Figure 3.22. SEM images of packaged SiN scanner: (a) SiN scanner with silicon rim and vertical comb, (b) magnified image of area of dotted square in (a), and (c) cross-section of packaged SiN scanner

Single chip was attached to PCB (Figure 3.23). Driving signal was delivered to SiN scanner through through-via and silver paste.

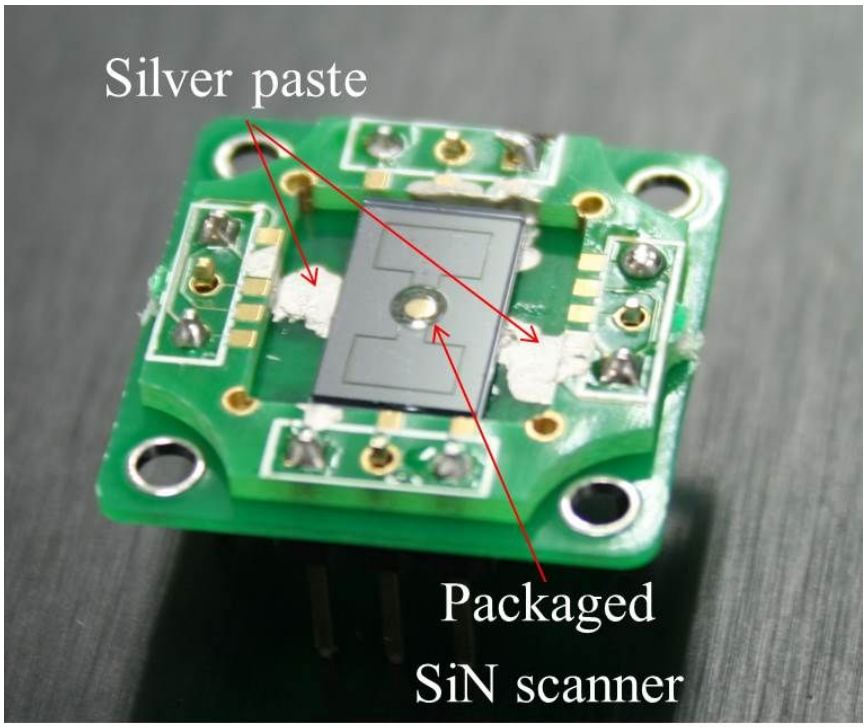


Figure 3.23. Packaged SiN scanner which was attacked to PCB

3.4 Wafer-level vacuum packaging with TWIn substrate

3.4.1 Previous work

3.4.1.1 TWIn substrate

Microelectromechanical systems (MEMS) have been exploited in novel devices, e.g., gyroscopes, accelerometers, RF filters, optical multiplexers, microlenses, and micro-pressure sensors. However, reliability has been a barrier for MEMS products achieving commercial success. Among various solutions for this problem, vacuum packaging of MEMS products is considered as the best solution [60, 61]. The packaging prevents contamination of the MEMS from external environments. Therefore, the lifetime and reliability of the MEMS are extended and improved. Furthermore, vacuum packaging improves the performance of MEMS devices. For instance, inertia sensors such as gyroscopes, accelerometers, and resonators operate with a larger quality factor which leads to improved sensitivity with a decreased damping ratio. The vacuum has low thermal conduction, isolates MEMS devices from external environments, and increases the thermal stability [62]. In addition, the packaging of MEMS devices leads to easier processes for integration with analog systems.

However, commercial chip level packaging requires separate packaging for every single chip and hence, results in a high cost. The majority of the MEMS

cost production is due to the packaging. Wafer-level packaging, on the other hand, seals every chip on the wafer at once. Therefore, a dramatic reduction in the packaging cost can be realized. Furthermore, MEMS devices are protected against mechanical impacts and contamination from following processes such as dicing.

Wafer-level packaging techniques are categorized into a lateral feed-through and vertical feed-through by the structure of the interconnection to the encapsulated devices in a cavity. The lateral feed-through establishes a metal line on the same surface of the MEMS device [63-67]. Therefore, the overall size of the MEMS device is larger than devices with the vertical feed-through. Furthermore, the fabrication process becomes complicated, which is unsuitable for batch processing. However, vertical feed-through attains the electrical interconnection using hole vias which are fabricated in a separate wafer. Therefore, the fabrication process is not complicated. Moreover, since the electrical interconnection is arranged vertically, the overall size of the MEMS device is smaller than in case of using the lateral feed-through.

The vertical feed-through is typically fabricated on a silicon wafer [68-73]. Hole vias are realized using a deep reactive- ion etch (DRIE) of the silicon. Then, a silicon dioxide (SiO_2) is deposited on the sidewall of the hole vias in order to isolate the electrical interconnection from the silicon substrate. Electroplating fills the hole vias with a metal. Those processes can easily establish high aspect-ratio hole vias. However, the SiO_2 layer can fail to

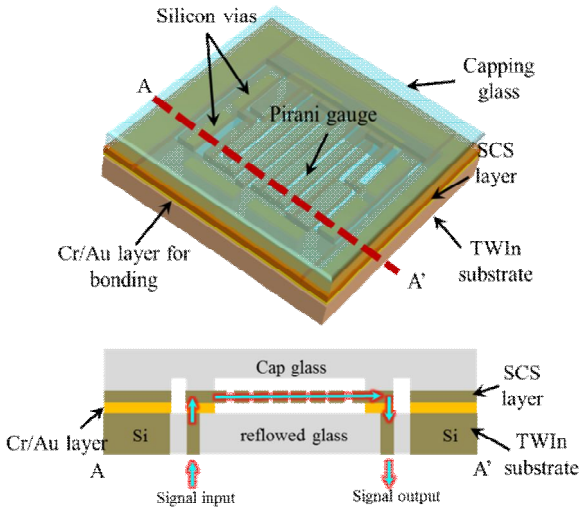
isolate the metal interconnection to the silicon substrate due to hole defects on the layer. Moreover, voids can be produced inside metal vias during the filling of high aspect-ratio holes through electroplating [74]. In order to circumvent those problems, a glass wafer is used as a substrate [75, 76]. However, the etch rate of glass using dry etching is very low. In addition, cracks can be produced by thermal stress during bonding if the coefficient of thermal expansion (CTE) is different between the glass substrate and the metal vias. Furthermore, the conical figure of the side walls of the hole vias in the glass substrate generates wafer bending caused by temperature gradations [77]. Moreover, the glass wafer cannot resolve the generation of voids during metal electroplating in high aspect-ratio holes.

We previously proposed the fabrication process for the silicon through-wafer interconnection (TWIn) which had no voids and has the same CTE as well as perfect isolation of hole vias [78]. The aim of this study was to fabricate the TWIn substrate for the vertical feed-through and develop a wafer-level packaging process for MEMS devices with a TWIn substrates. In order to demonstrate the vacuum sealing, a micro-Pirani gauge was fabricated and packaged.

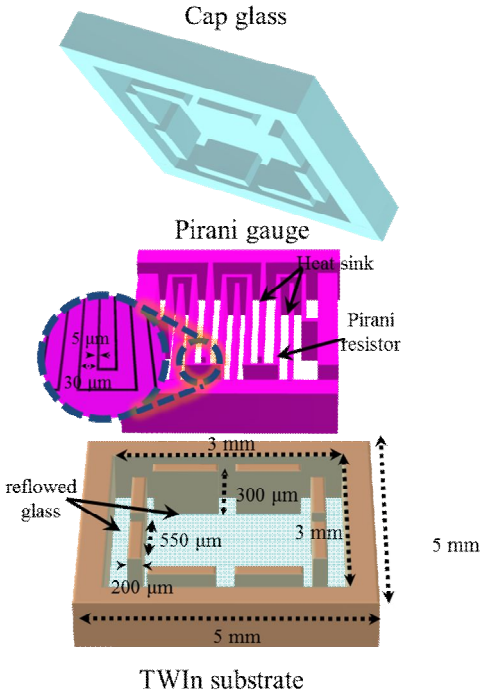
3.4.1.2 Design

The proposed wafer-level packaging consists of the TWIn substrate for an electrical interconnection, a single crystal silicon (SCS) layer for MEMS

devices, and a glass wafer for capping (Figure 3.24(a)). The TWIn substrate has silicon through-vias and reflowed glass surrounding silicon vias. The size of a single die is 5 mm × 5 mm and the reflowed glass occupies a 3 mm x 3 mm area in the center of the die (Figure 3.24(b)). Silicon vias are located in the reflowed glass. Outside of the reflowed glass is the silicon, which is used as a bonding surface for the SCS layer. The silicon via is made of the low resistivity silicon (LRS) wafer (ρ=0.001-0.003 Ω·cm) in order to reduce the electrical resistance of the vias. The silicon via has a size of 550 μm × 200 μm × 300 μm. The reflowed glass isolates silicon vias as well as occupies an area under which the MEMS devices are fabricated in the SCS layer. This structure has the advantage of having no voids inside the vias and no leakage current from vias caused by an isolation failure since the surrounding material of the vias is non-conductive. Furthermore, a parasitic capacitance between the device and a bottom plate can be removed since the bottom plate consists of glass [79]. Moreover, since borosilicate glass has a CTE equal to silicon, the TWIn structure can avoid cracks during bonding caused by different CTEs between the vias and the substrate.



(a)



(b)

Figure 3.24. Schematic view of (a) the wafer-level packaging for the MEMS device (the Pirani gauge), and (b) three components of the proposed packaging structure.

The SCS layer is placed on the TWIn substrate through a bonding process. A variety of MEMS devices, such as a resonator, an accelerometer, a gyroscope, and a RF switch can be fabricated on the SCS layer, which has the advantages of low residual stress, high mechanical strength, and high thermal resistance [5]. A silicon Pirani gauge is fabricated in order to monitor the vacuum level inside the packaging [80, 81]. The Pirani gauge consists of a Pirani resistor and a heat sink. The Pirani resistor generates heat as current from a power supply flows through the resistor. As the vacuum level increases and the air to carry away the generated heat decreases in the package, the temperature of the Pirani resistor increases, which changes the resistance of the Pirani resistor. Therefore, the pressure in the packaging can be measured by monitoring the resistance of the Pirani gauge.

Since the dynamic range of the Pirani gauge is proportional to the surface area of the Pirani resistor [80]. a meander structure for the Pirani resistor is adopted. Moreover, the great height of the resistor also increases the surface area and expands the dynamic range. The Pirani resistor with a width of 30 μm, a height of 90 μm, and a total length of 33.2 mm is designed to have a surface area of 3.99 mm^2 with a die area of only 2.52 mm^2. The heat sink adds a heat path from the Pirani resistor and increases the sensitivity within a dynamic range. The gap between the Pirani resistor and the heat sink is 5 μm.

The wafer-level packaging is established by capping the fabricated Pirani gauge with the glass wafer. Since the glass wafer has large permittivity and optical transparency, the proposed WLP allows a RF switch to reduce the signal loss due to parasitic capacitance between the switch and the capping material as well as allows an optical signal to be delivered. Conventional anodic bonding is done under a vacuum level ($<5\times10^{-5}$ Torr) for capping of the fabricated Pirani gauge with the glass wafer.

3.4.1.3 Fabrication process

LRS is used in order to increase the electrical conductance of the vias. The glass, which surrounds and isolates the silicon vias, is fabricated by the glass reflow method. Figure 3.25 shows the fabrication process of the TWIn substrate. Silicon dioxide (SiO_2) of 2 μm thickness is deposited and etched with ion etch and a vapor deposition equipment (P-5000, AMK) on the LRS wafer (Figure 3.25(a)). The SiO_2 layer is used as an etch mask for the deep reactive ion etch (DRIE) process to establish the trench, in which the glass flows around the silicon via.

The etch depth of the LRS wafer is 360 μm (Figure 3.25(b)). The SiO_2 etch mask is then removed by dipping it into 49% hydrofluoric acid (HF) for 10 min. A borosilicate glass wafer is anodically bonded in a vacuum condition ($<3\times10^{-3}$ Torr) (Figure 3.25(c)). The vacuum condition is essential for the

reflowed glass to flow into the etched trench by the pressure difference between the inside and outside of the trench. Glass reflowing is done by putting the bonded wafer into a furnace for 5 hr at 1020°C. The increase and decrease rate in temperature of the furnace are 15 °C/min. The fabrication of the TWIn substrate is completed by leveling the top and bottom surface on the bonded LRS wafer with a wafer-lapping by removing 20 μm and 220 μm, respectively, with a final thickness of 300 μm for the LRS wafer (Figure 3.25(d)).

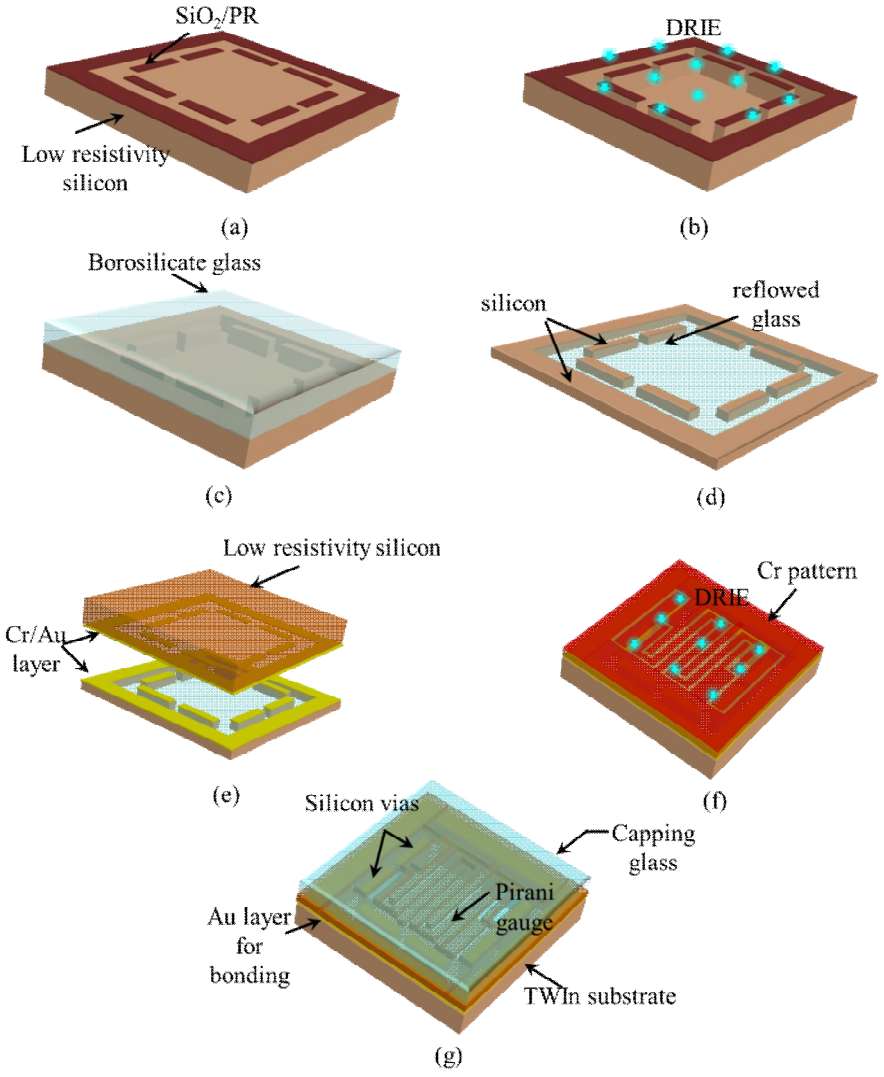


Figure 3.25. The fabrication process of the Pirani gauge and the WLP; (a) SiO_2/PR deposition and patterning, (b) DRIE of the silicon, (c) anodic bonding and glass reflow, (d) the wafer lapping of both the top and the bottom side, (e) eutectic bonding and wafer lapping of the LRS wafer, (f) Cr patterning and deep RIE for releasing the gauge, and (g) capping the Pirani gauge with the glass.

The MEMS device is fabricated on the SCS layer. The LRS wafer (0.001~0.003 ohm.cm) is used as the SCS layer. The SCS layer is formed by bonding the LRS wafer to the TWIn substrate and leveling to a designed device thickness with the wafer lapping. Au eutectic bonding including a Cr adhesion layer is used for the purpose of mechanically attaching the LRS wafer to the TWIn substrate as well as electrically connecting the Pirani gauge to the silicon via. In addition, the Cr layer establishes silicidation by annealing and achieves an ohmic contact between the Au and the silicon.

The fabrication of the SCS layer is initiated by bonding the LRS wafer to the TWIn substrate (Figure 3.25(e)). In order to achieve the ohmic contact, the native oxide on the LRS wafer and TWIn substrate is fully removed. They are dipped into a buffered oxide etchant (BOE, NH_4F:HF=5:1) for 20 sec, rinsed with deionized water for 6 min, and dried with N_2 gas. A Cr/Au layer of 70/1000 nm thickness is then deposited on the SCS wafer. On the TWIn substrate, the top side also has a Cr/Au layer of 70/1000 nm thickness, whereas the bottom side has a 30/200 nm thickness. The top side is used as the eutectic bonding surface, and the bottom side connects to the PCB pad. After Cr/Au deposition, a photoresist (PR) is patterned on the LSR wafer and on both sides of the TWIn substrate. The Cr/Au layer is then etched by a wet etchant. The PR mask is removed by SPM (H_2O_2:H_2SO_4=1:4) cleaning for 10 min. Eutectic bonding follows with 3000 N of press pressure at 370 °C for 2

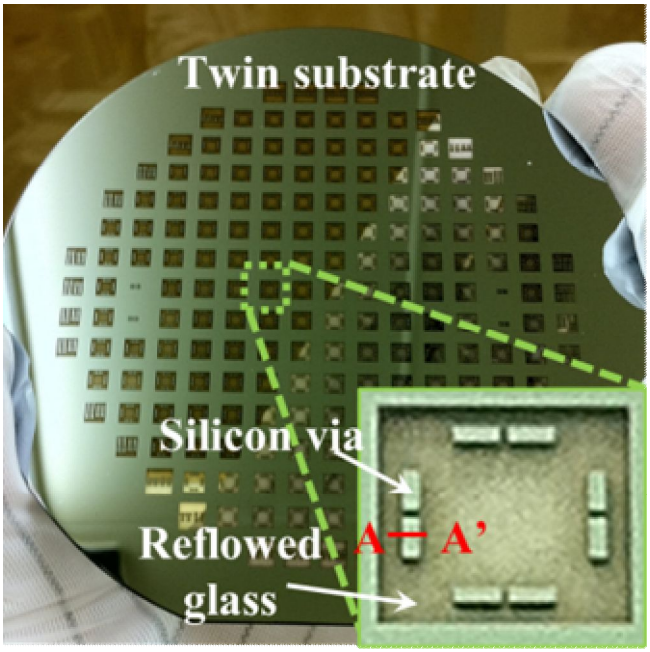
hr under vacuum conditions (<3×10^{-3} Torr) with a commercial bonder (EV-501, EVG). The bonding process achieves not only eutectic bonding but also Cr silicidation. Then the SCS layer is leveled with the wafer lapping to a final thickness of 90 μm on the TWIn substrate.

The Pirani gauge is fabricated in the SCS layer (Figure 3.25(f)). A Cr etch mask is patterned using the lift-off process through Cr deposition of 50 nm thickness. The Pirani resistor is released by the DRIE process with 90 μm deep etching using the Cr etch mask. Cr is then removed by the RIE equipment (PlasmaPro 800Plus, OXFORD instruments). The Cr is fully removed for the current uniformly distributing in the Pirani resistor.

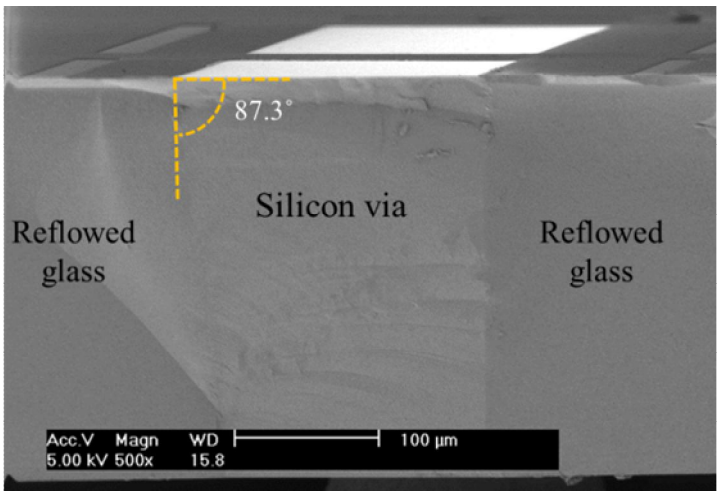
WLP is accomplished by capping the SCS layer with a glass wafer (Figure 3.25(g)). A cavity between the SCS layer and the capping glass wafer is developed by forming a trench on the capping glass wafer. The trench is fabricated by HF wet etch. A 30/200 nm thickness of the Cr/Au film is evaporated and lifted off in an acetone solution. Before etching by HF solution, the back side of the glass wafer is protected by a temporarily bonded silicon wafer using PR. Then glass is wet etched for 8.5 min to form a 60 μm cavity. Removal of silicon wafer and Cr/Au is followed. The capping glass wafer is anodically bonded to the Pirani gauge under the vacuum conditions (<5×10^{-5} Torr). The packaged wafer is diced into chips.

3.4.1.4 Results and discussion

Figure 4.3 shows the fabricated TWIn substrate with the glass reflow process. The reflowed glass appears transparent in the TWIn substrate (Figure 3.26(a)). The magnified image demonstrates that the reflowed glass surrounded the silicon vias in the center of a single die. Figure 3.26(b) shows a cross-section of a silicon through-via and the reflowed glass. No voids were found inside the silicon via and the reflowed glass successfully enclosed the silicon via. The slope angle of the silicon via was 87.3 ° due to an isotropic etch during the DRIE process. Consequently, size of the silicon via on the bottom side was smaller at 514 μm × 190 μm than that on the top side at 550 μm × 200 μm. However, this shrinkage was only less than a 10 % decrease in size.



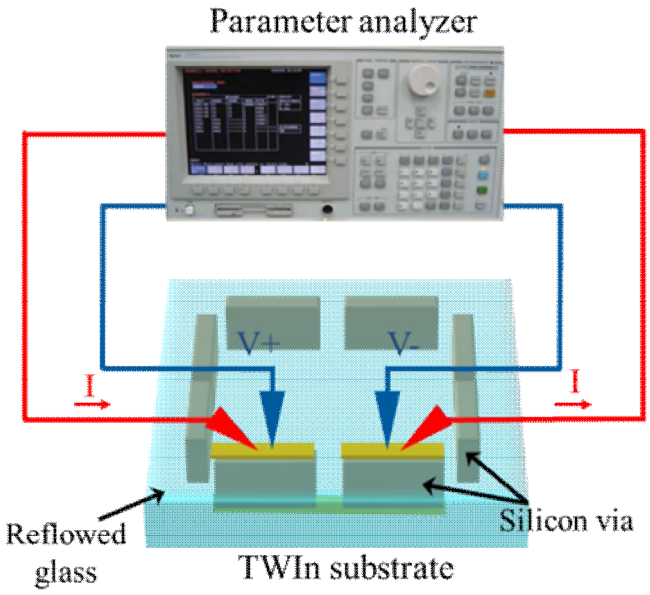
(a)



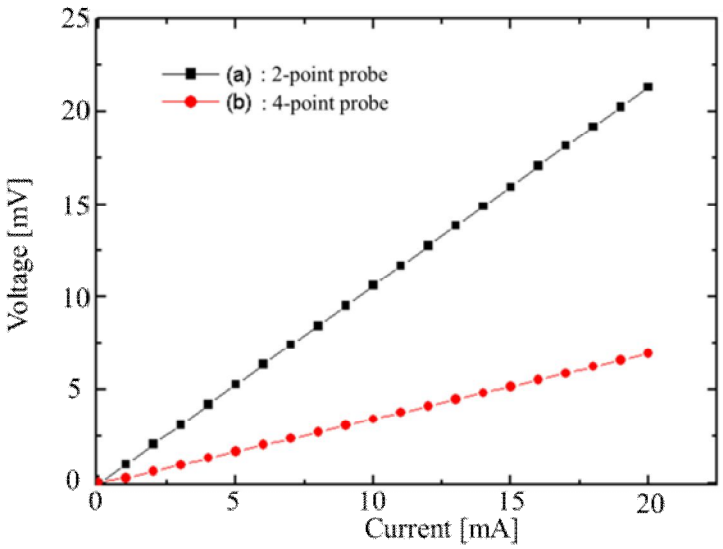
(b)

Figure 3.26. Fabrication result of the TWIn substrate: (a) photograph of the TWIn substrate, and (b) the SEM image of the cross-section along A-A'.

In order to measure the resistance of the silicon through-via, Cr/Au patterns were formed on the TWIn substrate. First, the surface of the TWIn substrate was cleaned with BOE followed by deposition of 30/200 nm thickness of the Cr/Au film. The formation of the Cr silicide was achieved by annealing at 350°C for 2 hr. Figure 3.27(a) shows a schematic of the experimental setup to measure the resistance of silicon vias. The four-point probe method was used to exclude the parasitic resistance including the contact resistance. DC current was supplied and corresponding voltage was measured by a parameter analyzer (4156C, Agilent). Figure 3.27(b) shows the measurement results. The results show that ohmic contact with help of Cr silicide. Curve (a) shows the measurement results of a two-point probe method whereas curve (b) shows the results of the four-point probe method. The difference between curves (a) and (b) were caused by the parasitic resistance. The measured resistance of curve (b) was 340 mΩ, while that of the silicon via was 89 mΩ excluding the Au resistance. The calculated one was 65.3 mΩ based on the measured dimensions and the resistivity of silicon, which was 2.20×10^{-3} Ω·cm. The discrepancy between the calculated and measured resistance could be caused by an unexpected minute-parasitic resistance along the measurement setup such as cable resistance. Nevertheless, the resistance of the silicon via was small enough so not to affect the total resistance of the device, i.e., the Pirani gauge.



(a)



(b)

Figure 3.27.(a) Measurement setup for the resistance of the silicon via, and (b) measurement result

The Pirani gauge was fabricated in the LRS layer, which was bonded to the TWIn substrate with Au eutectic bonding. The dimension of fabricated Pirani resistor was measured to be as follows: 30.8 μm width, 4.2 μm gap, and 92.4 μm height (Figure 3.28(a)-(d)). The cross-section of the Pirani resistor and heat sink shows an ideal anisotropic-etch profile with an 89.8° slope angle. One possible reason why the width was enlarged from the design value of 30 μm could be due to the larger width of the negative PR pattern in the lift-off process.

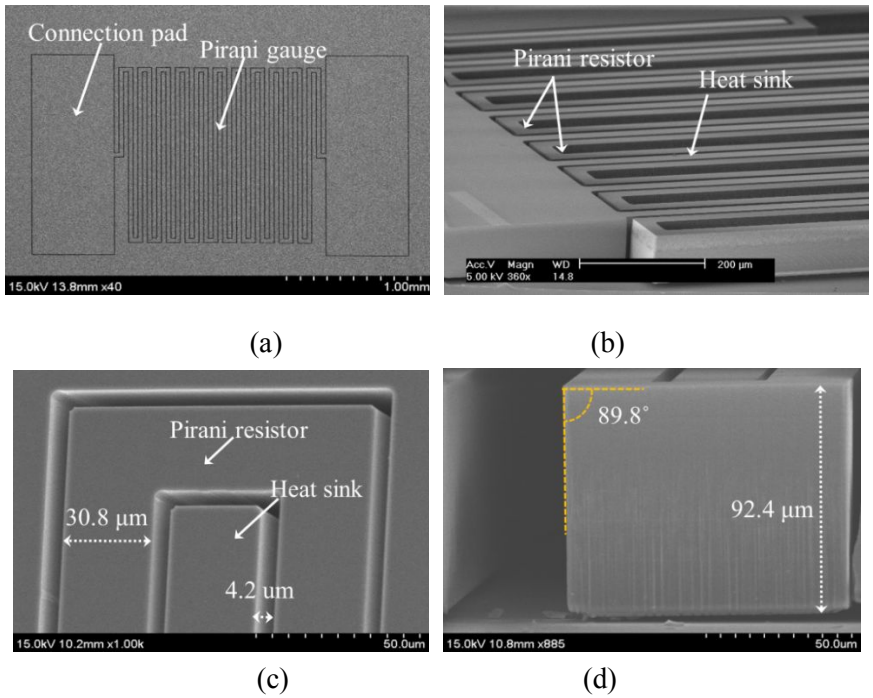


Figure 3.28. SEM images of the Pirani gauge fabricated.

The resistance of the Pirani gauge was measured with the four-point probe method. Figure 3.29 shows the measured resistance of the Pirani resistor. Curve (a) shows a Schottky contact caused by the unsuccessful removal of native oxides on the TWIn substrate and LRS wafer. In contrast, curve (b) shows that the Pirani gauge was an ideal resistor with the full removal of the native oxide and formation of the Cr silicide. The resistance of the Pirani gauge was 258.5 Ω. The design value was 271 Ω. The calculated resistance based on the measured dimension was 259 Ω and matched well with the measurement results. This result shows that the main factor for the reduced resistance from that of the design value was the enlarged width and height of the Pirani resistor caused by an error from the negative PR pattern for the Cr lift-off process.

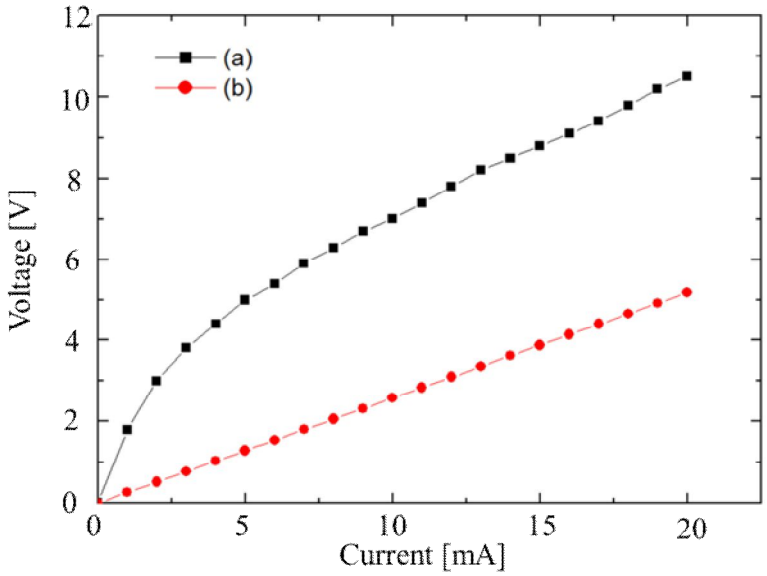
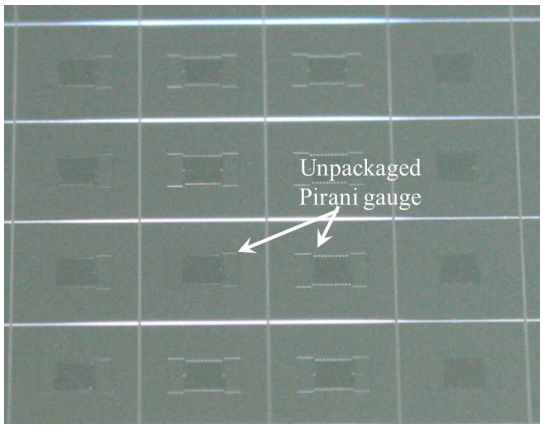
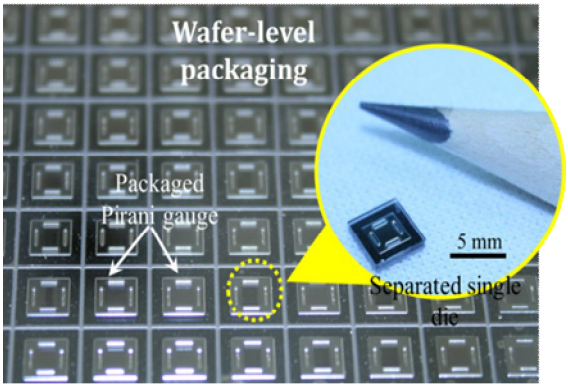


Figure 3.29. Measurement result of the resistance of the Pirani resistor

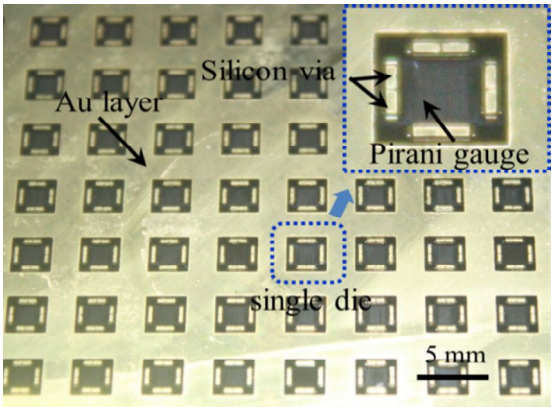
The Pirani gauge fabricated on the TWIn substrate was packaged by bonding to a capping glass wafer. Figure 3.30 shows the success of the wafer-level packaging of the Pirani gauge. Figure 3.30(a)-(b) shows that the glass wafer capped the Pirani gauge, which was placed in the trench. The wafer-level packaged Pirani gauge was separated into single chips by dicing. Moreover, a photograph of the bottom side of the TWIn substrate (Figure 3.30(c)) proves that the TWIn substrate had no cracks from stress through the eutectic and anodic bonding processes. This implies that the silicon via with the flowed glass prevents cracks from stress due to different CTEs between the via and substrate unlike the metal through-via.



(a)



(b)

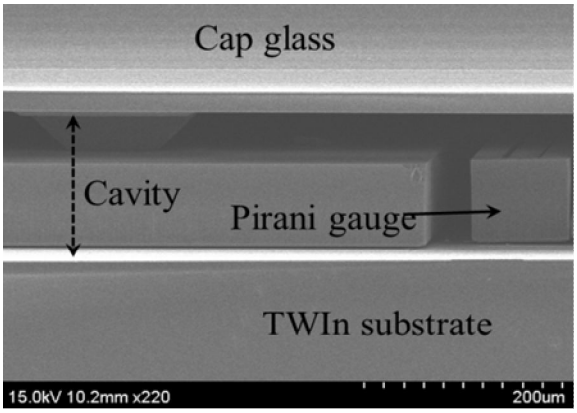


(c)

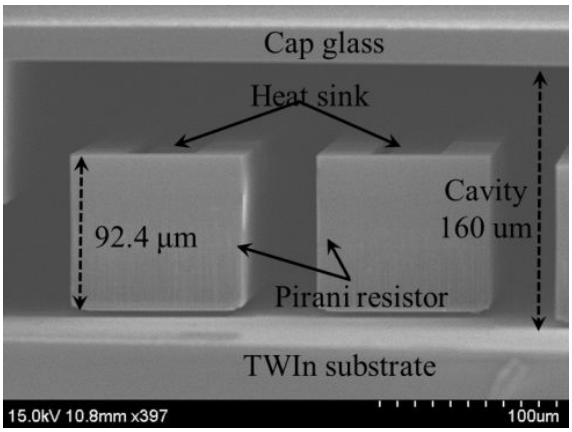
Figure 3.30. The Pirani gauge (a) before and (b) after the WLP. (c) the bottom side of the packaged Pirani gauge.

Figure 3.31 shows scanning electron microscopy (SEM) images of the packaged Pirani gauge. The cavity between the capping glass wafer and the TWIn substrate was fabricated, and the Pirani gauge was successfully packaged in the cavity. The height of the cavity between the TWIn substrate and the capping glass wafer was 160 μm with an error of less than 6 % from the design value. Figure 3.31(c) shows the eutectic bonding and anodic bonding interfaces.

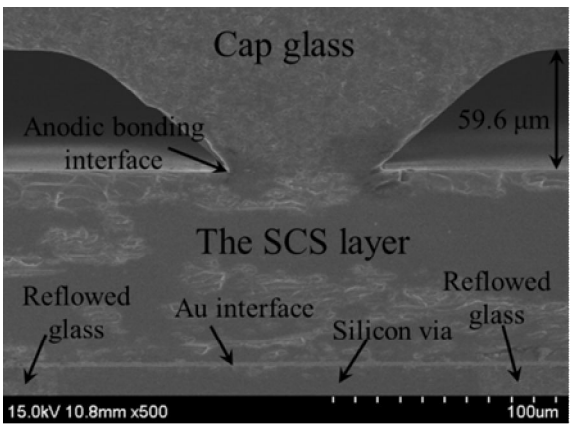
The bonding strength was tested in order to confirm successful eutectic bonding between the TWIn substrate and Pirani gauge. Multipurpose bond tester (DAGE 4000, Nordson Company) was used and the bonding interface was pushed with uniform velocity. The measured shear strength was 60 N with 25 mm^2 of die area. Considering 25 N minimum force for microelectronic devices as based on the standard of the MIL-STD-883F, this result indicates the proposed packaging platform is sufficient for use with packaging of microelectronic devices.



(a)



(b)



(c)

Figure 3.31. SEM images of the packaged Pirani gauge. (a) The Pirani gauge in the cavity of the package, (b) magnified image of the gauge, and (c) bond interfaces.

3.4.1.5 Test results

The calibration of the Pirani gauge was implemented using a conventional Wheatstone bridge circuit. Three resistors with a resistance error less than 1% from the Pirani resistance were used for the circuit. The output voltage, V_{out}, was measured with a multimeter (34401A, Agilent). Even tiny variations in the voltage source results in large deviations in the measurement results. Therefore, a high precision and stable DC power source (E9647A, Agilent) applied the constant voltage across the Wheatstone bridge circuit with resolution of 0.1 mV.

A separated single die was connected to the external address line through a printed circuit board (PCB). Figure 3.32 shows the unpackaged and packaged Pirani gauges, which were attached to the PCB. The PCB had plated through-holes, which were used to connect to the silicon vias in the TWIn substrate. Transmission lines were positioned on the back side of the PCB. The attachment and electrical connection of the die to the PCB were accomplished by an anisotropic conductive film (TSB21000SL3-35A, Telephus Inc.) at 190 °C with >2 MPa press pressure.

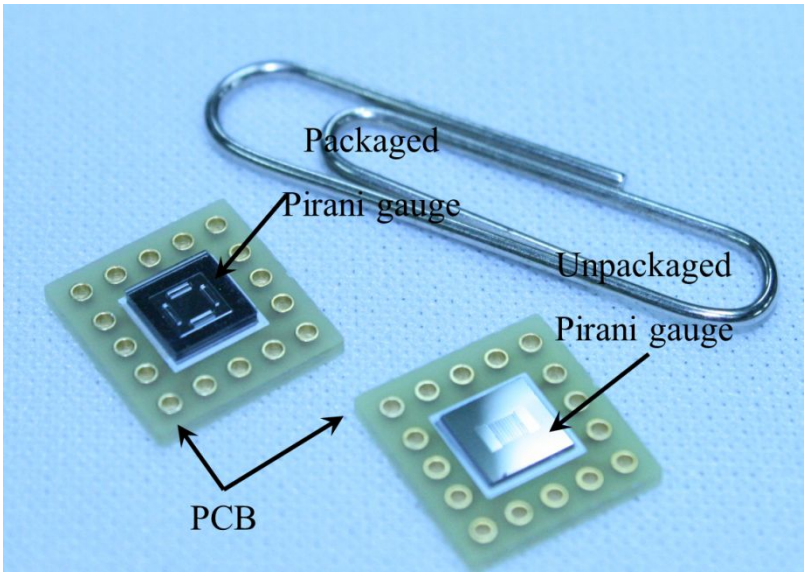
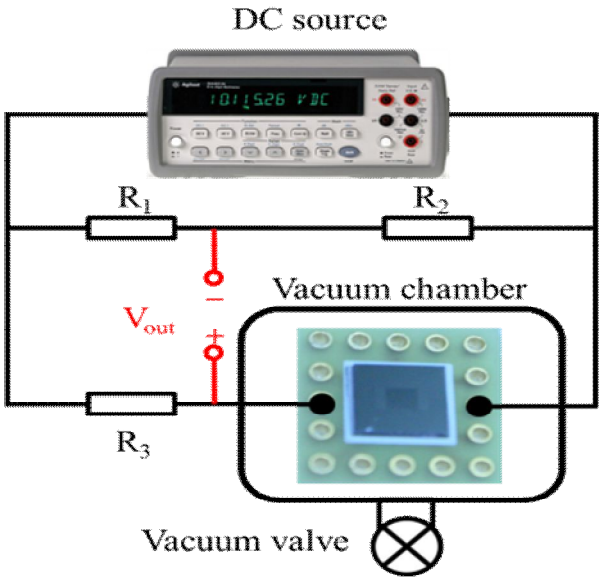


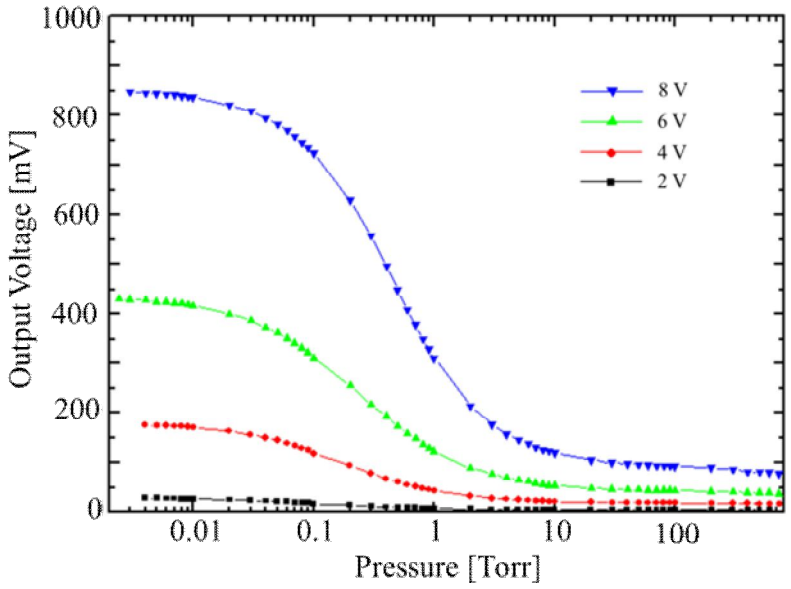
Figure 3.32. Packaged and unpackaged Pirani gauge attached to the PCB having plated through-holes.

The fabricated unpackaged Pirani gauge was attached to the PCB in order to obtain a calibration curve. The single die was loaded into a vacuum chamber to plot the V_{out} of the Wheatstone bridge circuit versus the vacuum level. Figure 3.33(a) shows a schematic of the measurement setup. The vacuum level was controlled by a vacuum valve on the chamber. After evacuating the chamber in the pressure of less than 1×10^{-5} Torr, the vacuum level was decreased by releasing the vacuum valve. Figure 3.33(b) shows the measurement results. The applied voltage varied from 2 to 8 V. As the applied voltage increased, the average sensitivity of the Pirani gauge, the slope of the figure, increased. For 2 V, 4 V, 6 V, and 8 V, the input voltage had a sensitivity of 2.21 mV/Torr, 14.87 mV/Torr, 36.18 mV/Torr, and 71.82 mV/Torr,

respectively. Therefore, an 8V input voltage was preferred in terms of sensitivity. Meanwhile, the dynamic range for 2 V, 4 V, and 6 V was 0.01-10 Torr. This result agrees with previous results that the dynamic range of a Pirani gauge was mainly defined by the thermal conductance of an ambient gas and substrate. However, the 8V input voltage had a reduced dynamic range of 0.1 – 10 Torr. The main reason for this result could be the increased conductance of the silicon Pirani resistor at high temperatures. Even though the conductance of the intentionally doped silicon remains roughly constant in a broad range of temperatures, additional increases in conductivity take place through the thermal ionization of the silicon atoms above ~ 600K [82]. In the case of 8 V, the temperature of the Pirani gauge with less than 0.1 Torr may exceed the critical temperature for constant conductance, and the output voltage of the Wheatstone bridge circuit cannot increase following the increasing temperature of the Pirani resistor. In order to demonstrate this assumption, the temperature of the Pirani resistor for an 8 V input voltage at a pressure of 0.1 Torr was calculated.



(a)



(b)

Figure 3.33. (a) Measurement setup for calibration of the Pirani gauge composed of resistors in error with less than 1% from the Pirani resistor, and (b) calibration curves according to the DC input voltage

The temperature coefficient of the resistance (TCR) for the gauge was extracted through the measurement curve of the resistance versus temperature (Figure 3.34). The measured TCR was 1.5×10^{-3} /K, which was in agreement with the previous result [83]. Based on the output voltage of the Wheatstone bridge circuit, the resistance of the Pirani gauge was 370.0 Ω at 0.1 Torr, and the calculated temperature of the Pirani gauge was 581.9 K. This result shows that the main reason for the reduced dynamic range is the non-constant resistance of the silicon Pirani resistor.

To satisfy the sensitivity as well as the dynamic range, a calibration curve was used for the 6 V input voltage.

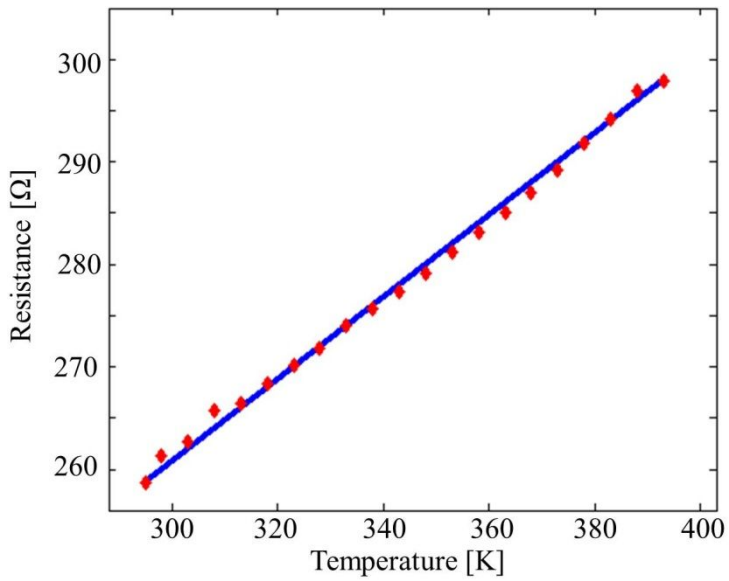
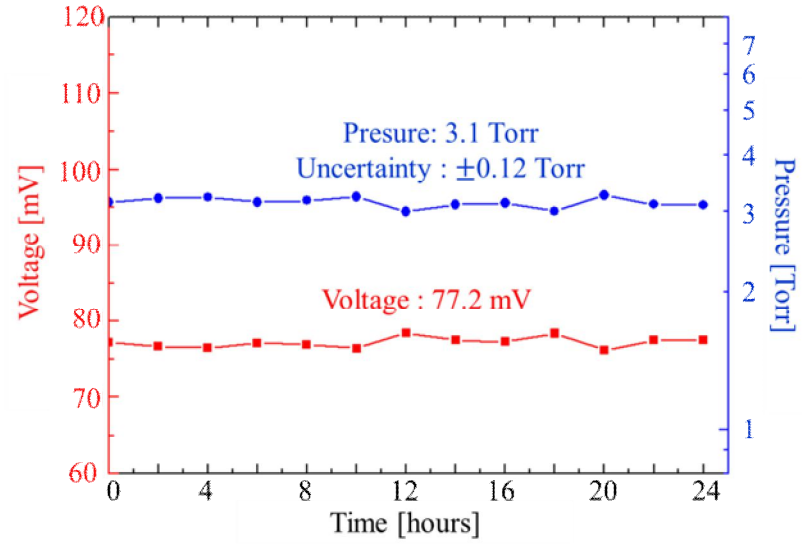
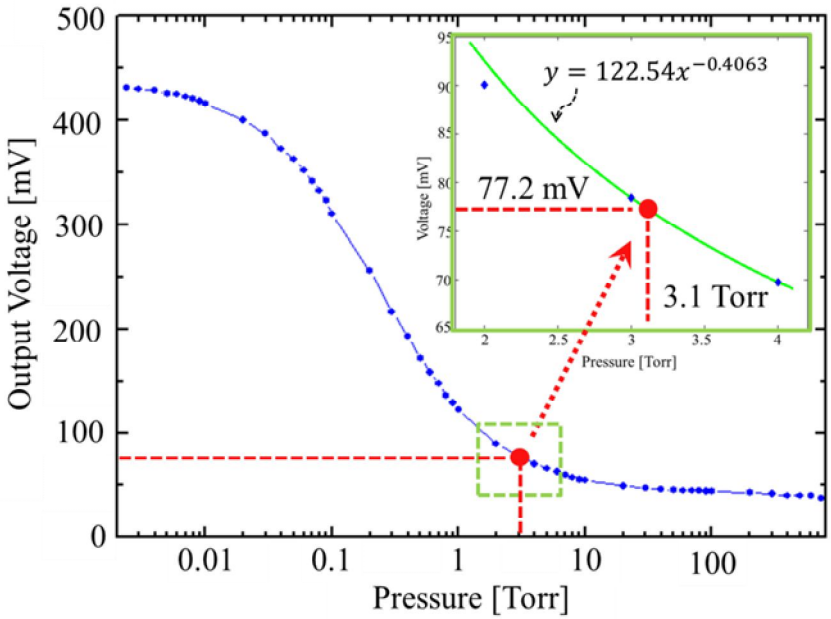


Figure 3.34. The resistance versus temperature of the Pirani resistor for measuring the TCR.

The vacuum level inside the package was measured with the Pirani gauge, which was integrated in the cavity. The output voltage of the Wheatstone bridge circuit was measured with the packaged Pirani gauge every 2 hr for 24 hr after packaging was completed. Figure 3.35 shows the measurement results including the output voltage as well as the corresponding vacuum level inside the packaging. The average output voltage was 77.2 mV with 1.1 mV uncertainty (Figure 3.35(a)). The corresponding vacuum level was extracted with a calibration curve. This corresponded to 3.1 Torr with $\pm$0.12 Torr uncertainty (Figure 3.35(b)). There was also no voltage drop during the 24 hr. This result shows that there was no leakage after packaging. The vacuum level during the packaging process was less than 5×10^{-5} Torr. A lower vacuum level than the packaging process could be caused by outgassing from the glass and other materials [71, 84].



(a)



(b)

Figure 3.35.(a) The variation of output voltage and corresponding vacuum level for 24 hr, and (b) the vacuum level in the packaging

3.4.1.6 Uncertainty analysis

The uncertainty of the vacuum level for 24 hr was not considered as the variation in vacuum level inside the package. The uncertainty of the measurement results could be caused by other sources and were analyzed.

The noise of the measurement system could cause uncertainty in the measurement results. Figure 3.36 shows the variations of the measurement results for the vacuum level and input voltage at every 1 min for 1 hr. The measurement results show that the uncertainty of the vacuum level was ±0.13 Torr, which was similar with that for 24 hr. This result shows that the uncertainty for long-term measurement of the vacuum level is not caused by the packaging leakage. Meanwhile, the variation in the input voltage was ±0.9 mV. The corresponding deviation of the vacuum level was calculated to be ±3 mTorr much smaller than the measured value. Furthermore, the time variation in the vacuum level did not match with that of the input voltage. Those results demonstrate that deviation in the input voltage was not the major source of the measurement uncertainty.

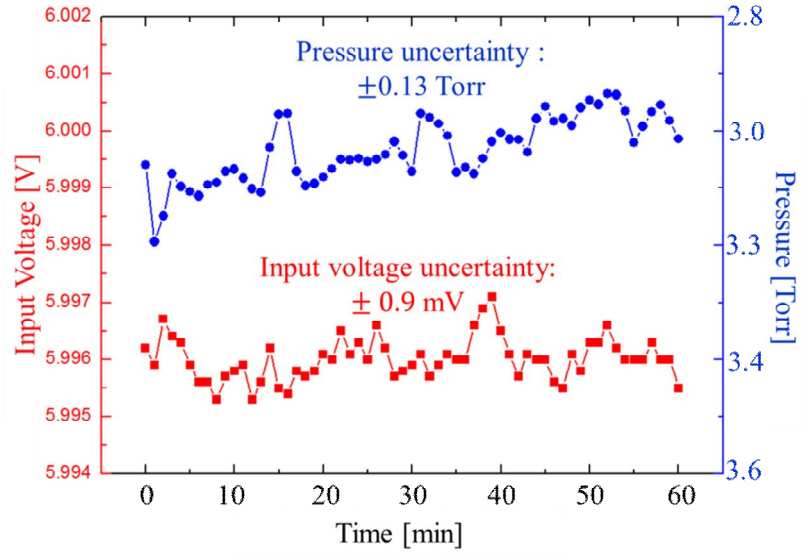


Figure 3.36. The measurement result of the variation of the input voltage and the vacuum level for 60 min.

The temperature may affect the output voltage of the Wheatstone bridge circuit. As the temperature varies, the resistance of the Pirani resistor also varies along with the TCR and the output voltage changes as well. The measured TCR of the Pirani resistor was 1.5×10^{-3} /K (Figure 3.34). During vacuum level testing, ambient temperature was 294.8 K with ±3 K uncertainty and the corresponding uncertainty in resistance was ±121.4 mΩ (Figure 3.37). The deviation of the temperature was small since the measurement was done in a cleanroom with a constant temperature. However, the calculated uncertainty of the vacuum level according to the variation in temperature was ±0.14 Torr.

This result demonstrates that the temperature deviation was the major source of the measurement uncertainty of the vacuum level. The uncertainty may be suppressed by adding the compensation circuit of the temperature variation.

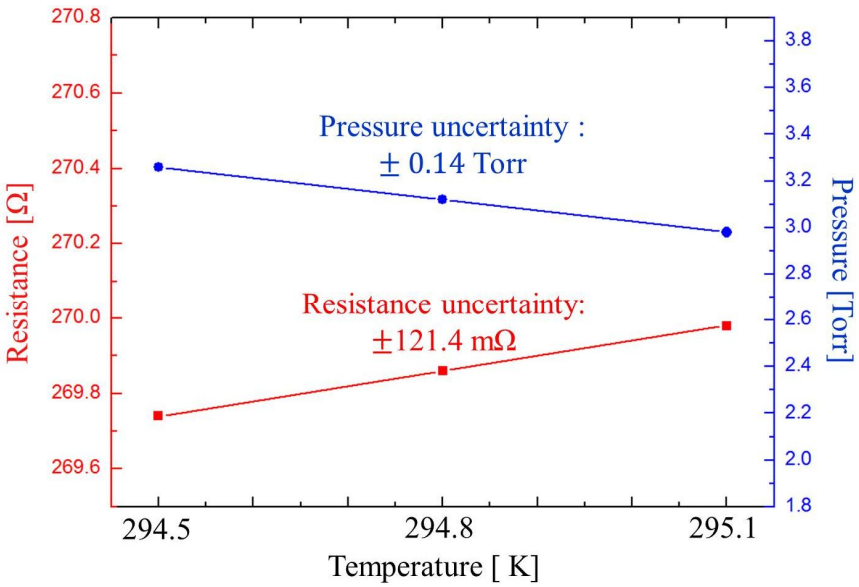


Figure 3.37. The calculation result about the effect of the temperature deviation on the variation of the resistance of Pirani resistor as well as the pressure in the packaging based on the measured TCR

3.4.2 Overall process

Abbreviated fabrication process is shown in Figure 3.38. Silicon wafer was bonded with intermediate layer of Cr/Au to silicon through-via substrate. Fabrication of vertical combs and silicon rim was then followed by anodically bonding to bottom glass wafer. Silicon through-via substrate was prepared by glass reflow process and silicon dry etching.

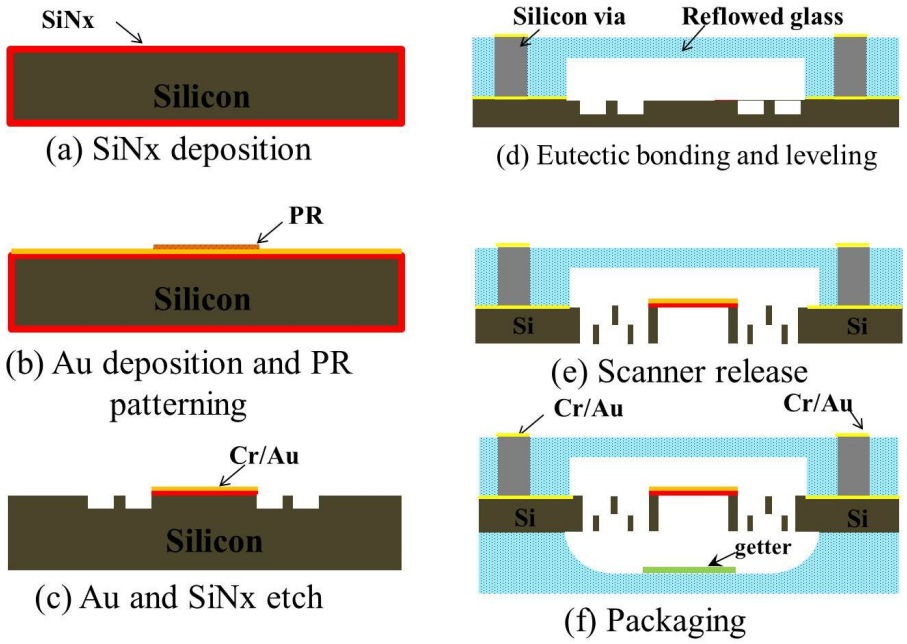


Figure 3.38. Abbreviated fabrication process of silicon nitride scanner and wafer-level vacuum

3.4.3 TWIn with deep cavity

Figure 3.39 shows an abbreviated fabrication process of silicon through-via with deep glass cavity. First, Cr coats a low-resistance silicon wafer by thermal evaporation method to be used as an etching mask of silicon. Then, photoresist (AZ4330) is removed only in the region where the silicon is etched in next step (Figure 3.39(a)). The wet etching of Cr by a mask of the photoresist as well as dry etching of the silicon by a mask of Cr is followed (Figure 3.39(b)). Etching depth at this step determines the thickness of the glass cover at the top of the glass cavity. Etching masks are removed by cleaning (Figure 3.39(c)). Then, Cr deposition is followed by photolithography (Figure 3.39(d)). Cr is then wet etchied, and silicon is dry etched (Figure 3.39(e)). After removal of the etch mask, siliocn wafer is anodically bonded to a borosilicate glass in vacuum condition ($<6\times10^{-3}$ Torr) (Figure 3.39(f)). The vacuum condition is essential for the reflowed borosilicate glass to be sucked in the cavity of the silicon wafer. The reflow process of glass is carried out in a furnace (Figure 3.39(g)). Chemical-mechanical polishing in both sides of the wafer for wafer planarization defines thickness of TWIn substrate (Figure 3.39(h)). At this time, silicon through-via is exposed in both sides of wafer.. Cr deposition and photolithography are followed by Cr wet etch (Figure 3.39(i)). Finally, silicon is etched to form deep cavity, and etch masks are removed by cleaning (Figure

3.39(j)).

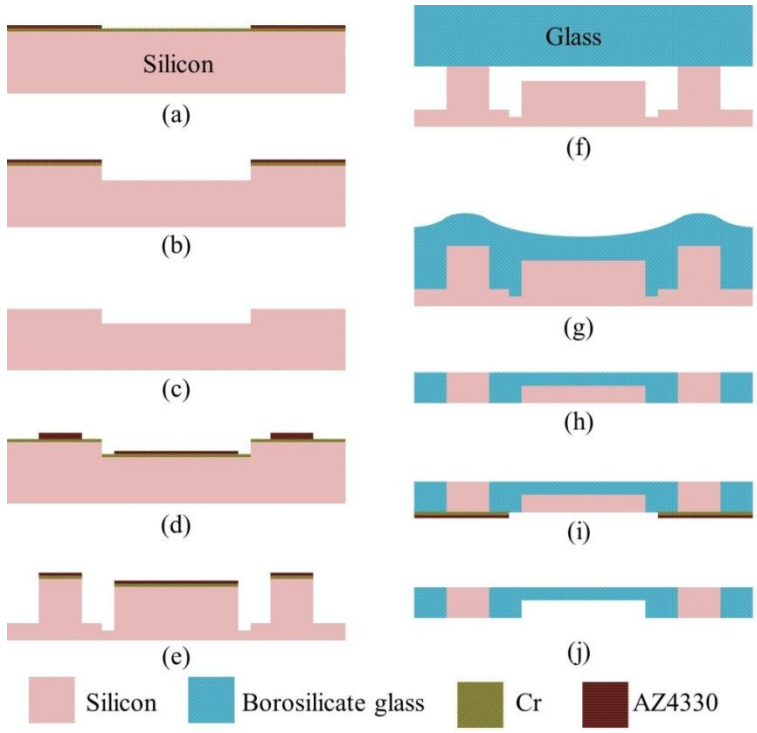
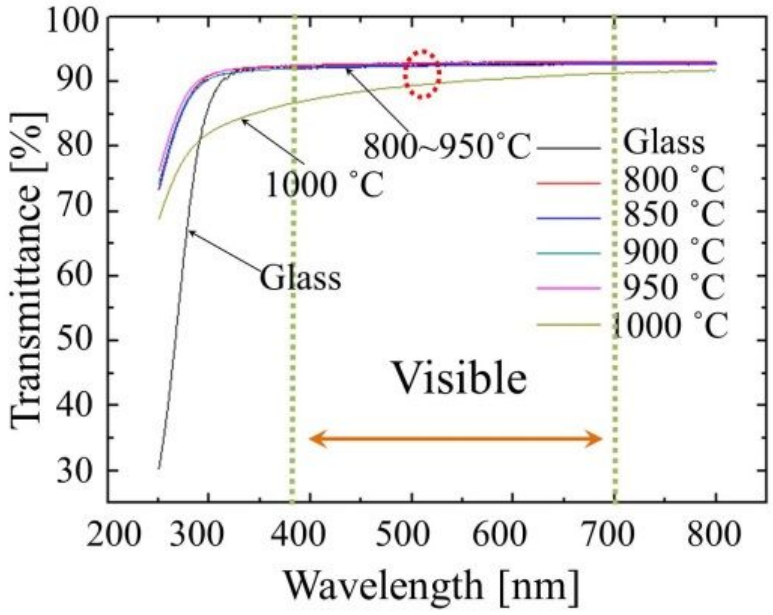


Figure 3.39. Process flow of deep-cavity-integrated TWIn substrate

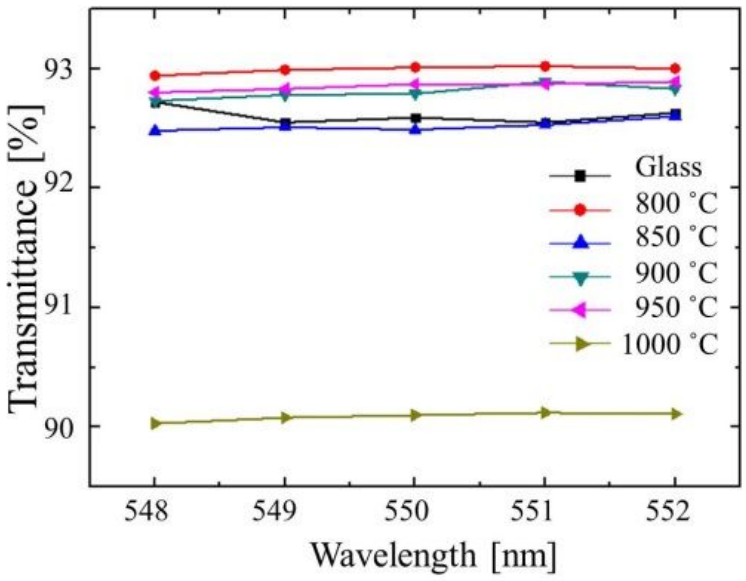
In order to achieve optically transparent cavity of silicon through-via substrate, optimization of proposed fabrication process was required. Major factors affected transparency of cavity were the smooth surface of silicon cavity in silicon-etching step (Figure 3.39(b)) and the transparency of glass after the reflow process and CMP (Figure 3.39(h)). Each factor was investigated.

3.4.3.1 Thermal reflow

Thermal reflow process achieves 3-D structure of glass by increasing the temperature in furnace up to transition point and filling into the silicon mold. During reflow process, glass crystallization can be occurred and deteriorates the transparency of reflowed glass. Therefore, optimization of reflow process has been required for optically transparent window in silicon through-via substrate. Possible factors affecting the transparency in reflow process was reflow time and reflow temperature. First, effect of reflow time has been investigated. After anodically bonded to silicon, glass wafer was reflowed in temperature ranged from 800℃ to 1100℃. Reflow time was fixed to 3 hr. Reflowed glass wafer with thickness of 200 μm was then remained by CMP. Transmittance of reflowed glass was measured using UV/VIS/NIR spectrophotometer (Cary 5000, Agilent Technologies). Figure 3.40(a) shows measurement results, and Figure 3(b) is magnified image of dotted red circle in Figure 3.40(a). There was not a considerable decrease of transmittance in reflow temperature of 800~950 ˚C. However, it significantly reduced in the reflow temperature of 1000 ˚C. Average transmittance in visible spectrum (390-700 nm) was summarized in Table 3.3.



(a)



(b)

Figure 3.40. Transmittance of reflowed glass in different reflow temperature

Table 3.3. Transmittance test results as reflow temperature in reflow time of 5 hr in visible spectrum

Reflow temperature	800 ˚C	**850 ˚C**	900 ˚C	950 ˚C	1000 ˚C	Borosilicate glass
Transmittance (average)	92.93 %	**92.45 %**	92.68 %	92.79 %	89.65 %	92.57 %

Compared with bare borosilicate glass, transmittance of reflowed glass in temperature of less than 950℃ was not changed. However, Transmittance in glass reflowed in 1000℃ reduced about 3 %. This can be caused by larger grain size formed during cooling step. In Figure 3.40(a), transmittance of glass reflowed in 1000℃ became higher as the wave length increased. This can be explained the large grain size of re-solidified glass. In scanning electron microscope (SEM) images, large grain size in glass reflowed in 1000℃ can be observed in Figure 3.41

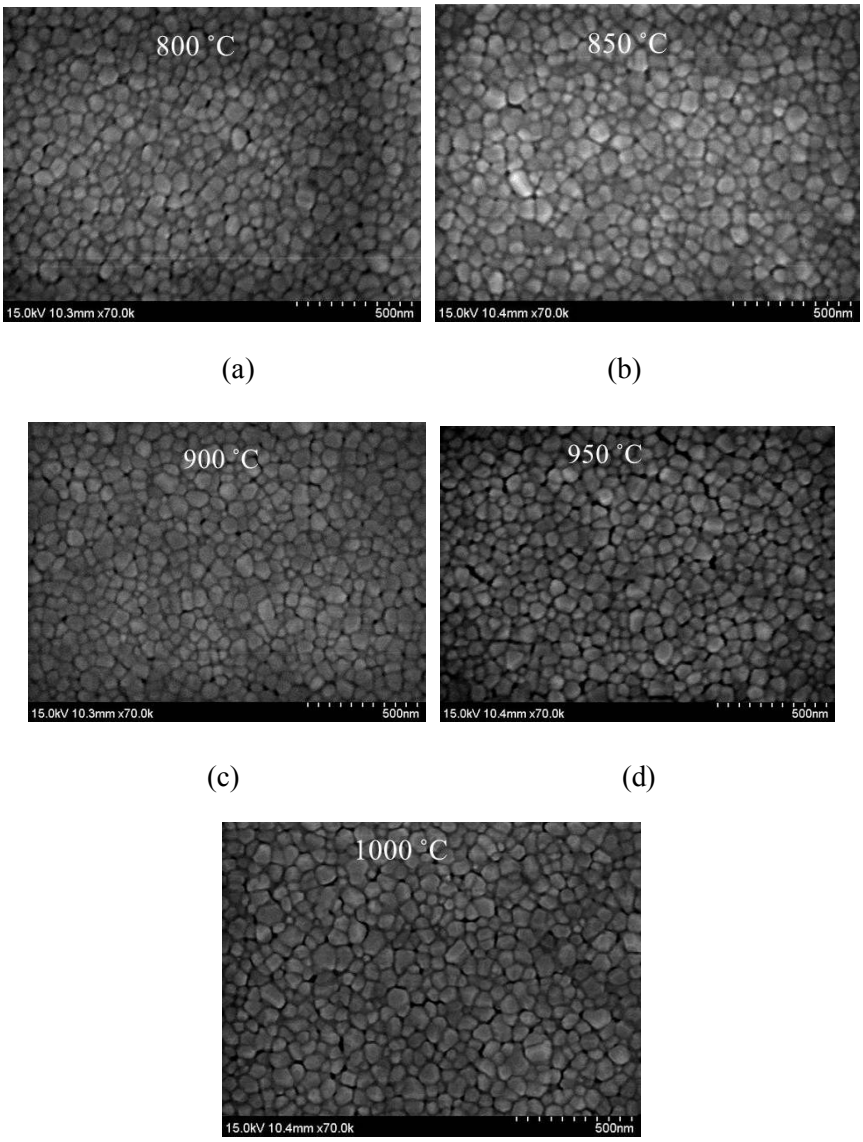


Figure 3.41 SEM images of reflowed glass in different temperature

Effect of reflow time on the transparency of reflowed glass was investigated as well. Borosilicate glass was reflowed in temperature of 900℃ for various reflow time ranged from 3 to 11 hr. Measured transmittance in each case was

plotted in Figure 3.42. Even though transmittance was not changed remarkable in the reflow time of 5 hr or less, it significantly decreased as reflow time increased in more than 7 hr. Table 3.4 summarizes averages of transmittance in visible spectrum according to the reflow time.

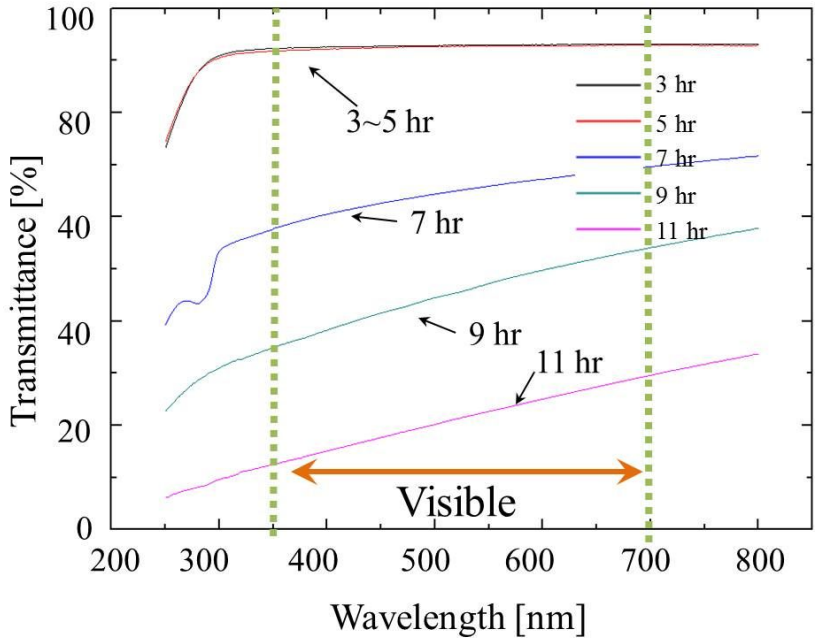
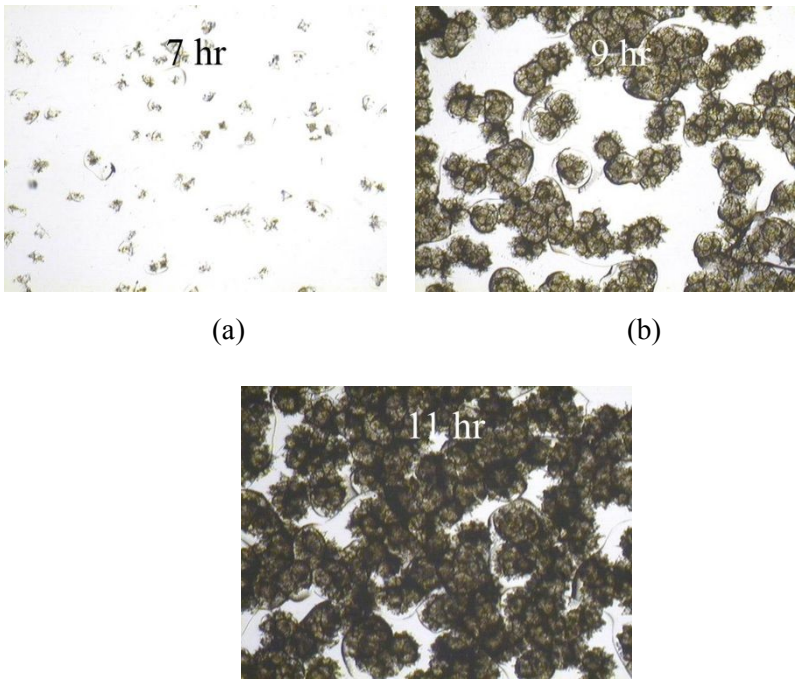


Figure 3.42. Transmittance of reflowed glass according to reflow time

Table 3.4. Transmittance test results as reflow time in reflow temparture of 850˚in visible spectrum

Reflow time	3 hr	**5 hr**	7 hr	9 hr	11 hr	Borosilicate glass
Transmittance (average)	92.07 %	**91.84 %**	63.14 %	44.56 %	21.04 %	92.57 %

Decrease of transmittance was due to the generation of glass crystallization which was optically opaque. Figure 3.43 shows the microscope images of reflowed glass. Area occupied by opaque crystallization was increased as reflow time increased. Crystallization was not observed in the glass reflowed below 5 hr. These results implied that main factor affecting transparency of reflowed glass in reflow process was reflow time. Based on these results, we have chosen the reflow process of 900℃ and 5 hr as optimized condition as higher temperature and longer time of the reflow process ensured successful filling of reflowed glass into the mold unless the crystallization was not occurred.



(a) (b)

(c)

Figure 3.43. Microscopic images (× 5) of crystallization in the reflowed glass in different reflow time with reflow temperature of 900℃.

3.4.3.2 Smooth surface

Not only the transparency of the reflowed glass, but also the surface roughness of etched silicon (Figure 3.39(b)) affect the optical transmittance of the cavity in silicon through-via substrate because silicon surface was used as mold of glass cavity in reflow process. Therefore, roughness of etched silicon was required to be less than 1/10 of visible wavelength. Conventional method for smooth surface of etched silicon has been the wet etching using KOH or TMAH. However, we could not reproduce the smooth surface with reported

process due to low repeatability of Si wet etching technique. Instead of wet etching, dry etching using deep reactive ion etch (DRIE) was applied to fabricate trenches in silicon for high repeatability, high etching rate and uniformity of etching depth throughout a wafer of dry etching. Figure 3.44 shows dry etching results of silicon with different condition. Compared to the Bosch process (Ra=67 nm), dry etch using SF6 plasma successfully offered smooth surface (Ra=0.42 nm) enough to be used for optical component (<λ/10).

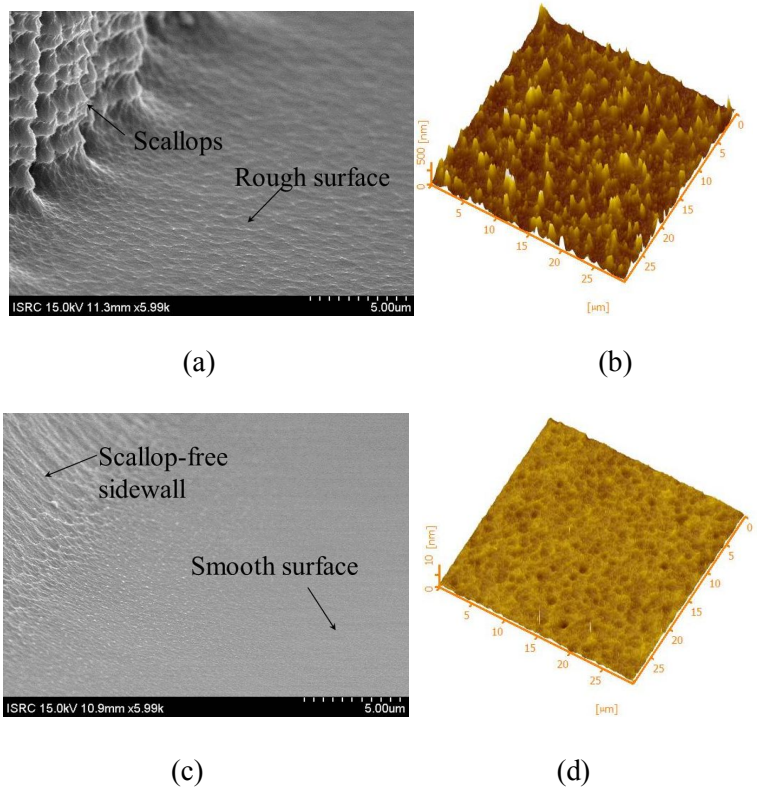
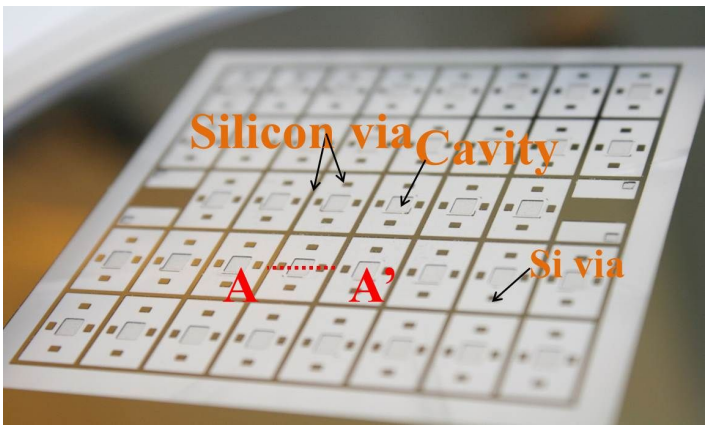


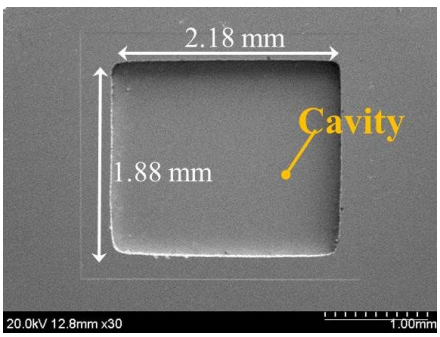
Figure 3.44. SEM and AFM images of dry-etched silicon using (a-b) Bosch process and (c-d) SF6 plasma only

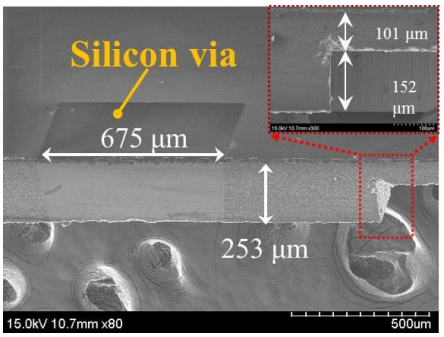
3.4.4 Fabrication results

Using optimized process, the silicon through-via substrate with optically transparent deep-cavity was successfully fabricated (Figure 3.45). Figure 3.45(a) shows the integration of silicon through-vias and deep cavity. Measured dimensions of cavity were 2.18 mm × 1.88 mm × 152 μm (W×L×H) (Figure 3.45(b)-(c)).



(a)





(b) (c)

Figure 3.45. (a) TWIn substrate with deep cavity, (b) SEM image of cavity, and (c) cross section along AA'

With the silicon through-via substrate, SiN microscanner was successfully packaged in wafer level as shown in Figure 3.46. A single chip was separated using dicing saw and attached to the PCB (Figure 3.47).

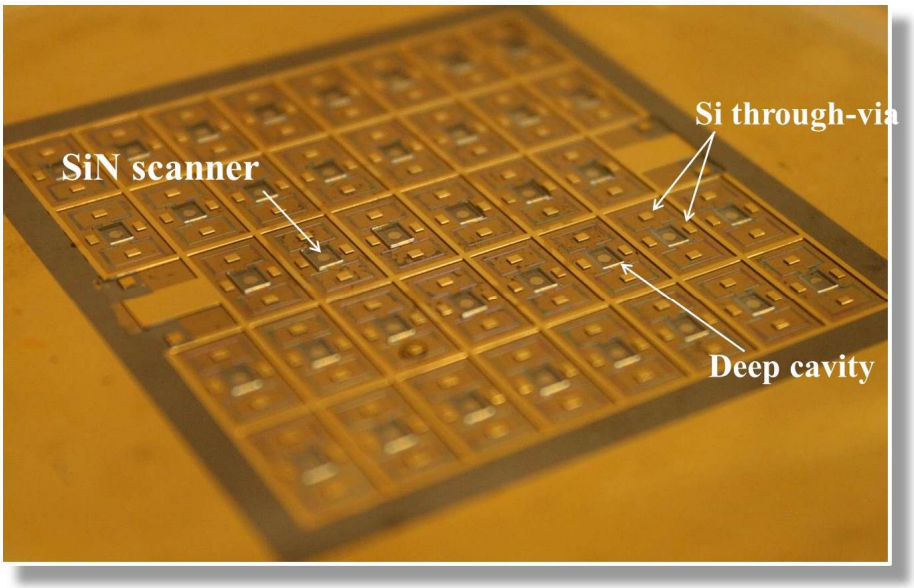


Figure 3.46. SiN scanner packaged using TWIn substrate in wafer-level

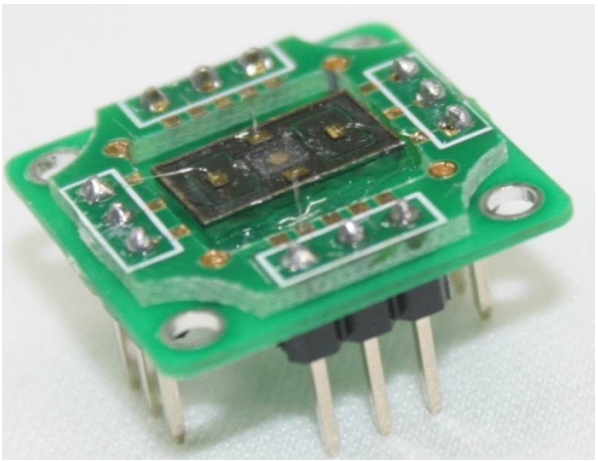


Figure 3.47. Separated SiN scanner which was attached to PCB

.3.5 Conclusion

This chapter proposed and demonstrated fabrication process of SiN scanner and wafer-level vacuum packaging. SiN mirror plate was successfully formed using dry etching of silicon due to etching selectivity to silicon. Silicon rim and vertical comb actuators attached to the edge of silicon rim were formed successfully as well. Fabrication techniques for wafer-level vacuum packaging using glass cap and TWIn substrate were developed. SEM images demonstrated successfully encapsulated SiN scanner.

Chapter 4

Characterization of SiN scanner and vacuum packaging

This chapter contains characterization of fabricated SiN scanner. Optical characteristics of SiN mirror plate including roughness, flatness and reflectivity are measured. Dynamic characteristics in atmosphere are investigated. Optical performance and vacuum packaging properties are measured. Reliability test of packaging are done as well.

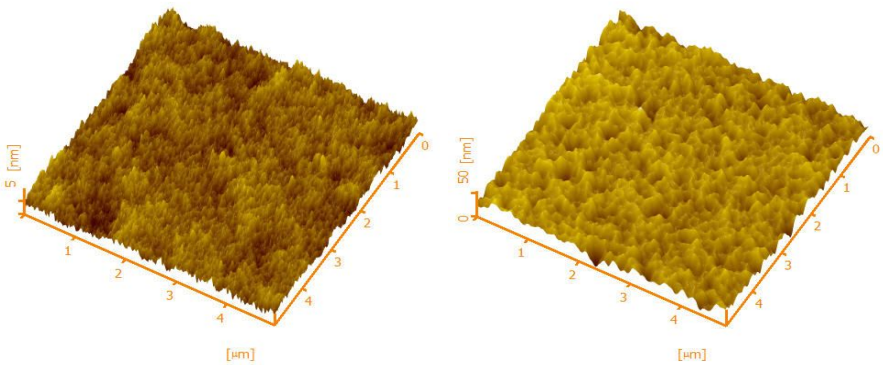
4.1 Introduction

In previous section, we proposed fabrication process of proposed SiN scanner and wafer-level vacuum packaging. This chapter deals with measurement results of optical characteristics of fabricated SiN scanner and optical components such as glass cap and TWIn substrate. Section 4.2 deals with characteristics of non-packaged SiN scanner. Section 4.3 shows optical measurement results of packaged SiN scanner using the glass cap. Section 4.4 deals with measured performance of vacuum-packaged SiN scanner with TWIn substrate. Conclusion is dealt in Section 4.5.

4.2 Characterization of SiN scanner

4.2.1 Surface roughness and reflectivity of SiN mirror plate

An optical reflective surface requires a roughness of less than 1/10 of the visible spectrum. The fabricated roughness of the silicon nitride thin-film mirror plate was measured using an atomic-force microscope (AFM). Figure 4.1 shows the AFM measurement results. Silicon nitride film deposited by LPCVD had a roughness of 0.89 nm. In contrast, the roughness of the fabricated mirror plate increased to 4.88 nm. Degradation of the surface smoothness was caused by stain which occurred during the release step of the wet-etching process, including the removal of the photoresist and the Cr mask. However, the roughness was less than 1/10 of the visible spectrum. Hence, the fabricated mirror plate was deemed sufficient for use as a reflective surface.



(a) (b)

Figure 4.1. AFM images of the SiN mirror plate: (a) SiN thin film (Ra= 0.89 nm) and (b) Cr/Au reflective metal (Ra=4.88 nm)

The reflectivity of the Cr/Au metal film was measured using a UV/VIS/NIR spectrometer (Lambda 95, PerkinElmer). The measurement results shown in Figure 4.2 demonstrate reflectivity in the visible spectrum is 40.2 % and 105.4% in minimum and maximum value, respectively. Higher reflectivity could be achieved by Al metal film.

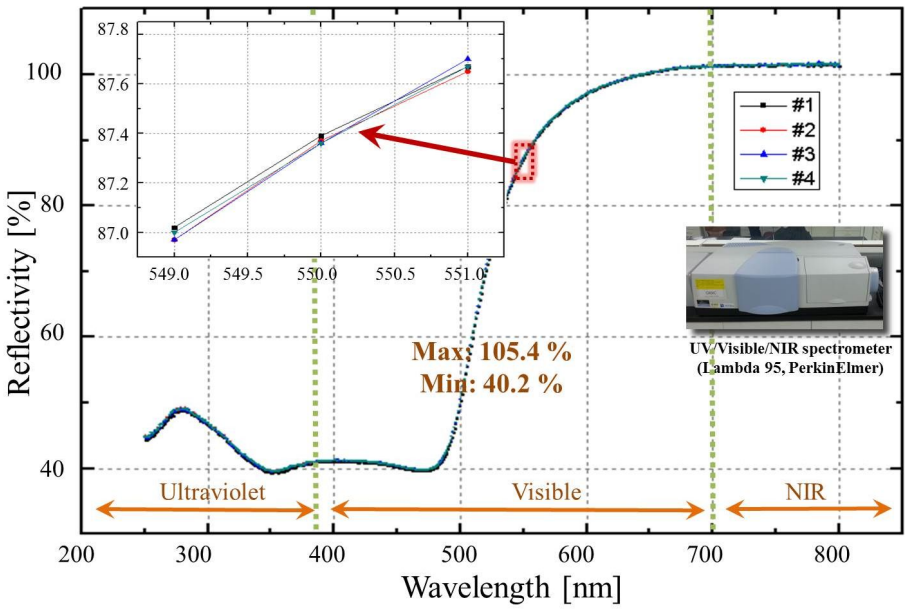


Figure 4.2. Reflectivity of Cr/Au reflective metal

4.2.2 Flatness of silicon nitride mirror plate

Deformation of the silicon-rim-reinforced silicon nitride mirror plate was measured by a LED-light interferometer (Zygo Co). Figure 4.3 shows measurement setup and Figure 4.4 is measured deformation of reference scanner. Table 4.1 summaries the measurement results and the evaluated ROC in all types. The maximum deformation in the mirror plate increased as the width of the silicon rim decreased, as expected. All types had a ROC larger than 300 mm, which was the minimum value required [85]. Simulated deformation results suggest that the residual stress of the fabricated mirror plate composed of SiN and Cr/Au increased from the initial stress formed during the LPCVD deposition of the SiN. Possible factors were the residual stress of the Cr/Au film and subsequent fabrication steps.

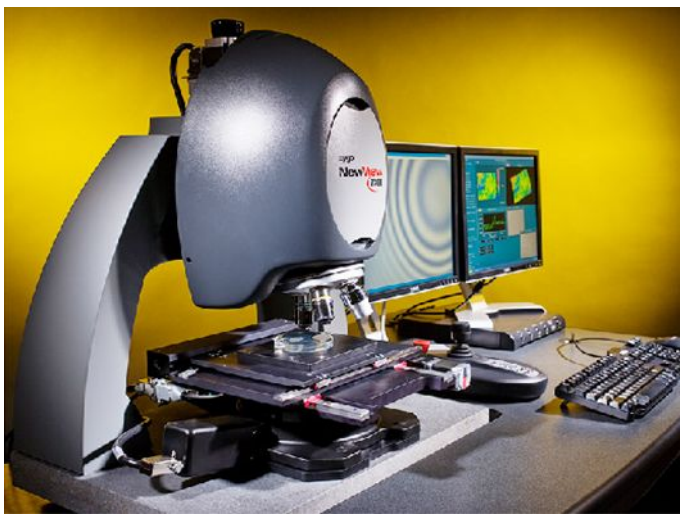


Figure 4.3. LED-light interferometer (Zygo Co.)

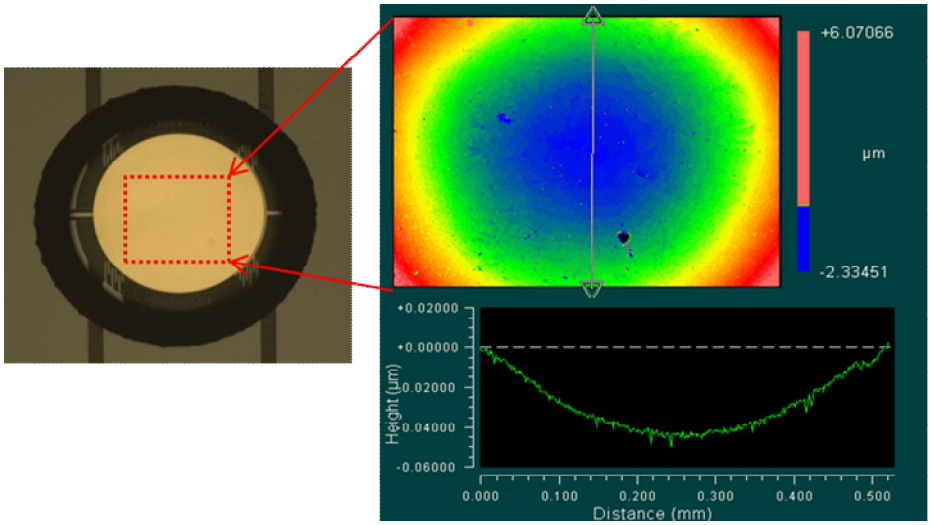


Figure 4.4. Deformation measurement of reference mirror using LED-light interferometer

Table 4.1. Measured ROC of each type of SiN scanner

Type	Maximum deformation [nm]	Radius-of-Curvature (ROC) [mm]	
		Simulation	Result
Si	λ/10 (41)	11910	3048
Rim20	7λ/10 (281)	806.5	444.8
Rim50	4.8λ/10 (194.1)	1136	644.0
Rim100	3.6λ/10 (145.1)	1574	861.5

4.2.3 Resonant frequency and optical tilt angle

The resonant frequency of the silicon nitride scanner was measured using a laser Doppler vibrometer (LDV). The frequency responses of each type are

illustrated in Figure 4.5. The measured values are shown in Table 4.2. The resonant frequencies were estimated from the fabricated dimensions, and the error from the measured values was less than 2%. The main factor which caused the difference between the design and measured resonant frequencies was the reduced spring width due to undercutting during the deep-reactive-ion etching of the silicon.

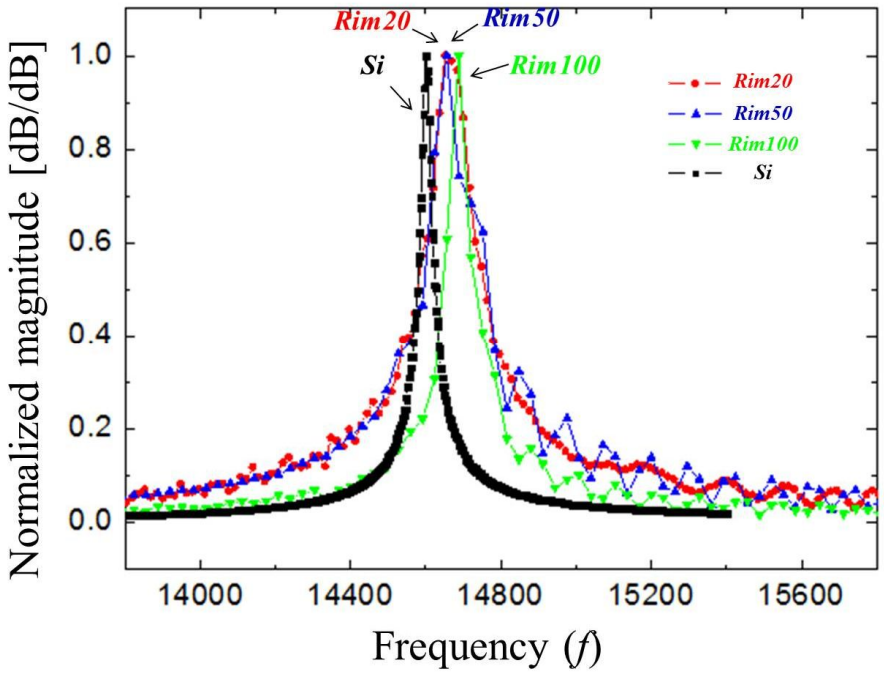
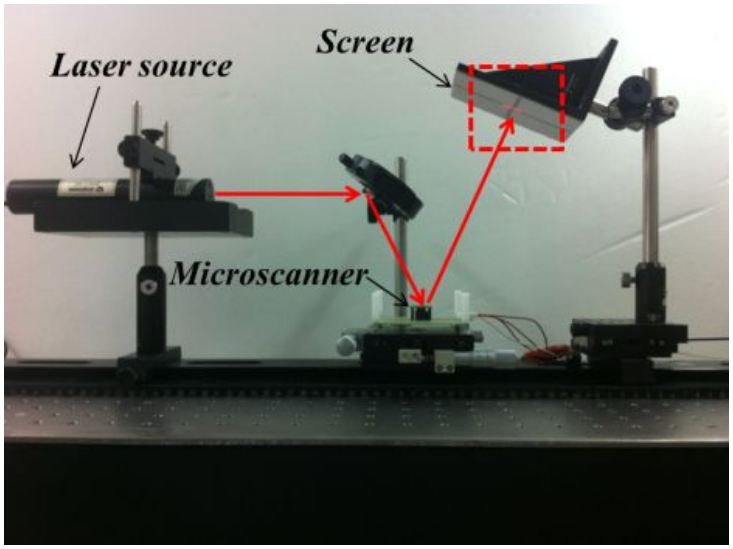


Figure 4.5. Frequency response of each types.

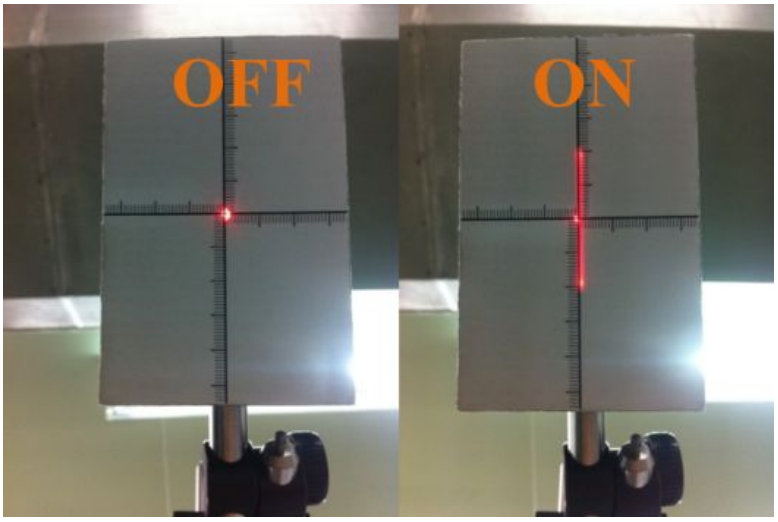
Table 4.2. Measured dimensions and resonant frequencies of each type

Type		Si	Rim20	Rim50	Rim100
f_o	Design	15 kHz			
	Estimated	14.86 kHz	14.94 kHz	14.85 kHz	14.90 kHz
	Measured	14.60 kHz	14.65 kHz	14.66 kHz	14.69 kHz
	Error	**1.75 %**	**1.94 %**	**1.28 %**	**1.41 %**

The optical tilt angle was measured as well. A sinusoidal signal was applied at the resonant frequency of the microscanner. Figures 4.6(a) and (b) respectively show the measurement setup and a magnified image of the screen in the ON and OFF states of the microscanner.



(a)



(b)

Figure 4.6. (a) Measurement setup and (b) magnified image of screen in ON and OFF state of microscanner

Figure 4.7 shows the measurement results of each type. At a similar resonant frequency, Rim20 showed a 41% decrease of the driving voltage compared to

the reference. This result demonstrated that the silicon nitride scanner decreased the driving voltage compared with conventional silicon micro-scanner.

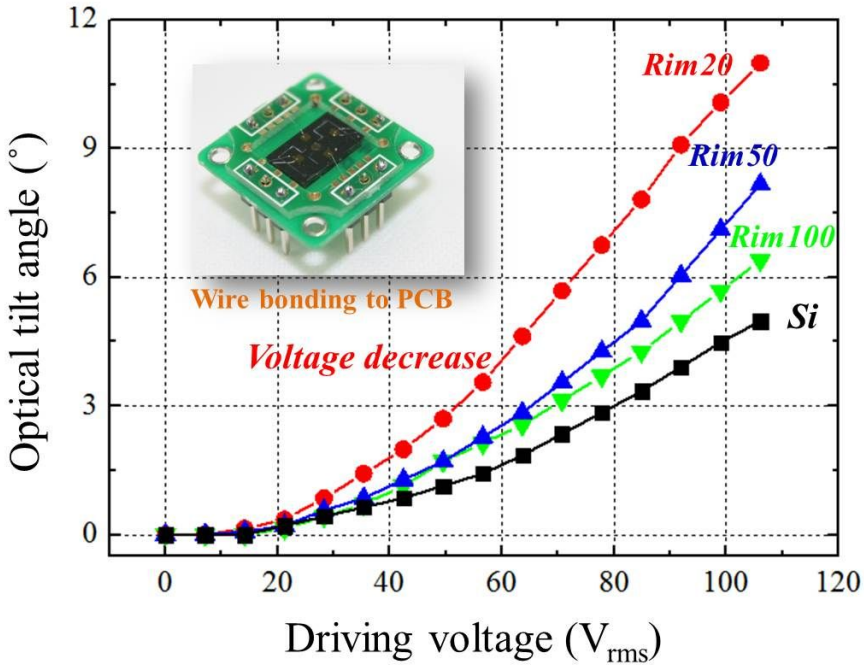


Figure 4.7. Measurement results of optical tilt angle according to driving voltage

4.2.4 Characteristics in vacuum condition

In order to measure the dynamic range of the silicon nitride microscanner, we measured the optical tilt angle under a vacuum condition. Figure 4.8 shows the measurement setup. A laser beam was used to light the microscanner in the vertical direction and the tilt angle was measured using a

protractor. The ambient pressure in the vacuum chamber was decreased by a turbo pump and a rotary pump connected to a bellows pipe.

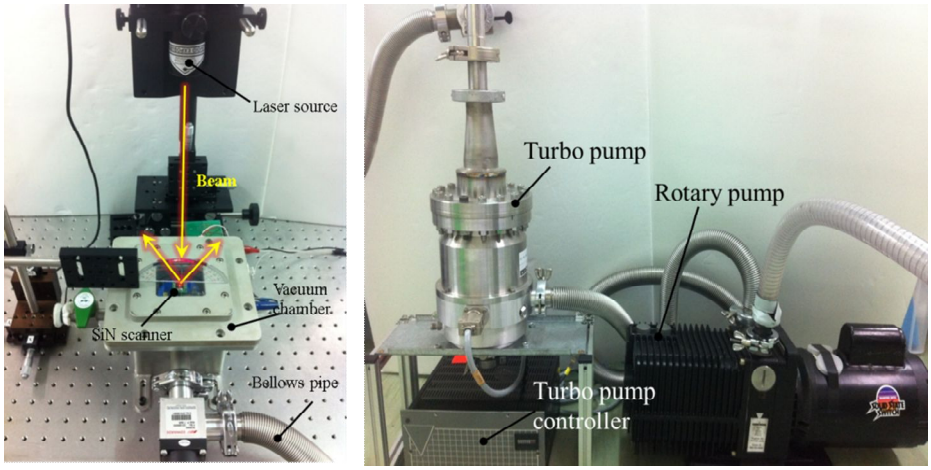
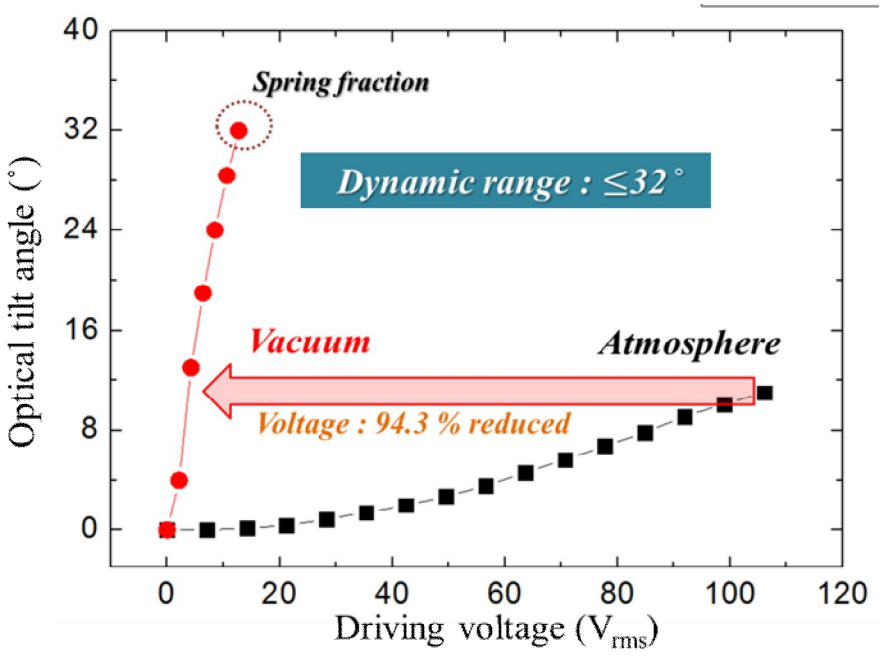


Figure 4.8. Measurement setup for operation of microscanner in vacuum condition

The measurement results are shown in Figure 4.9. The dynamic range is 32° in Figure 4.9(a). The optical tilt angle according to the driving voltage at 1.2 mTorr is shown in Figure 4.9(b). These results suggest that the proposed silicon nitride scanner has a large dynamic range of 32° compared to previously reported studies showing a range of 8 ° or less. The driving voltage decreased by 94.3% of that of scanner actuated in the atmosphere due to the increase of the quality factor.

(a)



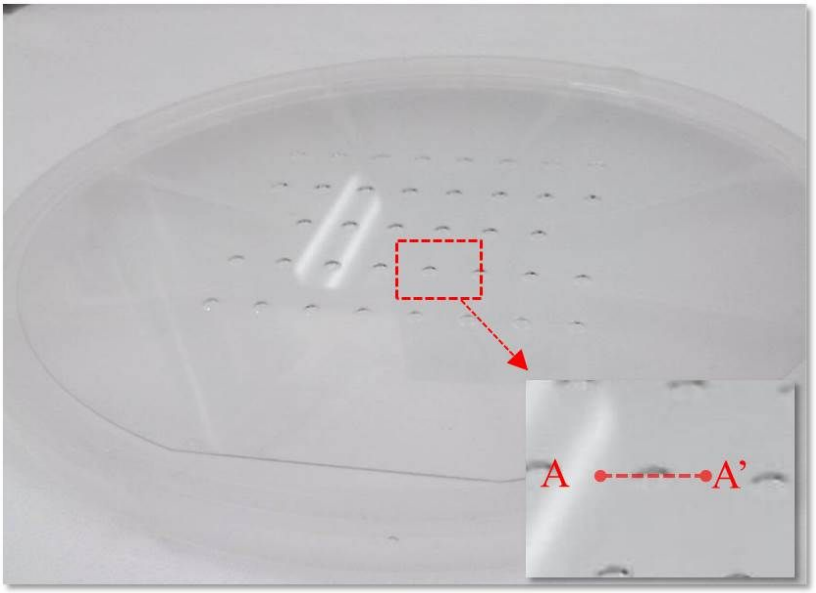
(b)

Figure 4.9. (a) Photograph of the operation of the microscanner and (b) measurement results of the optical tilt angle under a vacuum condition

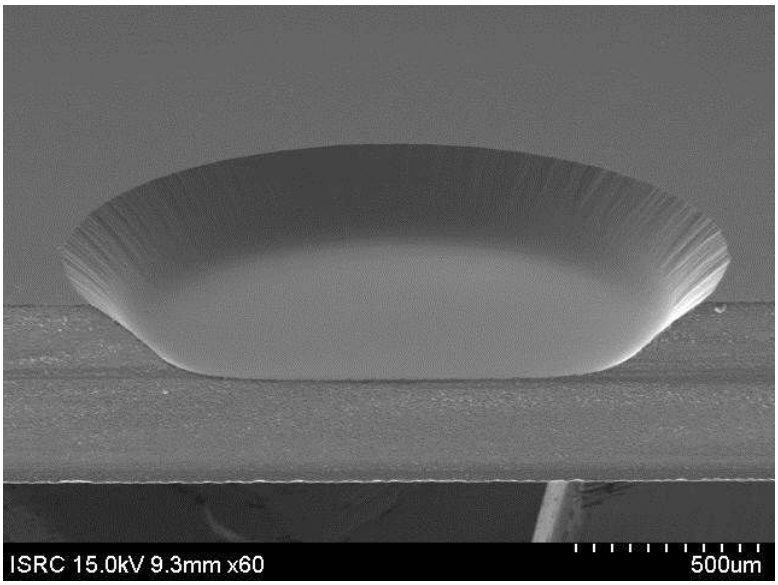
4.3 Characterization of SiN scanner packaged with glass cap

4.3.1 Glass cap with deep cavity

In top glass wafer, cavity provides space for actuaion of microscanner. Therefore, lare dynamic range needs deep cavity. In mirror plate of diameter of 1mm, optical tilt angle of 90 ° can be obtained with cavity of depth of 190 μm or more. Futhermore, cavity in top glass wafer requires excellent optical characteristics because laser beam path through the surface of cavity. Moreover, sufficient size of cavity in diameter was need for large tilt angle of cavity for avoiding distorsion of laser beam. Figure 4.10 shows top glass wafer with deep cavity fabricated by wet etching in HF solution. Depth and diameter of etched surface of cavity was measured to be 219 μm and 924 μm, respectively, and large enough to be used. Etched surface in cavity has no defect and pits.



(a)

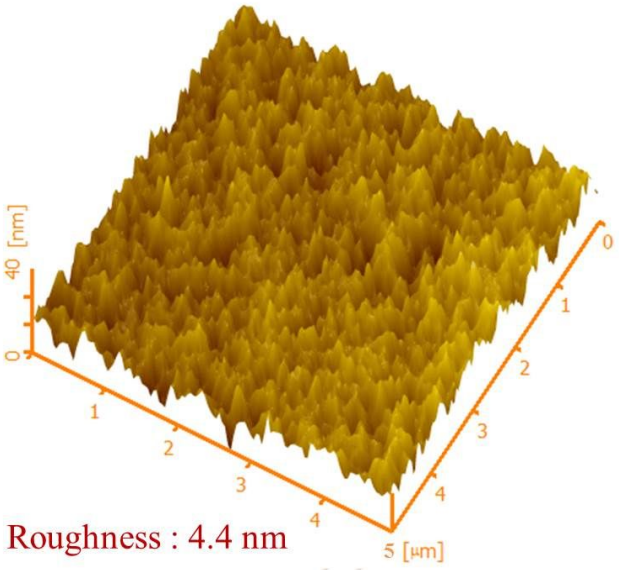


(b)

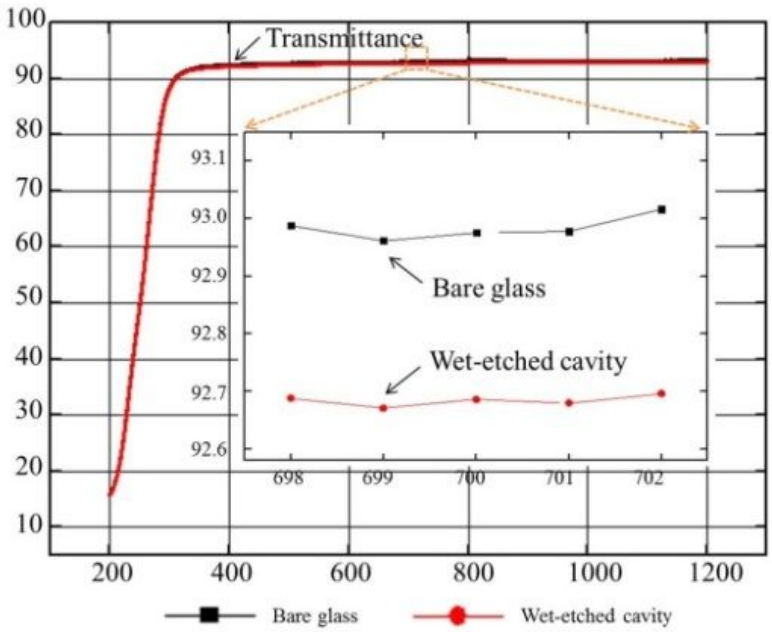
Figure 4.10. Fabricated top glass wafer: (a) photoraph of top glass wafer with deep cavity and (b) SEM image of cross-section along AA'

Optical characteristics of cavity has been confirmed. Surface roughness (R_a) was measured using Atomic Force Microscope (AFM) (Figure 4.11(a)). Measured value of 4.4 nm demonstrated smooth surface enough to be used as optical window because this was less than 1/10 of visible wavelength (390~700 nm). Optical transmittance was evaluated using UV/VIS/NIR spectrophotometer (Cary 5000, Agilent Technologies) as well. Compared with bare wafer, transmittance in visible wavelength of etched surface of cavity reduced 0.31% (Figure 4.11(b)). Difference was due to increased roughness of etched surface. However, error was less than 0.33% and transmittance was larger than 92% in visible spectrum.

I investigated optical image of filter paper seen through bare wafer and wet-etched cavity using microscope. Images through wet-etched surface were not significantly distorted comparing to bare wafers (Figure 4.12). This suggested deep cavity manufactured in glass cap was suitable for micro-devices requiring high solution of optical image.

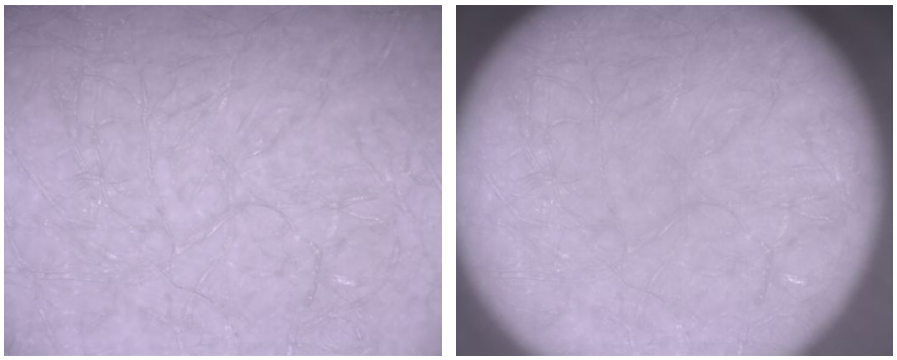


(a)



(b)

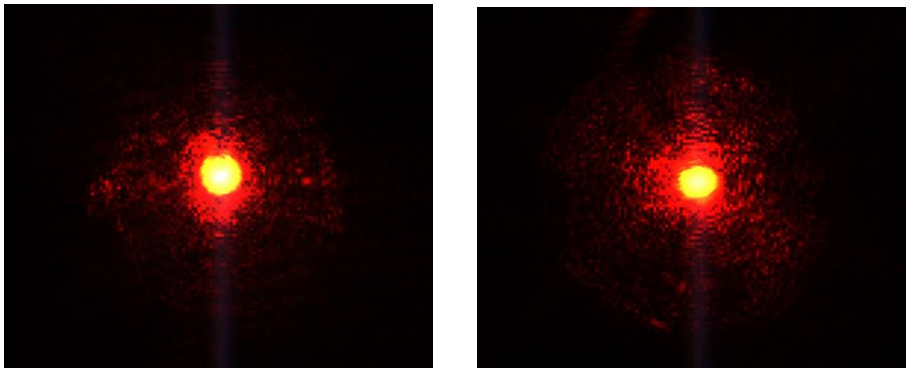
Figure 4.11. (a) AFM image of surface of cavity and (b) transmittance of cavity



(a) (b)

Figure 4.12. Microscopic images (100×) of filter paper through (a) bare glass wafer and (b) wet etched cavity. Black regions in the corners of (b) are results of etched trenches

The distortion of the laser ray was also investigated. Figure 4.13 shows no distortion of the laser signal when the ray of the laser passed through the fabricated cavity. A He-Ne laser with a wavelength of 633 nm and a CCD camera were used. The laser ray passed through a bare glass wafer as well as a deep cavity. Significant distortion was not detected



(a) (b)

Figure 4.13. CCD images of He-Ne laser spot passed through (a) the borosilicate bare glass, and (b) wet-etched deep cavity

Finally, the uniformity of the etch depth of the cavity was measured, as shown in Figure 4.14. The average value was 217.0 μm, though the standard deviation was only 0.46 μm. The maximum and minimum etching depths were 216.0 and 217.9 μm, respectively. High uniformity of the etch depth was preferred because it implied uniformity of fabrication and following optical properties of cavity.

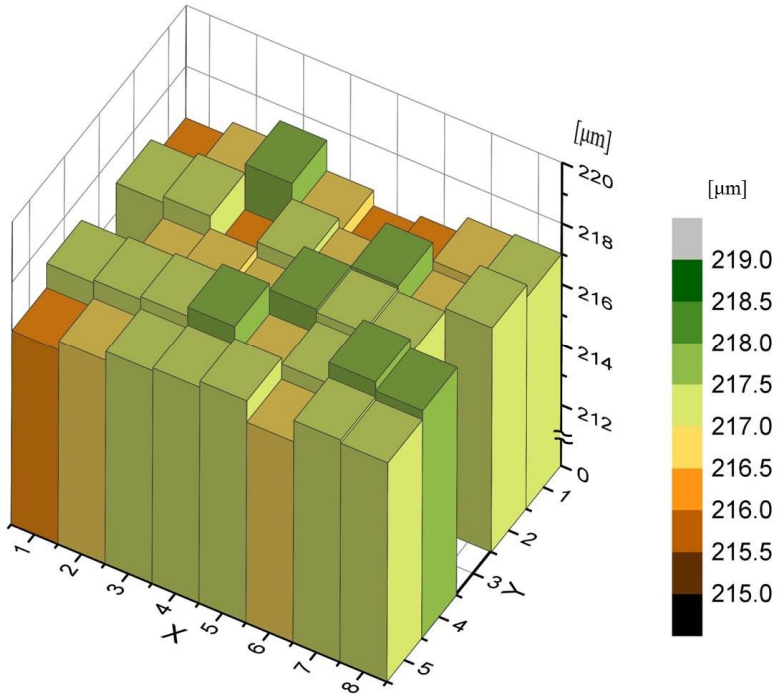


Figure 4.14. The etching depth of the deep cavity in the top glass wafer

4.3.2 Dynamic and optical characteristics

Performance characteristics of SiN scanner have been demonstrated by electrostatic vertical comb driver. Figure 4.15 shows frequency response of vacuum-packaged SiN scanner. High resonant frequency of 14.82 kHz implied realization of high speed scanning. Q factor was measured to be 3189, which is much larger than 216 of unpackaged one. Vacuum packaging decreases density of gas molecules around scanner and reduces energy loss due to viscous flow of gas molecules. Therefore, Q factor increases and low driving voltages can be obtained in vacuum packaging. For example, in

vacuum level of 12 mTorr, Q factor was approximately 12900 and optical tilt angle of 13 ˚ was achieved at driving voltage of 4.2 V_{rms}. However, Q factor was 266 and driving voltage of 106 V_{rms} was needed to tilt laser beam to 11 ˚. Q factor of fabricated SiN scanner was corresponded to vacuum level of 1.3 Torr which is 1/700 of atmosphere. High vacuum level expected to lower driving voltage of SiN scanner.

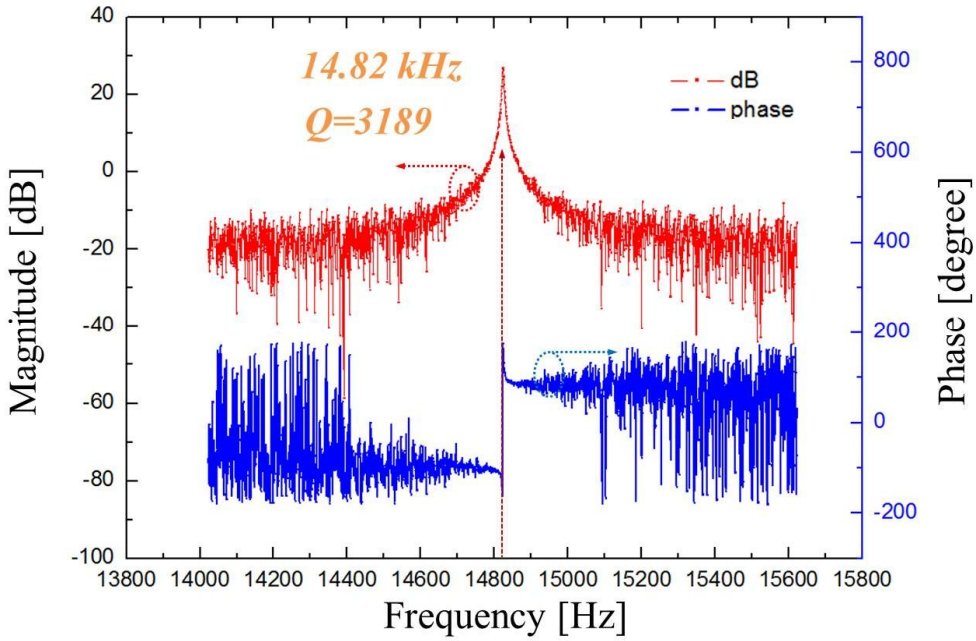
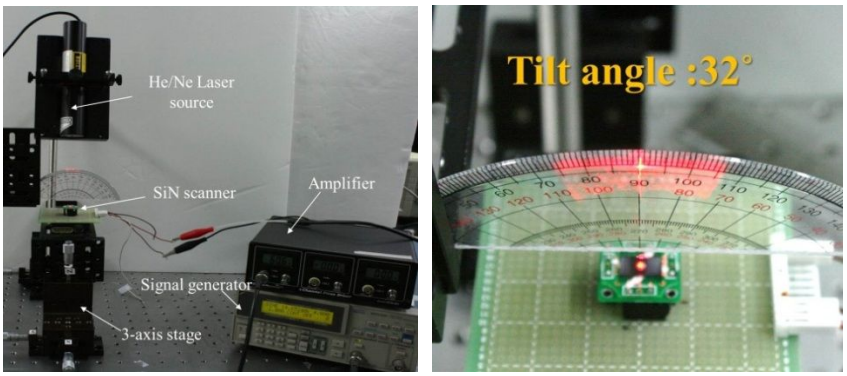
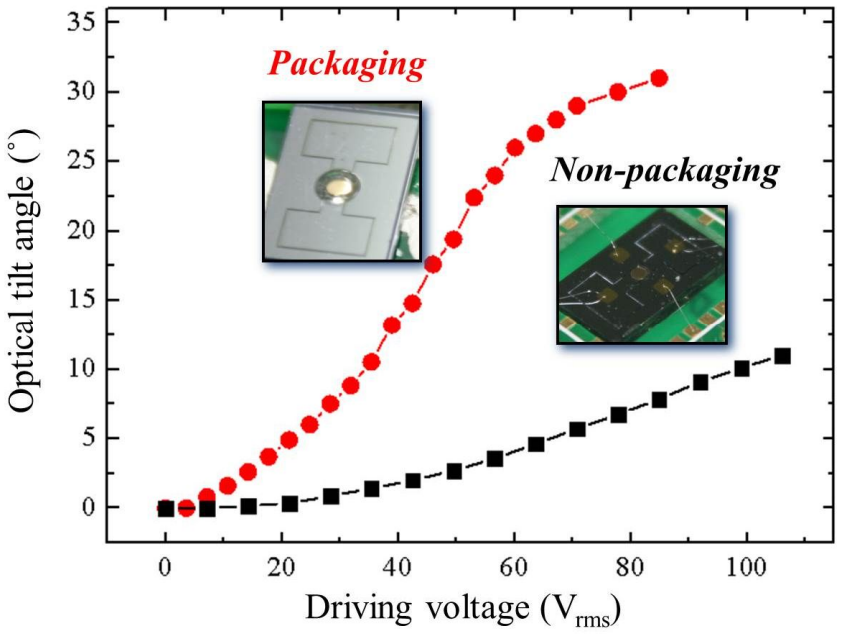


Figure 4.15. Frequency response of packaged SiN scanner



(a) (b)



(c)

Figure 4.16. Optical characteristic of scanner: (a) Measurement setup, (b) operation of SiN scanner in optical tilt angle of 32 ˚, and (c) measured curves of optical tilt angle according to driving voltage in packaged and non-packaged scanner

Large tilt angle of SiN scanner has been demonstrated using He/Ne laser source of 633 nm wavelength. Figure 4.16(a) and (b) shows measurement setup and optical tilt angle of 32 ° at 85 V_{rms}. Compared with previous works, dynamic range increased 4 times or more. Optical tilt angle according to driving voltage is plotted in Figure 4.16(c). Driving voltage was shrunk 70 % at the most compared with non-packaged SiN scanner.

Response time of SiN scanner has been measured. Displacement of steered laser ray by microscanner was observed using Position Sensitive Detector (PSD) (Figure 4.17(a)). Measured signal was compared with driving signal in oscilloscope and Figure 4.17(b) shows measurement result. Evaluated rising and falling time was 115 ms and 125 ms, respectively (Figure 4.17(c) and (d)). Considering several milliseconds of conventional scanners in atmosphere, response of SiN scanner was slow. This was due to reduced damping coefficient by vacuum condition in spring-mass-damping system. However, because being related only to turn-on and turn-off time of scanner, response time of about 0.1 sec has not deteriorated quality of optical scanning.

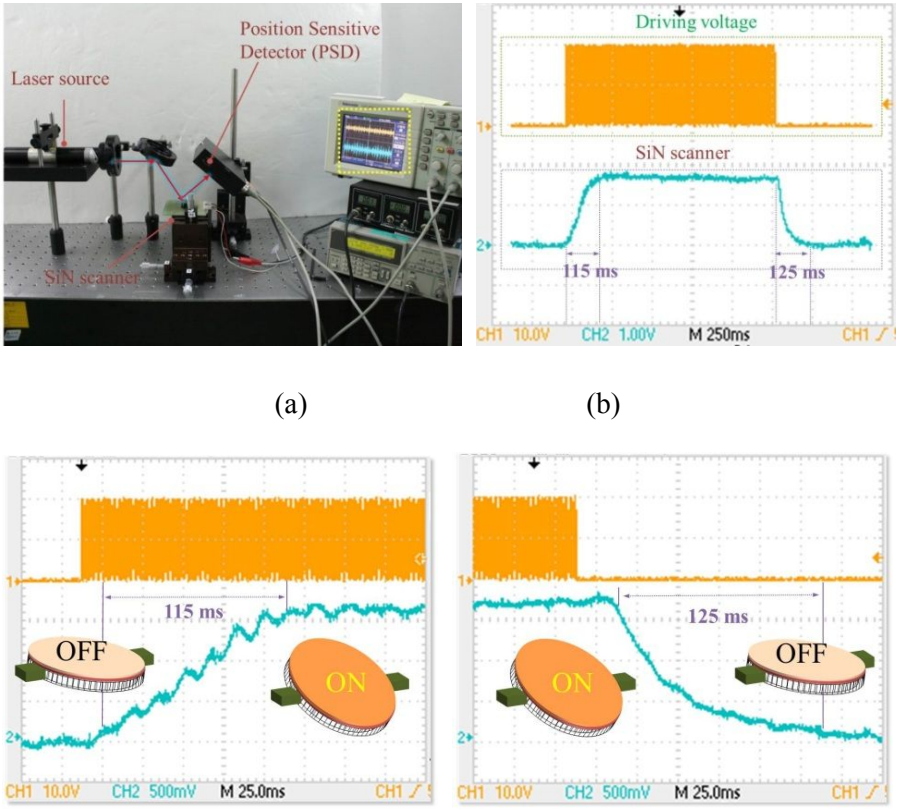
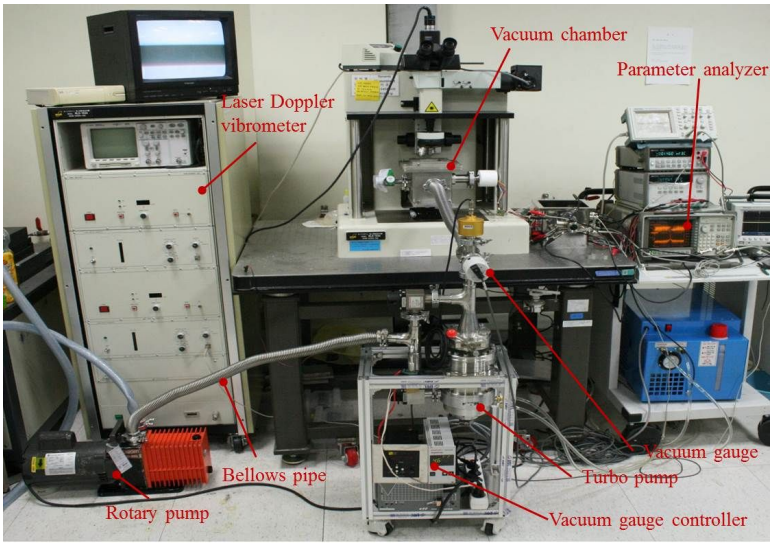


Figure 4.17. Response time: (a) Measurement setup, (b) measured response of scanner, (c) rising time, and (d) falling time

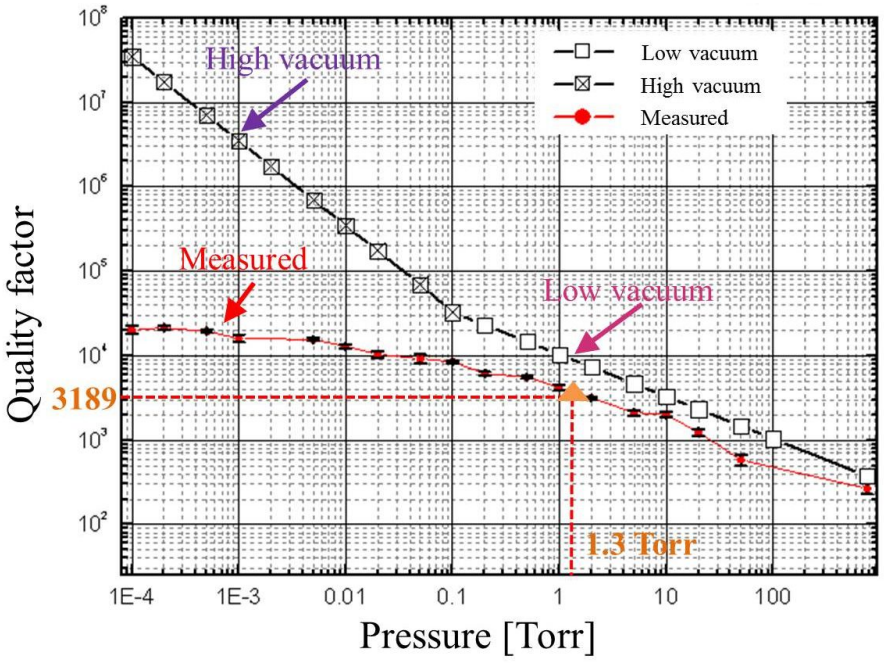
4.3.3 Vacuum level

Vacuum level of packaged SiN scanner has been investigated. The top glass wafer of SiN scanner was removed using HF solution and Q factor according to ambient pressure was measured. Figure 4.18(a) shows measurement system. Non-packaged SiN scanner was put into vacuum chamber, and vacuum level of chamber was controlled by rotary and turbo pump. Laser Doppler

Vibrometer (LDV) in combination with parameter analyzer observed Q factor in vacuum condition. In Figure 4.18(b), solid line of red and black plots measured and calculated values, respectively. In low vacuum level, measured curve matched calculated one well. Howver, in high vacuum level, Q factor has not increased and approached to about 3e4. Error between measurement and calculation values was caused by the transfer of dominant energy loss from viscous friction of gas molecules to the others including surface, support and thermoelastic damping loss in high vacuum level. Because accurate theory for modeling these losses has not been developed yet, investigation of converged value of Q factor of SiN scanner has been beyond our work. Q factor of vacuum-packaged SiN scanner corresponded to vacuum level of 1.3 Torr. Vacuum level during anodic bonding process for packaging the scanner was 5×10^{-4} Torr. Decrease of vacuum level was owed to outgas from glass and materials in packaged cavity. However, wafer-level vacuum packaging of this work accomplished vacuum level of 1/700 of atmosphere and Q factor of 12 times than that of the non-packaged scanner. Higher vacuum level can be obtained using commercial product of getter such as non-evaporable getter (NEG)



(a)



(b)

Figure 4.18. (a) Measurement setup and (b) measured curve of Q factor according to ambient pressure

4.3.4 Reliability/stability test of packaging

Along with high vacuum level, long-term maintenance of vacuum level has been important property of vacuum packaging of devices. Time variation of Q factor can be used for evaluating maintenance of vacuum level. Figure 4.19 shows variation of Q factors during 70 days. Average of Q factor was 3184 with uncertainty of 26. This corresponded to vacuum level of 1.3 Torr with ± 0.04 Torr uncertainty. This results implied that no leakage was detected during 70 days.

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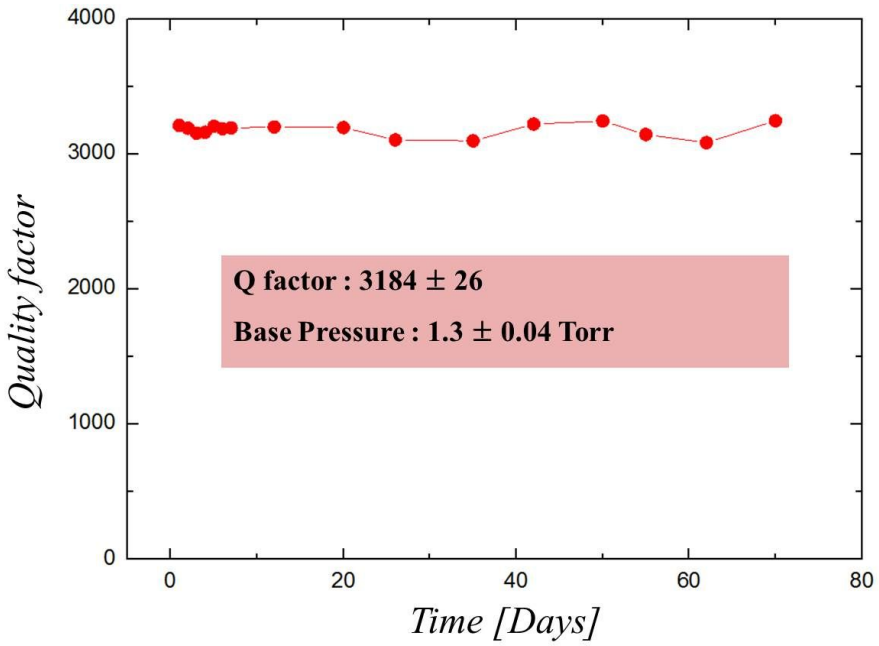
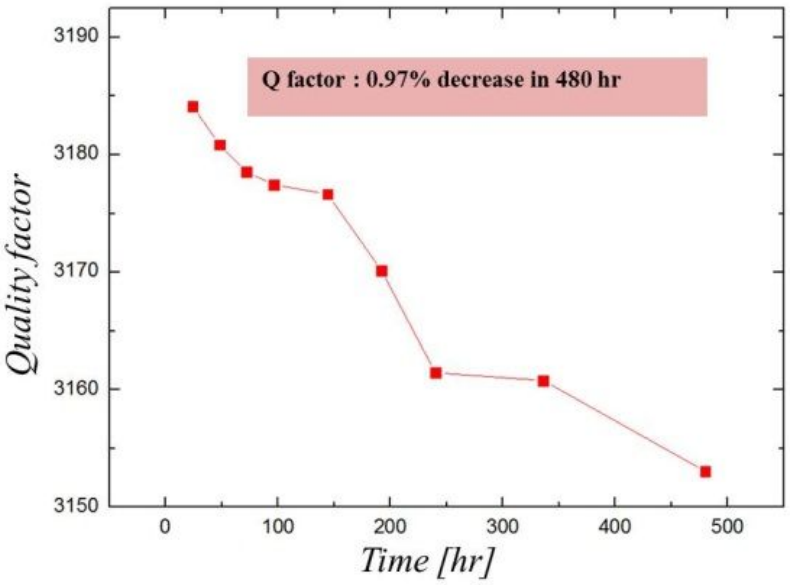


Figure 4.19. Long time maintenance of Q factor

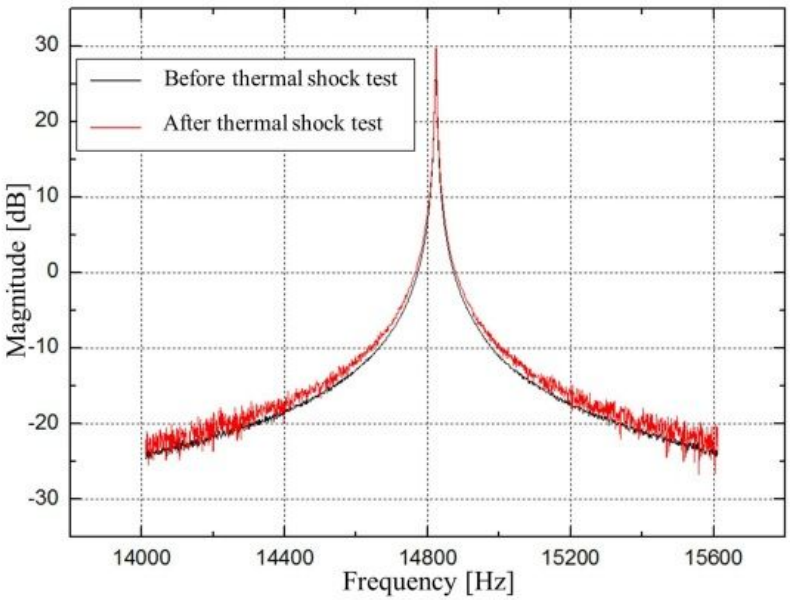
In order to measure maintenance of vacuum level more, life acceleration characteristics has been measured as well. Deterioration of vacuum level in

packaging was mainly caused by diffusion of ambient gases into packaged cavity. Diffusion can be accelerated by stress from temperature variation and pressure difference. As time goes by, Q factor decreases exponentially and failure of vacuum packaging is defined by decrease of Q factor to 50% from initial value. However, because unacceptable long-time observation is required in the case of much slow decrease of Q factor, life acceleration in high temperature is effective to reduce measurement time. Packaged SiN scanner was put into heat chamber of 120 ˚C and actuated with driving signal of 21 V_{rms} Variation of Q factor was investigated for 480 hr and plotted in Figure 4.20(a). Measurement result showed decrease of 0.97 % from initial value. This suggested life time of packaged scanner was larger than several thousand hours in life acceleration test.

Thermal shock test has been applied for investigating reliability of vacuum packaging using environmental chamber (TSE-11A,ESPEC) based on the test method standard of MIL-STD-883F [86]. The packaged scanner was placed in the chamber and the load was then subjected to condition of 100 ℃ 20min and 0 ℃ 20 min for a duration of 20 cycles. Figure 4.20(b) shows Q factor before and after the test. Significant degradation of vacuum packaging was not found.



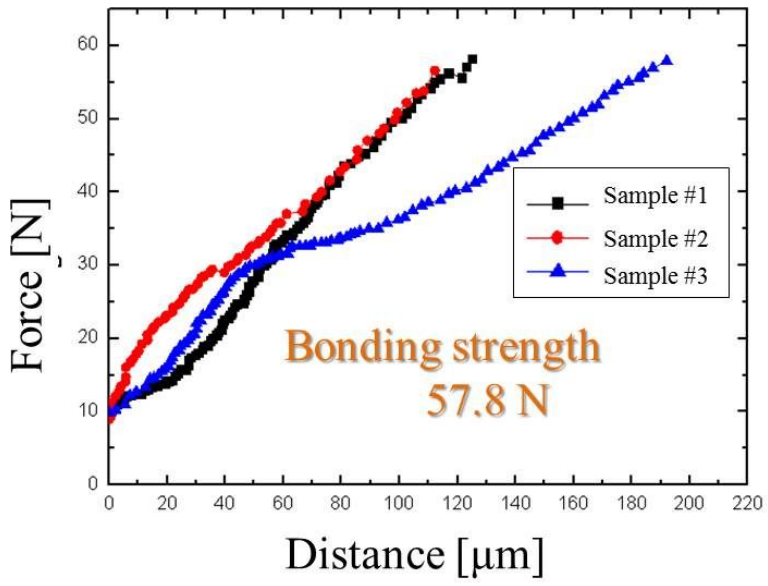
(a)



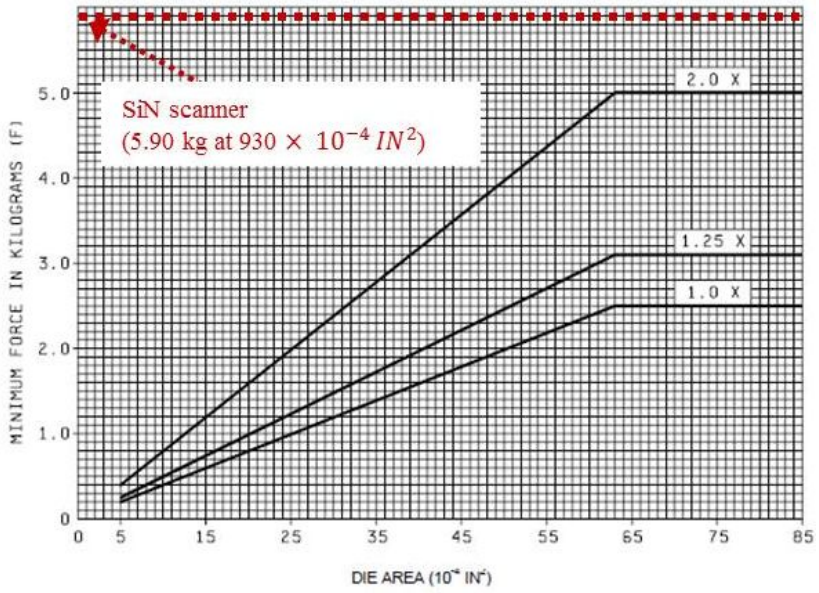
(b)

Figure 4.20. Reliability test of vacuum packaging: (a) life acceleration in high temperature of 120℃ and (b) thermal shock test

Die shear strength of vacuum packaging has been measured. Lateral force was applied to top glass cap and minimum force for detaching glass cap from a die was measured. Figure 4.21(a) shows measurement results and die shear strength was 57.8 N (5.90 kg) in average. Strength satisfied minimum force required (Figure 4.21(b)).



(a)



(b)

Figure 4.21. (a) Measurement result of die shear strength and (b) minimum force required by military standard (MIL-STD-883F)

4.4 Characterization of SiN scanner packaged with TWIn substrate

4.4.1 TWIn substrate with deep cavity

Optical transmittance of optical window was measured and Figure 4.22 shows transmittance of 75.2 % and 87.1% in minimum and maximum value, respectively.

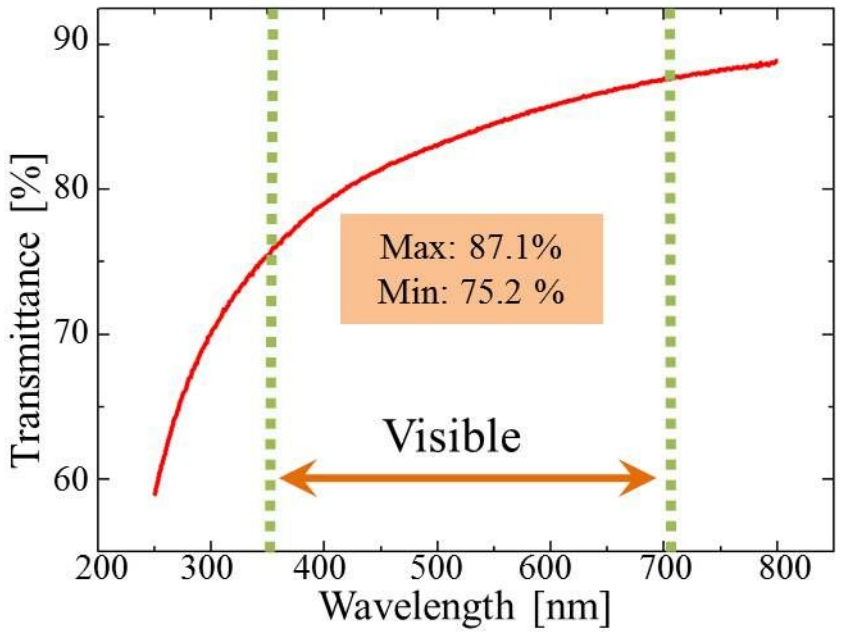
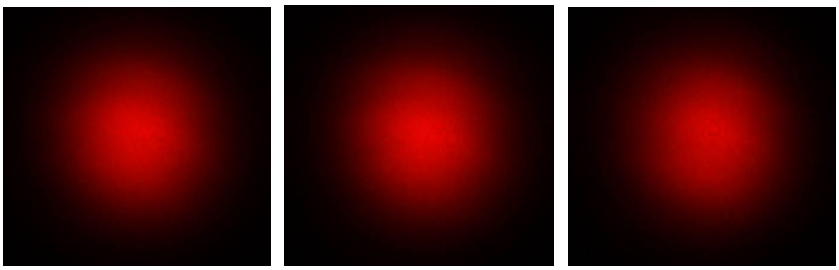


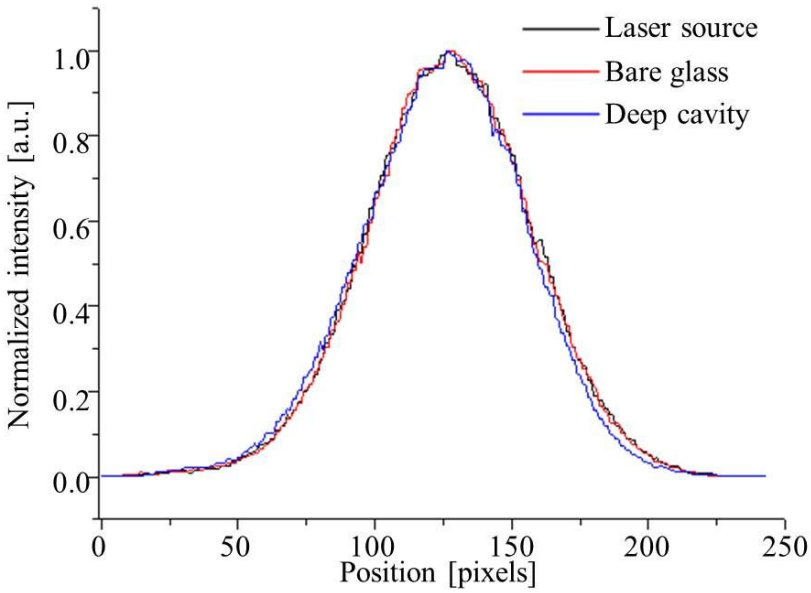
Figure 4.22. Transmittance of fabricated deep cavity of TWIn substrate

The feasibility for optical component was confirmed by investigating the laser beam profile passed through the deep cavity (Figure 4.23(a)-(c)).

Compared with profile of laser source and glass-passed beam, no distortion was found in laser beam passed through cavity. Intensity profiles showed no differences between each case as well (Figure 4.23(d)).



(a) (b) (c)

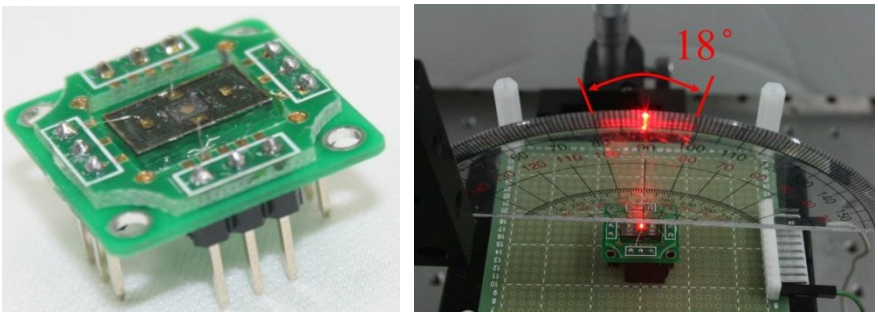


(d)

Figure 4.23. A 0.95 mW He-Ne laser beam profile (a) without samples, (b) with bare glass, and (c) with deep cavity. (d) The two-dimensional intensity profile of laser beam in each case.

4.4.2 Dynamic and optical characteristics

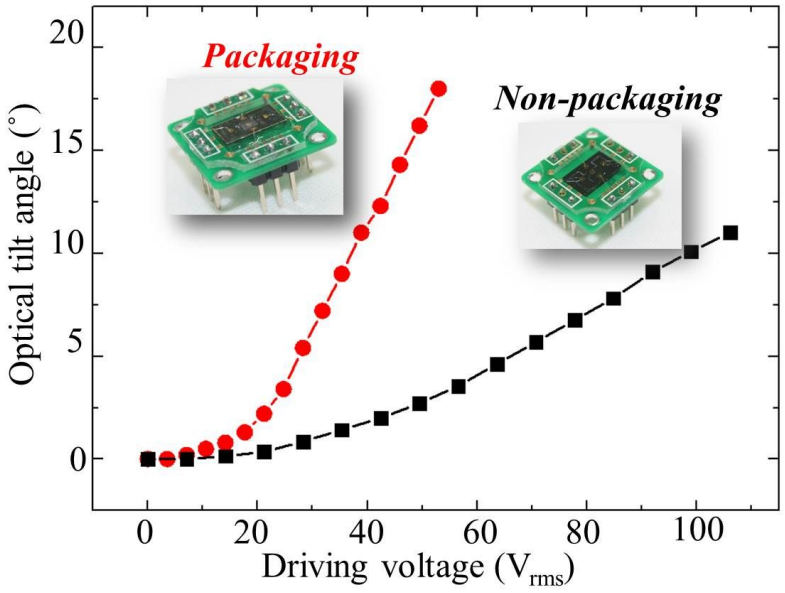
. Characteristics of packaged microscanner were measured as well. Silicon nitride scanner attached to PCB showed large dynamic range of 18 ° at 53.3 V_{rms} in Figure 4.24.



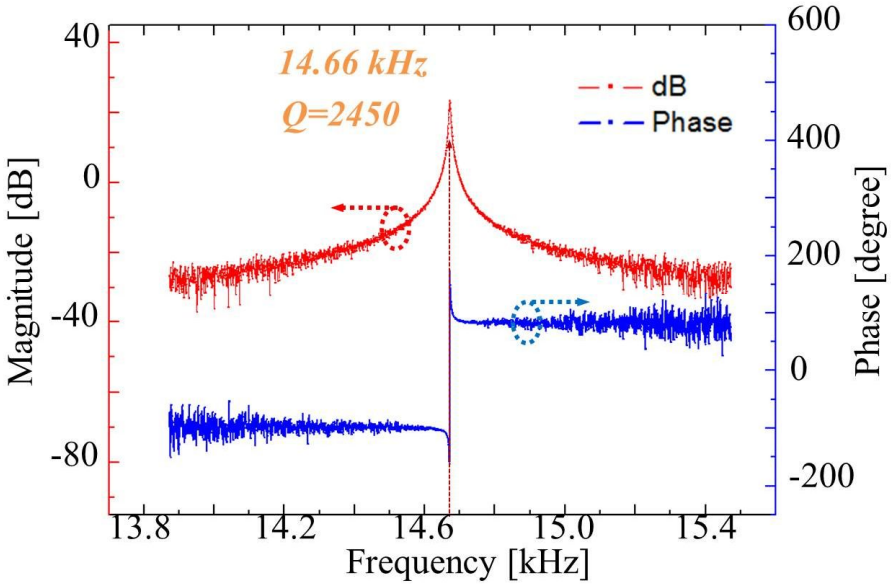
(a) (b)

Figure 4.24. Photography of (a) fabricated microscanner and (b) scanner operation with driving voltage of 53 V_{rms}

Optical tilt angle according to driving voltage is shown in Figure 4.25(a). Laser Doppler vibrometer measured resonant frequency of 14.66 kHz and quality factor of 2450 in Figure 4.25(b).



(a)



(b)

Figure 4.25. (a) Optical tilt angle and (b) frequency response of SiN scanner

4.4.3 Vacuum level and packaging reliability

Based on measurement of quality (Q) factor according to ambient pressure, this quality factor corresponded to vacuum level of approximately 3 Torr (Figure 4.26).

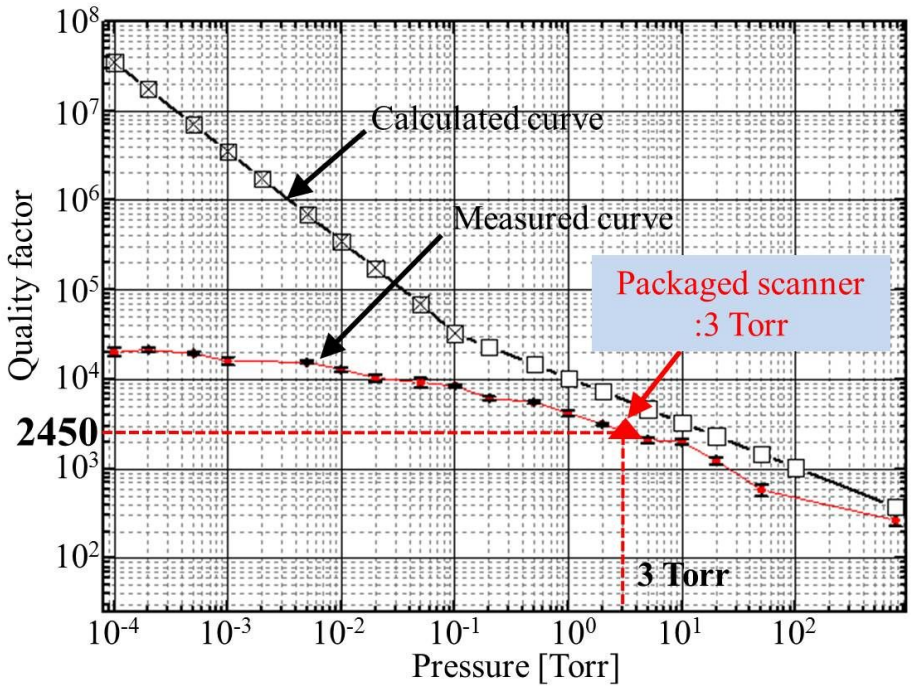
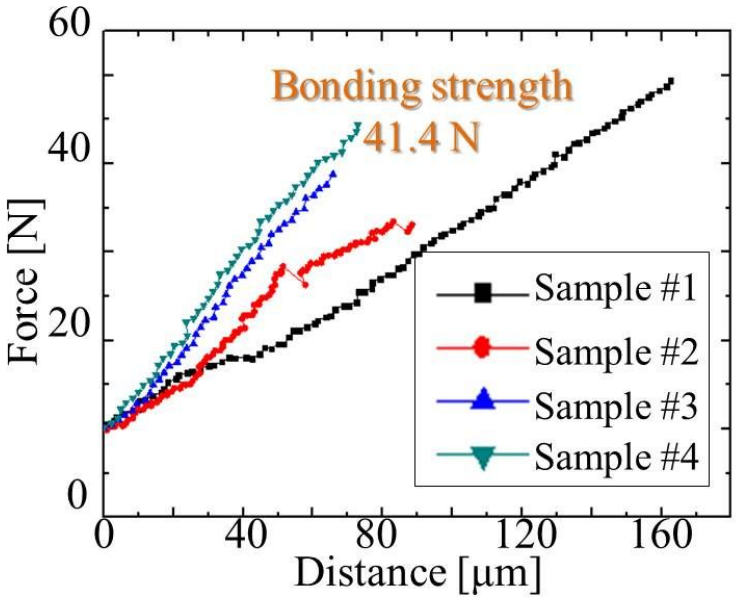
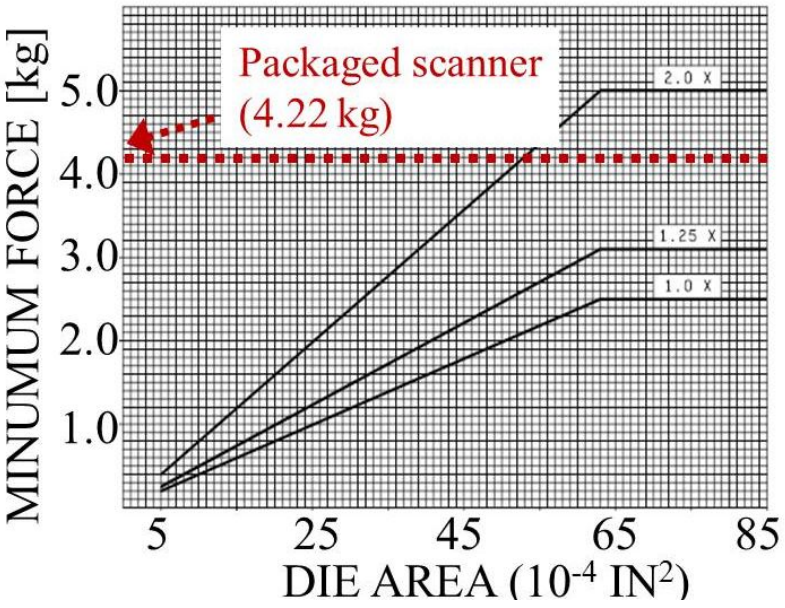


Figure 4.26. Measured curve of quality factor according to ambient pressure, and corresponding vacuum level of packaged microscanner

Die shear strength was 41.4 N in average (Figure 4.27(a)), and this satisfied minimum bonding strength of micro devices based on military standard (MIL-STD-883F) (Figure 4.27(b)).



(a)



(b)

Figure 4.27. (a) Measurement result of die shear strength and (b) minimum required strength based on military standard

4.5 Discusion

For an optical tilt angle over 32˚, the torsional spring was fractured, as shown in Figure 4.28. This caused a limited dynamic range of the SiN microscanner. The spring fracture was caused by the weakness of the torsional springs because the maximum stress usually occurs on this component. Simulation results using the finite element method (FEM) in Figure 4.29 show that the maximum stress occurs on the center of the side wall of the torsional spring; the maximum stress was 6.52 GPa when the scanning angle was 32˚ (Figure 4.30). This was close to the facture strength of silicon, at 7.68 GPa [87].

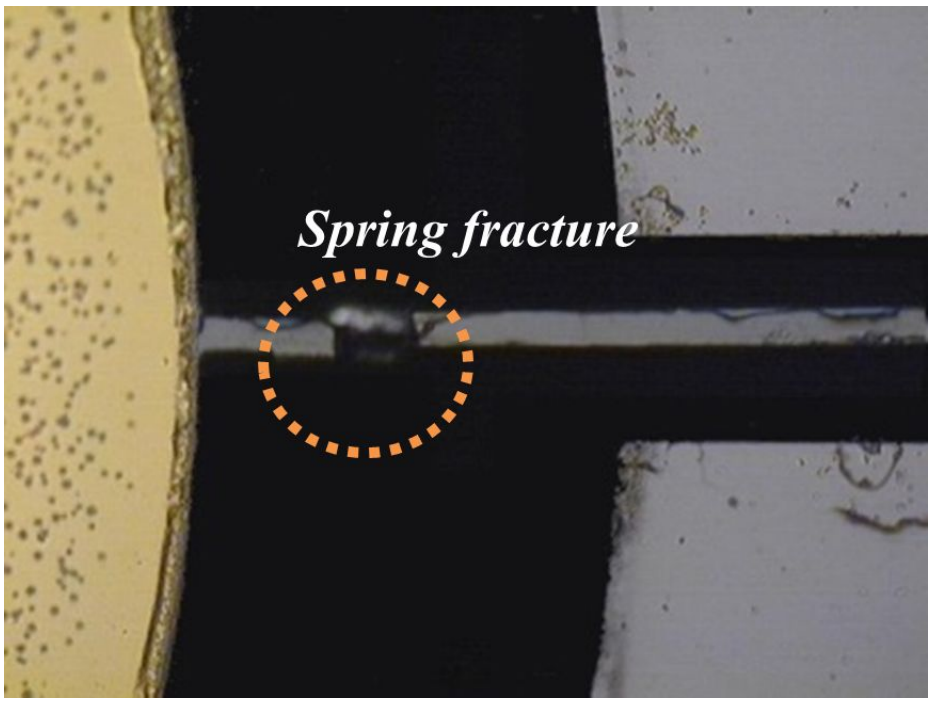
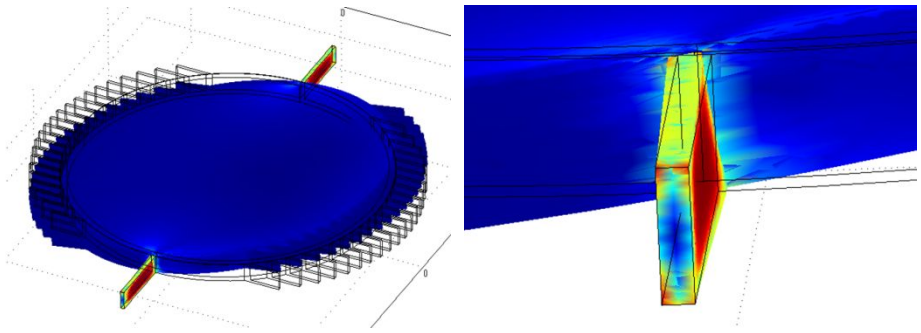


Figure 4.28. Photography of spring fracture



(a) (b)

Figure 4.29. FEM simulation result of stress: (a) Generated stress in torsional spring and (b) magnified image

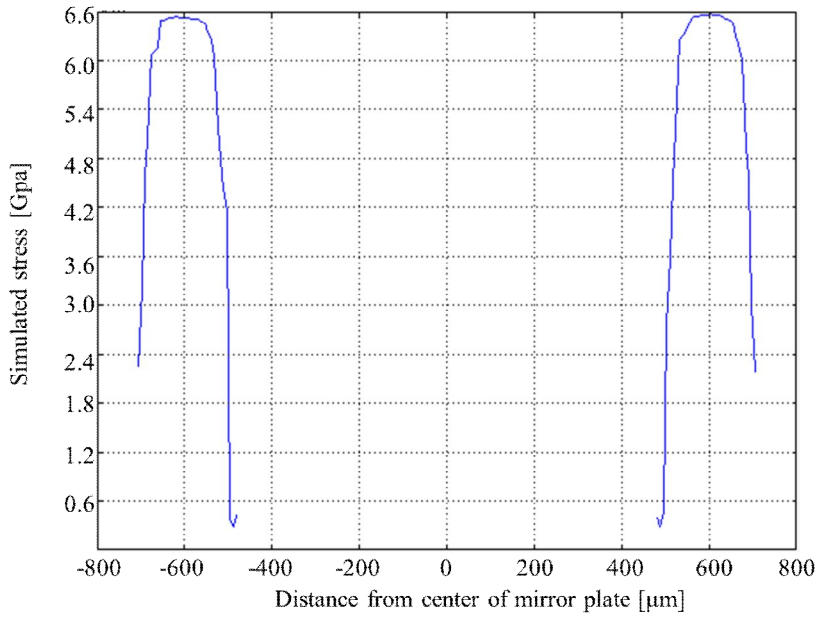


Figure 4.30. Cross-sectional profile of simulated stress in torsional spring

An interesting finding was that the FEM showed that the effect of the residual stress of the SiN thin film on the maximum stress in the torsional

spring was imperceptible. An improved design of the spring is expected to increase the dynamic range efficiently (Table 4.3).

Table 4.3. Simulation results of induced stress and maximum tilt angle

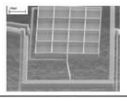
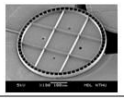
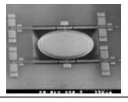
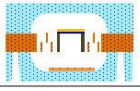
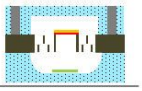
Case	**I**	**II**	**III**
Residual stress	60 MPa	0 MPa	60 MPa
Spring dimension	L=210 μm W=12 μm T=50 μm	L=210 μm W=12 μm T=50 μm	L=420 μm W=15.4 μm T=50 μm
Resonant frequency	15 kHz		
Simulated stress	6.52 GPa	6.52 GPa	3.36 GPa
Max. tilt angle (7.68 GPa)	37.7 ° (800 × 600)	37.7 ° (800 × 600)	73.1 ° (1280 × 1024)

4.6 Conclusion

This work demonstrated the novel silicon nitride scanner with silicon rim. Large dynamic range as well as optical flatness was achieved in high resonant frequency of 14.82 kHz. ROC of SiN mirror plate was 357 mm. Dynamic range of 32˚was achieved, which was four times or more than that of previous studies. Moreover, vacuum packaging of scanner was successfully obtained resulting in low driving voltage and protection of scanner from environment. Wafer-level process of vacuum packaging provided benefit of low cost of production. Reliability of vacuum packaging was demonstrated by life acceleration test, thermal shock test, die shear strength measurement.

Measurement results in this work was summarized and compared with reported studies about SiN microscanner as well as poly silicon scanner in Table 4.4. Among reported research, studies which included sufficient data was only mentioned. Proposed SiN scanner in this work had comparable diameter of 1 mm. Moreover, ROC of 445 mm in this work was a sole study satisfying minimum ROC (>300 mm) as microscanner. Furthermore, high resonant frequency of larger than 14.6 kHz was achieved. Speaking of actuator and dynamic range, vertical comb actuator offered large dynamic range of 32˚in maximum, compared with previous studies. In addition, two-times larger scanner efficiency ($\theta \cdot D/V^2$) was accomplished with high vacuum level of 1.3 Torr in maximum using wafer-level vacuum packaging.

Table 4.4. Comparison with previous work of thin film microscanner

Mirror plate	**Poly-Si**		**SiN**	**This work**	
Research group	UC Berkeley 	Tsing Hua Univ. 	Tsing Hua Univ. 	Packaging (Glass cap) 	Packaging (TWIn) 
Mirror Diameter	1 mm	0.5 mm	0.435 mm	1 mm	
ROC	N/A	150 mm	179 mm	445 mm	
Resonant frequency	1 kHz	1.8 kHz	17.7 kHz	14.81 kHz	14.68 kHz
Actuator	Lateral comb	Vertical comb	Parallel plate	**Vertical comb**	
Vacuum level	Atmosphere	Atmosphere	Atmosphere	**1.3 Torr**	**3.0 Torr**
Maximum 2θ	8.25° ($61\ V_{rms}$)	11.2° ($50\ V_{rms}$)	5.5° ($33.0\ V_{rms}$)	32° **($84.8\ V_{rms}$)**	**18° ($55.3\ V_{rms}$)**
$\theta \cdot D/V^2$ [deg·μm/V²]	**2.22**	**2.24**	**2.20**	**4.45**	**5.89**

Chapter 5

Conclusion

This dissertation presents novel method to achieve large dynamic range as well as large ROC of silicon nitride thin film micromirror. This paper demonstrates a high-speed silicon nitride (SiN) scanner with a large dynamic range. A SiN mirror plate with a diameter of 1 mm was stiffened by a silicon rim and driven by vertical combs. The silicon rim and vertical combs secure a large dynamic range as well as flatness of the SiN mirror plate. Wafer-level vacuum packaging provides a high Q factor and protection from the external environment. The device opens the door to the possibility of optical scanning at a high-resolution and a low driving voltage with high reliability.

This paper proposes a novel approach for an optical flat mirror plate in conjunction with a large tilt angle in a SiN scanner through the use of a silicon rim. The silicon rim, attached to the edge of the SiN film, increases the flatness of the mirror plate and enables a vertical comb to be assembled. The vertical comb provides the SiN scanner with a large tilt angle. Silicon-rim-reinforced silicon nitride scanner was fabricated and investigated feasibility of large ROC and large dynamic range. Silicon rim successfully fabricated and stiffened silicon nitride thin film. Vertical combs were attached to the silicon

rim with thickness of 25 μm. 20-100 μm-width Silicon rim was tested to investigate optimized width of silicon rim. Conventional silicon mirror plate was fabricated to compare the performance with silicon nitride scanner. All of them were designed to be same resonant frequency of 15 kHz by different spring width. Mechanical and optical properties were measured, and ROC of more than 300 mm and driving voltage of 40 % decrease from silicon mirror plate were shown. Large dynamic range of 32 ° was measured using vacuum chamber of ambient pressure of 1.2 mm Torr.

Moreover, this approach packages the SiN scanner at a low pressure, resulting in additional shrinkage of the driving voltage owing to the low energy loss due to the viscous flow of the gas molecules. Furthermore, the vacuum packaging protects the SiN scanner from the environment and secures the reliability of the performance of the device. The radius-of-curvature of the mirror plate was 357 mm and its dynamic range was 32° at 85 V_{rms} at a resonant frequency of 14.82 kHz.

The silicon nitride microscanner packaging with TWIn substrate has improved fabrication of through-via and led to better production yields and simplicity of back-end process including the wiring and PCB attachment. The through-wafer interconnection (TWIn) substrate was adapted to offer advanced packaging process. Fabrication method for deep cavity of TWIn substrate was investigated and optimized for optical transparency of cavity in order to prevent from optical signal distortion. Optical verification of cavity

suggests its feasibility as optical window for microscanner. SiN scanner packaging using proposed TWIn substrate is demonstrated. Vacuum level of 3.1 Torr and tilt angle of 18 ° at 53.5 V_{rms} have been measured.

This work contributes development of fabrication techniques in MEMS devices. Dry etching technique using SiN thin film as etching stop layer was demonstrated in deep reactive ion etching of silicon. This technique enabled the SiN mirror plate to be achieved without additional process of deposition and wet etching of silicon. Meanwhile, triple-stack anodic bonding was simply achieved using foil for electron moving path. Moreover, novel wet etching technique of glass wafer using Cr/Au and dehydrated AZ4330 was proposed for optically smooth surface and deep cavity. Glass-reflow technique for high transmittance of TWIn substrate was realized. Dry etching process for optically smooth surface of cavity in TWIn substrate was proposed as well.

There have been improvable points in this work. Larger ROC and higher reflectivity of mirror plate could be achieved using lower stress and higher reflective metal of Al. Higher dynamic range of more than 32° could be possible with improved design of torsional spring which reduces maximum shear stress generated during torsional operation of mirror plate. Higher scanner efficiency ($\theta \cdot D/V^2$) could be realized with smaller comb-gap and more combs in actuator.

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국문초록

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본 연구는 높은 평평도와 동시에 큰 구동 각도를 지는 질리콘 질화막 스캐너를 구현하기 위한 방법으로 단결정 실리콘 테두리와 수직 빗살 구동기가 집적된 실리콘 질화막 스캐너를 제안한다. 실리콘 질화막의 외각에 붙는 실리콘 테두리는 박막 미러판의 평평도를 증가시킬 뿐 아니라, 수직 빗살 구동기가 구현될 수 있도록 한다. 수직 빗살 구동기는 기존의 질화막 스캐너 연구들에서 적용했던 평행평판형 구동기와 달리 풀-인 현상이 없고, 따라서 매우 큰 구동 각도 구현을 가능하게 한다. 더불어, 진공 패키징을 통해 저전압에서 이러한 큰 구동 각도 달성을 가능하게 하였다. 본 연구는 실리콘 테두리로 강화된 실리콘 질화막 스캐너의 설계 및 이를 구현하기 위한 공정 방법을 제안하였고, 실제 제작에 성공하였다. 실리콘 질화막 미러판의 지름은 1 mm 이며, 실리콘 테두리의 폭은 20 μm, 50 μm, 100 μm로 달리하면서 최적의 스캐너 설계에 대해 분석하였다. 실리콘 테두리 및 스프링의 두께는 50 μm 이다. 수직 빗살 콤 구동

기는 폭 10 μm, 길이 100 μm 이며, 두께는 25 μm로 설계하였다. 제안하는 실리콘 질화막 스캐너의 성능을 기존의 일반적인 실리콘 스캐너와 비교하기 위하여 두께 50 μm 의 실리콘 미러판을 지닌 스캐너도 제작하였다. 공진 주파수는 모두 15 kHz 를 지니도록 설계하였다. 측정 결과, 실리콘 테두리를 지닌 실리콘 질화막 스캐너는 모두 최소 ROC (Radius-of-curvature) 요구치인 300 mm 이상을 보였다. 일반적인 실리콘 스캐너와 비교하였을 때, 최대 40% 의 구동 전압 감소 효과를 달성하였다. 특히, 제안한 실리콘 테두리를 지닌 실리콘 질화막 스캐너는 최대 광학 구동 각도가 32° 로, 기존의 연구결과들에 비해 최대 6배 가까운 구동 각도 증가를 달성하였다.

본 연구는 큰 구동 각도를 지닌 실리콘 질화막 스캐너의 제작 뿐만 아니라, 이를 웨이퍼 단위 공정 기술로 스캐너 진공패키징의 모듈화에도 성공하였다. 진공 패키징은 대기 중의 가스 분자와의 충돌로 인한 에너지 손실이 줄게 되어, 스캐너의 공진 구동 시에 필요한 에너지, 즉 구동 전압을 획기적으로 감소시킨다. 뿐만 아니라, 외부 습기와 먼지, 온도 변화로부터 스캐너를 보호하여 소자의 수명 연장 및 구동 신뢰성 향상도 기대할 수 있다. 따라서 스캐너의 진공 패키징에 대한 연구가 많이 진행되고 있다. 본 연구에서는 큰 구동 각도를 지닌 실리콘 질화막 스캐너의 제작 뿐만 아니라, 웨이퍼 단위 진공 패키징 기술 또한 제안하며 이를 실제 제작에 성공하여 높은 진공도 특성을 확인하였다. 먼저 깊은 공극을 지닌 유리 기판을 이용

한 진공 패키징 기술을 제안하였으며, 상압의 1/700 수준인 1.3 Torr 의 진공도를 달성하였고, 85 V_{rms} 에서 32 ° 구동 각도를 구현하였다. 또한 깊은 공극을 지닌 실리콘 관통기판을 이용한 진공패키징 기술도 제안하여 패키징에 성공하였다. 패키징 진공도는 3.0 Torr 였으며, 53.5 V_{rms} 에서 18 ° 의 구동각도를 달성하였다.

본 연구에서 제안하는 실리콘 테두리로 강화된 실리콘 질화막 스캐너와 이의 웨이퍼 단위 진공 패키징 기술은 최대 광학 구동각도 측면에서 최대 6배 이상의 향상을 보인 뛰어난 특성을 보였다. 또한 구동 각도 측면에서 동일 조건의 기존 실리콘 스캐너에 비해 최대 41%의 구동 전압 감소 효과도 증명하였다. 이러한 연구는 초소형 스캐너 연구에 중요한 진전에 기여할 것으로 기대되며, 저전압에 구동하는 고해상도 초소형 스캐너 제작에 초석이 될 것으로 기대된다.

감사의 글

7년간의 대학원 생활에 걸쳐 수많은 고마운 분들의 도움이 없었다면 지금의 박사 학위 논문은 없었을 것입니다. 학위 논문을 마무리 하면서 숨가빴던 대학원 생활이 주마등처럼 스쳐 지나갑니다.

먼저 연구를 시작할 수 있도록 기회를 주시고, 부족한 점이 많은 제자를 감싸주시고 한 명의 연구자로 서게 해주신 김용권 교수님께 깊은 감사의 말씀을 드립니다. 교수께서 심어 주신 연구자로써의 자세와 도리를 잊지 않고, 연구실의 이름을 드높일 수 있는 자랑스러운 제자가 되도록 노력하겠습니다. 박사 학위 논문이 완성되도록 조언을 아끼지 않아 주신 전국진 교수님, 박남규 교수님, 김호성 교수님, 지창현 교수님께도 깊은 감사의 말씀을 드립니다.

아무것도 모르던 신입생 때 참여한 MEMS 우주망원경 과제에서 부족하다 나무라지 않으시고 따뜻한 격려와 함께 지식을 아낌없이 나누어 주신 박일흥 교수님, 이직 교수님, 남신우 박사님, 정인석 교수님께 감사 드립니다. 신입생부터 박사 때까지 때로는 연구실 선배로써 아껴 주시고, 때로는 교수로써 연구 지도를 해주신 박재형 교수님께도 깊은 감사를 드립니다. 짧은 기간이었으나 격의 없이 대해 주시고 연구자로써의 열정을 가르쳐 주신 이승기 교수님. 교수님의 식지 않는 열정을 본받아 사회에 나가서도 초심을 잃지 않는 연구자가 되도록 하겠습니다.

눈치 없고 천방 지축이었던 저를 보듬어 주신 연구실 선배님들께도 정말 감사 드립니다. 멀리 부산으로 가신 종만형. 연구실에서도 오래 같이 있지 못했고 부산에 계셔서 자주 뵙지도 못했지만, 따뜻한 웃음을 잃지 않으시고 열정적으로 실험하시는 자세는 대학원 생활 내내 저의 큰 귀감이 되었습니다. 넉넉한 웃음의 형균형. 긴장했던 신입생 때 편안한 웃음으로 맞아 주셔서 큰 어려움 없이 연구실에 적응할 수 있었습니다. 얼마 후면 잠시 미국으로 가시는 용성형. 인생 선배로써, 연구실 형으로써 주셨던 수 많은 조언들이 큰 힘이 되었습니다. 무사히 돌아 오시길 빌며 귀국 후에는 자주 뵈었으면 좋겠습니다. 전북대학교로 가진 정무형. 학교에 있을 때나 졸업 하신 후에나 변함 없이 후배들을 아껴 주시고 격의 없이 대해주셔서 정

말 감사했습니다. 형께서 주신 따뜻한 호의에 부끄럽지 않은 후배가 되도록 노력하겠습니다. 미국에 자리잡으신 병욱형. 형과 함께한 공정과 운동, 마이에미 여행은 정말 잊을 수 없습니다. 그리고 일 적으로나 가정 적으로나 항상 최선을 다하고 이루어 내시는 모습은 정말 자랑스럽고 닮고 싶었습니다. 모범을 보여주신 형이 있었기에 후회 없는 대학원 생활이 될 수 있었습니다. 수 많은 밤을 새우는 실험을 같이한 민수와 진아야. 정말 힘든 석사 시기를 보냈지만 너희들이 있어 웃으면서 버틸 수 있었고 그래서 많은 것을 얻을 수 있었다. 모든 어려움을 극복하고 박사를 마친 진아. 너무 축하하고 힘들었던 만큼 앞으로는 멋진 일만 있을 것으로 믿는다. 민수도 곧 미국에서 무사히 박사를 마칠 것으로 믿고 한국에서 조금 더 자주 볼 수 있었으면 좋겠다. 든든한 연구실 동기들 은성형, 용석. 은석형도 이번에 같이 졸업하게 되어 정말 기뻐. 분위기 메이커 형이 있었기에 긴 7년의 연구실 생활을 즐겁게 해나갈 수 있었어. 삼성에 자리잡은 용석아. 운동부터 회식, 엠티와 연구실 운영까지 모든 대학원 생활에 함께한 추억이 너무 많았고 선후배간을 잘 조율하고 이끌어가는 네가 있어 든든했다. 케티에서 고생하는 영태형. 가정을 꾸리느라, 연구하느라 바쁘면서도 찾아가면 따뜻한 음료수로 격려해주셔서 정말 고마웠습니다. 팀 선배 승택형. 연구뿐만 아니라 인생 선배로써 아낌없이 해주신 조언 너무 감사했어요. 이번에 학위 마치시는 것 정말 축하 드리고, 고생하신 만큼 앞으로 좋은 일들이 많을 것으로 믿습니다. 뺀질이 성현아. 바로 밑 후배라 엄격히 대할 때도 있었지만, 밝은 성격으로 후배들과 잘 이끌고 연구실 분위기 이끌어서 항상 고마웠다. 심사를 준비하는 고율아. 차분한 성격으로 연구실을 잘 이끌어 갈 것으로 믿고 올해 심사도 잘 끝낼 것으로 믿는다. 팀 후배 준근아. 다른 과제를 수행하게 되어 함께 연구했던 시간이 적어 많이 챙겨주지 못해 미안했다. 그럼에도 변함없는 성실한 자세로 묵묵히 연구를 수행하여 좋은 결과를 내고 후배들에게 귀감이 되는 네가 자랑스럽다. 팀 후배 승현아. 언제나 솔선수범하고 자신의 일처럼 형의 연구를 도와주는 든든한 네 덕분에 힘든 박사 연구를 무사히 마칠 수 있었다. 이제 막 들어온 팀 후배 대곤아. 함께한 시간이 길지 않아 선배로써 많은 것을 주지 못해 아쉽지만, 밝고 성실한 너라면 연구실에 잘 적응하고 좋은 연구로 무사히 졸업할 수 있을 것으로 믿는다. 유학을 준비하는 현석아. 밝고 책임감 강한 현석이 덕분에 많이 웃을 수 있었고 도움 많이 받았다. 똑똑한 현석이니 미국 나가서도 잘할 거라 믿고

자주 연락하자. 마찬가지로 유학을 준비하는 승현아. 운동 잘하고 사나이다운 너라면 미국에서도 적응 잘 하고 무사히 학위 마칠 것으로 믿는다. 연구실 해피 바이러스 정기야. 순수한 네가 있어 밝은 연구실이 될 수 있었고 많이 웃을 수 있었다. 유승현, 이승현, 현석 포함해서 결혼식에서 도움도 잊을 수 없지. 탈없이 팔이 나길 빌고, 후배들 잘 이끌어서 계속 밝은 연구실 만들어 가길 바란다. 후배 성환이도 석사 무사히 마치고 사회에 나가서도 지금처럼 잘 할 것으로 믿는다. 오랜 시간 같이 있지 못했지만 착하고 밝은 신입생들 석원, 민혜, 영민이도 즐거운 연구로 좋은 성과 낼 것으로 믿는다.

사랑하는 부모님. 지금의 제가 있는 것은 전부, 믿어주시고 든든한 버팀목이 되어주신 사랑하는 부모님 덕분입니다. 맨손으로 시작하셔서 온갖 어려움 속에서도, 사랑으로 보듬어 주시고 오랜 기간의 공부 뒷바라지 해주신 부모님의 사랑을 생각하면 가슴이 먹먹해 집니다. 그 크신 사랑을 어찌 다 갚을 지요. 부디 조금이나마 더 갚을 수 있도록 오래오래 제 곁에 건강히 있어주시길 소원합니다. 사랑하는 누나. 우리 집의 자랑으로 든든한 누나가 있어 걱정 없이 오랜 학업을 마칠 수 있었어. 멀리 떨어져 있었어도, 따뜻하게 챙겨줘서 정말 고마워. 이제 졸업도 하고 대전에서 가까이 살게 되니 든든한 동생이 되도록 할게.

사랑하는 장인어른, 장모님. 학생의 신분으로 부족함이 많은 저를 따뜻하게 받아주시고 사랑을 나누어 주셔서 정말 감사합니다. 무사히 학업을 마친 지금, 자랑스럽고 든든한 사위가 되도록 노력하겠습니다. 그리고 행복한 가정을 꾸려 은혜에 보답하겠습니다.

마지막으로 사랑하고 존경하는 아내 융경이에게 감사의 말을 남깁니다. 길어지는 학업에도 변치 않는 사랑으로 감싸주고 기다려줘서 정말 고맙다. 융경이가 있었기에 오랜 학업 기간을 견딜 수 있었어. 학생의 신분으로 결혼 후에도 많은 것을 해주지 못했지만, 혼자 회사 생활로 가정을 이끌어주고 든든하게 곁을 지켜준 융경이에게 미안하고 고마운 마음을 금할 수 없구나. 인생의 동반자로써 곁에 두고 고마움을 평생 갚으며 살게. 그리고 이제 태어날 우리 아기와 함께 앞으로는 행복한 일들만 있을 거라 믿고, 대전에서 아름다운 가정 꾸리자. 사랑한다.

2014년 2월

진주영