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AlGaN/GaN Schottky Barrier Diodes for High Power and Fast Switching Applications

고 전력과 고속 스위칭 응용을 위한 AlGaN/GaN 쇼트키 접합 다이오드

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전 남 철

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Abstract

AlGaN/GaN Schottky Barrier Diodes for High Power and Fast Switching Applications

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In recent years, aluminum gallium nitride (AlGaN)/ gallium nitride (GaN) heterostructure devices have received great attention as high efficiency power devices due to their superior properties, such as high current density, high breakdown field, and fast recovery time. This dissertation presents the investigations of AlGaN/GaN Schottky barrier diodes (SBDs) and high electron mobility transistors (HEMTs) as a power switching devices.

Schottky HEMTs were fabricated on the AlGaN/GaN heterostructure with a silicon carbon nitride (SiCN) capping layer. With a 5-nm-thick SiCN capping layer, two-dimensional electron gas (2DEG) carrier concentration was increased

about 51 % compared with a conventional AlGaN/GaN heterostructure, due to the neutralization of negative polarization charges at the AlGaN surface. Thus, maximum drain current of the Schottky HEMT with SiCN capping layer was increased about 10 % compared with a conventional Schottky HEMT. Schottky HEMT with an integrated Schottky-drain protection diode was fabricated. Low turn-on voltage of 0.7 V and blocking capability over 100 V was measured with a SiCN-SBD.

Recessed Schottky contact was studied as an AlGaN/GaN SBD scheme. Two-step etching composed of dry etching and wet digital etching with 5 nm/cycle etch rate was proposed as an epi-layer etching method. Due to the surface treatment of wet digital etching, the ideality and Schottky barrier height of SBDs were improved from 1.35 and 0.60 eV to 1.19 and 0.73 eV, respectively.

Influence of anode recess depth was analyzed and optimum recess depth was determined. As a result, the AlGaN/GaN SBD with turn-on voltage of 0.52 V, ideality factor of 1.17, Schottky barrier height of 0.76 eV, forward current of 127 mA/mm at 1.5 V, and reverse current of 2 μA/mm at -1100 V was fabricated. Failure of the fabricated diode was not observed at the 200 °C, 200 V reverse stress condition during 200 hours.

Double field plate structure to increase the breakdown voltage of AlGaN/GaN SBD was also studied. The electric field distribution effect of the field plates was clearly verified by device simulation. Experimental result shows the increase of breakdown voltage from 925 V to 1065 V with the double field plate structure.

AlGaN/GaN SBD with anode edge terminated SiN_x layer was proposed to reduce the reverse current. Reverse leakage current of the proposed diode was decreased about 10^3 order due to the suppression of the surface current. The fabricated diodes shows the good forward and reverse current uniformity.

The multi-finger lateral-type AlGaN/GaN SBDs were successfully implemented with a 5 mm^2 active area. The fabricated diode exhibits the forward current of 7.1 A at 1.5 V, specific on-resistance of 6.1 $m\Omega \cdot cm^2$, reverse current of 12.5 μA at -600 V, and breakdown voltage of 1080 V. The figure of merit (V_{BR}^2/R_{on}) is 192 MW/cm^2, which is one of the highest value of the lateral-type large area GaN SBDs ever published. Reverse recovery time of the fabricated diode was measured as 10 ns. These results indicate that the proposed AlGaN/GaN SBDs are adequate for fast switching applications with low losses.

Key words: Power device, GaN, AlGaN/GaN heterostructure, Schottky barrier diode (SBD), High electron mobility transistor (HEMT), Recess etching, Passivation, Silicon nitride (SiN_x), On-resistance, Breakdown, Pulsed I-V, Edge termination

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Chapter 1. Introduction

1.1 Demand on high efficiency power devices

Today's advanced solid-state power devices with high efficiency are driven by the needs on the so-called 'green-IT' issues for the global environmental protection and energy saving issues. Figure 1-1 shows the power switching devices (e.g., gate turn-off thyristor, insulated-gate bipolar transistor, bipolar, metal-oxide-semiconductor field-effect-transistor) applications. While higher frequency and ever higher power handling capabilities are sought, portability is also a key factor because there is increasing pressure to make these devices smaller and more efficient [1].

Figure 1-2 shows the positioning of power devices with respect to operating voltages and product ranges. Traditional Si MOSFETs are replaced with IGBT in low-voltage, high-end solution due to its relatively high performances. Thanks to price competitiveness, IGBT is getting a more shares in high-voltage and low-end solution. These steady growth of IGBT markets including motor drivers and electric vehicle (EV) are expecting as 6 billion dollars in 2018 [2]. However, Si power devices such as IGBT and MOSFET have their inherent performance limitations, such as power density and operation temperature. Thus, compound semiconductors SiC and GaN are becoming a substitutes of Si power devices. Commercial SiC is becoming a high-end device solution and GaN is under research stage.

Figure-of-merit (FOM) value which is defined as multiplication of on-resistance

($R_{ds,\,on}$) and gate charge (Q_g) is widely used for power device evaluation. Small on-resistance and gate charge is needed to achieve a high efficiency power device systems with low power loss and high switching frequency. Thus, there has been significant improvement on technology to reduce the FOM. Figure 1-3 shows the development progress of Si power device from bipolar transistor to super junction transistor. However, Si power devices would be faced with a technical plateau. In contrast with Si power devices, GaN power devices are expecting to provide the drastic improvements.

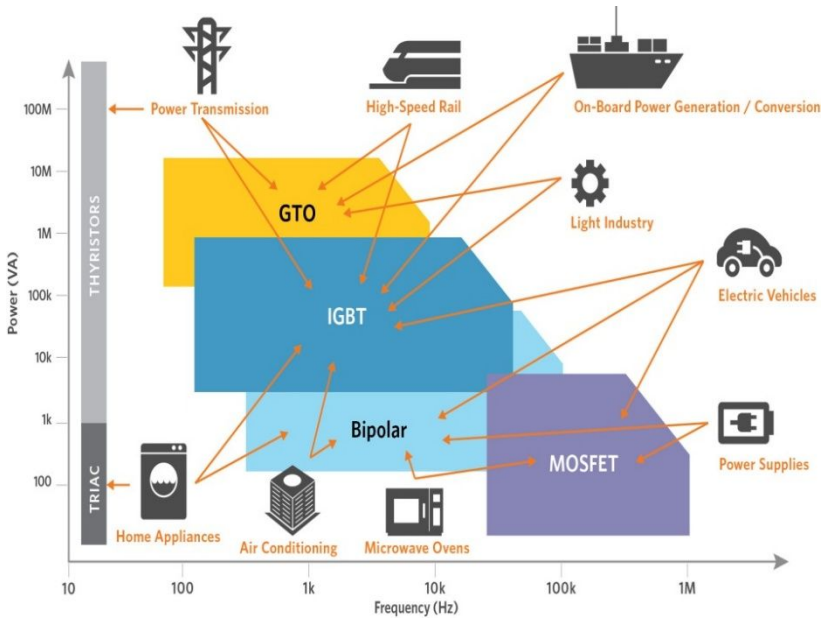


Fig. 1-1. Power switching device applications [1]

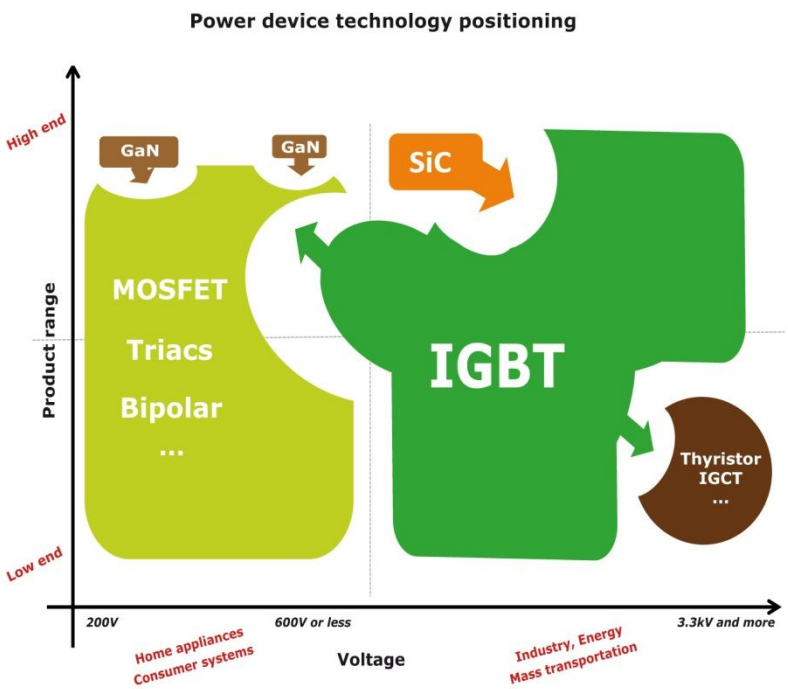


Fig. 1-2. Power device technology positioning [2]

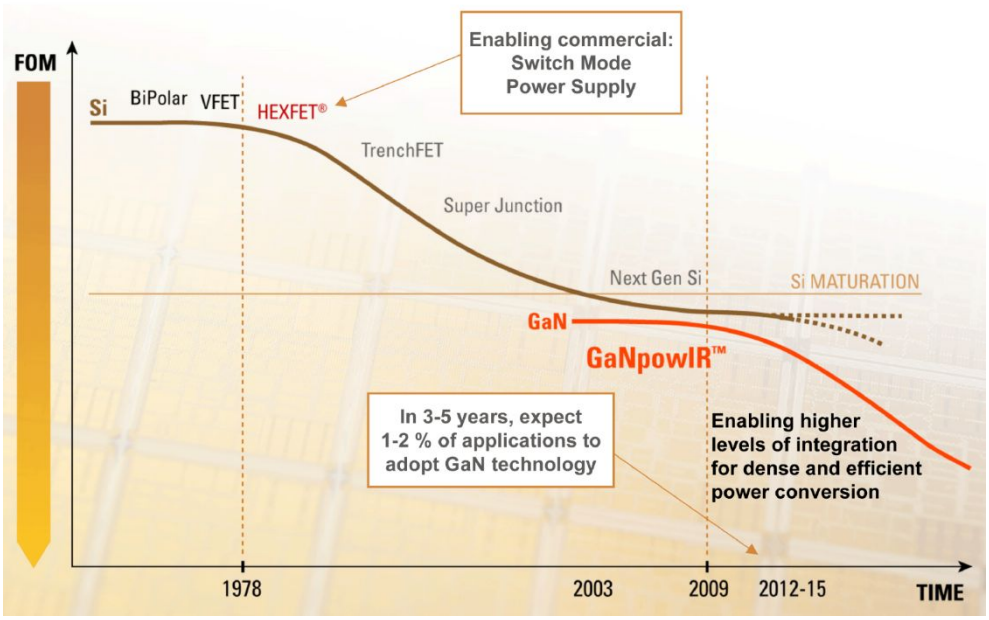


Fig. 1-3. Development progress of Si power device [3]

1.2 GaN material properties

The material properties of wide bandgap semiconductors are summarized in Table 1-1 [4], [5]. GaAs and GaN have direct bandgap which is suitable for light absorbing and emitting. Especially, GaN is a direct bandgap semiconductor material with a 3.45 eV bandgap, which corresponds to near-ultraviolet light (364 nm) [6]. Wide bandgaps of SiC and GaN are favorable to the critical electric field, because the critical electric field is tends to proportional with the bandgap. Moreover, SiC and GaN are competitive materials considering the electron mobility and saturation velocity.

Several figure-of-merits were published in the literatures to compare the materials properties. In 1965, Johnson derived a figure-of-merit

$$\text{JFOM} = \frac{E_c \cdot v_{sat}}{\pi} \tag{1.1}$$

where E_C is the critical electric field and v_{sat} is the carrier saturation drift velocity [7], [8].

In 1982, Baliga derived a figure-of-merit

$$\text{BFOM (low frequency)} = \varepsilon \cdot \mu \cdot E_C^3 \tag{1.2}$$

$$\text{BFOM (high frequency)} = \mu \cdot E_C^2 \tag{1.3}$$

where ε is the dielectric constant, μ is the carrier mobility, E_C is the critical electric

field of the semiconductor [8]-[10]. Low frequency BFOM was defined with an assumption that losses of power device are dominated by conductor losses. High frequency BFOM was defined with an assumption that losses of power device are dominated by switching loss. On the basis of these BFOMs, GaN is intensively superior to Si, GaAs and SiC as shown in Table 1-1. Therefore, GaN is promising and suitable material for power devices with low loss and fast switching.

Table 1-1. Material properties of wide bandgap semiconductors (300 K)

	Si	GaAs	4H-SiC	6H-SiC	GaN
Bandgap (eV)	1.12 Indirect	1.42 Direct	3.26 Indirect	2.86 Indirect	3.45 Direct
Dielectic constant	11.8	13.1	10	9.7	9.5
Bulk mobility ($cm^2/V \cdot s$)	1350 (μ_e) 450 (μ_h)	8500 (μ_e) 400 (μ_h)	720 (μ_e)	370 (μ_e) 75 (μ_h)	900 (μ_e) 10 (μ_h)
Saturation velocity (10^7 cm/s)	1	2	2	2	2.5
Critical Field (10^6 V/cm)	0.3	0.4	2.0	2.4	3.5
Thermal conductivity (W/cm·K)	1.3	0.55	4	5	1.3
BFOM ($\varepsilon \cdot \mu \cdot E_C^3$)	1	17	134	115	537

1.3 Substrates for epitaxy of GaN

Free-standing GaN power devices are premature to commercialized, even though the GaN optical devices such as laser diodes (LDs) and light emitting diodes (LEDs) were commercialized. Area-dependent high current density and breakdown voltage can be obtained with a vertical structure. Recently, vertical GaN power diode was reported by Sumitomo electric industries [11], [12]. However, price of 4-inch GaN-on-hydride vapor phase epitaxy (HVPE) wafer is over twice compared with 6-inch GaN-on-Si wafer in 2015 as shown in Fig. 1-4 [13]. Moreover, there is still severe defect density issue on bulk GaN substrate (~10^7 /cm^2) [14], [15]. Thus, lateral structure is a mainstream in GaN power devices.

Figure 1-5 shows the market size of GaN wafer with different substrate [13]. It is predicted that GaN-on-Si wafer will dominate the GaN market over 10 years due to its low cost and large wafer availability over 8-inch. GaN-on-SiC substrates have seen noteworthy progress in the last 10 years in terms of material quality, process yield, reproducibility and reliability [16]. SiC is the favorable substrate material for high power RF GaN HEMTs in production because of its high thermal conductivity (350 W/m/K), which plays an important role in minimizing the device temperature and improving the operational reliability [17].

Because GaN layers are grown on lattice and thermal expansion coefficient (CTE) mismatched foreign substrate, buffer layer structure with a low defect density is important. Carbon doping is one of the effective candidate to obtain high resistive buffer layer [4].

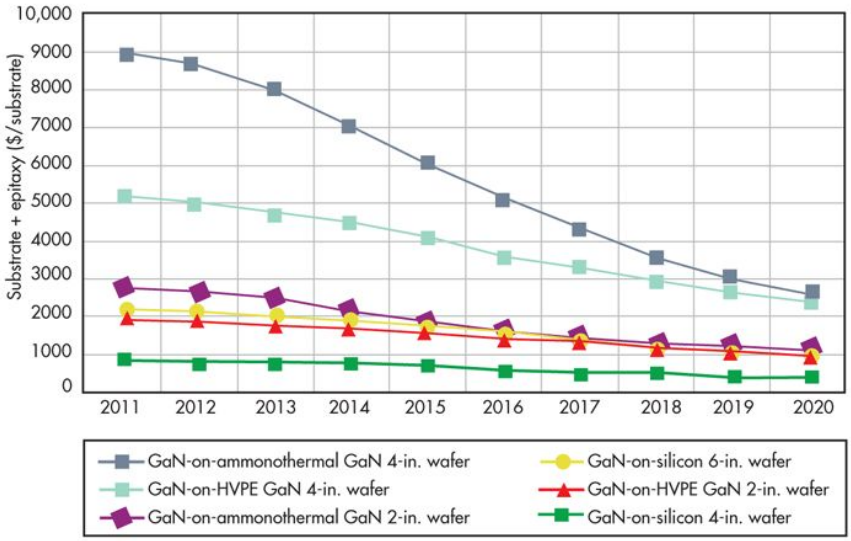


Fig. 1-4. GaN wafer prices forecast [13]

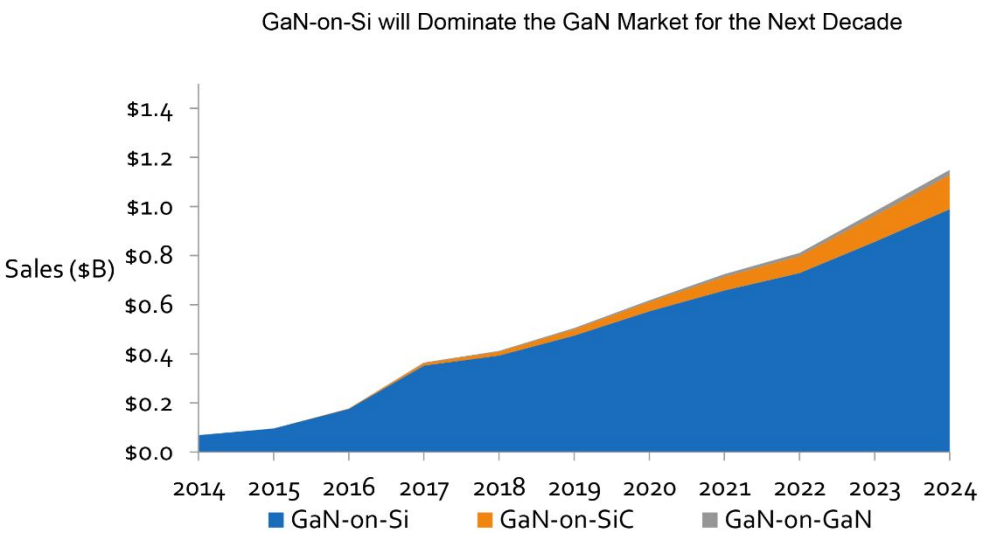


Fig. 1-5. Prediction of GaN wafer market size with Si, SiC, and GaN substrate [13]

1.4 AlGaN/GaN heterostructure

The distinctive feature of lateral device is a presence of a two-dimensional electron gas (2DEG) channel. Heterojunction is formed between AlGaN and GaN, because of large bandgap difference as shown in Fig. 1-6 [18]. With increasing the Al content of $Al_xGa_{1-x}N$, bandgap of $Al_xGa_{1-x}N$ is increased from 3.4 eV to 6.2 eV as depicted in Fig. 1-7 [19].

High carrier concentrations of 10^{13} cm^{-2} can be achieved in AlGaN/GaN heterostructures without doping. This high carrier concentrations can't be achieved with a bandgap discontinuity. Due to wurzite crystal structure of GaN, spontaneous polarization arises which is not found in conventional zincblende III-V semiconductors. Asymmetry of the bonding in wurzite crystal structure is an origin of spontaneous polarization as shown in Fig. 1-8 [20]. Piezoelectric polarization due to mechanical stress also attribute to the high carrier concentration at the AlGaN/GaN interface. Direction of polarization and interface charges in GaN/AlGaN/GaN heterostructure is shown in Fig. 1-9 [21]. Especially in wurtzite AlGaN/GaN based transistor structures, the piezoelectric polarization of the strained top layer is more than five times larger as compared to AlGaAs/GaAs structures, leading to a significant increase of the sheet carrier concentration at the interface [21]-[23].

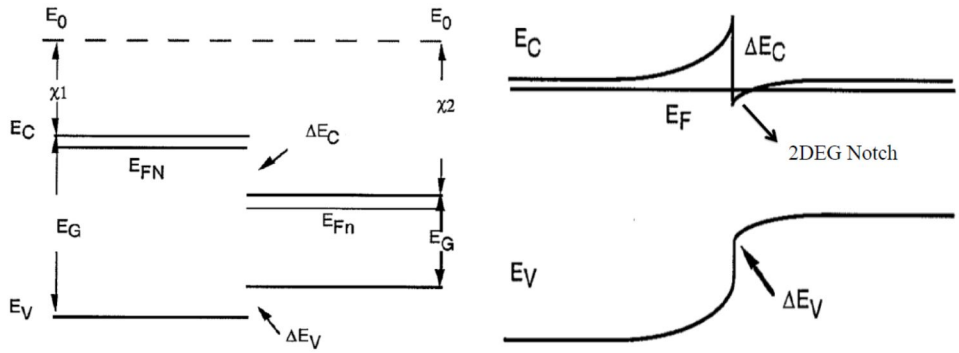


Fig. 1-6. Energy band diagram for heterostructure [18]

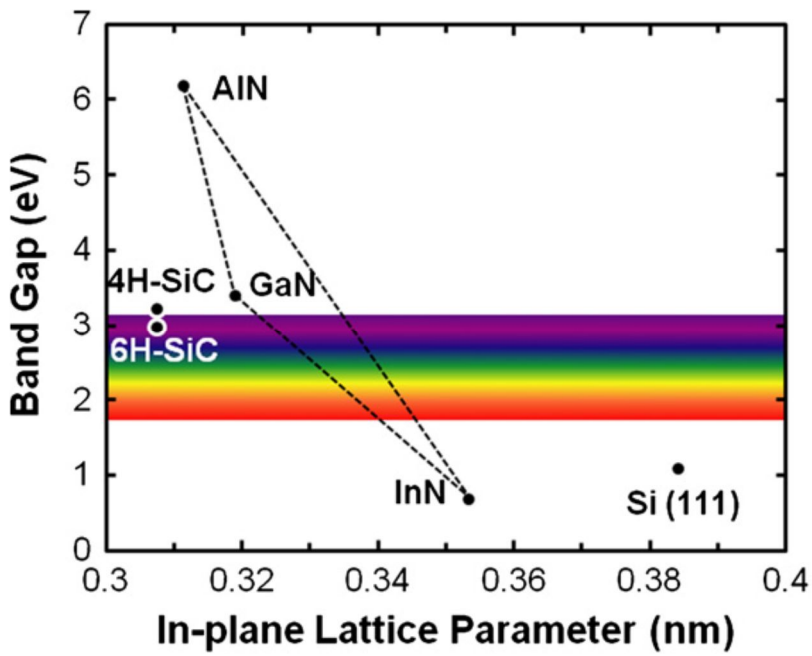


Fig. 1-7. Bandgaps for GaN (0001) and its related alloys [19]

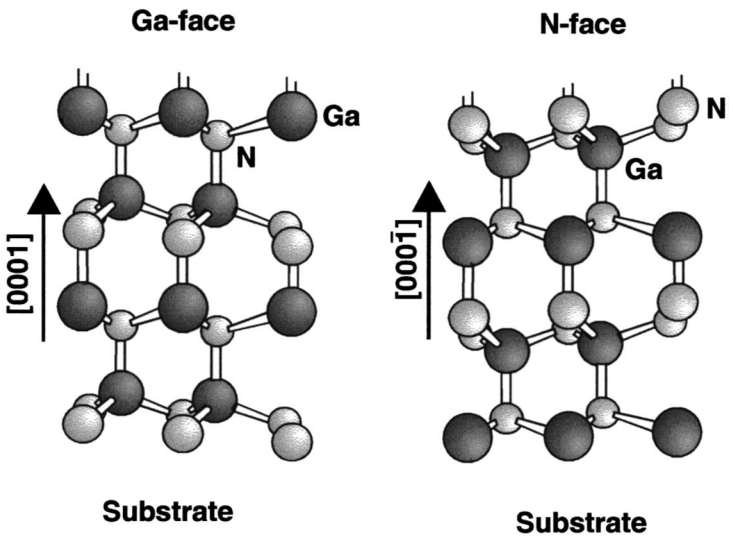
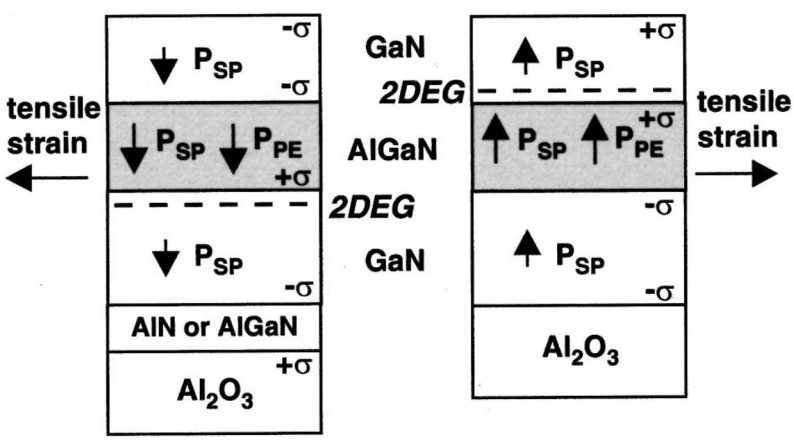


Fig. 1-8. Wurzite structure of Ga-face and N-face GaN [20]



(a) (b)

Fig. 1-9. Spontaneous and piezoelectric polarization of GaN/AlGaN/GaN heterostructure [21]

(a) Ga-face (b) N-face

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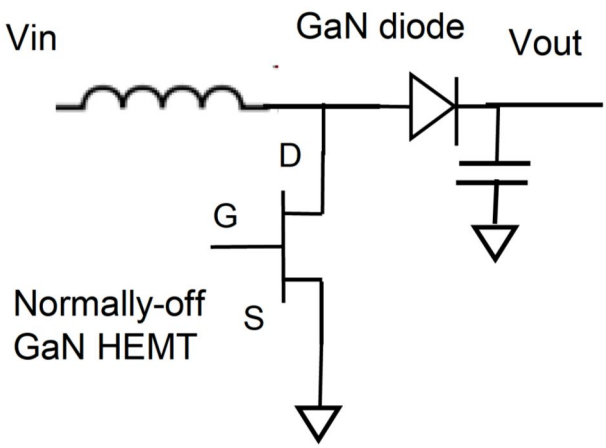
Chapter 2. Review of GaN Power Schottky Barrier Diodes

2.1 GaN power device module

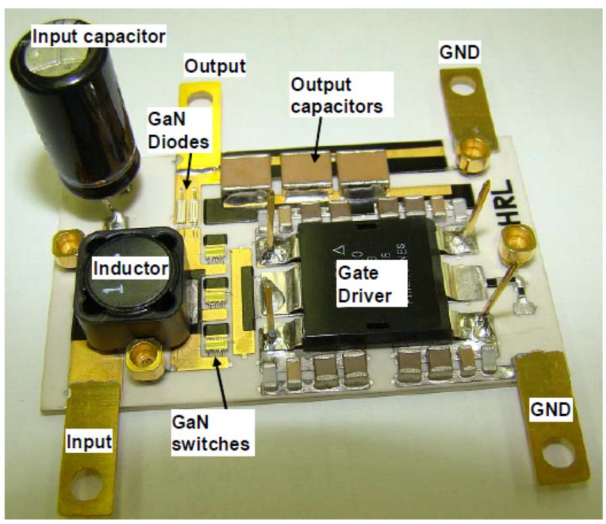
GaN-based power devices such as Schottky barrier diodes (SBDs) and high electron mobility transistors (HEMTs) have received great attention due to their superior properties, such as high saturation velocity, high carrier concentrations, and high breakdown field [1]-[6]. These properties of GaN material with high figure-of-merits enable the GaN power module to be efficient. As discussed in chapter 1.1, predictable new markets for GaN are motor inverters, solar DC/DC converters, and photovoltaic (PV) inverters, which are operated under 600 V [7]-[11].

The first all GaN boost converter with normally-off GaN HEMTs on Si substrates and GaN Schottky diodes on Sapphire substrates was demonstrated by HRL laboratory [12]. Brief schematic and photograph of the implemented boost converter are shown in Fig. 2-1 (a), (b). It is hard to fabricate the on-wafer capacitor and inductor, because of its large capacitance and inductance which is inversely proportional with a frequency. Thus, high switching frequency is favorable to reduce the volume size of chip capacitor and inductor. Figure 2-1 (c) shows the boost converter efficiency versus output power. With a maximum conversion efficiency of 95 %, power loss is about 5 %. Each loss components are charted in Fig. 2-1 (d). Switching loss possess 58 % and conduction loss by inductor, diode and FET possess 42 % of converter loss power. There has been

published data that switching loss occupies large portion of power module loss [13], [14].



(a)



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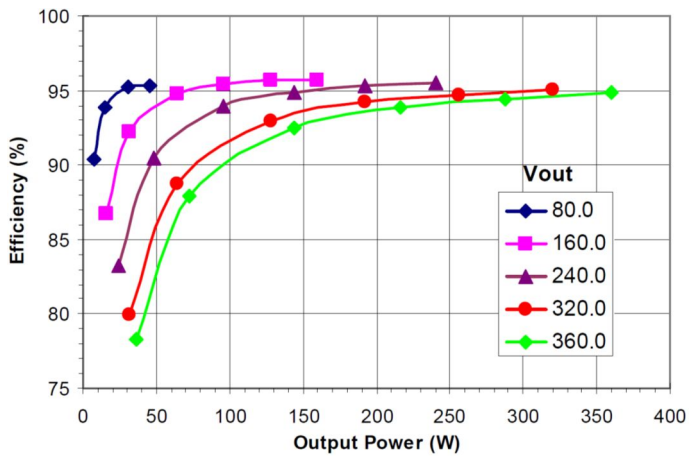
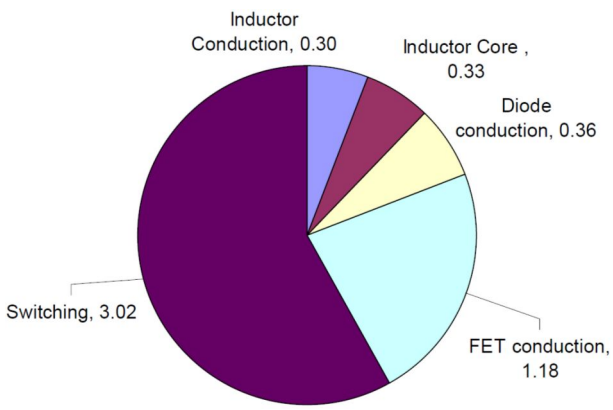


(c)



(d)

Fig. 2-1. GaN boost converter with 425 W output power at 1 MHz [12]

(50 % duty cycle, $V_{out} = 2 \times V_{in}$)

(a) Brief schematic (b) Photograph

(c) Efficiency (d) Power loss components of GaN boost converter

2.2 GaN power SBD requirements and issues

Rectifiers – in other words, diodes are indispensable device for most power electronic applications. Requirements on diodes are low turn-on voltage, low specific on-resistance, low reverse current under 1 μA, high breakdown voltage, and stable high temperature operation to minimize the power loss.

AlGaN/GaN SBDs have shown superior conduction properties due to large bandgap discontinuity of AlGaN heterostructure, spontaneous polarization due to wurzite structure, and piezoelectric polarization due to mechanical stress [15]-[18]. Wide bandgap property of GaN, paradoxically, is unfavorable in forward characteristics. Thus, device engineering is indispensable to get a two conflicting requirements on forward and reverse characteristics. Technical issues containing Schottky contact, ohmic contact, field plate, passivation, and buffer layer in AlGaN/GaN SBD to fulfill these requirements are shown in Fig. 2-2.

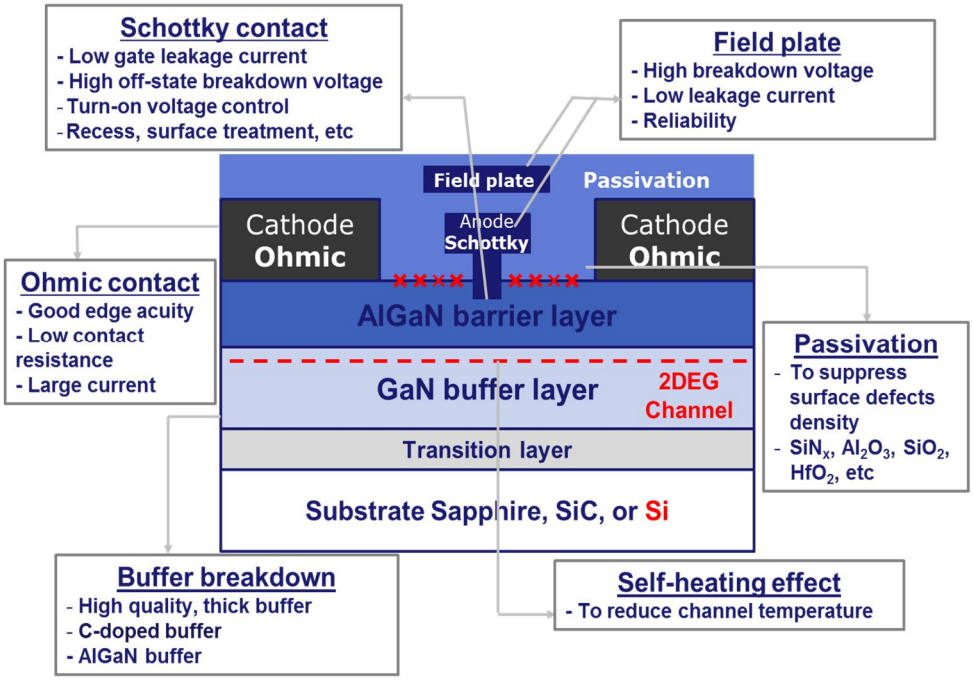


Figure 2-2. Technical issues in AlGaN/GaN SBD

2.3 GaN SBD Schemes

Various schemes used in GaN SBDs are listed in Table 2-1 and Fig. 2-3. Following paragraphs will briefly explain the various schemes ever published.

Field plate structure is a well-known scheme in GaN SBDs and HEMTs. In the reverse bias regime, electric field is concentrated at the edge of anode. With a field plate, breakdown voltage of SBD can be increased by effective electric field distribution. Recently, double field plate structure was proposed to enhance the breakdown voltage without degrade the forward characteristics [19].

In metal-semiconductor contact, Schottky barrier height is a difference between workfunction of Schottky metal and electron affinity of semiconductor. Thus, forward current of SBD can be increased with a low workfunction metal. Multi-metal stack with Ti and Ni anode was proposed to increase a forward current of GaN SBD [20]. However, reverse current was increased over 2 orders compared with Ni Schottky contact [20]. There is trade-off between forward current and reverse current. Thermal stability of a low workfunction metal would be a problem due to its relatively low melting point.

Anode edge termination is a method to enhance the reverse characteristics of SBDs. GaN Schottky barrier diodes with high-dose argon ion implantation to create a high resistivity layer at the periphery of the anode was reported [21], [22]. Elaborate control of the implantation is indispensable to gain a forward current without degradation in this approach. The breakdown voltage of SBD was increased with increasing implant length in the lateral direction due to the widening of depletion region [21].

Epi-layer engineering is essential to improve the GaN device performance. AlGaN/GaN SBD with silicon carbon nitride capping (SiCN) layer was proposed by Samsung LED [23]. Effective passivation of AlGaN surface with SiCN layer increases 2DEG carrier concentration of AlGaN/GaN heterostructure. Schottky barrier height can be decreased due to Si atoms which are acting as a positively charged ionized donors [23]. However, there is a difficulty with an epi-wafer accessibility.

Recessed anode scheme is a one of the candidates to implement the GaN SBD with a low turn-on voltage. Fully recessed SBD was reported by FBH berlin [24]. Because 2DEG channel is a highly n-doped GaN layer, Schottky barrier height can be decreased with fully recessed Schottky contact. Low damage recess etching is a critical process to achieve a low on-resistance and reverse current.

Anode and cathode of lateral field effect rectifier (L-FER) have an ohmic contacts [25], [26]. Forward and reverse current can be controlled with a fluorine-treated Schottky contact. 2DEG channel is fully depleted to acting as an enhancement-mode. Fluorine treatment can be replaced with a recess etching [27].

Table 2-1. Summary of GaN SBDs schemes

Schematics	Pros	Cons	References
Multiple field plate	High breakdown voltage	Additional process steps	[19]
Multi-metal stack anode	Low turn-on voltage High forward current	High reverse current Thermal stability	[20]
Anode edge termination	High breakdown voltage	Implantation optimization Special dopant (Fe)	[21], [22]
Capping layer engineering	Low turn-on voltage High forward current	Epi-layer growth	[23]
Recessed anode	Low turn-on voltage High forward current	Recess etching damage	[24]
Lateral field effect rectifier	Low turn-on voltage High forward current	F-ion controllability Uniformity	[25]-[27]

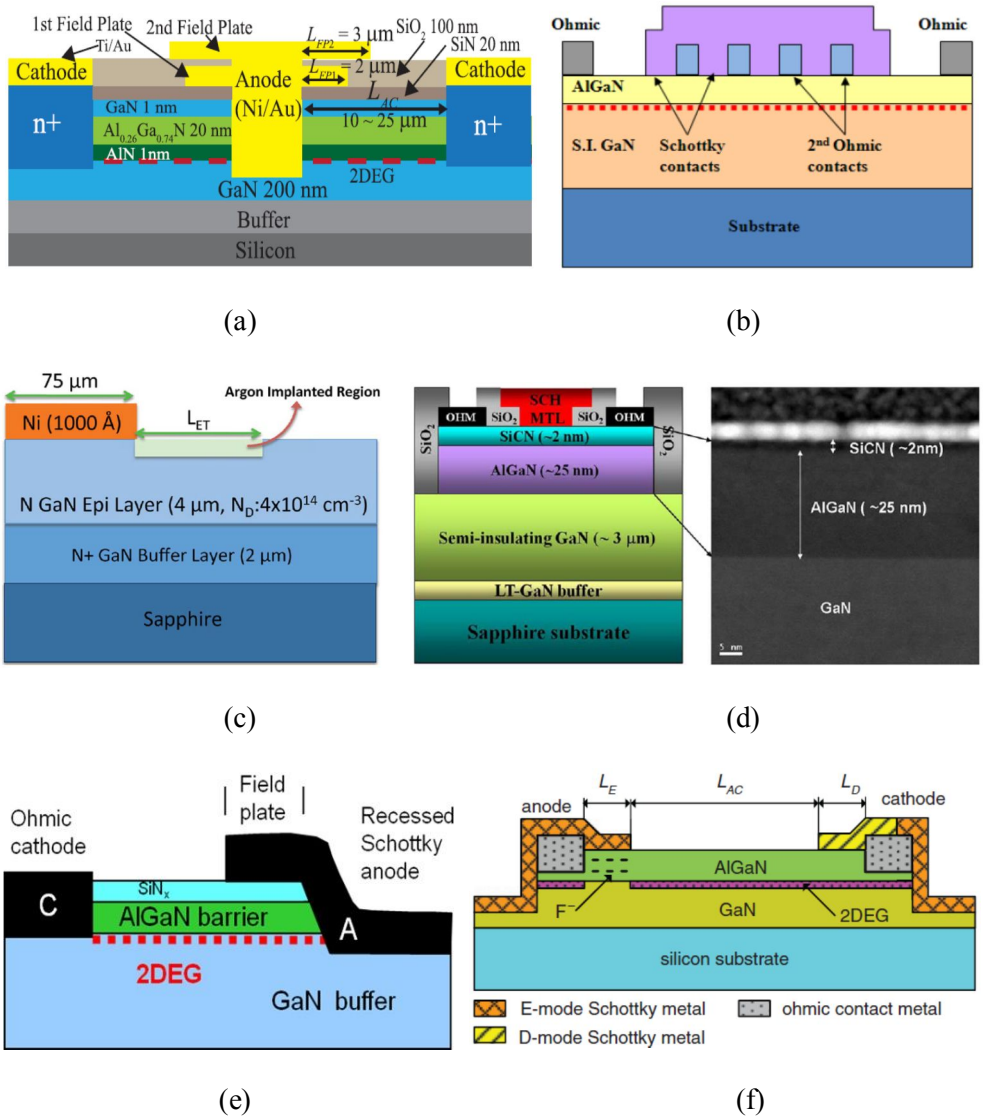


Fig. 2-3. Various GaN SBDs schematics [19]-[27]

(a) Multiple field plate (b) Multi-metal stack anode

(c) Anode edge termination (d) Capping layer engineering

(e) Recessed anode (f) Lateral field effect rectifier

2.4 SBD and HEMT on AlGaN/GaN heterostructure with SiCN capping layer

2.4.1 Introduction

Passivation of an AlGaN/GaN heterostructure is essential to improve the surface states which can cause the leakage current and current collapse. Generally, passivation layers are grown separately with epi-layers (i.e., ex-situ). It was also reported that an in-situ grown SiN_x layer is more effective in passivating the surface of the AlGaN/GaN HEMT, because epi-layers are protected during processing [28].

Protection diodes were used to protect the device during IC operations, like class-S switch mode amplifier and power switching ICs. There are some researches on AlGaN/GaN HEMT with an integrated Schottky-drain protection diode [29], [30]. The problem of this approach is a reduced drain current due to the voltage drop and resistance of a Schottky-drain diode.

In this chapter, demonstration of the AlGaN/GaN HEMT with an in-situ deposited SiCN capping layer for improved electrical characteristics. Self-protected HEMT with a reverse drain blocking capability were also demonstrated on SiCN capping layer.

2.4.2 Characteristics of epi-wafer

AlGaN/GaN heterostructure with the in-situ SiCN capping layer proposed in this paper was grown on 4-in (0001) c-plane sapphire substrates using metal-organic chemical vapor deposition (MOCVD) [23]. Trimethylgallium (TMGa), trimetahylaluminum (TMAl), carbontetrabromide (CBr_4), ditertiarybutylsilane (DTBSi), and ammonia (NH_3) were used for the precursors for Ga, Al, C, Si, and N, respectively [23]. The layer structure consists of a 30-nm-thick low temperature (LT) GaN initial nucleation layer, a 3-μm-thick highly resistive GaN buffer layer, a 25-nm-thick $Al_{0.27}Ga_{0.73}N$ barrier, and a 5-nm-thick SiCN capping layer in growth sequence. All layers except the LT-GaN nucleation layer were grown at 1100 °C [23]. An $Al_{0.27}Ga_{0.73}N$/GaN heterostructure without the SiCN capping layer was also grown for comparison. Figure 2-4 shows the epi-structure with SiCN capping layer.

Root-mean-square (RMS) roughness of the surface with and without SiCN cap layer is shown in Fig. 2-5. RMS roughness was decreased from 0.60 nm to 0.48 nm with 5-nm-thick SiCN capping layer. Hall measurement data for AlGaN/GaN heterostructure with and without SiCN cap layer are depicted in Fig. 2-6. 2DEG carrier concentration was increased about 51 % with 5-nm-thick SiCN cap layer. Possible reason for the increase of 2DEG concentration is the positive interface ionic charges generated during the growth of the SiCN cap layer, such as Si^+ [31]. The Si atoms located at the SiCN/AlGaN interface act as positively charged ionized donors and hence partially neutralize the negative polarization charges of

the AlGaN surface, which thereby increases the 2DEG density to satisfy the charge neutrality [23].

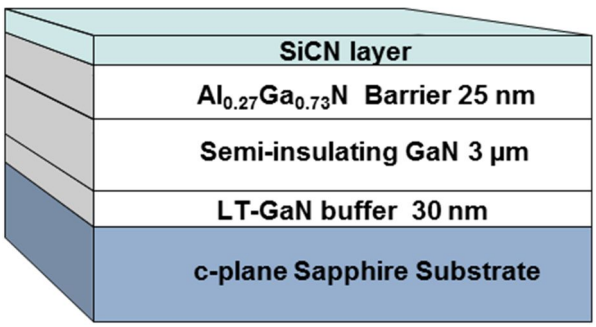


Fig. 2-4. Epi-structure of AlGaN/GaN heterostructure with SiCN capping layer

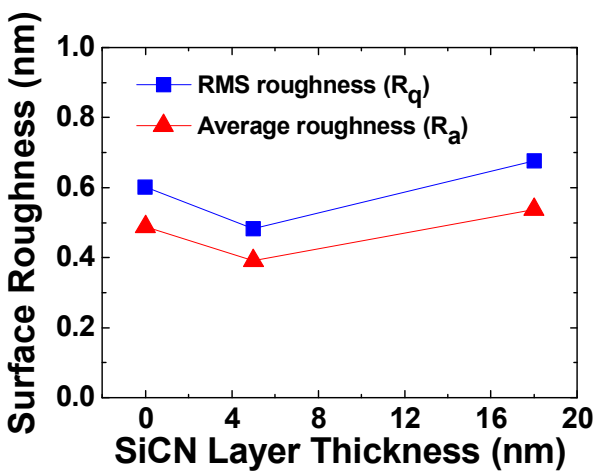


Fig. 2-5. Surface roughness of AlGaN/GaN heterostructure with and without SiCN capping layer

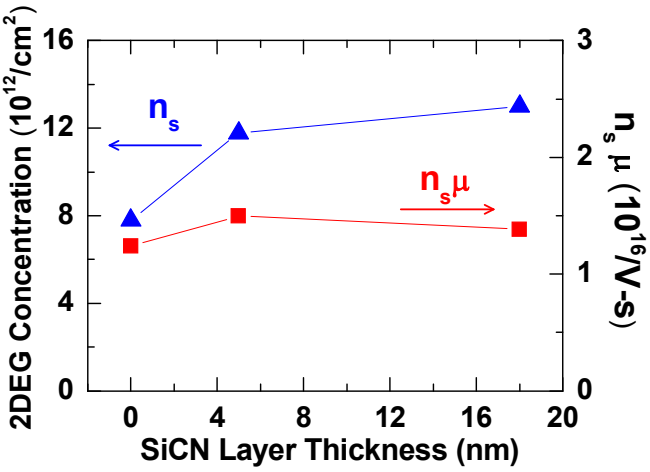
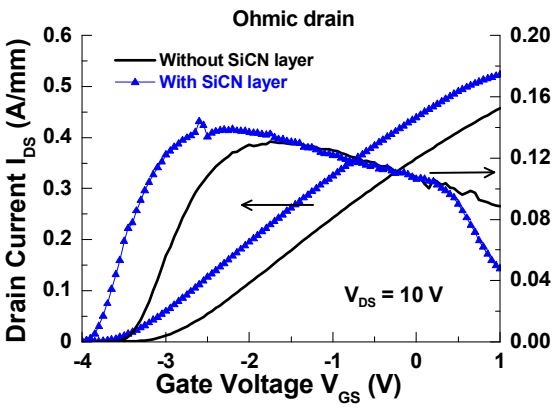


Fig. 2-6. Hall measurement results with and without SiCN capping layer

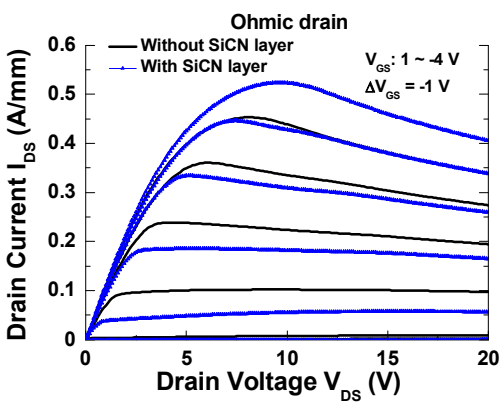
2.4.3 AlGaN/GaN HEMT with a SiCN cap layer (SiCN-HEMT)

Schottky HEMT and protection diode integrated HEMT were fabricated on AlGaN/GaN heterostructure with 5-nm-thick SiCN capping layer. Device mesa isolation was performed using BCl_3/Cl_2 mixture by inductively coupled plasma reactive ion etching (ICP-RIE). After cleaning with piranha and diluted HF (1:10) for 10 min, 30-nm-thick SiN_x layer was deposited using inductively coupled plasma chemical vapor deposition (ICP-CVD) at 350 °C. Ohmic contact metals of Si/Ti/Al/Mo/Au (5/20/80/35/50 nm) were deposited and followed by thermal annealing at 820 °C for 30 s in nitrogen ambient. The measured contact resistance and sheet resistance were 0.25 Ω·mm and 368 Ω/sq, respectively. Next, wet etching was used to etch the gate window, because SF_6 gas plasma can etch the SiCN cap layer. The next patterning process defined the gate and gate field plates. Finally, Ni/Au (20/380 nm) was deposited as a gate metal.

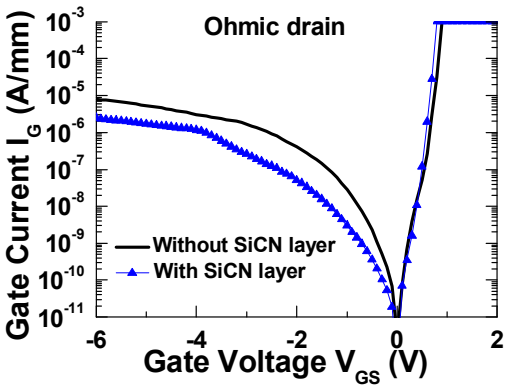
The gate length (L_G) and gate field plate length were 2 μm. The gate-to-source distance (L_{GS}) and gate-to-drain distance (L_{GD}) was 3 and 15 μm, respectively. Figure 2-7 shows the measured output characteristics of fabricated HEMTs with and without SiCN cap layer. Maximum drain current was increased 15 % in SiCN-HEMT compared with the conventional HEMT. Maximum transconductance was also increased 10 %, even though gate-to-channel distance was increased by the SiCN layer thickness. The reason for these improvements in SiCN-HEMT is due to the increase of the carrier concentration. The decrease of gate leakage current in SiCN-HEMT can be explained by the suppression of a tunneling current as explained in [23].



(a)



(b)



(c)

Fig. 2-7. Output characteristics of ohmic-drain HEMTs

(a) Transfer curve (b) Family curve (c) Gate current

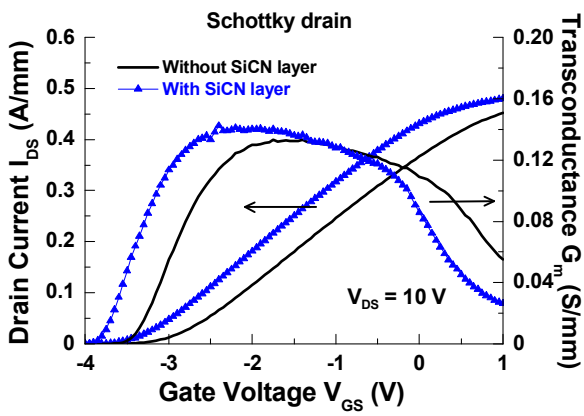
2.4.4 AlGaN/GaN HEMT with an integrated Schottky-drain protection diode

Purpose of the HEMT with a protection diode is to suppress a current flow in the HEMT during reverse bias conditions. GaN integrated Schottky-drain protection di-ode is promising, because GaN SBDs show high switching speed with low on resistance and large forward current. Major problem in integrated Schottky-drain protection diode is the knee voltage due to the voltage drop in Schottky contact at drain.

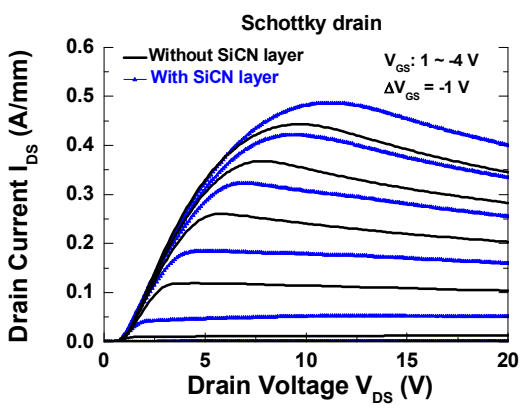
HEMT with an integrated Schottky-drain protection diode was fabricated. Measured output values of the AlGaN/GaN HEMT with Schottky-drain protection diode are shown in Fig. 2-8. Maximum drain current and transconductance of the SiCN-HEMT with a Schottky drain were increased by 10 % and 7 %, respectively. Moreover, gate leakage current is reduced in Schottky-drain HEMT compared with

ohmic-drain HEMT. However, Schottky-drain causes the decrease of maximum drain current 7 %, compared with an ohmic-drain HEMT. This is because a Schottky-drain has a higher contact resistance than an ohmic-drain. It is encouraging that the drain current can be increased with a SiCN capping layer, even protection diode was integrated. Turn on voltage of the Schottky-drain diode was 0.7 V for both with and without SiCN capping layer. Table 2-2 shows summary of the output characteristics of fabricated HEMTs.

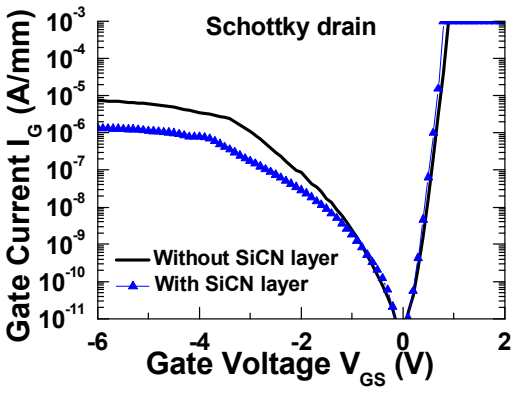
The reverse drain current in the on-state (V_{GS} = 0 V) and the threshold state (V_{GS} = -4 V) are shown in Fig. 2-9. It shows the reverse blocking capability over -100 V for both on and threshold state of the Schottky-drain diode. It was expected that a lower knee voltage due to the lower Schottky barrier height of SiCN-SBDs [23]. However, there was not a noticeable difference in a knee voltage with and without SiCN capping layer, as shown in Fig. 2-8. Thus, further studies are needed to lower the knee voltage.


Schottky drain
Without SiCN layer
With SiCN layer
V_{DS} = 10 V
Drain Current I_{DS} (A/mm)
Transconductance G_m (S/mm)
Gate Voltage V_{GS} (V)
0.6
0.5
0.4
0.3
0.2
0.1
0
0.20
0.16
0.12
0.08
0.04
0
-4
-3
-2
-1
0
1

(a)


Schottky drain
Without SiCN layer
With SiCN layer
V_{GS}: 1 ~ -4 V
ΔV_{GS} = -1 V
Drain Current I_{DS} (A/mm)
Drain Voltage V_{DS} (V)
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
5
10
15
20

(b)



(c)

Fig. 2-8. Output characteristics of Schottky-drain HEMTs

(a) Transfer curve (b) Family curve (c) Gate current

Table 2-2. Summary of output characteristics of fabricated HEMTs

	Ohmic-drain		Schottky-drain	
	Without SiCN layer	With SiCN layer	Without SiCN layer	With SiCN layer
$I_{DS, Max}$ (mA/mm)	453.0	523.2	443	486
$G_{m, Max}$ (mS/mm)	130.2	143.8	133	143
I_G at V_{GS} = -6 V (μA/mm)	7.9	2.5	7.4	1.3

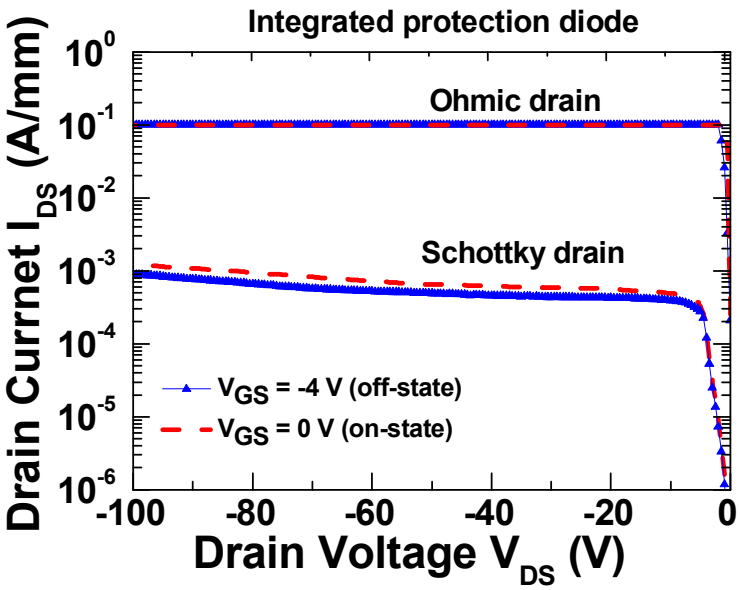


Fig. 2-9. Reverse blocking capability of HEMT with integrated protection diode

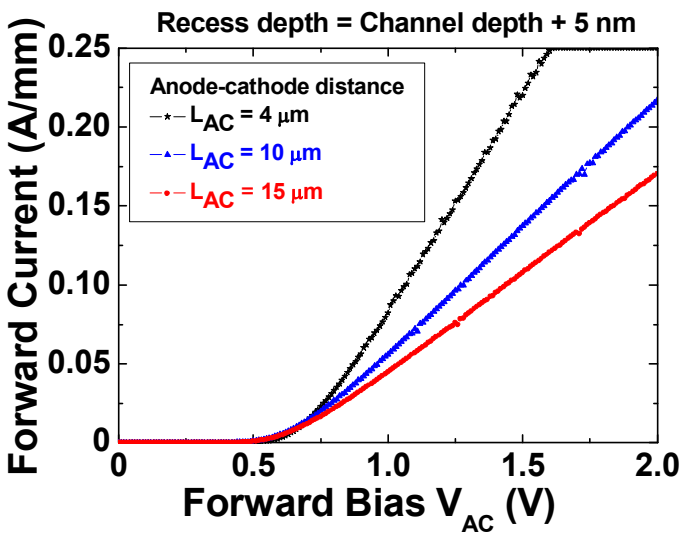
2.5 Recessed SBD and motivation of study

Fully recessed GaN SBD was fabricated to achieve a low turn-on voltage. Samples were passivated with 200-nm-thick SiN_x layer after mesa isolation. Ohmic contact was formed with 800 °C for 1 min annealing in N_2 ambient. Next, anode region was fully recess-etched under the 2DEG channel with depth of 29 nm. Additional Ni/Au as a Schottky contact and 2 μm length field plate metal was deposited.

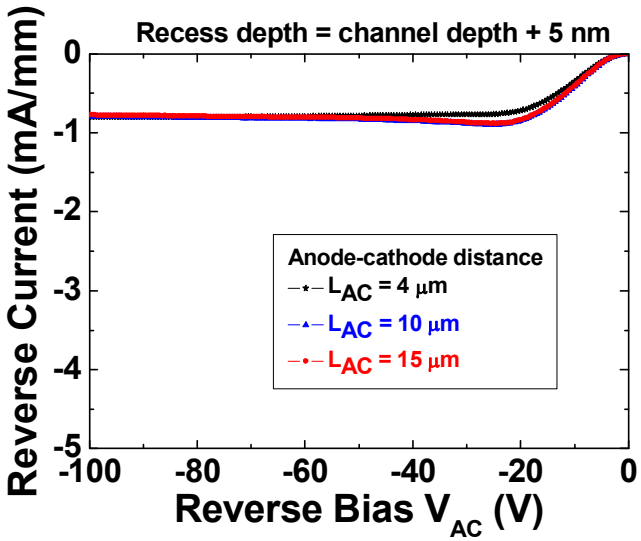
Figure 2-10 shows the electrical measurement data of the fabricated SBDs. Fig. 2-10 (a) and (b) show the forward and reverse characteristics of fabricated SBDs

with respect to anode-to-cathode distance (L_{AC}). The on-resistances of SBDs are inversely proportion to L_{AC}, because of channel resistance. However, reverse current are not varied with a L_{AC}, which means that reverse current are mainly affected by Schottky contact rather than channel resistance. The breakdown voltage was measured with Tektronix 370A curve tracer as shown in Fig. 2-11. The hysteresis is due to the capacitance in the bias tee. The SBD with L_{AC} of 10 μm and L_{AC} of 15 μm were measured as 536 V and 881 V, respectively. Although forward and breakdown characteristics of GaN SBDs were acceptable, large reverse current of fabricated SBD would severe influence on power device loss. The reverse current of SBD should be lower than 1 μA/mm for low loss operation of power systems.

Epi-layer engineering scheme reported in chapter 2.4 would be a promising candidate for the high efficiency power devices. However, epi-growth accessibility frustrates this approach which require high quality MOCVD equipment. Thus, following sections will discuss on recessed anode scheme. To fulfill the requirements on GaN SBD stated in chapter 2.2, in-depth study will be presented in following sections from recess etching to packaging methodology.


Recess depth = Channel depth + 5 nm
Anode-cathode distance
L_AC = 4 μm
L_AC = 10 μm
L_AC = 15 μm
Forward Current (A/mm)
0
0.05
0.10
0.15
0.20
0.25
0
0.5
1.0
1.5
2.0
Forward Bias V_AC (V)

(a)



(b)

Fig. 2-10. I-V characteristics of fully recessed GaN SBD

(a) Forward I-V curve (b) Reverse I-V curve

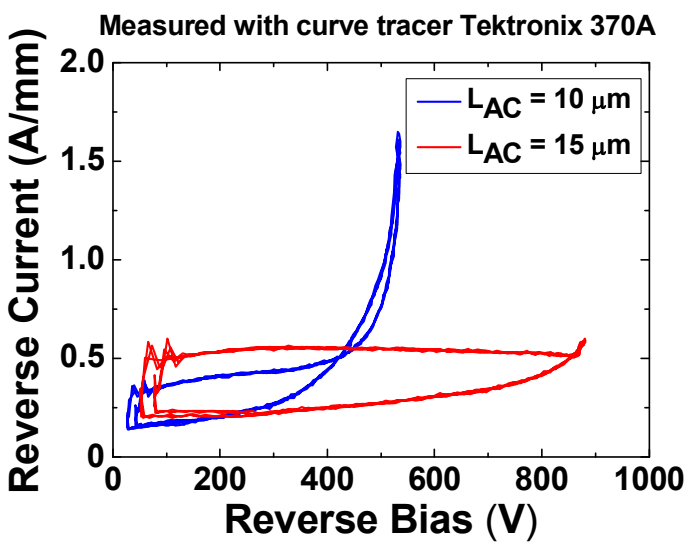


Fig. 2-11. Breakdown characteristics of fully recessed GaN SBD

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Chapter 3. Low Damage Digital Etching

3.1 An overview of digital etching

There have been numerous studies on reliability issues caused by surface imperfection of GaN epitaxial layer [1]-[3]. Moreover, device fabrication process involves plasma etching and high temperature annealing, which may generate GaN surface defects. The effects of the plasma treatment using N_2, NH_3, O_2, N_2O, CF_4, and SF_6 on GaN surface was investigated by several groups [4]-[14]. The basic purpose of plasma surface treatment is to remove unwanted contaminations on GaN surface. With O_2 or N_2O plasma treatment, oxide residues would be formed on GaN surface and it may give bad influences on current collapse and reliability [15], [16]. Thus, it is needed to remove the formed oxide layer after plasma treatment. Stoichiometric alterations of nitrogen and gallium deficiencies occur after each step of GaN surface treatment. Thus, the electrical characteristics of GaN HEMTs should be affected by such surface treatment.

Recessed gate is a well-known structure to implement SBDs with a low turn-on voltage and normally-off HEMTs which have received great attentions for power electronics applications [17], [18]. Wet recess etching is a conventional process in AlGaAs/GaAs heterostructures, because of moderate etch rate and etch stop layer. On the other hand, GaN is hard to etch away by wet etchants, thus dry recess etching is a prevalent process in AlGaN/GaN heterostructures. However, GaN surface is prone to be damaged by dry recess etching. Several groups suggested a so-called digital etching as a low damage recess etching technique [18]-[20].

Digital recess etching is consecutive repetitions of epitaxial layer oxidation and formed oxide removal process. The formed oxide can be etched with a wet etchant or dry plasma etching. Digital etching can be classified with wet digital etching and dry digital etching, with regard to the oxide etching method.

Figure 3-1 and 3-2 show the etch rate of wet digital etching using O_2 as an oxidation agent and HCl as a wet etchant. It is noticeable that etch rate increase with oxidation power increase. Etch depths also increase almost linearly, which means that wet digital etching is a self-limiting process. HCl only etches the formed oxides, not the GaN layer, thus low damage etching is possible. Reverse gate leakage current of recessed GaN HEMTs were decreased from 950 μA to 3 μA for Cl_2 recessed and digitally recessed structures, since the process does not intrinsically require the action of a plasma [19]. Drawback of the wet digital etching is a relatively long process time, because oxidation and etching are performed at different places, i.e., oxidation plasma chamber and wet station, respectively. Table 3-1 shows the wet digital etching condition used in device fabrication by UCSB.

Dry digital etching was reported by HRL laboratories [20]. Figure 3-3 shows the etch rate of dry digital etching using O_2 as an oxidation agent and BCl_3 as a dry etching plasma. The oxidation agent was O_2 plasma identical with a wet digital etching, however BCl_3 plasma was used to etching an oxidation layer. This process is called as semi-self-limiting, because BCl_3 plasma also can etch the GaN epi-layer unlike HCl wet etchant. The merit of the dry digital etching is a relatively short process time, because oxidation and etching are performed in one chamber. On the other hand, possibility of plasma damage on epi-layer is a drawback of dry digital etching due to its semi-self-limiting nature. Table 3-2 shows the dry digital

etching condition used in device fabrication by HRL laboratories.

In following sections, wet digital etching was developed and adopted in GaN devices because of its low damage and self-limiting property compared with a dry digital etching. Developed digital etching was estimated by Hall-effect measurements and buffer leakage current measurements. Influence of a wet digital etching on the electrical characteristics of recessed SBD and GaN HEMT are also reported.

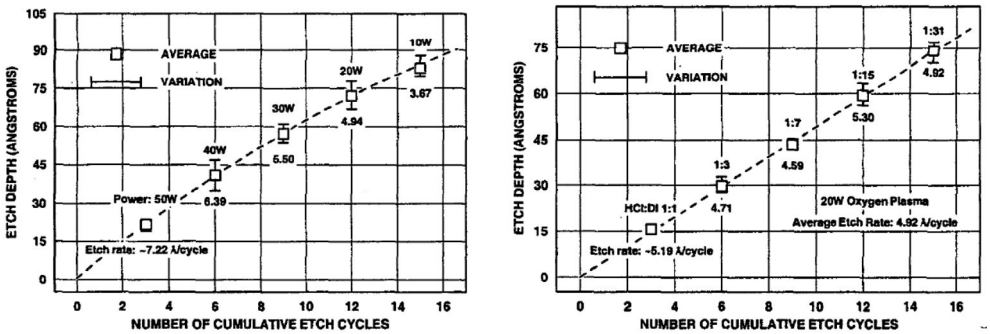


Fig. 3-1. Measured etch depths as a function of wet digital etch cycles for different oxygen plasma powers [19]

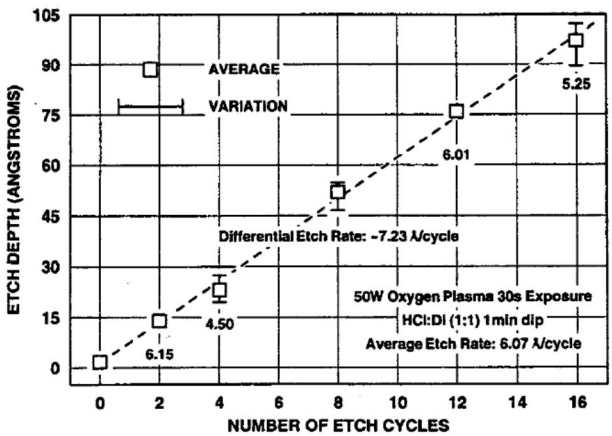


Fig. 3-2. Measured etch depths as a function of wet digital etch cycles with 50 W oxygen plasma [19]

Table 3-1. Wet digital etching condition by UCSB [19]

	Gas Chemical	Power (W)	Pressure (mTorr)	Time (sec)
Oxidation	O_2	50	300	30
Etch	HCl (1:1)	-	-	60

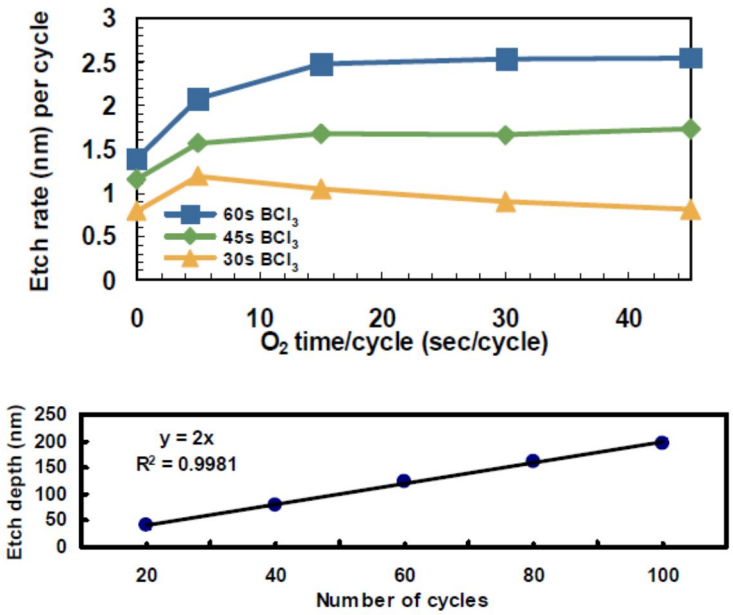


Fig. 3-3. Measured data of etch rate per cycle for a fixed BCl_3 plasma time per cycle and varying oxygen plasma time per cycle [20]

Table 3-2. Dry digital etching condition by HRL laboratories [20]

	Gas Chemical	Power (W)	Pressure (mTorr)	Time (sec)
Oxidation	O_2	50	100	30
Etch	BCl_3	15	15	45

3.2 Development of wet digital etching technique

Wet etching is pursued, because of low damage etching and self-limiting property. Samples were prepared to measure the digital etch rate. It is hard to find an etched region with depth under 10 nm by microscope, thus auxiliary structure is needed. Mesa isolation structure with a depth of 200 nm was formed after cleaning with sulfuric peroxide mixture (SPM) solution and hydrofluoric (HF) acid. 10-nm-thick SiN_x layer was deposited on GaN surface. SiN_x layer was etched with a SF_6 plasma and wet digital recess etching was executed on GaN surface with a SiN_x hard mask. N_2O plasma was preferred for surface oxidation, because O_2 plasma may create deep level traps which is related with a nitrogen deficiencies [10]. The oxidation using N_2O plasma was carried out with a low power of 20 W to avoid a plasma damage under a gas flow rate of 40 sccm, a chamber pressure of 200 mTorr, and a time of 180 sec for 1 cycle. The formed oxide removal was carried out by dipping the samples in diluted HCl (1:1) solution for 60 sec. Table 3-3 shows the developed wet digital etching technique condition.

Figure 3-4 shows the atomic force microscopy (AFM) image of a GaN surface after wet digital etching. The etch rate was measured as a function of number of digital etching cycles, i.e., 3, 6, 10 cycles as shown in Fig. 3-5 (a). Measured etch rate with respect to oxidation RF power is shown in Fig. 3-5 (b). Etch depths as a function of wet digital etching cycles and different oxygen plasma powers are depicted in Fig. 3-1, and Fig. 3-2. Suggested etch rate described in Fig. 3-1 is 0.49 nm/cycle for 20 W which is almost identical with Fig. 3-5 (a), although we used N_2O plasma as an oxidation agent. Figure 3-5 (c) shows the measured root mean

square (RMS) roughness of the GaN surface before and after wet digital etching. RMS roughness of etched surface was in the range of 0.56 ~ 0.59 nm, which is almost identical with a non-recessed surface.

Table 3-3. Developed wet digital etching condition

	Gas Chemical	Power (W)	Pressure (mTorr)	Time (sec)
Oxidation	N_2O	20	200	180
Etch	HCl (1:1)	-	-	60

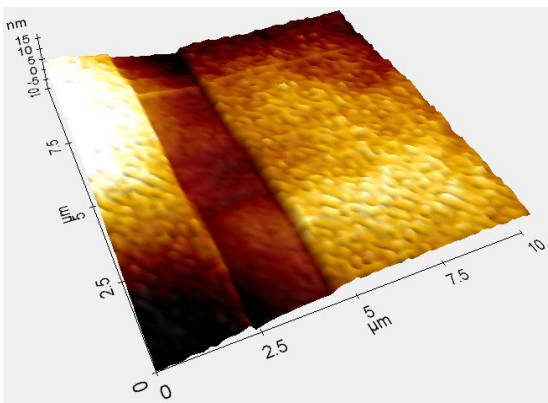
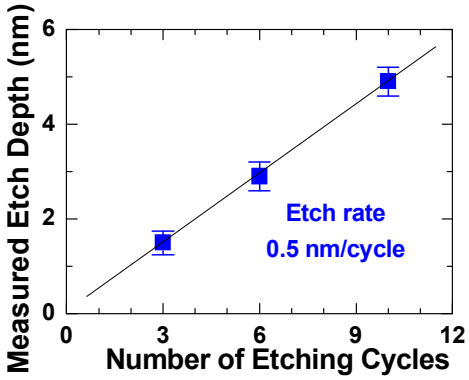
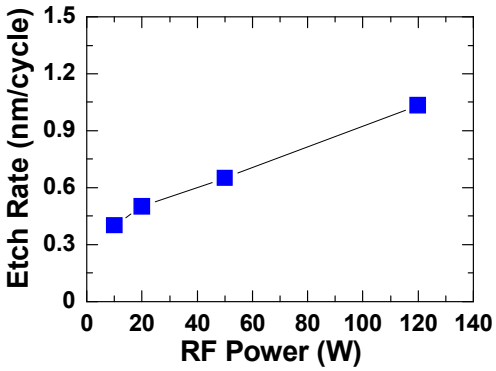


Fig. 3-4. AFM image of a GaN surface after wet digital etching

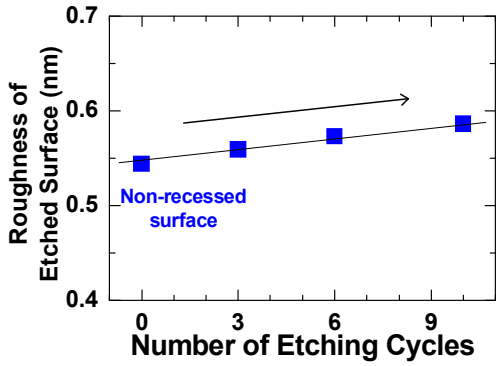
(Recess width = 2 μm, depth = 4.3 nm)



(a)



(b)



(c)

Fig. 3-5. Etch rate and roughness of GaN surface after wet digital etching

(a) Etch depth vs. number of etching cycles (b) Etch rate vs. RF power

(c) RMS roughness vs. number of cycles

3.3 Hall-effect measurement

Hall pattern was fabricated to verify the influence of digital etching on GaN surface. Mesa isolation was defined using inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3/Cl_2 gas (=2/18 sccm) mixture. The mesa etching was performed with a source power of 200 W, a bias power of 15 W, and a chamber pressure of 5 mTorr. DC self-bias of mesa etching condition was 60 V. A Si/Ti/Al/Mo/Au (=5/20/80/35/50 nm) metal stack was evaporated and annealed at 800 °C for 30 s in N_2 ambient for the ohmic contact formation. Figure 3-6 shows the microscope image of the fabricated Hall pattern.

In order to investigate the digital etching induced damage, the active area was exposed to the N_2O plasma and diluted HCl. Measured 2DEG carrier concentration (n_s) and multiplication of 2DEG concentration and electron mobility ($n_s\mu$) are shown in Fig. 3-7. It was observed that GaN surface and 2DEG was not deteriorated after digital etching. GaN surface and 2DEG can be degraded by an ion bombardment if high power plasma is applied on GaN surface [4]. 2DEG concentration was increased after digital etching which means the shift of surface potential. These results could be explained with the reduced surface trap charges (σ_{trap}) and the lowered surface potential by digital etching [4], [10]. Figure 3-8 shows the schematic of band diagram of AlGaN/GaN heterostructure with and without N_2 plasma treatment. Impurities on the GaN surface, (e.g., carbon, oxygen, excess Ga atoms) can be react with the N_2 plasma, hence leading to a surface stoichiometry recovery [4]. In this experiment, GaN surface traps would be increased during high temperature annealing.

Mesa-etched area was exposed to the digital etching, to investigate the digital etching effect on damaged surface. Figure 3-9 shows the buffer leakage current with and without digital etching. Buffer leakage current was drastically reduced by more than four orders of magnitude with digital etching. Initial buffer leakage current was about 1 μA/mm at -100 V, which might flow through the surface traps generated from dry mesa etching. The decrease in buffer leakage current with digital etching on mesa-etched GaN surface means that buffer leakage current was strongly dependent on surface conditions [14].

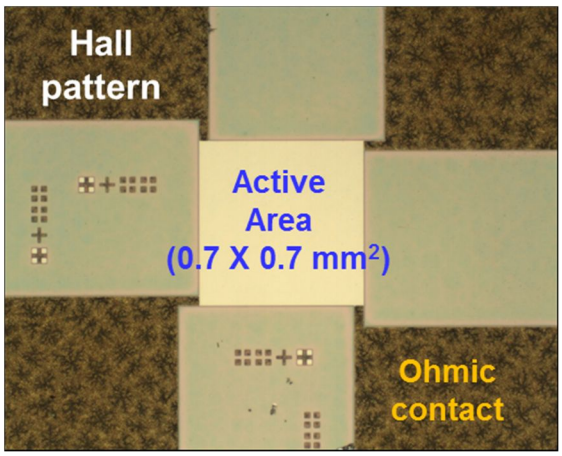


Fig. 3-6. Microscope image of the fabricated Hall pattern

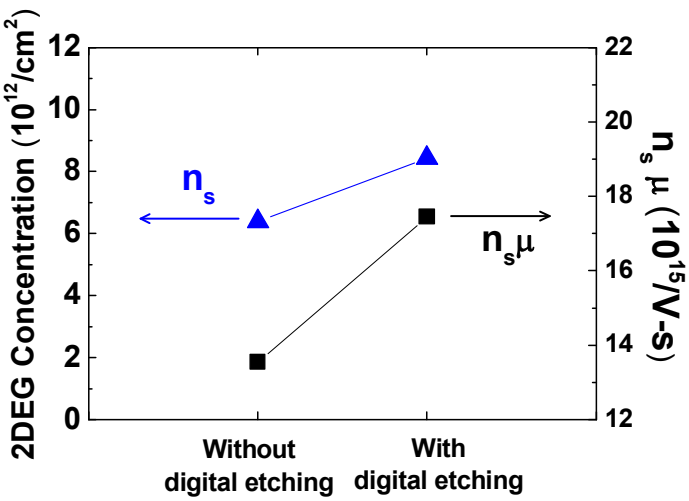
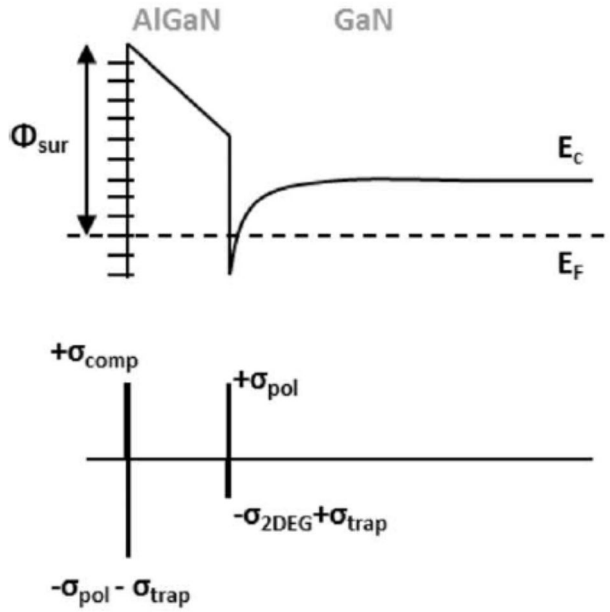
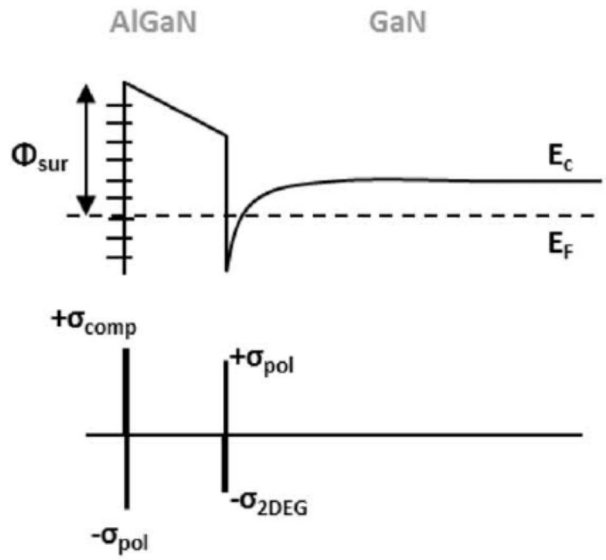


Fig. 3-7. 2DEG concentration (n_s) and multiplication of 2DEG concentration and electron mobility ($n_s\mu$) with and without digital etching



(a)



(b)

Fig. 3-8. Schematic of band diagram of AlGaN/GaN heterostructure [4]

(a) Without N_2 plasma treatment (b) With N_2 plasma treatment

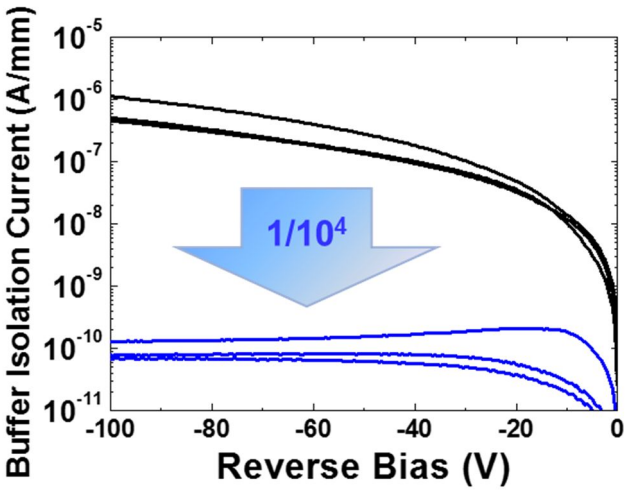


Fig. 3-9. Buffer isolation current with and without digital etching

3.4 The effects of digital etching on recessed SBDs

Figure 3-10 shows the epitaxial wafer structure for SBDs with digital etching. The epitaxial wafer structure used for SBDs consisted of a 4-nm GaN capping layer, a 20-nm $Al_{0.23}Ga_{0.77}N$ barrier, a 1.7-μm undoped-GaN buffer on an n-type Si (111) substrate. A schematic process flow of the SBD is shown in Fig. 3-11. Ohmic contact was first formed and mesa isolation was followed. The measured sheet resistance, carrier mobility, and 2DEG carrier concentrations were 410 Ω/sq, 1600 cm^2/Vs, and 1×10^{13} / cm^2, respectively. Next, anode region was fully recessed under the 2DEG channel to define a recessed Schottky contact. 34-nm was etched which is 10-nm deeper than a channel depth. Anode recess was carried out using BCl_3/Cl_2 (=2/18 sccm) gas mixture with a source power of 250 W, a bias power of 5 W, and a chamber pressure of 7 mTorr. DC self-bias of recess condition was 25 V. Additional 1-cycle digital etching was performed on the recessed area to alleviate the dry etching damage. A Ni/Au (=40/160 nm) metal was deposited to form a recessed Schottky contact. Then, a non-recessed Schottky metal was evaporated for comparison with a recessed Schottky contact. Finally, 200-nm-thick SiN_x film was deposited using SiH_4/NH_3 (=8/40 sccm) gas mixture with a RF power of 300 W, a chamber pressure of 20 mTorr, and a chuck temperature of 300 °C for surface passivation. Prior to surface passivation, the in-situ N_2 plasma was executed to reduce the nitrogen vacancies as described in ref. 21.

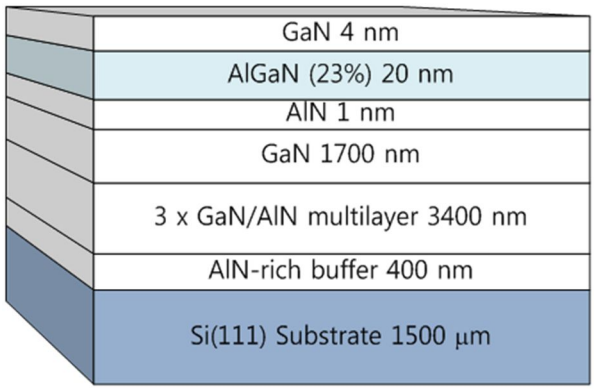


Fig. 3-10. Epitaxial wafer structure for SBDs with digital etching

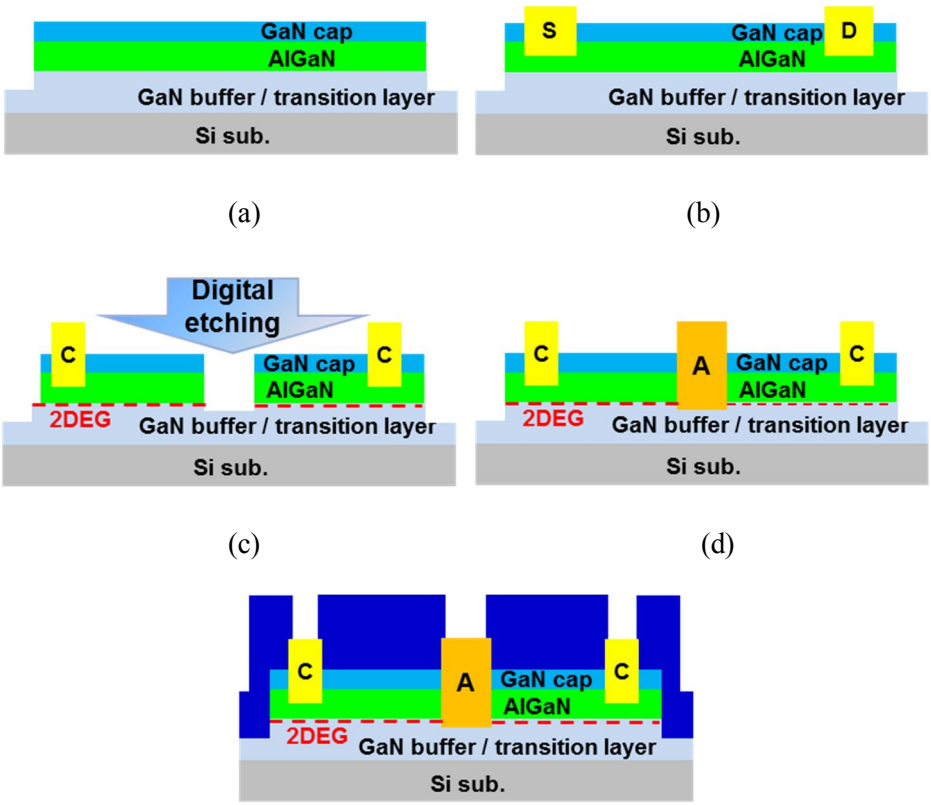


Fig. 3-11. Recessed SBD process flow with digital etching

(a) Mesa isolation

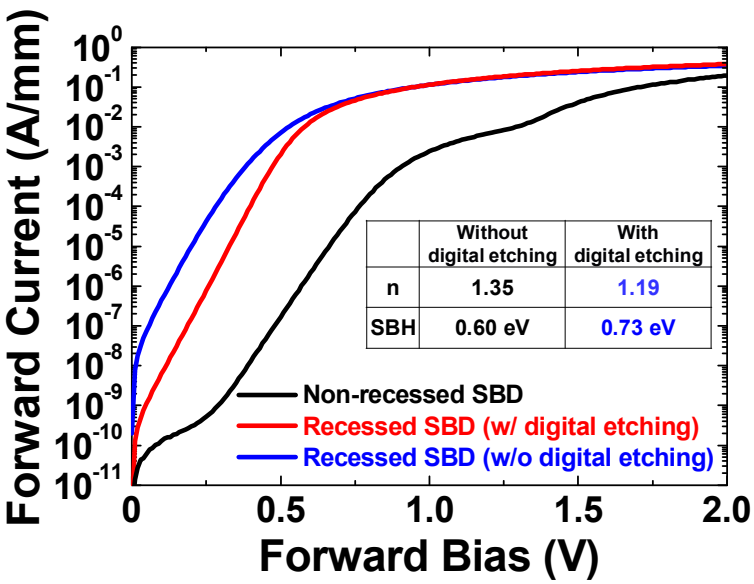
(b) Ohmic contact formation

(c) Anode recess (Dry etching, digital etching)

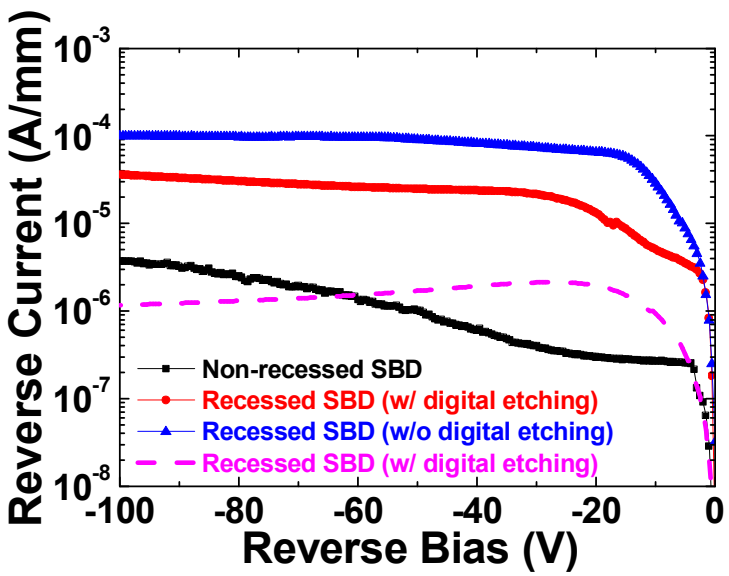
(d) Schottky metallization

(e) SiN_x passivation

Figure 3-12 shows the typical forward and reverse characteristics of the fabricated SBDs. The reduced turn-on voltages were obtained with fully recessed SBD structure compared with non-recessed SBD. The ideality factor and Schottky barrier height were 1.35 and 0.60 eV in the SBD without digital etching and 1.19 and 0.73 eV in the SBD with digital etching, respectively. The specific on-resistances were 1.28 and 1.13 $m\Omega \cdot cm^2$ for the SBDs without and with digital etching, respectively. The reverse currents were 100 and 36 μA/mm for the SBDs without and with digital etching, respectively. However, reduction of the reverse current was less than expectation from the results of chapter 3.3. This result can be explained as follows. DC self-bias of mesa etching and anode recess etching conditions were 60 V and 25 V, respectively. Etch rate of mesa etching and anode recess etching were 0.6 nm/s and 0.2 nm/s, respectively. Quality of mesa-etched GaN surface would be worse than anode recessed surface. Thus, effects of digital etching could be emphasized on mesa-etched surface. By adopting a digital etching process on both of GaN surface and anode recess area, reverse current was decreased by two orders of magnitude which is depicted as dash line in Fig. 3-12 (b). This result implies that a surface leakage current occupies a considerable portion of the overall leakage current. Reverse breakdown voltage of the fabricated SBD with an anode-to-cathode distance (L_{AC}) of 10 μm was 566 V. Figure 3-10 shows the breakdown voltage versus specific on-resistance graph.



(a)

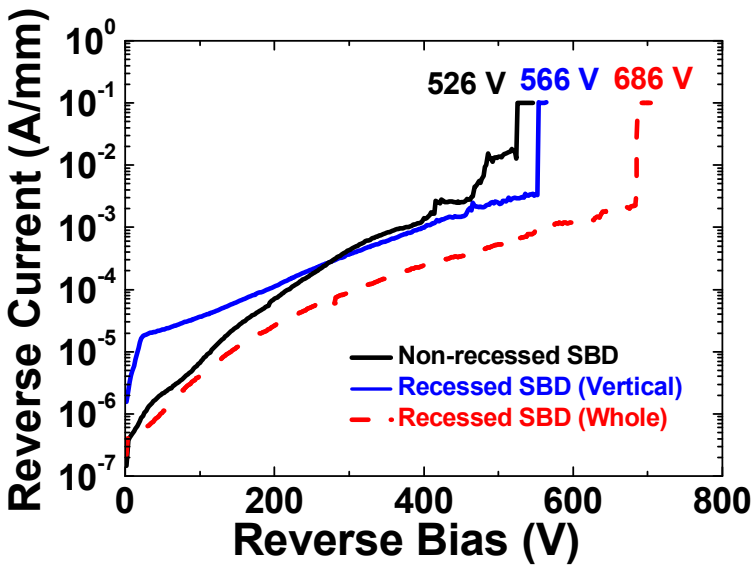


(b)

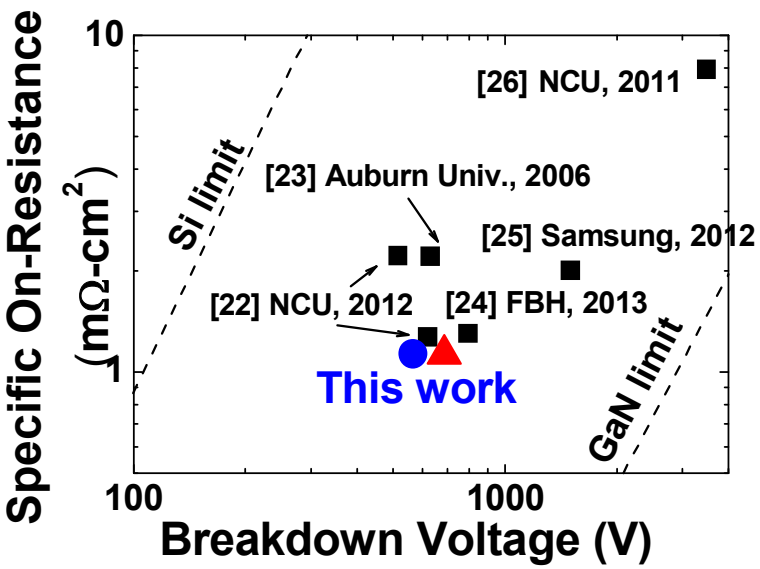
Fig. 3-12. I-V characteristics of SBD (L_{AC} = 10 μm)

(a) Forward current as a function of forward voltage

(b) Reverse current as a function of reverse voltage



(a)



(b)

Fig. 3-13. Breakdown characteristics of SBD (L_{AC} = 10 μm)

(a) Breakdown characteristics, Vertical; digital etching on anode recess area, Whole; digital etching on both of GaN surface and anode recess area

(b) R_{on} vs. breakdown voltage graph

3.5 The effects of digital etching on Schottky HEMTs

Figure 3-14 shows the epitaxial wafer structure for HEMTs with digital etching. The epi-layer structure consisted of a 4-nm GaN capping layer, a 20-nm $Al_{0.23}Ga_{0.77}N$ barrier, a 300-nm undoped GaN layer, and 3.9-μm carbon-doped GaN buffer layer on a Si substrate was used for this experiment. A schematic process flow of the Schottky HEMT is shown in Fig. 3-15. Ohmic contact was first formed and mesa isolation was followed for device isolation. The measured sheet resistance, carrier mobility, and 2DEG carrier concentrations were 477 Ω/sq, 2000 cm^2/Vs, and 8×10^{12} / cm^2, respectively. 1-cycle digital etching was performed on whole GaN surface to relieve the surface damage due to high temperature annealing process for ohmic contacts. A Ni/Au (=20/180 nm) metal stack was evaporated for the gate metallization. Prior to the gate metal deposition, we performed buffered oxide etchant (1:30) cleaning for 30 sec. Next, 200-nm-thick SiN_x film was deposited using SiH_4/NH_3 (=8/40 sccm) gas mixture with a RF power of 300 W, a chamber pressure of 20 mTorr, and a chuck temperature of 300 °C for surface passivation. Finally, gate field plate was deposited. The gate length (L_G) and the gate field plate length were 2 μm. The gate-to-source distance (L_{GS}) and the gate-to-drain distance (L_{GD}) were 3 μm and 10 μm, respectively.

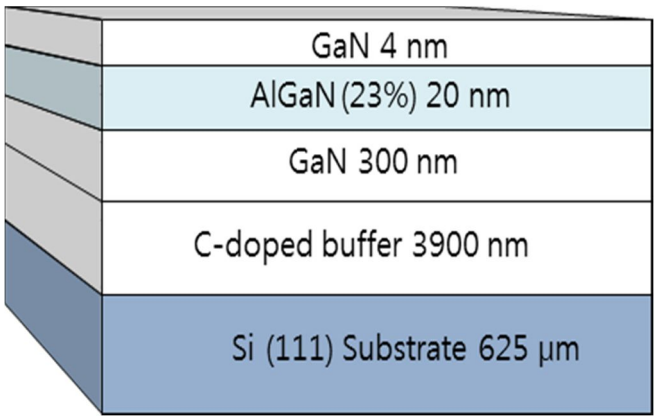


Fig. 3-14. Epitaxial wafer structure for HEMTs with digital etching

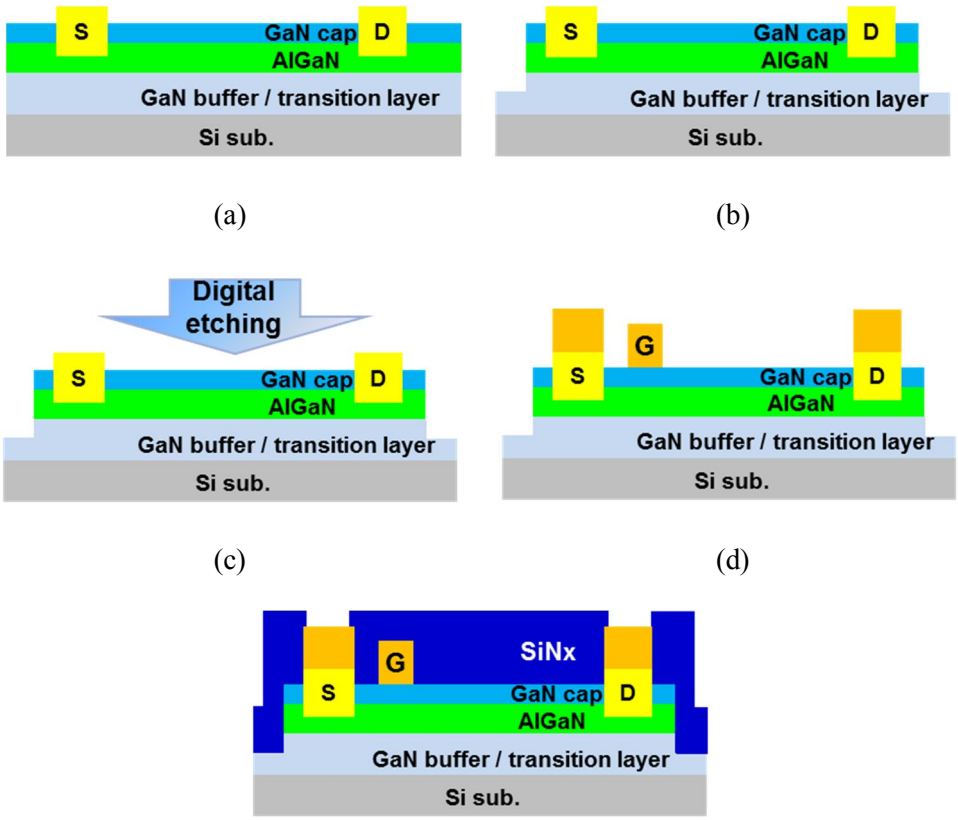


Fig. 3-15. Schottky HEMT process flow with digital etching

(a) Ohmic contact formation

(b) Mesa isolation

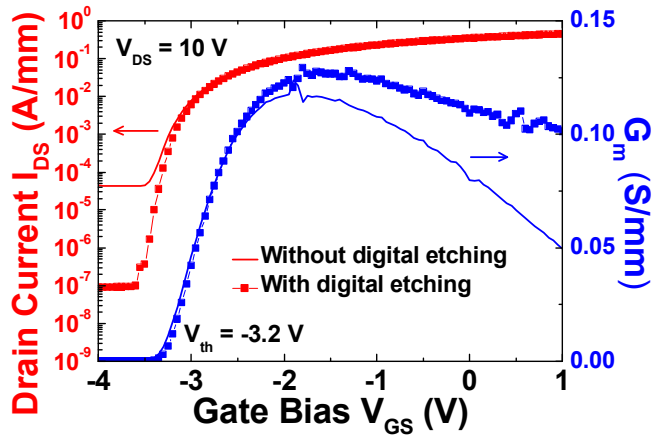
(c) Digital etching on whole GaN surface

(d) Schottky metallization

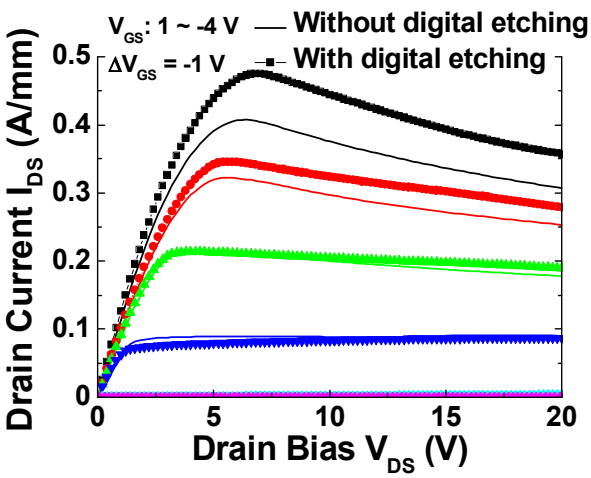
(e) SiN_x passivation

Figure 3-16 shows the output DC characteristics of GaN HEMTs with and without digital etching. The transfer curve of the device at the V_{DS} of 10 V is shown in Fig. 3-16 (a). Threshold voltages of both devices were -3.2 V. With digital etching, the drain current at pinch-off state (V_{GS} = -7 V) was decreased by more than two orders of magnitude. The extracted subthreshold slopes were 152 mV/dec and 70 mV/dec for the HEMTs without and with digital etching, respectively. The measured ON/OFF drain current ratios were 8.9×10^3 and 4.9×10^6 for the HEMTs without and with digital etching, respectively. Maximum drain current of the HEMT with digital etching was 475 mA/mm, which was increased by 16 % compared with the HEMT without digital etching, as shown in Fig. 3-16 (b). The specific on-resistance was slightly decreased from 1.21 to 1.15 $m\Omega \cdot cm^2$ in the HEMT with digital etching. Figure 3-16 (c) shows the gate reverse current. Gate reverse current was decreased by about two orders of magnitude in the HEMT with digital etching. These results reveals that current conduction path through the surface traps was blocked by digital etching on GaN surface.

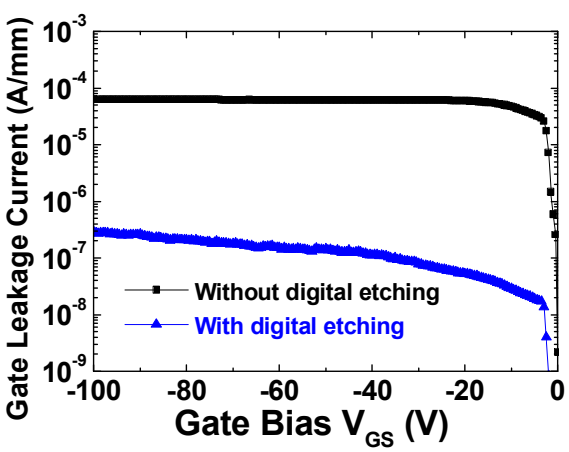
Figure 3-17 (a) shows the off-state breakdown voltage characteristics. Breakdown voltages were 725 V and 1025 V for the HEMTs without and with digital etching, respectively. Figure of merits (V_{BR}^2/R_{ON}) of the HEMTs without and with digital etching were 0.43 GW/cm^2 and 0.91 GW/cm^2, respectively. Figure 3-17 (b) shows the breakdown voltage versus specific on-resistance graph. Output DC characteristics of Schottky HEMTs with and without digital etching is summarized in Table 3-4.



(a)

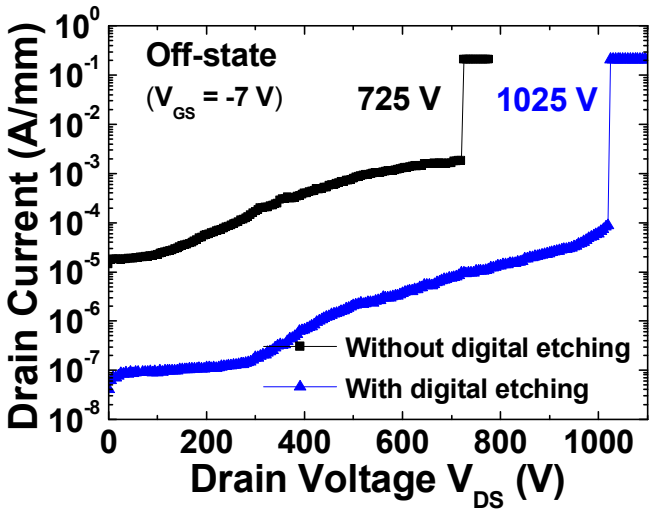


(b)

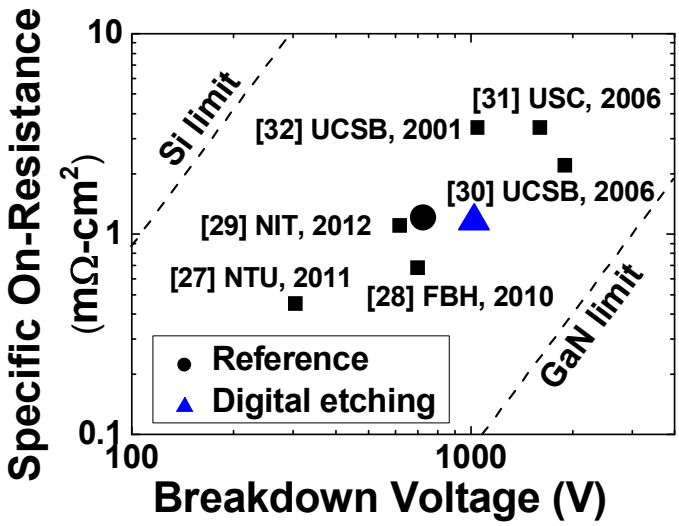


(c)

Fig. 3-16. Output DC characteristics of fabricated Schottky HEMTs with and without digital etching (a) Transfer curve (b) Family curve (c) Gate leakage current



(a)



(b)

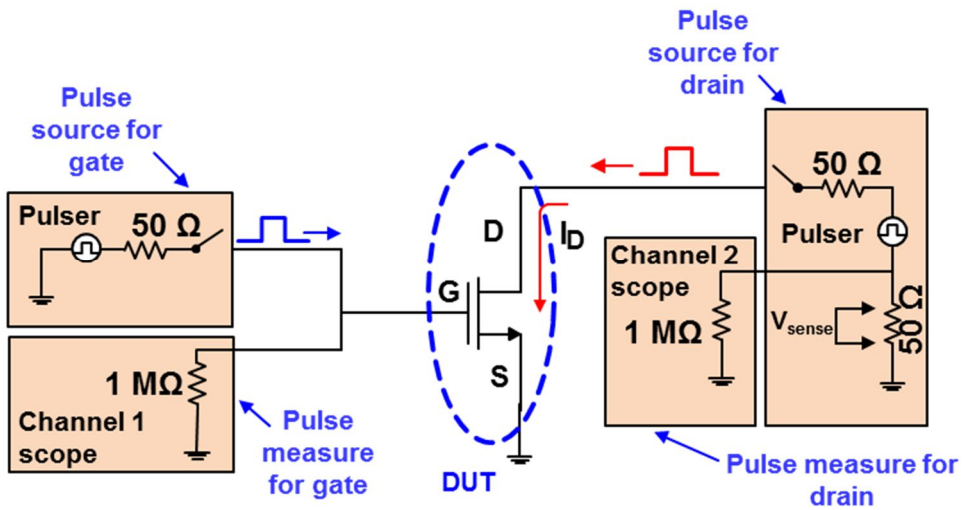
Fig. 3-17. Off-state breakdown characteristics (a) Breakdown characteristics

(b) Specific on-resistance vs. breakdown voltage graph of fabricated HEMTs

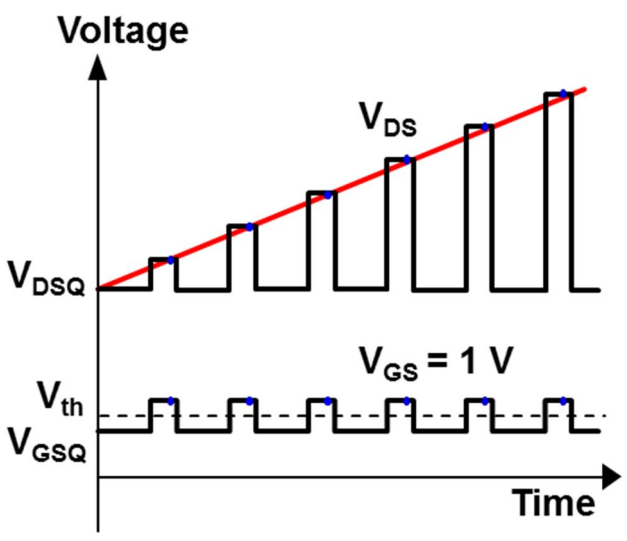
Table 3-4. Output DC characteristics of Schottky HEMTs with and without digital etching summary

	Without digital etching	With digital etching
Threshold voltage	-3.2 V	-3.2 V
On/Off ratio	8.9×10^3	4.9×10^6
Subthreshold slope	152 mV/dec	70 mV/dec
Maximum drain current	409 mA/mm	475 mA/mm
Gate leakage current at -100 V	6.3×10^{-5} A/mm	2.9×10^{-7} A/mm
Off-state breakdown voltage	725 V	1025 V

Pulsed I-V characteristics were measured to examine the effect of digital etching on charge trapping in the HEMTs. Figure 3-18 (a) shows the schematic of on-wafer pulsed I-V measurement system. Figure 3-18 (b) shows the pulse signal applied to the drain and gate of device under test. Pulsed I-V characteristics of fabricated GaN HEMTs with and without digital etching were measured as shown in Fig. 3-19. DC gate bias (V_{GS}) was fixed at 1 V, and drain bias (V_{DS}) was swept from 0 V to 40 V. The quiescent gate bias (V_{GSQ}) was fixed at -4 V to deplete the channel and the different quiescent drain bias (V_{DSQ}) of 0, 10, 20, 30, and 40 V was applied to emphasize the charge trapping effect. Serious current collapse was observed in the HEMT without digital etching. However, there was a negligible current collapse in the HEMT with digital etching, which might be due to the improved GaN surface with digital etching. It could be thought that GaN surface was improved after digital etching process.



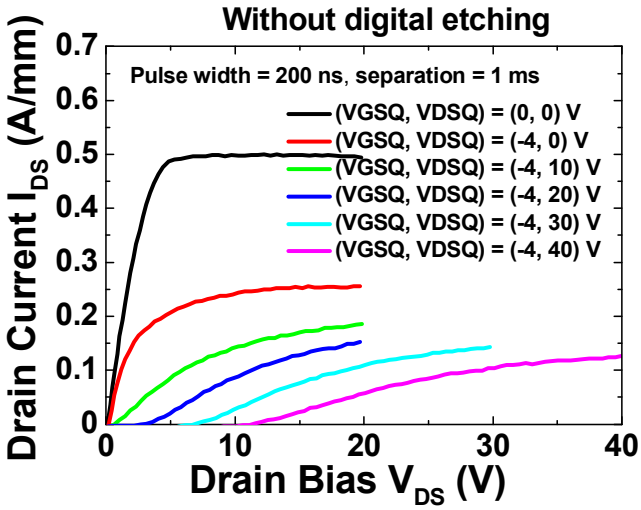
(a)



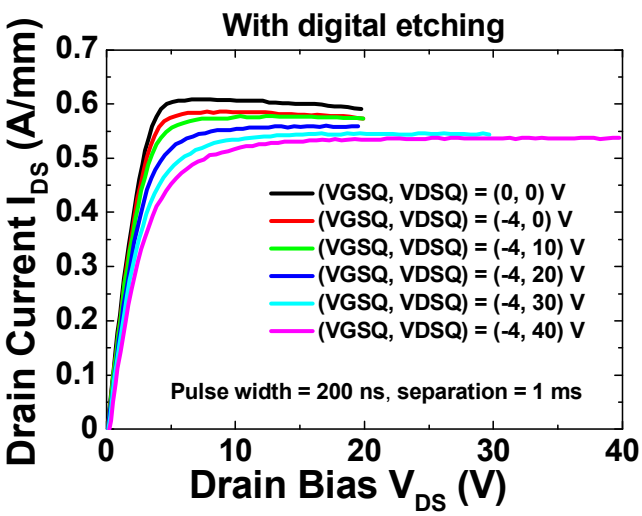
(b)

Fig. 3-18. (a) Schematic of on-wafer pulsed I-V measurement system

(b) Drain and gate pulse signal



(a)



(b)

Fig. 3-19. Pulsed I-V characteristics of fabricated Schottky HEMTs

(a) Without digital etching (b) With digital etching

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Chapter 4. Recessed AlGaN/GaN SBD

4.1 Introduction

Structural analysis and optimization of recessed GaN SBD will be discussed. Because current of lateral SBDs are flowing through the 2DEG channel, electrical characteristics of SBDs are depends on 2DEG channel-to-Schottky metal distance. Thus, study on recessed SBDs with different recess depths is necessary to understand the operation mechanism of recessed SBDs. Field plate structure is a key element in GaN power device. Peak electric field is usually concentrated on edge of anode. Optimization of field plate structure to distribute the electric field effectively is needed to increase the breakdown voltage.

In following sections, analysis of recessed SBD with respect to different recess depths and optimization of double field plate structure will be reported. Fabrication and electrical measurement including current-voltage (I-V), capacitance-voltage (C-V), breakdown voltage, and switching characteristics are discussed.

4.2 Influence of anode recess depth of AlGaN/GaN SBD

4.2.1 Device fabrication

The epi-layer structure consisted of a 4-nm GaN capping layer, a 20-nm $Al_{0.23}Ga_{0.77}N$ barrier, a 300-nm undoped GaN layer, and 3.9-μm carbon-doped GaN buffer layer on a Si substrate as depicted in Fig. 3-14 was used.

A schematic process flow of the GaN SBDs with different recess depths is shown in Fig. 4-1. The inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3/Cl_2 gas (=2/18 sccm) mixture was used to define mesa isolation structure. The mesa etching was performed with a source power of 200 W, a bias power of 15 W, and a chamber pressure of 5 mTorr. DC self-bias of mesa etching condition was 55 V. Organic residues on samples were cleaned with boiled solvent and sulfuric-peroxide mixture (SPM) solution. Surface native oxides were removed by dipping in diluted HF (1:10) for 10 min. Next, 10-nm-thick SiN_x layer was prepassivated on the GaN surface using inductively coupled plasma chemical vapor deposition (ICP-CVD) at 350 °C for surface protection during high temperature ohmic annealing [1]. Ohmic contact metals of Si/Ti/Al/Mo/Au (5/20/80/35/50 nm) were deposited by e-beam evaporation and annealed at 800 °C for 1 min in N_2 ambient. The measured contact resistance and sheet resistance were 0.4 Ω-mm and 480 Ω/sq, respectively. The mobility and the carrier concentration of the 2-DEG formed at the AlGaN/GaN heterointerface were 2120 cm^2/V-s and 7 × 10^{12}/cm^2, respectively, estimated by the Hall measurement. Prepassivated SiN_x layer was etched away with 7:1 buffered oxide etchant (BOE). Next, anode region was recess-etched with

different depths, i.e., 14, 29, 34 nm. Anode recess was carried out using BCl_3/Cl_2 (=2/18 sccm) gas mixture with a source power of 250 W, a bias power of 5 W, and a chamber pressure of 7 mTorr. DC self-bias and etch rate of recess condition was 20 V and 0.15 nm/s, respectively. Additional wet digital etching was performed on the recessed area to alleviate the dry etching damage as explained in chapter 3. The oxidation using N_2O plasma was carried out with a low power of 20 W under a gas flow rate of 40 sccm, a chamber pressure of 200 mTorr, and a time of 180 sec for 1 cycle. The formed oxide removal was carried out by dipping the samples in diluted HCl (1:1) solution for 60 sec. A Ni/Au (=40/160 nm) metal was deposited to form a recessed Schottky contact. 200-nm-thick SiN_x film was deposited at 300 °C for surface passivation. The condition of SiN_x deposition was SiH_4/NH_3 (=8/40 sccm) gas mixture with a RF power of 300 W, a chamber pressure of 20 mTorr, and a chuck temperature of 300 °C. Prior to surface passivation, the in-situ N_2 plasma was executed. Additional Ni/Au was deposited as a field plate with 2 μm length after opening through holes in the SiN_x layer.

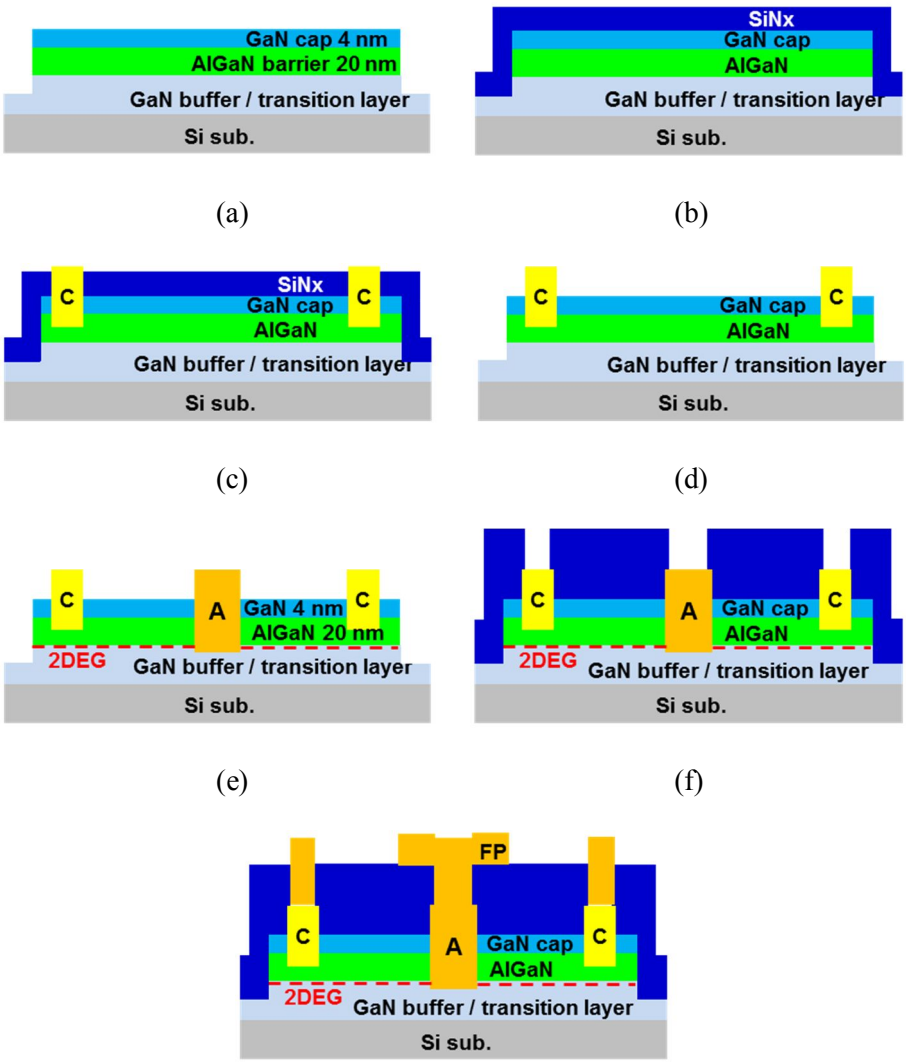


Fig. 4-1. Recessed GaN SBD process flow with prepassivation process

(a) Mesa isolation (b) SiN_x prepassivation

(c) Ohmic contact formation (d) Prepassivated SiN_x layer removal

(e) Recessed anode formation (f) SiN_x passivation

(g) Field plate and pad deposition

4.2.2 I-V characteristics

With the recess depths of 29 nm and 34 nm, Schottky anodes are formed beneath the 2DEG channel, because total thickness of GaN capping layer and AlGaN barrier layer are 24 nm. Figure 4-2 shows the transmission electron microscopy (TEM) image of fully recessed anode. It is clearly observed that the recessed Schottky contact was formed from the TEM image. Slanted anode structure was formed because of low power etching of epi-layer.

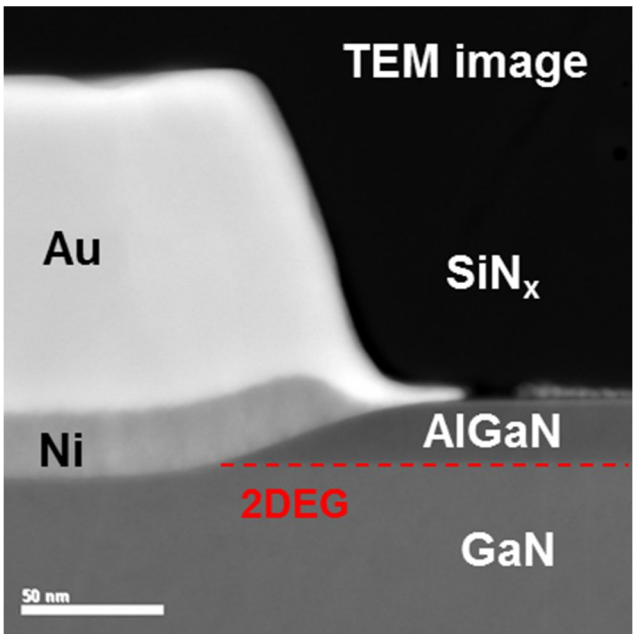


Fig. 4-2. TEM image of fully recessed Schottky contact

(2DEG Channel depth = 24 nm, recess depth = 29 nm)

Figure 4-3 (a) shows the typical forward I-V characteristics of the GaN SBDs with respect to recess depths. The anode-to-cathode distance (L_{AC}) was 10 μm. On resistance of recessed SBDs are almost identical with a non-recessed SBD, which means that recess etching damage is insignificant. Two-step etching composed of dry recess etching and wet digital etching described in chapter 3 contributes to low on-resistance of recessed SBDs. Non-recessed SBD shows the forward turn-on voltage of 1.3 V. The forward turn-on voltage of recessed SBD fabricated with 14 nm recess depth is decreased as 0.9 V because of effective Schottky barrier height (SBH). Lowest forward turn-on voltage of 0.6 V was obtained with fully-recessed SBDs fabricated with 29 and 34 nm recess depths. It means that lowered and uniform forward turn-on voltage can be obtained with the fully recessed Schottky contacts. The forward current of fully recessed SBD is 127 mA/mm at forward bias of 1.5 V which is comparable with a rectifier with gated ohmic anode and a recessed SBD reported by FBH berlin [2]-[5]. Low turn-on voltage and on-resistance of fully recessed SBDs are advantageous to reduce the switching loss of power switching systems. The ideality factor and SBH calculated from the thermionic theory [6] are shown in Table 4-1. From the thermionic emission, diode current can Schottky barrier height can be expressed as below.

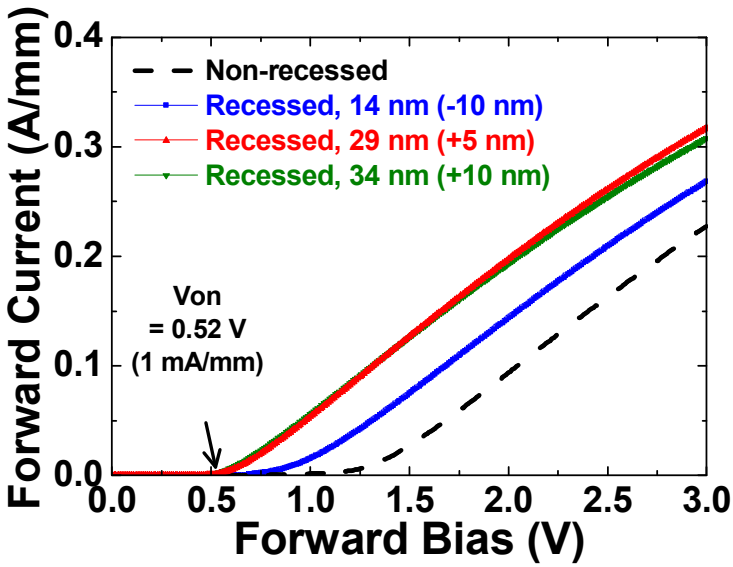
$$I = I_S \exp\left(\frac{qV}{nk_BT}\right) \tag{4.1}$$

$$\Phi_B = \left(\frac{k_BT}{q}\right) \mathrm{In}\left(\frac{AA^*T^2}{I_S}\right) \tag{4.2}$$

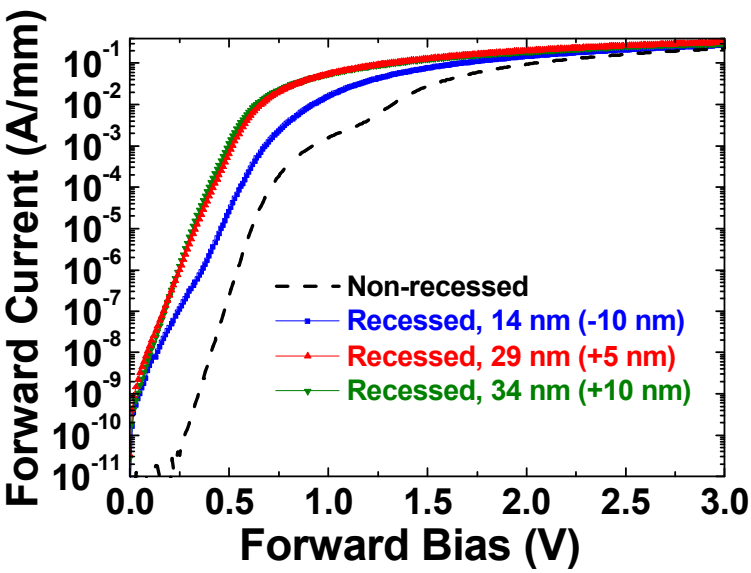
where I_S is the saturation current density, n is the ideality factor, K_B is the Boltzmann constant, T is the absolute temperature, Φ_B is the Schottky barrier

height, A is the contact area, and A* is the effective Richardson constant. Fully recessed SBDs show better quality of Schottky contacts in terms of ideality and SBH.

The reverse characteristics are shown in Fig. 4-4. The measurement limit was 1100 V. The reverse current of fully recessed SBDs are around 2 μA/mm at -1100 V. The reverse current of recessed SBD fabricated with 14 nm recess depth is increased as 12 μA/mm which is correlated with a poor ideality factor. Figure 4-5 shows the on-resistance versus breakdown voltage graph.



(a)



(b)

Fig. 4-3. Forward I-V characteristics of SBD with prepassivation process

(a) Linear (b) Log scale

Table 4-1. Ideality factor and Schottky barrier height of fabricated SBDs

Channel depth 24 nm	Non-recessed	Recessed (14 nm)	Recessed (29 nm)	Recessed (34 nm)
Ideality factor	1.22	1.60	1.17	1.23
Schottky barrier height (eV)	1.03	0.78	0.76	0.75

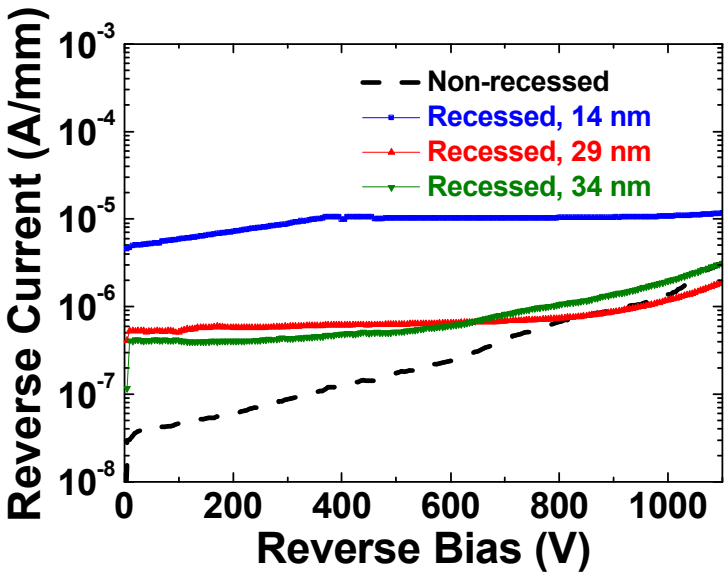


Fig. 4-4. Reverse I-V characteristics of fabricated GaN SBDs

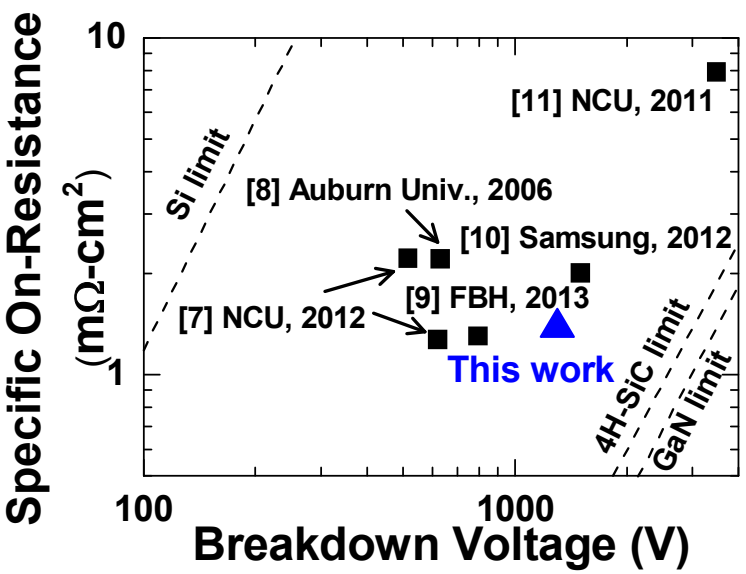
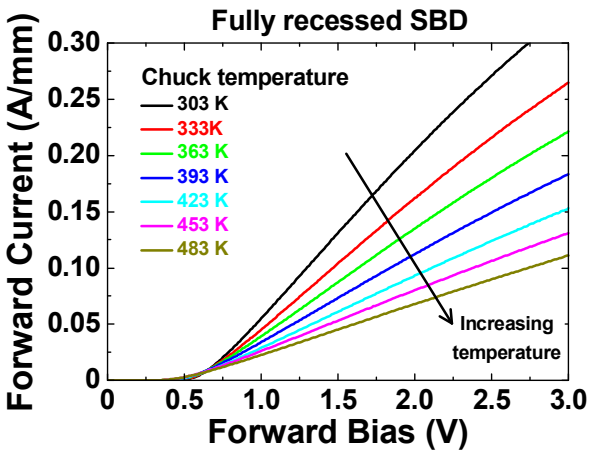
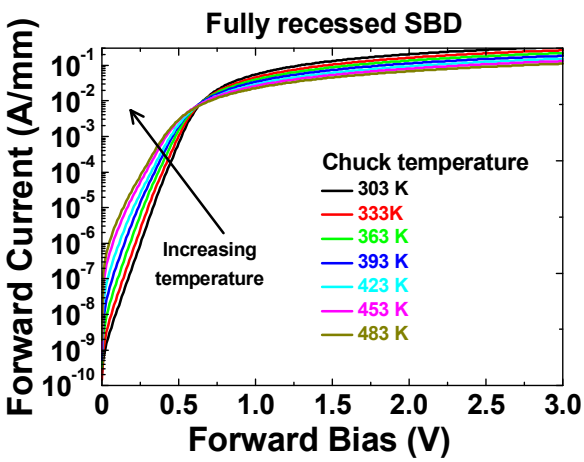


Fig. 4-5. R_{on} vs. breakdown voltage graph of fabricated fully recessed SBD

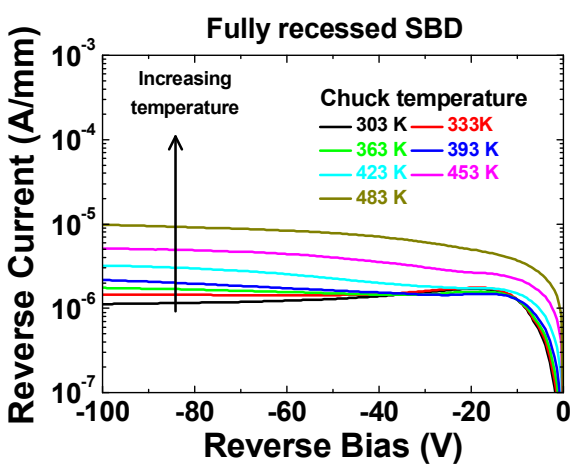
Measured I-V characteristics of fully recessed SBD at elevated chuck temperatures from 303 K to 483 K with 30 K steps are shown in Fig. 4-6. Specimen was heated on the hot chuck over 10 minutes at every different temperatures. As chuck temperature increases, series resistance of SBD increases, Schottky barrier height decreases, and reverse current decreases. Figure 4-7 shows the on-resistance and reverse current -100 V as a function of chuck temperature for the non-recessed SBD and recessed SBD. It is observed that on resistance of both SBDs were increased by a factor of 3 after increase of chuck temperature from 303 K to 483 K due to the increase of channel resistance. Reverse current was exponentially increased with increasing chuck temperature. The activation energy (E_A) which is the slope of the Fig. 4-7 (b) was calculated from the Arrhenius equation ($e^{-E_A/RT}$) [12]. From the linear fitting of ln (J) versus 1/temperature, the activation energy of the recessed SBD is estimated as 0.14 eV. Schottky barrier height of recessed SBD extracted from I-V curve was 0.76 eV as shown in Table 4-1. It can be deduced that traps are located at 0.62 eV below the conduction band (E_C - 0.62 eV) from the experimental data. The trap at the level of 'E_C - 0.613 eV' had been reported in n-type GaN which is related with the nitrogen vacancies [13]. On the other hand, activation energy of non-recessed SBD above 363 K is estimated as 0.72 eV. Schottky barrier height of recessed SBD extracted from I-V curve was 1.03 eV as shown in Table 1. It can be deduced that traps are located at 0.31 eV below the conduction band (E_C - 0.31 eV) from the experimental data. The trap at the level of 'E_C - 0.3 eV' had been reported in GaN surface [14], [15]. Figure 4-8 shows the energy band diagram with Frenkle-Poole emission. Electrons with activation energy can pass through the traps from Schottky metal to 2DEG channel.



(a)



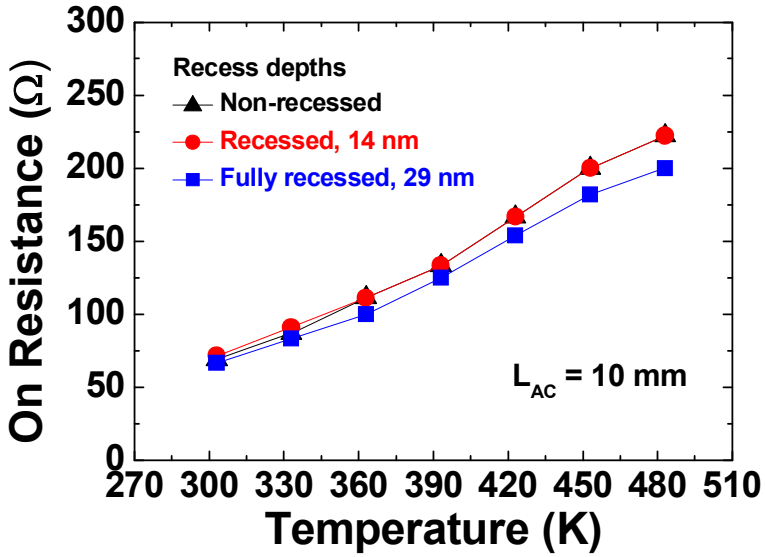
(b)



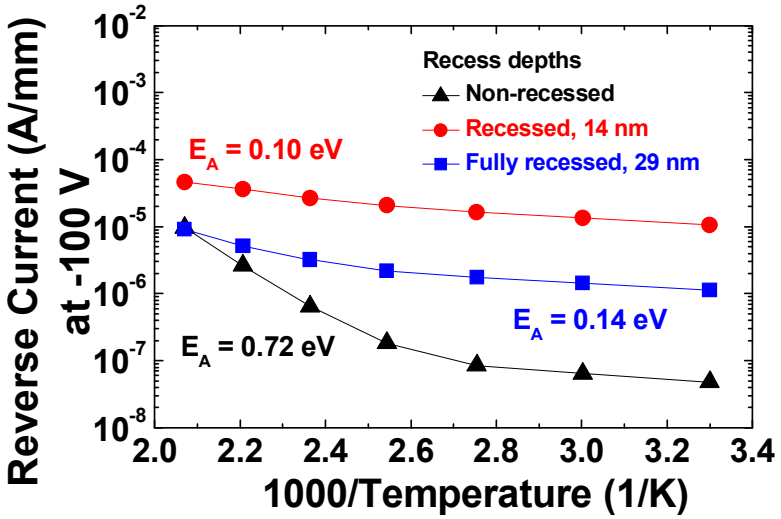
(c)

Fig. 4-6. I-V-T characteristics of fully recessed SBD

(a) Forward linear scale (b) Forward log scale (c) Reverse



(a)



(b)

Fig. 4-7. I-V-T characteristics summary (30 °C ~ 210 °C)

(a) On-resistance (b) reverse current at -100 V

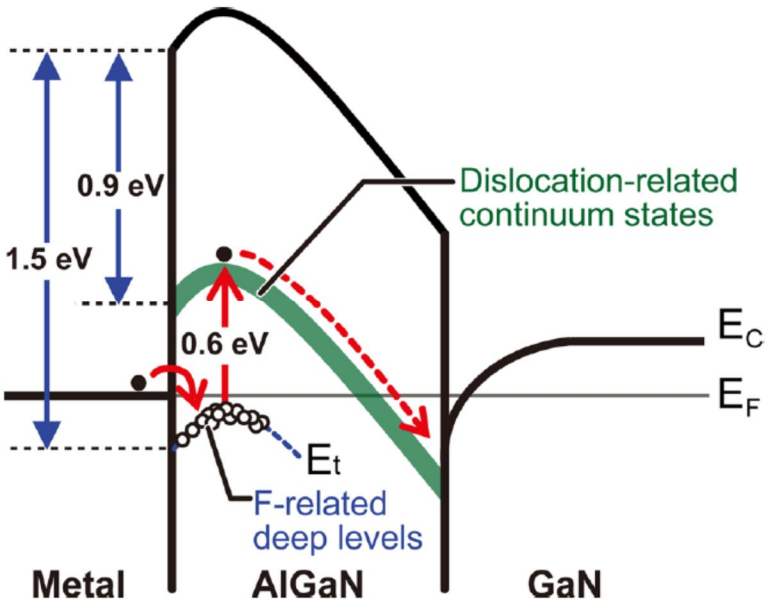


Fig. 4-8. A schematic energy band diagram showing the proposed Frenkel-Poole emission mechanism in the SBDs with CF_4 plasma treatment (E_A = 0.6 eV) [12]

4.2.3 C-V characteristics

The C-V curves of fabricated GaN SBDs are shown in Fig. 4-9. Measured frequency and AC voltage were 1 MHz and 30 mV, respectively. The capacitances measured at 0 V are 28 pF for non-recessed SBD and 0.4 pF for fully-recessed SBD, respectively. Small capacitance of fully recessed SBD is due to the direct contact between 2DEG and Schottky metal. The capacitance of recessed SBD fabricated with 14 nm recess depth is 62 pF at 0 V which is larger than capacitance of non-recessed SBD. This is because spacing between Schottky metal and 2DEG was decreased by recess etching. Small capacitance in fully recessed SBD enables fast switching, because switching time is proportional to maximum capacitance and pinch-off voltage [16].

$$\tau_{switching} = C_{max} \times V_{pinch\text{-}off} / I_{on} \quad (4.3)$$

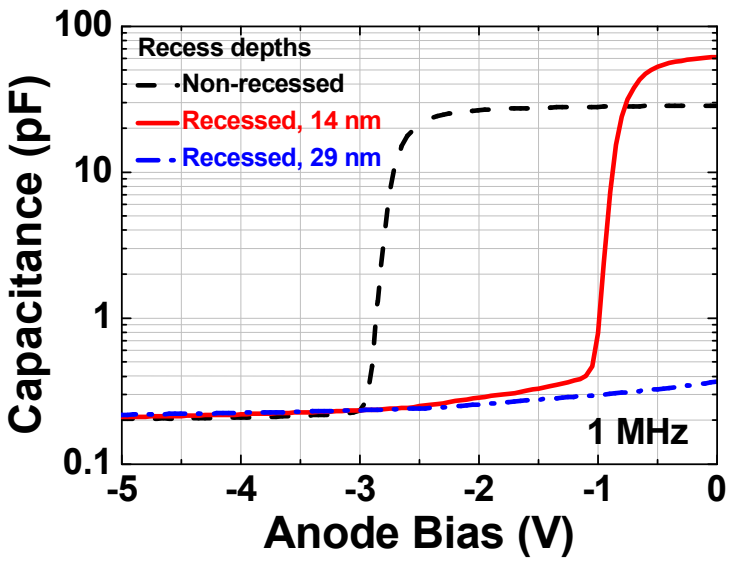


Fig. 4-9. C-V curve of SBD with prepassivation process

4.2.4 Reliability test

Fluorinert has a high dielectric strength of 18 MV/m as compared with 3 MV/m for the air [17], [18]. Thus, breakdown voltage of GaN HEMT can be underestimated in an air ambient as shown in Fig. 4-10.

To check the reliability, high reverse bias was applied to the fully recessed SBDs. Figure 4-11 (a) shows the variation of reverse current during 600 V reverse bias stress condition in a Fluorinert ambient. Figure 4-11 (b) shows the variation of reverse current during 200 V reverse stress condition on 200 °C hot chuck in air ambient. Because boiling point of Fluorinert (FC-40) is 165 °C [19], Fluorinert was not used on hot chuck. Fig. 11 (b). Failure of SBD was not observed in both test conditions.

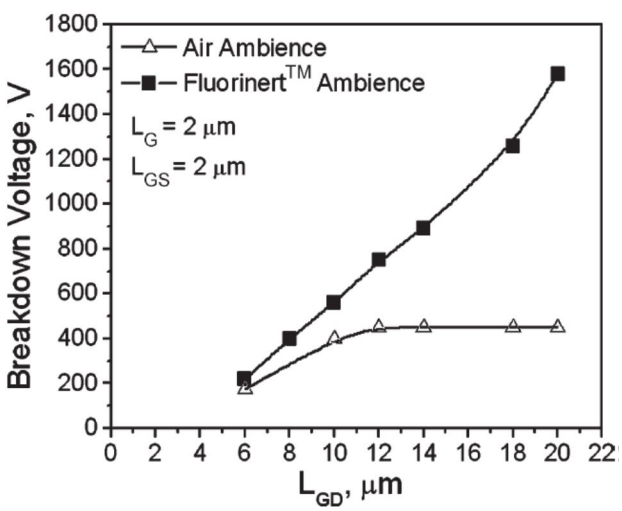
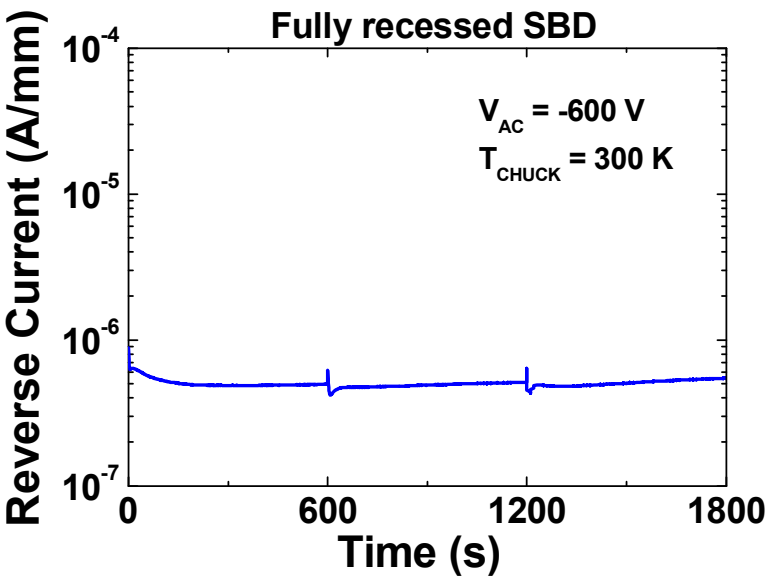
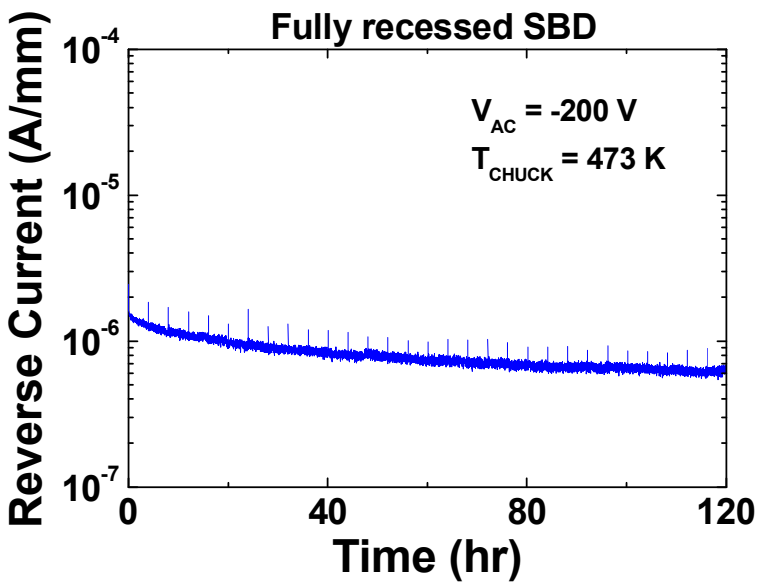


Fig. 4-10. L_{GD}−V_{BR} dependence of the GaN HEMT devices measured in air and Fluorinert ambience [17]



(a)



(b)

Fig. 4-11. Reverse current of fully recessed SBD under stress

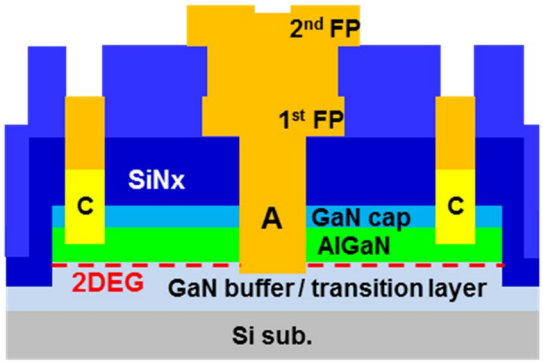
(a) High reverse bias stress (b) High temperature and reverse bias stress

4.3 SBD with double field plate

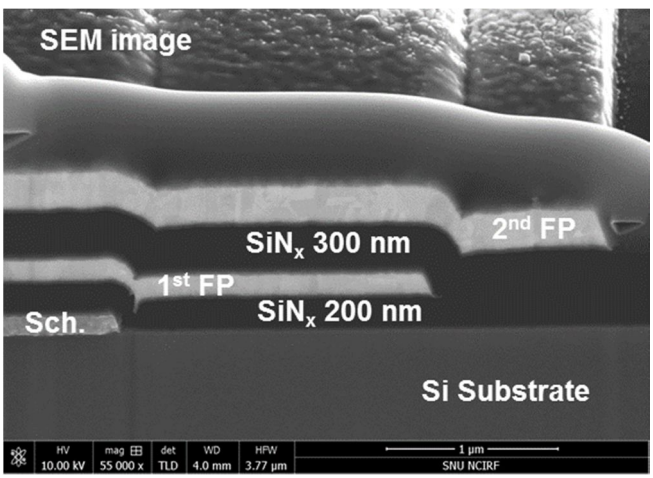
4.3.1 Fabrication and simulation

SBD with single field plate was fabricated with identical process as explained in chapter 4.2.1. Samples were cleaned with a solvent and BOE to remove the unwanted contamination and oxide layer which would be generated during mid-term measurement. Next, 300-nm-thick SiN_x layer was deposited with a SiH_4/NH_3 (=8/40 sccm) gas mixture, a 300 W RF power, and a 20 mTorr chamber pressure at the 250 °C chuck temperature. Finally, via-hole etching and 2nd field plate metallization were followed. Figure 4-12 (a) shows the schematic cross-sectional view of AlGaN/GaN SBD with double field plate. The length of 1st field plate and 2nd field plate were 2 and 3 μm from anode edge, respectively. It is clearly observable that the formation of the double field plate structure from the scanning electron microscope (SEM) image as shown in Fig. 4-12 (b).

Electric field distribution at 2DEG channel layer was simulated using Atlas Silvaco software. Figure 4-13 (a) and (b) shows the field distribution at the reverse bias of 600 V and 1200 V, respectively. The workfunction of Schottky metal was assumed as 5.1 eV. The anode-to-cathode distance was assumed as 10 μm. Electric field was concentrated at the anode edge and field plate edge. In both case of reverse bias conditions, the peak electric field was reduced with a double field plate structure. Considering the critical field of GaN, double field plate structure would be favorable than single field plate structure in the breakdown characteristics.



(a)

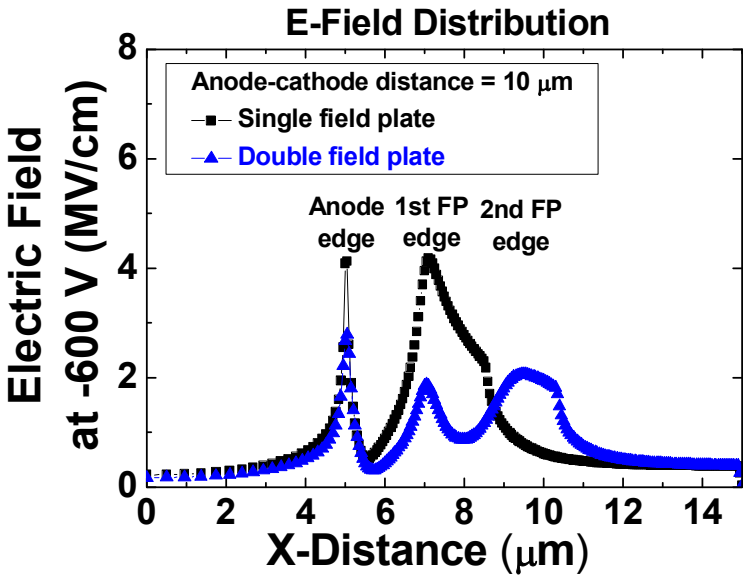


(b)

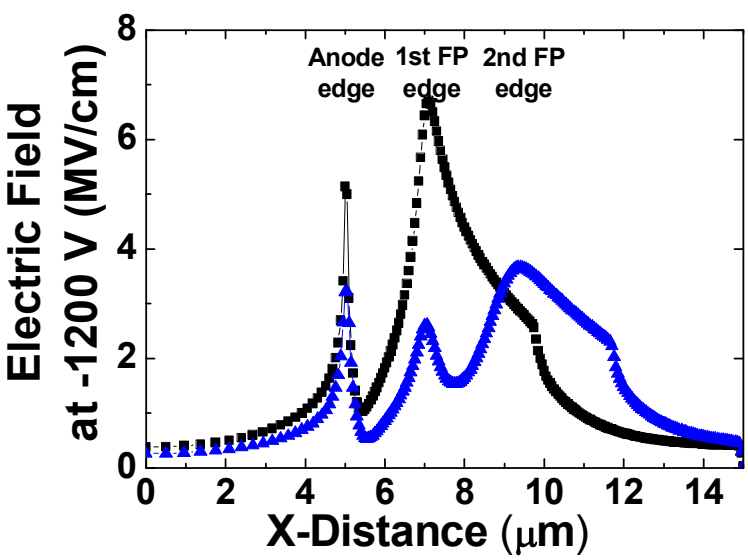
Fig. 4-12. Double field plate structure

(a) Schematic cross-sectional view of AlGaN/GaN SBD with double field plate

(b) SEM image of double field plate structure



(a)



(b)

Fig. 4-13. Simulation results of electric field at 2DEG channel

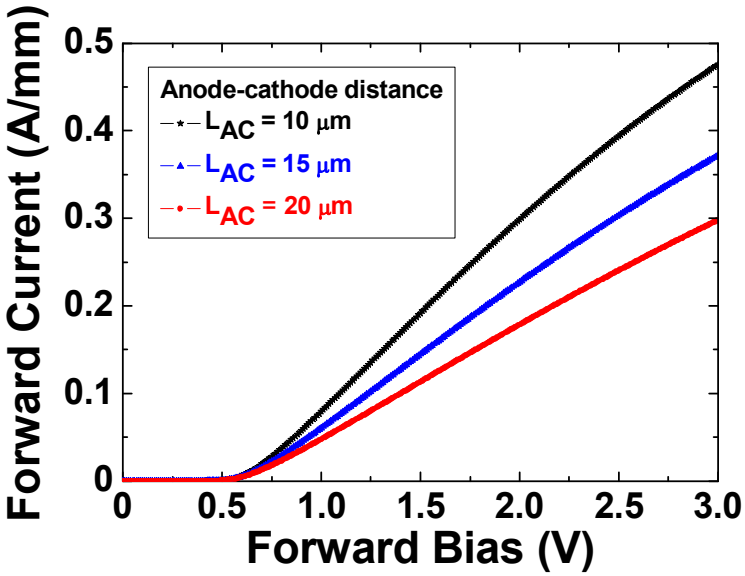
(a) Reverse bias of 600 V

(b) Reverse bias of 1200 V

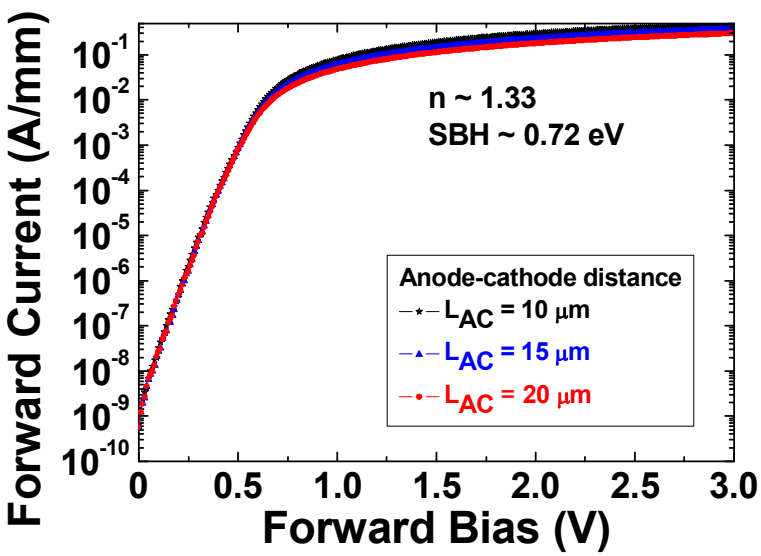
4.3.2 Measurement results

Figure 4-14 shows the forward current of AlGaN/GaN SBDs with double field plate. Low turn-on voltage of 0.51 V was obtained. On-resistance of the SBDs were increased with increasing anode-to-cathode distance from 10 μm to 20 μm due to the channel resistance. Since the forward current for $V < V_{on}$ is dominated by the Schottky junction, identical ideality factor and Schottky barrier height of 1.33 and 0.72 eV were calculated.

Figure 4-15 shows the breakdown characteristics of fabricated AlGaN/GaN SBDs. Both diodes with the single and the double field plates show the reverse current level of 10^{-7} A/mm. Breakdown voltage was increased about 15 % with the double field plate structure compared with the single field plate structure. University of Notre Dame announced the 5 ~ 25 % breakdown voltage improvement with the double field plate structure [16].



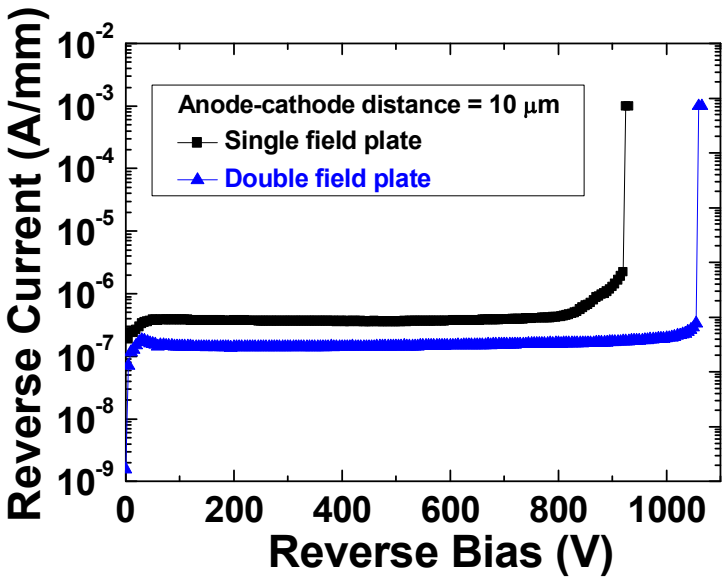
(a)



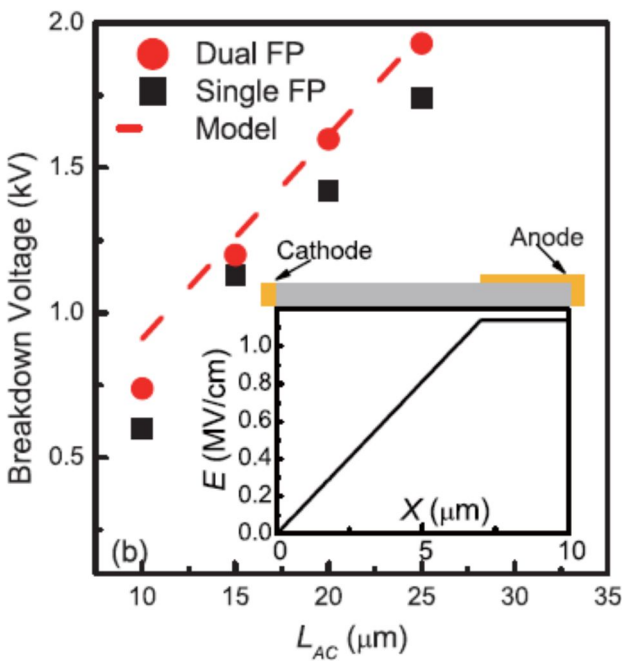
(b)

Fig. 4-14. Forward current of SBD with double field plate

(a) Linear (b) Log scale



(a)



(b)

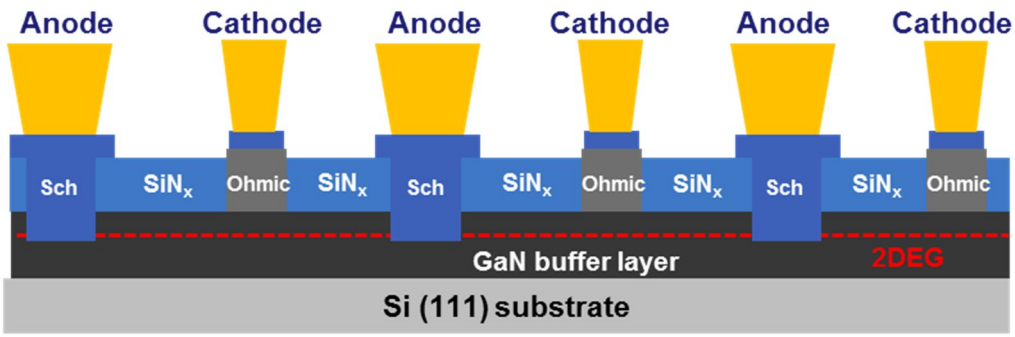
Fig. 4-15. Breakdown characteristics of GaN SBD with double field plate

(a) Measured data (b) [16]

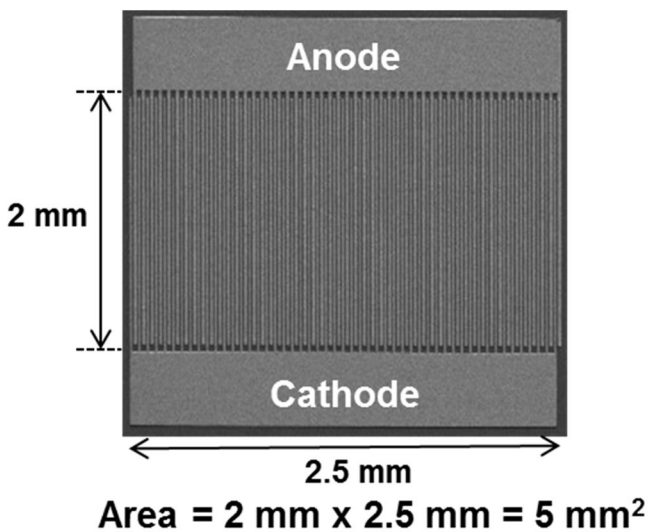
4.4 Large area GaN SBD with fully recessed anode

The multi-finger lateral-type GaN SBDs with fully recessed anodes were fabricated. Anode and cathode electrodes were electroplated with 10 μm height to decrease series resistance of large area SBDs. Schematic cross-sectional view and SEM iamge are shown in Fig. 4-16. Large area SBDs were fabricated with 100 mm width and 15 μm anode-to-cathode distance. Length of the anodes and cathodes were both 10 μm. Active area of large area SBDs was 5 mm^2. The forward current at 1.5 V is 7.1 A as depicted in Fig. 4-17 (a). The reverse breakdown voltage at leakage current of 100 μA is 1080 V as depicted in Fig. 4-17 (b). Specific on-resistance is 6.1 $m\Omega\text{-}cm^2$. Fully recessed anode and electroplated electrodes contribute to reduce the specific on-resistance. The figure of merit V_{BR}^2/R_{on} of fabricated large area SBD is 192 MW/cm^2 which is one of the highest value of the lateral-type large area GaN SBDs ever reported. Table 4-2 shows I-V characteristics of other group's results for comparison.

Figure 4-18 (a) shows a C-V curve of the fabricated large area GaN SBD. The capacitance measured at reverse bias of 20 V is 31 pF which is smaller than recently published data by FBH berlin [5]. These capacitances of SBDs are related with a switching property and small capacitance enables fast switching times as also explained in unit device.



(a)

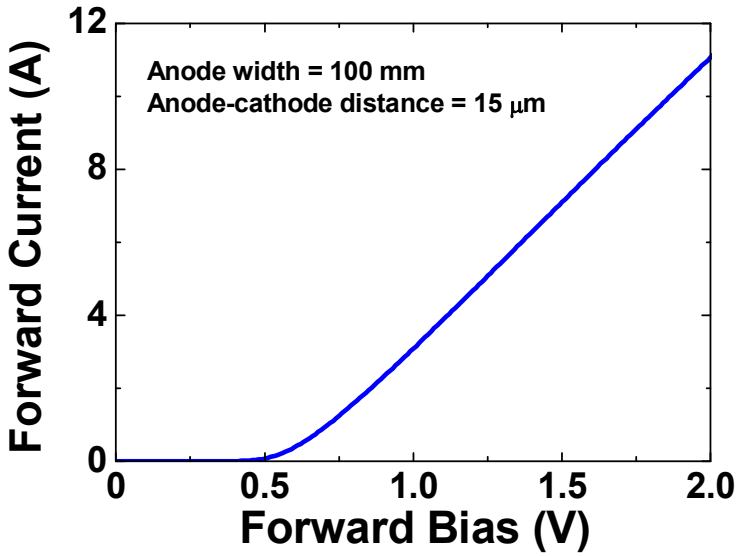


(b)

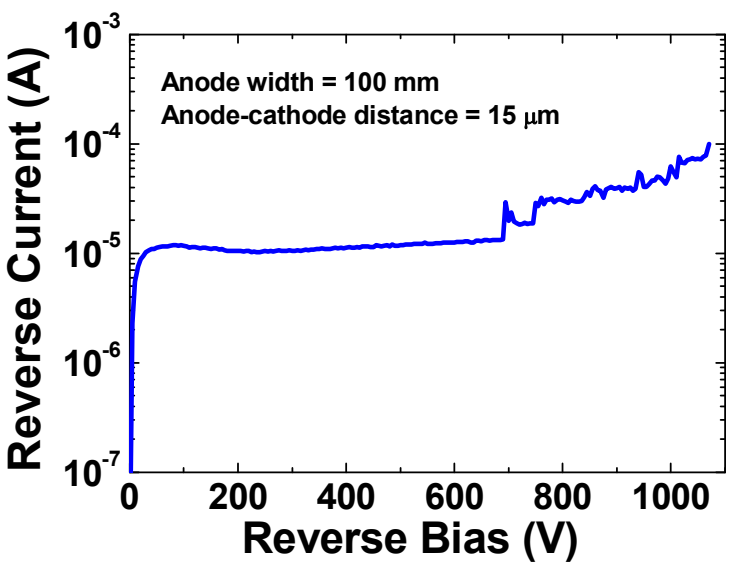
Fig. 4-16. Large area SBD with fully recessed anode structure

(a) Cross-sectional schematic view

(b) Scanning electron microscope (SEM) image



(a)



(b)

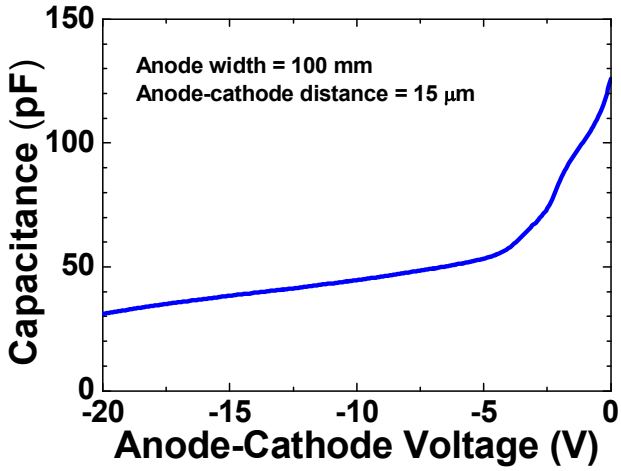
Fig. 4-17. I-V characteristics of large area GaN SBD with fully recessed anode

(a) Forward I-V characteristic

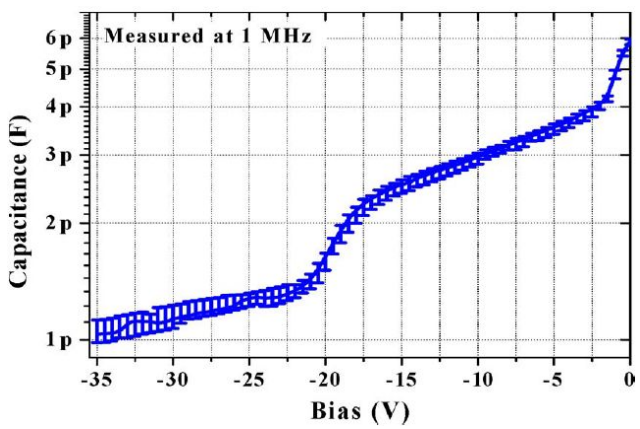
(b) Reverse breakdown characteristic

Table 4-2. Comparison of I-V performance

	Cree (C3D04065A)	ROHM (SCS210KE2)	Samsung [20]	Micro GaN (MGG-1T0617D-CA)	This work
Material	SiC	SiC	GaN	GaN	GaN
Size (mm^2)	-	-	9	-	5
I_F (A) at 1.5 V	4.5	5	4.5	5.4	7.0
I_R (μA) at -600 V	0.4	0.008	6	500	12.5



(a)



(b)

Fig. 4-18. C-V curve of large area GaN SBD with fully recessed anode

(a) This work (b) FBH berlin [5]

Fabricated large area GaN SBDs have been packaged using TO-220 packages to measure the switching property. GaN SBD dies were attatched to TO-220 package as shown in Fig. 4-19 with AuSn paste. Figure 4-20 shows a reverse recovery waveform of the GaN SBD. The GaN SBD was switched from the forward current (I_F) of 5.4 A to the reverse bias of 415 V with di/dt = 215 A/μs. The measured reverse recovery time (T_{rr}) and charge (Q_{rr}) are 10 ns and 5.2 nC, respectively. Table 4-3 compares the reverse recovery times with other group's results. Fabricated GaN SBD in this work shows the lowest reverse recovery charges. It was reported that the reverse recovery characteristics of GaN SBD were worse than those of SiC diode due to the relatively large size of a lateral structure [20]. In this study, fast switching properties were achieved from the GaN SBD with a lateral structure due to the improved specific on-resistance. Switching losses are generated by the amount of integrating the product of current and voltage during T_{rr} [23]. Thus, we regard our SBDs are adequate for low loss and high frequency power switching applications.

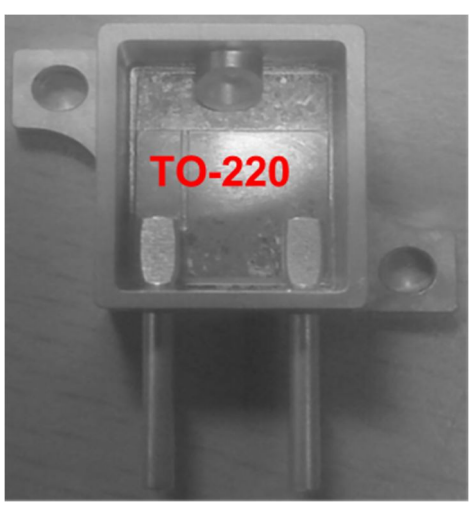
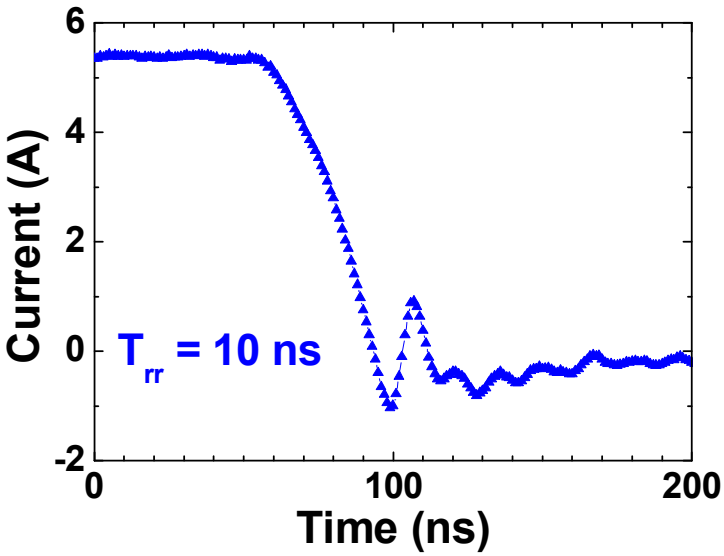
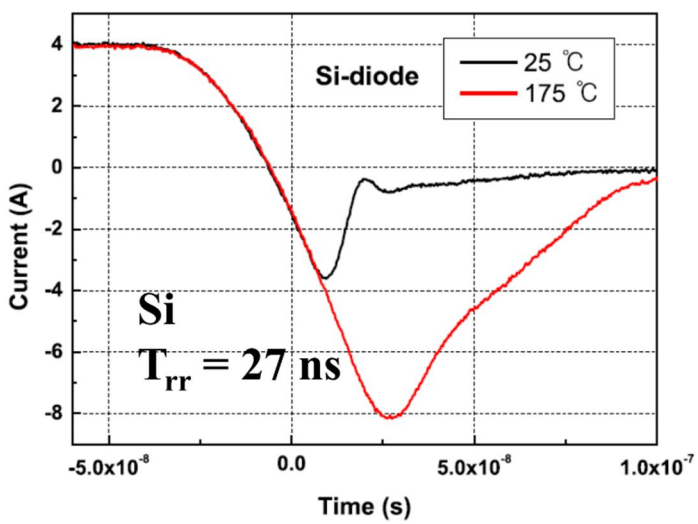


Fig. 4-19. Photograph of TO-220 package



(a)



(b)

Fig. 4-20. Reverse recovery waveform of SBD

(a) Fabricated GaN SBD (b) Si diode [20]

Table 4-3. Comparison of switching performance

Chip size (mm^2)	I_F (A)	V_{DD} (V)	di/dt (A/μs)	T_{rr} (ns)	Q_{rr} (nC)	Schemes	References
-	1.0	30	60	9	-	Lateral	[21]
-	0.0125	-	-	20	-	Vertical	[22]
1.1	5.0	380	3400	5.2	19.4	Vertical	[23]
-	2.0	300	-	11	5.57	Lateral	[24]
9.0	4.0	400	200	19.4	19.7	Lateral	[20]
5.0	5.4	415	215	10	5.2	Lateral	This work

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Chapter 5. AlGaN/GaN SBD with Anode Edge Termination

5.1 Introduction

It has been studied about digital etching and prepassivation process to improve the device performances in chapter 3 and 4, respectively. Figure 5-1 shows the off-state breakdown characteristics of the fabricated Schottky HEMTs. It is noticeable that digital etching and prepassivation process increase off-state breakdown voltage of Schottky HEMTs over 300 V compared with reference process. Off-state leakage current of Schottky HEMT was suppressed under 1 μA at 600 V by prepassivation process which protect the GaN surface during high temperature annealing to form the ohmic contact.

Pulsed I-V characteristics were measured to evaluate the current collapse phenomena as shown in Fig. 5-2. Current collapse was improved with digital etching and prepassivation process compared with reference process. However, fabricated HEMT with prepassivation process does not shows the acceptable current collapse performance even though the leakage current was decreased compared with digital etching process. It means that GaN surface would be damaged even with a SiN_x prepassivation layer. Other probable hypothesis is GaN surface would be contaminated or oxidized. Because SiN_x prepassivation layer was removed after ohmic process, GaN surface were exposed to air during subsequent process. Thus, so-called redeposition process which contains SF_6 plasma surface treatment was proposed. Moreover, GaN surface was protected during whole

process flow. Figure 5-3 shows the proposed Schottky HEMT process flow.

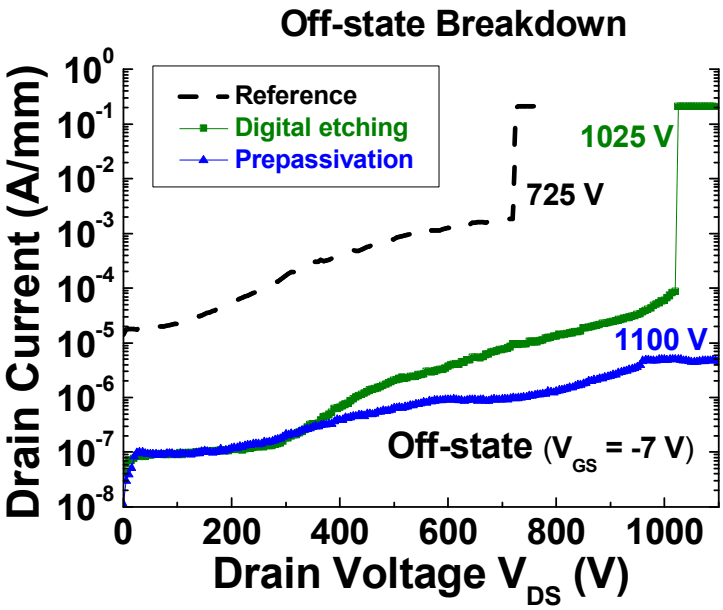
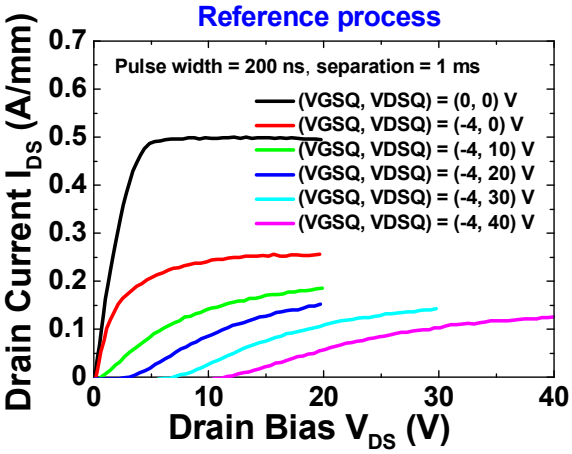


Fig. 5-1. Off-state leakage current of fabricated HEMTs

with digital etching and prepassivation process (V_{GS} = -7 V)



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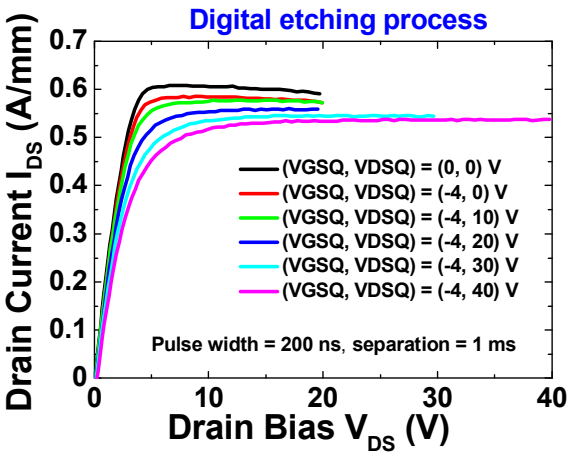

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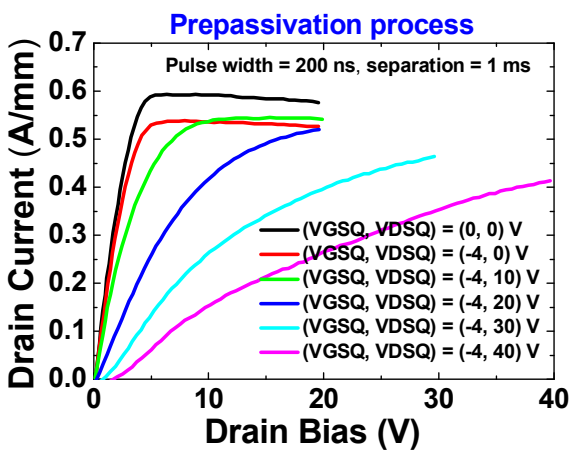


(c)

Fig. 5-2. Pulsed I-V characteristics of fabricated HEMTs

(a) Reference (b) Digital etching (c) Prepassivation process

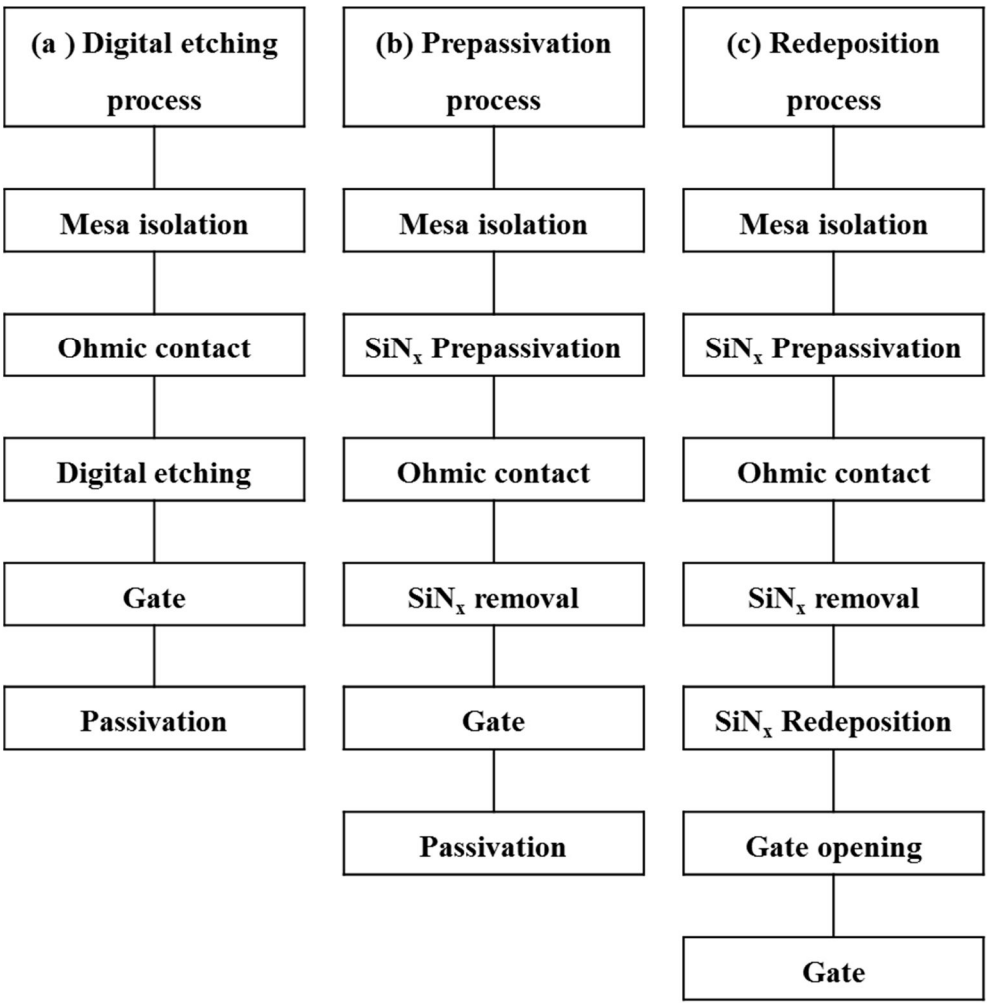


Fig. 5-3. Proposed Schottky HEMT process flow

(a) Digital etching process

(b) Prepassivation process

(c) Redeposition process

5.2 Redeposition process with SF_6 plasma treatment

5.2.1 Process description

Redeposition process was proposed to solve the current collapse issue discussed in chapter 5.1. Figure 5-3 shows the process flows containing redeposition step. The mesa etching was performed on epi-wafer. 10-nm-thick SiN_x film was passivated on epi-wafer after cleaning. Ohmic contact metals were deposited and annealed at 800 °C for 1 min in N_2 ambient. Then, SiN_x film was etched with low power SF_6 plasma. Studies on fluorine-based treatment on GaN surface was reported by several groups [1]-[6]. Because F^- ion can deplete the 2DEG channel, normally-off HEMTs and lateral field effect rectifiers can be fabricated with fluorine treatment. In the case of redeposition process, purpose of SF_6 plasma treatment is a surface treatment, not a depletion of 2DEG channel. Since SiN_x is a hard dielectric material to etch away, plasma etching processes are typically employed for the removal. GaN surface was treated with SF_6 plasma, because SiN_x layer was intentionally over-etched. 200-nm-thick SiN_x film was redeposited at 300 °C. SiN_x layer was deposited right after prepassivated film removal, GaN surface was protected during whole process flow. Gate and pad opening was performed with SF_6 plasma etching. Finally, Ni/Au Schottky metal was deposited.

5.2.2 Development of low power SF_6 plasma treatment

The influence of SF_6 plasma on GaN surface was investigated by Hall-effect measurements using Van der Pauw's method. In order to investigate the SF_6 plasma induced damage, the active area was exposed to SF_6 plasma generated in a capacitively coupled plasma (CCP) etcher. SF_6 plasma treatment conditions were a gas flow rate of 100 sccm and a chamber pressure of 0.1 Torr. The measured DC self-bias voltage and SiN_x etch rates for various RF powers are shown in Fig. 5-4. Both DC self-bias voltage and SiN_x etch rate were decreased with decreasing the RF power. A DC self-bias voltage of 1 V and a SiN_x etch rate of 7.3 nm/min were obtained at a RF power of 10 W.

The 2DEG concentration as functions of RF power and duration is shown in Fig. 5-5 (a). Regardless of the RF power level, increase in the 2DEG concentration was observed after short time exposure (i.e., 2 min) to SF_6 plasma. We speculate that this increase is associated with the annihilation of surface traps and/or contaminations [7]. As shown in Fig. 5-5, it was observed that the 2DEG concentration and electron mobility were deteriorated after SF_6 plasma treatment with high RF powers and long durations, such as 20 min exposure with 20, 50, and 100 W. It is due to surface ion bombardment effects with high power plasmas. However, no noticeable degradation was observed even after 20 min for the sample exposed to the SF_6 plasma with 10 W. Thus, the RF power of 10 W was decided to be the low damage SF_6 etching process.

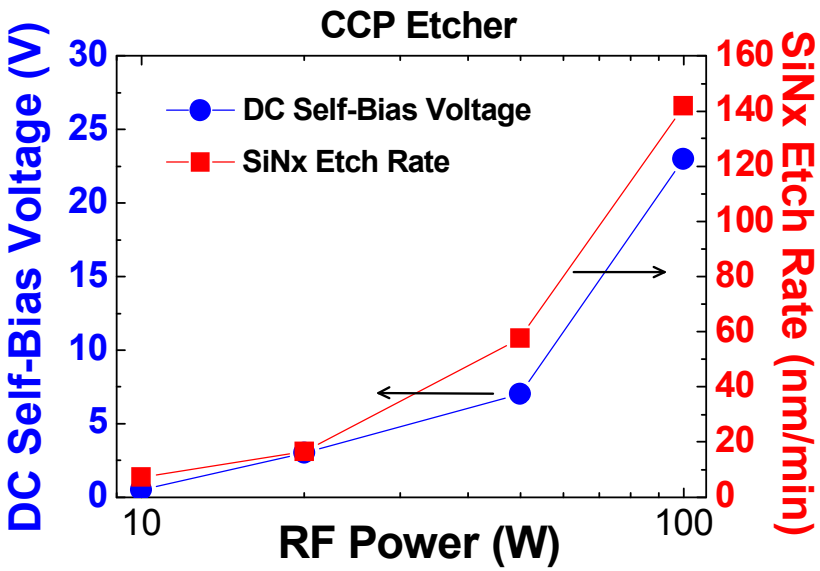
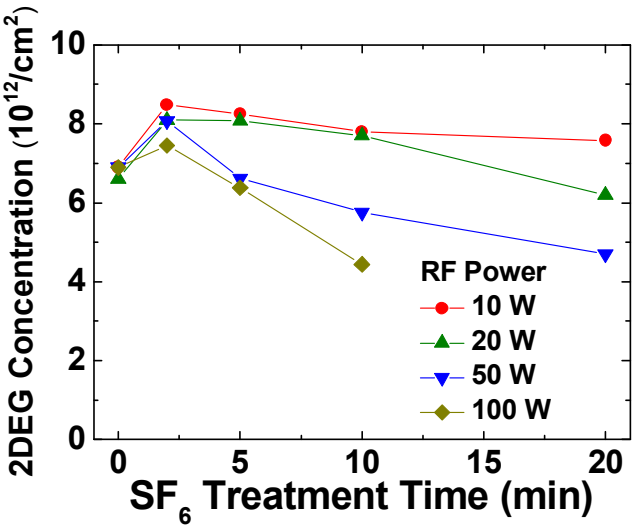
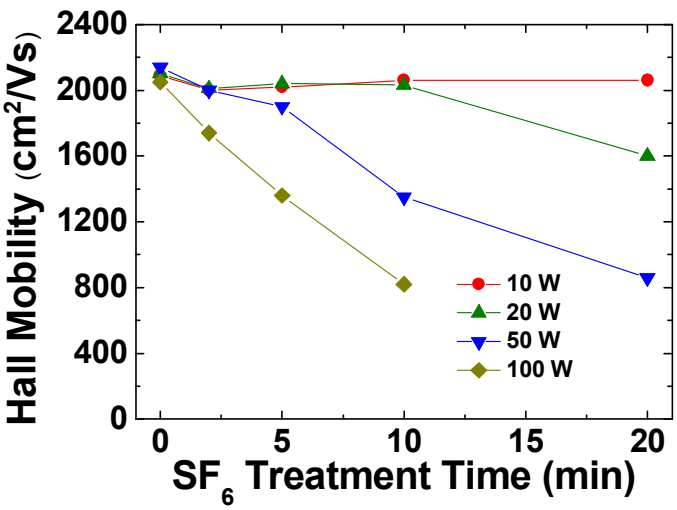


Fig. 5-4. DC self-bias voltage and SiN_x etch rate with respect to RF power (CCP etcher)



(a)



(b)

Fig. 5-5. Hall-effect measurement varying a RF power and SF_6 plasma treatment time

(a) 2DEG carrier concentration (b) Hall mobility

Similar experiment was executed with an inductively coupled plasma (ICP) etcher for comparison with a CCP etcher. The measured DC self-bias voltage and SiN_x etch rates for various pressure are shown in Fig. 5-6. SF_6 plasma treatment conditions were a gas flow rate of 50 sccm, a source power of 100 W, and a bias power of 10 W. SiN_x etch rate was decreased with increasing chamber pressure. DC self-bias voltage was saturated as 17 V with increasing chamber pressure over 20 mTorr. A DC self-bias voltage of 1 V and a SiN_x etch rate of 5.5 nm/min were obtained at a RF power of 100/10 W and chamber pressure of 20 mTorr.

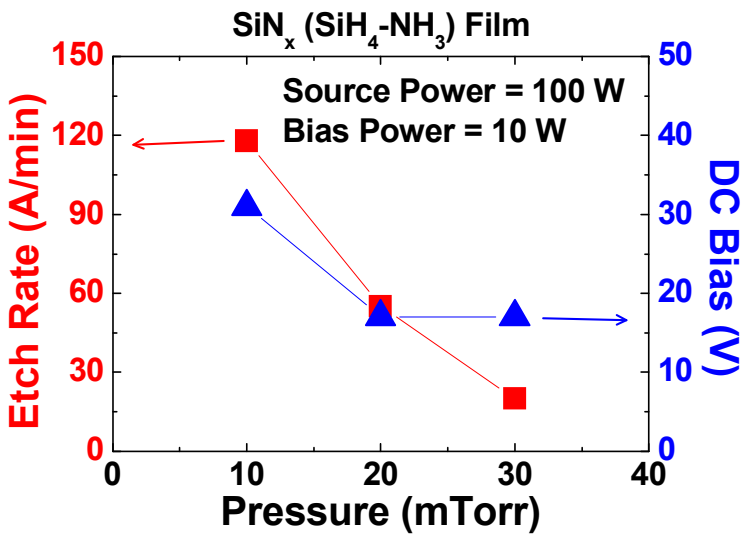


Fig. 5-6. DC self-bias voltage and SiN_x etch rate with respect to chamber pressure (ICP etcher)

5.2.3 Schottky HEMT with redeposition process

Schottky HEMTs were fabricated using redeposition process as described in Fig. 5-3. For comparison with a Schottky HEMT with a SF_6 plasma surface treatment, SiN_x removal was also executed with buffered oxide etchant (1:7) wet etchant. Figure 5-7 shows the buffer isolation current with a redeposition process. Both samples with a wet chemical (BOE) treatment and a SF_6 plasma treatment show the isolation current about 10 nm/mm which would not influence on the gate leakage of Schottky HEMTs. Figure 5-8 shows the gate leakage current of the fabricated Schottky HEMTs with a different SF_6 plasma etching time. The gate leakage current was decreased with a SF_6 plasma treatment with a CCP etcher, especially with etching time of 2 min [8]. However, almost identical gate current was measured with an ICP etcher.

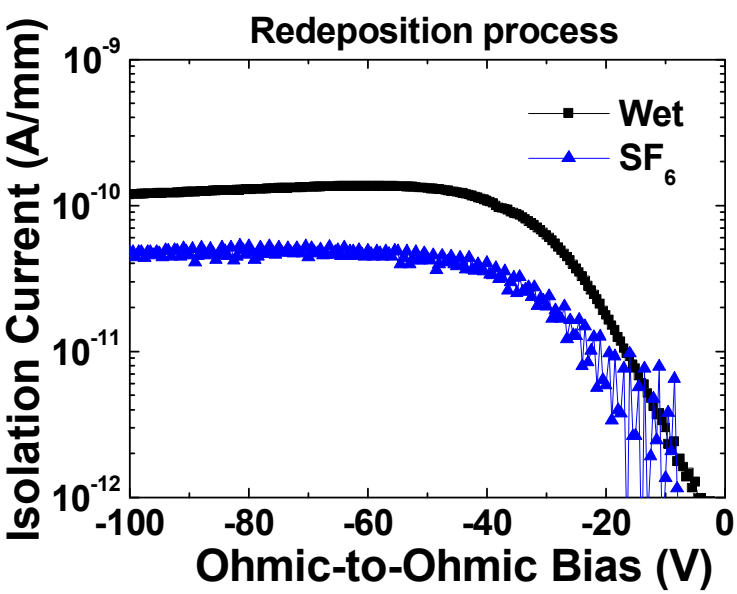
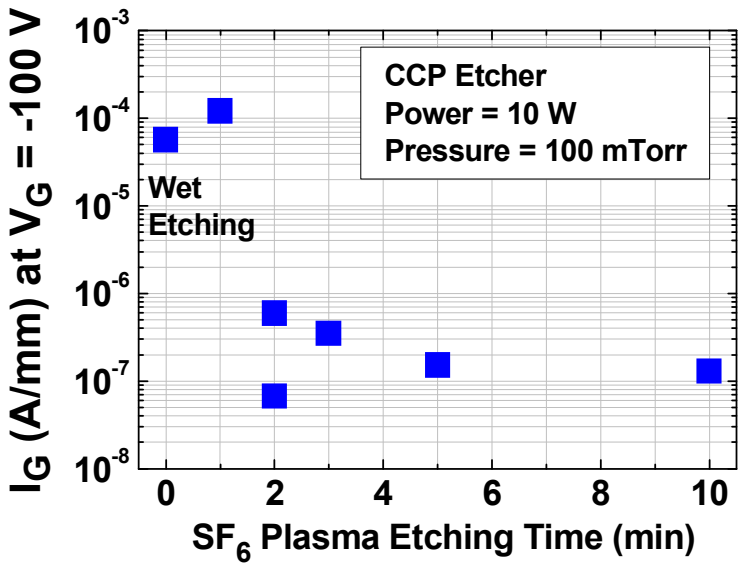
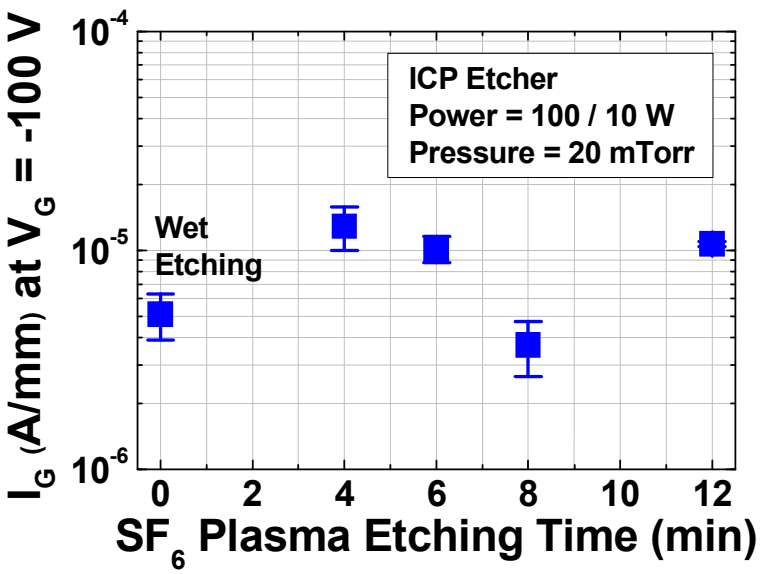


Fig. 5-7. Buffer isolation current



(a) [8]



(b)

Fig. 5-8. Gate leakage current of Schottky HEMT with different SF_6 plasma etching time

(a) CCP etcher with a etch rate of 7.3 nm/min

(b) ICP etcher with a etch rate of 5.5 nm/min

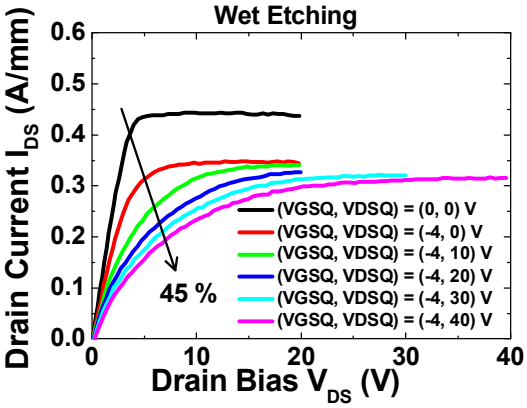
Figure 5-9 shows the pulsed I-V characteristics of the fabricated Schottky HEMTs with a different SF_6 plasma etching time. Gate length and gate-to-drain distance are 2 μm and 3 μm, respectively. Gate quiescent bias (V_{GSQ}) was -4 V to pinch-off the channel and drain quiescent bias (V_{DSQ}) was varied from 0 V to 40 V. DC gate bias (V_{GS}) was 1 V, and drain bias (V_{DS}) was swept from 0 V to 40 V. Current collapse ratio I_{pulse} (-4, 40) / I_{pulse} (-4, 40) is shown in Fig. 5-9 (f). I_{pulse} (-4, 40) and I_{pulse} (-4, 40) are drain current near the knee voltage defined as follows.

I_{pulse} (0, 0) = I_{DS} (V_{GSQ} = 0 V, V_{DSQ} = 0 V) at V_{GS} = 1 V, V_{DS} = 5 V

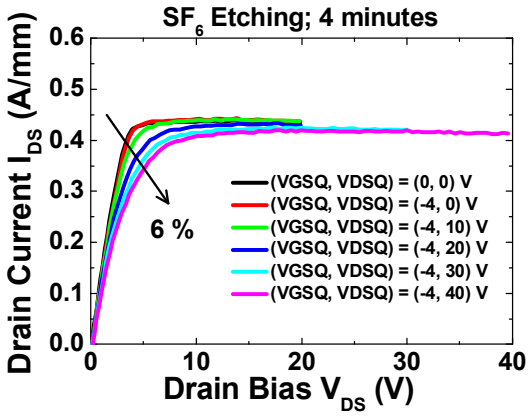
I_{pulse} (-4, 40) = I_{DS} (V_{GSQ} = -4 V, V_{DSQ} = 40 V) at V_{GS} = 1 V, V_{DS} = 10 V

It is clear that SF_6 plasma treatment improves the pulsed I-V characteristics. However, there is serious current collapse in the Schottky HEMT with a wet etching. Improved GaN surface with a SF_6 plasma treatment means that the diminishment of surface traps like nitrogen-vacancies which cause current collapse phenomenon.

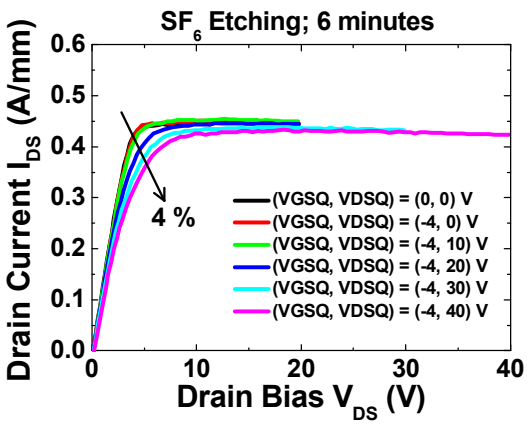
Figure 5-10 shows the off-state breakdown characteristics of the fabricated Schottky HEMTs discussed in the previous chapters. Off-state breakdown voltage of Schottky HEMT with a redeposition process was over 1100 V and leakage current level is 7.4 μA/mm at -600 V. The breakdown voltages versus specific on-resistance discussed in the previous chapters are shown in Fig. 5-11.


Wet Etching
Drain Current I_{DS} (A/mm)
Drain Bias V_{DS} (V)
45 %
(VGSQ, VDSQ) = (0, 0) V
(VGSQ, VDSQ) = (-4, 0) V
(VGSQ, VDSQ) = (-4, 10) V
(VGSQ, VDSQ) = (-4, 20) V
(VGSQ, VDSQ) = (-4, 30) V
(VGSQ, VDSQ) = (-4, 40) V

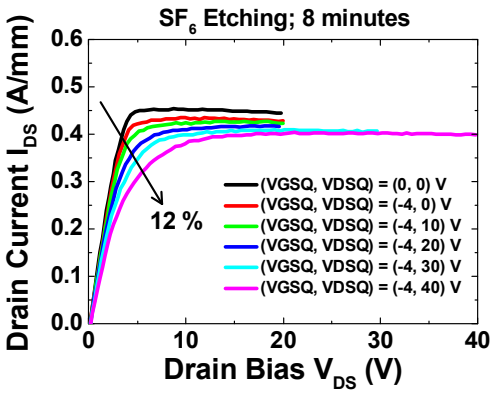
(a)


SF_6 Etching; 4 minutes
Drain Current I_{DS} (A/mm)
Drain Bias V_{DS} (V)
6 %
(VGSQ, VDSQ) = (0, 0) V
(VGSQ, VDSQ) = (-4, 0) V
(VGSQ, VDSQ) = (-4, 10) V
(VGSQ, VDSQ) = (-4, 20) V
(VGSQ, VDSQ) = (-4, 30) V
(VGSQ, VDSQ) = (-4, 40) V

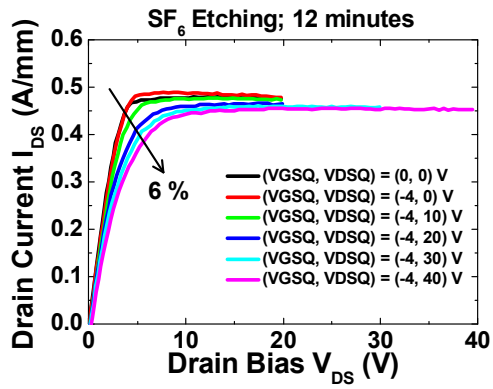
(b)


SF_6 Etching; 6 minutes
Drain Current I_{DS} (A/mm)
Drain Bias V_{DS} (V)
4 %
(VGSQ, VDSQ) = (0, 0) V
(VGSQ, VDSQ) = (-4, 0) V
(VGSQ, VDSQ) = (-4, 10) V
(VGSQ, VDSQ) = (-4, 20) V
(VGSQ, VDSQ) = (-4, 30) V
(VGSQ, VDSQ) = (-4, 40) V

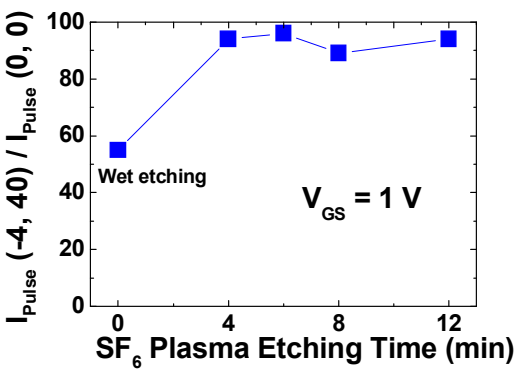
(c)



(d)



(e)



(f)

Fig. 5-9. Pulsed I-V characteristics of Schottky HEMT with different SF_6 plasma etching time

(a) Wet etching (b) 4 min (c) 6 min (d) 8 min (e) 12 min (f) current collapse ratio

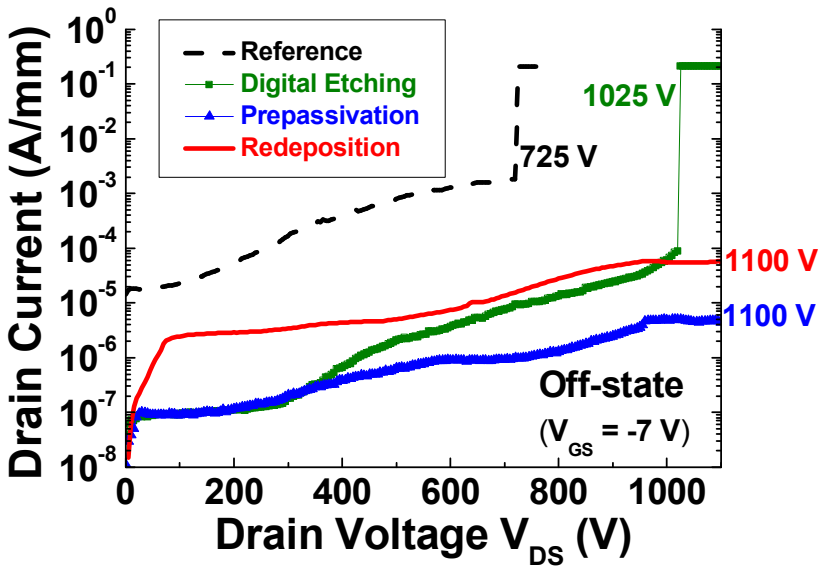


Fig. 5-10. Off-state breakdown characteristics of fabricated Schottky HEMTs

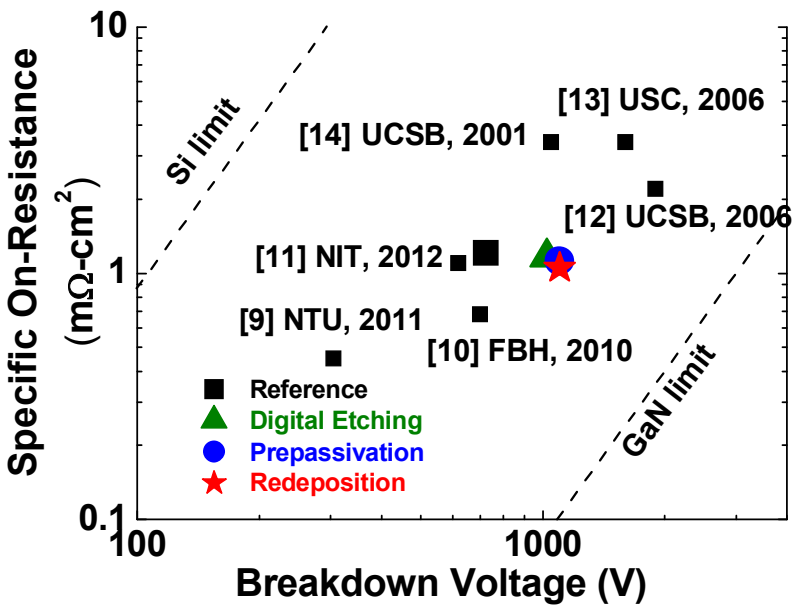


Fig. 5-11. Breakdown voltage vs. specific on-resistance of fabricated Schottky HEMTs

5.3 AlGaN/GaN SBD with anode edge terminated SiN_x layer

5.3.1 Unit SBD fabrication

Redeposition process with a SF_6 plasma treatment drastically reduced the current collapse issues described in chapter 5.2. However, leakage current level of HEMT with a redeposition process was 1 order larger than HEMT with a prepassivation process. In general, reverse current level of a SBD is strongly correlated with a leakage level of Schottky HEMT. Thus, anode edge terminated GaN SBD was proposed to reduce the reverse current of SBD with a redeposition process.

The epi-layer structure consisted of a 4-nm GaN capping layer, a 20-nm $Al_{0.23}Ga_{0.77}N$ barrier, a 300-nm undoped GaN layer, and 3.9-μm carbon-doped GaN buffer layer on a Si substrate as explained in Fig. 3-14 was used. Samples were cleaned with boiled solvent, SPM, diluted HF (1:10). Next, 10-nm-thick SiN_x layer was deposited on the GaN surface using ICP-CVD at 350 °C for surface protection during high temperature ohmic annealing. Ohmic contact was formed with an 800 °C annealing. Mesa isolation structure was formed with ICP-RIE with BCl_3/Cl_2 gas plasma. Wide recess was executed with different depths, i.e., 14, 17.5, 21 nm. 2DEG channel was not fully recess-etched intentionally, thus acting as normally-on. Two-step etching discussed in chapter 3 was used for low damage epi-layer etching. Next, whole sample surface was etched with a SF_6 plasma for 6 minutes to remove the prepassivated 10-nm-thick SiN_x layer and to treat the GaN surface as discussed in chapter 5-2. 200-nm-thick SiN_x film was deposited at 300 °C for surface passivation. Anode region was fully recessed to form the 2DEG-

metal Schottky contact. Finally, Ni/Au (=40/160 nm) metal was deposited to form a Schottky contact and anode field plate with 2 μm length.

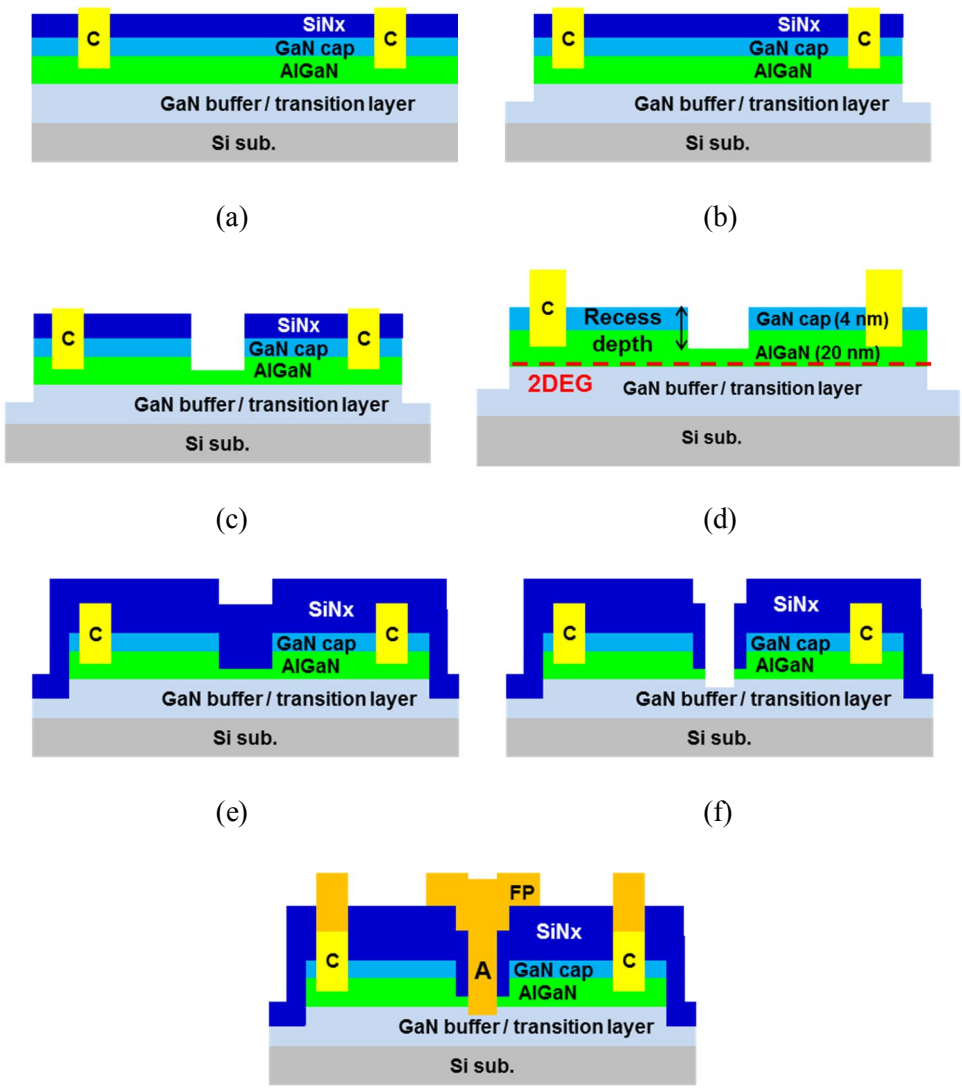


Fig. 5-12. Process flow of GaN SBD with anode edge termination

(a) Prepassivation and ohmic contact formation

(b) Mesa isolation (c) Wide recess

(d) SiN_x removal with SF_6 plasma etching

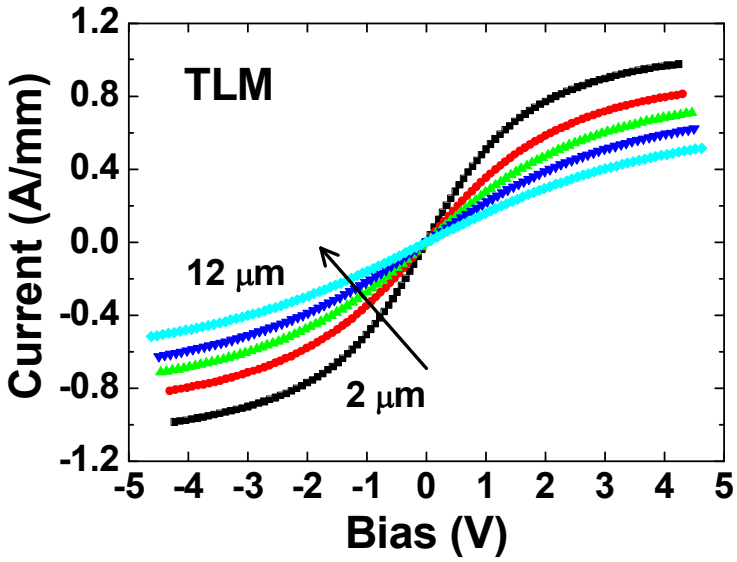
(e) SiN_x redeposition

(f) Anode full recess

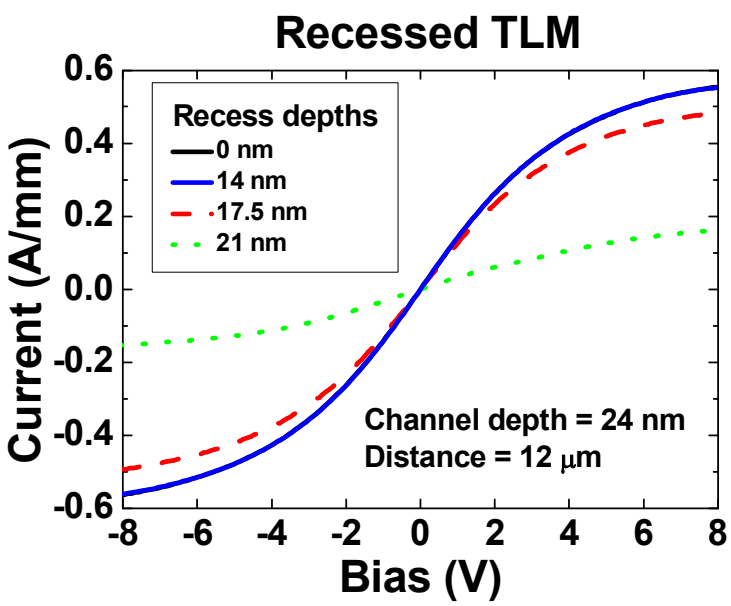
(g) Schottky metal deposition

5.3.2 Unit SBD measurement results

Ohmic contact resistance of 0.42 Ω-mm and sheet resistance of 450 Ω/sq were measured as shown in Fig. 5-13 (a). Spacing between ohmic contacts are 2, 4, 6, 8, 12 μm. Recessed TLM structure shown in Fig. 5-12 (e) was measured to check the influence of wide recess depths on ohmic-to-ohmic current. Figure 5-13 (b) shows the recessed TLM results. Identical ohmic-to-ohmic current flows with the recess depths of 0 nm and 14 nm, which means that 2DEG channel carrier concentration and mobility was not degraded. Ohmic-to-ohmic current decreased with the recess depths of 17.5 nm and 21 nm, which means that 2DEG carrier concentration was decreased.



(a)



(b)

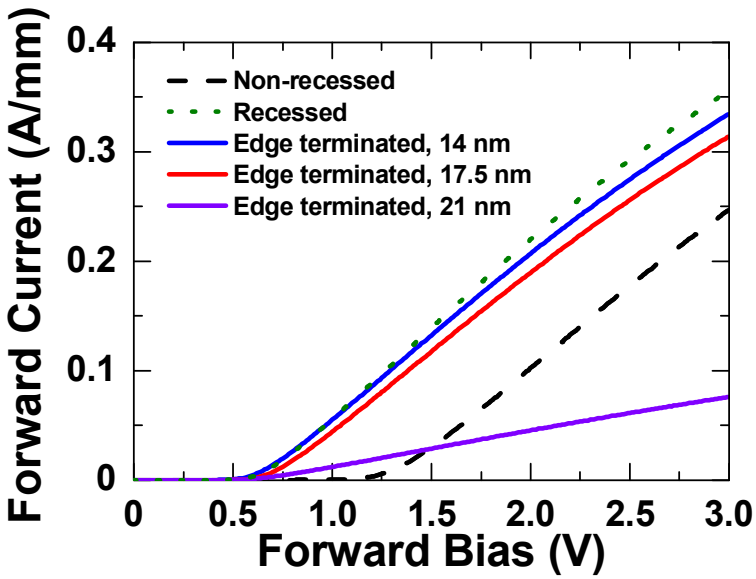
Fig. 5-13. TLM current

(a) Conventional TLM (b) Recessed TLM

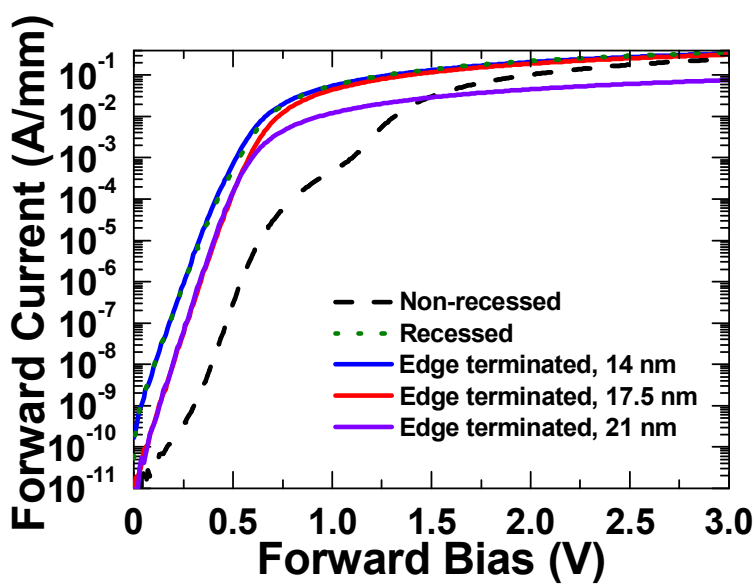
Figure 5-14 (a) shows the typical forward I-V characteristics of the GaN SBDs with respect to wide recess depths. The SBDs with an anode-to-cathode distance (L_{AC}) of 10 μm were measured. On resistance of recessed SBDs are decreased with the increase of wide recess depths are increased which is similar trends with the recessed TLM depicted in Fig. 5-13. Non-recessed SBD shows the forward turn-on voltage of 1.1 V. The forward turn-on voltages of recessed SBDs are 0.6 V, because of fully recessed Schottky contact. Figure 5-14 (b) show the forward I-V characteristics with log-scale. The ideality factor and SBH calculated from the thermionic theory are shown in Table 5-1. SBH decreased with recessed Schottky contacts. Among recessed SBDs, better ideality factor and higher SBH were obtained with the wide recess depths of 17.5 nm and 21 nm. Thus, it could be thought that reduced forward current is correlated with the improved Schottky contacts.

The reverse characteristics are shown in Fig. 5-15. The reverse bias was applied to 1100 V due to limitation of measurement equipment. The reverse current level of edge terminated SBDs are inversely proportional to wide recess depths which are related with an on-resistance. Edge terminated SBD with wide recess depth of 17.5 nm is adequate considering both forward current and reverse current.

Uniformity of fabricated SBDs are estimated as shown in Fig. 5-16. Forward voltages corresponding with a forward current at the 1 mA/mm and 100 mA/mm are counted. Standard deviation of the forward voltages was 0.013 V. Standard deviation of the reverse current was 0.76 μA/mm at -100 V. Thus, the uniformity of the edge terminated SBDs are enough to fabricate the large area SBDs.



(a)



(b)

Fig. 5-14. Forward I-V characteristics

(a) Linear (b) Log scale

Table 5-1. Ideality factor and Schottky barrier height of fabricated SBDs

Channel depth 24 nm	Non-recessed	Recessed	Edge terminated (14 nm)	Edge terminated (17.5 nm)	Edge terminated (21 nm)
Ideality factor	1.20	1.27	1.26	1.16	1.16
Schottky barrier height (eV)	1.00	0.76	0.76	0.84	0.84

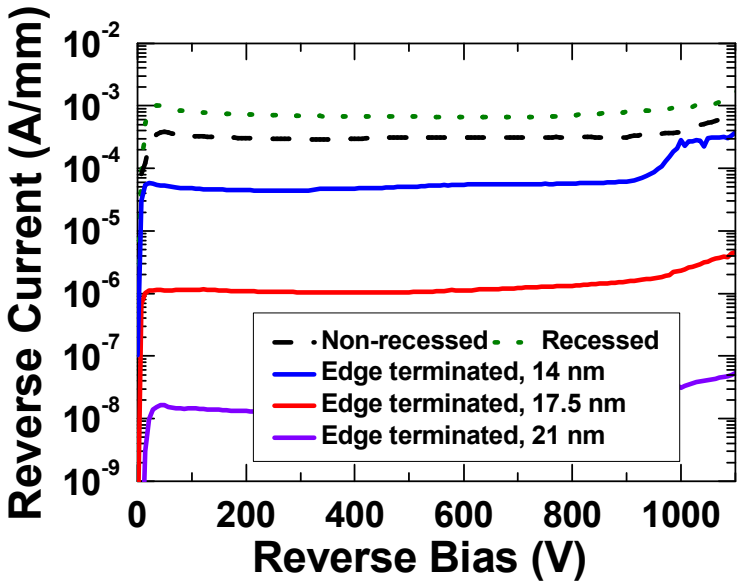


Fig. 5-15. Reverse I-V characteristics

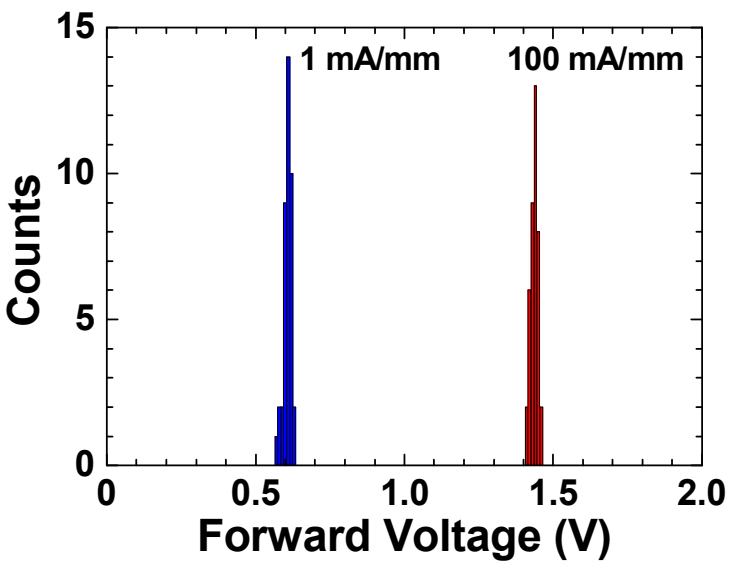


Fig. 5-16. Forward I-V characteristics uniformity (40 devices)

The C-V curves of SBDs are shown in Fig. 5-17. Measured small signal frequency and AC voltage were 1 MHz and 30 mV, respectively. The capacitances measured at 0 V are 30 pF for non-recessed SBD. Edge terminated SBDs shows very small capacitance due to the fully recessed Schottky contacts. SBD with recess depths of 14 nm and 17.5 nm was not fully depleted at the bias of -7 V due to the metal-insulator-semiconductor structure. It is expected that fast switching speed of fabricated SBDs, since the edge terminated SBDs are based on 2DEG-metal Schottky contact

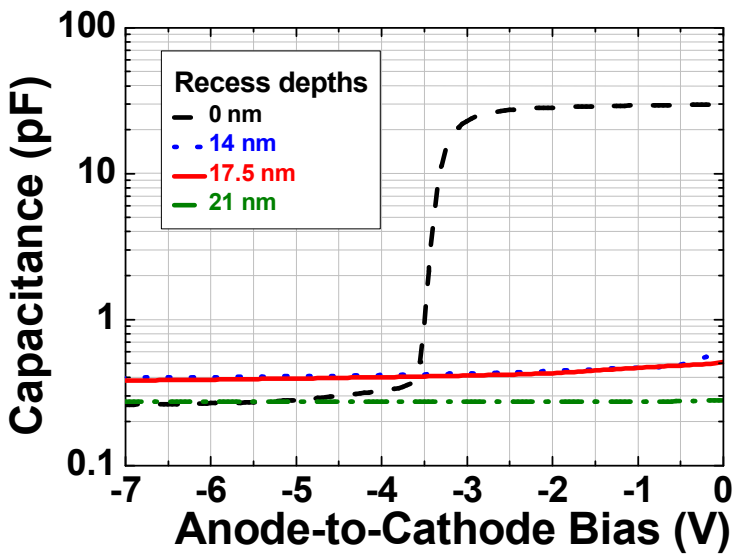
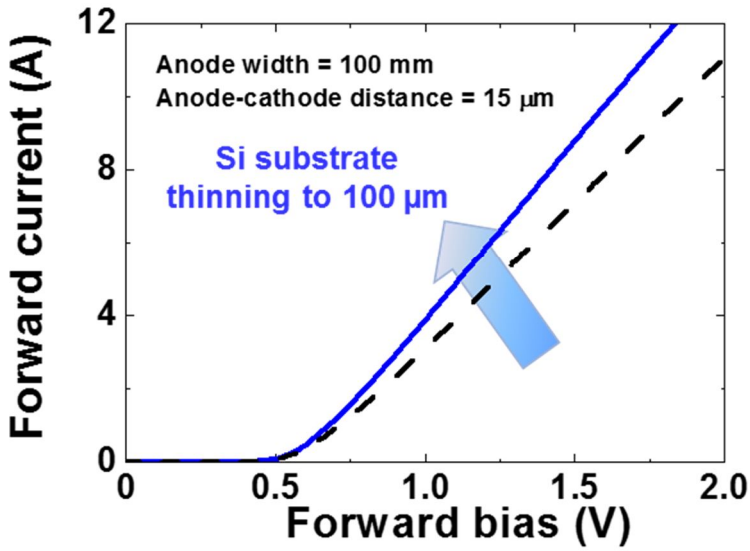


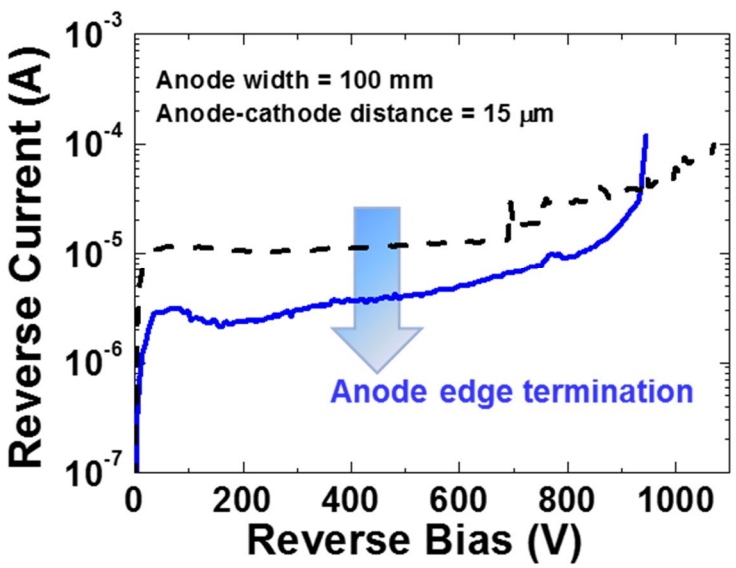
Fig. 5-17. C-V curve of edge terminated GaN SBDs

5.3.3 Large area GaN SBD with edge termination

The multi-finger lateral-type GaN SBDs with anode edge terminations were fabricated. Large area SBDs with 100 mm width and 15 μm anode-to-cathode distance were fabricated. Anode length and cathode length were both 10 μm. Active area of large area SBDs was 5 mm^2 which is identical with a fully recessed SBDs discussed in chapter 4.4. The forward current at 1.5 V is 8.7 A as depicted in Fig. 5-18 (a). The reverse breakdown voltage at leakage current of 100 μA is 945 V as depicted in Fig. 5-18 (b). Specific on-resistance is 5.0 mΩ-cm^2. To reduce the on-resistance of SBDs, electrodes were electroplated and Si backside was thinned to 100 μm. The figure of merit V_{BR}^2/R_{on} of fabricated large area SBD is 180 MW/cm^2 which is one of the highest value of the lateral-type large area GaN SBDs ever reported. Table 5-2 shows I-V characteristics of other group's results for comparison.



(a)



(b)

Fig. 5-18. I-V characteristics of fabricated large area SBD with edge termination

(a) Forward I-V characteristic

(b) Reverse breakdown characteristic

Table 5-2. Comparison of I-V performance

	Cree (C3D04065A)	ROHM (SCS210KE2)	Samsung [15]	Fully recessed	Edge terminated
Material	SiC	SiC	GaN	GaN	GaN
Size (mm^2)	-	-	9	5	5
I_F (A) at 1.5 V	4.5	5	4.5	7.0	8.7
I_R (μA) at -600 V	0.4	0.008	6	12.5	4.3

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Chapter 6. Thin-Film Based Packaging Technology

6.1 Introduction

The needs for a low-volume and high performance module make the packaging issues more important from power module to millimeter-wave frequency [1]-[5]. Benzocyclobutene (BCB) based thin-film technology can be a good candidate for these packaging trends, because BCB has a low relative dielectric constant (2.65) and a low tangent loss (0.002 at 10 GHz). Thin-film technology using BCB not only provides excellent electrical performance, but is also capable of achieving high-resolution patterns, which is favorable in high frequency compared with liquid crystal polymer (LCP) or low-temperature co-fired ceramic (LTCC) based system-on-package (SOP) technology [6]-[8]. Thanks to these advantages, there have been various applications using BCB-based thin-film technology, such as power-combining modules and RF transceiver module [3], [4], [9]-[11].

However, there is a mechanical barrier to use of BCB as a passivation insulator. In the following sections, adhesion and mechanical stress issues of BCB will be discussed.

6.2 Improvement of BCB adhesion on Cr/Au metal layer

One of the mechanical problems in BCB for module application is an adhesion issue. The inertness of gold makes it adequate for the metal layer of GaN interconnection layer. Unfortunately, its inertness means that gold does not adhere well with organic materials such as BCB and polyimide. There are many reports that organic materials have a very poor interfacial fracture resistance (adhesion) to gold [12]-[15]. However, the adhesion between BCB and inorganic materials, such as SiO_2 and SiN_x is good [16]. Thus, the insertion of a layer of inorganic materials between gold and BCB can improve the adhesion.

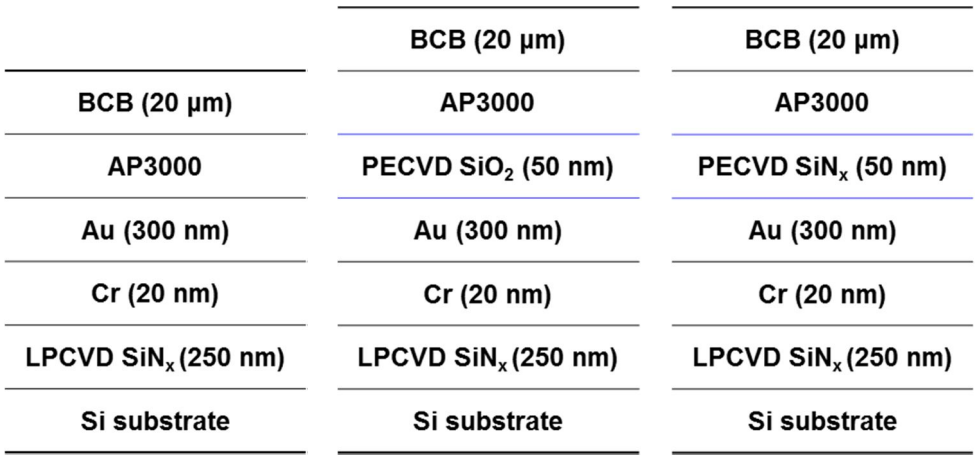
Figure 6-1 shows the whole structures of the samples for the adhesion experiment. The structures are similar to the conventional interconnection line used in the GaN power device. The difference between samples are the presence of additional plasma-enhanced chemical vapor deposition (PECVD) SiO_2 and SiN_x layers. Oxygen plasma treatment was carried out for every interface to remove carbon contaminants and activate the surface. Gold oxide was removed by annealing before PECVD SiO_2 or SiN_x deposition [17].

Stresses of all the thin films used in the experiment was measured, because stresses present in thin films can cause deformation, fracture, and even delamination. Table 6-1 shows the process conditions and stresses of the thin films used in the experiment. The measured stresses of the thin films were below 1 GPa and relatively low enough to prevent serious adhesion failure. The stress of PECVD SiO_2 or SiN_x can be lowered by the adjusting low frequency (187 kHz) and high frequency (13.56 MHz) power, as described in ref. 18. However, some

compressive stresses are needed for stress compensation, as will be described in following section.

The adhesive tape test, diesaw test as a qualitative method and shear test as a quantitative method were executed to evaluate the adhesion strength of the BCB-based module structure, as shown in Fig. 6-1 [19]-[21]. Figure 6-2 shows the microscope image of conventional and PECVD SiO_2 inserted structure which are shown in Fig. 6-1 after the diesaw test at a speed of 10 mm/s by a DAD-3350 dicing saw. In conventional structure, most of the BCB was delaminated from Cr/Au because the adhesion strength between Au and BCB was too weak against the external force during sawing. Moreover, the remaining BCB on Cr/Au in Fig. 6-2(a) was peeled off by the adhesive tape test. In SiO_2 or SiN_x inserted structure, most of the BCB was not delaminated from Cr/Au by the adhesive tape test and the diesaw test, even after the samples were kept at 85 °C/85% relative humidity (RH) condition for more than 1000 h. This is because inserted layer of SiO_2 or SiN_x has a high bonding strength to both Au and BCB and holds them well.

BCB bumps of cylindrical shape and 5.5 μm height were fabricated for the shear test as shown in Fig. 6-3. A dry-etch BCB film was etched vertically for the shear test in a capacitively coupled plasma (CCP) etcher. The dry etch conditions were gas flows of O_2, 60 sccm; CF_4, 40 sccm; Ar, 10 sccm; a chamber pressure of 0.04 Torr, and an RF power of 200 W. Figure 6-4 shows the shear test results. As expected, SiO_2 or SiN_x inserted structure show much higher shear strength than conventional structure. The shear strength is not constant as the BCB bump diameter changes, which may be due to the concentration of stresses in the interface near the shear tool [21]. The dotted line represents the shear strength of BCB on a BCB bump for comparison [21].



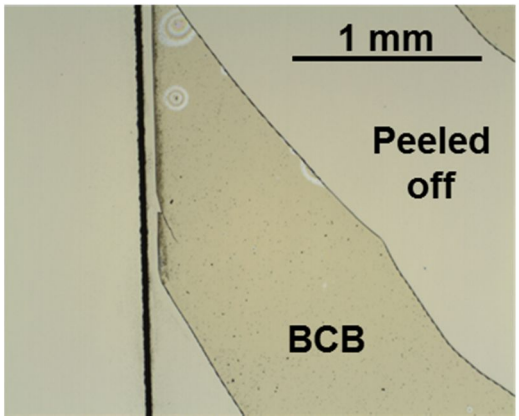
(a) (b) (c)

Fig. 6-1. Structure of the experimental samples for adhesion experiments

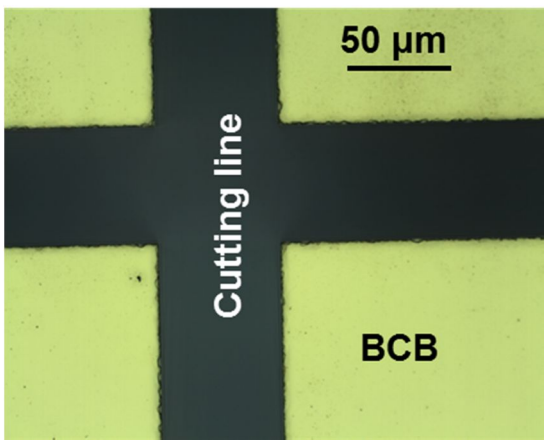
(a) Conventional (b) SiO_2 inserted (c) SiN_x inserted structure

Table 6-1. Process conditions and stress of thin films

Layer	Process conditions	Stress (MPa)
BCB	Cured at 250 °C for 1 hr	27
PECVD SiO_2	Deposited at 300 °C	-432
PECVD SiN_x	Deposited at 300 °C	-210
Cr/Au	Evaporated at 3×10^{-6} Torr	14
LPCVD SiN_x	Deposited at 800 °C	70



(a)



(b)

Fig. 6-2. Microscope image after diesaw test at a speed of 10 mm/s by a DAD-3350 dicing saw

(a) Failed conventional structure

(b) SiO_2 inserted structure after 1000 h of 85 °C/85% RH reliability test

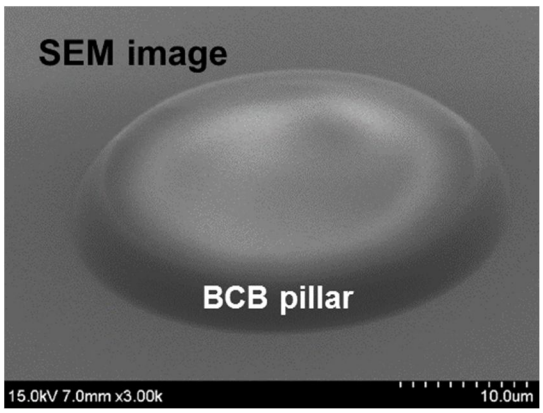


Fig. 6-3. Scanning electron microscope (SEM) image of BCB pillar

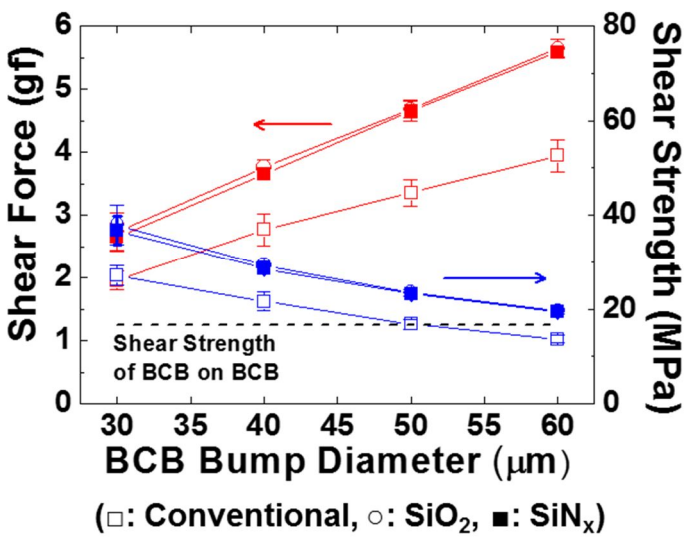


Fig. 6-4. Shear test results of BCB

6.3 Stress compensation

Stresses arise from the deposition of thin films during the semiconductor process. BCB, which is a thermosetting material, is fully cured at 250 °C and a tensile stress of 28 MPa develops at room temperature. Film stress can be estimated by the measurement of the radius of curvature of the Si substrate using an optical laser. If a film with tensile stress is deposited on a Si substrate, the Si wafer will bend to relax the film stress. The wafer bow caused by a 20-μm-thick BCB layer on a Si substrate can be calculated from the Stoney formula [22],

$$\sigma_f = \frac{E_s}{1-\nu_s}\frac{{t_s}^2}{6t_f}\left(\frac{1}{R}-\frac{1}{R_0}\right) \tag{6.1}$$

$$\text{wafer bow} = \frac{(\text{radius of wafer})^2}{2R} \tag{6.2}$$

where σ_f is the average film stress, $E_s/(1-\nu_s)$ is the biaxial elastic modulus of the substrate, t_s and t_f are the substrate and film thickness, respectively, and R_0 and R are radius of curvature of the substrate before and after the film deposition, respectively. If it is assumed that the 4 inch wafer was perfectly flat before film deposition, the calculated radius of curvature is 14.8 μm and the wafer bow is 84.4 μm after the 20-μm-thick BCB layer was deposited. Wafer bow causes several process problems, such as vacuum processing and heat dissipation during dry etching to a heat sink. The importance of wafer bow was already reported in the fabrication of three-dimensional (3D) integrated circuits [23].

To solve this problem, stress compensation toward the compressive direction is

needed. PECVD SiO_2 usually has compressive stress on the Si substrate, because the coefficient of thermal expansion (CTE) of SiO_2 is smaller than that of Si. In a previous chapter, a PECVD SiO_2 layer was deposited on Cr/Au to improve the adhesion with BCB. Thus, PECVD SiO_2 can be used to give a compressive stress to a thin film stack without any redundant process step. Figure 6-5 shows the 4 inch Si wafer bow at a subsequential process steps. A 1-μm-thick Cr/Au layer was deposited instead of 320-nm-thick Cr/Au in the modified structure. A 1-μm-thick SiO_2 layer was deposited on the Cr/Au for stress compensation. PECVD SiN_x could be also used as a stress compensator, but the thickness of SiN_x should be twice that of SiO_2, because the stress of SiN_x (-210 MPa) is half that of SiO_2 (-432 MPa).

The force per unit width, which equals with stress multiplication film thickness, of the multilayer is the sum of the forces of each layer [24]. In this way, the wafer bow is calculated as 22.0 μm after the coating of a 20-μm-thick BCB, as depicted in Fig. 4(b). However, the measured wafer bow is 33.3 μm larger than calculated value. The reason for this discrepancy is the structural change of the Cr/Au during the deposition process of the SiO_2. The deposition temperature and time for a 1-μm-thick SiO_2 layer were 300 °C and 30 min, respectively, which are sufficient to change the structure of the Cr/Au grains and vacancies. Generally, structural changes in metal can cause plastic deformation and increase tensile stress [25], [26]. Nevertheless, the wafer bow was lowered from 79.3 μm without SiO_2 to 55.2 μm with SiO_2. A thickness over 1 μm of SiO_2 will give more compressive force. However, there is a limitation for SiO_2 thickness because SiO_2 must be etched away to form an electrical connection. The deposition of a film with more compressive stress on the front side or a film with tensile stress on the backside of

the wafer may solve these stress-related problems.

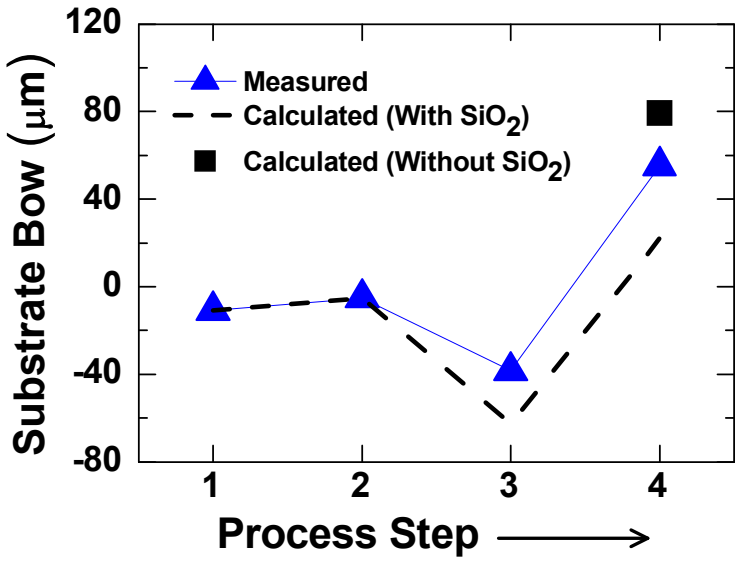


Fig. 6-5. Substrate bow at a subsequential process steps

Process 1. Initial 4-inch wafer

Process 2. LPCVD SiN_x and Cr/Au deposition

Process 3. 1-μm-thick SiO_2 deposition

Process 4. 20-μm-thick BCB coating

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Chapter 7. Conclusions and Future Works

Demand on high efficiency power modules is increasing day by day. According to these trends, GaN has been emerged as a breakthrough material to satisfy a high efficiency power devices. GaN has a high electron mobility, high saturation velocity, and high critical voltage. Thus, Baliga's figure of merit of GaN is much higher than Si. AlGaN/GaN heterostructure shows high carrier concentration confinement over 10^{13} cm^{-2}, due to large bandgap discontinuity and polarization effect. Thanks to these advantages, AlGaN/GaN power devices show superior on-state conduction and high reverse blocking capability. However, undesired high turn-on voltage of AlGaN/GaN SBD due to the wide bandgap of GaN is linked with on-state losses.

In this work, recessed Schottky contact scheme was used to achieve the AlGaN/GaN SBD requirements. Chapter 3 describes the development of wet digital etching with self-limiting property. The measured etch rate of wet digital etching was 0.5 nm per cycle. GaN process involves epi-layer etching and high temperature annealing steps. Thus, GaN surface is prone to be damaged during device fabrication. Recovery of deteriorated GaN surface was verified with a measurement of Hall pattern and buffer isolation current. Digital etching was applied to the fabrication of SBDs and HEMTs. By adoption of a digital etching on SBD, ideality factor and Schottky barrier height were improved from 1.35 to 1.19 and 0.60 eV to 0.73 eV, respectively. On/off ratio of Schottky HEMT was increased from 8.9×10^3 to 4.9×10^6 with a digital etching. Breakdown voltage of Schottky HEMT was also increased from 725 V to 1025 V with a digital etching.

In chapter 4, recessed AlGaN/GaN SBDs were analyzed with respect to the anode recess depths. With a fully recessed anode, AlGaN/GaN SBD with turn-on voltage of 0.52 V, ideality factor of 1.17, Schottky barrier height of 0.76 eV, forward current of 127 mA/mm at 1.5 V, and reverse current of 2 μA/mm at -1100 V was fabricated. The reliability of fabricated diode was evaluated through the high temperature and high reverse bias test. Double field plate structure was also studied to increase the breakdown voltage of SBD. The electric field distribution of AlGaN/GaN SBD at the reverse bias condition was simulated with device simulator. Measured breakdown voltage was increased from 925 V to 1065 V with the double field plate structure. Based on aforementioned device engineering, large area AlGaN/GaN SBD with fully recessed anode was fabricated. The forward current of 7.1 A at 1.5 V, specific on-resistance of 6.1 $m\Omega \cdot cm^2$, reverse current of 12.5 μA at -600 V, and reverse breakdown voltage of 1080 V were measured. Calculated figure of merit (V_{BR}^2/R_{on}) is 192 MW/cm^2, which is one of the highest value of the lateral-type large area GaN SBDs ever reported. Fast reverse recovery time of 10 ns was measured with the fabricated SBD.

In chapter 5, anode edge terminated AlGaN/GaN SBDs were proposed. Forward current and reverse current were varied with a recess etching depths. With an optimum recess depth of 17.5 nm (i.e., remained AlGaN barrier layer of 6.5 nm), SBD with ideality factor of 1.16 and Schottky barrier height of 0.84 eV was fabricated. Multi-finger large area SBD was fabricated with the anode edge termination and showed a forward current of 8.7 A at 1.5 V, specific on-resistance of 5.0 $m\Omega \cdot cm^2$, reverse current of 4.3 μA at -600 V, and reverse breakdown voltage of 945 V. Fabricated large area SBD exhibits a figure of merit (V_{BR}^2/R_{on}) as 180 MW/cm^2. These results indicate that fabricated AlGaN/GaN SBDs are adequate for

fast switching applications with low losses.

Finally, mechanical issues including adhesion and mechanical stress of BCB was discussed in chapter 6. Improvement of BCB adhesion and relief of BCB stress was obtained with an additional SiO_2 and SiN_x layer. Developed technique can be applicable to the inter-metal dielectric of power device.

Integration of SBD and normally-off MIS-HEMT would be a next step of this work. Using a redeposition process as discussed in chapter 5, hetero-integration is possible as shown in Fig. 7-1. The advantage of this structure is the elimination of off-chip interconnection between diode and FET, which brings increase of interconnection resistance and inductance. It is indispensable to use of integrated power devices to increasing the operating frequency of power module.

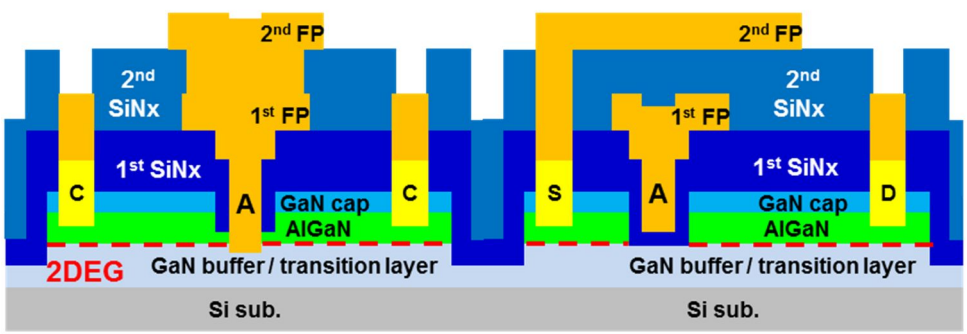

Fig. 7-1. Schematic of SBD & normally-off MIS-HEMT integration

초 록

최근에 알루미늄갈륨질화막/갈륨질화막 (AlGaN/GaN) 이종 접합 구조를 이용한 소자가 고 효율 전력 소자로서 큰 주목을 받고 있다. 이는 이러한 소자가 큰 전류 밀도, 높은 항복 전압 특성과 빠른 회복 시간을 갖기 때문이다. 본 논문은 전력 스위칭 소자로서 AlGaN/GaN 이종 접합 구조를 이용한 쇼트키 접합 다이오드 (SBD)와 쇼트키 접합 트랜지스터 (HEMT)에 관한 연구를 다루고 있다.

AlGaN/GaN 이종 접합 구조에 SiCN capping 층이 포함된 에피층을 사용하여 쇼트키 접합 HEMT를 제작하였다. 5 nm 두께의 SiCN 층을 포함한 에피층에서 그렇지 않은 에피층에 비해서 이차원 전자 가스 (2DEG) 캐리어 농도가 51 % 가량 증가하였다. 이는 AlGaN 표면의 negative polarization 전하가 중성화 되었기 때문이다. SiCN capping 층을 포함한 에피층을 사용하여 HEMT를 제작하여 10 % 가량의 드레인 전류 향상을 확인하였다. 또한, 보호 다이오드가 내장된 쇼트키-드레인 구조의 HEMT를 제작하였다. 이 다이오드는 0.7 V의 작은 on 전압과 100 V 이상의 blocking 능력을 가진 것으로 측정되었다.

AlGaN/GaN 다이오드 구조로서 recessed 쇼트키 접합이 연구되었다. 건식 식각과 5 nm/cycle의 식각 속도를 갖는 습식 digital 식각의 이중 식각 방법을 에피층을 식각하는 방법으로 제안하였다. 습식 digital 식각의 표면 처리 효과 때문에 제작한 다이오드의 ideality factor와 쇼트키 접합 높

이가 각각 1.35와 0.60 eV에서 1.19와 0.73 eV로 향상되었다.

애노드 recess 깊이의 영향을 분석하고 최적의 식각 깊이를 결정하였다. 그 결과로 0.52 V의 on 전압, 1.17의 ideality factor, 0.76 eV의 쇼트키 접합 높이, 1.5 V 기준으로 127 mA/mm의 순방향 전류, -1100 V 기준으로 2 μA/mm의 역방향 전류를 갖는 다이오드를 제작하였다. 제작한 다이오드는 200 °C, 200 V의 스트레스 조건에서 200 시간 동안 파괴되지 않았다.

다이오드의 항복 전압을 증가 시키기 위해서 이중 전계 판 구조가 연구되었다. 소자 시뮬레이션을 통해서 전계 판의 전기장 분산 효과를 확인하였다. 또한, 실험을 통하여 이중 전계 판 구조가 항복 전압을 925 V에서 1065 V까지 증가시킴을 확인하였다.

애노드 가장자리 termination 방법을 사용한 다이오드를 제안하였다. 이 구조를 통하면 표면 전류를 억제시킬 수 있기 때문에 다이오드의 역방향 전류를 10^3 배 가량 줄일 수 있었다. 제작한 다이오드는 우수한 균일도를 보여주었다.

앞선 단위 소자 연구를 바탕으로 multi-finger lateral-type AlGaN/GaN 쇼트키 접합 다이오드를 제작하였다. 제작한 대면적 다이오드는 1.5 V를 기준으로 7.1 A의 순방향 전류, 6.1 mΩ·cm^{2}의 specific on 저항, -600 V를 기준으로 12.5 μA의 역방향 전류, 1080 V의 항복 전압 특성을 보여준다. 이를 토대로 계산한 figure-of-merit (V_{BR}^2/R_{on})은 192 MW/cm^{2}이다. 이는 지금까지 발표된 lateral-type 대면적 GaN 다이오드 중에서 가장 높은 값 중 하나이다. 역 회복 시간은 10 ns로 측정되었다. 이러한 결과는 제안한 AlGaN/GaN 쇼트키 접합 다이오드가 저 손실 고속 스위칭 응용에 적합

함을 말해준다.

주요어: 전력 소자, 갈륨 질화막, 알루미늄갈륨질화막/갈륨질화막 이종 접합 구조, 쇼트키 접합 다이오드, 실리콘 질화막, 항복 전압

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