Ph. D. DISSERTATION

GIDL characteristics on $Si_{1-x}Ge_x$ pFinFET for Low Power Transistors

저전력용 트랜지스터를 위한 $Si_{1-x}Ge_x$ pFinFET 의 GIDL 특성

BY

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ABSTRACT

This dissertation presents an investigation of Gate-Induced-Drain-Leakage (GIDL) current in SiliconGermanium (SiGe) p-type FinFET for low power transistors and proposes the guidelines to reduce GIDL current. First, the main mechanism of GIDL current in FinFET was thoroughly investigated because conventional GIDL current is unexpected event in FinFET. Therefore, GIDL current in FinFET is analyzed by comparing that in MOSFET which has the same device specification as the FinFET. Second, the effects of Ge fraction and its distribution in internal fin on GIDL current were analyzed considering actually manufactured fin in SiGe FinFET. Third, the analysis of GIDL current by the device specifications and doping profile in drain region was presented. As a result, guidelines are presented considering the results above. The main mechanism and the characteristics of GIDL current in FinFET which are investigated in this dissertation would be and index to improve the characteristics of manufactured SiGe FinFET.

Key Words: SiliconGermanium (SiGe), finFET, Gate-Induced-Drain-Leakage (GIDL) band-to-band tunneling, TCAD simulation

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CONTENTS

Chapter 1

Introduction

1.1 Multigate MOSFET

The performance of semiconductor has been improved by scaling the gate length [1-3]. However, as the distance between source and drain regions decreases, the effect of electric potential from source and drain regions on channel increases while an ability of the gate to control channel region decreases. It is called ‘short channel effect (SHE)’ that limits the device scaling, and the Drain-Induced-Barrier-Lowering (DIBL) has been studied as the typical type of SHE [4-11]. As a result, various types of FET has been studied to overcome the limitation of device scaling.

Figure 1. shows the DIBL characteristics calculated by MASTAR according to gate length at bulk, FDSOI and DG MOSFET. Bulk, FDSOI, and DG MOSFET indicate the conventional MOSFET, fully depleted MOSFET that has a thin body on insulator [12-14], and double gate MOSFET that a channel is wrapped by two gate [15-18]. In case of the conventional type of one-gate MOSFET including FDSOI and bulk, as the gate length is shrunken below 10 nm, high value of DIBL over 100 mV/V which is considered as a tolerable value for transistor is expected. Only DG MOSFET would allow the transistor to

be scaled down continuously.

Figure 2. shows the gate length expected by ITRS for high performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits [19-20]. It shows which type of transistor can be used for short channel device. Beyond 2016, gate length would be shrunken to 10 nm, and DG MOSFET would be the only solution.

FinFET is a new type of transistor evolved from DG MOSFET [21-25]. As shown in Figure 3, FinFET is different from the conventional bulk MOSFET since channel region is surrounded by gate on three sides. Therefore, since the ability of gate to control the channel region is strong, it is considered as a transistor for the next generation. In this dissertation, a new type of gate-induced-drain-leakage current in FinFET will be investigated.

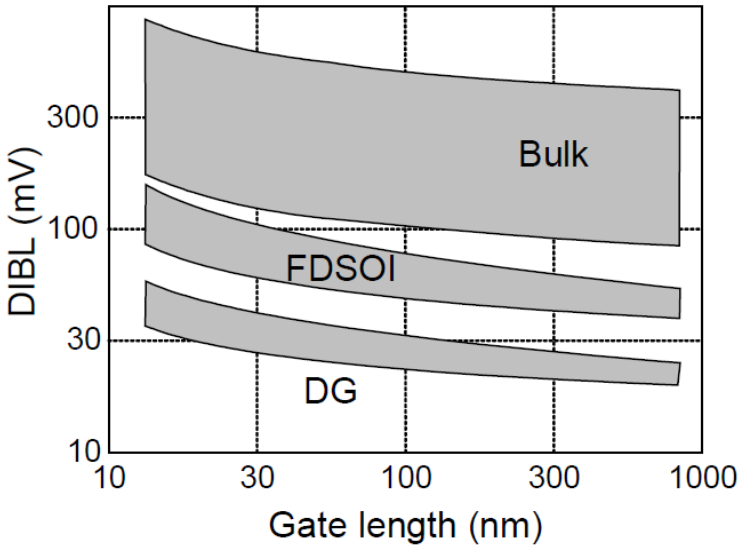


Fig. 1. DIBL characteristics calculated by MASTAR according to gate length at Bulk, fully depleted SOI (FDSOI), and double-gate (DG) MOSFET [20]

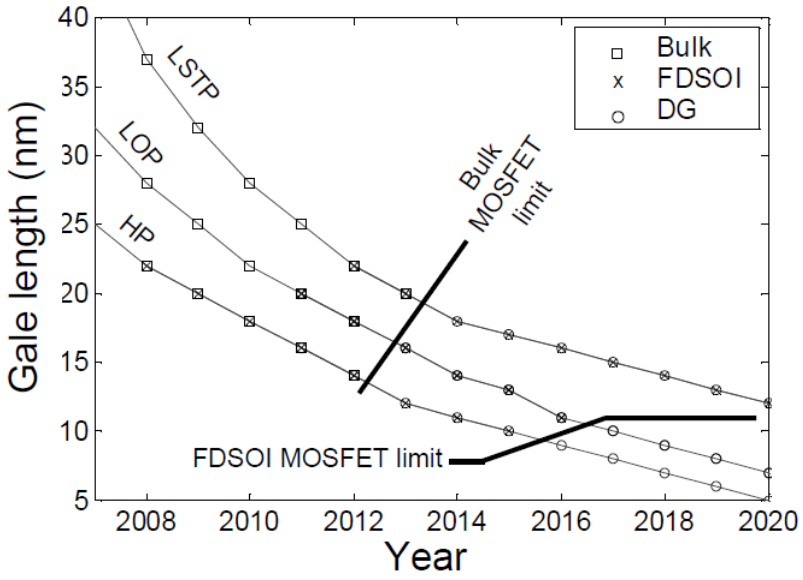


Fig. 2. Gate length that each transistor can be used under the various purposes expected by ITRS [19-20]

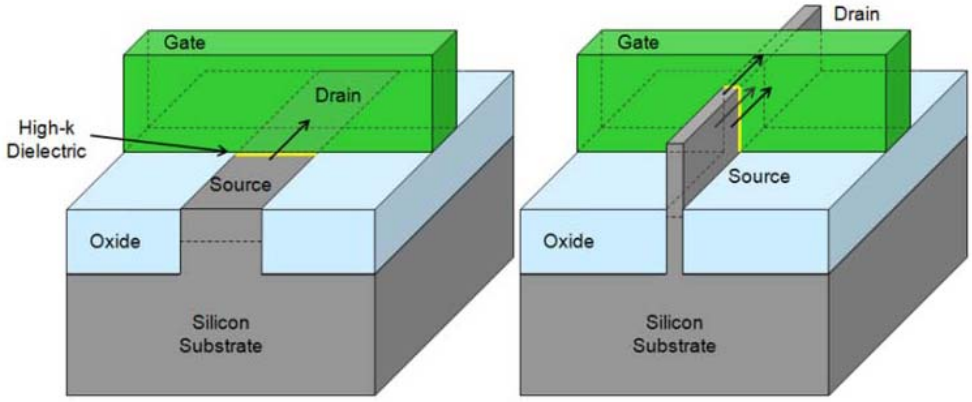


Fig. 3. Structure of conventional MOSFET and FinFET [1]

1.2 SiliconGermainum (SiGe) characteristics

The electron current density of transistor can be expressed as :

$$J_n = q\mu_n n\varepsilon \quad (1)$$

Where n is the electron density, and μ_n is the electron mobility in channel. To improve the performance of transistor, n and μ_n should increase, and high μ_n can be achieved by decreasing the effective mass.

Figure 4 shows the bandgap of various cadidtated material for channel according to lattice constatnt [26]. Circle size shows the relative electron/hole mass at each material. Since germanium (Ge) has lower hole effective mass and smaller bandgap than those of silicon (Si), Ge has higher hole mobility and density of intrinsic carrier than those of Si. In addition, since the difference of lattice constant between Ge and Si is smaller than any other candidated materials, Ge was chosen to be used as channel material with silicon in pMOSFET [27-30].

As one of the main technology for performance improvement, strain engineering has been investigated since strain effects was adopted to CMOS technology [31-35]. As shown in figure 5, holoe mobility at Si and Ge is improved by strain engineering. However, effect of strain engineering on the hole mobility is much larger at Ge than at Si. Therefore, Ge is considered as more suitable material for strain engineering technology than Si.

In recent transistor, SiGe is widely used as a channel material becase of above strong point of Ge. As shown in figure 6, CMOS inverter, that channel material is SiGe, has lower gate delay at the same operating voltage (V_{DD}) than that in Si channel transistor [36]. From above strong points as the channel material, SiGe would be the main channel material, and therefore FinFET simulated in this dissertation use SiGe as a channel material.

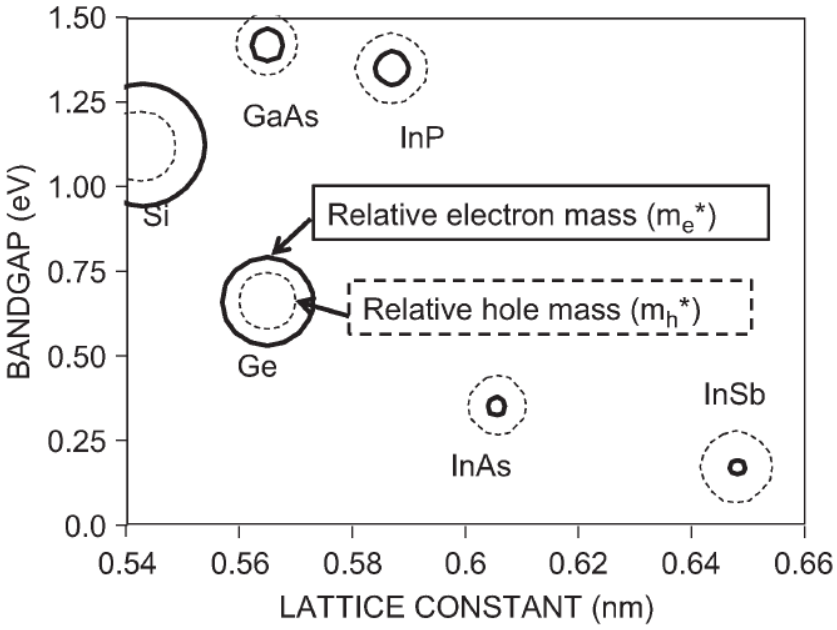


Fig. 4. Bandgap according to various materials with lattice constant [26]

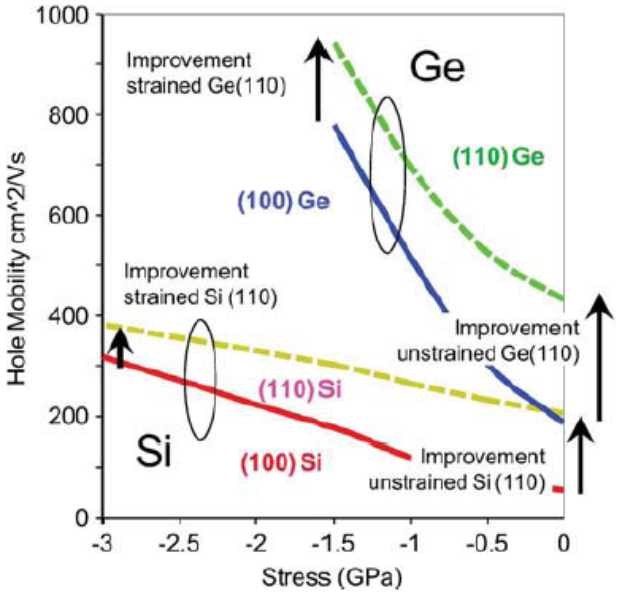


Fig. 5. Comparison of hole mobility according to stress at silicon and germanium [26]

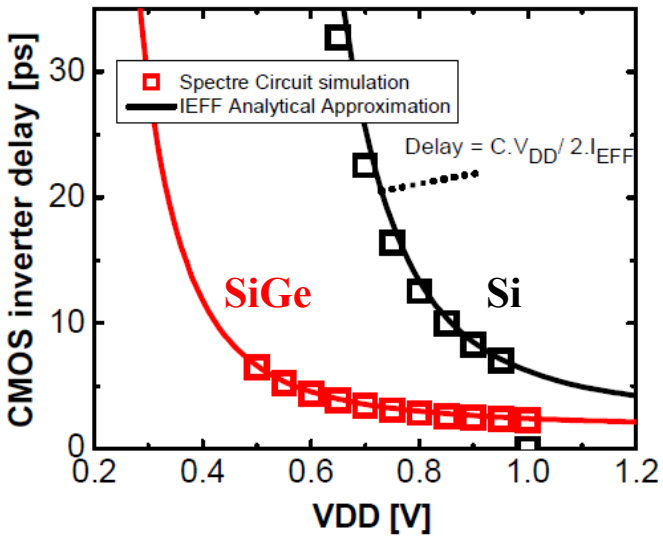


Fig. 6. Comparison of CMOS inverter delay according to V_{DD} at silicon and germanium [36]

1.3 Scope and Organization

The main subject of this paper is the analysis of Gate-Induced-Drain-Leakage current (GIDL) in $Si_{1-x}Ge_x$ FinFET. In this thesis, the Sentaurus simulator from Synopsys Co. Ltd., is used for the TCAD simulation. Device specification of $Si_{1-x}Ge_x$ FinFET is based on the ITRS 2013. In chapter 2, mechanisms of GIDL current in $Si_{1-x}Ge_x$ FinFET are analyzed by comparing that in conventional MOSFET. In chapter 3, the effect of device specification on GIDL current is investigated, and guidelines for $Si_{1-x}Ge_x$ FinFET to reduce GIDL current are provided. Finally, the paper is concluded in Chapter 4.

Chapter 2
Gate-Induced-Drain-Leakage (GIDL) current in FinFET

2.1 Introduction

Gate-Induced-Drain-Leakage (GIDL) current is one of the main leakage current in conventional MOSFET [1-4]. At off-state in transistor, it is expected that drain current decreases with decreasing gate voltage. However, as shown in Figure 1, when the negative gate bias that absolute value is larger than flat band voltage is applied in nMOSFET, it is observed that drain current at off-statet increases continuously [5].

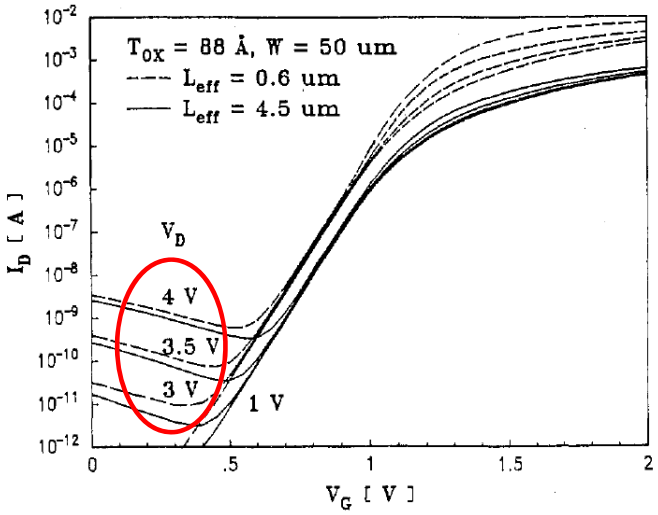


Fig. 1. Drain current according to gate voltage in nMOSFET. Drain current increases continuously even at off-state [5]

Figure 2 shows the cross section of nMOSFET when negative gate bias and positive drain bias are applied, respectively. Under above bias conditions, generation-recombination process occurs in the overlapped region between gate and high doped drain regions. It is known as the main cause of increasing drain current at off-state.

For accurate investigation of leakage current, band-diagram at the overlapped region between gate and drain regions is described in figure 3. As shown in figure, it is the mechanisms of GIDL that electrons from the valence band are tunneled out to the conduction band. There are two mechanisms of electron tunneling. One is the diect tunneling from the valence band to conduction band, which is called (1) band-to-band tunneling [1,4,6]. The other is the electron tunneling assisted by interface trap, which is called (2) trap-assisted tunneling [7-10]. Generated electrons in conduction band drained away to the drain contact while holes in valence band drained to the substrate contact. This was the process of GIDL current in nMOSFET. GIDL current is the main component of leakage current in transistor, and therefore critical factor that determines the performance in low stanby power digital circuits.

FinFET has the structure that channel region is surrounded by gate on three sides. Therefore, it has been usually considered as the future device for short channel transistor because of strong ability to control channel region. In additions, GIDL current is expected to decrease in FinFET because of strong gate controllability [11]. However, many researches have shown the GIDL current in FinFET, which is different result from what it is expected [12-14]. Recent report from figure. 4 shows that GIDL current is still a main leakage component in SOI FinFET. However, the explanation about GIDL mechanism in

FinFET still follows the conventional GIDL mechanism in MOSFET even though band-to-band tunneling generation does not occur at the interface between gate-to-drain overlap and gate regions [15]. There can be a new type of mechanisms for GIDL in FinFET. In this chapter, the main reason of leakage current in FinFET is analyzed by comparing with conventional MOSFET.

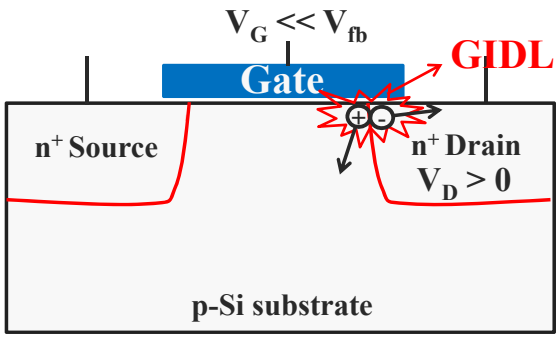


Fig. 2. Cross section of nMOSFET when negative gate bias and positive drain bias are applied, respectively [1-3]

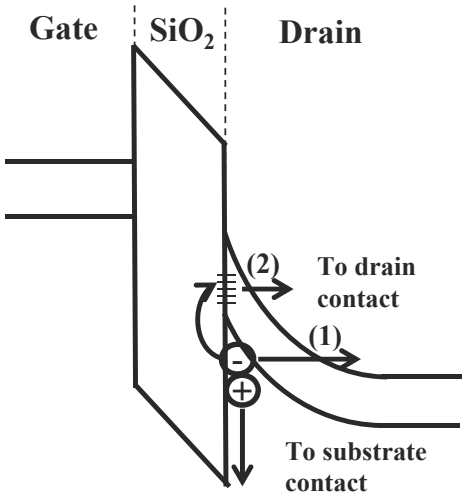


Fig. 3. Energy band diagram at the overlapped region between gate and drain regions [1-10]

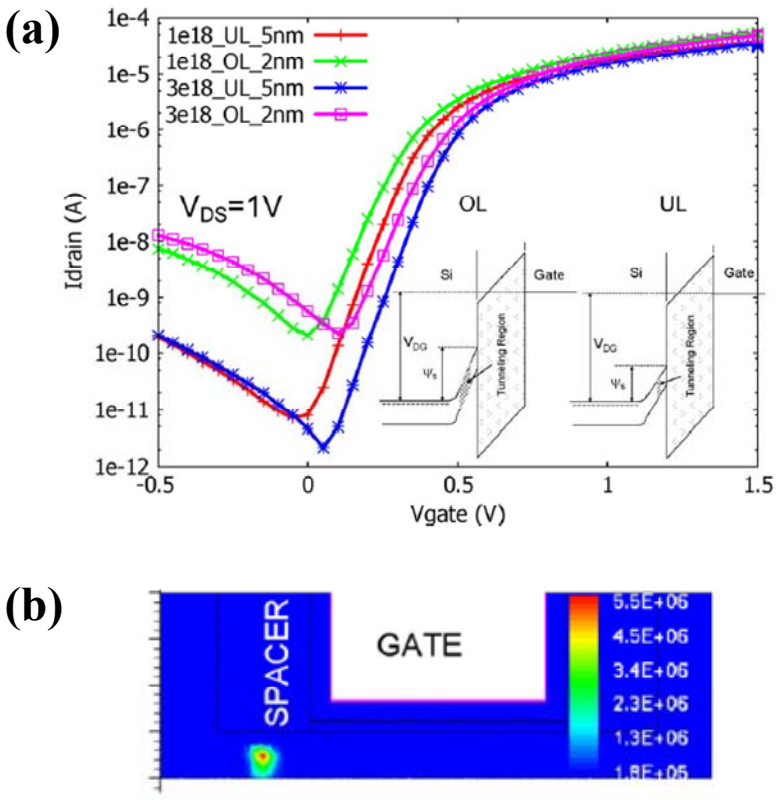


Fig. 4. (a) I_D-V_{GS} curves for $1x10^{18}$ and $3x10^{18}$ cm^{-3} body-doped NFET devices. (b) Band-to-band generation current at half fin height for the case shown in (a) [15]

2.2 Modeling of GIDL current

The main mechanims of GIDL current in the conventional MOSFET are band-to-band tunneling and trap-assisted tunneling. These tunneling mechanis are the same as the generation-recombination process in that electrons are tunneled out to the conduction band from the valence band. Generation-recombination process is modeled by Shockley Read Hall (SRH) process, which describes the exchange process of carriers between the conduction band and valence band [16,17]. It is can be expressed as :

$$R_{SRH} = \frac{np - n_i^2}{\tau_p\left(n + n_i \cdot exp\left(\frac{E_T - E_i}{kT}\right)\right) + \tau_n\left(p + n_i \cdot exp\left(\frac{E_T - E_i}{kT}\right)\right)} \quad (1)$$

where n and p are the density of electron and hole. E_T is a energy level of trap. T_n and τ_p are the life time of electron and hole, respectively.

As a result, revised SRH model will be used by adapting band-to-band tunneling and trap-assisted tunneling models in this dissertation. Total recombination process is a superposition of band-to-band tunneling and trap-assisted tunneling processes. Revised SRH model can be expressed as [18]:

$$R_{SRH.Rev} = R_{trap} + R_{bbt} \quad (2)$$

that also can be expressed as the conventioanl SRH model under the low electric field condition. R_{trap} describes the electron tunneling by interface/bulk traps and includes the conventional SRH recombination mechanism. R_{bbt} expresses band-to-band tunneling process. In this sub-chapter, models for band-to-band tunneling and trap-assisted tunneling process will be explained.

2.2.1 Hurkx trap assisted tunneling model

Trap assisted tunneling indicates the tunneling process that an electron from valence band are captured at the trap and detrapped to the conduction band. Traps contributing trap assisted tunneling process would be located at the interface or at the center of band gap. Its process is similar to the generation recombination process that carriers are thermally generated by recombination-generation (R-G) centers. Since the net recombination rate via traps is determined by the density of carriers and the probability of carrier emission from a trap. Based on R-G process, hurkx trap assisted tunneling model modifies the lifetimes and capture cross sections , which become functions of the trap assisted tunneling factor Γ_{tat} [18,19].

$$\tau = \tau_0 / \left(1 + \Gamma_{tat}\right) \quad , \quad \sigma = \sigma_0 \left(1 + \Gamma_{tat}\right) \tag{3}$$

As a result, Shockley Read Hall (SRH) expression is revised as [18,19]:

$$R_{trap} = \frac{np - n_i^2}{\frac{\tau_p}{1+\Gamma_p}\left(n + n_i \cdot exp\left(\frac{E_T - E_i}{kT}\right)\right) + \frac{\tau_n}{1+\Gamma_n}\left(p + n_i \cdot exp\left(\frac{E_T - E_i}{kT}\right)\right)} \tag{4}$$

Hurkx trap-assisted tunneling model is uesed by modifying SRH model in GIDL simulation.

2.2.2 Hurkx band-to-band tunneling model

Band-to-band tunneling basically describe the direct transition of the electron from the valence band to conduction band. However, Silicon including SiGe is indirect semiconductor that carrier transitions including electron-phonon interaction occurs. Therefore, various models for band-to-band tunneling have been studied, and hurkx model is the well-known model for indirect semiconductor. Theory of hurkx band-to-band tunneling model is based on the work of Keldysh and Kane [19-21]. Tunneling carriers are modeled by an additional generation-recombination process. Tunneling contribution R_{bbt} is expressed as [18]:

$$R_{bbt} = A \cdot D \cdot \left(\frac{F}{1V/cm} \right)^{P} exp\left(\frac{B \cdot E_g(T)^{3/2}}{E_g(300K)^{3/2} F} \right) \quad (5)$$

The coefficients A ($cm^{-3}s^{-1}$) and B (V/cm) are considered as the fitting parameters. F is applied electric field, and P shows the effects of electric field on generation-recombination process which is set to be 2.5. To analyze the GIDL characteristics, hurkx band-to-band tunneling model is used in this dissertation.

2.3 Comparison of GIDL between MOSFET and FinFET

2.3.1 Simulation setup

Figure 5 (a) and (b) show the structure of SiGe pMOSFET and pFinFET for the investigation of GIDL characteristics [22]. Sentaurus simulator from Synopsys Co. Ltd., is used for the TCAD simulation. Both FETs have the same channel length that is long enough to suppress the short channel effects (SCE) for accurate comparison of only GIDL characteristics between pMOSFET and pFinFET. Width in pMOSFET, that is critical factor to determines the current, is equivalent to the circumference of the fin in pFinFET. Both FET also have the same junction depth. In both FETs, channel mateiral is SiGe, and Ge fractioin of channel region is different from that of drain region so that strain engineering should be performed. As a result of those process, there are more traps in SiGe MOSFET than Si MOSFET. Black box (A) indicates the interface region between gate dielectric and channel regions where interface traps are assumed to be located. Black box (B) indicates the bulk region under the spacer between channel and drain regions. There are bulk traps induced by the lattice mismatch of $Si_{1-x}Ge_x$ material between channel and drain regions [23]. Substrate and source/drain regions are doped by arsenic of $1x10^{15}$ cm^{-3} and boron of $1x10^{20}$ cm^{-3}, respectively. Hurkx band-to-band and trap-assisted tunneling models are considered for the GIDL current.

Figure 6 shows the trap profile at the interface between the gate dielectric and channel

that is indicated by black box (A) in figure 5. Profile of interface traps consists of dono-like-trap and acceptor-like trap, and peak density is assumed to be $5x10^{12}$ $eV^{-1}cm^{-2}$. Peak level is assumed to be 1 eV away from each band edge. Black box (B) also has the same trap profile as that of black box (A) except from the peack density that is assumed to be $5x10^{19}$ $eV^{-1}cm^{-3}$.

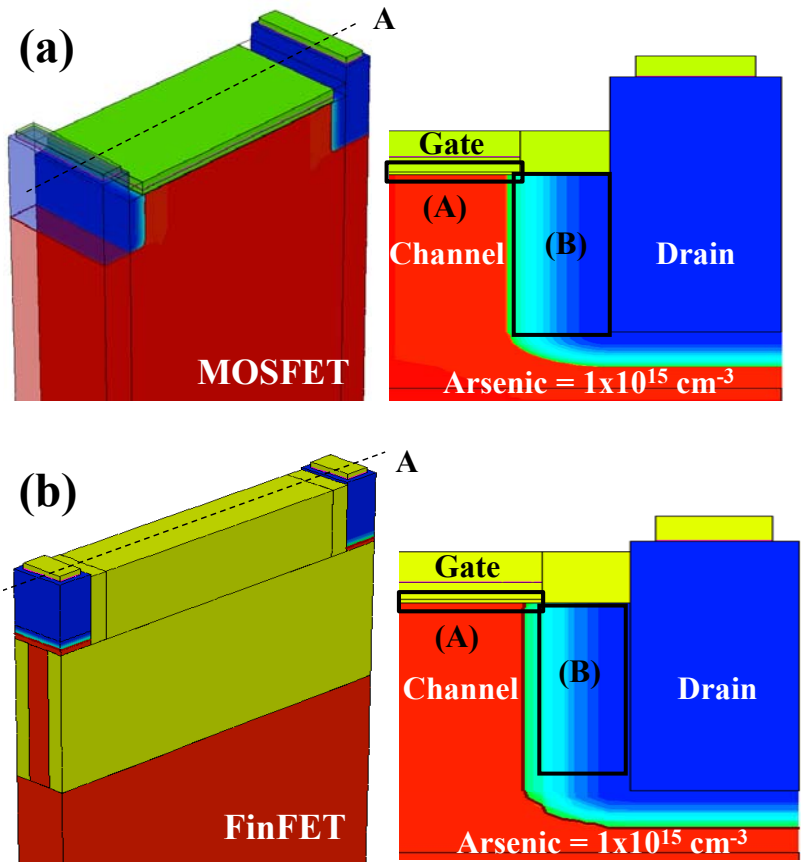


Fig. 5. Structure of SiGe (a) pMOSFET and (b) pFinFET

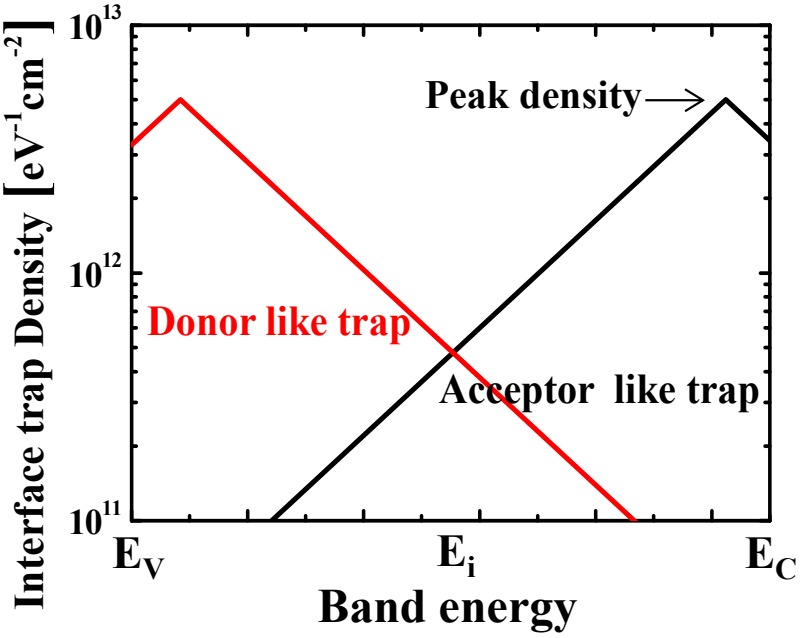


Fig. 6. Profile of interface trap at the interface between gate dielectric and channel (Box (A)). Peak density is assumed to be $5x10^{12}$ $eV^{-1}cm^{-2}$. Peak level is assumed to be 1 eV away from each band edge

2.3.2 Band-to-band tunneling mechanism in FinFET

Figure 7 shows the drain current induced by only band-to-band tunnleing (BBT) component in pMOSFET and pFinFET. BBT component can be extracted by subtracting the current without tunneling models from the current with only BBT model. Since FinFET has strong gate controllability on channel region, it is not expected that GIDL current by BBT mechanism occurs. However, as shown in figure 7, it is observed that GIDL current by BBT mechanism in FinFET still exsist and has the almost same value of current as that of MOSFET. The conventional BBT generation in MOSFET occurs at the interface between gate dielectric and lightly-doped-drain (LDD) regions. In FinFET, a new type of BBT generation would be exsist.

Figure 8 (a) and (b) show the distribution of BBT generation at the gate edge in the cross section of SiGe pMOSFET and pFinFET. It shows the apparent difference of BBT mechanism in MOSFET and FinFET. White box indicates the gate-to-drain overlap region. In conventioanl MOSFET, BBT generation occurs at the gate-to-drain overlap region and near the interface region of the gate edge as shown in figure 8 (a). However, BBT generation rarely occurs at the gate-to-drain region in FinFET while a large amount of BBT generation occurs under the spacer region and internal region of Fin. As a result, BBT generation that occurs under the spacer region is the one of mechanisms of GIDL current in FinFET. For accurate analysis of BBT mechanism in FinFET, energy band diagram of the case of FinFET would be described with that of MOSFET.

Figure 9 (a) and (b) show the schematics of energy band diagram that describes the

BBT generation in MOSFET and FinFET. Figure 9 (a) shows the energy band diagram for the BBT generation at the interface of gate-to-drain overlap region. In MOSFET, since the ability of gate to control channel potential is weak, electric potential at the edge of channel region has a tendency to follow the potential of drain region. Therefore, as the difference of applied voltage between gate and drain regions increases, the surface potential at the interface between gate and gate-to-drain region of channel also increases. As a result, as band bending at the interface occurs, electrons in the valence band are directly tunneled to the conduction band, which is BBT mechanism contributing GIDL current in conventional MOSFET.

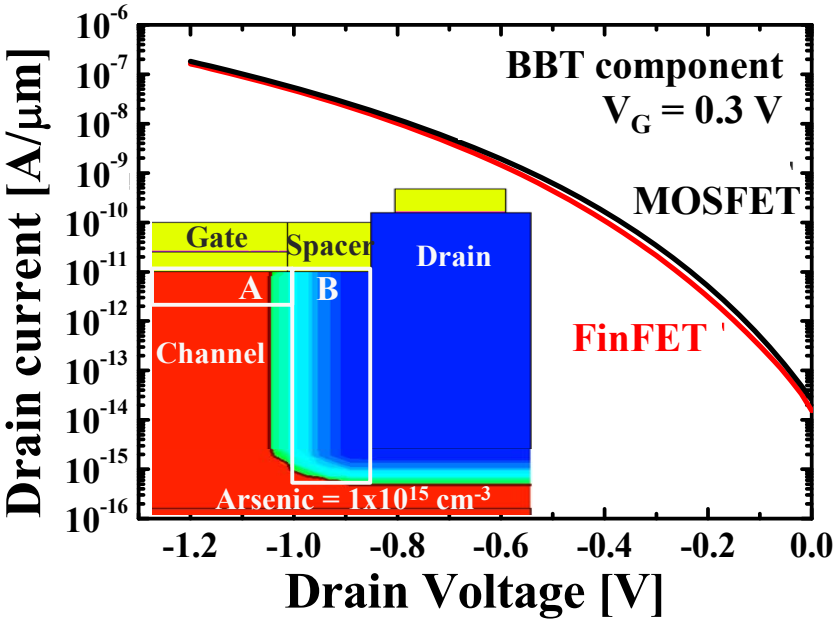


Fig. 7. Comparison of drain current by only band-to-band tunneling in SiGe pMOSFET and pFinFET. White box A at the cross section of FinFET in inset is the place where the conventional BBT generation occurs.

However, in case of FinFET, surface potential is smaller than that of the MOSFET because of strong controllability of gate. Instead, the electric potential difference between gate-to-drain overlap region and drain regions becomes larger according to the difference of voltage applied to gate and drain. Therefore, BBT generation as shown in figure 9 (b) occurs dominantly under ther spacer region.

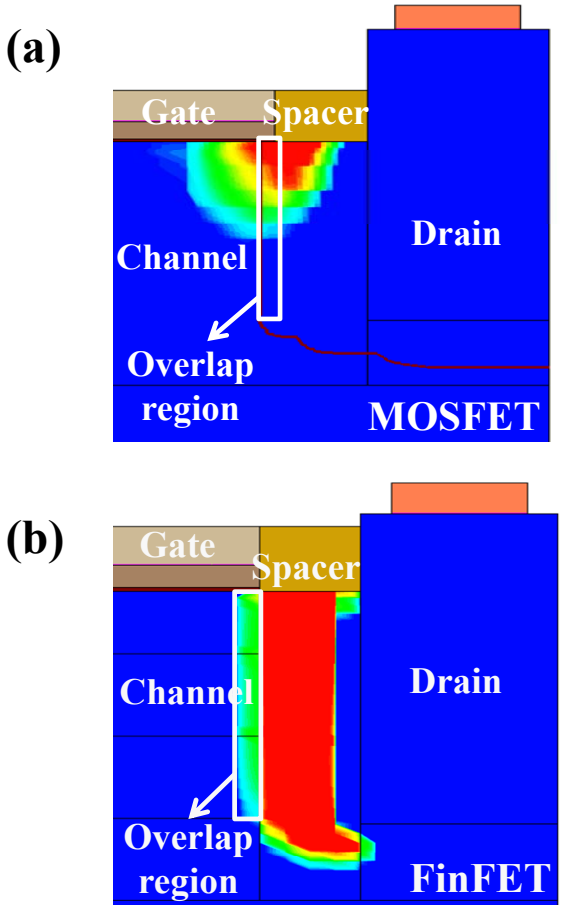


Fig. 8. Distribution of band-to-band tunneling generation in SiGe (a) pMOSFET and (b) pFinFET

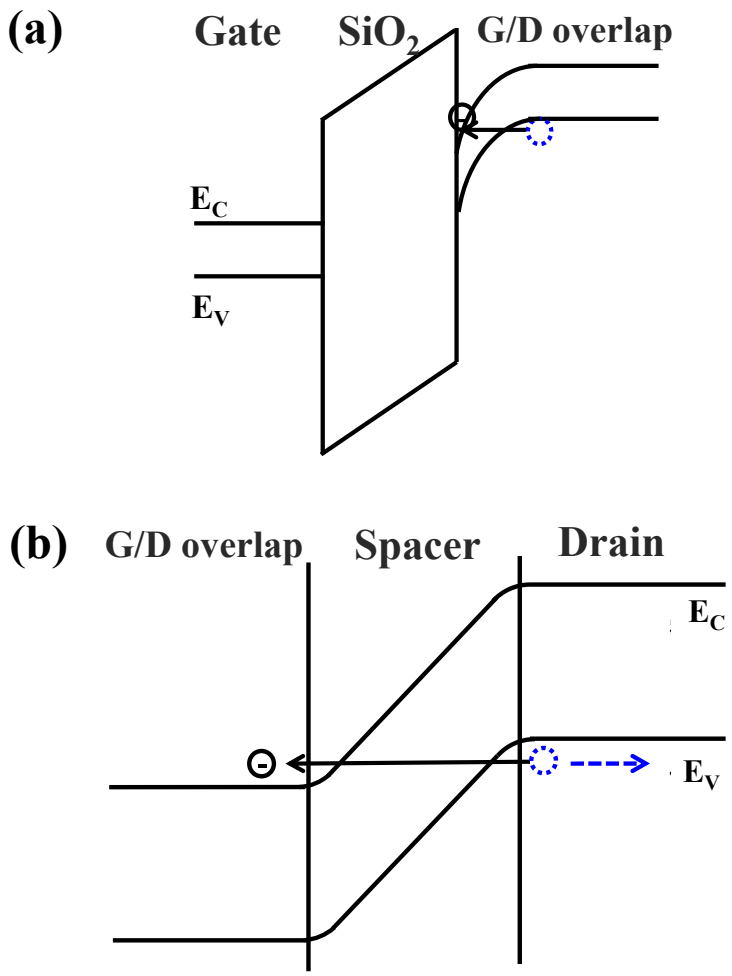


Fig. 9. Schematic of energy band diagram describing band-to-band tunneling generation in SiGe (a) pMOSFET and (b) pFinFET

2.3.3 Trap-assisted tunneling mechanism in FinFET

Figure 10 (a) and (b) show the schematic of energy band diagram under the condition that trap-assisted tunneling (TAT) occurs. Figure 10 (a) shows the mechanism of TAT occurred in conventional MOSFET. TAT is the one of the tunneling mechanisms that electrons in valence band are transported to the conduction band by the interface traps at the low electric field before BBT generation occurs. Recently, for the improvement of the mobility in transistors, strain engineering is performd by developing SiGe in source and drain regions. In transistor that uses SiGe source/drain to apply a stress effect to channel region, bulk traps between channel and drain regions are generated because of the lattice mismatch. Figure 10 (b) shows the TAT generation by bulk traps in SiGe source/drain FET. In MOSFET and FinFET, the dominant TAT mechanism is different by the structural difference. Figure 10 (a) is the dominant TAT mechanism for MOSFET while the other is for FinFET.

Figure 11 (a) and (b) show the extracted drain current by trap-assisted tunneling (TAT) through interface and bulk traps in SiGe pMOSFET and pFinFET. In case of SiGe pMOSFET, TAT current by interface traps is larger than that by bulk traps. As mentioned in previous sub-chapter, since the band bending at the interface is large, TAT generation by interface traps is dominant. In case of SiGe pFinFET, TAT current by bulk traps is larger than that by interface traps. This is because strong gate controllability induce a small electric field at the interface between gate dielectric and gate-to-drain regions is small while electric field induced by the electric potential difference between channel and

drain regions is large enough to generate TAT current.

Figure. 12 shows the energy band diagram of both FETs plotted along the dotted line in the structure of an inset. Since the slope of energy band means the electric field, it is confirmed that electric field at the interface in MOSFET is much larger than that in FinFET. Therefore, TAT by interface traps in MOSFET is larger than that in FinFET. However, since TAT by bulk trap in finFET is almost equal to TAT in MOSFET, TAT in FinFET is one of the mechanisms of GIDL current under the low electric field conditon.

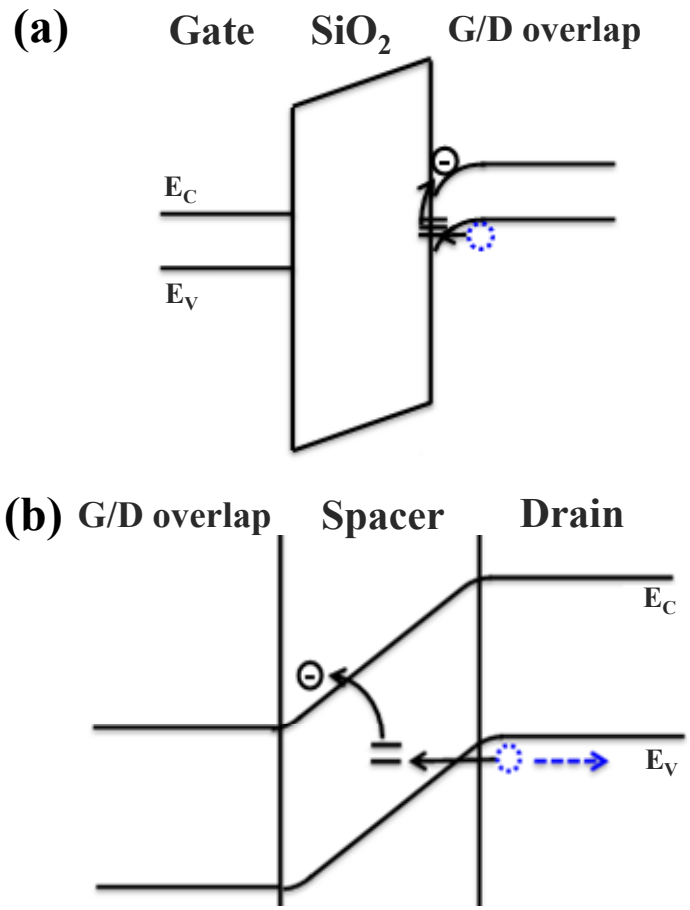


Fig. 10. Schematic of energy band diagram describing trap-assisted tunneling generation in SiGe (a) pMOSFET and (b) pFinFET [17]

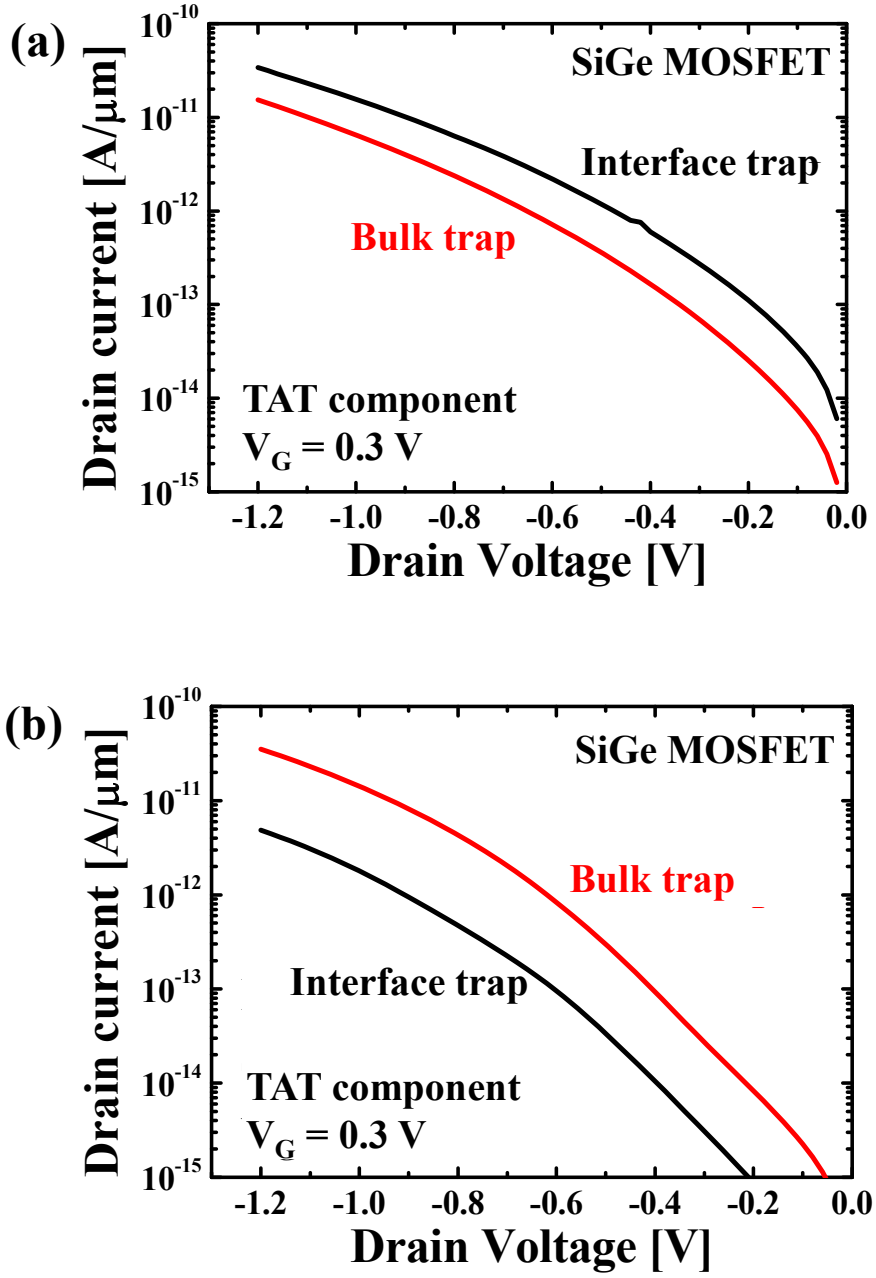


Fig. 11. Extracted drain current by trap-assisted tunneling through interface and bulk traps in SiGe (a) pMOSFET and (b) pFinFET

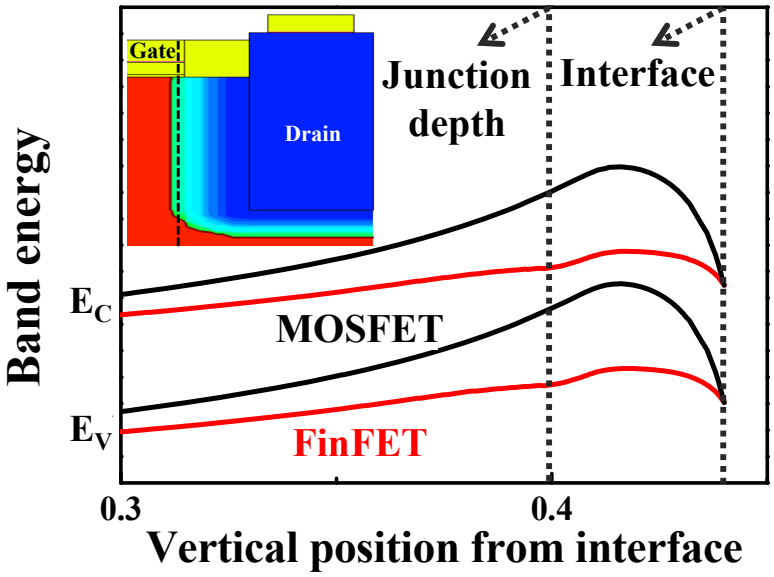


Fig. 12. Schematic of energy band diagram plotted along the dotted line in the structure of inset. PMOSFET has larger electric field at the interface than pFinFET [17]

2.3.4 Conclusion

In this chapter, GIDL mechanism in SiGe pFinFET is analyzed by comparing with thatin SiGe pMOSFET. In case of FinFET, GIDL mechanism is different from the conventional GILD mechanism that occurred at the interface between gate dielectric and gate-to-drain overlap regions because structural characteristics of FinFET makes the gate contriollability on channel strong. GIDL mechanism in SiGe pFinFET consists of band-to-band tuneling and trap-assisted tunneling by bulk trap between channel and drain regions. At strong electric field, band-to-band tunneling occurs dominantly by laterally apllied electric field. Therefore, to reduce the GIDL current in SiGe pFinFET, it needs to reduce the lateral electric field applied between channel and drain regions.

2.4 Summary

Conventional GIDL mechanism consists of the band-to-band tunneling and trap-assisted tunneling at the interface between gate dielectric and gate-to-drain regions. In FinFET, GIDL current was not expected because FinFET has a strong ability to control channel region. However, GIDL current still exsists and confirmed by TCAD simulaton. Hurkx model that modifies shockley-read-hall model is used to adapt the GIDL mechanism that consists of band-to-band tunneling and trap-assisted tunneling in TCAD simulator. Dominant mechanism of GIDL current in SiGe pFinFET is band-to-band tunneling current that occurred by strong electric field applied between chanel and drain regions. Since band-to-band tunneling generation is affected by lateral electric field, detailed research is needed to maintain low electric field.

Chapter 3
Effects of device specifications on GIDL

3.1. Introduction

In the previous chapter, main mechanism of GIDL in FinFET was analyzed. Although band-to-band tunneling and trap-assisted-tunneling currents are still dominant mechanism of GIDL current, they are different mechanisms from the conventional GIDL mechanism of MOSFET in that GIDL in FinFET occurs under the spacer. Since GIDL in FinFET occurs by a strong electric field or tunneling probability at the junction between channel and drain regions, it would be controlled by device specification such as fin shape, junction depth, doping profile and Ge fraction in channel and drain region. In this chapter, GIDL characteristics were analyzed according to device specifications and the guideline was presented to determine desirable device specfication.

3.2. Effects of germanium fraction in $Si_{1-x}Ge_x$ pFinFET on GIDL

Since mobility of germanium (Ge) is higher than that of silicon (Si), it would be desirable to use Ge as a channel material rather than Si in new type transistor such as a FinFET. However, Ge fraction in $Si_{1-x}Ge_x$ changes band-gap and has a great effect on leakage current including band-to-band tunneling (BBT) and sub-threshold leakage current [1-3]. In addition, since a short channel device induces a high electric field between channel and drain region, leakage current becomes larger with decreasing devise size. Therefore, effects of Ge fraction on leakage current should be analyzed thoroughly in $Si_{1-x}Ge_x$ pFinFET.

In this chapter, effects of Ge fraction in $Si_{1-x}Ge_x$ pFinFET on GIDL characteristics are analyzed. First, distribution of Ge fraction in channel and drain region is assumed to be uniform and proportion of leakage components is investigated according to Ge fraction. Second, non-uniform distribution of Ge fraction in channel region is assumed considering actual manufactured $Si_{1-x}Ge_x$ FinFET and desirable distribution of Ge fraction is presented.

3.2.1 Uniform germanium fraction

Figure 1 shows the off-current characteristics according to Ge fraction of $Si_{1-x}Ge_x$ (x=0.2, 0.4, 0.6 and 0.8) in channel region. Ge fraction is assumed to be uniformly distributed in whole channel region of fin. Threshold voltage is set to be the same value for accurate comparison of off-current. It is observed that off current increases as Ge fraction in channel region increases. For accurate analysis, off-current is divided into two main components.

Figure 2 shows the main components divided from off-current and the amount of current at the lowest level from Fig. 1 according to Ge fraction. Right axis is the amount of drain current and Left axis shows proportion of each component that consists of drain current at the same time. First, off-current at the lowest level increases with increasing Ge fraction because the amount of band-to-band tunneling and sub-threshold leakage components increases. Since band-gap of SiGe decreases as Ge fraction increases, it increases the probability of electron tunneling from valence band to conduction band. In addition, sub-threshold leakage current also increases in small band-gap material because of increasing density of intrinsic carriers in conduction band. However, increasing amounts of two components are different according to the range of Ge fraction. From 20 % to 60 % of Ge fraction, the increasing amount of band-to-band tunneling components is larger than that of sub-threshold leakage component, and band-to-band tunneling becomes dominant mechanism above Ge fraction of 40 %. Although proportion of sub-threshold leakage components increases over Ge fraction of 60 %, it is obvious

that bnad-to-band tunneling mechanism is dominant mechanism of off-current in SiGe FinFET which has Ge fraction of 40 % and over.

Figure 3 shows the off-state characteristics according to Ge fraction of $Si_{1-x}Ge_x$ (x=0.2, 0.4, 0.6 and 0.8) in drain region. In drain region, Ge material is also used to apply the compressive stress to the channel region, which increases the hole mobility in p-type SiGe channel. Although its effects on off-current is smaller than that of Ge fraction in channel region, off-current decreases with increasing Ge fraction, which has the reverse effect to what Ge fraction in channel region has.

Figure 4 shows the energy band diagram between channel and drain region according to Ge fraction (0.2 and 0.8) in drain region. Since drain voltage is not applied, intrinsic internal electric field is determined from the slope of energy band under the spacer region where band-to-band tunneling occurs. In case of Ge fraction of 20 % in drain region, since it has larger average electric field under the spacer region than that of 80 %, it has a better condition for band-to-band tunneling generation to occur.

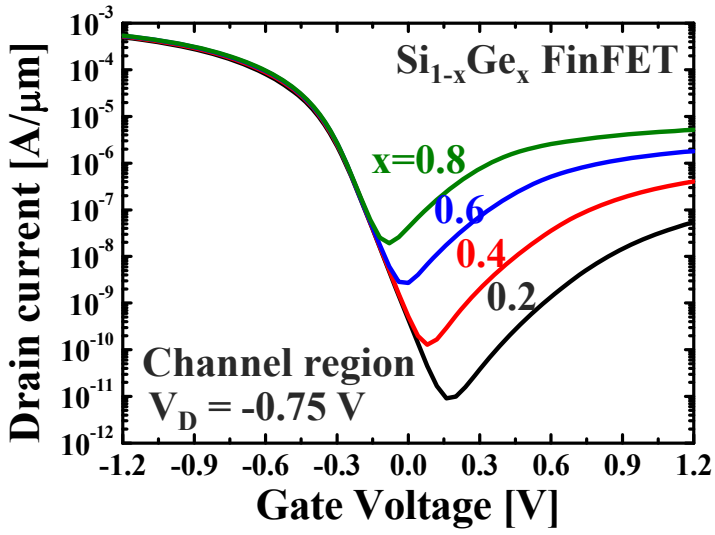


Fig. 1. Off-current characteristics according to uniformly distributed Ge fraction (0.2, 0.4, 0.6 and 0.8) in channel region

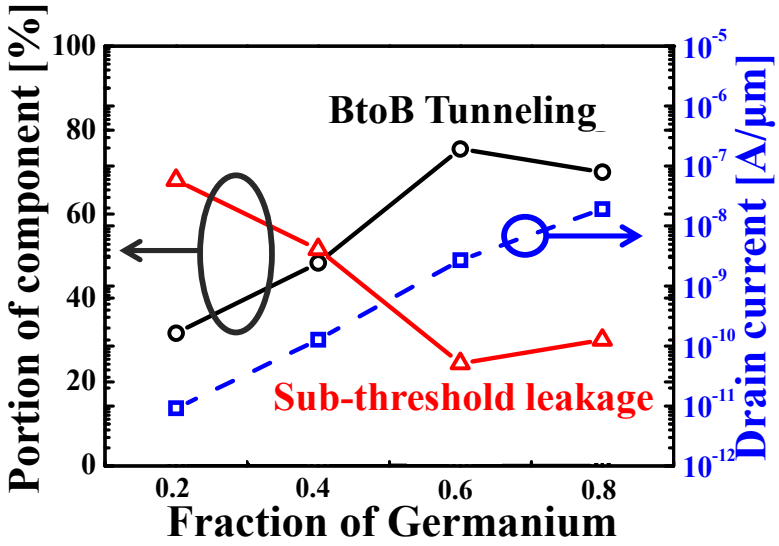


Fig. 2. Proportion of main components (band-to-band tunneling and sub-threshold leakage current) in leakage current and off-current at the lowest level according to Ge fraction

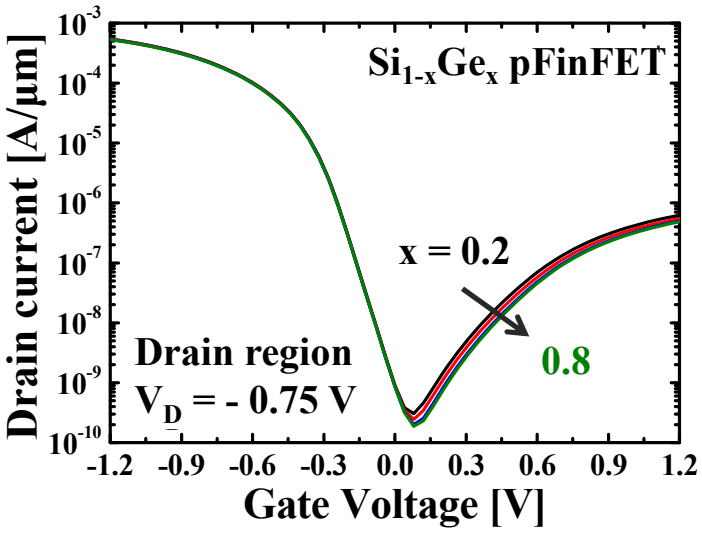


Fig. 3. Off-current characteristics according to uniformly distributed germanium fraction (0.2, 0.4, 0.6 and 0.8) in drain region

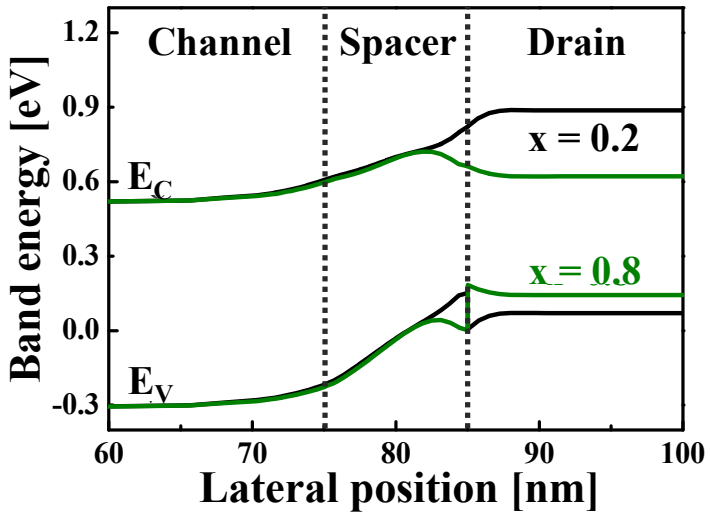


Fig. 4. Band diagram between channel and drain region according to Ge fraction (0.2 and 0.8) in drain region

3.2.2 Non-uniform internal Ge fraction

Table 1 shows the conditions of non-uniformly distributed Ge fraction in fin region [4]. Fin is divided into 4 regions to describe the actual distribution of Ge fraction. Case ‘a’ is the condition that the maximum value of Ge fraction is located at the top region of the fin while case ‘b’ is the reverse case of case ‘a’. Maximum value of Ge fraction is assumed to be 0.7 and 0.5, which decrease by 0.1 between each divided region.

Figure 5 shows the off-current characteristics according to the conditions in Table 1. It is observed that GIDL current at Case ‘a1’ is larger than that at Case ‘b1’. In addition, GIDL current becomes larger as the maximum value of Ge fraction increases by comparing Case ‘a1’ with Case ‘a2’.

Figure 6 is the distribution of band-to-band tunneling generation in internal fin at each condition. It is known that band-to-band tunneling current increase with the increasing Ge fraction of SiGe because of band gap narrowing. Therefore, band-to-band tunneling of Case ‘a1’ occurs more than that of Case ‘a2’ in whole fin region. In case of ‘b1’, since the maximum value of Ge fraction is located at the bottom of the fin, distribution of band-to-band generation is wider than that of Case ‘a1’. However, since the electric field applied between channel and drain regions at the bottom of the fin is smaller than that at the top of the fin, the total amount of band-to-band tunneling current of Case ‘a1’ is larger than that of Case ‘b1’. For accurate comparison, I_D-V_D curve is also investigated.

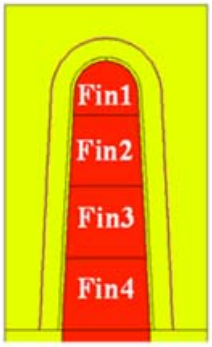
As shown in Fig. 7, the components of off-current are analyzed from I_D-V_D curve of Case ‘a2’. The component independent from the drain voltage is sub-threshold leakage

current, which is main mechanism of off-current until drain voltage is about -0.8 V. As drain voltage decrease over -0.8 V, band-to-band tunneling current becomes the main mechanism of off-current because of a sufficient electric field applied between channel and drain regions. It is assumed that trap-assisted tunneling does not occur because it is much smaller than other mechanisms.

Figure 8 shows I_D-V_D characteristics in Case ‘a2’ and ‘b2’ according to various gate bias conditions (V_G = 0, 0.3 and 0.75 V). Considering previous results from Fig. 7 and the drain current at V_G = 0.75 V in Fig. 8, it is confirmed that Case ‘a2’ has larger band-to-band tunneling component than Case ‘b2’, and the reason is well described in Fig. 6. It is also observed that Case ‘a2’ has larger sub-threshold current than Case ‘b2’ from the result at V_G = 0 V.

Figure 9 shows the distribution of hole current in channel region at off-state (V_G = 0 V) in Case ‘a2’ and ‘b2’. It is observed that the hole current density is high at the top region of fin at Case ‘a2’, and Case ‘b2’ has a reverse tendency. Since the density of intrinsic carrier in SiGe becomes higher as the Ge fraction increases, Case ‘a2’ has higher density of intrinsic carrier at the top region of fin than that at the bottom region of fin. In addition, since lateral electric field at the top region is larger than that at the bottom region, Case ‘a2’ has larger sub-threshold leakage current than Case ‘b2’.

As a result, to decrease the band-to-band tunneling current and sub-threshold leakage current, Ge fraction at the top region of fin in SiGe FinFET should be lower than that at the bottom region of fin.



Case	a1	b1	a2	b2
Fin1	0.7	0.4	0.5	0.2
Fin2	0.6	0.5	0.4	0.3
Fin3	0.5	0.6	0.3	0.4
Fin4	0.4	0.7	0.2	0.5

Table. 1. Ge fraction conditions in internal fin

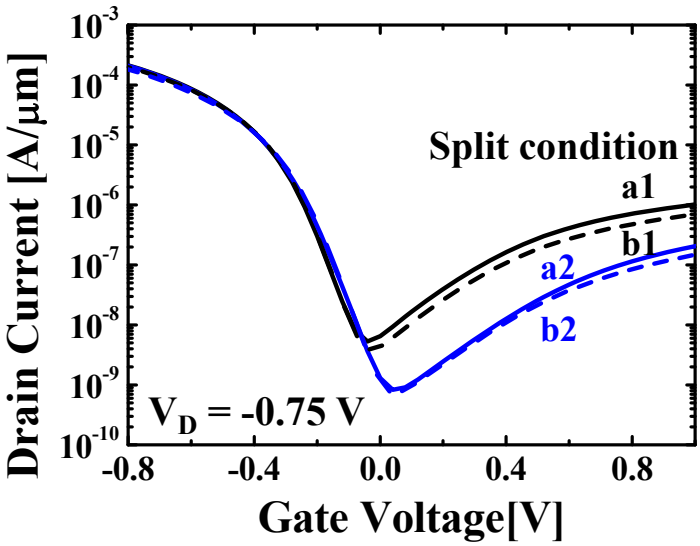


Fig. 5. Off-current characteristics according to non-uniformly distributed germanium fraction in channel region

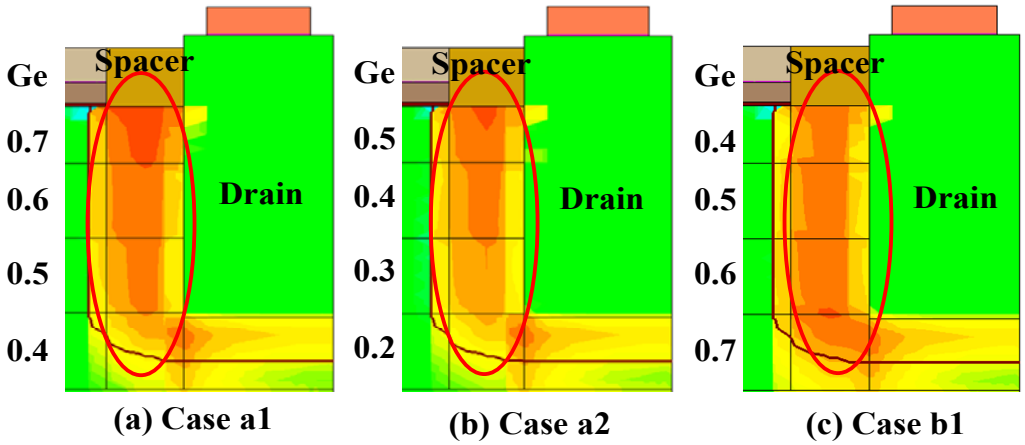


Fig. 6. Distribution of band-to-band tunneling generation according to Ge fraction conditions

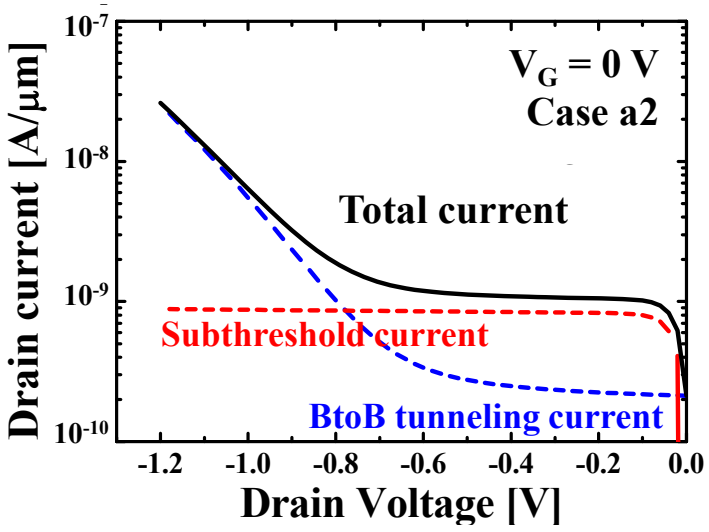


Fig. 7. Main components (band-to-band tunneling and sub-threshold current) at off-states in Case a2

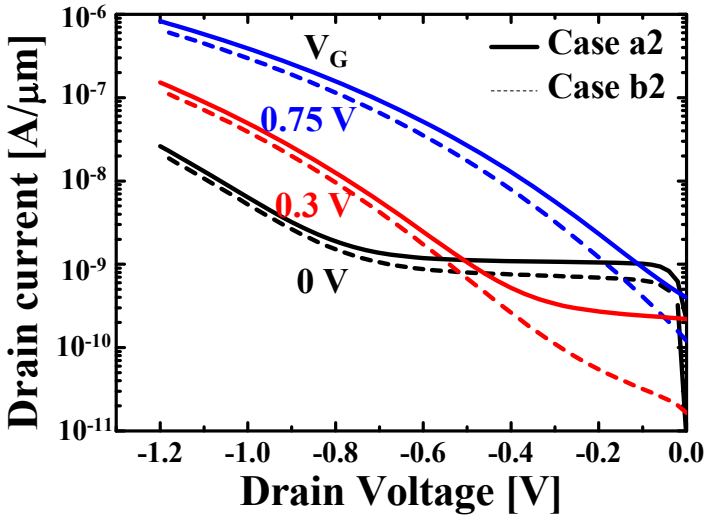


Fig. 8. I_D-V_D characteristics between Case a2 and b2 according to various gate bias

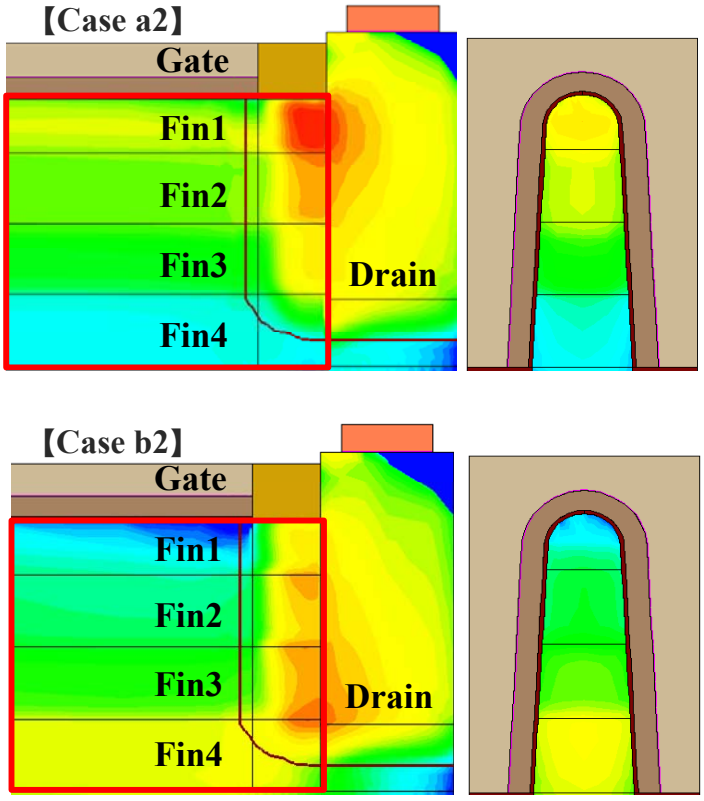


Fig. 9. Distribution of hole current in channel region at case a2 and b2

3.2.3 Conclusion

In this sub-chapter, effects of Ge fraction of SiGe pFinFET on GIDL current are investigated. Since higher Ge fraction in channel region and lower Ge fraction in drain region increases band-to-band tunneling generation under the spacer region, it is desirable to manufacture pFinFET which has lower Ge fraction in channel and higher Ge fraction in drain as long as Ge fraction guarantees the on-current. In real manufactured FinFET, Ge fraction of SiGe would be non-uniformly distributed in fin region. Under this condition, it is suggested that Ge fraction at the top region of fin in SiGe FinFET should be lower than that at the bottom region of fin.

3.3. Effects of manufacturing process conditions on GIDL

Manufacturing process conditions determine the structure of FinFET, so that it has great effects on the performance of the device. The regions of FinFET which have a direct effect on the performance are the channel and source/drain regions. The channel region is determined by the fin shape in FinFET. It determines the electric field and carrier density at the edge of the fin and has various effects on the characteristics of the device. Source/drain contacts also directly determines the performance especially in short channel device. In this sub-chapter, effects of fin shape and source/drain contacts on GIDL current are investigated.

3.3.1 Effects of corner process

Fin shape is directly determined by degree of corner rounding of fin. It affects the vertical electric field at the top of the fin and the hot carrier effect (HCI) or positive/negative bias temperature instability (NBTI/PBTI).

Figure 10 shows the contour of the fin and the definitions of manufacturing process parameters. Width of the fin is set to be measured at the middle of the fin, and the degree of corner rounding means an edge of the top region of fin.

Figure 11 shows the effect of corner rounding on the off-current. It is also observed that the degree of corner rounding does not affect the GIDL characteristics. It is suggested that the degree of corner rounding should be analyzed in terms of HCI or NBTI/PBTI.

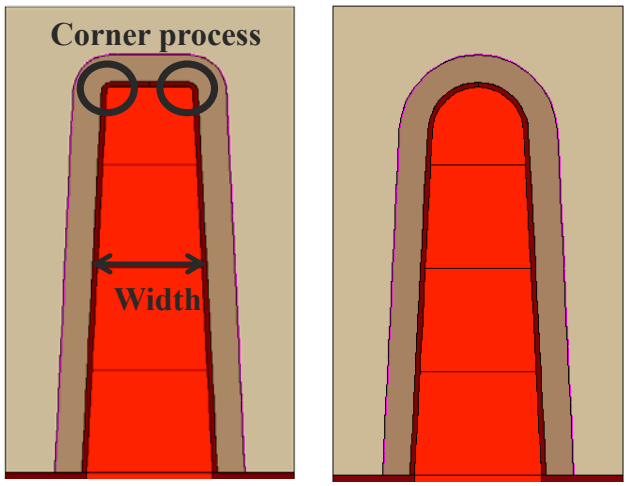


Fig. 10. Definition of manufacturing process parameters in internal fin

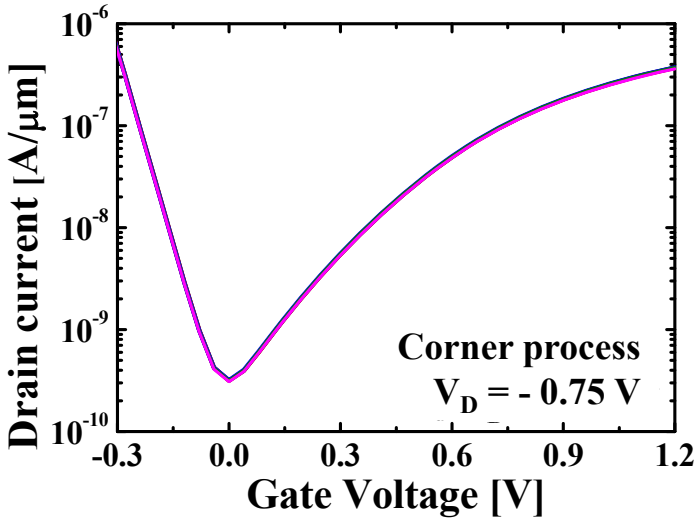


Fig. 11. Off-current characteristics according corner process

3.3.2 Effects of fin width

In addition to corner process, fin width is the one of the important parameters determining the performance in FinFET because as the fin width decreases, it induce the volume inversion that electron or hole inversion occurs at the center of the internal fin. In addition, conduction band splits into sub-bands, so that threshold voltage increases [5-7]. In this sub-chapter, effects of fin width on GIDL current are analyzed.

Figure 12 shows the off-current characteristics according to fin width. It is concluded that fin width does not affect the GIDL characteristics. Study on the fin width of the FinFET should focus on mobility and carrier density.

Figure 13 shows the I_D-V_G curve according to quantum effect model in FinFET which fin width is 3 nm. It is observed that the absolute value of threshold voltage (V_g) of drain current with quantum effect model increases by 0.035 V. As the fin width decreases sufficiently, quantum effect occurs, so that the conduction band of channel region splits into sub-bands. Therefore, increasing gate voltage is needed to reach an inversion carrier concentration. In addition, localized sub-bands cause the effective band-gap to increase, so that GIDL current with quantum effect decreases. As a result, GIDL current can be decrease with quantum effect.

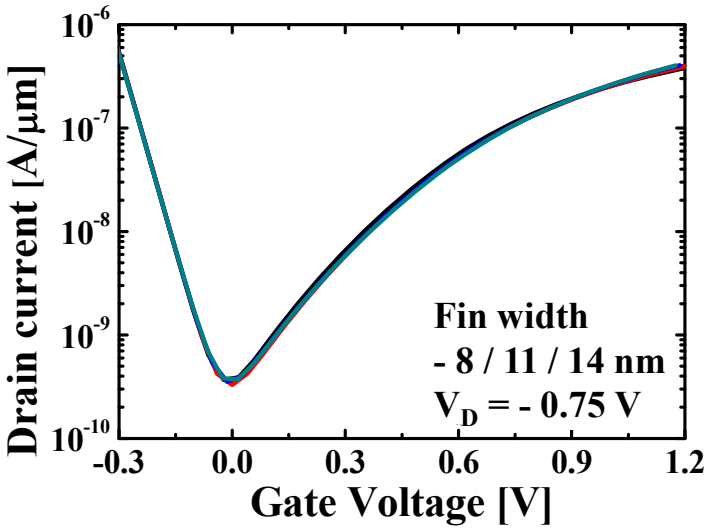


Fig. 12. Off-current characteristics according fin width

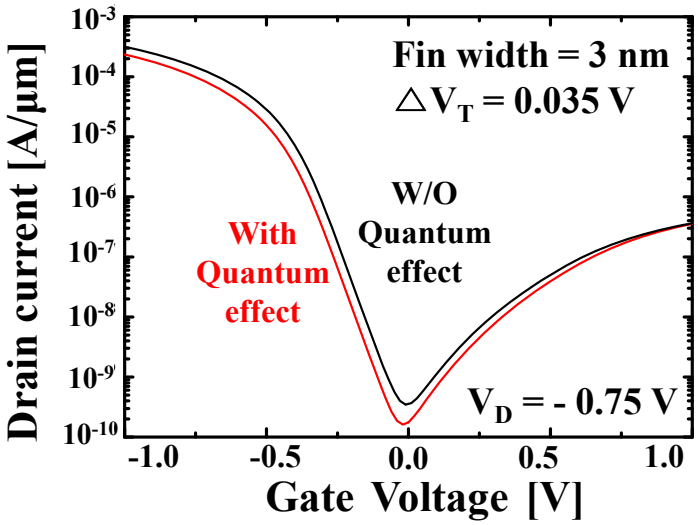


Fig. 13. I_D-V_G curve comparison according to quantum effect model

3.3.3 Effects of source/drain contacts

As the channel length decreases, external resistance becomes an important factor to determine the performance of the device. It is caused by Schottky contact that induces the electrical barrier between source/drain metals and semiconductor channel. By the Schottky-Moot rule, Schottky barrier height is predicted as the difference between the metal workfunction and semiconductor electron affinity. However, the observed barrier height is different from the calculated value because of Fermi level pinning between the metal and semiconductor. As shown in figure 14 (a), metal work function is pinned to the charge neutral level of semiconductor by metal-induced gap states, so that Schottky barrier height increases [8,9]. To release the Fermi level pinning of metal-semiconductor contact, thin interfacial dielectrics are used as shown in figure 14 (b). Dielectric between metal and semiconductor reduce the metal-induced gap state, so that calculated Schottky

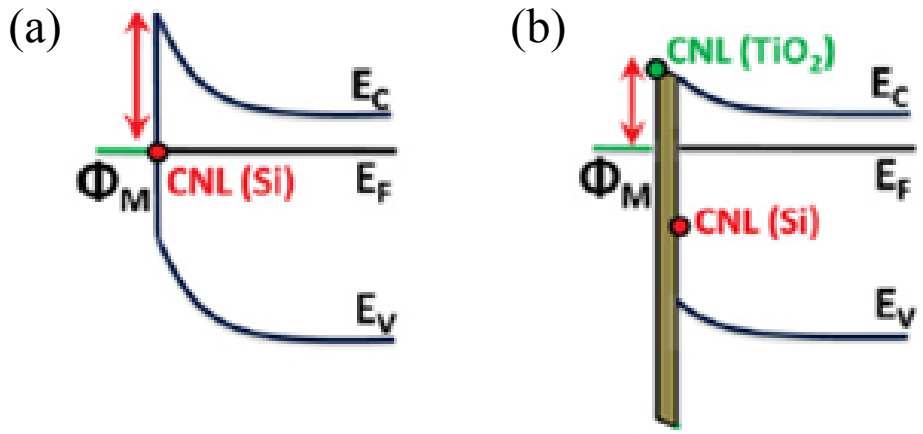


Fig. 14. Comparison of band diagram showing (a) metal-semiconductor (MS) contact and (b) metal-insulator-semiconductor (MIS) contact [9]

Barrier height can be obtained. In additions, by using dielectric such as TiO_2 and ZnO which have the similar value of electron affinity with a semiconductor, additional barrier height between semiconductor and dielectric also can be reduced [10,11].

To apply the Fermi-level pinning, the effective metal workfunction is calculated as

$$\Phi_{Meff} = S \cdot \Phi_M + (1 - S) \cdot \Phi_{CNL} \quad (1)$$

where Φ_M is the workfunction of metal and Φ_{CNL} is the energy between charge neutral level (CNL) and vacuum for the semiconductor [11]. *S* is the pinning factor showing the degree of Fermi-level pinning.

Figure 15 shows the experimental and calculated pinning factor according to the band-gap for the generally used semiconductor [11]. In case of high value of pinning factor close to 1, effective metal workfunction follows the metal workfunction. However, in case of Ge or Si which has low pinning factor, it suffers from Fermi-level pinning. In this simulation, $Si_{0.6}Ge_{0.4}$ is used as the material for channel, and therefore pinning factor is assumed to 0.2.

Table 2 shows the parameters to simulate Schottky contact that Fermi level pinning is assumed. Copper is used as the source/drain metal and Φ_{Meff} is calculated as 4.5784 eV from the original value of 4.7 eV for copper workfunction. FinFET with M-I-S contact has $1x10^{20}$ cm^{-3} doping concentration in source/drain regions.

Figure 16 (a) shows the I_D-V_G curve in linear scale according to S/D contact states. Drain current by Schottky contact increases as the doping concentration increases because

tunneling barrier thickness becomes thin. In case of M-I-S contact used FinFET, it shows the same on-current as that of FinFET that source/drain doping concentration is about $5x10^{20}$ cm^{-3}. Figure 16 (b) shows the same I_D-V_G curve in log scale according to S/D contact states. It is observed that although on-current is directly changed by effect of S/D contact states, off-current at GIDL region is rarely affected by S/D contact states because resistance of channel region is much larger than contact resistance.

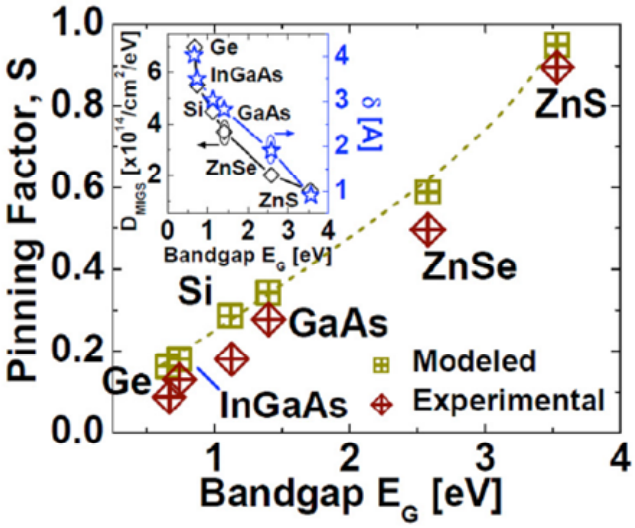


Fig. 15. Calculated and experimental pinning factor according to band-gap for various semiconductor [11]

Metal	Copper
S/D semiconductor	$Si_{0.6}Ge_{0.4}$
S factor	0.2
Φ_{Meff}	4.5784 eV
Φ_{M}	4.7 eV
Φ_{CNL}	4.548 eV

Table 2. Parameters used in simulation to apply effect of Fermi level pinning to simulator

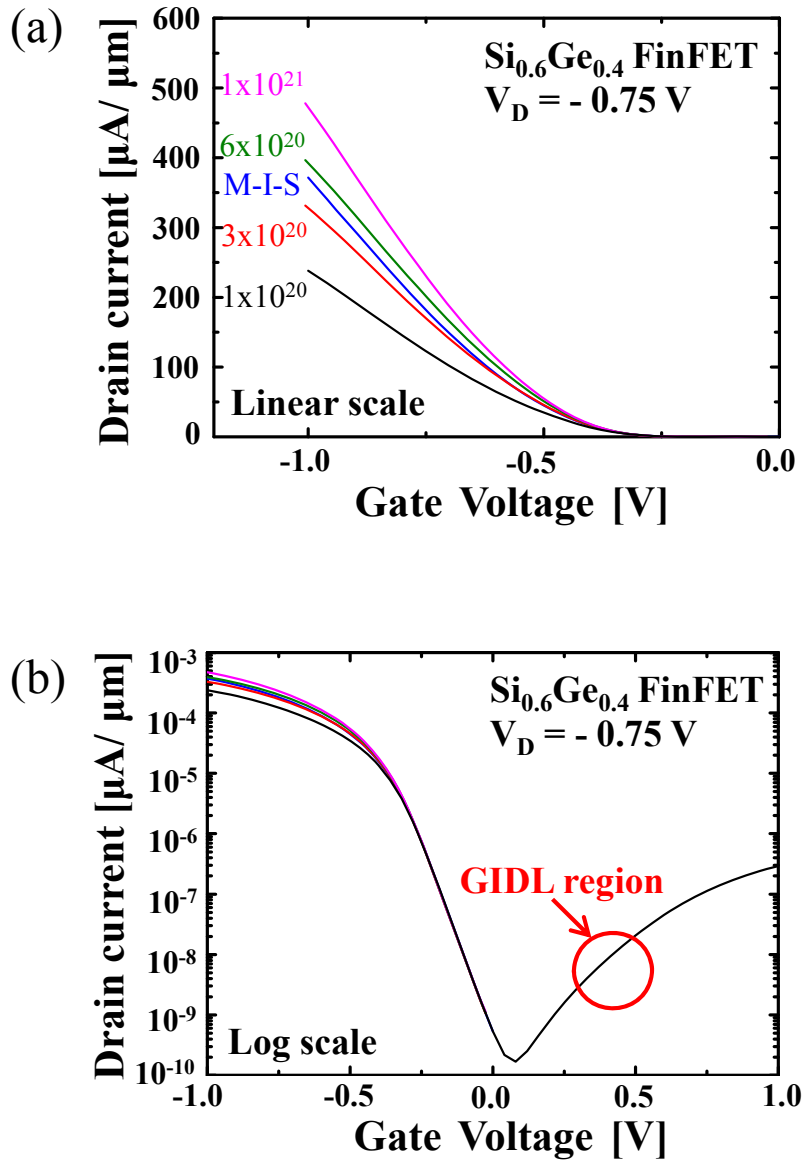


Fig. 16. Drain current characteristics according to Source/Drain (S/D) contact state in (a) linear scale and (b) log scale. M-I-S contact shows the on current that is the same as that of FinFET that source/drain doping concentration is about $5x10^{20}$ cm^{-3}

3.4. Effects of doping profile on GIDL

In case of transistors that use SiGe as the channel material, detailed research to reduce the BBT generation should be performed because small band-gap of SiGe is vulnerable to BBT generation. Band-to-band tunneling (BBT) current that is the main mechanism of GIDL current in SiGe pFinFET occurs by lateral electric field under the spacer region between channel and drain. To reduce lateral electric field between channel and drain, possible solution is to adjust doping profile at the the gate-to-drain overlap region, which is generally modified to enhance the characteristics of conventional MOFET [12,13].

In this sub-chapter, the guideline to reduce GIDL current in SiGe pFinFET will be proposed by analyzing the effects of doping concentration of drain and doping profile developed at the gate-to-drain overlap region on GIDL current.

3.4.1 Effects of gate-to-drain overlap region

Figure 17 shows the doping profile between channel and drain regions according to the length of gate-to-drain overlap region. Doping concentration at the edge of drain is fixed at $1x10^{20}$ cm^{-3}, and the length of gate-to-drain overlap region is set to be from 2 nm to 8 nm.

Since the potential difference between channel and drain regions is not large enough to cause GIDL current at low gate bias, main component of off-current is sub-threshold leakage current. Figure 18. (a) shows the I_D-V_D characteristics at V_G = 0 V according to gate-to-drain overlap region but there is not any difference between each drain current. This result shows that gate-to-drain overlap region does not affect the sub-threshold leakage current. However, as the gate bias increases, sub-threshold leakage current is suppressed, and GIDL current begins to occur by increasing potential difference between channel and drain regions. Figure 18. (b) shows the drain current characteristics at off state (V_G = 0.3 V). Under this bias condition, main component of leakage current is band-to-band tunneling, which increases with the increasing length of gate-to-drain overlap region.

Figure 19 shows the energy band diagram between channel and drain regions according to each length of overlap region at V_G = 0.3 V and V_D = -0.75 V, which is the region of band-to-band tunneling current. As shown in figure, there is enough band bending by potential difference between channel and drain regions, and band-to-band

tunneling occurs. As the length of overlap region increases, the location of energy band diagram becomes closer to the channel region. By the invasion of boron doping from drain to channel region, the energy band in channel region would be expected to increase. However, by the strong gate controllability on channel region, the energy band in channel region would not increase to what is expected, and it cause steeper energy band bending in the case of long overlap region. Therefore, an electric field increases as the length of overlap region increases.

Figure 20 shows the total amount of band-to-band tunneling generation in the fin. As mentioned above, since a lateral electric field increases as the length of overlap region increases, band-to-band tunneling generation also increases. As a result, it is desirable to decrease the length of gate-to-drain overlap region.

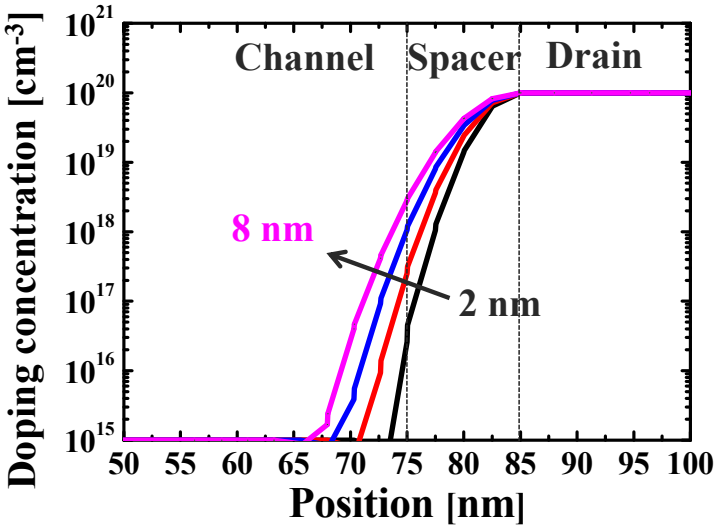


Fig. 17. Doping profile between channel and drain regions according to the length of gate-to-drain overlap region

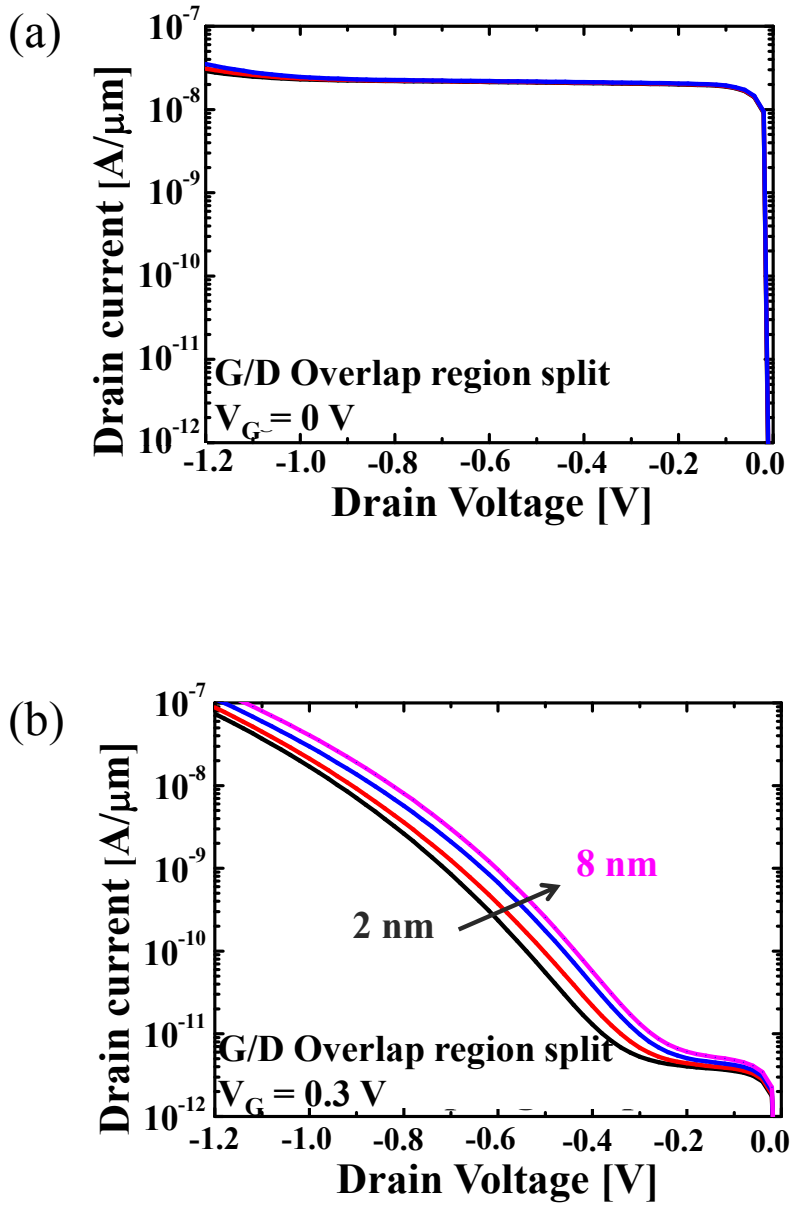


Fig. 18. Drain current characteristics at off state (Vg = 0 and 0.3 V) according to the length of gate-to-drain overlap region

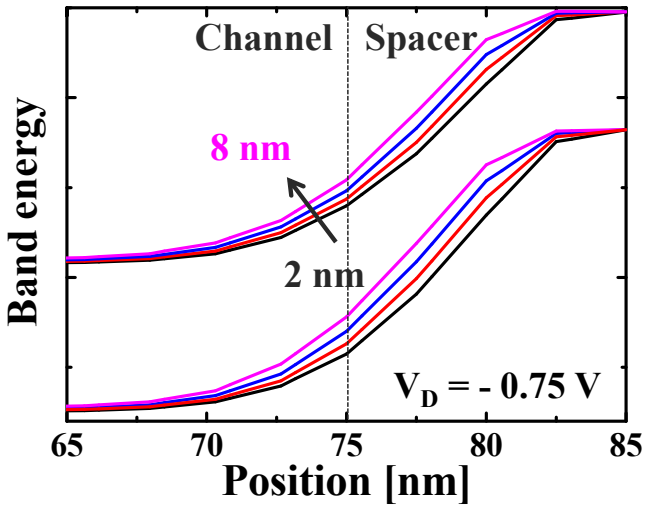


Fig. 19. Energy band diagram between channel and drain regions according to the length of gate-to-drain overlap region

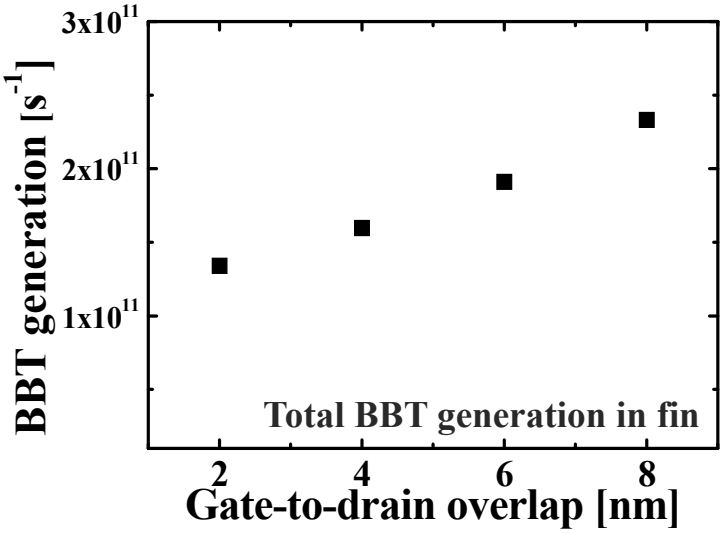


Fig. 20. Band-to-band tunneling generation according to the length of gate-to-drain overlap region

3.4.2 Effects of drain doping concentration

Figure 21 shows the doping profile between channel and drain regions according to the concentration of drain doping. Gate-to-drain overlap region is fixed at 2 nm, and doping concentration at channel region is $1x10^{15}$ cm^{-3} while doping concentration at the edge of drain is set to be from $1x10^{20}$ to $5x10^{20}$ cm^{-3}.

Figure 22 shows the I_D-V_D characteristics at V_G = 0 V. As mentioned in previous sub-chapter, sub-threshold leakage current is dominant component of off-current under above bias conditions and is independent of doping concentration of drain region.

Figure 23 shows the I_D-V_G characteristics at V_D = -0.75 V. It is observed that as the doping concentration of drain region increases, off-current by band-to-band tunneling mechanism increases. This result is also explained by increasing lateral electric field between channel and drain regions.

Figure 24 is the distribution of band-to-band tunneling generation according to the doping concentration of drain region. It is observed that band-to-band tunneling generation occurs dominantly under the spacer region, and high doping concentration of drain region induce larger band-to-band tunneling generation than any other conditions. It is because the potential difference between channel and drain regions becomes larger at high doping concentration of drain region. Therefore, it is desirable to reduce the difference of doping concentration between channel and drain regions.

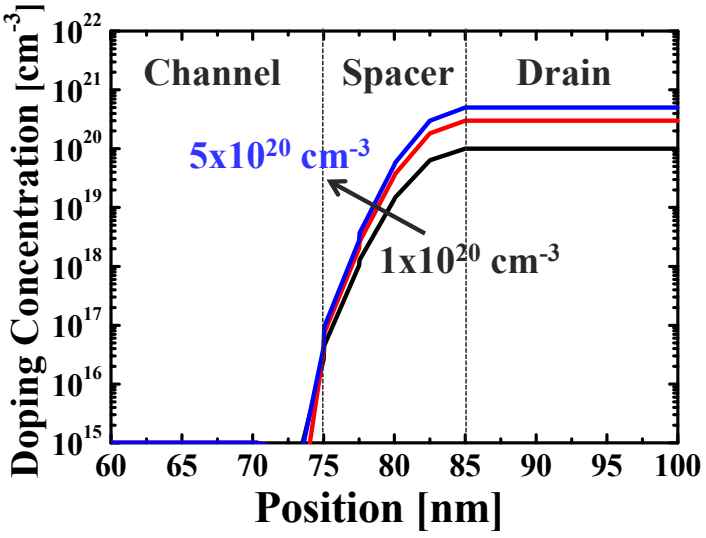


Fig. 21. Doping profile between channel and drain regions according to the doping concentration of drain region

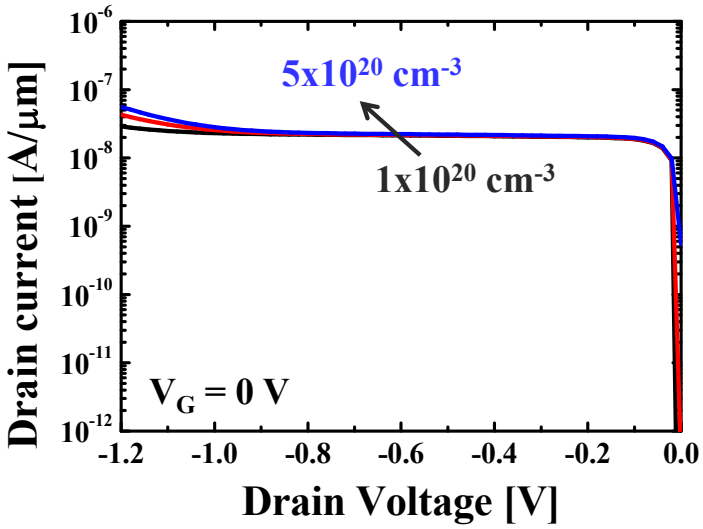


Fig. 22. Drain current characteristics at off state (Vg = 0 V) according to the doping concentration of drain region

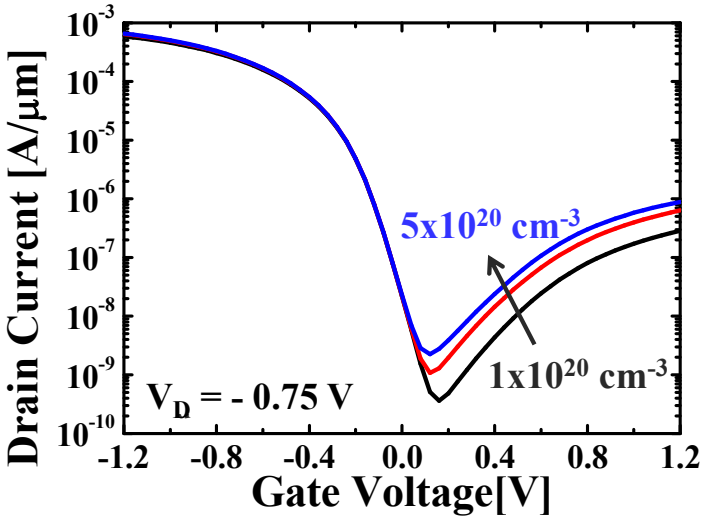


Fig. 23. Off-current characteristics according to the doping concentration of drain region

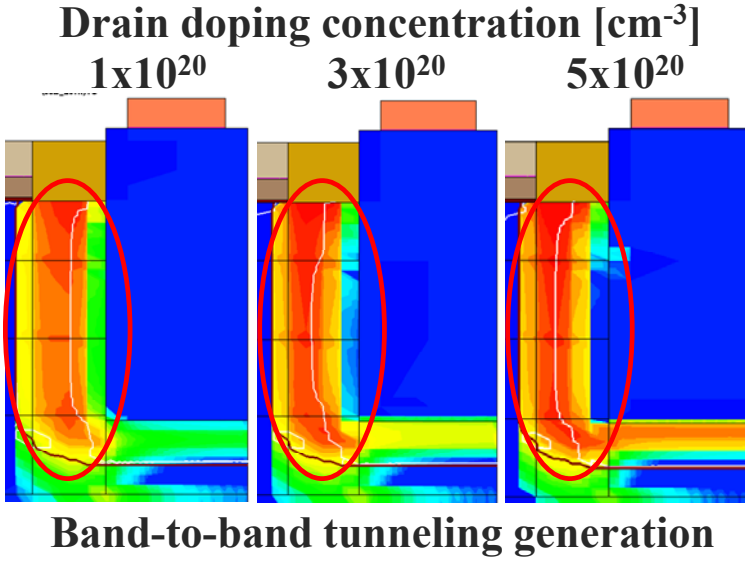


Fig. 24. Distribution of band-to-band tunneling generation according to the doping concentration of drain region

3.4.3 Conclusion

In this sub-chapter, effects of doping profile developed between channel and drain on the GIDL current is investigated. Since doping profile has an effects on the lateral electric field applied between channel and drain, it needs to be studied to reduce the band-to-band tunneling (BBT) generation that is the dominant mechanism of GIDL current. First, as the gate-to-drain overlap length increases, BBT generation also increases. It is because the lateral electric field applied between channel and drain increases by the steep band-bending as the gate-to-drain overlap increases. Second, it is the GIDL characteristics according to doping concentration of drain region. High doping concentration in source/drain regions has been proposed to reduce the contact resistance at source/drain regions. However, it increases BBT generation because the lateral electric field increases as the difference of doping concentration between channel and drain regions increases. As a result, it is desirable that for the FinFET of low-power transistors, gate-to-drain overlap regions should decrease, and doping concentration of drain region also should be low as long as the on current is guaranteed.

3.5 Junction depth under the drain region

To reduce V_t roll-off that threshold voltage decreases as the channel length decreases [14-16], it has been important to decrease junction depth by drain doping developed around gate edge. In contrast, junction depth developed under the drain region has not been investigated because it was not considered as an important factor to determine the performance of transistors. In this sub-chapter, however, it is confirmed that junction depth under the drain region would be an important factor to determine the leakage current in SiGe pFinFET.

Figure 25 (a) and (b) shows the cross section of SiGe pFinFET according to junction depth under the drain region. SiGe pFinFET is manufactured by developing the SiGe on Si wafer. Therefore, material of fin region for channel is SiGe, and that of substrate under the fin is Si. Considering manufacture processes, junction depth is assumed to be – 10 nm and + 10 nm from the gate edge line that is shown as white dotted line. In case of junction depth of + 10 nm, drain doping permeates the Si substrate that is at the un-doped state. As a result, since energy band between SiGe and Si is changed, it would have an effect on the current characteristics. This change rarely affects the on-current but the off-current.

Figure 26 shows the band-to-band tunneling (BBT) generation according to relative junction depth based on gate edge line. It is observed that as junction depth increases beyond gate edge line, BBT generation increases steeply. This component is also one of the main mechanisms that consist of leakage current in FinFET. To confirm the origin of BBT current, the distribution of BBT generation would be plotted.

Figure 27 shows the distribution of BBT generation according to relative junction depth that is – 10 nm and + 10 nm based on gate edge line. Before junction depth that is shown as dark red line touches the gate edge line, BBT generation under the spacer region is the dominant mechanism of GIDL current. However, as the relative junction depth increases beyond the gate edge line, additional BBT generation occurs at the boundary region between SiGe drain and Si substrate. To analyze the cause of additional BBT generation, it needs to investigate energy band diagram at each case.

As shown in figure 28, energy band diagram is plotted according to relative junction depth that is – 10 nm and + 10 nm based on gate edge line at thermal equilibrium state. Since the doped type of Si is changed from un-doped state to p-doped state by drain doping, energy band of Si around gate edge line is changed. As a result, in case of relative junction depth of + 10 nm (blue line), intrinsic electric field applied between SiGe and Si is larger than that of – 10 nm (black line). Therefore, as the energy band of drain region increases by increasing negative drain voltage, band-to-band tunneling generation that electrons in the valence band of SiGe drain are tunneled out to the conduction band of Si substrate occurs easily in junction depth of + 10 nm (blue line). From the simulation result, it is desirable that SiGe drain doping should not permeate the Si substrate not to generate additional BBT current in FinFET.

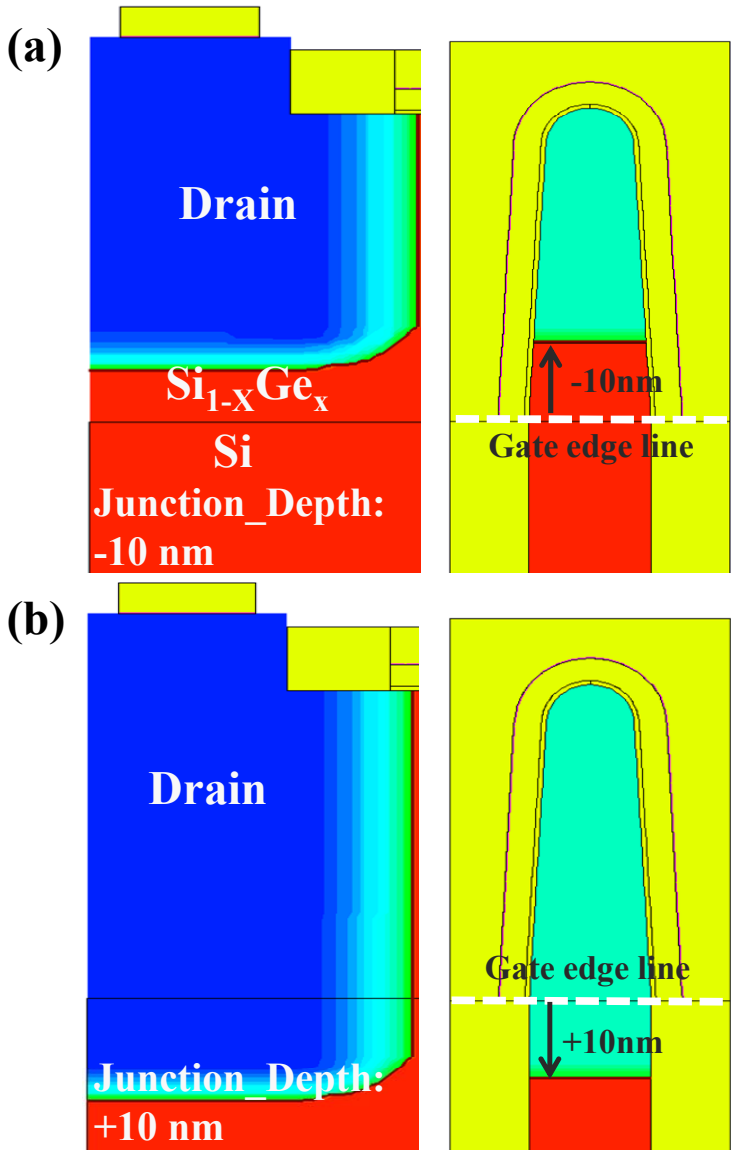


Fig. 25. Cross section of SiGe bulk pFinFET according to junction depth under the drain region. Based on the gate edge line that is shown as white dotted line, SiGe is developed as a channel material on Si substrate.

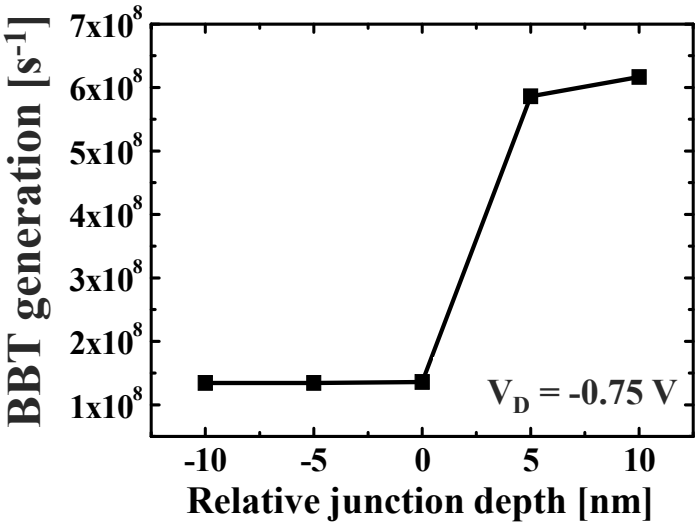


Fig. 26. Band-to-band generation according to relative junction depth based on gate edge line

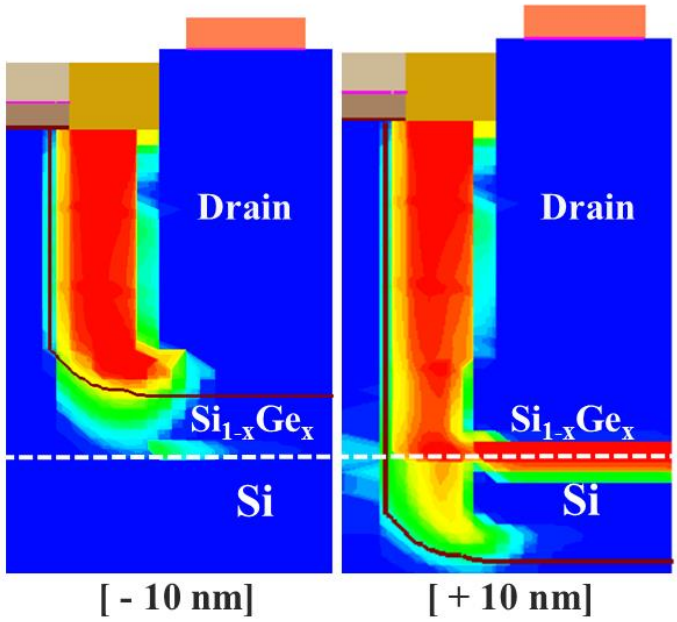


Fig. 27. Distribution of band-to-band tunneling generation according to junction depth under the drain region (-10 nm and + 10 nm)

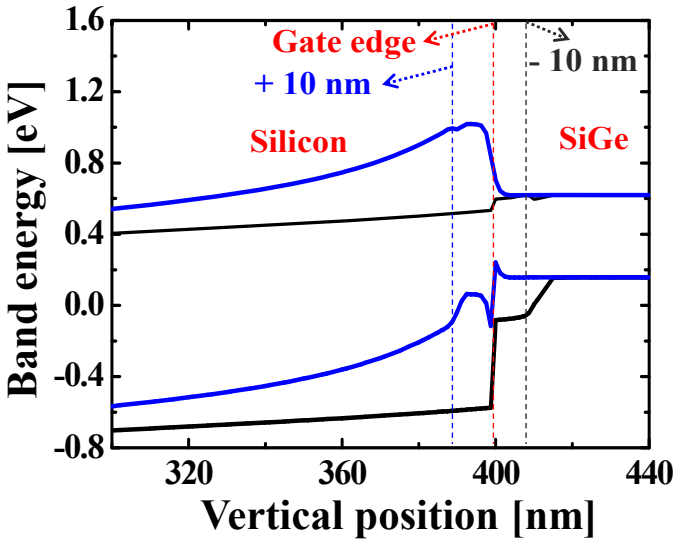


Fig. 28. Schematic of energy band diagram according to junction depth (-10 nm and +10 nm) at thermal equilibrium state. As boron for drain doping permeates the Si substrate (blue line), intrinsic electric field is developed and make band-to-band tunneling generate easily

3.6 Summary

Previous chapter, it is confirmed that the mechanisms of GIDL current in SiGe pFinFET are the trap-assisted tunneling (TAT) and band-to-band tunneling (BBT) that occur between channel and drain regions. In this chapter, various factors that would affect the GIDL current are investigated, and guideline to reduce the GIDL current is proposed. First, Ge fraction of SiGe pFinFET is investigated as the dominant factor to affect GIDL current because it determines the performance of transistors directly. In SiGe pFinFET, it is desirable that high Ge fraction in channel and low Ge fraction in source/drain are developed as long as Ge fraction guarantees the on-current. In addition, it is suggested that Ge fraction at the top region of fin should be lower than that at the bottom region of fin. Second, doping profile developed between channel and drain on the GIDL current is also important factor to determine the GIDL current. It is desirable that for the FinFET of low-power transistors, gate-to-drain overlap regions should decrease, and doping concentration of drain region also should be low as long as the on current is guaranteed. Finally, junction depth under the drain region is considered as the factor to generate additional BBT current. To block additional BBT current by structural cause, it is desirable that SiGe drain doping should not permeate the Si substrate. However, manufacturing process conditions such as corner process, fin width, and S/D contact states do not affect the GIDL characteristics.

Chapter 4

Optimization of $Si_{1-x}Ge_x$ pFinFET for low-power transistors

In this chapter, performance of $Si_{1-x}Ge_x$ pFinFET is investigated by considering the results to reduce GIDL current from previous chapter. The performance of the device by optimized conditions is compared with that by worst conditions.

To assess performance, basic device specifications are assumed by 7 nm node technology requirements from ITRS 2013. Channel length is set to be 14.6 nm, and threshold voltage is 0.459 V. To consider the stress effect by the lattice mismatch between channel and source/drain regions, stress effect is assumed from the previous research [1]. It is assumed that stress effect is determined by only the difference of lattice constant of two regions between channel and source/drain regions. The most important parameter to affect the device performance is the fraction of Ge. As Ge fraction increases, hole mobility increases while the strain effect decreases because the difference of lattice constant between channel and drain regions decreases. Gate-to-drain overlap length is also one of the parameters to affect GIDL current. Optimized value is set to 1.46 nm that is 10 % of channel length while worst value is about 2.9 nm that is 20 % of channel length. Other parameters such as S/D doping concentration and junction depth are set to be the same value because effects of those parameters are weak in short channel device.

Assessment items for performance of the device are Subthreshold-Swing (S.S.), Drain-Induced-Barrier- Lowering (DIBL), On/Off currents, On/Off ratio, and $G_{m,peak}$.

Table 1 shows the simulation results of device performance according to device specifications of $Si_{1-x}Ge_x$ pFinFET. Since Ge fraction changes the band-gap and stress effect, Ge fraction dominantly determines the device performance. Until the 30 % of Ge fraction, S.S. and DIBL are almost same but abruptly increase beyond 40 % of Ge fraction in $Si_{1-x}Ge_x$ pFinFET. Although off-current and on/off ratio of $Si_{0.85}Ge_{0.15}$ pFinFET is better than that of $Si_{0.8}Ge_{0.2}$ pFinFET, $Si_{0.8}Ge_{0.2}$ pFinFET has largest on-current among the device specifications, which is about 10 % larger than that of $Si_{0.85}Ge_{0.15}$ pFinFET. In additions, as Ge fraction increases, off-current increases, and therefore on/off ratio decreases beyond $Si_{0.8}Ge_{0.2}$ pFinFET. As a result, $Si_{1-x}Ge_x$ pFinFET of optimized condition is $Si_{0.8}Ge_{0.2}$ pFinFET rather than $Si_{0.85}Ge_{0.15}$ pFinFET because larger on-current of $Si_{0.8}Ge_{0.2}$ pFinFET can satisfy the requirement of ITRS 2013 easily while other performance parameters maintain acceptable values. As Ge fraction increases beyond 50 %, stress effect becomes weak because the difference of lattice mismatch between channel and drain regions decreases. Therefore, on-current of $Si_{0.4}Ge_{0.6}$ pFinFET decreases abruptly compared with $Si_{0.5}Ge_{0.5}$ pFinFET though S.S. and DIBL decrease. In addition, on/off ratio and $G_{m,peak}$ also decrease. As a result, $Si_{0.4}Ge_{0.6}$ pFinFET is set to be the $Si_{1-x}Ge_x$ pFinFET of worst conditions.

Figure 1 shows the comparison of device performance for $Si_{1-x}Ge_x$ pFinFET simulated by optimized and worst conditions. Optimized one is $Si_{0.8}Ge_{0.2}$ pFinFET while worst case is $Si_{0.4}Ge_{0.6}$ pFinFET. $Si_{0.8}Ge_{0.2}$ pFinFET has larger on-current, on/off ratio, and $G_{m,peak}$

than those of $Si_{0.4}Ge_{0.6}$ pFinFET because performance is improved by large compressive strain effect. In additions, since $Si_{0.8}Ge_{0.2}$ pFinFET has larger band gap than that of $Si_{0.4}Ge_{0.6}$ pFinFET, it shows lower off-current characteristics, so that S.S. and DIBL are also low. As a result, optimized $Si_{1-x}Ge_x$ pFinFET for low power transistors in 7 nm node technology is $Si_{0.8}Ge_{0.2}$ pFinFET.

pFinFET	**$Si_{0.85}Ge_{0.15}$**	**$Si_{0.8}Ge_{0.2}$**	**$Si_{0.75}Ge_{0.25}$**	**$Si_{0.7}Ge_{0.3}$**	**$Si_{0.6}Ge_{0.4}$**	**$Si_{0.5}Ge_{0.5}$**	**$Si_{0.4}Ge_{0.6}$**
Stress [Gpa]	**- 3.37**	**- 3.25**	**- 3.12**	**- 2.98**	**- 2.66**	**- 2.26**	**- 1.73**
S.S. [mV/dec]	**94**	**96**	**98**	**102**	**108**	**116**	**111**
DIBL [mV/V]	**71**	**71**	**71**	**74**	**83**	**90**	**83**
On-current [μA/μm]	**432.4**	**476.3**	**447.35**	**447.35**	**449.65**	**430.1**	**369**
Off-current [nA/μm]	**9.0**	**15.2**	**25.1**	**43.1**	**97.1**	**183.7**	**277**
On/Off ratio	**$4.81x10^4$**	**$3.13x10^4$**	**$1.78x10^4$**	**$1.03x10^4$**	**$4.63x10^3$**	**$2.34x10^3$**	**$1.3x10^3$**
$G_{m,peak}$ [μS/μm]	**2054**	**2186**	**2191**	**2153**	**2039**	**2028**	**1781**

Table. 1. Device performance according to various device specifications of $Si_{1-x}Ge_x$ pFinFET

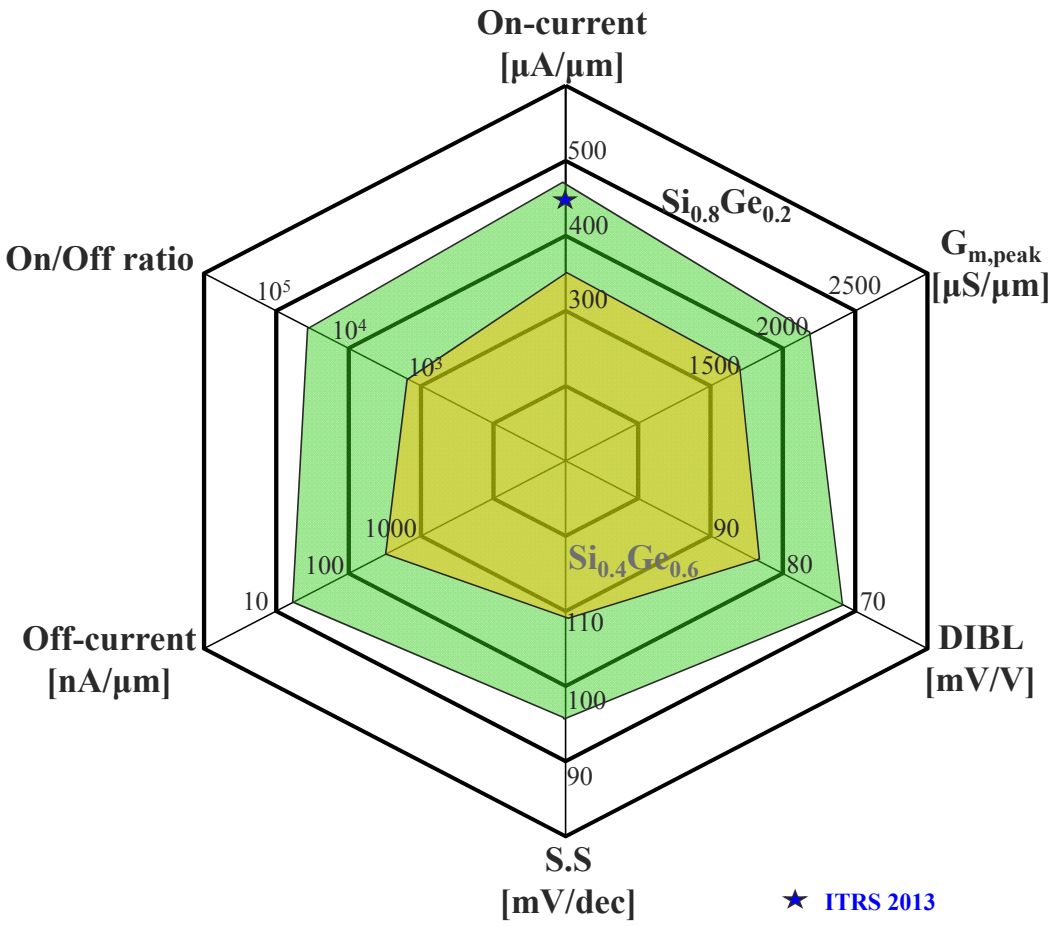


Fig. 1. Comparison of device performance for $Si_{1-x}Ge_x$ pFinFET simulated by optimized and worst conditions. Optimized one is $Si_{0.8}Ge_{0.2}$ pFinFET while worst case is $Si_{0.4}Ge_{0.6}$ pFinFET. Star point at the axis for on-current is the reference point by ITRS 2013.

Chapter 5

Conclusion

GIDL current is the main leakage current in conventional MOSFET. However, as the structure of transistor is changed to FinFET that channel is surrounded by gate in three ways, GIDL current is not expected because of strong ability to controal channel potentrial. Different from its expectation, GIDL current is still observed in FinFET and is the main leakage current. To investigate the mechanism of GIDL current in FinFET, GIDL current is simulated in Sentaurus TCAD. The mechanisms of GIDL current are trap-assisted tunneling (TAT) and band-to-band tunneling (BBT) that are modeled by Hurkx model based on Shockley-Read-Hall (SRH). As a result, it is confirmed that TAT and BBT current in FinFET occur by lateral electric field applied between channel and drain region. To reduce GIDL current in SiGe pFinFET, various factors are analyzed, and the guideline for low-power transistors is proposed. First, Ge fraction of SiGe pFinFET is investigated as the dominant factor to affect GIDL current. In SiGe pFinFET, it is desirable that high Ge fraction in channel and low Ge fraction in source/drain are developed. In addition, it is suggested that Ge fraction at the top region of fin should be lower than that at the bottom region of fin. Second, It is desirable that for the FinFET of low-power transistors, gate-to-drain overlap regions should decrease, and doping concentration of drain region also should be low as long as the on current is guaranteed. Finally, to block additional BBT current by structural cause, it is desirable that SiGe drain

doping should not permeate the Si substrate. From the previous results, it is confirmed that optimized SiGe pFinFET in 7 nm node technology is $Si_{0.8}Ge_{0.2}$ pFinFET because it has large compressive stress and band-gap. These results will be very useful to manufacture the SiGe pFinFET for low-power transistors.

Appendix A. Analysis of leakage current by strain engineering

A.1 Introduction

Strain engineering technology that uses two materials with different lattice constant is widely investigated to improve the mobility in transistors. As shown in figure. 1, the material with small lattice constant is engineered by the material with large lattice constant. States of strained material beomes ‘tensile’ or ‘compressive’ according to the direction or position of material. In this strained material, carrier mobility can be improved because changed E-K diagram by engineered lattice constant can decrease carrier effectrive mass. However, interface traps are generated by the lattice mismatch at the boundary region between two materials, and band-gap of engineered material is also changed [1-3]. These results affect the leakage current including sub-threshold leakage current, trap-assisted tunneling, and band-to-band tunneling.

Figure 2 shows the structure of Si bulk FinFET simulated in the appendix. Si layer that cosists of source, drain and fin regions is engineered to tensile state by SiGe substrate. Therefore, impoved electron moblity is expected but interface traps generated at the boundary region between Si drain and SiGe substrate and change of band-gap are also

expected to affect the performance of transistor. In this appendix, effects of interface traps and change of band-gap on leakage current will be investigated.

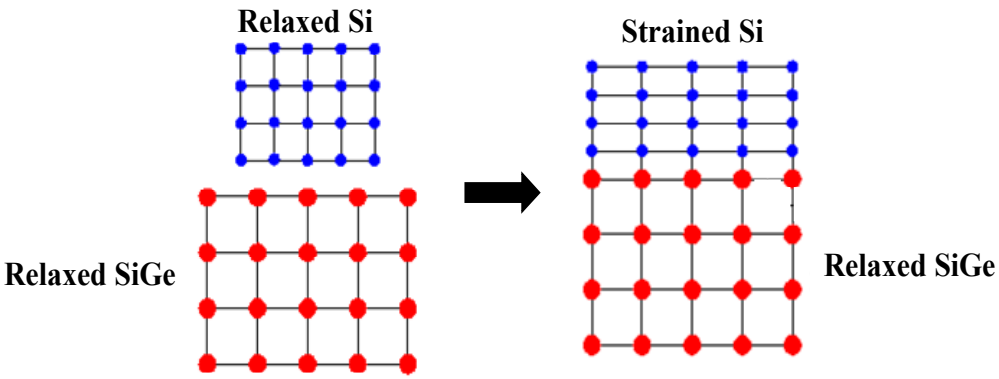


Fig. 1. Strain engineering technology that uses two materials with different lattice constant

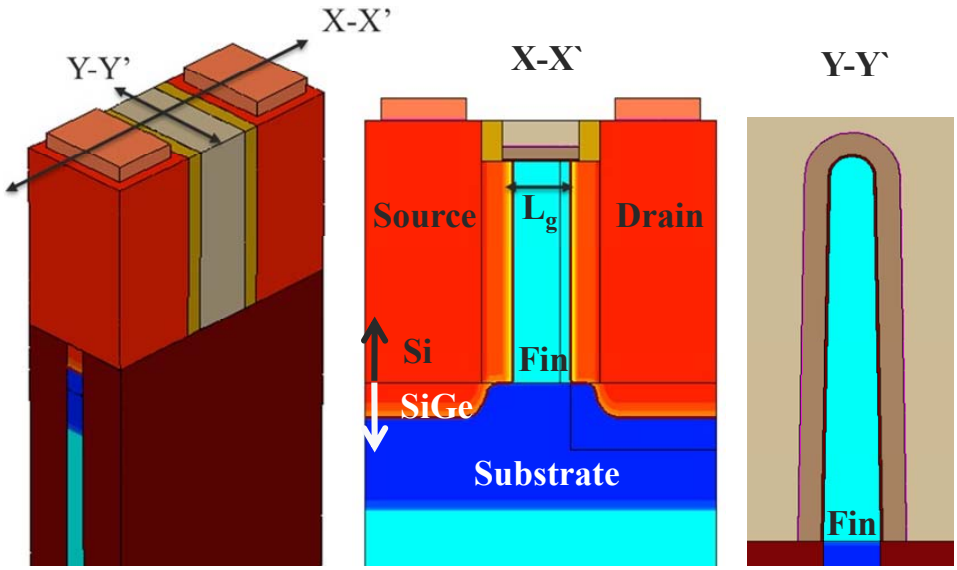


Fig. 2. Structure of Si bulk FinFET simulated in this appendix. Si layer on SiGe substrate consists of source, drain, and fin regions

A.2 Eeffect of interface traps on leakage current

Figure. 3 (a) shows the cross section of bulk Si FinFET. Since traps are generated by lattice mismatch at the region between Si drain and SiGe substrate, traps are assumed to be randomly located in a white box under the drain region. The number of traps are assumed to be from 1 to 50. Equivalent value of trap density is from $5.5x10^{17}$ cm^{-3} to $2.75x10^{19}$ cm^{-3}. Figure. 3 (b) shows the schematic of energy band diagram describing the mechanism of leakage current by traps at the boundary region between drain and substrate. As band-bending occurs by positive bias that are applied to n-doped drain region, trap-assisted tunneling (TAT) that electrons in the valence band of p-doped substrate are tunneled to the conduction band of n-doped drain occurs and contributes to leakage current.

Figure 4 shows the simulation process to extract the leakage component generated by traps. In figure 4 (a), there is a p-n junction between source/drain and substrate because source/drain are doped by n-type, and substrate is doped by p-type. Therefore, as V_{DD} is applied to source/drain/gate, forward-bais diode is developed between source/drain and substrate, and junction leakage current is generated. In case of (b), the additional leakage current by traps is obtained with basic p-n junction leakage current. As a result, the difference of leakage current between (a) and (b) is the only leakage component by traps.

Figure 5 shows the junction leakage current according to the number of traps. It is observed that junction leakage current with traps increases a hundred times more than that without the traps. As a result, since the interface trpas between Si and SiGe generated by

strain engineering cause a additional leakage current, it needs to investigate the solution to suppress the generation of traps by strain engineering.

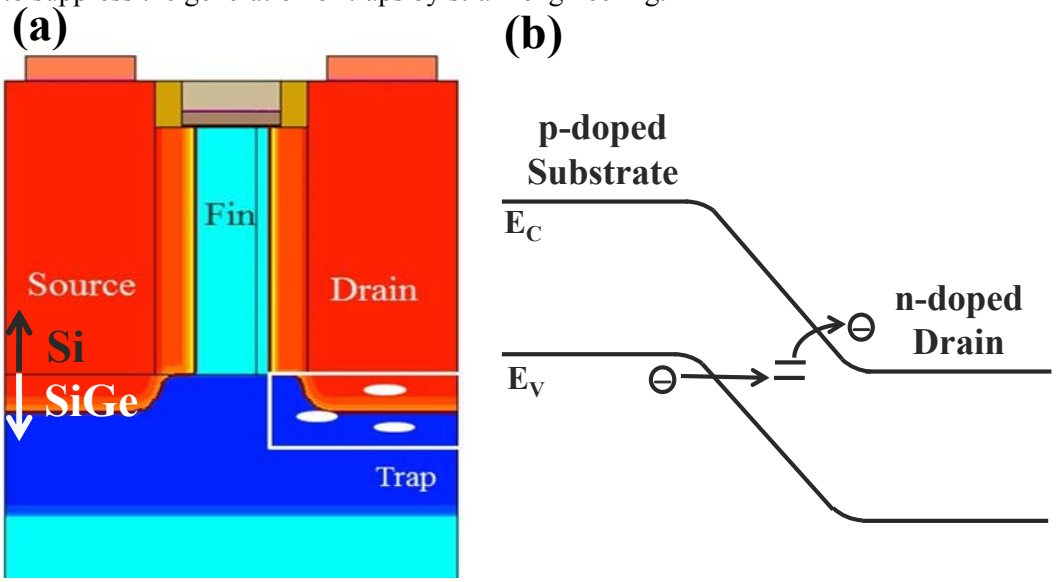


Fig. 3. (a) Cross section of bulk Si FinFET that traps between drain and substrate are assumed. (b) Schematic of energy band diagram describing trap-assisted tunneling generation by traps between drain and substrate regions.

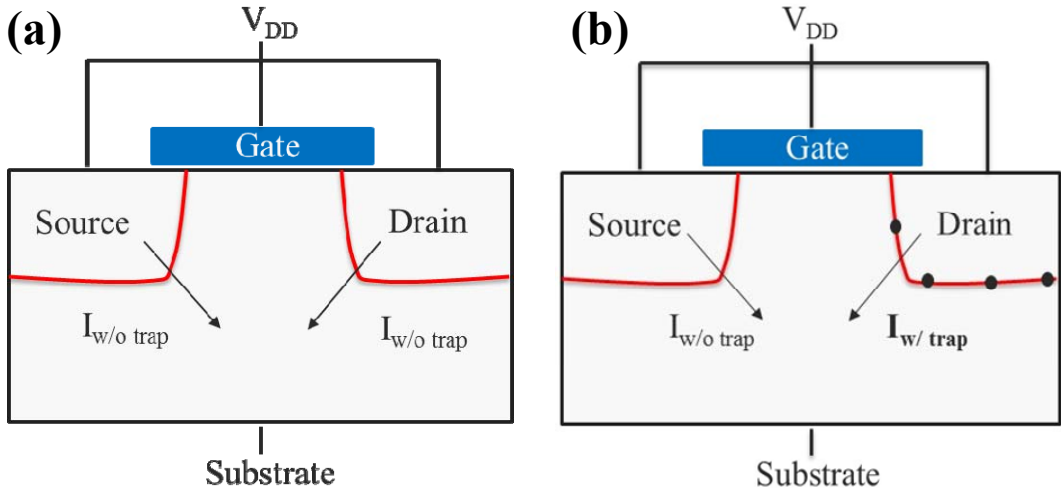


Fig. 4. Simulation process to measure the leakage current by traps. The difference of I_{sub} between (a) and (b) is the current by traps

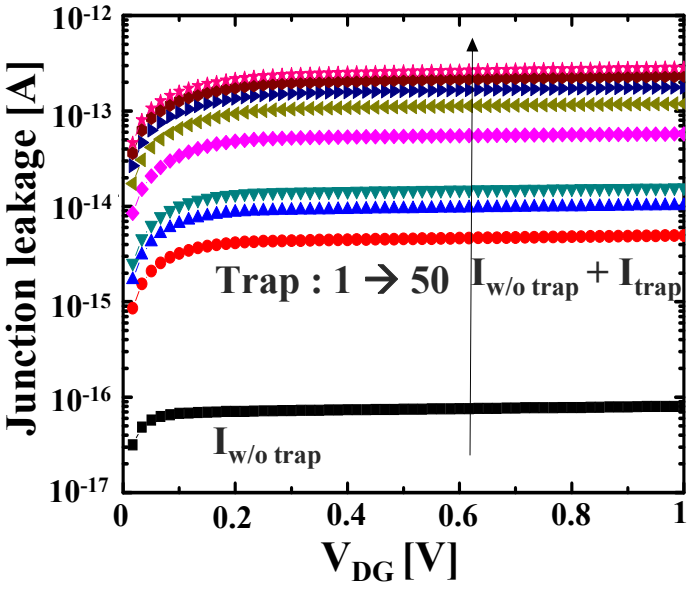


Fig. 5. Junction leakage current according to the number of traps at the region between Si drain and SiGe substrate

A.3 Effect of band-gap on leakage current

Figure 6 shows the effect of variation of band-gap according to the location where band-to-band tunneling (BBT) current occurs. The variation of band-gap is set to be from 0 eV to 0.12 eV by 6-level. Figure 6 (a) shows the GIDL characteristics by BBT when the variation of band-gap occurs at the region between drain and substrate. It is observed that BBT generation increases as band-gap decreases because the tunneling probability increases. Figure (b) shows the effects of BBT generation on GIDL according to the variation of band-gap at the region between channel and drain. It is comfirmed that the effect of variation of band-gap on GIDL current is than that at the region between drain and substrate. To explain the result, BBT hurkx model is specified in :

$$R_{bbt} = A \cdot D \cdot \left(\frac{F}{1V/cm} \right)^{P} exp\left(\frac{B \cdot E_g(T)^{3/2}}{E_g(300K)^{3/2} F} \right) \quad (1)$$

As mentioned in chapter 2, BBT generation is determined by the electric field as well as the tunneling probability by the scale of band-gap. Therefore, in case that the variation of band-gap occurs at the region near the drain contact, large electric field is applied, and the effect of variation of band-gap on BBT generation becomes larger. As a result, the effect of variation of band-gap on GIDL current is larger at the region between channel and drain, and solution to supress the band-gap variation is needed to reduce the additional BBT generation.

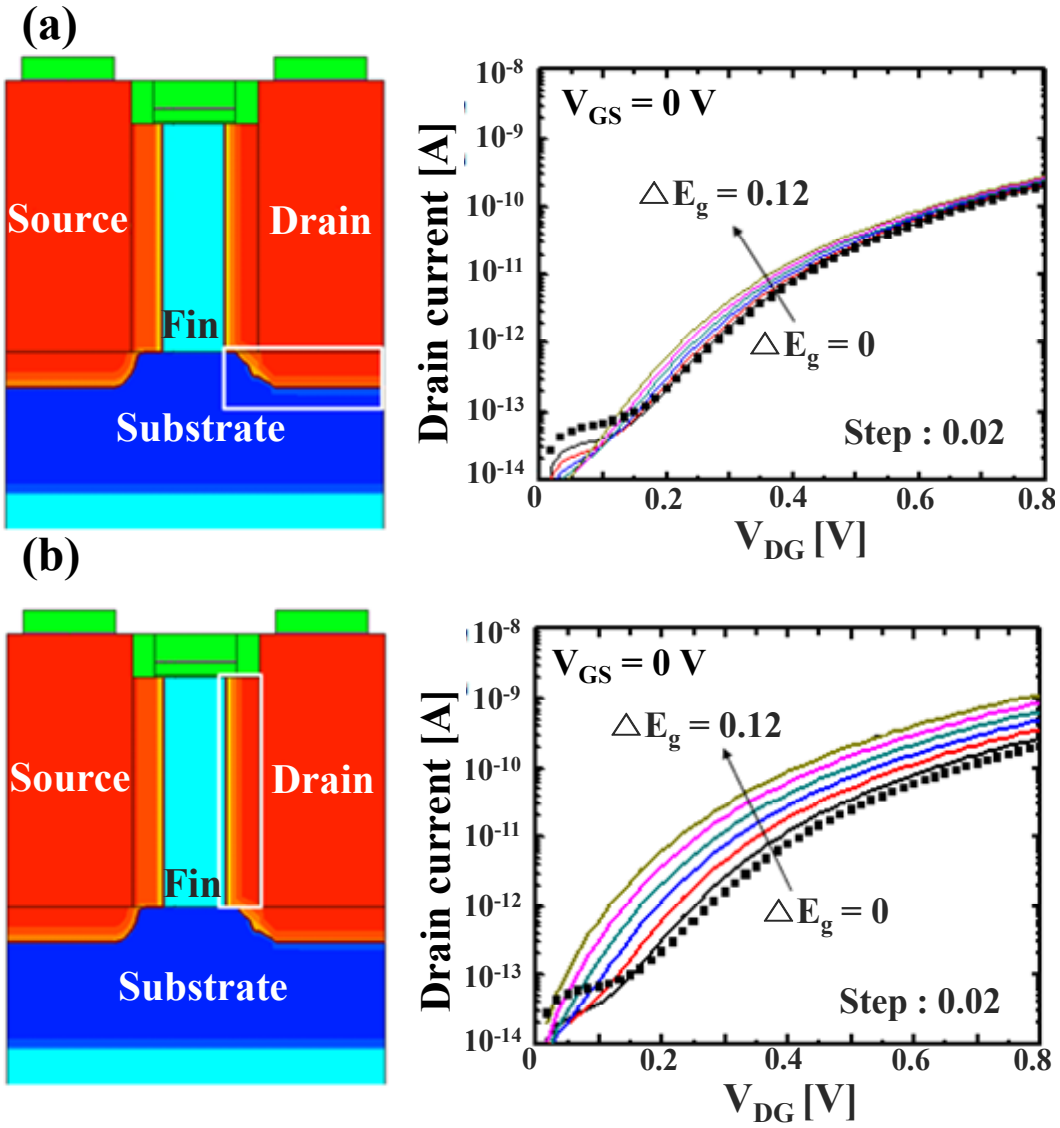


Fig. 6. Leakage current characteristics by band-to-band tunneling according to the variation of band-gap at two different regions

A.3 Conclusion

Strain engineering technology is widely investigated to improve the mobility in transistors. The material with small lattice constant is engineered by the material with large lattice constant. In this strained material, carrier mobility can be improved because changed E-K diagram by engineered lattice constant can decrease carrier effectrive mass. However, interface traps are generated by the lattice mismatch at the boundary region between two materials, and band-gap of engineered material is also changed.

Interface traps between Si and SiGe can induce the additional leakage current. It is confirmed that junction leakage current with traps increases a hundred times more than that without the traps. Strain engineering also changes the band-gap of material, so that the additional leakage current by BBT occurs. Since the tunneling probability increases in small band-gap material, leakage current by BBT increases. In additions, in case that the variation of band-gap occurs at the region between channel and drain, the effect of band-gap variation on leakage current is strong because the electric field at the region near the drain contact is strong. As a result, the solution to reduce the side effects of strain engineering should be investigated to suppress the additional leakage current.

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초 록

본 논문에서는 저전력 트랜지스터를 위한 SiliconGermanium (SiGe) 채널을 사용하는 p타입 핀펫의 Gate-Induced-Drain-Leakge (GIDL) 전류를 시뮬레이션을 통해 심도있게 분석하고, 누설전류를 감소시키기 위한 방안을 제시하였다. 첫번째로 본 논문에서 연구한 핀펫과 소자의 물리적 조건이 동일하게 설계된 모스펫에서 발생하는 GIDL 전류 메커니즘을 비교하여 핀펫에서 발생하는 주된 메커니즘을 분석하였다. 두번째로 소자의 채널 물질로 사용되는 SiGe 물질의 Ge 비율과 fin 내부의 분포에 따른 GIDL 전류에 미치는 영향을 분석하였다. 세번째로 핀펫에서 소자의 물리적 조건과 드레인 영역의 도핑 프로파일이 GIDL 전류에 미치는 영향을 분석하였다. 본 논문에서 연구된 핀펫에서 발생하는 GIDL의 주된 메커니즘과 소자의 물리적 조건에 따른 특성은 실제 제작된 SiGe 핀펫의 특성 향상에 큰 도움이 될 것이다.

주요어: SiGe, 핀펫, GIDL, band-to-band tunneling, trap-assisted tunneling, TCAD 시뮬레이션

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