Ph.D. DISSERTATION

A STUDY ON ENVELOPE TRACKING CMOS RF POWER AMPLIFIER FOR MOBILE APPLICATIONS

이동통신용 포락선 추적 CMOS 전력 증폭기에 관한 연구

BY

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SCHOOL OF ELETRICAL ENGINEERING AND
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지도 교수 서 광 석

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Abstract

In this dissertation, three advanced techniques to solve system issues in CMOS envelope tracking power amplifier (ET PA) is presented.

First of all, a dynamic FET stack control technique is developed to enhance the efficiency of the envelope tracking power amplifier (ET PA) system for low-voltage operation. The power cell used in the two-stage PA is a quadruple stacked FET structure with dynamic stacking controller to reconfigure the power cell into the quasi-triple or quasi-double stacks according to the magnitude of the input envelope signal. Proposed power cell boosts the peak efficiency in the low V_{DD} region by bypassing the stack entering the triode region and re-optimizing the load impedance so that all the FETs operate under the saturation and the optimum load conditions. A detailed analysis is presented to understand the gain and phase step discontinuities at the stack switching points, and the circuit techniques to equalize the gain and phase between the adjacent stack configurations are developed. The proposed two-stage stack-controlled PA is fabricated with 0.32-μm Silicon-on-insulator (SOI) CMOS process together with the envelope amplifier (EA). Full long term evolution (LTE) characterization is performed using LTE signals with a peak to average power ratio (PAPR) of 6.7 dB and signal bandwidths (BW) of 10- and 20-MHz. With 10-MHz signals, dynamic stacking provides 3.5% power added efficiency (PAE) improvement over the static stack at 25.7 dBm, resulting in 47.5% PAE with 26.6 dB gain. 20-MHz LTE test shows an overall PAE of 45.9% with evolved universal terrestrial radio access (E-UTRA) adjacent channel leakage ratio (ACLR) of –33 dBc with memory-less digital pre-distortion (DPD). Even with the

lower efficiency of the EA compared with the state-of-the-art results, the measured overall system efficiency with 3.4 V maximum voltage is comparable with those reported using GaAs HBT's with 5 V supplies, which clearly demonstrates the advantages of the proposed dynamic stack control.

Second, a linear CMOS envelope tracking power amplifier is developed for wideband long term evolution-advanced (LTE-A) applications without using DPD. AM-AM distortion of the ET PA is flattened by the iso-gain envelope shaping while AM-PM distortion is compensated by the integrated phase linearizer. A single ET calibration step is required to generate the iso-gain shaping function, whose output is used to internally generate the control signal to the phase linearizer. Bandwidth limitation of the proposed approach is carefully investigated through the envelope simulation, which shows that the proposed approach can support wider bandwidth signal if the gain bandwidth product (GBW) of the operational trans-conductance amplifier (OTA) in the phase linearizer is large enough. The two-stage RF PA with the proposed phase linearizer is fabricated in 0.28-μm SOI CMOS process, and tested together with 0.32-μm SOI CMOS EA to demonstrate full ET PA system. When tested with a 40-MHz BW, intra-band contiguous carrier aggregation (CA) LTE-A signals, the overall system PAE of the ET PA system is 37% at 24 dBm output power. CA evolved universal terrestrial radio access adjacent channel leakage ratios (CA E-UTRA$_{ACLRs}$) is improved from –25.7 to –33 dBc by the phase linearizer. 40-MHz AM-AM and AM-PM dynamic characteristics of the ET PA are also measured to verify the effectiveness of the proposed linearizer. The overall efficiency of this work using CMOS FETs is comparable to or better than the most of the reported ET LTE PAs using GaAs and SiGe HBTs.

Finally, a wideband EA with diode rectifier current injector is developed to overcome the problems of the conventional hybrid type EAs for 80-MHz BW LTE applications. The proposed EA is composed of a bias modulator and diode rectifier current injection circuit. The operation principle and efficiency of the proposed EA is investigated based on the equation based analysis. The proposed EA takes two input signals which are iso-gain shaped envelope signal and CW RF signal which has same carrier frequency to the RF PA's input RF signal. The proposed EA and 2-stage RF PA with a phase linearizer are fabricated in same 0.28-μm SOI CMOS process and overall ET PA is tested using wideband LTE signals up to 80-MHz. When tested using 80-MHz BW LTE signal, the overall system PAE reaches 41.2% at 25.2 dBm output power with –33.5 dBc E-UTRA$_{ACLR}$. A wideband performance is characterized using various bandwidth LTE signals which shows only 2.5 dB ACLR degradation without PAE degradation as the signal bandwidth is increased from 20- to 80-MHz. The measured Rx band noise using 5-MHz BW LTE signal at 50 MHz frequency offset is –126.1 dBm/Hz, which meets the system requirements. This is a first demonstration of the CMOS ET PA that covers 80-MHz BW LTE signals.

Keywords : AM-AM, AM-PM, Carrier aggregation, CMOS, crest factor reduction (CFR), digital pre-distortion (DPD), diode rectifier, dynamic stacking, efficiency, envelope amplifier (EA), envelope tracking (ET), linearizer, long term evolution (LTE), long term evolution-advanced (LTE-A), power amplifier (PA), Rx band noise (RxBN), silicon-on-insulator (SOI), switching noise, wideband.

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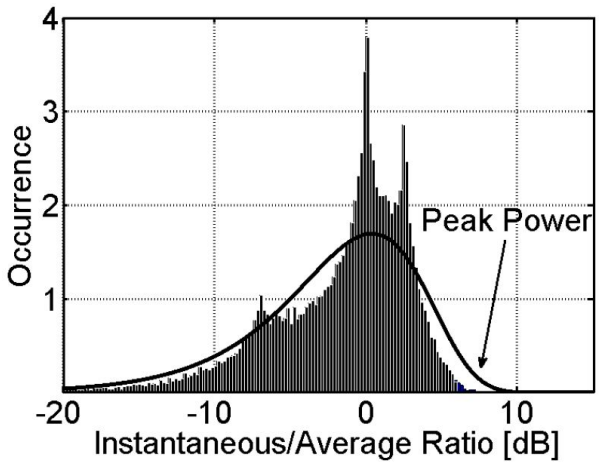
Chapter 1

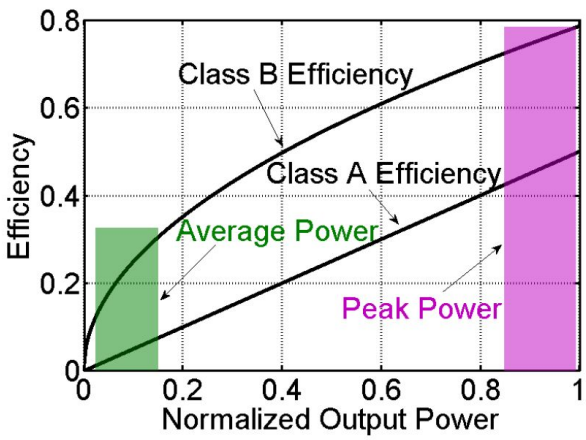
Introduction

1.1 Motivation

Modern multi-mode mobile phones require 4G long term evolution (LTE), and long term evolution-advanced (LTE-A) coverage on top of the existing 3G wideband code division multiple access (W-CDMA). This presents special challenge to the design of high-efficiency RF power amplifiers (RF PA's) due to a wide range of peak-to-average-power ratio (PAPR) of the transmit signals. For example, W-CDMA voice signal has only 3.4 dB PAPR while a 20-MHz BW fully-loaded 16-QAM LTE signal has a PAPR as high as 7.43 dB. Moreover, the PAPR of wideband LTE-A signals whose maximum bandwidth is extended to 100-MHz by aggregating 5 carriers is generally higher than 9~10 dB. Fig. 1.1 (a) is a histogram of the 20-MHz BW 16-QAM LTE signal. Even if the most of power is concentrated in 0 dB region, still there are a few powers at the high power region. To meet the stringent linearity requirements, the RF PA should be operated in back-off power region not to lose the signal information at the high power region. However, the RF PA with a static bias control suffers from steep efficiency degradation at the backed-off power levels. Fig. 1.1 (b) shows the normalized



(a)



(b)

Fig. 1.1. (a) Histogram of the fully loaded 20-MHz BW 16-QAM LTE signal. (b) Normalized efficiency of the Class-A and Class-B RF power amplifier.

efficiency of the class-A and Class-B RF PAs. The peak efficiency of the ideal Class-B is as high as 78.5% while the efficiency at the back-off power region is dropped to only 30~35%. Envelope tracking (ET) is widely investigated to overcome this problem especially for 3G/4G mobile handset applications.

The envelope tracking is a bias modulation technique to achieve the high overall system efficiency. Fig. 1.2 is a block diagram of the typical ET PA architecture. The ET PA has two circuit blocks which are envelope amplifier (EA) and RF PA. In ET PA applications, the drain (or collector) bias of the RF PA is dynamic modulated by the EA in order to the RF PA operates in the saturation mode. In this dissertation, both EA and RF PA are fabricated in silicon-on-insulator (SOI) CMOS process and three advanced design techniques to overcome the several system level issues inherited by the inferior RF characteristics of the CMOS FET are presented.

1.2 Dissertation organization

Fig. 1.2 is a block diagram that shows the scope of this dissertation. The EA and RF PA are implemented using SOI CMOS process and advanced design techniques are introduced in each chapter.

In chapter 2, a dynamic FET stack control for enhanced efficiency in ET PA is presented. Although many researches have demonstrated ET PA system using CMOS RF PAs, their overall system PAE were not matched to the ET PAs with GaAs or SiGe ET PAs. In this chapter, device level investigation of the CMOS ET PA is performed to identify the reason why CMOS ET PAs generally have low efficiency compared to the HBT ET PAs. Also, circuit design to enhance the overall system PAE of the CMOS ET PA using a new concept of dynamic FET stack control is demonstrated. The performance of the overall ET PA system with a proposed concept is measured using 10- and 20-MHz BW LTE signals which shows 3.5 and 3% efficiency enhancement without the linearity deterioration.

Chapter 3 proposes the effective linearization technique to compensate both AM-AM and AM-PM distortion of the ET PA in wideband LTE-A signals. Even if the conventional linearization method for ET PA has been a digital pre-distortion (DPD), the DPD has several system level issues which makes the DPD not applicable in wideband signals. A circuit design technique to linearize the distortions of the ET PA is demonstrated in this chapter and verified by the 40-MHz BW LTE-A test.

Chapter 4 focuses on the design of the EA that overcomes problems inherited from the conventional hybrid type EAs. The proposed EA which is composed of bias modulator and diode rectifier current injection circuit is introduced in this

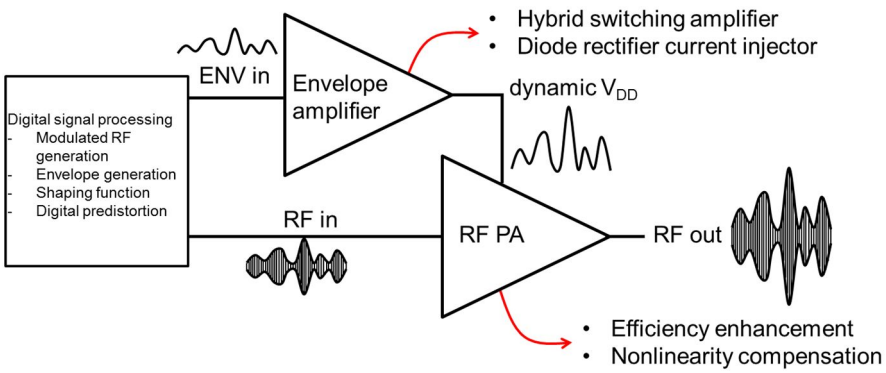


Fig. 1.2. The envelope tracking RF power amplifier architecture and scope of this work.

chapter and its operation principle and potential for wideband ET application are demonstrated. A wideband ET PA test using 80-MHz BW LTE signal is presented together with an Rx band noise measurement data to clearly demonstrate the advantages of the proposed concept.

Finally the dissertation ends with conclusions in Chapter 5 which summarizes the three design techniques for RF PA and EA, demonstrated in this dissertation.

Chapter 2

Dynamic Stack-Controlled CMOS RF Power Amplifier for Wideband Envelope Tracking

2.1 Introduction

As the communication era is evolved from third generation wideband code division multiple access (3G W-CDMA) to fourth generation long term evolution (4G LTE), the demand for highly efficient power amplifiers (PAs) for mobile phones increases to extend the battery life. However, designing a highly efficient PA for LTE is a challenging work due to a high peak-to-average-power ratio (PAPR) of the modern modulation scheme and the stringent linearity requirements. To overcome this problem, various efficiency enhancement techniques have been investigated so far, including Doherty PA, out-phasing PA, digital mode PA, and so on [1]-[3]. However, each configuration has its own disadvantages respectively. For example, although a high power added efficiency (PAE) of 43.6% has been demonstrated using CMOS Doherty amplifier with good linearity in [1], they used bulky $\lambda/4$ transformer in the output matching network, which restricts the RF

bandwidth of the amplifier. Likewise, out-phasing PA suffers from the similar problems due to the reactive compensation components inside the power combiner [2]. The maximum continuous wave (CW) output power of the digital mode PA is limited to 25 dBm [3].

An envelope tracking PA (ET PA) has been given much attraction because of their superior efficiency performance, in particular, for high PAPR signals such as LTE [4]-[16]. Because the overall efficiency of ET PA is a weighted product of the efficiency of the envelope amplifier (EA) and RF PA, both components should be optimized to deliver the best system efficiency. To address the efficiency enhancement of the EAs, a number of papers have recently been published. For example, Hassan *et al.*, demonstrated excellent 48% overall PAE ET PA using 83% efficiency dual switching EA in [4]. Likewise, AC-coupled multilevel regulator is introduced in [5], resulting in 86% EA efficiency. Moreover, the potential for a single ET PA to cover broad RF bandwidth (BW) has been demonstrated in [6].

ET PAs for mobile phones have been recently demonstrated using GaAs HBTs and BiCMOS transistors, showing very high overall system efficiencies ([4], [7], [8]). Most of these works employed advances in the EA design and used 5 V voltage drive, which requires a separate boost DC-DC converter to work in a mobile phone with 3.7 V nominal battery. CMOS-based ET PA has also been demonstrated with 5 V max supply using the thick-gate oxide FETs in the cascode FETs [9]. However, the efficiency was not as high as GaAs counterparts. Considering the breakdown voltage limitation of CMOS devices and the battery voltage requirement from the mobile phones, it is preferred to develop a CMOS ET

PA for 3.4 V maximum supply operation. However, relatively large knee voltage in CMOS and the limitation of FET stacking limits RF PA performance.

In this work, low-voltage operation of stacked CMOS ET PA is demonstrated using a new concept of dynamic stack control. A two-stage dynamic stack-controlled ET PA operating with 3.4 V maximum voltage maintains high efficiencies down to 5 dB backed-off power region, and shows overall PAE higher than 47% for 10-MHz LTE signal with 6.7 dB PAPR. This chapter is organized as follows. Section 2.2 presents the operation principle of dynamic stack control as well as the detailed analysis to solve the potential linearity issues arising from the dynamic stack control. In Section 2.3, the detailed circuit design of the two-stage RF PA using silicon-on-insulator (SOI) CMOS process is explained together with the design of the envelope amplifier implemented using the same process. The measurement results are shown in Section 2.4, which includes CW data, dynamic AM-AM/AM-PM data as well as full LTE characterization data using both 10- and 20-MHz bandwidth LTE signals.

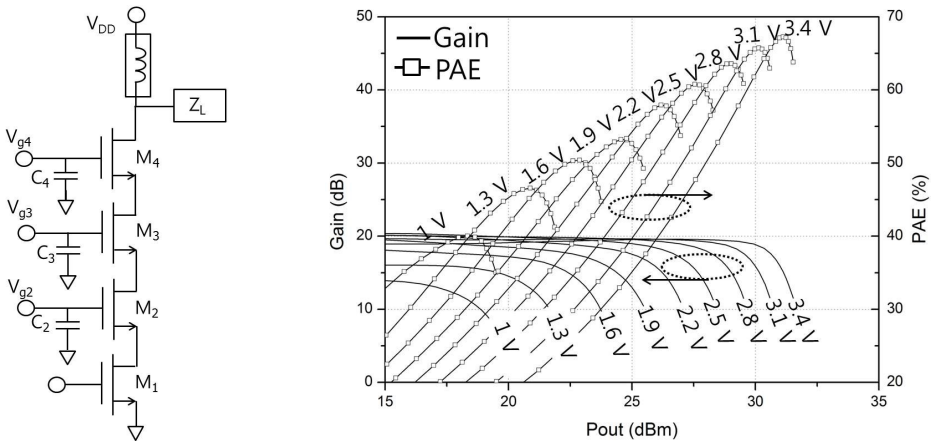
2.2 Operation Principle of the Proposed Power Cell

2.2.1 Dynamic FET Stack Control

The Fig. 2.1 (a) is the circuit schematic of a single-stage quadruple-stack power cell, and the simulated CW gain and PAE are plotted in Fig. 2.1 (b) as the DC drain biases (V_{DD}) are swept from 1 to 3.4 V in 0.3 V steps. The peak PAE gradually decreases as the V_{DD} is lowered, which results in the degraded overall system efficiency of 3G/4G ET PAs because most of the power is concentrated in 5~6 dB backed-off power levels from the maximum output power for modern communication schemes, such as LTE.

The lowering of the peak PAEs at lower V_{DD} is attributed to the non-optimal load impedance as V_{DD} is lowered [17]. Fig. 2.2 shows the optimum load impedance (Z_{opt}) for PAE, calculated from the load-pull simulation of the quadruple-stack CMOS FET cell as V_{DD} is reduced from 3.4 to 1.8 V in 0.4 V steps. Z_{opt} is 6.1+j7.3 Ω at V_{DD}=3.4 V, which is the pre-determined impedance that the PA load matching circuit is designed for. As V_{DD} is lowered, Z_{opt} moves counter-clockwise roughly along the constant-G circle due to the sharp increase of junction capacitance in the knee region, which results in severe PAE degradation at low voltages. Similar problem can also happen in GaAs HBTs. However, the problem is much more serious in CMOS FETs due to its stacked cell structure and relatively large knee voltage region. Also, ET PAs using GaAs HBTs often employ the boost converter to crank up the voltage levels up to 5-6V [10], which is not effective for CMOS FETs due to the low breakdown voltage.

This problem can be overcome by operating each FET in the saturation region to stay away from the knee voltage, where the junction capacitance increases sharply.



(a) (b)

Fig. 2.1. (a) schematic of the quadruple-stack power cell, and (b) simulated CW gain and PAE as the drain biases are swept from 1 to 3.4 V in 0.3V steps.

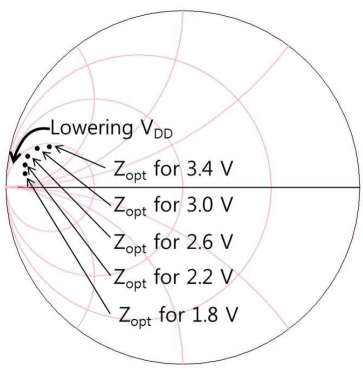


Fig. 2.2. Simulated optimum load impedance (Z_{opt}) of the quadruple-stack power cell as a function of V_{DD}

For example in [9] and [11], dynamic gate bias control circuit is employed in CG FET of the cascode PA to prevent the PA from operating in the triode region. However, the measured PAE improvement was limited to only 0.5% [9] due to the insufficient V_{DD} headroom. Instead, we have proposed dynamic FET stack control for effective efficiency enhancement for ET PA operation [12]. The key idea is to control the number of the active FET stacks in the power cell according to the

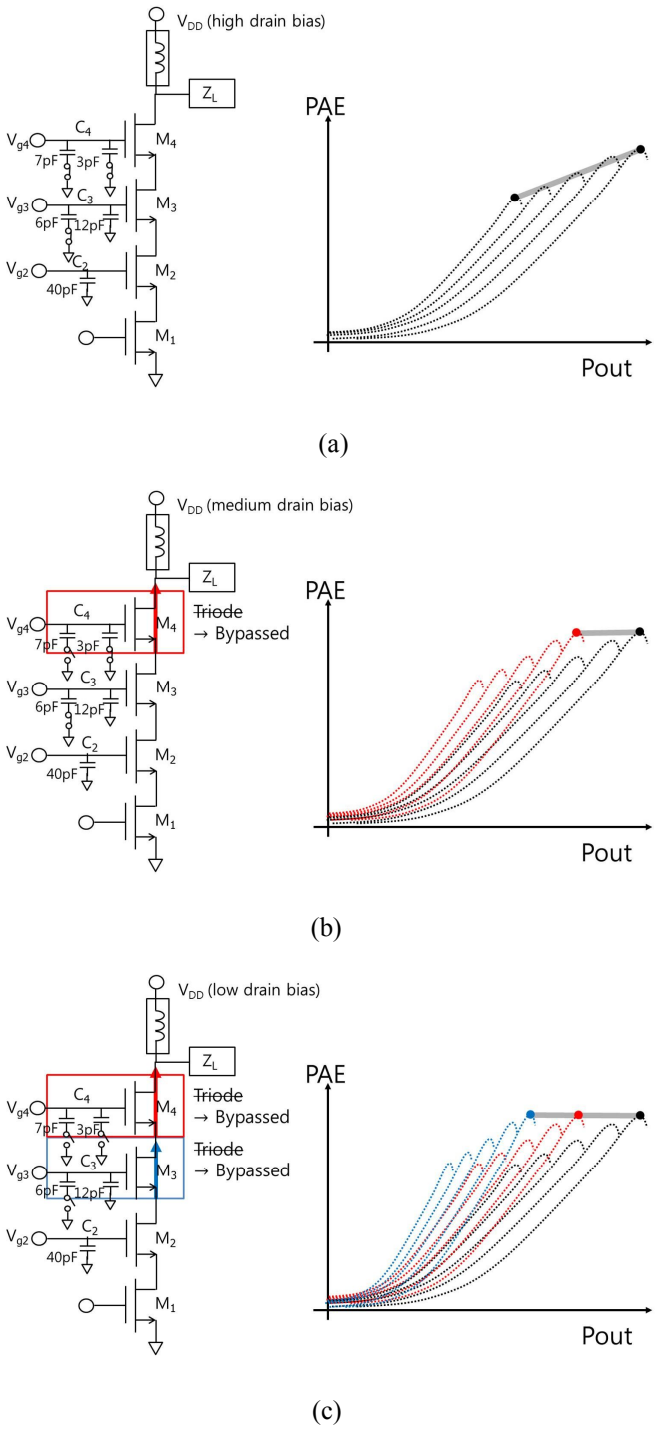
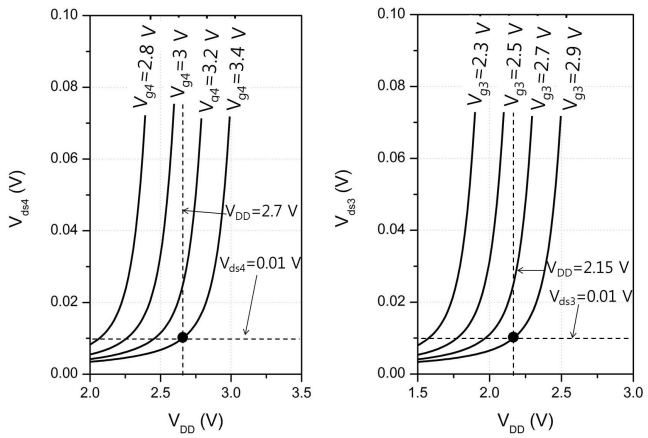


Fig. 2.3. Schematic and PAE trajectory of the quadruple stacked power cell in (a) Quadruple-stack state (b) Quasi-triple stack state (c) Quasi-double stack state.



(a) (b)

Fig. 2.4. Simulated voltage drop across (a) M_4 and (b) M_3 to determine the gate bias levels.

instantaneous drain voltage level, and synthesize the optimum load impedance for each stack configuration.

Fig. 2.3 shows the operation principle of dynamic stack control. When the drain bias is in the highest state, all four FETs are activated in the saturation region, corresponding to quadruple-stack operation in Fig. 2.3 (a). Since all the FETs operate in the saturation region, the pre-determined load impedance matches the optimum loadpull impedance, resulting in the highest peak PAE. As the drain bias is lowered (quasi-triple stack state in Fig. 2.3 (b)), the uppermost FET (M_4) goes into the triode region, generating load impedance mismatch. To prevent the efficiency degradation, the uppermost FET is bypassed, resulting in a quasi-triple stack operation. In this mode, the uppermost FET does not produce any gain.

Finally, when the drain bias level is further reduced (quasi-double stack state in Fig. 2.3 (c)), M_3 also operates into the triode region. To avoid the efficiency degradation, M_3 is also bypassed on top of M_4, resulting in a quasi-double stack operation.

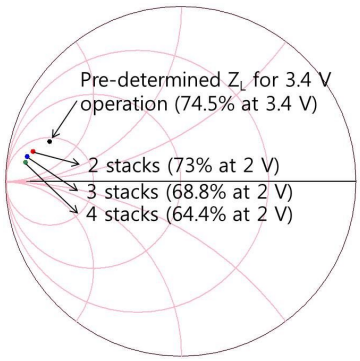
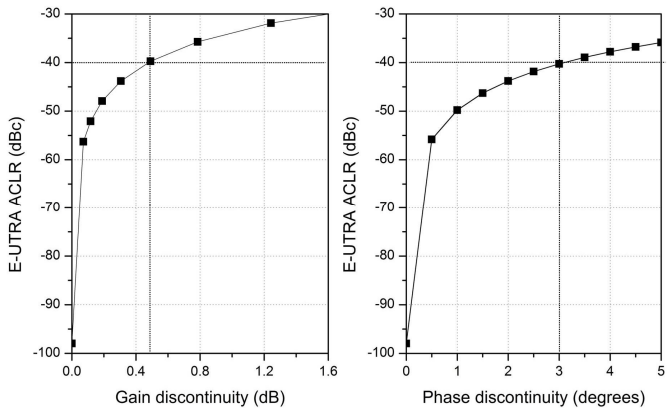


Fig. 2.5. Simulated Z_{opt} for PAE as the stack is reconfigured from quadruple to quasi-triple and to quasi-double stack. The loadpull simulation is performed at 2 V V_{DD}.

For optimum efficiency operation, the PA should be designed carefully to satisfy two conditions. First, the proper bias has to be applied to the bypassed FET so that the on-state resistance and the voltage across the bypassed FET are negligible. Second, the load impedance presented to the reduced stack should be adjusted to provide the optimum load impedance. To satisfy the first condition, we should determine the drain bias level to trigger FET bypassing and then, find the gate bias of the FETs to be bypassed. Based on CW simulation results using different number of stacks (similar to Fig. 2.1 (b)), we have determined the first switching point to reduce the number of stacks from four to three is 2 dB back-off from the maximum power. The corresponding V_{DD} level to bypass M_4 is calculated to be 2.7 V. The gate bias to the M_4 (V_{g4}) is then determined based on the voltage drop requirement across M_4 (V_{ds4}). Fig. 2.4 (a) shows the calculated V_{ds4} as a function of V_{DD} with various V_{g4}. If we set the maximum allowable voltage drop of M_4 at 0.01 V, V_{g4} should be higher than 3.4 V. Following the same logic, the second switching power is determined to be 4 dB back-off from the maximum power, which corresponds to the second V_{DD} switching point of 2.15 V. Based on the DC



(a) (b)

Fig. 2.6. Simulated E-UTRA ACLR as a function of (a) gain and (b) phase step discontinuity. The input signal is 20-MHz BW 6.7 dB PAPR LTE signal.

simulation results for M_3 shown in Fig.2.4 (b), the gate bias to M_3 (V_{g3}) is determined to be 2.9 V, which guarantees less than 0.01 V voltage drop of the M_3 (V_{ds3}).

The second condition of load impedance adjustment is fulfilled by reducing the capacitance at the gate terminal of the bypassed FET. For example, the load impedance for the quasi-triple stack is adjusted by disconnecting one of the two shunt capacitors attached to the gate terminal of M_4. The total capacitance at the gate terminal of M_4 (C_4) is reduced from 10 to 3 pF by floating 7 pF shunt capacitor using a switch as shown in Fig. 2.3 (b). Likewise, the capacitance at the gate terminal of M_3 is reduced from 18 to 12 pF while the remaining capacitance at the gate terminal of M_4 is totally floated from the ground when M_3 is bypassed for quasi-double stack operation. The actual capacitance ratio for C_4 and C_3 are determined based on the gain discontinuity analysis, which is explained in the next section.

The load-pull simulation is performed using the proposed dynamic power cell to verify the efficiency enhancement. Fig. 2.5 shows the optimum load point (Z_{opt}) in reference to the pre-determined load impedance (Z_L) of 6.1+j7.3 Ω as the number of the stack is reduced from 4 to 2. The drain bias used for this simulation is 2 V, which corresponds to the average bias for 6.7 dB PAPR LTE signal. It can be found from Fig. 2.5 that the optimum load impedance moves toward the pre-determined Z_L as we decrease the number of the stacks. As a result, the efficiency at the pre-determined Z_L increases from 45.5% in quadruple stack to 55.4% in quasi-triple stack, and finally reaches 62.3% in quasi-double stack, even at a low V_{DD} of 2 V.

2.2.2 Gain and Phase Step Discontinuities

When the capacitors at the gate of CG FETs, M_3 and M_4, are switched in and out dynamically, there can be abrupt step discontinuities in gain and phase. Fig. 2.6 shows the simulated evolved universal terrestrial radio access adjacent channel leakage ratios (E-UTRA ACLRs) when various levels of AM and PM discontinuities are introduced. The signal used in the simulation is 20-MHz BW, 6.7 dB PAPR, QPSK LTE signal. To show the effect most effectively, the discontinuities are introduced in the highest probability power levels (~6 dB back off). From these figures, it can be concluded that one should avoid the gain step larger than 0.45 dB and phase step larger than 3° to meet -40 dBc criteria. Gain and phase discontinuities should be compensated in the analog domain since digital methods such as memory-less digital pre-distortion cannot correct for the abrupt discontinuities.

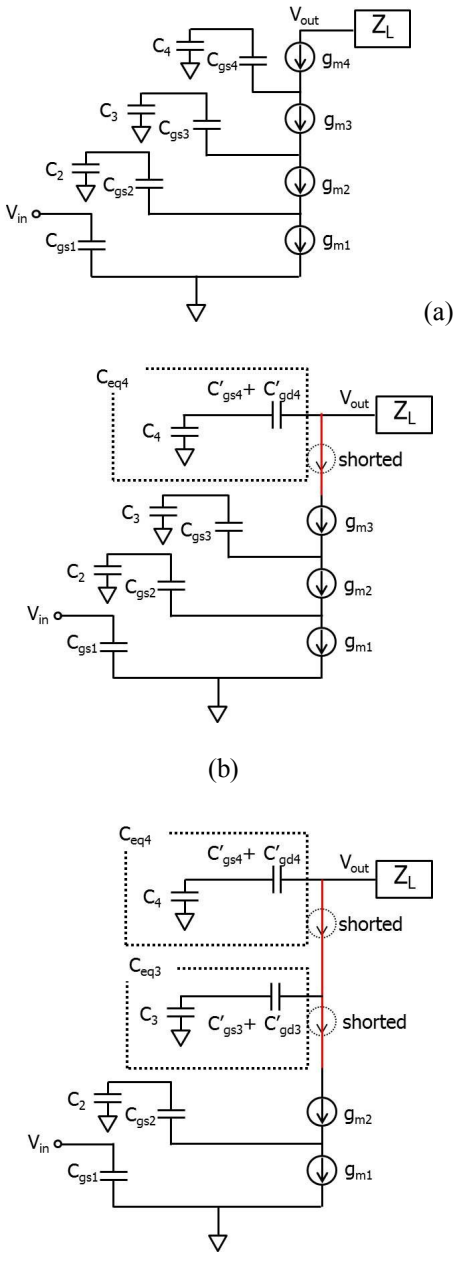


Fig. 2.7. Simplified equivalent circuit model of the power cell. (a) Quadruple-stack operation, (b) Quasi-triple stack operation and (c) Quasi-double stack operation.

To this end, we have performed analytical analysis to derive the gain and phase discontinuities as the number of FET stacks is reduced using the simplified equivalent circuit of Fig. 2.7 (a). It is simplified from Fig. 2.3 (a) by assuming that all the FETs operate in the saturation region so that R_{ds} may be assumed large enough, and C_{gd} and C_{ds} small enough to be ignored [18]. Through KCL node equations, the following voltage transfer function is derived.

$$A_{v,Q} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+\frac{j\omega C_{gs3}}{g_{m3}}\right)\left(1+\frac{j\omega C_{gs4}}{g_{m4}}\right)}. \tag{1}$$

The subscript Q in $A_{v,Q}$ represents quadruple-stack operation. This result is identical to that derived in [19], and can be used to derive the gain and phase discontinuity. If we assume that the size of each CG and CS FET is identical (i.e., $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$, and $C_{gs1} = C_{gs2} = C_{gs3} = C_{gs4} = C_{gs}$), then (1) can be simplified as follows;

$$A_{v,Q} \cong \frac{g_{m1}(r_L + jx_L)}{\left(1+\frac{j\omega C_{gs}}{g_m}\right)^3}. \tag{2}$$

where r_L and x_L are real and imaginary part of Z_L respectively.

When M_4 is bypassed for quasi-triple stack operation, the equivalent circuit of the power cell reduces to that shown in Fig. 2.7 (b). The transfer function in this mode can be easily derived from (1) by replacing $Z_L/(1+j\omega C_{gs4}/g_{m4})$ with $Z_L||(1/j\omega C_{eq4})$ as

$$A_{v,T} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+\frac{j\omega C_{gs3}}{g_{m3}}\right)\left(1+j\omega C_{eq4}Z_L\right)}$$

$$\cong \frac{g_m(r_L+jx_L)}{\left(1-\omega x_L C_{eq4}\right)\left(1+\frac{j\omega C_{gs}}{g_m}\right)^2\left(1+\frac{j\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right)}. \tag{3}$$

where C_{eq4} is the total capacitance at the gate of M_4 ($C_{eq4}=(C'_{gs4}C_4+C'_{gd4}C_4)/(C'_{gs4}+C'_{gd4}+C_4)$) The subscript T in $A_{v,T}$ represents quasi-triple stack. Likewise, the transfer function of quasi-double stacked state is

$$A_{v,D} = \frac{g_{m1}Z_L}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+j\omega C_{eq3}Z_L\right)\left(1+j\omega C_{eq4}Z_L\right)}$$

$$\cong \frac{g_m(r_L+jx_L)}{\left(1-\omega x_L C_{eq3}\right)\left(1-\omega x_L C_{eq4}\right)\left(1+\frac{j\omega C_{gs}}{g_m}\right)} \times \frac{1}{\left(1+\frac{j\omega r_L C_{eq3}}{1-\omega x_L C_{eq3}}\right)\left(1+\frac{j\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right)}. \tag{4}$$

where C_{eq3} is the total capacitance at the gate of M_3 ($C_{eq3}=(C'_{gs3}C_3+C'_{gd3}C_3)/(C'_{gs3}+C'_{gd3}+C_3)$). Again, the subscript D in $A_{v,D}$ denotes quasi-double stack. From (3) and (4), it can be seen that the gain is a function of C_3 and C_4 in double and triple stacked operation. Therefore, one can minimize gain and phase step discontinuity at the switching points by carefully determining the values of C_3 and C_4. The magnitude of the voltage gain at each state can be easily derived from (2), (3), and (4) by assuming $\omega C_{gs} \ll 1$, and the results are

$$\left|A_{v,Q}\right| \cong g_m\sqrt{r_L^2+x_L^2} \tag{5}$$

$$\left|A_{v,T}\right| \cong \frac{\left|A_{V,Q}\right|}{\sqrt{\left(\omega r_L C_{eq4}\right)^2+(1-\omega x_L C_{eq4})^2}} \tag{6}$$

$$\left|A_{v,D}\right| \cong \frac{\left|A_{V,T}\right|}{\sqrt{\left(\omega r_L C_{eq3}\right)^2+(1-\omega x_L C_{eq3})^2}} \tag{7}$$

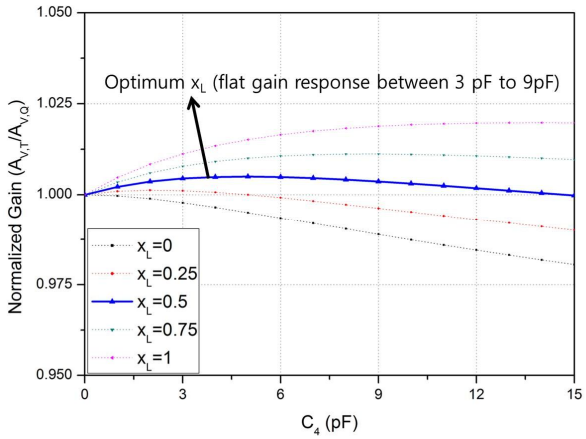


Fig. 2.8. The gain ratio between the quadruple stack and quasi-triple stack as a function of the capacitance at the gate terminal of M_4 (C_4) for different reactance of the load impedance.

To minimize the gain step during the dynamic switching of M_4, we need to understand the dependence of the gain step between $|A_{V,T}|$ and $|A_{V,Q}|$ on C_4 under various load impedance conditions. Fig. 2.8 shows $|A_{V,T}|$ normalized to $|A_{V,Q}|$ as a function of C_4. For this simulation, the frequency is 0.837 GHz, r_L is fixed at 5 Ω, $C_{gd4}+C_{gs4}$ is 15 pF while x_L is swept from 0 to 1 Ω in 0.25 Ω steps. When x_L = 0 Ω, there is no chance to equalize the gain due to M_4 switching. This means that conventional PAs such as Class AB PAs cannot support proposed dynamic switching scheme. However, since most of the high-efficiency PAs utilize finite reactance for waveform shaping as in the case of Class-F and Class-J, this does not pose any practical issues. As x_L is increased, the normalized gain shows a peak higher than 1 at a certain C_4, which means that there are potentially two C_4 values at which the gain step vanishes. Moreover, by proper selection of x_L such as x_L= 0.5 Ω, we can obtain almost flat gain response regardless of C_4. The choice of x_L is thus a trade-off between the efficiency and the linearity. In this work, we have chosen x_L of 2.7 Ω to achieve almost no gain step while compromising the

efficiency by 2.2%. The gain step discontinuity between quasi-triple and quasi-double stacks is also minimized following the same method.

The phase of the voltage transfer function at each stack operation is derived using (2), (3), and (4) as follows.

$$\angle A_{v,Q} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - 3\tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) \tag{8}$$

$$\angle A_{v,T} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) \tag{9}$$

$$\angle A_{v,D} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega C_{gs}}{g_m}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) - \tan^{-1}\left(\frac{\omega r_L C_{eq3}}{1-\omega x_L C_{eq3}}\right) \tag{10}$$

It can be found from (9) that changing the gate capacitance by partially floating C_4 during stack switching will cause abrupt phase discontinuity. The amount of phase discontinuity during the M_4 switching is

$$\Delta\angle A_{V,T} = -\tan^{-1}\left(\frac{\omega r_L C_{eq4}}{1-\omega x_L C_{eq4}}\right) + \tan^{-1}\left(\frac{\omega r_L C'_{eq4}}{1-\omega x_L C'_{eq4}}\right) \tag{11}$$

where C'_{eq4} is equivalent gate terminal capacitance of the M_4 after a portion of C_4 is disconnected from the ground. Because ωC_{eq4} is much lower than unity in most cases, we can use $\tan^{-1} x \cong x$ approximation to simplify (11) as

$$\Delta\angle A_{V,T} \cong \tan^{-1}\left(\omega r_L\left(C'_{eq4} - C_{eq4}\right)\right). \tag{12}$$

Likewise, the step discontinuity in quasi double state can be derived in the same way by using (10).

$$\Delta\angle A_{V,D} \cong \tan^{-1}\left(\omega r_L\left(C'_{eq3} - C_{eq3} - C'_{eq4}\right)\right). \tag{13}$$

The phase step discontinuity during M_4 switching is calculated to be –5.26˚ using Eq. (12) while that during M_3 switching is –6˚ using Eq. (13).

The phase step discontinuity is compensated in this work by changing the shunt capacitance in the input matching network instead of changing the capacitance of the load matching network since the latter results in the degradation in the overall PA efficiencies. The detailed circuit design is presented in the next section.

2.3 Design and Implementation

2.3.1 Power Amplifier Design

Fig. 2.9 is the complete circuit schematic of the proposed two-stage RF PA. The unit FET size in the power cell is 9.6-mm and that of the driver stage is 2-mm. Miller capacitors are inserted between the drain and source node of CG FET in the power cell to provide appropriate second harmonic termination [6], [20]. Two comparators, A_3 and A_4 turn on and off the switches, S_{41}, S_{42} and S_{31}, to change the total capacitance loading at the gate terminals of M_3 and M_4. The FET size used for S_{41}, and S_{42} is designed to be 1-mm, and that for S_{31} is 0.5-mm, considering on-state resistance and off-state capacitance. Instead of using the minimum gate length of 0.32-μm allowed by the foundry process, the gate length of S_{41} and S_{42} is extended to 1.4-μm while that of S_{31} to 0.8-μm to avoid the device breakdown due to large voltage swing. For phase step compensation, two additional switches, S_{43}, and S_{33}, are used in the input matching circuit. When these switches are turned on, the input matching circuit presents additional phase delay to compensate for the phase discontinuity at the stack switching points. The transistors used for these input switches have the gate width of 0.1-mm and the gate length of 0.8-μm.

The proposed RF PA takes two input signals, the modulated RF input signal and the envelope signal itself. The magnitude of the input envelope signal mirrors that of the dynamic drain bias since it is the same one used to generate the modulated drain bias by the ET modulator. When the magnitude of the input envelope is in its highest state, namely greater than ref_4, two comparators (A_4 and A_3) turn on all the switches, S_{41}, S_{42} and S_{31} to operate the power cell in the quadruple-stack mode. Two switches, S_{43}, and S_{33}, in the input matching circuit are turned off to

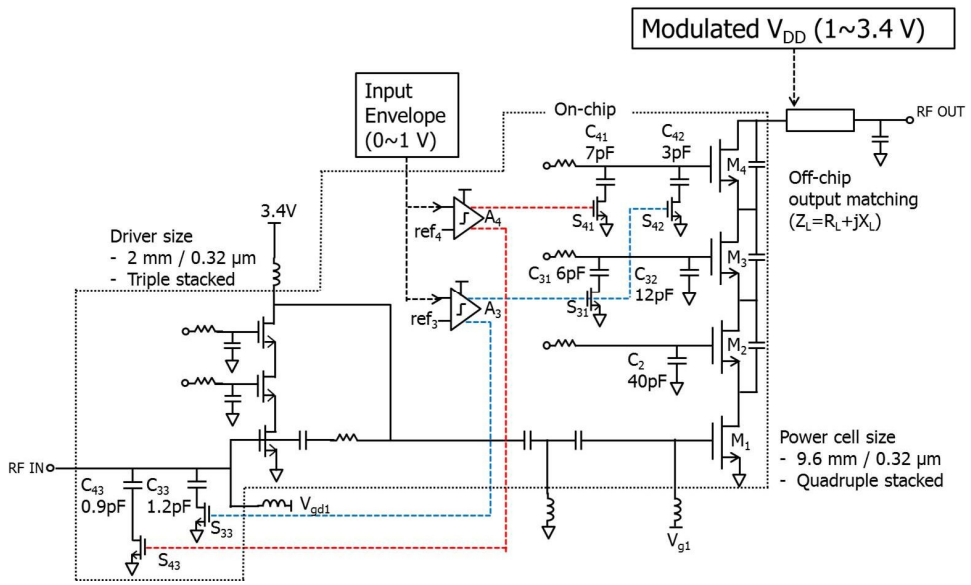


Fig. 2.9. Detailed circuit schematic of the entire 2-stage RF PA with dynamic stack control circuits.

disconnect the shunt capacitors, C_{43}, and C_{33} so that no additional phase delay is provided by the input matching circuit.

When the magnitude of the input envelope falls below a certain level, which is set by the reference voltage input (ref_4) to the comparator, A_4, the power cell is reconfigured to a quasi-triple stack. In this state, A_4 turns off S_{41} and turns on S_{43} while A_3 maintains the same state as the quadruple-stack mode. By floating C_{41}, the total capacitance loading at the gate terminal of M_4 is reduced from 10 to 3 pF, which effectively bypasses M_4 and adjusts the optimum load impedance to recover the efficiency. Besides, with S_{43} turned on, the input matching circuit is loaded with C_{43} shunt capacitor, which provides the additional phase shift to compensate for the phase step discontinuity at the switching point.

When the magnitude of the input envelope is reduced further, the power cell is reconfigured again to a quasi-double stack. In this state, the comparator A_3 turns off

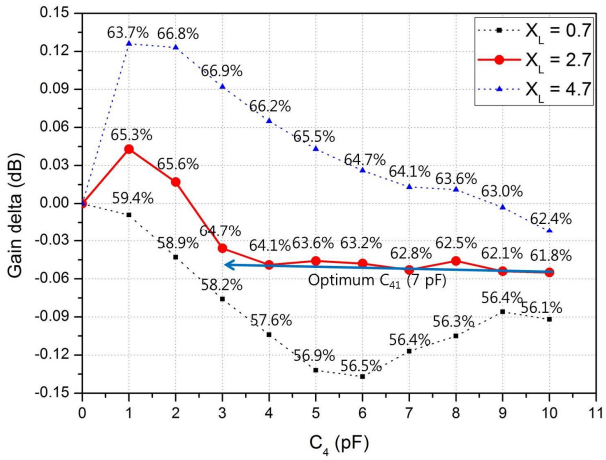
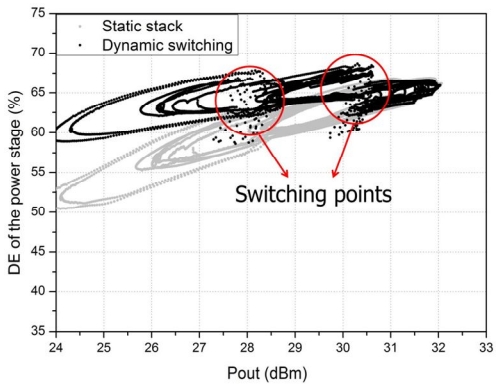


Fig. 2.10. Simulated gain step and drain efficiency as a function of C_4 for three different load reactance (X_L) values.

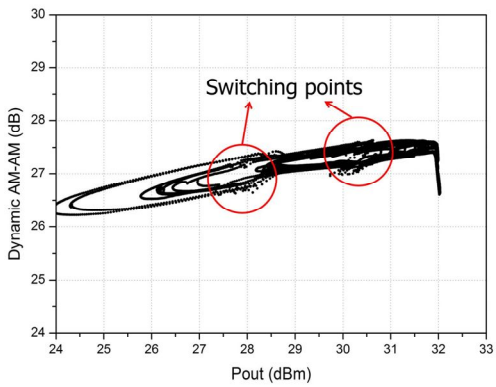
S_{42} and S_{31} while turning on S_{33}. The reduced total capacitance at the gate terminal of M_3 and M_4 effectively recovers the efficiency. In this way, optimum efficiencies can be achieved over a wide range of V_{DD}. The phase step discontinuity between quasi-triple and quasi-double stacks is compensated for by turning on the additional shunt capacitance, C_{33}, in the input matching circuit.

The values of the gate terminal capacitances of CG FETs (C_2, C_3, and C_4) are carefully chosen based on the analysis in the previous section. According to the simulation, 10 pF, 18 pF, and 40 pF for C_4, C_3, and C_2, respectively, provide the peak efficiency of 63% at 3.4 V drain bias while ensuring safe operation avoiding voltage breakdown. The gate biases of CG FETs are supplied through a resistive divider while those of CS FETs are applied through the external chip inductor for reduced memory effect.

As explained in the previous section, the choice of reactance of the load impedance (X_L) affects not only the overall efficiency but also the gain step discontinuity in conjunction with the choice of C_4. This effect has been simulated



(a)



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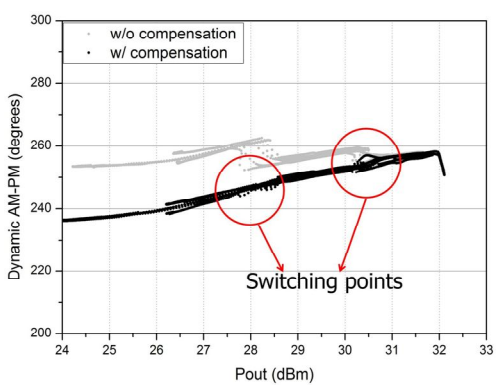


(c)

Fig. 2.11. Simulated dynamic characteristics of the entire ET PA. (a) Instantaneous drain efficiency of the power stage. (b) Dynamic AM-AM plot. (c) Dynamic AM-PM plot.

using the harmonic balance simulation of the entire circuit. Fig. 2.10 shows the simulated gain step in dB scale as a function of C_4, for three different X_L values, 0.7, 2.7 and 4.7 Ω. The drain efficiency at each point is also specified in the label. The drain bias used for the simulation is 2.8 V, which corresponds to a switching reference voltage, ref_4, of the M_4. Even if the actual values are different between the simplified analysis of Fig. 2.8 and the complete circuit simulation of Fig. 2.10, the gain step curves follow the similar characteristics, showing peaky behavior as X_L is increased. Although X_L = 4.7 Ω case shows better efficiency, we have selected a lower X_L of 2.7 Ω considering flat and minimal gain step for a wide range of C_4. This load condition provides 2.9% efficiency enhancement from 61.8% to 64.7% with negligible gain step discontinuity by floating 7 pF out of total C_4 of 10 pF. A similar simulation has been performed to find the gate terminal capacitance values to minimize the gain step discontinuity when switching from quasi-triple to quasi-double stack modes at 2.2 V. The simulated phase discontinuity during M_4 switching is –7˚ while that during M_3 switching is –9˚. These values are in good agreement with the theoretical predictions based on Eqs. (12) and (13) presented in the previous section. The capacitor values in the input matching circuit, C_{43} and C_{33}, are determined to 0.9 pF and 1.2 pF, respectively, which effectively compensate for the phase step discontinuity during dynamic stack switching. Switching the input matching capacitor may degrade the input return loss of the RF PA. However, the worst-case return loss of the RF PA even after phase step compensation is still better than 10 dB.

To verify the dynamic performance of the entire two-stage PA, envelop simulation is performed using ADS and the results are plotted in Fig. 2.11. The

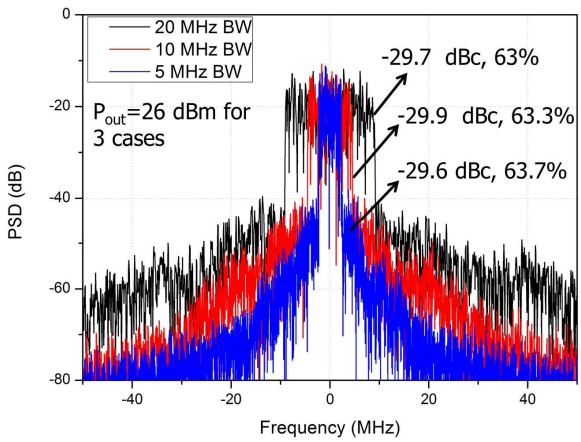


Fig. 2.12. Simulated output spectrum of the entire ET PA with various modulation signal bandwidths (5/10/20-MHz). No pre-distortion is applied for this simulation.

input signals used in the simulation are based on W-CDMA waveform at 837 MHz and only the drain voltage of the power stage is modulated by the envelope amplifier. Fig. 2.11 (a) compares the instantaneous drain efficiency (DE) of the proposed dynamic stack with that of the static stack, where all four FET stacks are used across the entire V_{DD} range. In the dynamic stack scheme, M_4 is bypassed around the output power of 30.5 dBm while both M_3 and M_4 are bypassed around 28 dBm. Dynamic stack control provides ~7% efficiency enhancement at 6 dB back-off power (32 dBm – 6 dB = 26 dBm). Fig. 2.11 (b) and (c) show the simulated dynamic AM-AM and AM-PM characteristics, the smoothness and tightness of which are critical in achieving the adequate linearity after digital pre-distortion. No abrupt gain and phase steps are observed near the switching points. Slightly wider dispersion is observed near the switching points, which is attributed to the capacitive feed-through of the switch control signal from the comparator. For reference, dynamic AM-PM without phase step correction is shown in Fig. 2.11 (c)

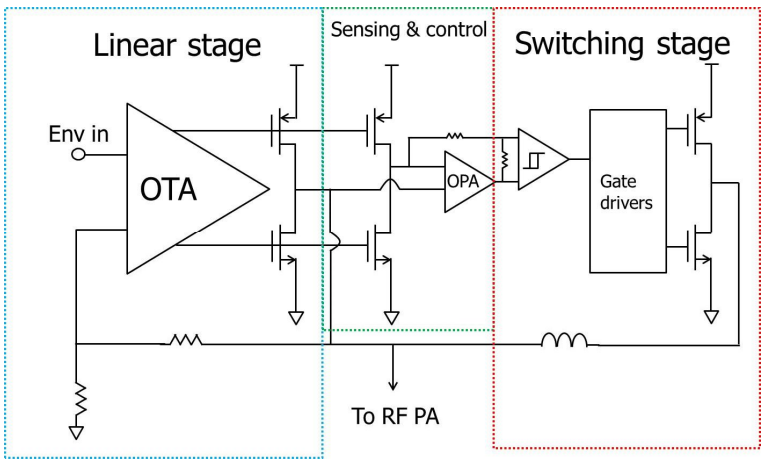


Fig. 2.13. Circuit schematic of the designed envelope amplifier.

as well. It can be seen that the use of the input capacitance switching effectively compensates for the phase step discontinuity at the switching points.

To verify the circuit performance over a wide signal bandwidth, the envelope simulation is performed to calculate the output spectrum using 6.7 dB PAPR QPSK LTE sig nals with various signal bandwidths up to 20-MHz. No linearization using digital pre-distortion is used for this simulation. Calculated ACLR degradation is negligible going from 5- to 20-MHz bandwidth as shown in Fig. 2.12. This is due to the fact that the gain and phase steps are corrected and maintained consistently over a wide switching voltage range. It is worthwhile to note that the efficiency drops slightly as the signal bandwidth increases. This is attributed to the dynamic switching loss caused by nonzero rise/fall time of the switch control signals generated by the comparator.

2.3.2 Envelope Amplifier Design

A simple envelope amplifier is also designed using the same SOI CMOS process to demonstrate the complete ET PA system. Since the main purpose of this work is

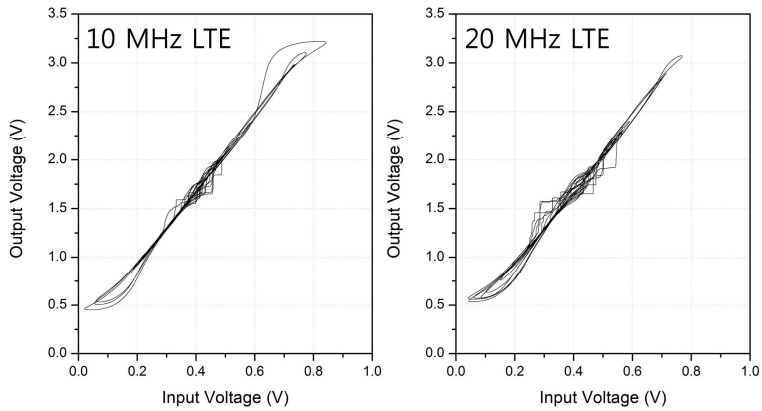


Fig. 2.14. Simulated input and output voltage response of the envelope amplifier using LTE signals with different signal bandwidths (10/20-MHz). More pronounced cross-over distortion is observed with 20-MHz signal.

to present the new ET PA concept not the envelope amplifier, the circuit is based on a widely used hybrid approach composed of a linear stage and switching stage [13], as shown in the Fig. 2.13. The gate length of all the FETs, except for output NMOS FET is 0.32-μm for standard 2.5 V I/O operations. Instead of using a cascode configuration to avoid the breakdown, the gate length of the output NMOS FETs is extended from 0.32-μm to 0.7-μm, which allows 3.4 V V_{DD} operation.

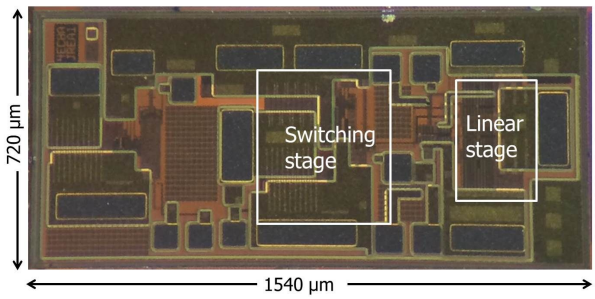
According to the small signal AC simulation, the open loop DC gain of the linear stage exceeds 50 dB under 8 Ω // 80 pF load condition. The unity gain bandwidth is about 250 MHz with 50^{o} phase margin in the same load, which is sufficient for supporting 20-MHz BW LTE operation [14]. Fig. 2.14 is the simulated input-output voltage response using 10-/20-MHz QPSK envelope signal after the delay adjustment. The crossover distortion centered around the midpoint of V_{DD} range is observed, which can cause AM and PM dispersion in ET PA system and degrade the linearity [21]. This effect is more pronounced as the signal bandwidth is increased as in the case of 20-MHz test. More sophisticated EA design is required

to further improve the linearity [15]. Measured efficiency of the envelope amplifier with fully-loaded, 10-MHz BW QPSK LTE envelope signal with 7.5 Ω resistive load is 77% [12], which is 6~9% lower than state-of-the-art dual switching envelope amplifier (~83%, [4], [16]), and multiple regulator (~86%, [5]).

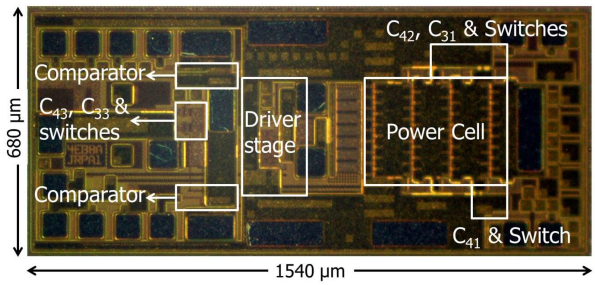
2.4 Measurement Results

Both envelope amplifier and proposed RF PA are fabricated using the same 0.32-μm SOI CMOS process. Fig. 2.15 (a) and (b) are the chip photographs of envelope amplifier and RF PA, respectively, and Fig. 2.15 (c) is the photograph of the evaluation board containing both chips on 5 cm×5 cm sized FR4 substrate. Multiple ground pads are placed to reduce the inductance of grounding wire bonds for both RF PA and EA.

Fig. 2.16 is a measured CW performance of the proposed two-stage RF PA with 837 MHz sinusoidal input signal by sweeping the DC drain bias of the power stage from 1 to 3.4 V in 0.3 V steps. The output power reaches 30.3 dBm with 64 % peak PAE. The corresponding DE of the power stage is 68.5% at 3.4 V. By reducing the number of operating stacks at 2.8 V and 2.2 V, overall PAE is boosted for a wide range of V_{DD}s, showing higher than 60% PAE down to 5 dB back-off from maximum output power. Total current consumption in the comparators is less than 1 mA with 2.5 V supply. It can be also seen from Fig. 2.16 (a) and (b) that the peak efficiencies occur near the same compression level for different stack configurations. For example, at 2.8 V V_{DD}, peak efficiencies for both quadruple stack state and quasi-triple stack state occur at P5dB. Likewise, at 2.2 V V_{DD}, peak efficiencies for three cases occur at P4.5dB. The details of the gain steps at the switching points are shown in Fig. 2.16 (c) and Fig. 2.16 (d). When the overall ET system tracks pre-defined shaping function, the gain step discontinuity between the quadruple stack state and quasi-triple stack state states is less than 0.08 dB for a wide range of V_{DD}s from 2.5 to 3.1 V. Likewise, the gain discontinuity between the quasi-triple stack state and quasi-double stack state is less than 0.04 dB for a wide



(a)



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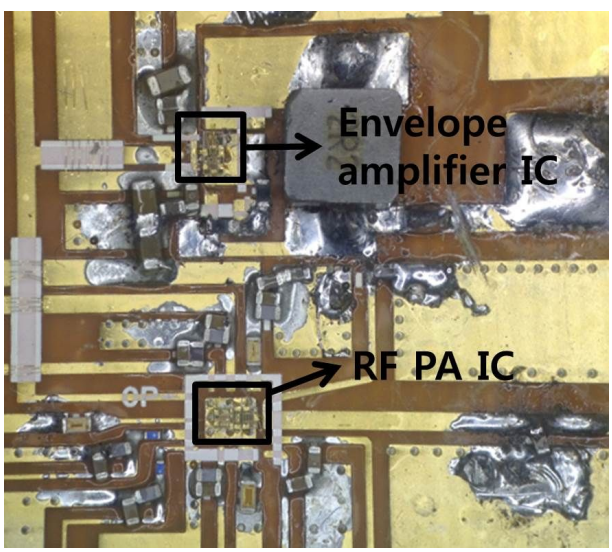
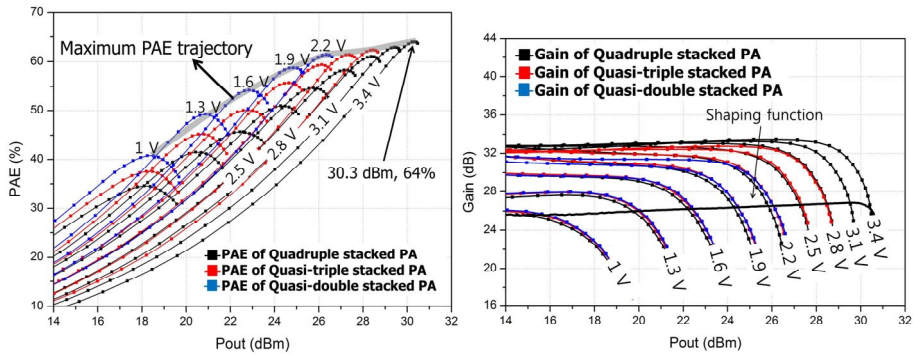
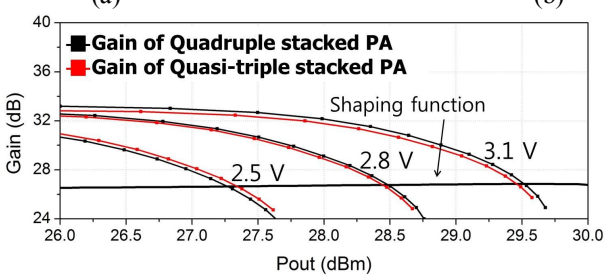


(c)

Fig. 2.15. Chip and test module photographs. Die photographs of (a) the envelope amplifier and (b) 2-stage RF PA, and (c) Photograph of the test module.



(a) (b)



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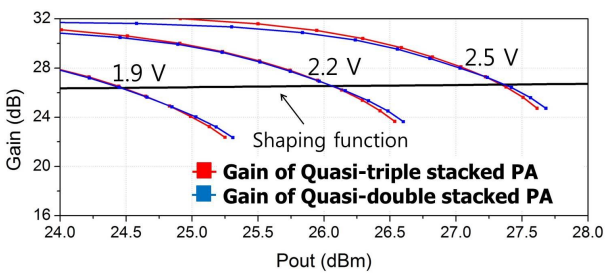


(d)

Fig. 2.16. Measured 837 MHz CW performance of the proposed 2-stage RF PA by sweeping the drain bias from 1 to 3.4 V. (a) PAE. (b) Gain. (c) Expanded gain plot to show the gain discontinuity between quadruple stack and quasi-triple stack. (d) Expanded gain plot to show gain discontinuity between quasi-triple stack and quasi-double stack.

range of V_{DD}s from 1.9 to 2.5 V. This verifies the design methodology presented in the previous section to determine the load impedance (x_L) and the switching capacitance ratio (C_{41}:C_{42}).

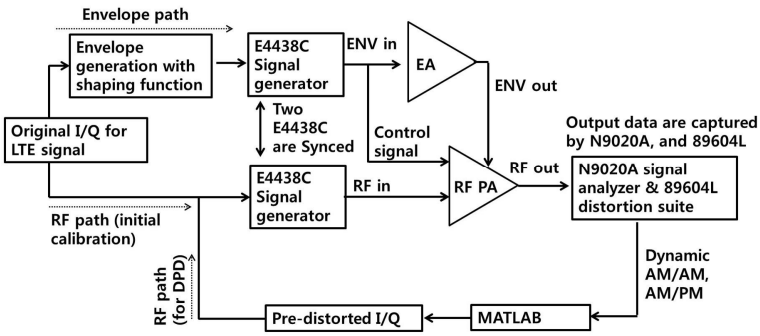
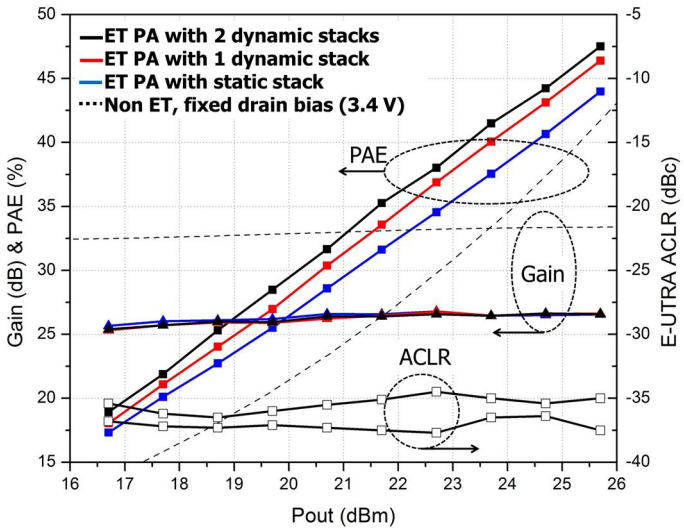


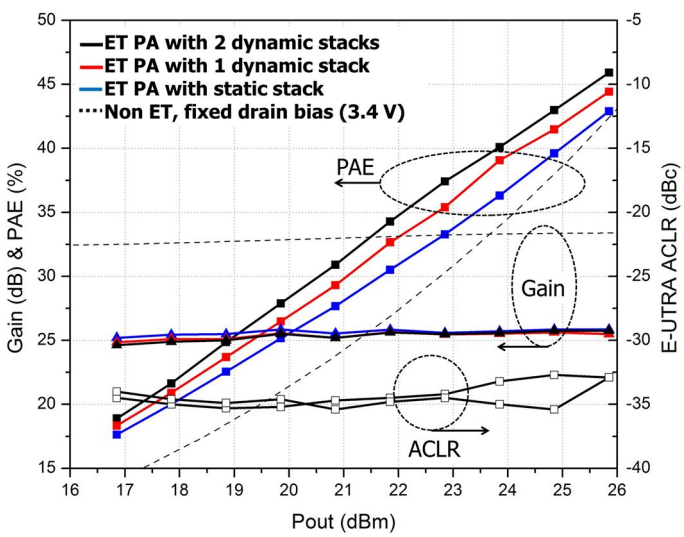
Fig. 2.17. Block diagram of the ET PA measurement setup.

Fig. 2.17 is a block diagram for ET PA system test setup. Modulated RF signal is generated by up-converting I/Q, which are sampled at 245.76 MHz. The input signal to EA and the control signal to PA are generated from the same I/Q with an exponential shaping function [15] depicted in Fig. 2.16. These signals are then downloaded to two synchronized Agilent's E4438C signal generators. The output RF signal of the ET PA is captured by Agilent's N9020A signal analyzer, and then 89604L distortion suite is used to measure the dynamic AM-AM and AM-PM characteristics as shown in the Fig. 2.17. Once the output data is read from signal analyzer, the pre-distorted I/Q is generated by MATLAB. Since iso-gain shaping function is used to flatten the gain of ET PA, the order of the polynomial used for gain pre- distortion is limited to 3. On the other hand, 9th-order polynomial is employed for phase pre-distortion since AM-PM distortion in the top 20 dB power range is as high as 20°. The pre-distorted I,Q is then downloaded back to the RF signal generator for testing with pre-distortion.

Fig. 2.18 shows the measured performance of the overall ET PA system using fully loaded LTE signals with bandwidths of 10- and 20-MHz. QPSK-modulated LTE signal is centered at 837 MHz and shows a PAPR of 6.7 dB with 0.01%



(a)



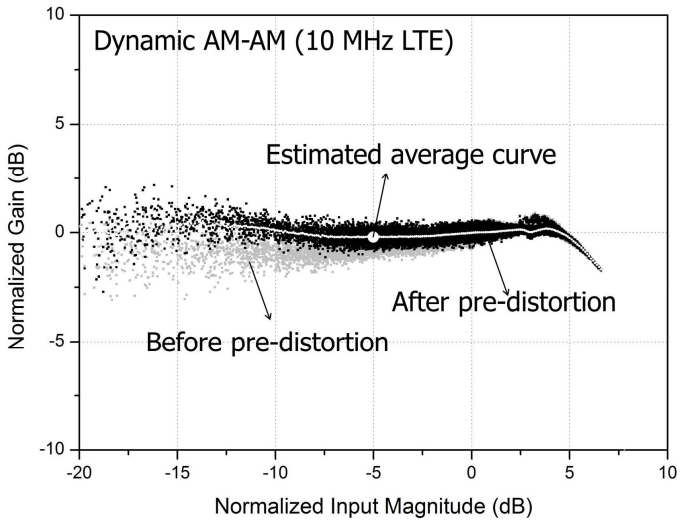
(b)

Fig. 2.18. Measured performance of the dynamic stack-controlled ET PA in comparison with static stack and partially stack-controlled PA using (a) 10-MHz LTE and (b) 20-MHz LTE signals. Non-ET PA data is also shown as a reference.

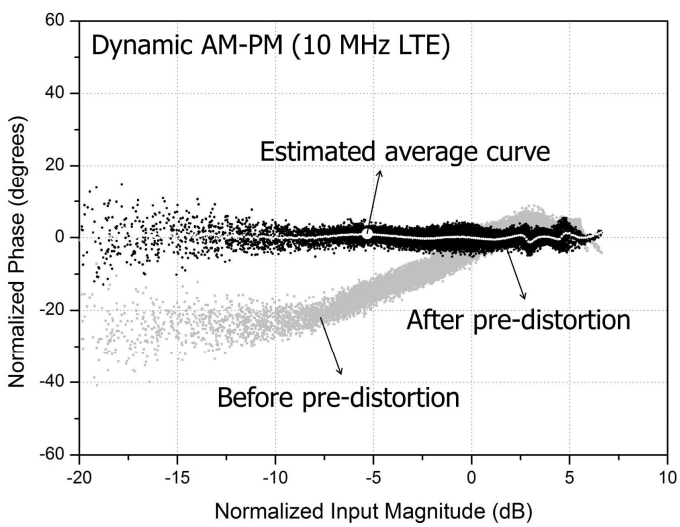
probability. The measured PAE includes the power consumption from the envelope amplifier, the driver stage and the control circuit as well as the loss from the load matching network, whereas DE of the power stage excludes the power consumption of the driver stage. To investigate the efficiency enhancement effect

of the proposed power cell, four different cases are compared, an ET PA with 2 dynamic stacks, an ET PA with 1 dynamic stack, an ET PA with static stack PA, and a non-ET PA with a fixed bias of 3.4 V. Since the peak efficiencies occur at the same compression point for all three stack configurations, it is fair to use the same shaping function to compare the overall ET PA efficiency. For 10-MHz LTE case shown in Fig. 2.18 (a), dynamic stacking provides 3.5% PAE improvement at the maximum linear output power of 25.7 dBm, resulting in 47.5% PAE and 51.4% DE of the power stage with 26.6 dB gain. The measured E-UTRA ACLR after digital pre-distortion is –35 dBc, and EVM is 3.34% for 2-dynamic stack control. Both E-UTRA ACLR and EVM show sufficient margin against system requirements. Proposed ET PA is also tested using 20-MHz LTE signal to verify wideband operation as shown in Fig. 2.18 (b). In 20-MHz LTE testing, PAE and DE at the maximum linear output power of 25.9 dBm is 45.9%, 50.8% respectively with 25.8 dB gain, which is 3% higher than static- stack ET PA. The measured E-UTRA ACLR after digital pre-distortion is –33 dBc, and EVM is 2.81%. The degraded ACLR for 20-MHz LTE signal is mainly attributed to the pronounced cross-over distortion of the EA with larger signal bandwidth. (see Fig. 2.14)

The PAE gap between 10-MHz and 20-MHz LTE for 2 dynamic stack control is 1.6%, which is slightly higher than the gap of the static-stack case (1.1%). This is attributed to non-zero rise/fall time of the comparator, as explained in Sec. III-A. This can be improved by employing deep-submicron CMOS process for faster switching.



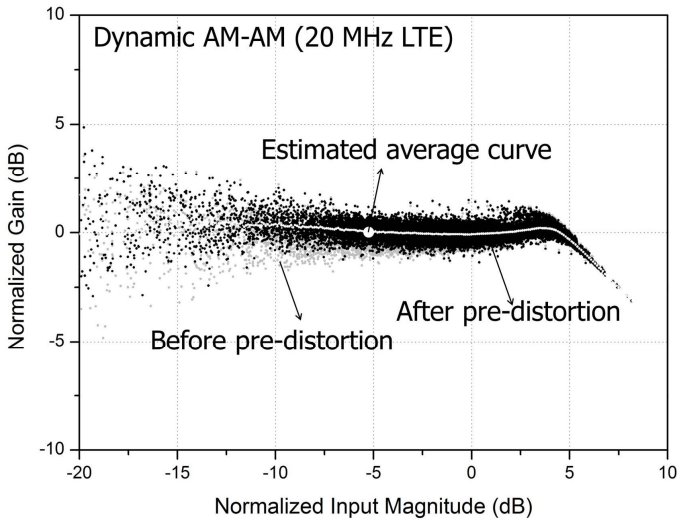
(a)



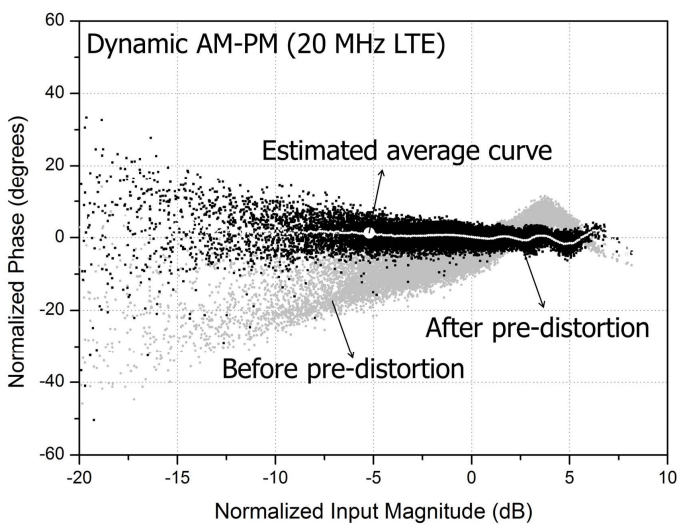
(b)

Fig. 2.19. Measured dynamic characteristics of the ET PA using 10-MHz LTE signal at 25.7 dBm output power. (a) Dynamic AM-AM. (b) Dynamic AM-PM.

Further investigation of the linearity impact due to dynamic switching has been performed by measuring dynamic AM-AM/AM-PM characteristics of the ET PA after digital pre-distortion using 10-MHz (Fig. 2.19) and 20-MHz LTE (Fig. 2.20) signals. The curves showing the statistical average at each power level is also



(a)



(b)

Fig. 2.20. Measured dynamic characteristics of the ET PA using 20-MHz LTE signal at 25.9 dBm output power. (a) Dynamic AM-AM. (b) Dynamic AM-PM.

shown with white dots to clearly reveal the step discontinuities, if any. As shown in Fig. 2.19 (a) and Fig. 2.20 (a), the gain step discontinuities are contained to less than 0.1 dB for both signal bandwidths. Phase step discontinuities are effectively compensated to less than 2° for both signal bandwidths as shown in Fig. 2.19 (b),

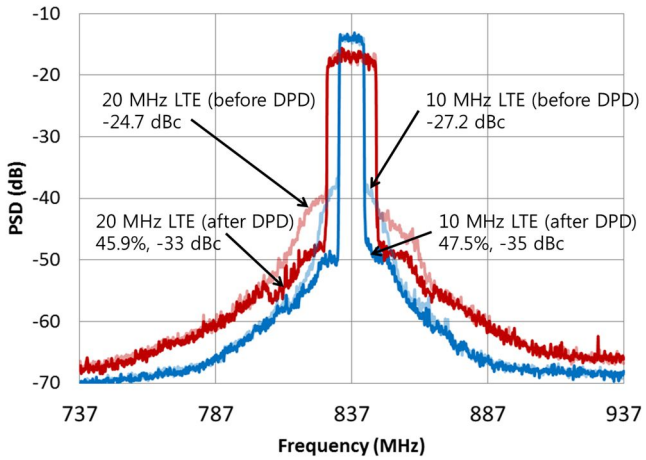


Fig. 2.21. Measured output power spectrum of the entire ET PA with dynamic stack control using 10-MHz and 20-MHz LTE signals

and Fig. 2.20 (b). Fig. 2.21 is the output spectrum of the entire ET PA system with 10- and 20-MHz BW LTE signals measured with 200 MHz span. Compared with the static-stack case, the out-of-band noise increases from –131 dBm/Hz to –128.6 dBm/Hz when M_4 is switched in and out due to the additional quantization noise and dynamic effects.

Table 2.1 is a comparison table of the state-of-the-art ET PAs for mobile LTE terminal. Without any efficiency enhancement techniques in the envelope amplifier and crest factor reduction techniques, our work shows overall system efficiencies comparable with the state-of-the-art ET PAs using dual switcher ([4], [16]), and AC-coupled multilevel regulators ([5]). In particular, the power stage efficiency demonstrated in our work is the highest among the reported silicon-based PAs. It is also worthwhile to note that the PA of this work operates with an envelope amplifier with a maximum voltage of 3.4 V instead of 5 V as in the case of [4], [8], [9], and [10], which means that the ET PA system can be operated directly from the battery and can thus avoid the potential issues by the boost converter.

TABLE 2.1

Performance Comparison Table of ET PA systems for Mobile LTE Terminals

Reference	[4]	[5]	[8][1]		[9][1]	[16][1]	[7]	**This work**	
Frequency (GHz)	2.535	N/A	0.7	0.7	1.85	0.782	1.71	**0.837**	**0.837**
BW (MHz)	20	10	10	20	10	10	10	**10**	**20**
PAPR (dB)	6.7	6.7	7.5	7.5	7.5	6.6	7.44	**6.7**	**6.7**
PA Technology	GaAs HBT	N/A	SiGe HBT	SiGe HBT	0.18-μm CMOS	0.35-μm SOS CMOS	GaAs HBT	**0.32-μm SOI CMOS**	**0.32-μm SOI CMOS**
P_{out} (dBm)	28.3	26.4	27.6	27.4	26.5	29.3	28	**25.7**	**25.9**
Overall system PAE (%)	48	39	36.4 37.1[2]	35.6 36.3[2]	34.1 37.9[2]	50.1 50.6[2]	44.3	**47.5** **(44)[3]** **51.4[4]**	**45.9** **(42.9)[3]** **50.8[4]**
E-UTRA-$_{ACLR}$ (dBc)	–41.4	–37.3	N/A	N/A	–34.2	–46.5	–35.1	**–35**	**–33**
V_{DD} (V)	5.5	3.8	5	5	5	N/A	5	**3.4**	**3.4**

[1]: single stage RF PAs

[2]: estimated DE

[3]: PAE of the static stack ET PA

[4]: Measured DE of the power stage

2.5 Conclusions

In this work, we have developed a new concept of dynamic stack control to enhance the efficiencies of CMOS stacked FET PAs for low-voltage ET operation. The potential issues due to the dynamic stack control have been identified as the gain and phase step discontinuities, and the circuit designs to compensate for the step discontinuities are developed using the detailed circuit analysis.

A two-stage dynamic stack-controlled PA is designed and fabricated using SOI CMOS process for operation at 837 MHz. CW characterization shows that the dynamic stack-controlled PA maintains PAEs higher than 60% down to 5 dB back-off from the maximum output power. To verify the linearity impact from dynamic stacking, dynamic AM-AM and AM-PM have been measured, which showed negligible gain and phase steps at the stack switching points. Full LTE characterization is performed using fully loaded LTE signals with a PAPR of 6.7 dB and signal bandwidths of 10- and 20-MHz. With 10-MHz LTE signals, dynamic stacking provides 3.5% PAE improvement over the static stack at the maximum linear output power of 25.7 dBm, resulting in 47.5% PAE with 26.6 dB gain. DE of the power stage is as high as 51.4%. 20-MHz LTE test shows that the proposed PA is capable of handling wideband signals.

Even if the measured efficiency of the EA is lower than the state-of-the-art EA results, the measured overall system efficiency with 3.4V supply is comparable with those reported using GaAs HBTs with 5 V operation, which clearly demonstrates the advantages of the proposed concept.

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Chapter 3

A Linear DPD-Less CMOS Envelope Tracking RF Power Amplifier with Integrated Phase Linearizer for LTE-Advanced Applications

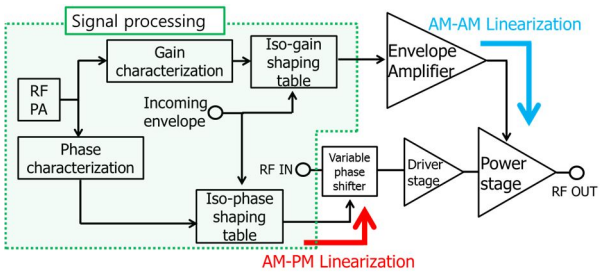
3.1 Introduction

Modern mobile phones demand highly efficient RF power amplifier (RF PA) to extend the battery life. However, designing a highly efficient RF PA for modern communication systems faces technical challenges due to the stringent linearity requirement, which is of the regulatory nature and cannot be compromised. In particular, the PA efficiency may suffer considerably for the modern long term evolution (LTE) standards since they typically employ higher-level modulation schemes, resulting in a high peak to average power ratio (PAPR) of the transmit signals. An RF PA biased at a fixed collector/drain voltage would then require a large power back off to meet the linearity requirement at the peak power. At the average output power, the PA efficiency degradation is inevitable. To overcome this problem, various efficiency enhancement techniques, such as Doherty[1], out-

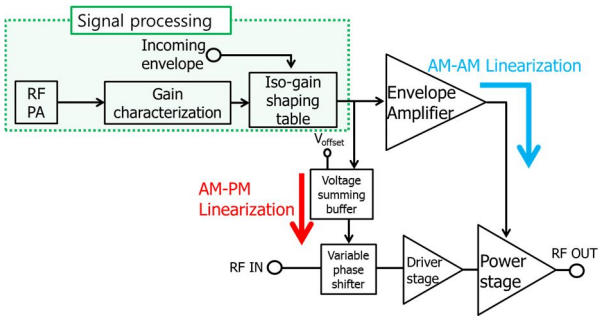
phasing[2], and envelope tracking (ET) have been investigated, among which ET techniques have been most widely used for the practical mobile phones [3]-[16].

Most of the published ET PAs for mobile LTE applications employ digital pre-distortion (DPD) to linearize the distortion generated by the transistors and supply modulation [3]-[8]. For example, 20-MHz BW LTE ET PA system is demonstrated in [3] using GaAs HBT RF PA and CMOS envelope amplifier (EA) showing –49 dBc adjacent channel leakage ratio (ACLR) with DPD. An ET PA system with SiGe HBT RF PA and EA has also been presented in [4], showing evolved universal terrestrial radio access ACLR ($\text{E-UTRA}_{\text{ACLR}}$) of –44 dBc with DPD. DPD linearization is also instrumental in linearizing CMOS ET PAs [5]-[7]. Unlike the HBT cases, the CMOS ET PA often suffers from significant AM-PM distortion during the ET operation due to the nonlinear junction capacitance and relatively large knee voltage. For example, with only AM-AM correction using iso-gain envelope shaping, the CMOS ET PAs show $\text{E-UTRA}_{\text{ALCR}}$ worse than –30 dBc while the application of AM-PM DPD improves $\text{E-UTRA}_{\text{ALCR}}$ to better than –33 dBc for fully-loaded 20-MHz LTE signals [5],[6].

LTE standards are evolving to support higher uplink speed. According to the 3rd generation partnership project (3GPP) LTE-advanced (LTE-A) specification Rel. 12 [17], the PAs are now required to meet various uplink carrier aggregation scenarios including the intra-band contiguous carrier aggregation (CA), where two LTE component carriers (CCs) are aggregated to expand the maximum operating bandwidth from 20- to 40-MHz. DPD can incur several system-level issues when handling wideband signals [9]. For example, the pre-distorted input signal to the PA is spread over excessively wide frequency spectrum, which prevents the use of



(a)



(b)

Fig. 3.1. Block diagram of the CMOS ET PA system with a phase linearizer. (a) Our previous work [9], which requires two shaping tables. (b) The proposed method, which requires only a single shaping table. The control signal for variable phase shifter is internally generated by the voltage summing buffer.

the input Tx filters, which can in some cases lead to unwanted Rx sensitivity degradation. In addition, wideband DPD consumes large amount of dc power due to the high-speed digital signal processing. To avoid these issues and prepare for future communication standards using even wider bandwidth signals, it is preferred to develop a linear ET PA system that does not rely on DPD for linearization.

In our previous work [9], we have proposed a DPD-less ET system based on dual shaping tables. It has demonstrated successful compensation of AM-AM and AM-PM distortions of CMOS PAs using 40-MHz BW LTE compatible signals. The block diagram of the previous work is shown in the Fig. 3.1 (a). On top of the iso-gain shaping, a separate iso-phase shaping table is used to generate a control signal

to the variable phase shifter to compensate for AM-PM distortion. Unlike other conventional methods relying on DPD and/or feedback loops, the proposed method has the potential of operating with wideband signals. Nonetheless, this technique requires additional calibration steps to calculate iso-phase shaping table, which may be an additional burden barring practical application to the mobile handsets.

In this work, we propose a DPD-less ET PA system based on a single shaping function. An iso-gain shaping function, which corrects AM-AM distortion, internally generates a control signal to the phase linearizer using an integrated voltage summing buffer so that both AM-AM and AM-PM linearization can be performed using a single calibration step (see 1 (b)). When tested with 40-MHz BW LTE-A signals, the fabricated DPD-less ET PA shows 37% overall system PAE with –33 dBc CA E-UTRA$_{ACLR}$.

This paper is organized as follows. Section 3.2 introduces operation principle of the proposed phase linearizer. In Section 3.3, the detailed circuit design of the two-stage CMOS RF PA with the phase linearizer is presented together with the wideband simulation results. Section 3.4 presents the measurement results of the implemented ET PA system with various LTE-A and LTE signals. Finally, this paper ends with conclusions in Section 3.5

3.2 Phase Compensation Circuit

Fig. 3.2 (a) is the simplified circuit schematic of the power stage PA used in our circuit. It is based on a triple-stacked structure using the SOI CMOS FETs with a gate length of 0.28-μm and width of 10-mm. The simulated CW gain and phase are plotted in Fig. 3.2 (b) as the drain biases (V_{DD}s) are swept from 1 to 3.4 V in 0.4 V steps. If we assume that the gain of the CMOS ET PA follows pre-defined 12 dB-gain shaping function (iso-gain shaping function) during ET operation as depicted in the Fig 2 (b), the corresponding AM-PM distortion will exceed 15°. This is mainly attributed to the nonlinear junction capacitance and relatively large knee voltage (~ 0.8 V) of the CMOS FETs. Fig 3 (a) and (b) are the intrinsic C_{gd} and C_{gs} of the 1-mm/0.28-μm NMOS FET extracted from measured S-parameters across the entire V_{gs} and V_{ds} bias voltages. C_{gd} and C_{gs} trajectories of the M_3 under the ET operation are also plotted in these figures to investigate the effect of C_{gd3} and C_{gs3} nonlinearities. From these figures, we can notice that when the dynamic drain bias is reduced to close to the knee voltage of the transistor, the uppermost FET, M_3, enters the triode region and C_{gd3} increases sharply.

To investigate how the increased C_{gd3} affects the overall AM-PM distortion of the ET PA, we have performed analytical analysis using simplified equivalent circuit model of Fig. 3.2 (a) as shown in the Fig. 3.4 (a). In this model, it is assumed that high drain bias (3.4 V) is applied to the RF PA, so all stacked FETs are operated in the saturation region. Since the measured C_{gd} (0.031 pF/mm) in the saturation region is much smaller than C_{gs} (0.42 pF/mm) (See Fig. 3.3), C_{gd}s are not included in this model for simplicity. By applying KCL equations at each node, the following voltage transfer function is derived [5],[18].

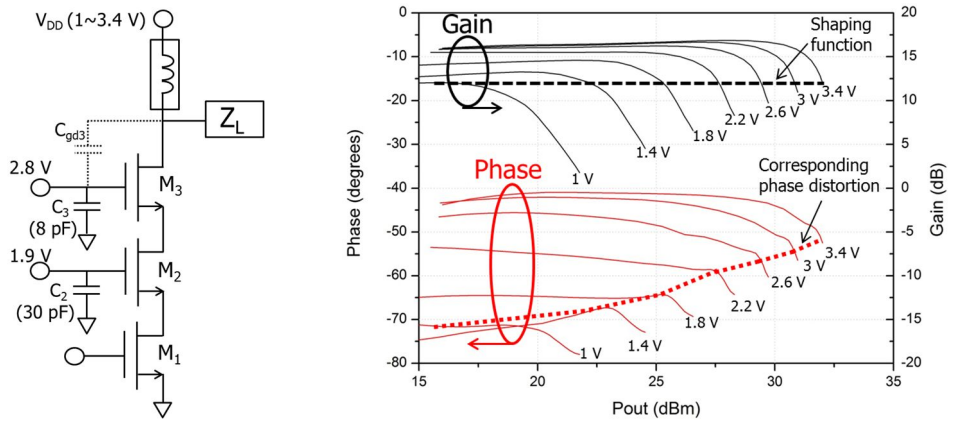


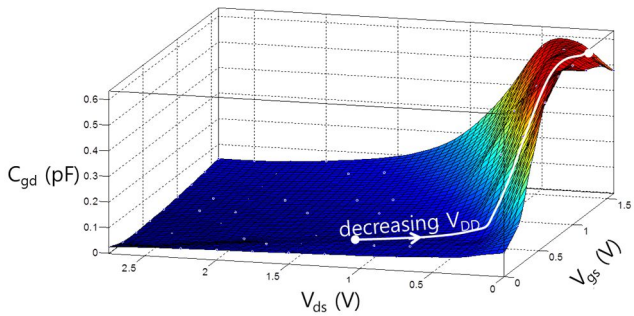
Fig. 3.2. (a) Simplified circuit schematic of the power stage PA and (b) its simulated CW gain and phase characteristics for various V_{DD}s.

$$A_{v,H} = \frac{g_{m1}(r_L + jx_L)}{\left(1+\frac{j\omega C_{gs2}}{g_{m2}}\right)\left(1+\frac{j\omega C_{gs3}}{g_{m3}}\right)} \tag{1}$$

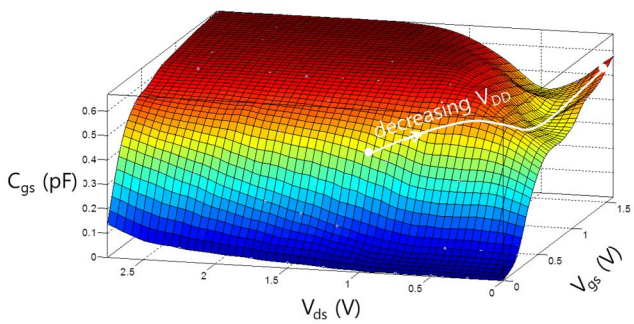
The subscript H in the $A_{v,H}$ refers to high drain bias condition, and r_L and x_L are real and imaginary part of the load impedance Z_L, respectively . The phase shift from V_{in} to V_{out} is thus

$$\angle A_{v,H} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega C_{gs2}}{g_{m2}}\right) - \tan^{-1}\left(\frac{\omega C_{gs3}}{g_{m3}}\right) \tag{2}$$

Where C_{gs}s and g_ms are the gate-source capacitances and trans-conductance of the NMOS FET in the saturation region respectively. It can be seen from (2) that most of AM-PM d istortion of the fixed-bias CMOS RF PA is attributed to the input power-dependent nonlinear C_{gs}. As reported in [19] and [20], the intrinsic C_{gs} increases as the input power increases, resulting in negative AM-PM slope in the high power region. The estimated AM-PM distortion using (2) is –7.85° while the



(a)



(b)

Fig. 3.3. Extracted intrinsic capacitance of the 1-mm/0.28-μm NMOS FET. (a) C_{gd}. (b) C_{gs}. In this figure, C_{gd} and C_{gs} trajectories of the M_3 under the ET operation are also plotted in white curves.

simulation result is –10.2°. 2.35° error is attributed to the nonlinear C_{gd}, which is not considered in (2).

The next step to calculate AM-PM distortion during the ET operation is to derive phase equation in the low drain bias condition. Generally, most of ET PAs utilizes the shaping function to prevent gain collapse at the low power region as described in the Fig. 3.2 (b). In this analysis, the minimum value of the dynamic drain bias is assumed to be 1 V, which pushes M_2, and M_3 into the deep triode while M_1 still operates in the saturation region. Therefore, the equivalent circuit can be modified to Fig. 3.4 (b) in the low drain bias condition. The voltage transfer function in this mode is

$$A_{v,L} = g_{m1}\left(Z_L \| \frac{1}{j\omega C_{eq2}} \| \frac{1}{j\omega C_{eq3}}\right) = \frac{g_{m1}(r_L + jx_L)}{\left(1-\omega x_L\left(C_{eq2}+C_{eq3}\right)\right)\left(1+j\frac{\omega r_L\left(C_{eq2}+C_{eq3}\right)}{1-\omega x_L\left(C_{eq2}+C_{eq3}\right)}\right)} \quad (3)$$

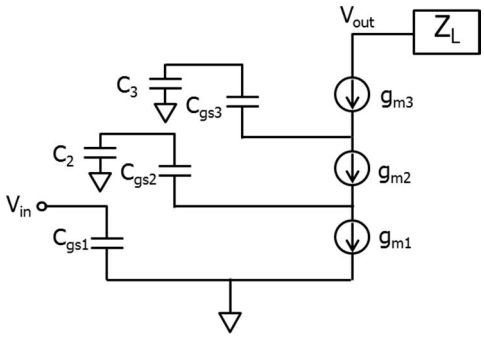
where two C_{eq}s (C_{eq2}, C_{eq3}) in the (3) are equivalent gate terminal capacitances of the M_2 and M_3 in the deep triode region respectively as shown in the Fig. 3.4 (b) ($C_{eq,i}=(C'_{gs,i}C_i+C'_{gd,i}C_i)/(C'_{gs,i}+C'_{gd,i}+C_i)$). The $'$ in the $C_{eq,i}$ equation refers internal capacitance of the NMOS FET in the deep triode region. Similarly, the subscript L in the $A_{v,L}$ refers to the low drain bias condition. In this case, the phase shift from V_{in} to V_{out} is

$$\angle A_{v,L} = \tan^{-1}\left(\frac{x_L}{r_L}\right) - \tan^{-1}\left(\frac{\omega r_L\left(C_{eq2}+C_{eq3}\right)}{1-\omega x_L\left(C_{eq2}+C_{eq3}\right)}\right) \quad (4)$$

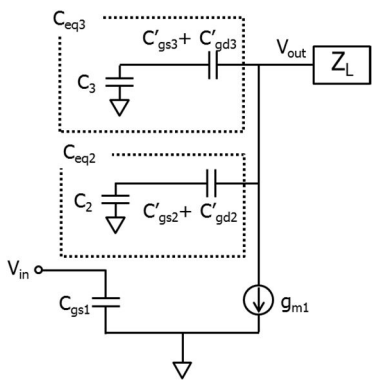
The phase difference between $\angle A_{v,H}$ and $\angle A_{v,L}$ corresponds to AM-PM distortion during the ET operation.

$$AM-PM = \angle A_{v,H} - \angle A_{v,L} = \tan^{-1}\left(\frac{\omega r_L\left(C_{eq2}+C_{eq3}\right)}{1-\omega x_L\left(C_{eq2}+C_{eq3}\right)}\right) - \tan^{-1}\left(\frac{\omega C_{gs2}}{g_{m2}}\right) - \tan^{-1}\left(\frac{\omega C_{gs3}}{g_{m3}}\right) \quad (5)$$

Since $\omega C_{gs}/g_m$ is much smaller than unity in most cases, we can conclude that the m ost of AM-PM distortion during the ET operation is attributed to the increased C'_{gd}s in the triode region. The increased C'_{gd3}, and C'_{gd2} are parallel combined with C'_{gs3} and C'_{gs2} and shunts the load impedance to the ground together with C_3, and C_2. Thus, the overall AM-PM of the RF PA is distorted in the low drain bias region, resulting in the negative phase slope as V_{DD} is reduced. The calculated AM-PM distortion using (5) is 19.5°, which is similar to the simulation result in the Fig 3.2



(a)



(b)

Fig. 3.4. Equivalent circuit model of the tripled-stacked RF PA when the drain bias is in (a) high state, and (b) low state.

(b). In this work, we have developed a phase compensation circuit to linearize the phase distortion of the power-stage PA during the ET operation.

To quantify how the phase distortion affects the overall PA linearity, we have simulated CA E-UTRA$_{ACLR}$ using 40-MHz BW, 6.53 dB PAPR intra-band contiguous carrier-aggregated signal. The modeled RF PA used in this simulation are free from memory effect and presents no gain distortion, but shows various amount of phase distortion ranging from 0° to 20°. Fig 5 is a simulated CA E-UTRA$_{ACLR}$ versus the amount of AM-PM distortion. According to this simulation, the AM-PM distortion should be less than 8.5° to meet –40 dBc ACLR and less

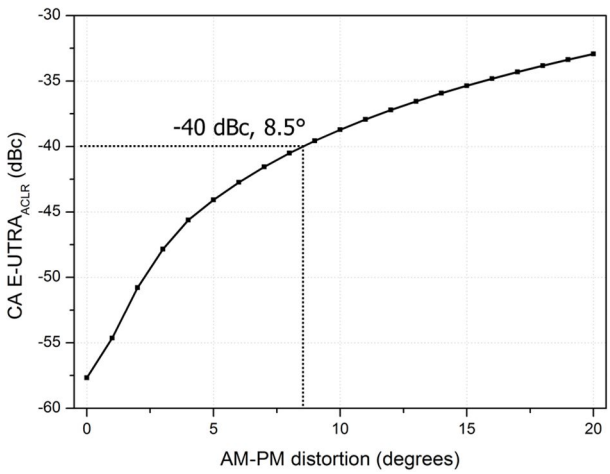


Fig. 3.5. Simulated CA E-UTRA$_{ACLR}$ of the RF PA when the various levels of AM-PM distortion is introduced. The input signal is 40-MHz BW, 6.53 dB PAPR LTE-A signal.

than 19° for –33 dBc ACLR. Moreover, if one considers the PA and ET memory effects, it will require much tighter AM-PM distortion to meet the stringent linearity specs.

To overcome this problem, a simple correction circuit (SCC) is proposed in [10], which utilizes the modulated drain bias at the output of the EA to control the capacitance of the input matching varactor. Also in [11], both common source and common gate biases of the cascode CMOS PA is dynamically controlled using adaptive bias control circuit. The main drawback of the reported linearizers is the limited operating BW since they rely on a feedback loop in the main RF signal path; due to the timing misalignment between envelope and RF signals, there can be significant timing mismatch especially for wideband operation.

Fig. 3.6 shows the operation principle of the proposed phase linearizer to flatten the AM-PM response of the ET PA. Figures 6 (a) and 6 (b) illustrates the two extreme cases of V_{DD} swing. With the iso-gain shaping applied to the ET PA, the corresponding AM-PM characteristics exhibit large distortion due to the phase

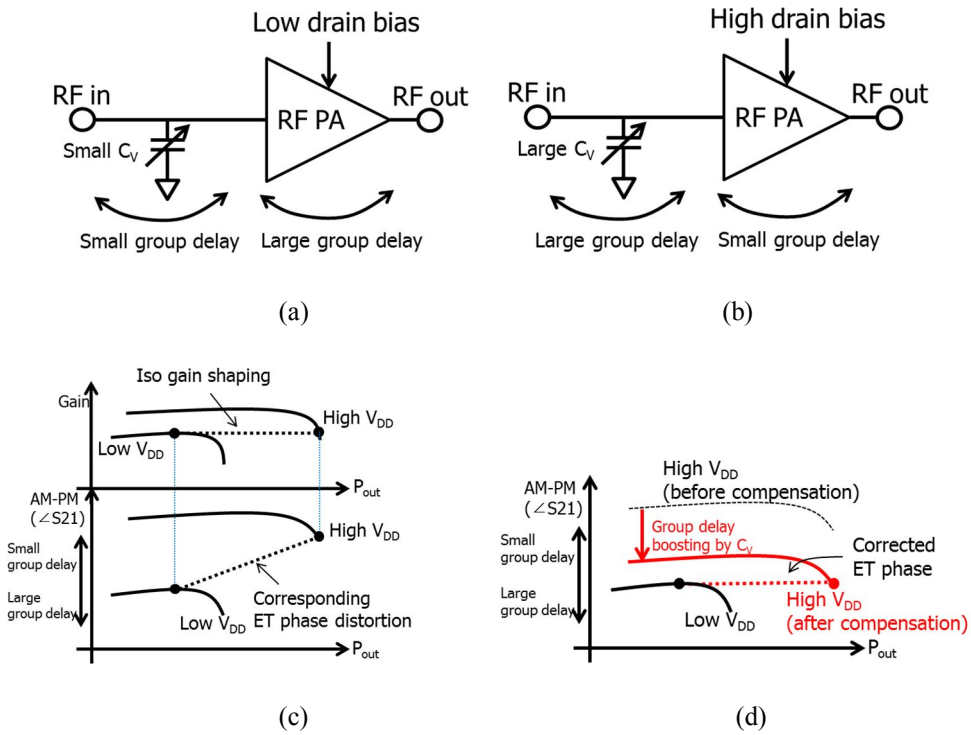


Fig. 3.6. AM-PM compensation mechanism by adjusting the capacitance of the input matching varactor. (a) Operation with low drain bias. (b) Operation with high drain bias. (c) ET gain and phase trajectory when iso-gain shaping is applied. (d) Corrected ET phase distortion by boosting the group delay using large C_V in the high drain bias region.

difference of the RF PA between low and high V_{DD}s as shown in the Fig. 3.6 (c). The phase distortion can be compensated by increasing the capacitance of input matching capacitor (C_V) to boost the group delay at high V_{DD}, as shown in the Fig. 3.6 (d). The phase shift provided by ΔC_V is

$$AM-PM_{comp} = -\tan^{-1}\left(\frac{\omega \Delta C_V R_{in} R_o}{R_{in}+R_o}\right) \quad (6)$$

where R_{in} and R_o are the input impedances of the RF PA and the signal source, respectively. If we assume that the input of the RF PA is matched to 50 Ω (R_{in}), the required ΔC_V to compensate 19.5° AM-PM distortion is calculated as 2.7 pF. In other words, the input matching network including C_V works as a "variable phase

shifter" and performs the function of an analog phase pre-distorter. The actual C_V tuning range is carefully determined by harmonic balance and envelope simulations.

The control signal to C_V is fed from the integrated voltage summing buffer, which sums up the iso-gain shaping voltage and an offset voltage (V_{offset}), as shown in Fig. 3.1 (b). V_{offset} adjusts the dc offset of the iso-gain shaped envelope signal, and can be used for tuning the overall ET PA linearity.

3.3 Detailed ET PA Design and Simulation

3.3.1 Power Amplifier Design

Fig. 3.7 is the detailed circuit schematic of the two-stage CMOS RF PA with the integrated phase linearizer. It is a two-stage design with triple-stacked FETs with a unit transistor size of 10-mm in the power stage and double-stacked FETs with a size of 2-mm in the driver stage. Stacked FETs are used to prevent the voltage breakdown for 3.4 V V_{DD} operation [18]. Miller capacitors are connected between drain and source terminals of common gate FETs (M_2, M_3) to provide appropriate second harmonic termination at the inner stacks [21],[22]. The gate terminals of the common-gate FETs are biased with resistive dividers while those for the common-source FETs are biased with the external chip inductors to minimize the memory effect.

The proposed phase linearizer is employed at the input matching network of the RF PA. It consists of a shunt inductor (L_i), a varactor (C_V), an RF bypass capacitor (C_B), and a voltage summing buffer as shown in Fig. 3.7. C_V, C_B, and L_i form an input matching network for the RF PA as well as variable phase shifter. The input RF signal (RF IN) experiences group delay that can be dynamically adjusted by the output voltage of the voltage summing buffer (V_V). To compensate for the phase deviation up to 25° at 837 MHz, C_V capacitance range should be 2.7~6 pF. A large capacitor (C_B) of 20 pF is used in series with C_V to suppress the RF voltage swing at the output node of the voltage summing buffer. It is worthwhile to note that the output impedance of the voltage summing buffer has minimal impact on the input impedance of the variable phase shifter (C_{in}) since we designed the output stage of the voltage summing buffer with small FETs. The shunt connected L_i (7.5 nH) is

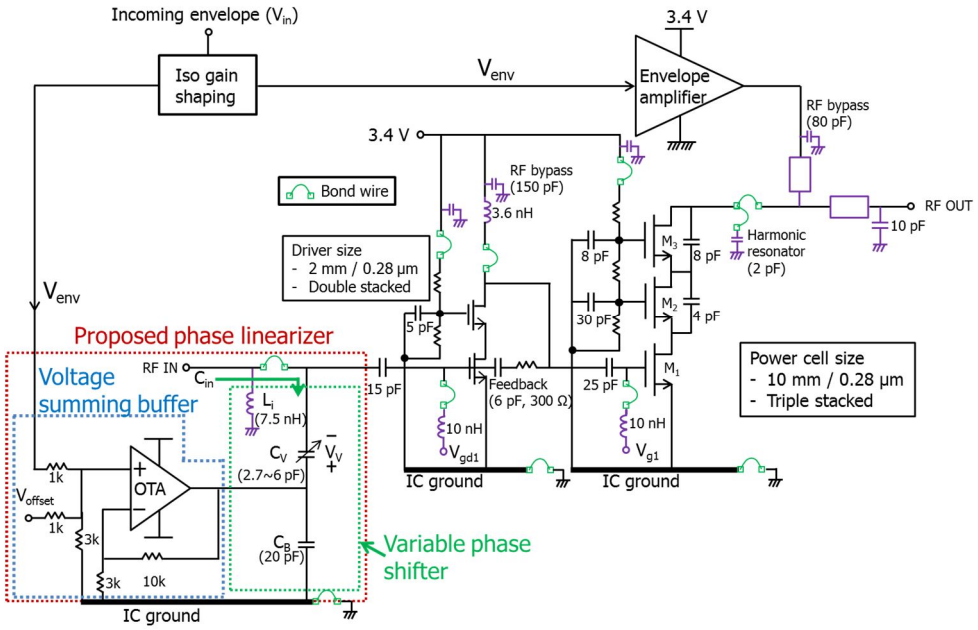


Fig. 3.7. Complete circuit schematic of the two-stage CMOS RF PA with the proposed phase linearizer. Off-chip components are indicated with purple color.

placed at the RF IN port to provide short circuit at the baseband frequencies. Since the voltage range of C_V to achieve the required capacitance variation is different from the iso-gain shaped envelope voltage range, the voltage summing buffer is used to adjust the voltage ranges. The voltage summing buffer is composed of an operational trans-conductance amplifier (OTA), a voltage summing network at the non-inverting input node (+) of the OTA, and a feedback network at the inverting input node (–) of the OTA. It takes two input signals, the iso-gain shaped envelope signal (V_{env}), which is the same as the EA input signal, and a dc offset voltage (V_{offset}). Following the KCL node equation at the + and – node of the OTA, and assuming that the OTA has ideal characteristics [23], the output signal of the OTA (V_V) is derived as follows.

$$V_V(t) = \frac{13}{7}\left(V_{env}(t) + V_{offset}\right) \tag{7}$$

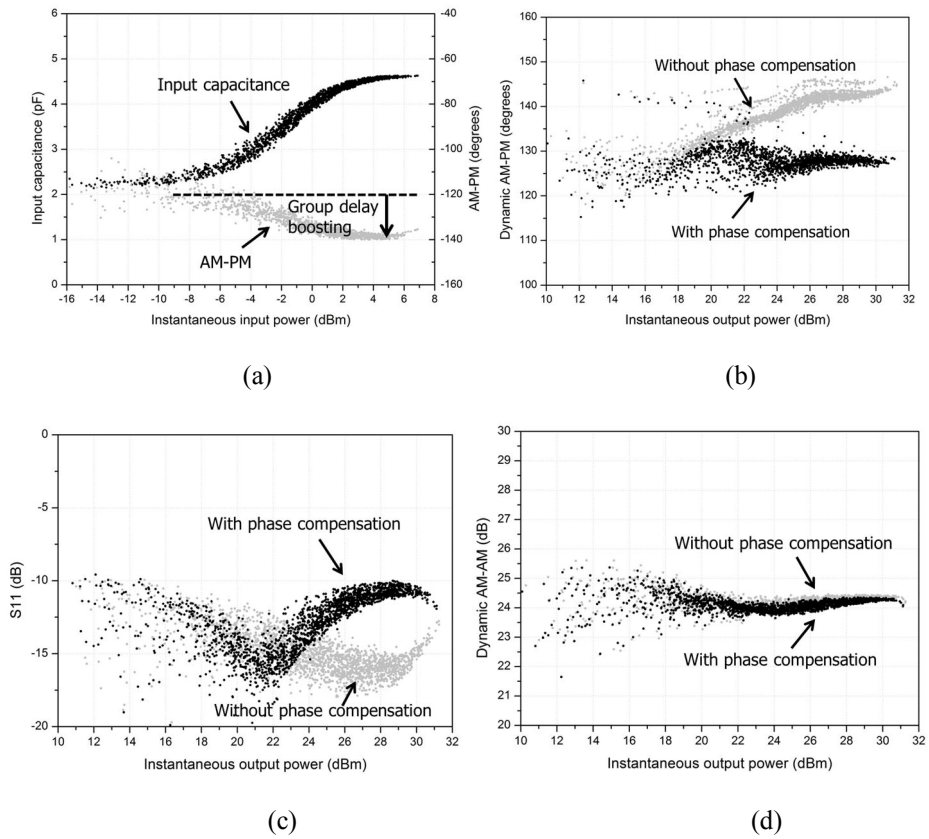


Fig. 3.8. Simulated dynamic characteristics of the ET PA with the proposed phase linearizer. (a) The input capacitance of the phase linearizer and AM-PM pre-distortion generated by the phase linearizer. (b) Dynamic AM-PM characteristics. (c) S_{11}. (d) Dynamic AM-AM of the entire PA with and without the phase linearizer.

To verify the effectiveness of the proposed phase linearizer, envelope simulation is performed in Fig. 3.8 to show the dynamic characteristics of the ET PA with the phase linearizer. The input signal used in this simulation is 20-MHz BW, 6.57 dB PAPR QPSK LTE signal centered at 0.837 GHz. An operational amplifier model provided by Keysight ADS is used to represent the EA. The gain bandwidth product (GBW) of the EA is set very high to exclude the memory effect from the EA, and V_{offset} is set at –0.75 V. A simple exponential shaping function is applied to the incoming envelope to prevent gain collapse at low power region. The simulated

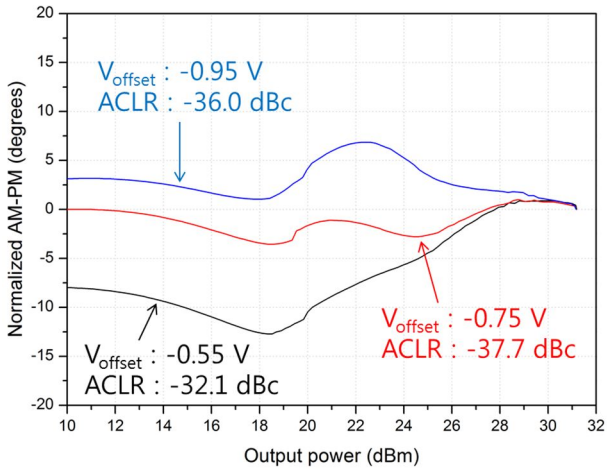


Fig. 3.9. Simulated AM-PM and E-UTRA$_{ACLR}$ of the ET PA with various V_{offset}s .

input capacitance ($C_{in} \sim C_V C_B/(C_V+C_B)$), and the AM-PM characteristics of the phase linearizer are plotted at each input power level in Fig. 3.8 (a). At the low input power region below –8 dBm, the input capacitance of the phase linearizer remains constant at ~2 pF, and the associated phase shift is almost constant. This is because the V_{env} remains almost constant at the low power region due to the envelope shaping. When the instantaneous input power exceeds –8 dBm, the input capacitance of the phase linearizer increases sharply from 2 to 4.6 pF ($\Delta C = 2.6$ pF) to boost the group delay, which decrease the phase by ~20° in the high power region. This simulation result validates the theoretical predictions based on (6), presented in the previous section. The negative phase slope of the phase linearizer compensates for the positive phase slope of the CMOS ET PA when an iso-gain shaping function is applied (see Fig. 3.6). Fig. 3.8 (b) shows the simulated dynamic AM-PM of the entire ET PA with and without the phase linearizer at 25.4 dBm output power. Without the phase compensation, severe AM-PM distortion up to 20° is observed in the top 15 dB output power range as expected. With the phase

linearizer turned on, the AM-PM variation has been reduced to less than 4° for the entire dynamic power range. As a result, the simulated E-UTRA$_{ACLR}$ is improved from –32.9 to –37.7 dBc.

AM-PM distortion of the ET PA may vary according to the bias conditions and the selected shaping functions. V_{offset} in the phase linearizer can be used as a tuning parameter to achieve the optimum ACLR performance for various AM-PM distortion cases. Fig. 3.9 is a simulated AM-PM of the ET PA with three V_{offset} voltages (–0.55, –0.75, and –0.95 V). A V_{offset} of –0.55 V results in a V_V swing range of –0.1 ~ 1.7 V, which under-compensates for the PA phase distortion. When V_{offset} is –0.75, V_V swing range becomes –0.45 to 1.6 V, which provides the optimum phase compensation, resulting in –37.7 dBc E-UTRA$_{ACLR}$. Finally, when the V_{offset} is decreased to –0.95 V, V_V swing range is lowered to –0.79 to 1.25 V, which over-compensates for the AM-PM distortion as evidenced by the negative AM-PM slope from 22 to 32 dBm.

Since the linearizer changes the capacitance (C_V) in the input matching network, the return loss of the RF PA may also be affected. To quantify this, S_{11} at each output power level is simulated as shown in the Fig. 3.8 (c). In the low power region, there is no S_{11} difference between the two cases as expected. When the instantaneous output increases above 20 dBm, the input return loss is degraded by 7 dB, but still better than 10 dB. The simulated dynamic AM-AM in both cases are also plotted in Fig. 3.8 (d), which shows that the phase linearizer does not affect AM-AM characteristics flattened by the iso-gain shaping function.

3.3.2 Bandwidth Consideration

The simulation results in the previous section have proven that the proposed phase linearizer can improve E-UTRA$_{ACLR}$ of the ET PA for 20-MHz BW LTE signals. Since the main idea of this work is to overcome the bandwidth limitation of DPD-based ET systems, we need to understand the bandwidth limitation of our approach. It is well known that the bandwidth limitation may come from the EA. Typical hybrid type EAs consisting of the linear stage and switching stage suffer from the memory effect for wideband signals due to the limited gain bandwidth (GBW) product of the linear stage. The reported GBW of the EA in 0.18-μm CMOS process is around 130 MHz [12],[13] which is not sufficient to support 40-MHz BW applications. The EA used in our work also shows a limited GBW of 178 MHz with 7.5 Ω//80 pF load. Aside from the bandwidth limitation of the EA, which is not the main scope of this work, the proposed phase linearizer can also impose the bandwidth limitation if the OTA cannot follow the signal with sufficient speed. To avoid this problem, the GBW of OTA in the phase linearizer is designed to be 230 MHz with 25 pF load, which is more than 5 times the signal bandwidth (40-MHz). To understand the bandwidth limitation coming from the phase linearizer only, we have simulated the entire ET PA system by replacing the EA with a very high speed op amp (GBW=500-MHz). Fig. 3.10 is the simulated E-UTRA$_{ACLR}$s as a function of LTE signal bandwidth at 25.4 dBm output power. 10- and 20-MHz BW signals are QPSK LTE signal with 6.53 dB PAPR, while 30- and 40-MHz BW signals are QPSK LTE compatible signals which are constructed by increasing the sampling rate of the 20-MHz BW LTE signal [9]. Calculated ACLR degradation is less than 0.5 dB as the signal bandwidth is increased from 10- to 40-

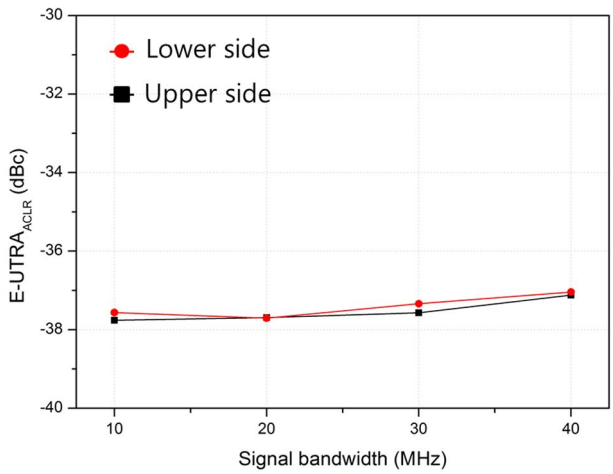


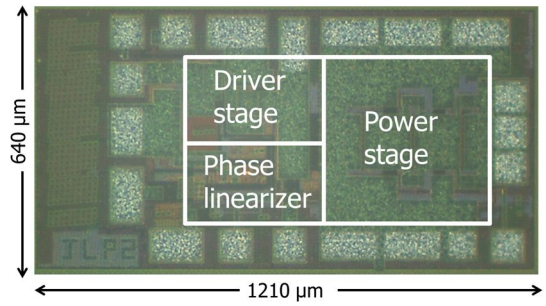
Fig. 3.10. Simulated E-UTRA$_{ACLR}$s of the ET PA as a function of signal bandwidths.

MHz. This basically shows that the phase linearizer can support wide bandwidth as long as the EA modulates the drain bias with high speed and fidelity. With further advances in the EA design, the proposed concept can potentially support LTE-A signals wider than 40-MHz.

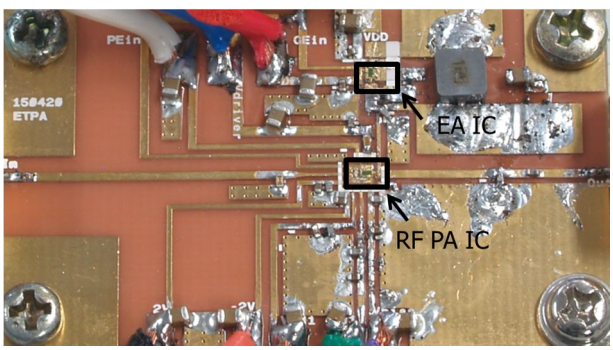
3.4 Measurement Results

A two-stage RF PA with the proposed phase linearizer is fabricated together with the EA using SOI CMOS process. The gate lengths used for the PA and EA are 0.28-μm and 0.32-μm, respectively. The EA is basically the same one developed in our previous work [5]. Fig. 3.11 (a) is the chip photograph of the two-stage CMOS RF PA with the phase linearizer, whose size is 640 μm×1210 μm including bond pads. Fig. 3.11 (b) is the photograph of the evaluation board containing both RF PA and EA chips on 5 cm×3 cm FR4 substrate (ε_r~4.6, tanδ~0.025). Off-chip output matching network composed of PCB transmission line and a shunt capacitor is used. The external inductor for the EA is 1.5 μH for 40-MHz BW operation. The measured average efficiency of the EA with 7.5 Ω resistive load using 40-MHz BW LTE-A envelope signal is plotted in Fig. 3.12. The EA shows 71.8% efficiency for 7.46 dB PAPR 40-MHz BW LTE-A envelope signal at 26.8 dBm average output power (V_{rms} = 1.9 V) with 3.4 V supply. For a 20-MHz BW LTE envelope signal, the envelope amplifier shows 78% efficiency, which is 7.8% lower than the state-of-the-art envelope amplifier [24].

The continuous wave (CW) performance of the RF PA is characterized using 0.837 GHz CW signal. The maximum PAE reaches 65.2% at 30.9 dBm output power with 3.4 V supply. The drain efficiency (DE) of the power stage is as high as 69.9% at the same output power. The current consumption in the phase linearizer is only 2 mA with 3.6 V supply rails (1.8 V V_{DD}, −1.8 V V_{SS}), which degrades the overall system PAE by 0.4% in 40-MHz BW LTE-A testing. For optimal linearity performance for 40-MHz ET operation, we apply 24.7 dB iso-gain shaping



(a)



(b)

Fig. 3.11. Chip and test module photographs. (a) Die photograph of the two-stage RF PA with the proposed phase linearizer and (b) photograph of the test module.

function with a voltage offset of 1.1 V using the exponential shaping function [3] as follows.

$$V_{DD}(t) = \beta\left(v_{in}(t) + \alpha e^{-(v_{in}(t)/\alpha)}\right) \tag{8}$$

where α is a detroughing constant to provide dc offset voltage in the low envelope region, and β is a scaling factor. For the 40-MHz test, α is set at 0.33, and β at 3.4.

Fig. 3.13 is the setup for testing the entire ET PA system. To improve the efficiency and linearity of the ET PA system, we applied the crest factor reduction (CFR) technique to the input signal using Keysight N7614B power amplifier studio software, which offers CFR algorithm, DPD linearization, and envelope signal

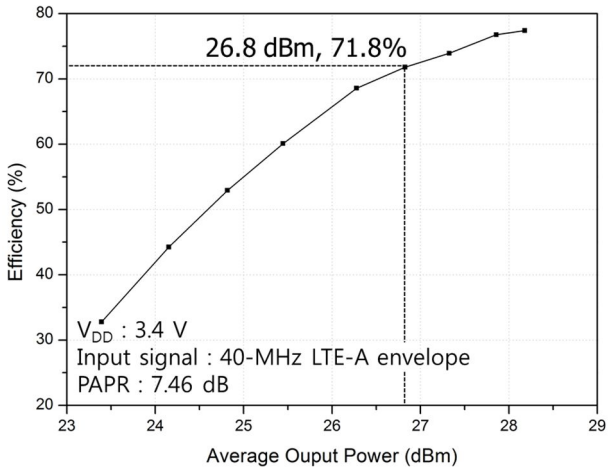


Fig. 3.12. Measured efficiency of the EA with 40-MHz BW LTE-A envelope signal

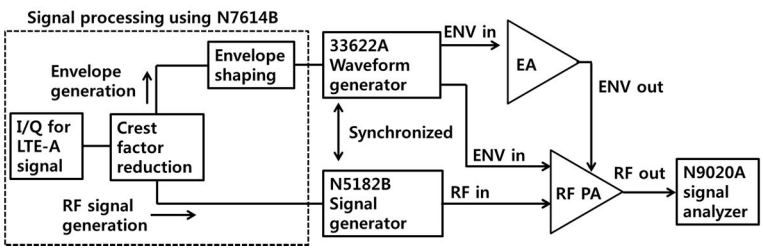


Fig. 3.13. Measurement setup for testing ET PA system

generation for ET PA characterization. The modulated RF signal and iso-gain shaped envelope signal are then generated, and downloaded to synchronized N5182B RF vector signal generator and 33622A arbitrary waveform generator, respectively. The timing alignment between RF input signal and two envelope signals for AM-AM and AM-PM compensation is performed sequentially. First, timing alignment between RF input signal and modulated drain bias is adjusted using N7614B without the phase compensation. After the AM synchronization, fine timing adjustment for PM synchronization is performed by adjusting the length of the external cables. In both cases, the optimum delay is determined by monitoring

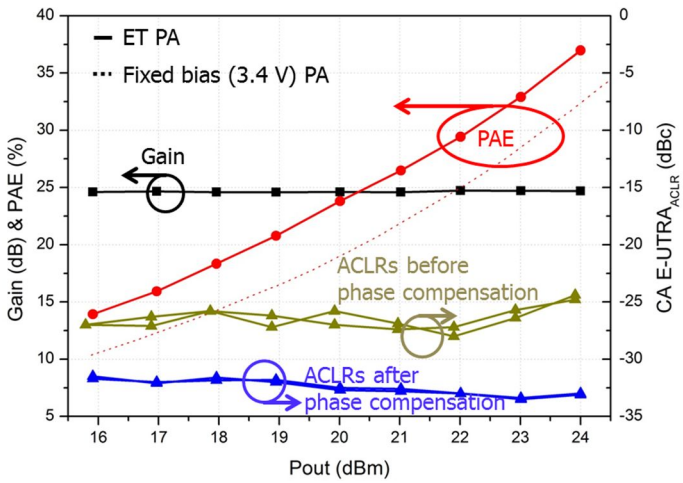
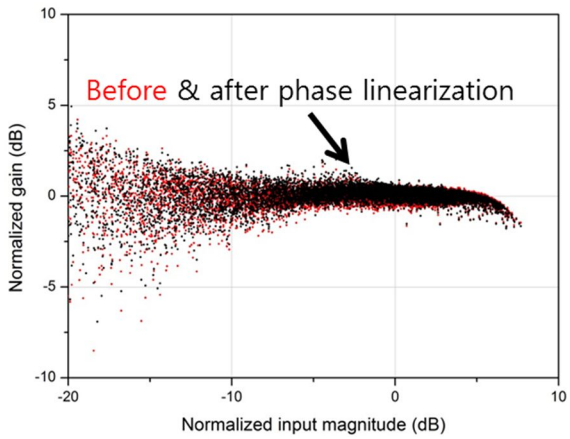


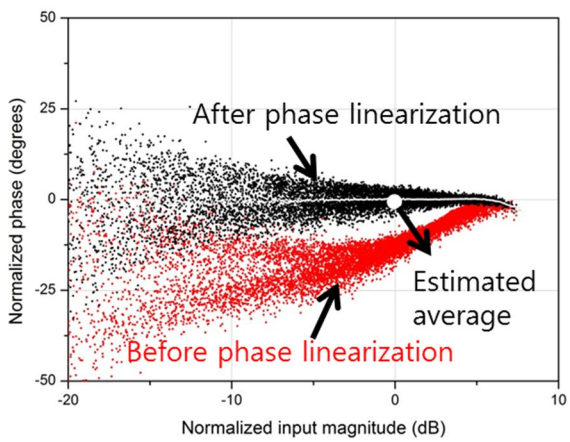
Fig. 3.14. Measured performance of the ET PA with the proposed phase linearizer using 40-MHz BW LTE-A signal (PAPR=7.46 dB) Non-ET data is also shown as a reference.

ACLR balance. The output signal of the ET PA is captured by N9020A signal analyzer to extract ACLR and dynamic characteristics.

First of all, the overall ET PA is tested with intra-band contiguous two-carrier aggregated 40-MHz BW LTE-A signal, where both lower (CC_1) and upper side component carrier (CC_2) have 20-MHz BW QPSK constellations. Since each CC has 20-MHz BW, and 100 resource blocks (RBs), i.e., fully loaded, the carrier aggregated signal has 40-MHz BW and 200 RBs. The PAPR of the resultant LTE-A signal is 8.97 dB at 0.01% probability. CFR technique is applied to reduce PAPR while compromising EVM and ACLR. A soft clipping of 2.59 dB clipping level results in 7.46 dB PAPR at 0.01%, –54.2 dBc CA E-UTRA$_{ACLR}$, and 3.36% EVM. This signal is used for the initial characterization of the fabricated PA for 40-MHz uplink CA test. Fig. 3.14 is the measured performance of the ET PA system as the output power is swept from 16 to 24 dBm. Measured overall system PAE, which includes the power consumption in the EA, RF PA and phase linearizer as well as the loss of the matching network, reaches 37% at the maximum linear output power



(a)



(b)

Fig. 3.15. Measured dynamic characteristics of the ET PA with 40-MHz BW LTE-A signal at 24 dBm output power. (a) Dynamic AM-AM. (b) Dynamic AM-PM characteristics.

of 24 dBm. The drain efficiency (DE) of the power stage is as high as 40.2%. Through iso-gain shaping, the gain is maintained to 24.7±0.1 dB. The measured PAE of the fixed bias (3.4 V) RF PA is also plotted in this figure as a reference. Since non-ET PA shows only 32.5 % at 24 dBm, it can be seen that ET provides 4.5% efficiency enhancement at 24 dBm. Even though the iso-gain envelope shaping is applied for flat AM-AM response, CA E-UTRA$_{ACLR}$ before the phase compensation is only –24.4 dBc at 24 dBm. By turning on the phase linearizer, CA E-UTRA$_{ACLR}$

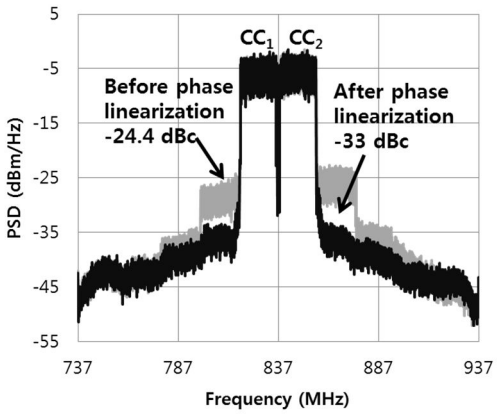


Fig. 3.16. Measured output spectra of the ET PA with 40-MHz BW LTE-A signal at 24 dBm output power.

is improved to –33 dBc, which provides 3 dB margin against the system specification. The overall gain difference with and without phase linearization is less than 0.1 dB, which means that the proposed phase linearizer does not perturb the gain profile as predicted in the previous section. EVMs after phase compensation are improved from 7.1 and 6.7% to 5.14 and 5.34% for CC_1 and CC_2 respectively.

Further investigation of the phase linearizer is performed by measuring the dynamic AM-AM and AM-PM of the ET PA with 40-MHz BW LTE-A signal. Fig. 3.15 compares the dynamic AM-AM and AM-PM of the ET PA before and after phase linearization at 24 dBm output power. As shown in Fig. 3.15 (b), large phase distortion (~ 20°) has been compensated through the phase linearizer, showing phase deviation less than 3° across the entire power range. It is worthwhile to note that the gain profile after linearization is remains almost unchanged.

Fig 16 shows the measured output spectra of the ET PA at the maximum linear output power levels with soft c lipped 40-MHz LTE-A signal. The proposed linearizer improves the CA E-UTRA$_{ACLR}$ by 8.6 dB.

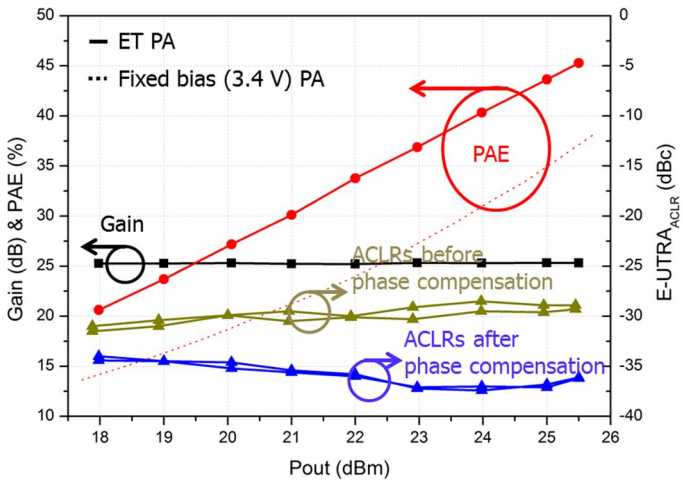


Fig. 3.17. Measured 20-MHz BW LTE performance of the ET PA with the proposed phase linearizer (PAPR=6.57 dB). Non-ET data is also shown as a reference.

20-MHz BW LTE test is also performed to benchmark the performance with other works. The LTE signal used in this measurement is fully loaded QPSK modulated signal with a PAPR 6.57 dB at 0.01% probability. CFR is not used in this measurement. The measured performance of the ET PA with 20-MHz BW LTE signal is plotted in the Fig. 3.17. The maximum linear output power reaches 25.5 dBm with 45.3% overall system PAE. The measured E-UTRA$_{ACLR}$ at 25.5 dBm is improved from –28.9 to –36.1 dBc and EVM from 4.31 to 2.67%. Better ACLRs in 20-MHz BW test compared to 40-MHz BW are mainly attributed to the reduced memory effect in the EA.

V_{offset} can be used as a tuning parameter, which is particularly useful in optimizing ACLR performance in the open-loop system employed in our approach. For example, the slope of the AM-PM distortion may not be consistent for different shaping functions. However, such various AM-PM distortions can be minimized by tuning V_{offset}. In the work, we have chosen 25.3 dB iso-gain shaping function and -

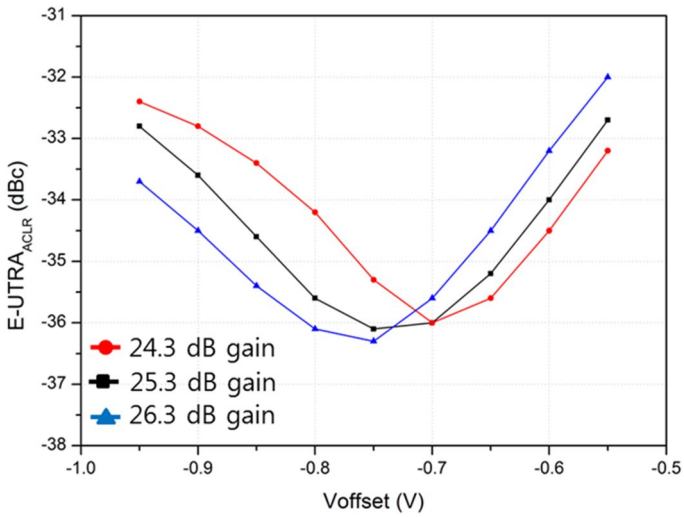


Fig. 3.18. Measured E-UTRA$_{ACLR}$ at 25.5 dBm output power with various $V_{offsets}$.

0.75 V V_{offset} for the best linearity and efficiency in the 20-MHz BW LTE test. To investigate the relationship between the shaping function and V_{offset}, we have measured the E-UTRA$_{ACLR}$ of our ET PA at 25.5 dBm output power with 20-MHz BW LTE signal for various V_{offset}s using three iso-gain shaping functions (24.3 dB, 25.3 dB, 26.3 dB) as shown in the Fig. 3.18. (Worst-side ACLR is plotted in this figure.) According to Fig. 3.18, we can find two features of the V_{offset}. First, if we assume that the V_{offset} is fixed around the optimum region, the output ACLR is not heavily dependent on the selected V_{offset}. For example, the ACLR degradation from 26.3 dB gain case to 24.3 dB gain case is only 1 dB when V_{offset} is fixed at -0.75 V. Moreover, the ACLR degradation in 25.3 dB case by changing the V_{offset} from -0.75 to -0.7 V is only 0.1 dB. Second, even if the optimum V_{offset} is slightly changed from –0.75 to -0.7 V as we decrease the gain from 26.3 to 24.3 dB, the system complexity to find optimum V_{offset} is much simpler than the typical digital pre-distortion or dual shaping table based linearization as in [9].

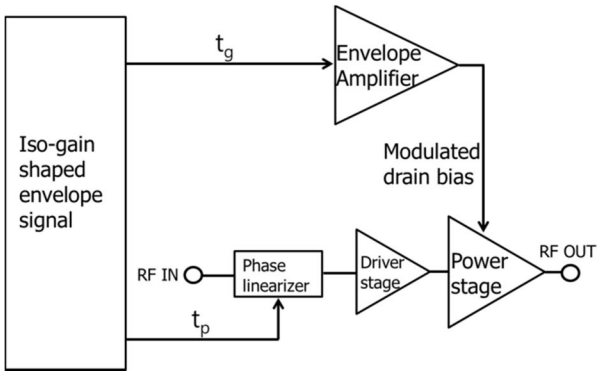


Fig. 3.19. Block diagram of the ET PA with three input signals.

Delay time alignment is an important system issue in most ET PA applications. Since our ET PA has three input signals, the timing mismatch among these signals should be minimized to show the best system ACLR performance. Refer to the block diagram of the ET PA system as shown in the Fig. 3. 19, we have performed AM synchronization first without the phase compensation, namely finding the optimum t_g, as in typical ET applications. In this case, the optimum time delay between RF signal and modulated drain bias can be determined by monitoring ACLR imbalance. After the AM synchronization, PM synchronization is performed by adjusting the time delay (t_p) of the input signal for the phase linearizer. Similar to the AM synchronization, the timing alignment for PM has been performed until the output ACLR reaches the best performance. Also, to investigate the ACLR degradation due to the delay mismatch, we have measured E-UTRA$_{ACLR}$ of our ET PA using 10-MHz BW QPSK LTE signal. When each delay is optimized to give the best system performance, the maximum linear output power reaches 25.5 dBm with 47.2% overall system PAE and -37.2 dBc E-UTRA$_{ACLR}$. The Fig. 3.19 shows the measured E-UTRA$_{ACLR}$ with various degrees of delay mismatches. To compare the ACLR sensitivity by the delay mismatches, four cases are compared. All cases

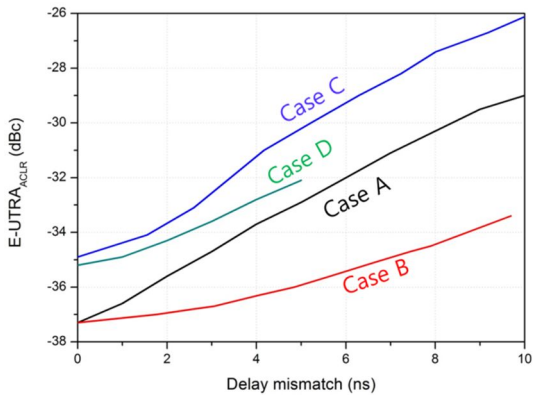


Fig. 3.20. Measured E-UTRA$_{ACLR}$ with various degrees of delay mismatches use 10-MHz BW LTE signal.

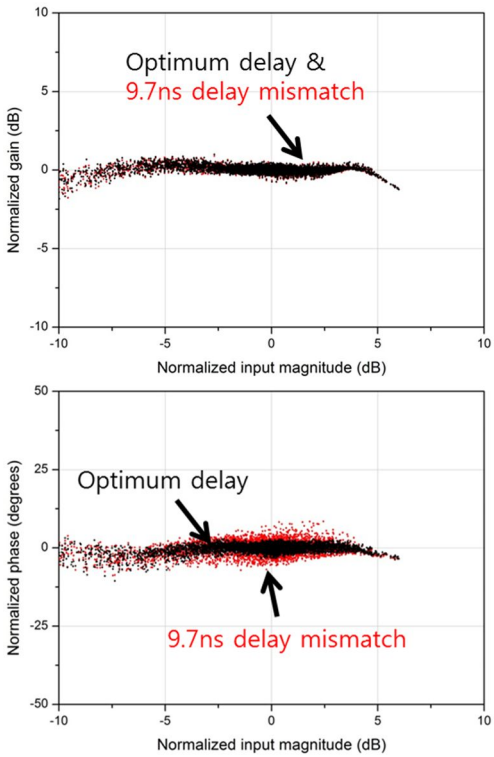
Case A : Proposed ET PA when both t_g and t_p are changed together.

Case B : Proposed ET PA when only t_p is changed.

Case C : ET PA in our previous work (S. Park *et al*., RFIC 2014 "Broadband CMOS stacked power amplifier using reconfigurable interstage network for envelope tracking application"). It is based on the same process technology (SOI CMOS), and very similar device configuration (two-stage tripled stacked RF PA). DPD linearization is used.

Case D : Kim *et al*., TMTT 2014, "Analysis of envelope-tracking power amplifier using mathematical modeling". The RF PA is fabricated in GaAs HBT process, and each data point is graphically estimated.

By comparing the Case A, C, and D, we can notice that the proposed ET PA (case A) has similar sensitivity on timing mismatches to the conventional ET PAs (Case C, D). This means that even if our ET PA utilizes two envelope signals, it does not show excessive sensitivity to the delay mismatch. Moreover, an interesting feature of our ET PA can be found by observing the Case B. Compared to the Case A, the PM delay misalignment (t_p) alone does not add any more ACLR degradation. This



(a) (b)

Fig. 3.21. (a) Measured dynamic AM-AM, and (b) dynamic AM-PM of the ET PA.

can be clearly verified by comparing the dynamic AM-AM and AM-PM of the ET PA with optimum delay and 9.7ns t_p delay mismatch as shown in the Fig. 3.21. As we can see in these figures, PM delay mismatch degrades only AM-PM memory effects while AM-AM memory effects are not affected by PM delay mismatch.

Finally, to evaluate the performance of the proposed PA under hard-clipped 40-MHz BW signals, aggressive CFR is applied to result in a 40-MHz BW CA signal with a PAPR of 5.74 dB, showing –49.4 dBc E-UTRA$_{ACLR}$, and 10.6% EVM. As expected, significant efficiency and power improvement is observed using hard clipped signal as shown in the Fig. 3.22. The maximum linear output power is extended from 24 to 25.1 dBm, and the overall system PAE from 37 to 40.5%.

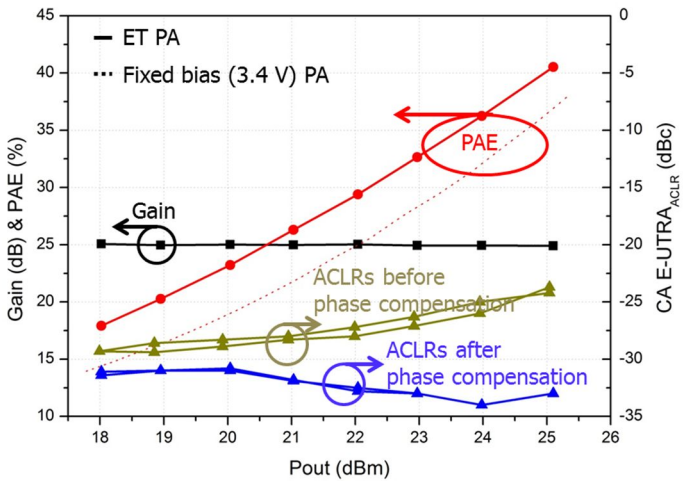


Fig. 3.22. Measured performance of the ET PA with the proposed phase linearizer using 40-MHz BW LTE-A signal, where the input signal PAPR is reduced from 8.97 to 5.74 dB by hard clipping. Non-ET data is also shown as a reference.

With the phase linearizer, CA E-UTRA$_{ACLR}$ is improved from –23.7 to –33 dBc, which is similar to the soft-clipped signal testing. EVMs for two CCs at the same output power are 11.14, and 11.18% respectively. EVM degradation mainly comes from the signal clipping process, which can be overcome by employing advanced CFR techniques.

Table I summarizes the performance of our ET PA in comparison with other state-of-the-arts using GaAs HBTs, SiGe HBTs, bulk, and SOI CMOS FETs. The overall ET system performance of this work using CMOS FETs is comparable or even better than the most of the reported ET PAs based on GaAs and SiGe HBTs. Further efficiency and linearity improvement is expected by employing the advanced techniques in the envelope amplifier [24]. Besides, since this work does not rely on the band-limited linearizers as in the case of [11] and DPDs [3]-[6], it can handle intra-band contiguous CA LTE-A signals with bandwidths up to 40-MHz.

TABLE 3.1

Performance Comparison Table of the Reported ET PAs for LTE Mobile Terminals

Reference	[3]	[14]	[4]	[6]	[5]	[11]	This work	
PA Tech.	GaAs HBT	GaAs HBT	SiGe HBT	0.32-μm SOI CMOS	0.32-μm SOI CMOS	0.18-μm CMOS	0.28-μm SOI CMOS	0.28-μm SOI CMOS
Frequency (GHz)	2.535	1.85	1.9	0.85	0.837	1.82	0.837	0.837
Signal BW (MHz)	20	10	10	20	20	10	20	40
Signal Config.	LTE 16-QAM	LTE 16-QAM	LTE QPSK	LTE QPSK	LTE QPSK	LTE 16-QAM	LTE QPSK	LTE-A QPSK
P_{out} (dBm)	29	27	26.5	26.1	25.9	27.5	25.5	24
Gain (dB)	28.5	24.2	28	24.8	25.8	14.2	25.3	24.7
Overall system PAE (%)	43	46.5	42	43.8	45.9	42.4	45.3	37
ACLR (dBc)	–49[2]	–33.4[1]	–44[1]	–34[1]	–33[1]	–36.5[1]	–36.1[1]	–33[3]
Output matching	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip
DPD	Yes	No	Yes	Yes	Yes	No	No	No

[1]: $\text{E-UTRA}_{\text{ACLR}}$

[2]: $\text{UTRA}_{\text{ACLR}}$

[3]: CA $\text{E-UTRA}_{\text{ACLR}}$

3.5 Conclusions

In this work, we have developed a two-stage CMOS ET PA with an integrated phase linearizer for wideband LTE-A applications up to 40-MHz. Instead of using DPD for linearization, a single shaping function is used to compensate for both AM- AM and AM-PM distortions of CMOS ET PAs. AM-AM distortion is flattened by conventional iso-gain envelope shaping while AM-PM distortion is compensated by the integrated phase linearizer. The control signal for the phase linearizer is internally generated by the integrated voltage summing buffer, which takes one of its inputs from the iso-gain shaping function block. Therefore, the proposed ET system works with only a single ET calibration step.

The bandwidth limitation of the proposed approach is carefully investigated through the envelope simulation of the entire PA system while replacing the EA with the ideal op amp. As long as the GBW of the OTA used in the voltage summing buffer is designed to be large enough, the proposed approach can support wider bandwidth signals with minimum impact on the system efficiency.

A two-stage RF PA with the integrated phase linearizer is fabricated using 0.28-μm SOI CMOS process for 0.837 GHz operation. The overall ET PA system, together with the 0.32-μm SOI CMOS EA is tested using 40-MHz BW LTE-A and 20-MHz BW LTE signals. The measured overall system PAE of the ET PA with 7.46 dB PAPR, 40-MHz BW LTE-A signal is 37% with –33 dBc CA E-UTRA$_{ACLR}$ at 24 dBm output power. To verify the effectiveness of the linearizer, the dynamic AM-AM and AM-PM characteristics have been measured, showing that AM-PM distortion of 20° is linearized through the phase linearizer. 20-MHz BW LTE test

shows that the measured overall system PAE and linearity of our CMOS ET PA is comparable or better than most of GaAs and SiGe HBT counterparts.

To our knowledge, this work is the first demonstration of DPD-less ET PA system for 40-MHz LTE-A applications. It further extends the potential of CMOS ET PAs for future mobile communication standards.

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Chapter 4

A Wideband Envelope Amplifier using Diode Rectifier Current Injection Circuit

4.1 Introduction

The envelope tracking (ET) technique offers back-off power efficiency enhancement of RF power amplifiers (RF PA) with high peak-to-average-power-ration (PAPR) signals such as long term evolution (LTE) and LTE-advanced (LTE-A). To achieve the high efficiency of the ET PA system, each envelope amplifier (EA) and RF PA should be optimally designed to give best efficiencies. A typical design methodology for the EA has been a hybrid approach which is a parallel combination of the linear stage and switching stage. The switching stage is a step down buck converter which provides the average current for the RF PA load with very high efficiency (~90%) while the linear stage provides the extra current for the RF PA load with high linearity and fidelity to track the input envelope accurately. Such hybrid type EAs have been investigated so far and widely used in most ET PAs for LTE, even LTE-A mobile applications [1]-[12]. However, conventional

hybrid type EAs have several system level problems especially when they handles wideband signals

First of all, the efficiency of the hybrid type EA decreases as the signal bandwidth goes up due to the larger switching loss in the switching stage. According to [1], the efficiency of the hybrid type EA decreases by 2.8% as the signal bandwidth is increased from 10- to 40-MHz. Since the overall system efficiency of the ET PA is a weighted product of the efficiency of the EA and RF PA, efficiency degradation of the ET PA in wideband operation is inevitable. For example, in our previous work [2], the overall system PAE of the ET PA with 20-MHz BW QPSK LTE signal is 45.3%, while that with the 40-MHz BW two carriers aggregated QPSK LTE-A is degraded to only 37%. The second problem of the hybrid EA is limited speed of the linear stage. The linear stage is required to have very high speed to achieve high fidelity; however, the gain bandwidth product (GBW) of the linear stage is often suffered from the large pole in the output stage FETs. Although the linear stage should have 5-6 times higher GBW than the signal bandwidth, the reported GBWs of the linear stage are limited to only 200-MHz, which is not sufficient to handle 40-MHz BW LTE-A signals [1]-[4]. Finally, the most serious problem of the hybrid EA is the out of band noise. The switching current from the switching stage causes crossover distortion at the midlevel of the output voltage, which results in severe memory effect of the ET PA [3], also Rx band noise performance degradation as well [5]-[8]. For example, although the authors in [8] demonstrated fully integrated ET PA system using 0.35-μm BiCMOS process, their work suffered from poor RxBN of –111 dBm/Hz due to the switching noise in the EA. Various noise canceling techniques have been demonstrated to

reduce the switching noise of the hybrid type EAs such as parallel linear stage, resonant frequency tuning [6],[7] noise bypass capacitor [8], and so on. However, these techniques generally increase the design complexity, or even cause the instability of the EA.

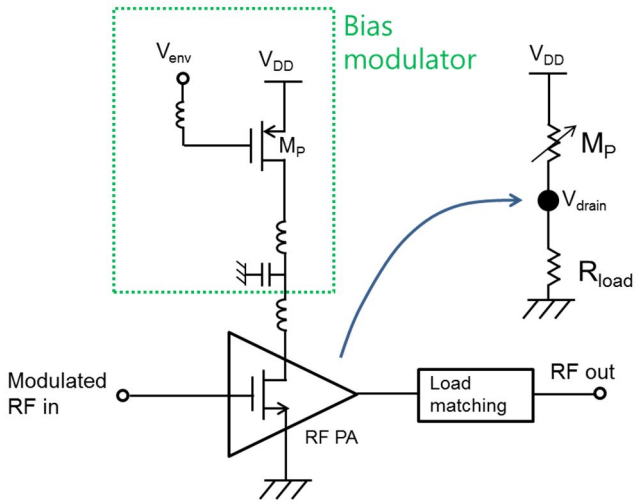
In this work, a wideband EA with the diode rectifier current injection circuit is presented to implement the 80-MHz BW LTE CMOS ET PA system. The proposed EA is designed and fabricated in 0.28-μm silicon-on-insulator (SOI) CMOS process without the switching stage to overcome problems inherited from the conventional EAs. Combined with the 2-stage CMOS RF PA, the ET PA system shows 41.2% overall system PAE, and –33.5 dBc E-UTRA$_{ACLR}$ at 25.2 dBm output power with 80-MHz BW LTE signal. This paper is organized as follows. Section 4.2 presents the operation principle and analytical analysis to derive the efficiency of the proposed EA. In Section 4.3, detailed design procedure of the proposed EA, also the RF PA using the same 0.28-μm SOI CMOS process. CW and envelope simulation results are also included in this section to clearly demonstrate the effectiveness of the proposed EA. Performances of the full ET PA system using various LTE signal bandwidth (20- to 80-MHz) are characterized in Section 4.4 with the Rx band noise measurement result. Finally this paper ends with the conclusions in Section 4.5.

4.2 Operation Principle of the proposed envelope amplifier

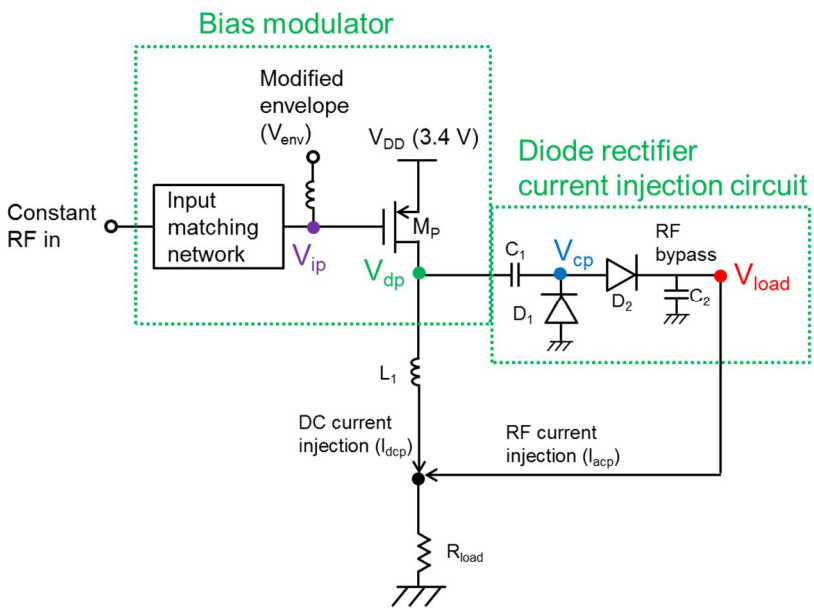
The Fig. 4.1 (a) shows the circuit schematic of the bias modulator which is simply composed of large sized PMOS FET (M_p, 10-mm/0.28-μm). Since the drain bias of the RF PA (V_{load}) is determined by a gate bias of the M_p (V_{env}), we can model the M_P to the variable resistor controlled by the gate bias of the M_p. Therefore, the efficiency of the bias modulator can be express as follows [13].

$$\eta = \frac{V_{load}}{V_{DD}} \tag{1}$$

The estimated average efficiency of the envelope amplifier using (1) for the 6.53 dB PAPR QPSK LTE envelope signal is only 56% (V_{rms} = 1.9 V), which significantly degrades the overall system PAE of the ET PA. To boost the efficiency of the bias modulator, we have added several circuit blocks as shown in the Fig. 4.1 (b). The proposed EA is divided into two sub circuits which are bias modulator (M_p) and diode rectifier current injection circuit. Unlike in Fig. 4.1 (a), the bias modulator in Fig. 4.1 (b) takes two input signals. The first one is the inversely shaped input envelope signal (V_{env}) to determine the output dc level of the EA. The other one is continuous wave (CW) mode RF signal (V_{RFp}) which has same frequency with the modulated input RF signal for the RF PA. In this work, we have selected 836.5 MHz for the carrier frequency to cover LTE band V (824-849 MHz). The input RF signal is amplified by the M_p, and the output matching network for the M_p is designed to have square RF voltage waveform at the drain node of the M_p like Class-F operation. The dc component of the square RF voltage directly goes to the RF PA while the ac component is coupled to the diode rectifier current injection circuit. The ac component of the RF voltage is rectified through the diode rectifier,



(a)



(b)

Fig. 4.1. (a) Circuit schematic of the simple bias modulator. (b) The proposed envelope amplifier which is composed of bias modulator and diode rectifier current injection circuit.

and then the RF current (I_{acp}) is injected to the RF PA together with dc current from the M_p (I_{dcp}).

In this section, the efficiency of the proposed EA is derived using the waveform based analysis. For this analysis, it is assumed that the magnitude of the V_{RFp} is large enough to operate M_p in the overdrive mode, where the M_p is regarded as an ideal switch. Inductance and capacitances of the RF choke (L_1), RF decoupling (C_1) and RF bypass (C_2) are assumed to very large. Also, the RF PA is modeled as R_{load} for simplicity. Figures in Fig. 4.2 are the voltage waveform at the each node depicted in the Fig. 4.1 (b) (V_{ip}, V_{dp}, V_{cp}, V_{load}). Fig. 4.2 (a) illustrates the input RF voltage waveform of the bias modulator (V_{ip}). The supply voltage for the M_p is 3.4 V, and its threshold is labeled as V_{thp}. When the magnitude of the V_{RFp} is below than the V_{thp}, the M_p is in turn-on state to conduct the current to the R_{load} during the time interval of α. In this state, the drain voltage of the M_p (V_{dp}) is pulled up to the supply rail (3.4 V). When the magnitude of the V_{RFp} exceeds the V_{thp}, the M_p is now in turn-off state. In this state, V_{dp} is built to square wave like class-F amplifier. Therefore, V_{dp} is approximated to a square wave where the duty cycle is α ($0<\alpha<1$), and amplitude is V_{DD} as shown in the Fig. 4.2 (b). The dc current component of the V_{dp} (I_{dcp}) directly goes to the R_{load} whose magnitude is $\alpha V_{DD}/R_{load}$ while the ac component is coupled to the diode rectifier. Since the output voltage of the EA is determined by α, which is controlled by V_{env}, sub-circuits including the input matching network and M_p can be referred as “bias modulator” as in the Fig. 4.1 (b).

The structure of the diode rectifier current injection circuit in this work has very similar configuration to the conventional voltage doublers [14],[15], while its operation principle is quite different since the output dc voltage of the envelope amplifier is fixed at αV_{DD}. The operation principle of the diode rectifier current

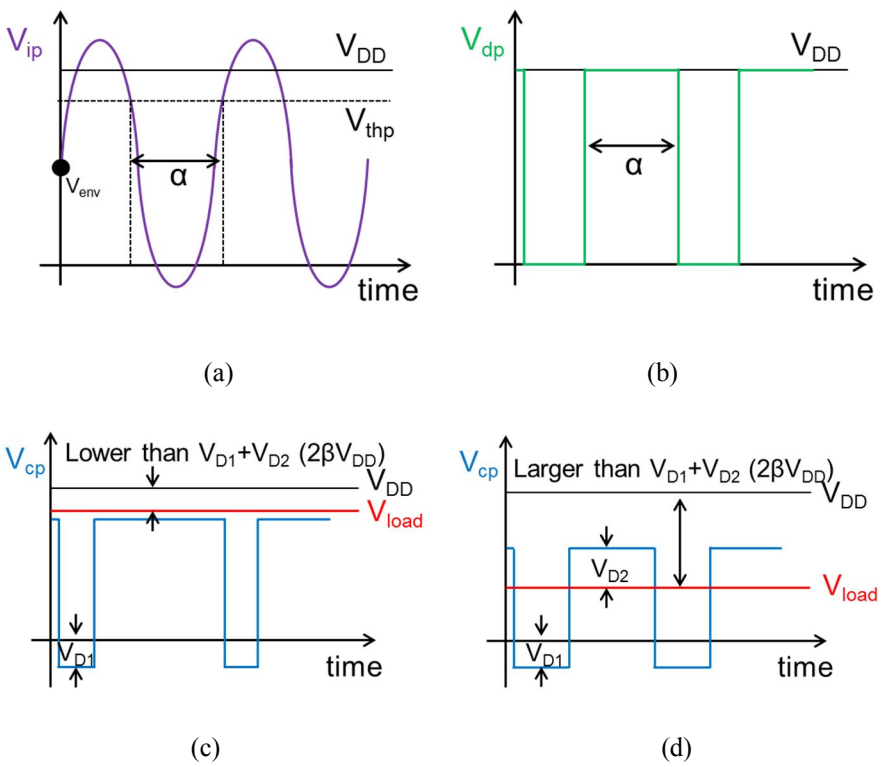


Fig. 4.2. RF voltage waveforms at (a) input of the envelope amplifier, (b) drain node of the M_p, (c) output of the current injection circuit in the high power mode, (d) output of the current injection circuit in the low power mode.

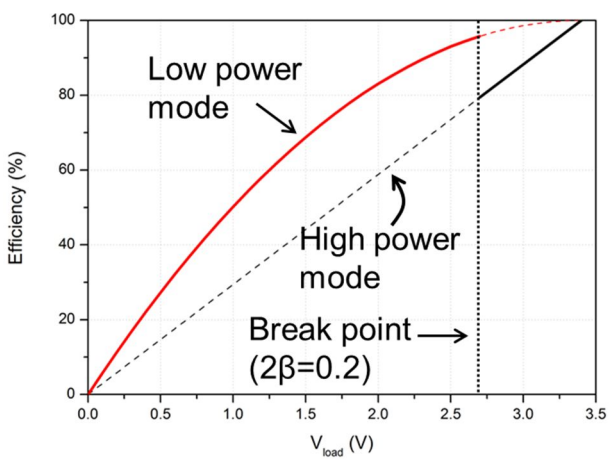


Fig. 4.3. Estimated efficiency of the proposed envelope amplifier using (6).

injection circuit can be identified by carefully investigating the voltage waveform at the each node in the circuit.

When V_{dp} falls to the ground, D_1 is turned on to draw the negative charges to charge the C_1. Therefore, V_{cp} pulls to the ground with a forward bias loss of D_1 (V_{D1}) as shown in the Fig. 4.2 (c), and (d). In this state, D_2 is turned off so the V_{cp} is isolated from the V_{load}. When V_{dp} starts to rise, D_1 is now turned off, C_1 is positively charged and the V_{cp} increases until the V_{cp} exceeds the $V_{load}+V_{D2}$. When V_{cp} reaches to $V_{load}+V_{D2}$, the positive charges which are stored in the C_1 is injected to the R_{load} through the D_2.

To derive the efficiency of the proposed EA, the operation of the EA should be divided into two modes which are high power mode, and low power mode respectively. High power mode occurs when the V_{load}, namely αV_{DD} exceeds the $V_{DD}-V_{D1}-V_{D2}$ as shown in the Fig. 4.2 (c). In this mode, there is no injected current from the diode rectifier, so the efficiency of the EA simply follows (1). If we defined the forward bias loss of the diode is a product of V_{DD} and scaling factor β, the breakpoint between high power mode and low power mode is

$$V_{break} = (1-2\beta)V_{DD} \tag{2}$$

When the V_{load} i.e., αV_{DD} is lower than V_{break}, the EA operates in the low power mode. In low power mode, the ac current is injected to the R_{load} during α which boosts the efficiency of the EA in the mid and low power region. Refer to Fig. 4.2 (d), the efficiency of the EA in this mode can be derived as follows. The average ac current injected to the R_{load} during α is

$$I_{acp} = \frac{\alpha(1-\alpha)V_{DD}}{R_{load}} \tag{2}$$

Therefore, the total current delivered to the RF PA load from the envelope amplifier is

$$I_{load} = I_{dcp} + I_{acp} = \frac{2\alpha(1-\alpha)V_{DD}}{R_{load}} \tag{3}$$

The average power delivered to the RF PA load, and average dc power consumption of the envelope amplifier are

$$P_{load} = V_{load} I_{load} = \alpha V_{DD} \frac{2\alpha(1-\alpha)V_{DD}}{R_{load}} \tag{4}$$

$$P_{dc} = \frac{\alpha V_{DD}^{\ 2}}{R_{load}} \tag{5}$$

Therefore, the efficiency of the envelope amplifier is

$$\begin{aligned} \eta &= \frac{V_{load}}{V_{DD}} && V_{load} > (1-2\beta)V_{DD} \\ &= \frac{V_{load}}{V_{DD}}\left(2-\frac{V_{load}}{V_{DD}}\right) && V_{load} > (1-2\beta)V_{DD} \end{aligned} \tag{6}$$

Fig. 4.3 is a calculated efficiency of the proposed envelope amplifier using two equations in (6). The efficiency curve with 2β=0.2, which corresponds to V_{D1}=V_{D2}=0.34 V is overlapped in this figure for a reference. At the average drain bias of 6.53 dB PAPR QPSK LTE signal (1.9 V), the efficiency of the EA is boosted from 56 to 81%.

4.3 Circuit design and simulation

4.3.1 Envelope amplifier and RF power amplifier design

Fig. 4.4 is a complete circuit schematic of the designed EA using 0.28-μm CMOS process. The bias modulation is only applied to the power stage of the 2-stage CMOS RF PA to prevent the severe gain and phase distortion in the low power region. The L_i, C_i, and L_c form an input matching network for M_p at 836.5 MHz center frequency. The RF choke inductor (L_c) is placed at the envelope signal path to prevent the interaction between RF signal generator and envelope waveform generator. The size of the bias modulator PMOS FET and two diode-connected NMOS FETs are 10mm/0.28-μm. RC feedback network is employed between the drain and source node of the M_p to prevent the oscillation. Load matching network which is composed of off-chip load matching capacitor (C_l), PCB transmission line, and RF bypass capacitor (C_{b2}) forms the low-pass filter type matching. The RF decoupling capacitor (C_d), and RF bypass capacitor (C_{b1}) are realized with off-chip metal-insulator-metal (MIM) capacitor to avoid the conduction, and dielectric loss of on-chip MIM capacitors.

A 2-stage RF PA is also designed using the same 0.28-μm SOI CMOS process to implement the full ET PA system. The detailed circuit schematic of the RF PA is shown in the Fig. 4.5. The driver and power cell of the RF PA are designed based on tripled stacked FET approach to prevent the voltage breakdown. Miller capacitors are connected between the drain and source node of the power cell FETs to enhance the peak efficiency [10]. The size of the unit driver and power cell FET are 2-mm/0.28-μm, and 10-mm/0.28-μm respectively. The output matching network of the RF PA is also realized using off-chip components. Even though the

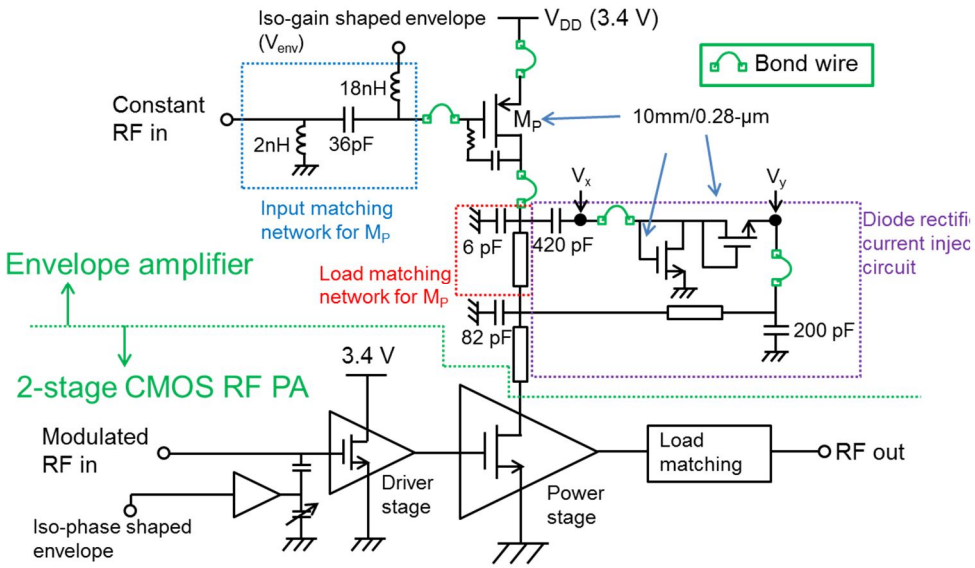


Fig. 4.4. Detailed circuit schematic of the designed envelope amplifier with diode rectifier current injection circuit.

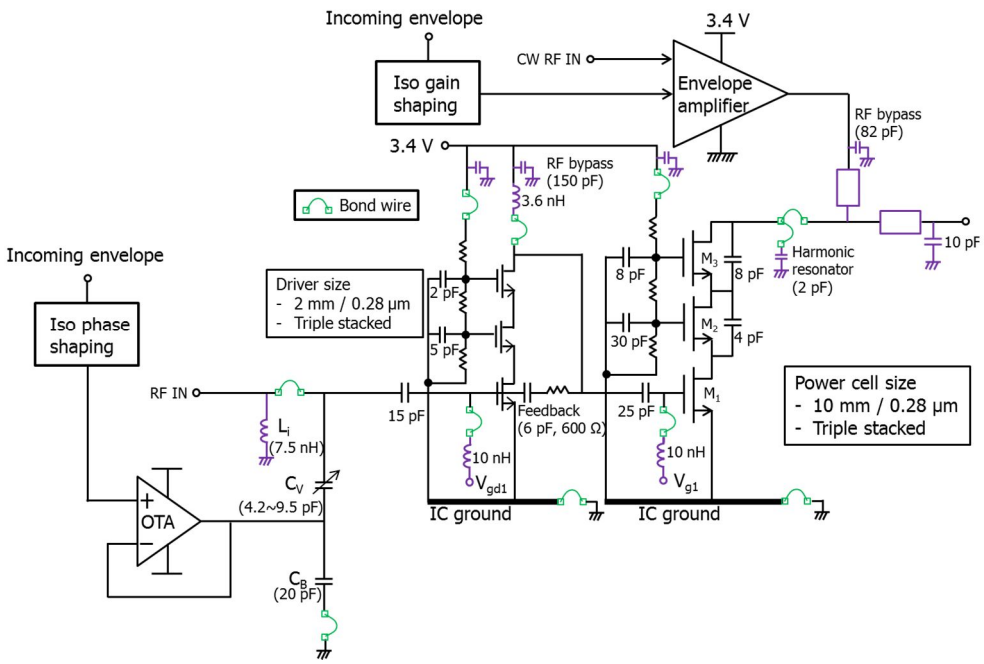
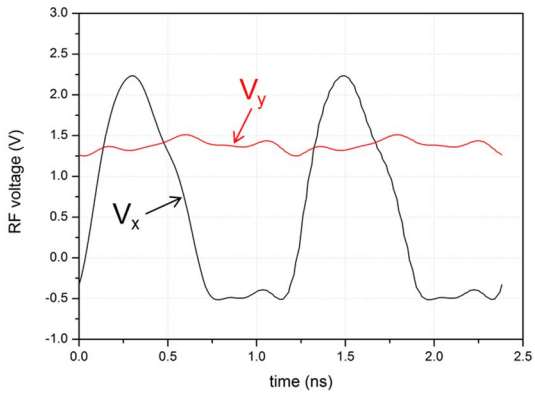
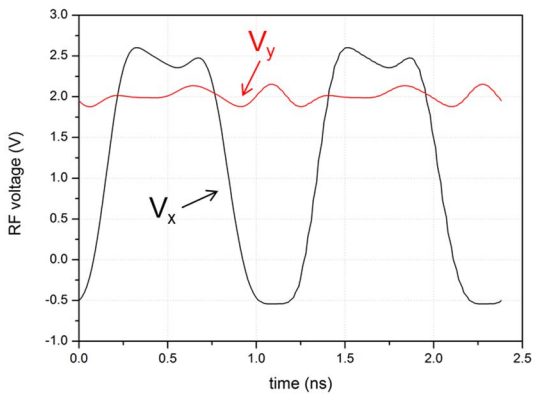


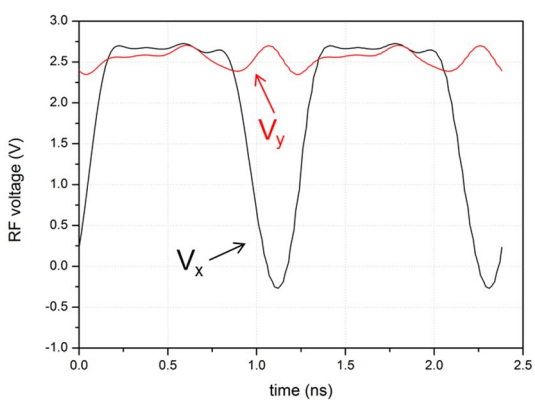
Fig. 4.5. Detailed circuit schematic of the designed 2-stage RF power amplifier with the AM-PM linearizer. Off-chip components are indicated with purple color.



(a)



(b)



(c)

Fig. 4.6. Simulated voltage waveforms at node V_x, and V_y in the Fig. 4.4 with three different V_{env}s. (a) 3.4 V, (b) 2.4 V, (c) 1.4 V.

gain profile of the ET PA can be flattened by an iso-gain shaping function, CMOS ET PAs generally suffer from the significant AM-PM distortion due to the bias dependent C_{gd}s [2],[9]. To compensate the AM-PM distortion, a dual-shaping table based linearization is utilized which is already demonstrated in our previous work [9]. The phase linearizer is employed at the input matching network of the RF PA to dynamically adjust the group delay of the RF input signal. In our previous work [2],[9], we have proven that the phase linearizer in this work has a capability to handle a wideband signal as long as the gain-bandwidth product (GBW) of the operational trans-conductance amplifier is large enough.

Fig. 4.6 are simulated voltage and current waveforms at the input and output nodes of the diode rectifier marked as V_x, and V_y in the Fig. 4.4, using Keysight's ADS harmonic balance simulation. The input RF power for the envelope amplifier is fixed at 12 dBm, with three V_{env}s which are 3.4, 2.4, and 1.4 V to compare waveforms at low, mid, and high power mode respectively. For this simulation, the input RF power for the 2-stage CMOS RF PA is fixed at 5 dBm.

When the V_{emv} is 3.4 V, the duty cycle of the V_x is small since the most of input RF voltage is higher than the threshold of the M_p. Therefore, the dc voltage level at the EA is set to low value around 1.3 V as shown in the Fig. 4.6 (a). It is worthwhile to note that the V_X in the Fig. 4.6 (a) does not have square voltage waveform. This is mainly attributed to the low trans-conductance of the M_p in the triode region. The non-square shaped V_x causes reducing the effective duty cycle of the V_x which means decreasing the time duration for injecting the RF current. This results in the efficiency degradation at low power region than the theoretical prediction in the previous section. During the time interval in which V_x is higher

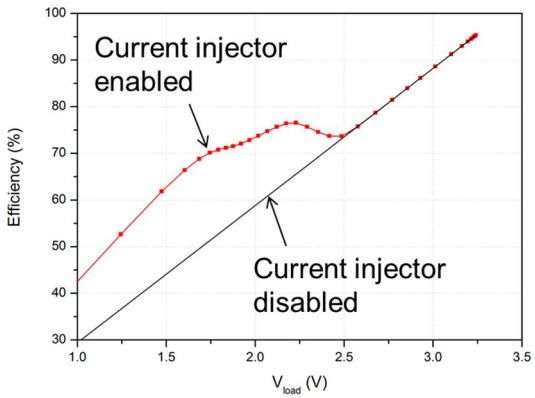


Fig. 4.7. Simulated efficiency of the envelope amplifier with 7.5 Ω resistive load.

than V_y+V_{D2}, the RF current is injected to the RF PA load. The average injected RF current to the RF PA, and the efficiency of the EA are simulated to 68 mA, and 57.5% respectively.

When the V_{env} is decreased to 2.4 V, the duty cycle of the V_x is increased which has square voltage waveform like Class-F amplifier as shown in the Fig. 4.6 (b). The average output dc voltage from the EA is 2 V, and the amount of the ac current injection is 67 mA. Despite the amount of the current injection is similar to the 3.4 V case, the efficiency of the EA is increased from 57.5% to 74%.

Finally, when the V_{env} is decreased down to 1.4 V as shown in the Fig. 4.6 (c), the duty cycle of the V_x is further increased resulting in 2.5 V dc voltage. In this state, V_y reaches the maximum peak of V_x, which does not meets the $V_x>V_y+V_{D2}$ criteria. Therefore RF current injection is hardly occurred in this state. Simulated ac current injection is lower than 1 mA while the efficiency of the EA is maintained to 74.8% due to the low voltage drop in the M_p.

Fig. 4.7 is a simulated efficiency of the envelope amplifier with and without diode rectifier current injection circuit. For this simulation, the RF PA is replaced by 7.5 Ω resistor for simplicity. As shown in this figure, a breakpoint around 2.5 V

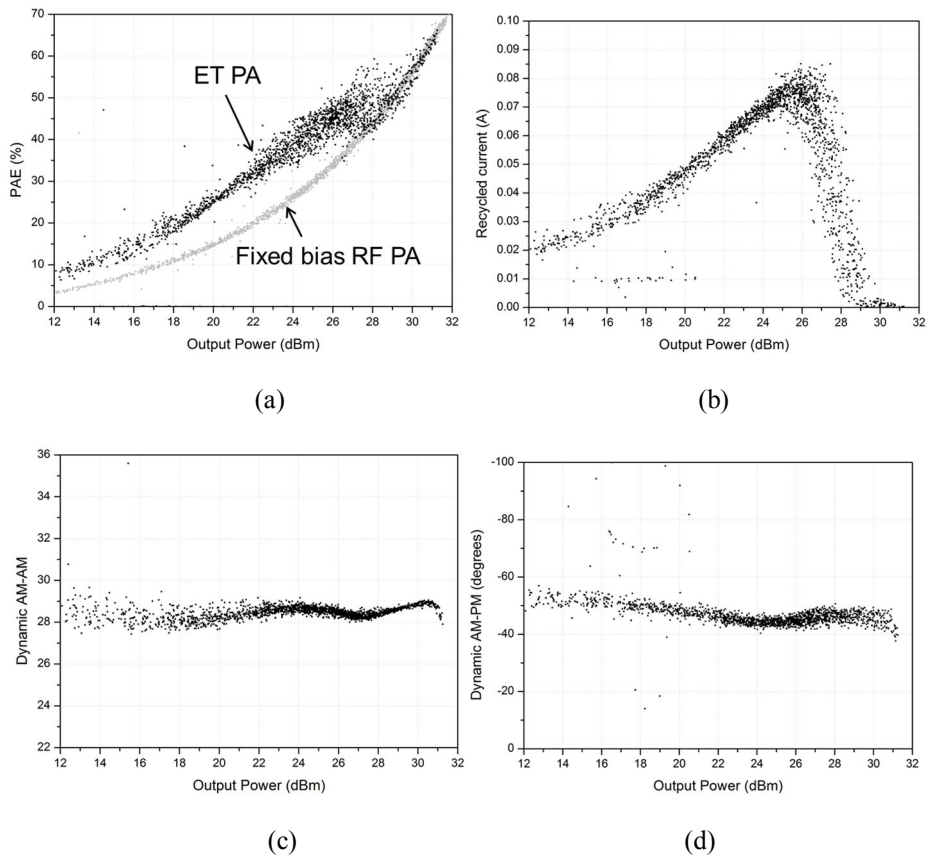


Fig. 4.8. Simulated performance of the ET PA at the 25.5 dBm output power with a proposed envelope amplifier using 20-MHz BW QPSK LTE signal. (a) PAE, (b) injected current from the diode rectifier current injector, (c) dynamic AM-AM, (d) dynamic AM-PM.

is clearly observed as discussed in the previous section. The efficiency of the proposed envelope amplifier at high power mode (>2.5 V) simply follows the efficiency without the current injector. When the load voltage is below than 2.5 V, the current injector is enabled, and boosts the efficiency by 15% at the 1.9 V load voltage.

4.3.2 Envelope simulation using wideband LTE signals

In the previous section, we have designed and simulated the static characteristics of the proposed envelope amplifier. In this section, an envelope simulation of the

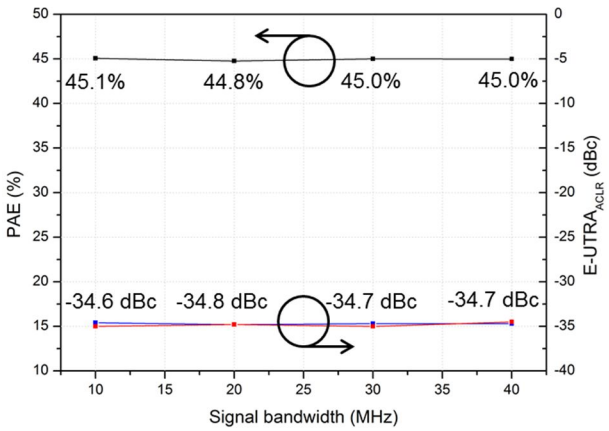


Fig. 4.9. Simulated overall system PAE and E-UTRA$_{ACLR}$ of the ET PA at 25.5 dBm output power with various LTE signal bandwidths.

entire ET PA system using LTE signals with various signal bandwidths is performed to verify the effectiveness of the proposed envelope amplifier.

First of all, 20-MHz BW QPSK LTE signal with a carrier frequency of 836.5 MHz is used as RF signal source to investigate the dynamic characteristics of the overall ET PA system. Fig. 4.8 are the simulated instantaneous overall system PAE, injected current, dynamic AM-AM, and dynamic AM-PM of the ET PA at 25.5 dBm average output power. For this simulation iso-gain and iso-phase shaping table are constructed by carefully investigate the static AM-AM and AM-PM characteristics, then utilized for linear operation. Fig. 4.8 (a) is a simulated overall system PAE of the ET PA. The simulated PAE of the fixed bias (3.4 V) RF PA is also plotted as a reference. At the high output power higher than 28 dBm, the efficiency of the ET PA follows the PAE curve of the fixed bias PA, while the efficiency at the mid and low power region is boosted more than 10%. Fig. 4.8 (b) is a simulated injected ac current from the current injection circuit. As expected from the static simulation in Fig. 4.7, the ac current is not injected at high power region (>28 dBm), but peaks at 26 dBm to 70 mA. Fig. 4.8 (c) and (d) are

simulated dynamic AM-AM and AM-PM at 25.5 dBm output power. The gain and phase profiles are linearized by the iso-gain and phase shaping function. No severe dispersion due to the insufficient speed of the EA and phase linearizer is observed. The calculated E-UTRA$_{ACLR}$ and overall system PAE of the ET PA at 25.5 dBm output power is –34.8 dBc, and 44.8% respectively. Further linearity improvement is expected by optimizing each shaping function to flatten the gain and phase profiles.

In Fig. 4.9, envelope simulation using various QPSK LTE signals where the signal bandwidth is swept from 10- to 40-MHz is performed to calculated E-UTRA$_{ACLR}$ and overall system PAE at 25.5 dBm output power. As shown in this figure, PAE and ACLR are maintained even in the 40-MHz BW LTE simulation. Unlike the conventional hybrid type EAs, which are generally suffered from low GBW of the linear stage, the proposed EA can support the wideband signal without compromising the PAE and ACLR. This figure clearly verifies the effectiveness of the proposed envelope amplifier in wideband operation.

4.4 Measurement results

The proposed EA and 2-stage RF PA are fabricated in same 0.28-μm SOI CMOS process. Fig. 4.10 shows photograph of the fabricated EA, RF PA chips, and implemented test board on 5 cm × 3 cm size FR4 substrate ($\varepsilon_r \sim 4.7$). Especially in Fig. 4.10 (d), magnified photograph of the entire EA circuit is presented. It is worthwhile to note that the proposed envelope amplifier occupies small test board area compared to the typical hybrid type envelope amplifier, since the proposed EA does not contain bulky μH-order external inductor.

Fig. 4.11 is a block diagram of the measurement setup. The QPSK LTE envelope and RF signal are generated by N7624B signal studio software and downloaded to the waveform generator and RF signal generator respectively. The incoming envelope signal is modified by the iso-gain and iso-phase shaping table and downloaded to the 33622A waveform generator. The modulated RF signal is generated by the N5182B signal generator while the CW RF signal for the EA is generated by separate E4438C signal generator. Each timing delay for AM and PM correction is adjusted sequentially by observing the ACLR imbalance [2]. The output of the ET PA is captured by N9020A to measure the ACLR and dynamic characteristics.

First of all, 836.5 MHz static performance of the ET PA is characterized with various V_{env}s as shown in the Fig. 4.12. For this measurement, V_{env} is swept from 0 to 3.4 V, and RF input power for the EA is fixed at 10 dBm. Only the drain bias of the power stage is modulated by the EA with 3.4 V supply while that of driver stage is fixed at 3.4 V. For a reference, a performance of fixed bias (3.4 V) RF PA is also plotted in this figure which shows 69% maximum PAE at the 30.5 dBm

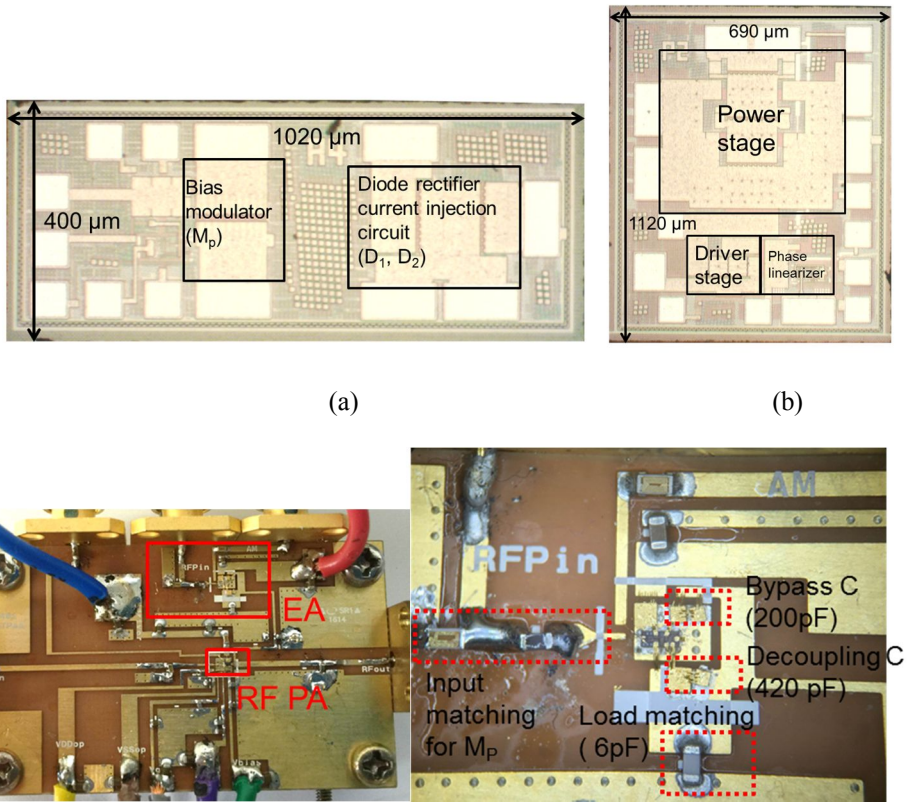


Fig. 4.10. Fabricated chips and implemented ET PA on FR4 substrate. (a) Envelope amplifier, (b) 2-stage RF PA, (c) test board, (d) expanded photograph of envelope amplifier.

output power. Drain efficiency of the power stage (DE) at the same output power is as high as 72.8%. The maximum PAE and output power after connecting the EA (V_{env}= 0 V) is slightly decreased by 3.5%, and 0.4 dB respectively due to the finite on-resistance of the M_p. The current consumption in the phase linearizer is only 2 mA, with 2.8 V supply rails. When the V_{env} is low (0~1.8V), the efficiency boosting compared to the fixed bias mode RF PA is negligible due to diode loss and low gain of the M_p in deep triode region, which is already predicted by waveform analysis in the Section 4.2, and envelope simulation in the Section 4.3. However, when the V_{env} is lower than 2 V, the overall system PAE is boosted by injecting

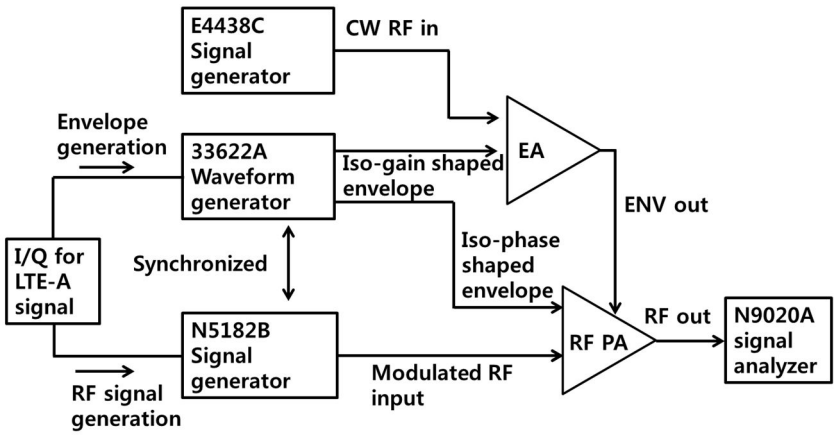


Fig. 4.11. Block diagram of measurement setup for the ET PA.

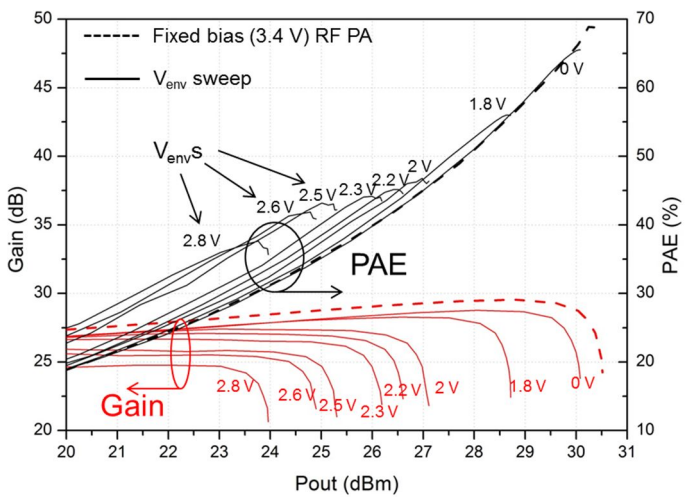


Fig. 4.12. Measured CW performance of the ET PA at 836.5 MHz.

additional ac currents to the RF PA. Compared to the PAE of the fixed bias RF PA at 6 dB back-off output power (24.5 dBm, 33%), the proposed current injector provides 9% efficiency boosting at the same output power. As a result, more than 40% PAE is maintained down to 6 dB back-off output power.

For the optimum efficiency and gain flatness in 80-MHz BW LTE test, we have applied the shaping function to the EA as

$$V_{env}(t) = V_{DD} - V_{DD}\left(v_{in}(t) + \alpha e^{-(v_{in}(t)/\alpha)}\right) \tag{7}$$

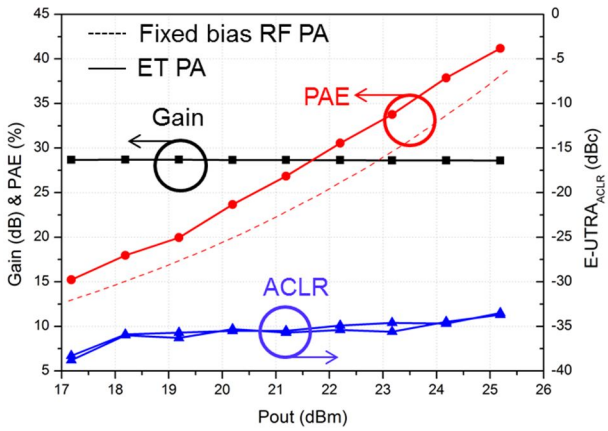


Fig. 4.13. Measured performance of the ET PA using 80-MHz BW QPSK LTE compatible signal.

where V_{DD} is a supply voltage to the EA (3.4 V), and α is a detroughing constant, which provides dc offset bias to prevent the gain collapse in the low power region. Note that the shaping function in (7) is an inverse version of the typical exponential envelope shaping function [11], which is widely used in hybrid type EAs.

Fig. 4.13 is a measured performance of the ET PA with 80-MHz BW QPSK LTE compatible signal whose PAPR is 6.53 dB at 0.01% probability. The maximum linear output power reaches 25.2 dBm with 41.2% overall system PAE, and –33.5 dBc E-UTRA$_{ALCR}$. The overall system PAE includes the power consumption in the driver stage, power stage, envelope amplifier, and phase linearizer in the RF PA. The 10 dBm CW RF input power for the envelope amplifier is also accounted for calculating the overall system PAE. The gain of the ET PA is maintained to 28.6 dB for 17.2 - 25.2 dBm output power range due to the iso-gain envelope shaping. In this figure, PAE of the fixed bias RF PA is also plotted with dashes for a reference which shows only 38 % at the 25.2 dBm output power. Therefore the ET offers 3.2% efficiency boosting even in the 80-MHz BW LTE test.

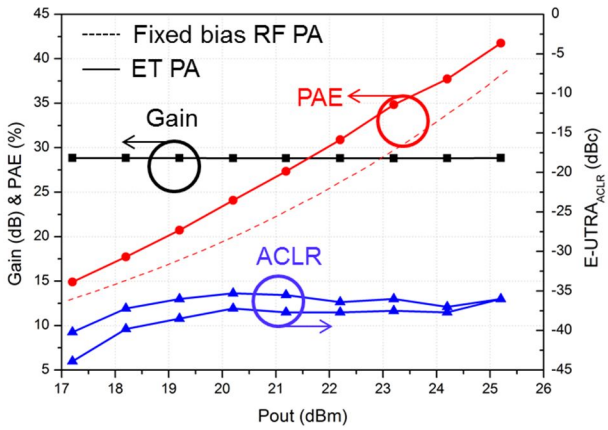
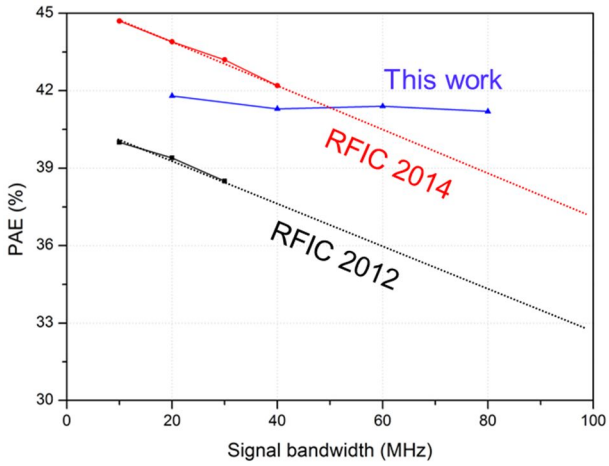


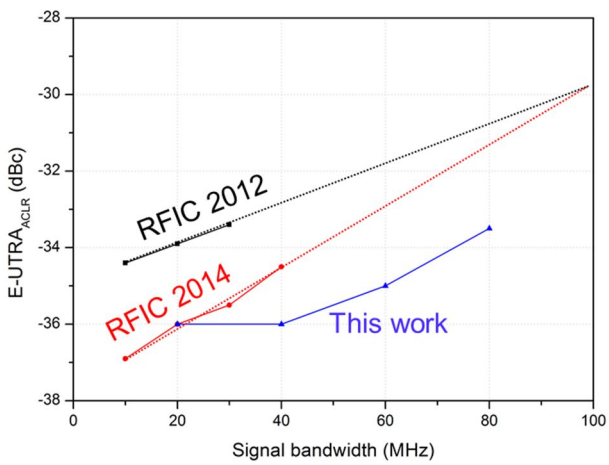
Fig. 4.14. Measured performance of the ET PA using 20-MHz BW QPSK LTE signal.

To benchmark the performance with other works, 20-MHz LTE test is also performed as shown in the Fig. 4.14. Compared to Fig. 4.13, the overall system PAE, gain, and E-UTRA$_{ACLR}$ show very similar characteristics to the 80-MHz BW LTE test. The overall system PAE at 25.2 dBm output power is 41.8% with 28.8 dB gain, and –36 dBc E-UTRA$_{ACLR}$. Similar to the 80-MHz LTE test, the ET provides 3.8% efficiency enhancement at 25.2 dBm output power.

Performances of the ET PA with various signal bandwidths are characterized in Fig. 4.15 (a), and (b). In these figures, overall system PAE and E-UTRA$_{ACLR}$ of the ET PA at 25.2 dBm output power is plotted as a function of signal bandwidth from 20- to 80-MHz. The overall system PAE is maintained around 41.2% from 20- to 80-MHz while the ACLR is slightly decreased by 2.5 dB at 80-MHz LTE test. The degraded ACLR is mainly attributed to the limited GBW of OTA in the phase linearizer which increases the AM-PM memory effect as addressed in the []. Aside from non- idealities of the phase linearizer, we can conclude from these figures that the proposed EA have capability to handle wideband LTE signal up to 80-MHz



(a)



(b)

Fig. 4.15. (a) Measured overall system PAE, and (b) E-UTRA$_{ACLR}$ of the ET PA at the maximum linear output power as a function of signal bandwidths. To compare the performance with other works, simple linear extrapolation curves are also plotted in these figures.

without any efficiency degradation. To compare the wideband performance of our ET PA with other works, PAE and ACLR of two published ET PA works are also plotted in the Fig. 4.15 (a), and (b). The red curves in these figures are performance of our previous ET PA work [9], while the black curves are those of other group's work [4]. It is worthwhile to note that EAs in both [9], and [4] have conventional

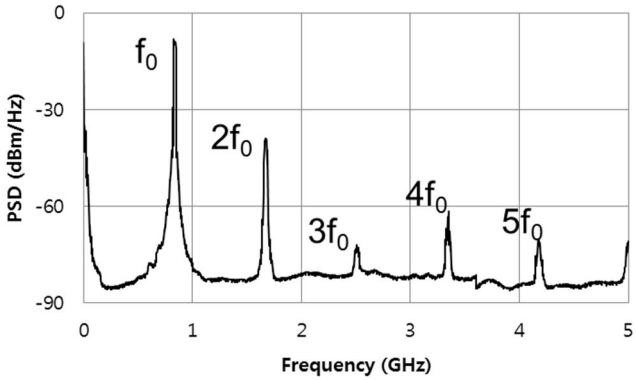


Fig. 4.16. Measured far-out spectrum (~5 GHz) of the ET PA.

hybrid type configuration. Since the published ET PAs up to date have not reported the 80-MHz BW performance, simple linear extrapolation curves are overlapped on each PAE and ACLR plots to compare the wideband performance. Even though the performance our ET PA with the proposed EA does not matched to the ET PAs with hybrid type EA in 20-MHz BW LTE test, the overall system PAE for 40-MHz LTE signal of this work is comparable to [9], with even better E-UTRA$_{ACLR}$ of –36 dBc. Moreover, it is expected that the overall system performances exceeds counterparts when the signal bandwidth is wider than 60-MHz. As explained in Section 4.2, further efficiency improvement is expected by using low forward loss diodes [14].

A far-out spectrum (~5 GHz) of the ET PA with 20-MHz BW LTE signal at 25.2 dBm output power is measured. No additional spur or noises are observed in this measurement.

Since our proposed EA does not have switching stage which typically degrades the RxBN performance, the measured RxBN of our ET PA is expected to show better performance than ET PAs with conventional hybrid type EAs. To this end, we have taken RxBN measurement using fully-loaded 5-MHz BW QPSK LTE

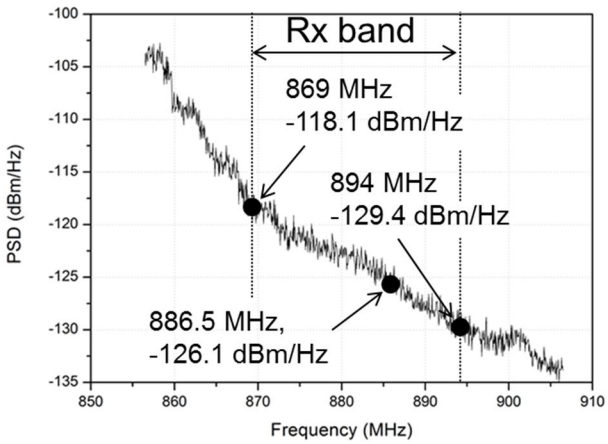


Fig. 4.17. Measured Rx band noise of the ET PA at 25.2 dBm output power. The input signal for the ET PA is 5-MHz BW QPSK LTE signal at 836.5 MHz.

signal with a carrier frequency of 836.5 MHz (LTE band V) at 25.2 dBm output power as shown in the Fig. 4.17. The measured RxBN at 50 MHz offset frequency (886.5 MHz) is –126.1 dBm/Hz, which meets the system requirements if 60 dB attenuation duplexer is assumed to be employed after the ET PA.

Table I compares the performance of the wideband ET PA with other published works. Most of published ET PAs has been tested with 10- or 20-MHz BW LTE signals. Even though the most of reported ET PAs suffer from increased memory effect and decreased efficiency of the EA in wideband signals, the ET PA with the proposed EA can support wideband signal up to 80-MHz.

TABLE 4.1

Performance Comparison Table of the Reported ET PAs for Wideband LTE Applications

Reference	2016/[7]	2015/[6]	2012/[4]	2014[9]	2013/[12]	**This work**
PA Tech.	GaAs HBT	N/A	GaAs HBT	0.28-μm SOI CMOS	GaN HEMT	**0.28-μm SOI CMOS**
EA Tech.	40-nm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.32-μm SOI CMOS	Discrete	**0.28-μm SOI CMOS**
Frequency (GHz)	1.85	1.747	1.74	0.837	9.23	**0.8365**
Signal BW (MHz)	10	10	30	40	60	**80**
Signal Config.	LTE 16-QAM	LTE	LTE 16-QAM	LTE QPSK	LTE-A	**LTE QPSK**
P_{out} (dBm)	27	26	27	25.5	30.2	**25.2**
Gain (dB)	23.8	N/A	29.8	25.1	7.4	**28.6**
Overall system PAE (%)	41.8	40.2	38.5	42.2	32.4	**41.2**
E-UTRA$_{ALCR}$ (dBc)	–34.3	–39.4	–33.4	–34.5	N/A	**–33.5**
RxBN (dBm/Hz)	–130.3[1]	–123.6[2]	N/A	N/A	N/A	**–126.1[3]**

[1]: 10-MHz BW, 80 MHz offset.

[2]: 10-MHz BW, 95 MHz offset.

[3]: 5-MHz BW, 50 MHz offset.

4.5 Conclusions and discussions

4.5.1 Conclusions

In this work, we have developed wideband EA to implement ET PA system that supports 80-MHz BW LTE application. The EA design approach in this work discards the conventional hybrid type EAs to overcome the efficiency and linearity degradation in wideband signal and Rx band noise problem. The proposed EA is composed of bias modulator and diode rectifier current injection circuit, where the output voltage of the EA is controlled by the bias modulator while the diode rectifier current injection circuit boosts the efficiency at a given output level. A detailed analysis to investigate the operation principle and efficiency of the proposed EA is presented, followed by simulation to support theoretical predictions. Both EA and 2-stage RF PA are fabricated in same 0.28-μm SOI CMOS process and entire ET PA system is tested with wideband LTE signals up to 80-MHz. When tested with 80-MHz LTE signal, the overall system PAE reaches 41.2% with –33.5 dBc E-UTRA$_{ACLR}$ at 25.2 dBm output power without the digital pre-distortion. Performance degradation due to the increased modulation bandwidth is characterized using various LTE signals, which shows the ACLR of ET PA in this work is degraded by only 2.5 dB without the PAE degradation. The measured Rx band noise at 50 MHz offset is –126.1 dBm/Hz without any noise reduction technique. This is the first demonstration of the CMOS ET PA system that supports 80-MHz BW LTE signals.

4.5.2 Envelope amplifier operation with modulated signal

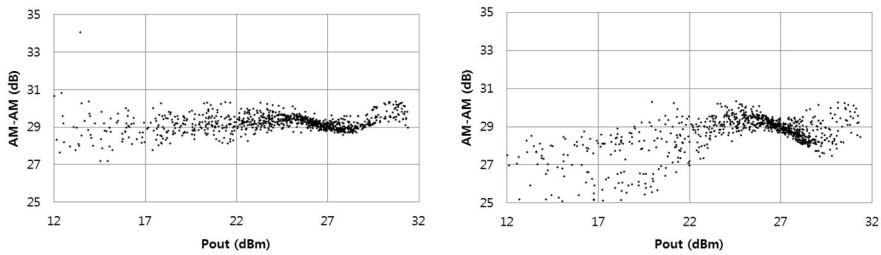
In section 4.2 and 4.3.1 we have analyzed and simulated the entire EA with two input signals. The first one is the re-shaped envelope signal to adequately modulate the drain bias of the RF PA, while the other is CW RF signal which has the same carrier frequency to the input of the RF PA. Even though the simulation and measurement results show successful operation of the EA using those two signals, we should find another substitution for the CW RF signal since baseband chip in modern handsets does not provide additional LO signal.

One of the most promising solution is operating the EA with modulated RF signal instead of CW RF signal which can be simply obtained by coupling the input power for the RF PA. To compare the RF performance of the ET PA system, we have simulated the entire ET PA system as shown in Fig. 4.18 using both CW RF signal ((a), (c), (e), (g)), and modulated RF signal ((b), (d), (f), (h)) at 25.5 dBm output power. For this simulation, the input power of the CW, and modulated RF signal is fixed at 10 dBm in both cases. Phase linearization using dual shaping function is not used in this simulation.

First of all, by comparing the AM-AM profile between two cases, we can observe slight gain compression at the 24~29 dBm output power region in Fig. 4.18 (b). This is mainly attributed to the excessive input power drive to the EA at high power region. This can be easily overcome by modifying the original shaping function to release the gain compression at the high power region. Since the gain profiles are different between two cases, the corresponding AM-PM distortions of two ET PAs are also slightly different as shown in the Fig. 4.18 (c), and (d). Moreover, by comparing the Fig. 4.18 (a), (c) and (b), (d), we can notice that the

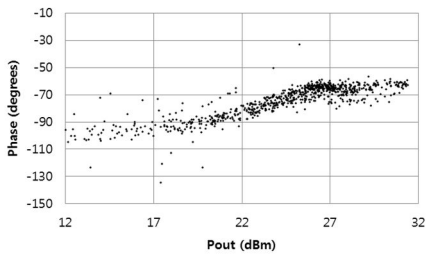
use of modulated signal does not expose additional dispersion. Therefore similar ACLR is expected to be obtained in modulated RF case after linearizing the AM-AM and AM-PM by DPD or analog linearization method.

Figures in Fig. 4.18 (e), and (f) are ac current injection from the diode rectifier current injection circuit. It is worthwhile to note that even though modulated RF signal is used in Fig. 4.18 (f), the amount of ac current injection is almost identical to the Fig. 4.18 (e), which means the use of modulated RF signal does not degrade the overall system PAE. This can be clearly verified by investigating the Fig. 4.18 (f), and (g). The simulated PAE in Fig. 4.18 (g) shows clear PAE break point and efficiency boosting at 27 dBm output power, which has good agreement in Fig 4.18 (f). The simulated overall system PAEs of the ET PA at 25.5 dBm output power in both cases are 45%. From these figures, we can conclude that the modulated RF signal is a good candidate for replacing the CW RF signal.

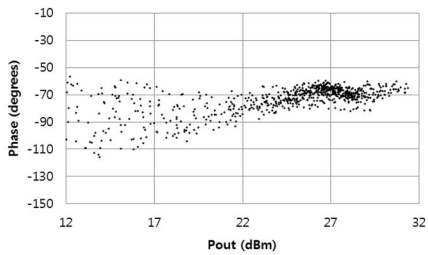


(a)

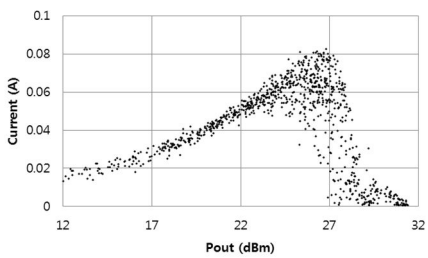
(b)



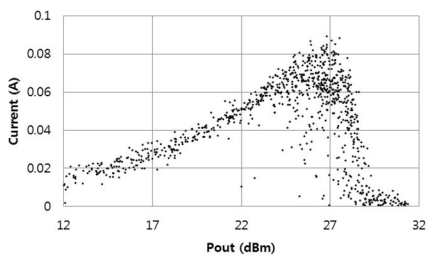
(c)



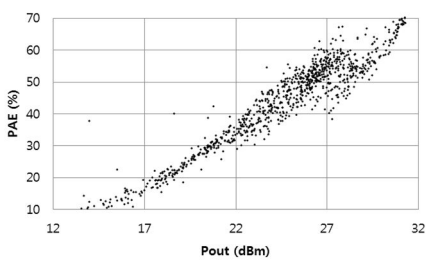
(d)



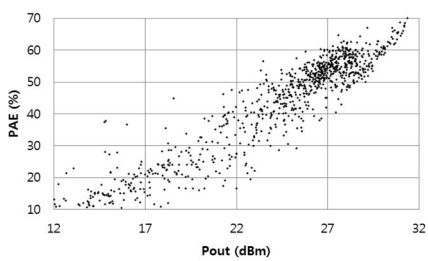
(e)



(f)



(g)



(h)

Fig. 4.18. Simulated RF performance of the ET PA system when the input signal for the EA are CW mode RF signal ((a), (c), (e), (g)), and modulated RF signal ((b), (d), (f), (h)).

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Chapter 5

Conclusions

In this dissertation, three advanced techniques to solve system issues in envelope tracking PAs are developed.

The second chapter demonstrated a CMOS RF PA design that dynamically selects the number of FET in stack which improves the back-off power efficiency while alleviating the high knee voltage limitation of CMOS FETs. The theory is clearly presented and supported with simulation and measurement data. The potential linearity degradation factor during the dynamic switching is identified as a gain and phase step discontinuities and circuit design to prevent linearity deterioration is presented. The proposed ET PA, from a system perspective, demonstrated high efficiency comparing to other CMOS PAs while providing acceptable linearity. Nevertheless, one of the most challenging performance metrics of ET PAs is the out of band noise. It is critical especially for FDD systems (such as 4G LTE). Although TX and RX are separated in frequency domain using duplexers, the attenuation, however, is typically around 50-60 dB. Since, this work proposed using switches to dynamically disable/enable FETs in the stacks, the

quantization noise contributed by the switching behavior needs to be carefully analyzed.

In the third chapter, a wideband phase linearizer to compensate AM-PM distortion of the CMOS ET PA to support 40-MHz BW LTE-A application is demonstrated. The proposed phase linearizer dynamically adjusts the group delay of the modulated input RF signal to flatten the overall AM-PM response. The AM-PM distortion of CMOS ET PAs mechanism is analyzed in device level using equivalent circuit model of the triple stacked FET and verified by the simulation and measurement. Bandwidth limitation of the proposed phase linearizer is carefully investigated using ac simulation of the OTA in the phase linearizer, and envelope simulation of the entire ET PA system. The measured performance shows comparable efficiencies to ET PAs with GaAs, or SiGe HBT RF PAs in 20-MHz BW LTE tests. However, the measured ACLR still does not match to ET PAs with digital pre-distortion due to the limited speed of the envelope amplifier. This is pronounced in 40-MHz test due to the high PAPR and wide bandwidth of the envelope signal. Further advances should be employed in designing the envelope amplifier to reduce the memory effect.

Finally, the fourth chapter demonstrates a novel envelope amplifier to overcome problems inherited from the conventional hybrid type envelope amplifiers. The operation principle and efficiency estimation of the proposed envelope amplifier is investigated using waveform based analysis, and full envelope simulation using LTE waveform is also presented. The implemented ET PA system demonstrated high efficiency with –33.5 dBc ACLR with 80-MHz BW LTE signal. The RxBN measurement is also performed which shows the ET PA with the proposed

envelope amplifier meets the low noise requirement of the LTE FDD system. However, the one of the main drawback of this work is that our proposed EA requires additional CW input signal to operate diode rectifier current injection circuit. Although the use of additional CW signal to the envelope amplifier does not pose any spectral noise issues, the baseband chip in modern mobile phones does not provide CW RF signal for EA operation. Since only available signal is up-converted modulated RF signal, a further work is required to investigate the impact of input modulated signal for EA on ET PA's linearity and efficiency.

초록

본 학위 논문에는 CMOS 포락선 추적 전력 증폭기의 시스템적인 이슈를 해결하기 위한 세 가지의 기술들을 제안하였다.

첫 번째로, 포락선 추적 전력 증폭기 시스템의 저 전압 동작을 위해 동적 FET 스택 조절 기법이 개발되었다. 2 단 전력 증폭기에 사용된 메인 셀은 4 단 스택 FET 구조로써 입력 포락선 신호의 크기에 따라 유사 2 단, 혹은 유사 3 단 스택 구조로 재구성이 된다. 제안된 메인 셀은 낮은 공급 전압 조건에서 트라이오드 영역으로 들어가는 FET 를 우회시키고 로드 임피던스를 최적화 함으로써 모든 FET 들이 포화 영역에서 동작하도록 만든다. 스택을 스위칭하는 시점의 전력 이득과 위상의 계단식 불연속성 현상을 이해가기 위한 자세한 이론적 분석이 소개되었고 인접한 스택 구성에서의 전력 이득과 위상을 동일화 시키는 회로 디자인이 진행되었다. 본 연구에서 제안한 스택이 컨트롤 되는 2 단 전력 증폭기와 포락선 증폭기는 0.32-μm SOI CMOS 공정을 통해 제작되었다. 6.7 dB PAPR 을 가지고 대역폭이 10-, 20-MHz 인 QPSK LTE 신호를 이용하여 LTE 특성을 측정하였다. 10-MHz 신호로 실험한 결과 동적 스택 조절 기법은 25.7 dBm 에서 정적 스택을 이용한 시스템과 비교했을 때 3.5%의 효율 향상을 만들어 47.5%의 시스템 효율, 26.6 dB 의 전력 이득을 얻을 수 있었다. 20-MHz LTE 테스트에 따르면 시스템 효율은 45.9%였고 디지털 선형왜곡 후의 E-UTRA$_{ACLR}$ 은 −33 dBc 였다. 비록 포락선 증폭기의 효율이 최근 발표된 것들보다 낮음에도 불구하고 최대 3.4 V 의 공급 전압을 이용한 본 연구의 포락선 추적 전력 증폭기 시스템은 5 V GaAs HBT 시스템과 견줄만한 성능을 가지고

있다. 이는 본 연구에서 제안한 동적 스택 조절 기법의 장점을 명확하게 보여주는 것이다.

두 번째로, 광대역 LTE-A 를 위한 선형 CMOS 포락선 추적 전력 증폭기 시스템이 개발되었다. 포락선 추적 전력 증폭기의 AM-AM 왜곡은 동-이득 포락선 변형 기법으로 선형화를 시키고, AM-PM 왜곡은 집적된 위상 선형회로에 의해 보상이 되었다. 동-이득 포락선 변형 함수를 작성하기 위한 한번의 교정이 필요하며 이 함수는 위상 선형 회로를 제어하기 위한 신호를 내부적으로 발생시키는 것에 사용된다. 제안된 위상 회로의 대역폭 한계에 관해 조사를 한 결과, 회로 내의 OTA 의 이득-대역폭 곱이 클 경우 더 넓은 대역폭을 지원할 수 있다는 것이 밝혀졌다. 제안된 위상 선형 회로가 집적된 2 단 전력 증폭기는 0.28-μm SOI CMOS 공정을 이용하여 제작되었으며 0.32-μm SOI CMOS 포락선 증폭기와 결합되어 포락선 추적 전력 증폭기 시스템을 구성하였다. 40-MHz 대역폭을 가지고 밴드 내의 두 개의 캐리어가 연속적으로 합쳐진 LTE-A 신호를 이용하여 테스트 한 결과, 시스템 출력 전력이 24 dBm 일 때, 37%의 효율을 얻을 수 있었다. 위상 선형화 후 CA E-UTRA$_{ACLR}$ 은 −25.7 에서 −33 dBc 로 개선되었다. 위상 선형화의 효과를 살펴보기 위하여 40-MHz AM-AM 특성과 AM-PM 특성을 측정하였다. 본 연구에서 제안한 CMOS 포락선 추적 전력 증폭기 시스템은 현재까지 보고된 GaAs, SiGe HBT 시스템과 견줄만한 시스템 효율을 보여주었다.

마지막으로, 종래의 혼성류 포락선 증폭기의 문제를 해결하기 위해 다이오드 정류기와 전류 주입기를 이용한 광대역 포락선 증폭기가 80-MHz 대역 LTE 용으로 개발 되었다. 제안된 포락선 증폭기는 바이어스 변조기와 다이오드 정류기 전류 주입 회로로 이루어져 있다. 제안된 포락선 증폭기의 동작 원리와 효율은 수식과 파형을 기반으로 하여 분석되었다. 본 연구의 포락선 증폭기는 동-이득 기법으로 변형된

포락선 신호와 RF 전력 증폭기의 입력 신호의 캐리어 주파수와 동일한 CW RF 신호를 입력으로 받는다. 포락선 증폭기와 위상 선형 회로가 집적된 2 단 전력 증폭기는 0.28-μm SOI CMOS 공정을 이용하여 제작되었으며, 80-MHz 에 달하는 광대역 LTE 신호를 이용하여 포락선 추적 전력 증폭기 시스템을 테스트하였다. 80-MHz 대역 LTE 신호로 측정한 결과 시스템 효율은 25.2 dBm 에서 41.2%였으며 이 때의 E-UTRA$_{ACLR}$ 은 −33.5 dBc 였다. 변조 대역폭에 따른 특성을 측정해본 결과 대역 폭이 20-MHz 에서 80-MHz 까지 증가함에도 불구하고 시스템 효율은 감소하지 않았으며 ACLR 은 2.5 dB 만이 감소하였다. 5-MHz 대역폭을 가지는 LTE 신호를 이용하여 50-MHz 떨어진 지점에서 Rx 밴드 잡음을 측정한 결과 −126.1 dBm/Hz 로써 시스템 요구사항을 만족했다. 본 연구를 통해 80-MHz 대역폭을 다룰 수 있는 포락선 추적 CMOS 전력 증폭기를 최초로 제안하였다.

주요어 : AM-AM, AM-PM, 반송파 묶음, CMOS, 파고율 저감, 디지털 선형왜곡 (DPD), 다이오드 정류기, 동적 스택 조절, 효율, 포락선 증폭기, 포락선 추적 기법 (ET), 선형회로, LTE, LTE-A, 전력 증폭기, Rx 밴드 잡음, SOI, 스위칭 잡음, 광대역.

학번 : 2012-30219