Ph.D. DISSERTATAION

Fabrication and Characterization of GaN-on-Si based RF and Power Devices

GaN-on-Si 기반의 고주파/고전력 소자의 제작 및 특성 분석

BY

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Abstract

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Owing to the unique capabilities of achieving high current density, high breakdown voltage, high cut-off frequency and high operating temperature, AlGaN/GaN high electron mobility transistors (HEMTs) are emerging as promising candidates for RF power amplifier and power switching devices. Nevertheless, despite the great potential of these new technologies, they still suffer from physical and fabrication issues which may prevent devices fabricated on GaN from achieving the performance required. This thesis presents a comprehensive study on the development of GaN-based high frequency, high power transistors.

This work can be divided into two parts, namely D-mode AlGaN/GaN schottky

HEMTs on silicon substrate for high power X-band operation and E-mode Si_3N_4/AlGaN/GaN metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HFETs) for power switching devices.

One of the main obstacle is the trapping effects, may be exacerbated when devices are operated in Radar systems. In this work, we will use a novel fluoride-based plasma treatment technique to reduce trapping phenomenon which originated from the surface, and then apply this treatment technique in conjunction with a field plate structure to a device for GaN-based RF applications. To improve overall device performance, a backend process with individually grounded source via formation has been developed to integrate large periphery devices. Based upon it, GaN HEMT amplifier with single chip of 3.6 mm gate periphery has been successfully developed. It exhibits very high power density of 8.1 W/mm with 29.4 W output power under V_{DS} = 38 V pulse operating condition.

Compared to the conventional depletion-mode AlGaN/GaN (D-mode), Enhancement mode (E-mode) devices are attracting a great interest as they allow simplistic circuity and safe operation. It is difficult to obtain E-mode operation with a low on-resistance and a high breakdown voltage. A gate recess technique will be crucial to realize an enhancement-mode operation and improve the transfer characteristics. To reduce the on resistance and enhance the drain current density, partially recessed MIS-HFETs are investigated. The gate recess was carried out using

a low-damage Cl_2/BCl_3-based RIE where the target etch depth was remains AlGaN barrier layer in order to improve the transfer characteristics. The occurring degradation of the mobility due to plasma etching-induced damage and scattering effect were effectively removed by partial gate recess technique. The technologies we developed have helped to give definitive direction in developing GaN-based high frequency, high power transistors.

Keywords: AlGaN/GaN HEMTs, Power density, X-band, Amplifier, Individually source via (ISV), Recessed metal-insulator-semiconductor (MIS) structure

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Chapter 1

Introduction

1.1 Background

The silicon technology is by far the dominant semiconductor industry [1]. The down scaling technology of Si based device is extending the performance of the silicon channel to its limit [2, 3]. Hence, compound materials, GaAs, SiGe, SiC, InP, II-VI and III-V have received significant attention to replace or to complement silicon.

The III-V compounds, such as GaAs, InGaAs and InAs exhibit outstanding electrion transport properties [4]. Transistors based on these materials are not being used in high power and high temperature applications because they have relatively narrow band-gap. Some III-V compounds semiconductors are used in light emitting diodes (LEDs) and detectors for optoelectronic devices. Driven by surging demand from the military and commercial wireless communications applications, the group III nitrides have continuously received attention [5, 6]. Among the group III nitrides, gallium nitride (GaN) has relatively large direct band gap. In particularly, enormous progress has been made in developing AlGaN/GaN high electron mobility transistors (HEMTs) as attractive candidate for high power, high efficiency microwave transistor amplifiers and switching devices [7-10]. The material properties of GaN compared to competing materials are presented in Table 1.1. The high charge carrier mobility and

high saturation velocity are important parameters to achieve high currents and high frequency operation. Gallium arsenide (GaAs) is the most studied compound semiconductor material. A primary advantage of fabricating transistor from this material is higher mobility and saturated drift velocity, which are capable of handling or providing high frequency operation. The electron mobility is approximately six times greater for GaAs than for silicon. The maximum GaAs drift velocity mobility is twice that of silicon for field strengths less than 2 x 10^4 V/cm. These advantages are attractive for space and military applications. GaAs has some problems. It has narrow band-gap results in a low breakdown field. This means that it is not suitable of the application of high operation voltage which limiting the output power density [11].

As the performance requirements of power amplifiers have increased to meet the growing demand, the research effort has been focused in developing wide band-gap semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) [12]. Due to its wide bandgap, GaN has superior material properties such as higher blocking voltage, higher operating temperature, and faster switching speeds [13]. The high saturation velocity leads to high saturation current densities and allows the fabrication of smaller size device with the same output power. Higher impedance allows for lower loss matching in amplifier. The high carrier concentration and high electron mobility leads to a low on resistance $R_{on,}$ which is important for switching devices [14-17].

TABLE 1.1[18]

COMPARISON OF PHYSICAL PROPERTIES OF GALLIUM NITRIDE WITH OTHER MATERIALS

Properties	Si	GaAs	4H-SiC	GaN	AlN
E_g	1.12	1.43	3.2	3.4	6.2
E_c (MV/cm)	0.25	0.3	2.2	3.3	1.2-1.4
ε_r	11.9	13.0	10.0	9.5	9.14
μ_n ($cm^2/V{\cdot}s$)	1300	8500	700	1600	300
v_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	
λ (W/cm·K)	1.5	0.5	3.5-5.0	1.3	2.85
Melting point(^oC)	1412	1240	>3000	>2500	>3000
JM	1	2.7	20	27.5	

E_g: Bandgap

E_c: Critical field

ε_r: Dielectric constant

μ_n: Electron mobility

μ_p: Hole mobility

v_{sat}: Saturation velocity

λ: Thermal conductivity

JM : Johnson's figure of merit

GaN-based materials have already demonstrated high power and high frequency performance that exceeds that of a much more mature GaAs technology. The performance is remarkable due to their ability to make hetero-structure in a material system. The large electron sheet densities and high motilities have been correlated to the spontaneous and piezoelectric polarizations [5, 18]. The most common growth direction of GaN is the normal to the [0001] basal plane, where the atoms are arranged in bilayers. These bilayers consist of two closely spaced hexagonal layers leading to polar surface, one with cations and the other with anions [19]. In the case of GaN, a basal surface should be either Ga- or N-faced as illustrated in Fig. 1.1 [18] . It should be note that the properties can depend significantly on whether the surface is faced by nitrogen or metal atoms. As a consequence of the noncentrosymmetry of the wurtzite structure and the large ionicity factor of the covalent metal-nitrogen bond, a large spontaneous polarization oriented along the hexagonal c-axis is predicted.

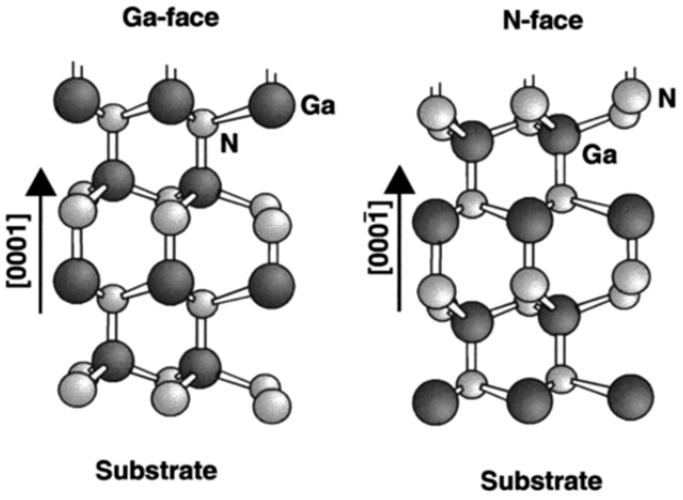

Fig. 1.1. Schematic drawing of the crystal structure of wurtzite Ga-face and N-face GaN [5].

The spontaneous polarization can cause electric fields of up to 3 MV/cm in group-III-nitride crystals, and strain in pseudomorphically grown AlGaN/GaN or InGaN/GaN heterostructures can cause an additional piezoelectric field of about 2 MV/cm[20]. These very high polarizations and resulting electric fields produce high interface charge densities at group-III-nitride interfaces and spatial separation of the hole and electron wave functions in GaN-based quantum well structures [21, 22].

In order to fully realize the potential of AlGaN/GaN structures, the key mechanisms controlling the formation of the 2DEG at the AlGaN/GaN interface must be well known [23-25]. It has been shown previously that piezoelectric effects can exert a substantial influence on charge density and electric field distributions in zincblende semiconductors grown in the (111) orientation, and the wurtzite crystal structure grown in the (0001) orientation [26, 27]. It has been shown that AlGaN/GaN heterojunction field effect transistors HFETs contain sheet carrier concentrations in the two-dimensional electron gas (2DEG) well in excess of 10^{13} cm^{-2} even in the absence of doping [28-30]. It is reported that unintentional dopants, interface states at the AlGaN/GaN interface, deep-level defects, and surface states may contribute on the 2DEG. Among several different theoretical models to explain the source of these mobile carriers in the two-dimensional gas, the most widely accepted one is that the 2DEG originates from the donor states on the AlGaN surface [31].

1.2 Substrate for Epitaxial Growth of GaN

The GaN devices have relies on hetero-epitaxial approaches by employing a variety of substrates including SiC, silicon, and sapphire substrates for development and industrial production of blue, green and white high brightness LEDs for lighting and high-power and high-frequency electronics. However, their performance is limited by the structure quality of the materials; improvement of crystalline quality of epitaxial grown GaN films is still a very important issue. It is well known that disadvantages of the heteroepitaxy, such as biaxial induced stress, mosaic crystal structure, and high density of threading dislocation which arises from a large lattice mismatch and the difference in thermal expansion coefficients between GaN and the substrates [32]. An additional drawback of most of the foreign substrates used for nitride-based devices is their low thermal and electrical conductivity. High power devices often require high output power and high current density, leading to high temperatures in the devices via self-heating, which reduce the device performance [33]. The choice of the substrate is crucial. Table 1.2 shows each of substrate options including freestanding GaN, SiC, sapphire and silicon has merits and short-comings. The data shows that an ideal substrate for a GaN epitaxial film will be a GaN itself, however, this approaches is limited due to difficult to be grown free standing GaN until now. Heteroepitaxial growth of GaN is usually performed on sapphire or SiC. Most of the advancements in epitaxial growth were first achieved on sapphire due to its availability, but it also has a high lattice mismatch and thermal mismatch to GaN.

SiC substrate is the very attractive substrate materials for fabricating RF power devices because of its high resistivity and high thermal conductivity compare to sapphire substrate. However, SiC substrate is very expensive and makes it difficult to have large diameter substrate technology. In particular, AlGaN/GaN grown on Si is becoming the mainstreaming technology due to high-quality, large area, and the cost advantage.

TABLE 1.2

Substrates for GaN epitaxial wafer

	Typical dislocation density ($/cm^2$)	Thermal conductivity (W/cm·K)	Lattice mismatch with GaN (%)	CTE difference with GaN (%)	Wafer size (Max.)
SiC	$5x10^6$	4.9	3.5	25	4"
Sapphire	$\sim10^8$	0.33	16	34	6"
GaN	$\sim10^5$	1.3	0	0	2"
Si	$\sim10^9$	1.3	17	54	8"

1.3 Research Aims and Objectives

AlGaN/GaN High Electron Mobility Transistors (HEMTs) are widely investigated for high frequency operation and power switching applications. The requirement for high power and high frequency requires transistors based on semiconductor materials with both large breakdown voltage and high electron velocity. The combination of high carrier concentration and high electron mobility results in a high current density and a low channel resistance [34]. Although significant progress has been achieved in the growth and processing technology for GaN has been achieved, there are still remain immediate solution. The GaN devices are mostly depletion-mode schottky gate HEMT. For power switching device, enhancement mode or normally-off devices would be preferable since it provide the desirable safe operation [16, 35]. Thus, the development of enhancement-mode (E-mode) GaN HEMTs has become essential to expand the range of their applications. E-mode GaN HEMTs enable a circuit to be simple, because the voltages applied to the gate and drain electrodes can be of a single polarity, and safety components can be omitted [36].

The main aim of this work is to develop E- and D-mode transistors technology with the following attributes:

For D-mode device: a high breakdown voltage characteristic, a low RF dispersion and a low source inductance using inductively source via process.

For E-mode device: a positive threshold voltage, a low specific on-resistance, a high drain current density and high breakdown voltage.

1.4 Organization of Thesis

The research work is focused on device design, fabrication process development, and device characterization. This thesis is divided into 6 chapters. This chapter gives a brief introduction of wide-bandgap materials properties and why gallium nitride (GaN) has been attracted in high frequency and high power applications.

Chapter 2 describes the fabrication process development of AlGaN/GaN HEMTs grown on Si substrates. Starting with etching technique for mesa isolation and ending with technology of air-bridges.

Chapter 3 discusses ICP etching as a way of fabricating vias with a tapered via sidewall and an elimination of the scalloping that result from the Bosch process. Then, the two-step etching process was proposed to control the angle of the sidewall for fabricating individual source via (ISV).

Chapter 3 gives an overview of the processing techniques for X-band operation. It describes the fabrication method used throughout the work to solve the problems faced by manufacturers. By the improved processing technique could be incorporated into the AlGaN/GaN HEMT process that is used to eliminate the DC-RF dispersion. A field plate structure in conjunction with a sloped gate profile was fabricated in this

work to effectively suppress the high electric field at the gate corner. Then, Wide-periphery was implemented with individual source via (ISV) process which provides very low inductance grounding to the source connection. The result of the performance of the devices are analyzed and discussed.

Chapter 5 presents the fabrication and characterization of the enhancement-mode MIS-HEMTs which employ PEALD SiN_x as a gate dielectric. The influence of the gate recess process variables is studied. The device performance of normally-off recessed-gate AlGaN/GaN MIS-HEMTs with and without thin AlGaN barrier will be presented. The comparison study on C-V measurements and the drain current transient measurement for recessed-gate AlGaN/GaN MIS-HEMTs was performed to study the influence of partial recess etching process. The improvement in on-resistance and trap characteristics will also be shown. The measured D.C and dynamic performance of AlGaN/GaN MIS-HEMTs will also be presented in this chapter.

Chapter 6 provides summary of the research project as well as the discussion for the potential future work.

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Chapter 2

Fabrication of AlGaN/GaN HEMTs on Si substrate

2.1 Introduction

This chapter will give the fabrication process of AlGaN/GaN based devices. The standard HEMT technology process will be described starting with the sample preparation through mesa isolation, ohmic contacts, Schottky contacts, and air-bridge technology. The basic process steps will be described and discussed. The processed HEMT in this work are based on AlGaN/GaN heterostructure grown on silicon substrate. To begin with, the epitaxial layer structures which we used in the experiment are outlined. Starting from the basic HEMT structure we have introduce different gate structure modifications to achieve the Schottky HEMT and MIS-HEMT devices.

2.2 Epitaxy Layer Structure

For a GaN HEMT structure, a crystal-wafer such as sapphire, silicon carbide, or silicon is employed as a base substrate. AlGaN/GaN heterostructure field-effect transistors (HFETs) have been widely investigated over a broad frequency range with nearly all structures heteroepitaxially grown on sapphire or silicon carbide (SiC) substrates [1]. Semi-insulating SiC substrate is the most successfully used for demonstration of high-power GaN-based HEMT because of its very high thermal conductivity compared to Silicon. GaN HEMTs on Si substrate become an alternative approach because of its low cost and mass production capabilities [2]. The easy etching of Silicon substrate offers also the opportunity to achieve self-supported GaN thick films or device transfer onto another substrate [3]. The HEMT epitaxial layer structure grown on silicon substrate starts with a monocrystalline AlN nucleation layer to reduce the misfit between Silicon and GaN buffer layer [4]. About $Al_xGa_{1-x}N$ barrier on top of the GaN buffer layer forms the two-dimensional electron gas (2DEG) at the $Al_xGa_{1-x}N$/GaN interface. This 2DEG mobility is affected by Al more fraction of the barrier and AlGaN barrier thickness. Increasing the Al mole fraction in the AlGaN layer will lead to higher, but will drop due to alloy disorder scattering and the crystal quality may degrade as well [5]. The 2D-electron lie very close to the AlGaN/GaN interface, which makes them very susceptible to any physical processes occurring at the interface such as interface roughness scattering, which is the dominant scattering mechanism at low temperatures. In order to alleviate such affects,

the separation between the 2D-carriers and the interface needs to be increased, which can be achieved if the AlGaN/GaN structures are capped with a GaN layer of appropriate thickness [6].

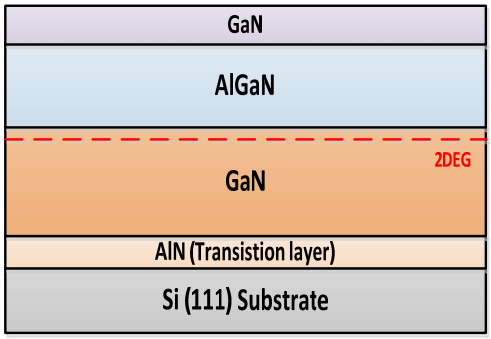

Fig 2.1 GaN HEMT structure based on Si (111) substrate.

2.3 Device Fabrication Processes

Device fabrication was carried out in the Inter-University Research Center, Seoul National University. The following will outline the process to take surface preparation through to the complete working device stage. The details were as follow:

2.3.1 Sample Preparation

The surfaces and interfaces between the various layers of semiconductor device structures are fundamental components of solid state architecture. As device size has diminished and the scale of integration has increased, the quality of these interfaces has become an increasingly important concern [7]. Surface cleanness is critical for the proper device operation. Although, a number of groups have investigated GaN cleaning procedures for device fabrication, there is no standard method of GaN surface cleaning due to the surface of the GaN is very sensitive and unique different from other III-V semiconductors. A typical surface cleaning may include organic solvent treatment and acid etches which are effective in removing the surface oxides and other contaminations. The samples are initially immersed in a glass beaker of acetone and placed into an ultra-sonic bath for 30 minutes. The acetone is then removed by placing the sample into methanol and isopropyl alcohol for 15 minutes in order. The surface cleaned with a mixture H_2SO_4/H_2O_2 (SPM cleaning) after solvent cleaning. After that samples are dips for 10 minutes in 10:1 diluted HF followed by rinse deionized water and dried with nitrogen. This procedure ensures that any contaminants are removed.

2.3.1 Mesa Isolation

Mesa isolation is an important step in fabrication of HEMT devices. Creation of islands of active layer on the sample interrupts the conductive 2DEG and provides an electrical insulation between two neighbor structures. The depth of mesa insulation has to be done with respect to the position of 2DEG [8]. Dry etching method provides a reliable pattern transfer compared to wet etching due to chemical stability of GaN. Previous work has investigated several various dry etching techniques such reactive ion etching (RIE), electron cyclotron resonance (ECR), and inductively coupled plasma (ICP). The chlorides of Ga, Al, and N are relatively volatile, making Cl_2, BCl_3 , and $SiCl_4$ the primary reagents used to etch III-N group materials [9]. Optimum etch strategies for the mesa isolation demand low plasma-induced damage, smooth surface and moderate etch rate. In this work, inductively coupled plasma reactive ion etching (ICP-RIE) using Cl_2-based gas mixtures was investigated. ICP power/RF power, operation pressure and Cl_2/BCl_3 gas ratio are altered to investigated results of etch rates and etched profiles. Satisfactory quality of mesa structures was obtained with a source RF power of 350 W, a bias RF power of 10 W, gases relation 2 sccm of BCl_3 /18 sccm of Cl_2 and a chamber pressure of 5 mTorr. The GaN etch rate was 5 Å/sec. One of the problems had to be solved was the choice of the right mask to perform the etching. With higher ICP/RF power can obtain higher GaN/photoresist etch selectivity, it can result in faceting of sidewall and weird sidewall profile due to photoresist mask erosion [10]. The SEM image of GaN

etching profile was shown Fig 2.2. It is observed that the PR mask is severely damaged by the energetic ion reaction during the ICP-RIE. In the case of the Ni mask, obtained sidewalls and roughness of etched surface were suitable for device fabrication.

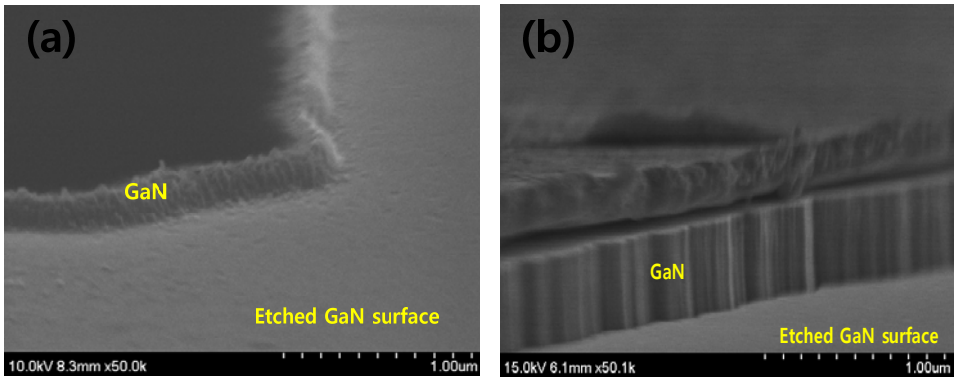

Fig 2.2 SEM images of a GaN mesa structure etched.

ICP-RIE by used resist mask (a) and Ni mask (b)

2.3.2 Ohmic Formation

Ohmic contacts of HEMT devices are critical parameters because the saturation current and transconductance are very sensitive to contact resistance. Low contact resistivity is very important to achieved excellent performance in these devices. Due to its wide-bandgap and high barrier height ohmic contact formation with low contact

resistance is more difficult to form. The mechanism of the ohmic contact formation has been proposed, namely, low Schottky barrier mechanism and tunneling contact mechanism. Ti-based multilayer metallization schemes for n-GaN with low contact resistance have been demonstrated [11]. The reaction of Ti with GaN to form TiN is essential in achieving low contact resistance. The formation of TiN layer during annealing leads to a smaller barrier height and thus a higher probability of carrier transport. In the tunneling contact mechanism, the N vacancies, created in the GaN layer by interfacial reaction during annealing, generate a heavily n-doped layer at the surface of the semiconductors which induces a large band bending [12-16]. There are a lot of studies dealing with ohmic contacts layers on GaN in the literature [17-21]. In this section, Si/Ti/Al/Mo/Au ohmic contact was suggested and optimized for low contact resistance. The epitaxial layers used in this work grown on Si substrate consisted of a 20 Å GaN capping layer, an 175 Å $Al_{0.26}GaN$ barrier layer, an 1 mm GaN buffer layer, and AlN/GaN transition layers from top to bottom. The steps for transfer length measurement (TLM) test structure fabrication were the following: (1) contact pad patterning using optical lithography, (2) recess etching using BCl_3/Cl_2 plasma in an inductively coupled plasma reactive ion etching system to reduce the distance between 2DEG and metal contacts, (3) Si/Ti/Al/Mo/Au multilayered metal contacts were evaporated, (4) the contacts were annealed in a rapid annealing system with a N_2 ambient. The ratio Ti/Al and annealing temperature plays an important role to achieved low contact resistance. To identify the effect of Ti/Al ratio with different

annealing temperature on the Ohmic performance of Si/Ti/Al/Mo/Au scheme, TLM analysis was carried out on Si/Ti/Al/Mo/Au schemes to extract values of contact resistance R_c. Lower contact resistance have been obtained in the case of ratio Ti(20 nm)/Al(80 nm) and this metal scheme turned to be ohmic at relatively lower annealing temperature. Shown in Fig 2.4 is the cross-section view of Si/Ti/Al/Mo/Au (=5/20/80/35/35 nm) at 780 °C for 60 sec. Intermetallic and interfacial reactions appear to be similar to that of Ti/Al based metal schemes where complex intermetallic reactions and vigorous interfacial TiN formation along dislocations have been observed [22, 23].

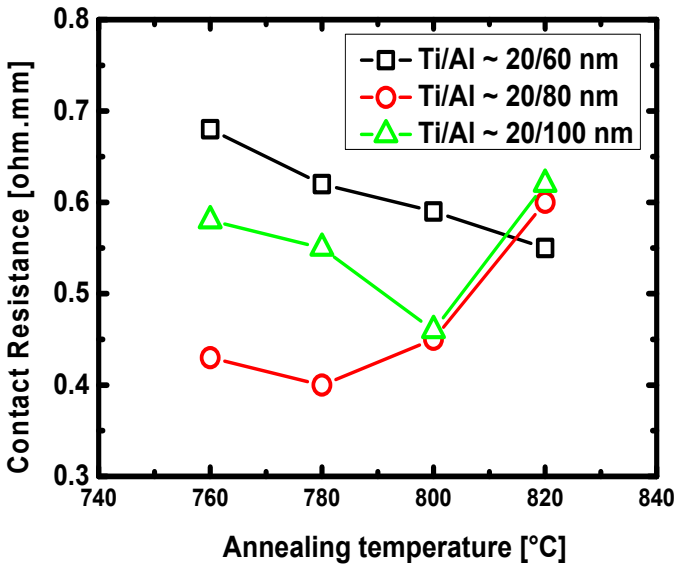

Fig 2.3 Variation of contact resistance (R_c) as a function of annealing temperature in RTA.

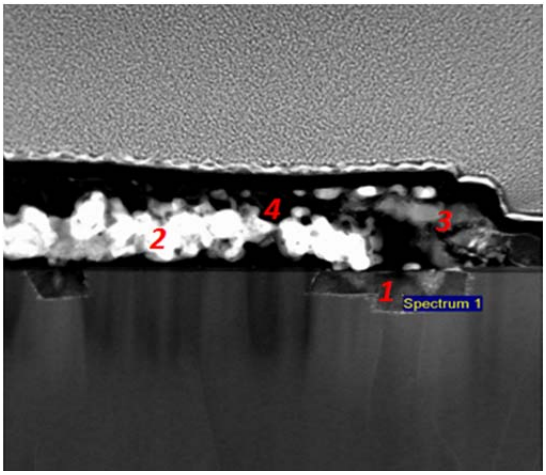

Fig 2.4 Cross-section STEM micrographs of Si/Ti/Al/Mo/Au (=5/20/80/35/35 nm) at 780 °C for 60 sec.

Table 2.1 Percent elemental composition of regions identified by the numbers indicated

No	Ti K	Au M	Mo L	Al K
1	85.37	14.63		
2		100		
3	3.59	4.41	90.95	1.06
4	33.84	61.81		4.35

2.3.3 Schottky Contacts

Schottky contacts are used as the key element for device operation where the width of the depletion layer underneath the Schottky barrier is to be controlled precisely as desired [24]. For an AlGaN/GaN based high electron mobility transistors, a Schottky gate contact with a large barrier height is critical factor to achieve low gate leakage current and high breakdown voltages. It has been shown that there is a large variation in the barrier height for different metal deposition onto GaN by various researchers. In this work, we present our results on the Schottky barrier properties of various metals (Ni/Au, Ni/Ir/Au, Pd/Ir/Au, Pt/Au and Ir/Au) on n-type GaN. Ideality factors and barrier heights were measured using I–V measurements. The barrier heights and ideality factors of various metals were determined using the thermionic emission theory given by

$$I = I_s\{exp[q(V - IR)/nkT] - 1\}$$

$$\text{where } I_s = AA^{**}T^2\exp(-\frac{q\phi_b}{kT})$$

where I_s is the saturation current, R is the series resistance, n is the ideality factor, T is the measurement temperature, A^{**} is the effective Richardson constant, A is the area and φ_b is the measured barrier height [25]. Table 2.2 summarizes a comparison of the electrical properties of the diodes consisting of bi-layer Schottky metals (Pt/Au and Ir/Au) and those of a tri-layer (Ni/Ir/Au, and Pd/Ir/Au). Each barrier height was found to be sensitive to contacts metal with several of the inserted metal. The parameters of

the as-deposited devices are considered to be determined whether the metal in contact with GaN is Ir or Pt as the diode with Ir/Au electrode had better values than that of Ni due to its higher work function. This can be seems that higher Schottky barrier should have been realized in those structures.

Table 2.2 Electrical parameters of various Schottky diodes on n-GaN

	As-deposit	
Schottky metal	$_{B}$ (I-V) (eV)	Leak at -100 V (A/mm)
Ni(20 nm)/Ir(20 nm)/Au	0.76	8E-6
Ni(3 nm)/Ir(20 nm)/Au	0.65	5E-6
Pd(3 nm)/Ir(20 nm)/Au	0.88	7E-6
Ir(20 nm)/Au	0.81	2E-8
Pt(40 nm)/Au	0.72	3E-7

As seen, the measured barrier heights can vary significantly between authors as is the case with Ni, Pt, Au, and Ir [25-29]. The discrepancy with our result would be related to the results of various factors such as the surface state of each GaN epilayer,

different defects present in the material and the preparation procedure for metal deposition.

2.3.4 Contact Pads

Contact pads have to be fabricated by using e-beam evaporation. The metal used for the contact pads is Ni (40 nm)/Au(360 nm) on top of GaN layer. Ni is used to provide good adhesion to the Gan surface. To prevent contact pads peeling-off during wire-bonding or thermal annealing process. Fabricated pads have to be stable at higher temperatures and have to be mechanical resistant. Solvent cleaning and O_2 plasma cleaning is necessary prior to the contact metal deposition step.

2.3.5 Air-bridge Interconnection

The multi-finger devices can be easily interdigitated to increasing output current and the power handling by making use of the air-bridge metal interconnection. After contact pads are made, the final step of multi-finger device processing is to connect the deposited contact pads and source metals using an air-bridge interconnect technique. The following will outline the air-bridge fabrication process in shown Fig 2.5.

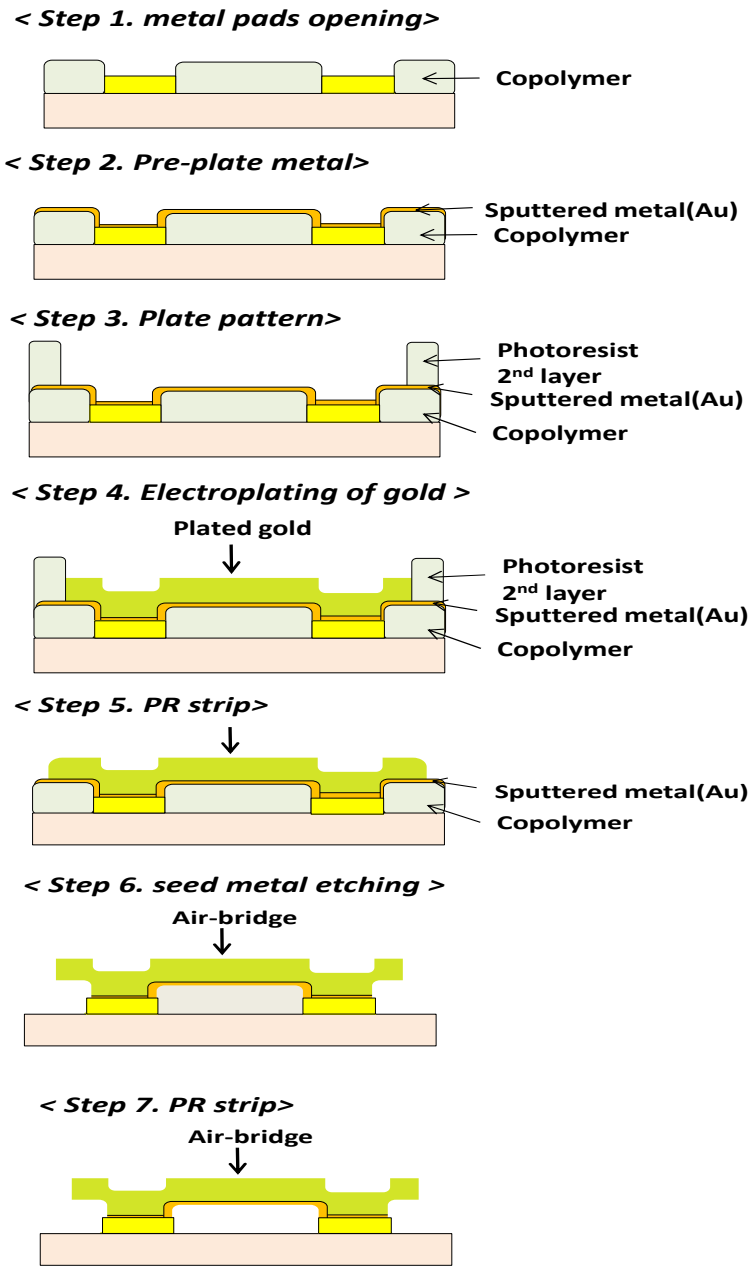

Fig 2.5 Air-bridge fabrication process flow

Air-Bridge Post

Air-bridge fabrication starts with air-bridge post material lithography step. We coated the copolymer resists as the air-bridge post material and then use AZ 4330 photoresist for photolithography process. Copolymer thickness is about 3.5 μm. It is etched away with RIE using O_2 plasma will be enough to make the bridge. And then, AZ 4330 was cleaned in acetone. Copolymer resist reflow process is applied at 210 ^{o}C for 3 minutes in order to achieve mechanically stable air-bridge formation. AFM measurement results of an air-bridge post before and after the reflow process are given in Fig 2.6.

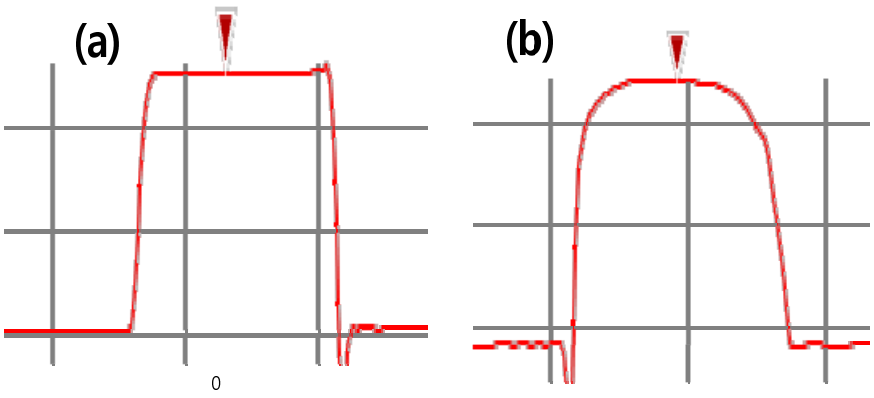

Fig 2.6 An air-bridge post profile before (a) and after (b) reflow process

Seed layer

Seed layer is formed by sputtering Ti (50 nm)/Au (200 nm) in order to form a conductive surface which required in gold electroplating process. Au was the major component of metal with Ti as an adhesion promoter to the semiconductor.

Air-bridge

After the seed metal is formed, lithography process is done using AZ 4620 photoresist to define the horizontal extent of any plated geometry whether it is part of an air-bridge or in contact with underlying metal. A 10 μm thick photoresist was carried out in order to 4 μm thick gold electroplating process.

Removal of the seed layer and air-bridge post

Removing of seed layer and post material is the most critical steps of the HEMT fabrication process. After Au electroplating, photoresist pattern was strip away by solvent. For seed layer stripping, wet processing is commonly used. However, it undercuts the plated gold line while wet processing can remove the seed layers. It causes excessive loss of plated metal, and raises uniformity and safety issues. The seed layer is removed by HF-based wet etchant as shown Fig 2.7.

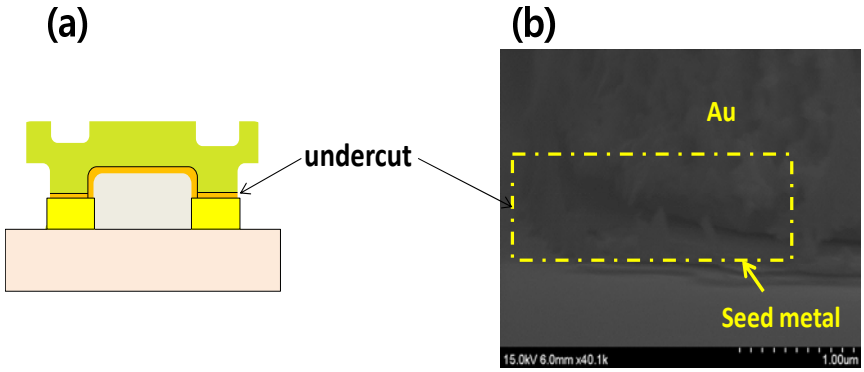

Fig 2.7 Schematic diagram of electroplated structure (a) and SEM images of (b) after seed-layer etch

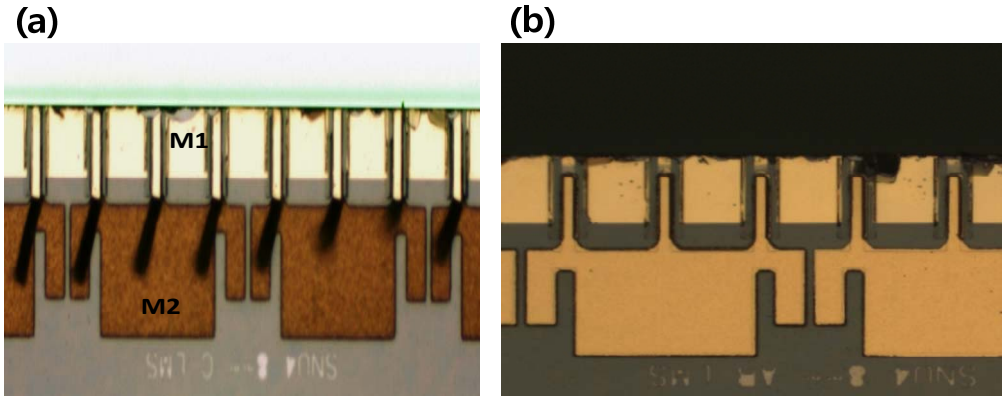

Fig 2.8 Adhesion test through dicing saw after seed-layer etching by (a) wet process and (b) dry process

Wet etching of gold usually results in an isotropic profile but in the presence of another metal, a vertical or reentrant profile with much greater undercut is often observed is shown Fig 2.7. This typically occurs when etching a gold film with an underlying adhesion layer of Cr, Ti or TiW. Such effects have been noted by a number of authors, and it is thought to be caused by the two metals forming a galvanic couple [30].

Adhesion problem which related to undercut profile is still important for fabricating gold-plated interconnects in GaN HEMT devices. Fig 2.8(a) shows that removing a simple Ti/Au seed layer by wet etching proved unsuccessful because undercut the plated gold line during the seed metal removal process. The high stability and superior adhesion make the dry etching process well suited for electroplating process in Fig 2.8 (b). Using the gold etchant is prone to undercutting arising from galvanic effects. Dry methods which utilize reactive ion etching have a number of important advantages over other methods. Finally, air-bridge post should be removed by chemicals or alternatively oxygen plasma process. We tested several approaches such as acetones with ultra-sonic and oxygen plasma for resist stripping. In case of O_2 plasma ashing, air-bridge post was removed without any residue.

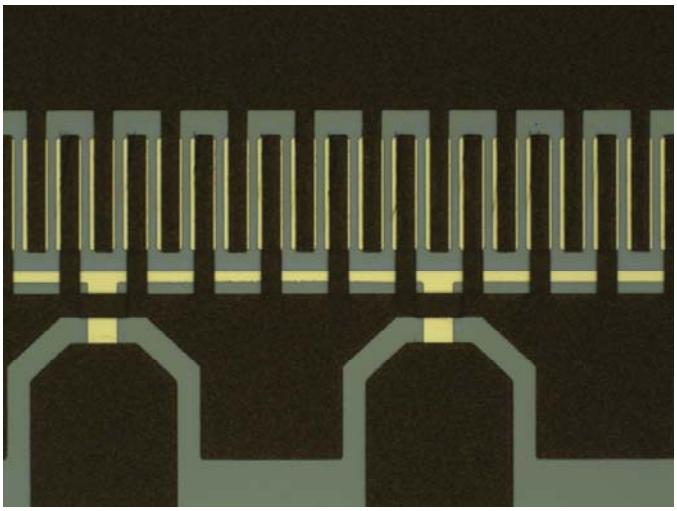

Fig 2.9 Photo of the fabricated air-bridges

2.4 Reference

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Chapter 3

Au-Plated Through-Wafer Vias for AlGaN/GaN HEMTs on Si substrate

3.1 Introduction

This chapter will describe backend process of large periphery device for X-band. After transistors are fabricated, electric connection through the backside via is often used to further improve device performance [1]. Backside via holes is necessary to provide reliable grounding paths in devices and circuits. In addition, it reduces source inductance and results in higher gain and power at millimeter wave frequencies [2, 3]. Minimization of source inductance has been previously demonstrated on the GaAs PHEMT-based MMIC's by the use of individually grounded source finger vias [4]. Dry etching by Inductively Coupled Plasma (ICP) of GaN is a promising candidate for backside via etching because of the excellent chemical stability. Wafer thinning and backside metallization technology can be used for forming via-holes.

3.2 Via-hole Fabrication

Bosch process is widely used in the fabrication of through silicon via (TSV) holes for 3-D integrated circuit and 3-D Packaging applications mainly due to its high silicon etch rate and selectivity to mask [5-8]. Bosch etch process consists of series of isotropic etching and passivation steps caused by rapid switching between etch and passivation process which is normally integral in a reactive ion etch process [9-11]. Common Bosch process has highly vertical profile sidewalls and high aspect ratio. Bosch processed TSV cross-sectional sample images are shown in Fig 3.1. In the Bosch process, Scallops are formed during the silicon etching step. While it is difficult to achieved smooth sidewalls due to switching between etch.

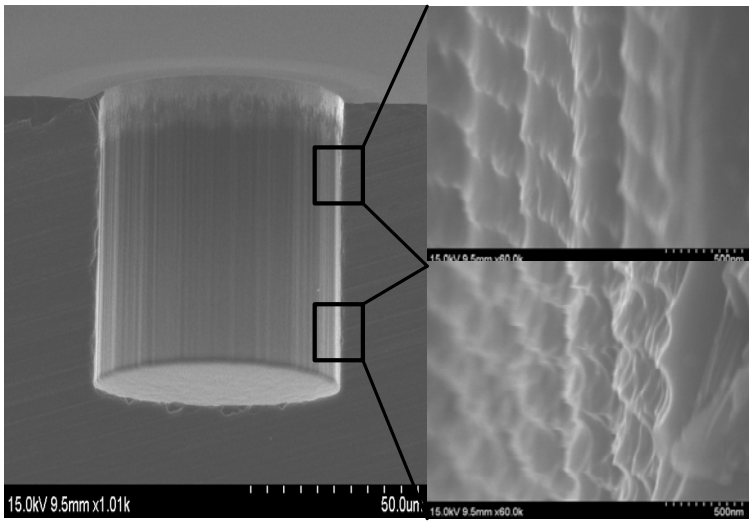


Fig 3.1 SEM cross sectional views of a via from Bosch process

3.2.1 Experiments

The main motivation for via tapering is that it helps in conformal deposition of Au seed metallization over the sidewalls of the deep silicon vias [12-15]. Fig 3.2 (a) and Fig 3.2 (b) show the vias after gold electroplating has been done. In both these cases, the gold electroplating process results in trapped voids inside the via structures. This result caused by the electroplating reaction rate is more at the top than at the bottom due to rapid replenishment of plating solutions. The results thus indicate that either the gold electroplating process needs improvement or the top corner of the via needs to be tapered in order to eliminate the voids from forming during gold electroplating process.

It is possible to suit specific needs in the fabrication process of AlGaN/GaN HEMTs with individually grounded source finger vias. It further enables a void free gold via electroplating. To utilize the individually grounded source finger vias, source via profile should be change vertical profile to taper shape. The via tapering process can easily formed either by modifying the conventional SF_6/C_4F_8 based Bosch process or by using SF_6/O_2 based etching process [16, 17]. In this chapter, we demonstrate backend process with individually grounded via-hole for X-band GaN HEMTs using ICP etching.

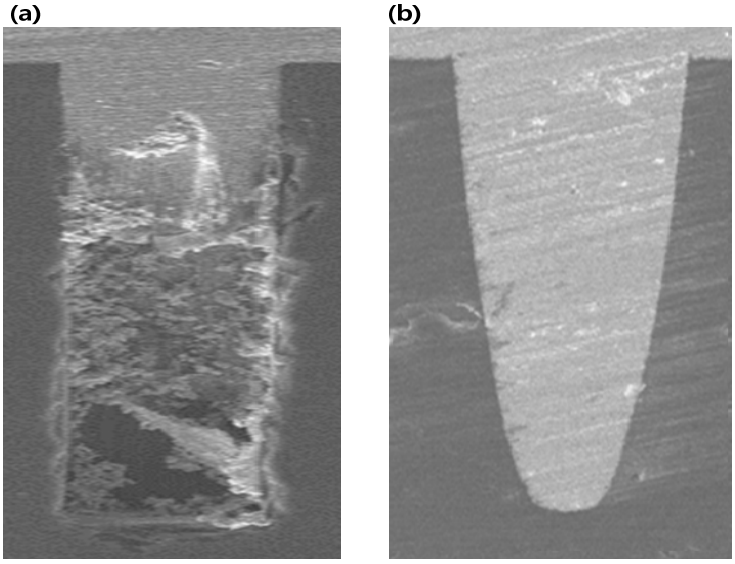


Fig 3.2 SEM cross sectional images of vias etched after standard gold plating

3.2.2 Tapered Source Via Formation

The tapered silicon via etch process consists of two silicon etching steps. The 1st etching step is a high etch-rate silicon etching process is performed deep silicon vias of required depth followed by photoresist stripping by oxygen plasma. The 2nd etching step is designed to control the taper angle of the via through the global isotropic etch. Tapered via etching experiments were carried out on a Plasma Therm Inductively coupled Plasma (ICP) etcher. Inductively Coupled Plasma (ICP) refers to a system configuration where plasma is generated by means of inductively coupling RF power in the source while independently controlling the ion energy bombarding the substrate via the applied bias power. In this tool, the plasma source power and platen supply was generated by a 2500 W 2 MHz, a 600 W 13.56 MHz generator respectively.

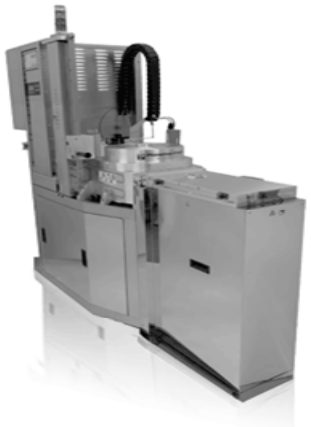


Fig 3.3 Inductively coupled Plasma (ICP) etcher of Plasma-Therm

A diagram illustrating the determination of the sidewall angle θ, local bowing, undercut, and the size of via-hole base is shown in Fig 3.4. A 10 μm thick AZ 4620 photoresist was spin coated and the lithography was performed to define TSV opening. Test square patterns of dimension range from 10 to 100 μm. The target via depth was around 60 μm. To examine the profile of the etched vias, visualization of the via profiles using scanning electron microscopy (SEM) is used.

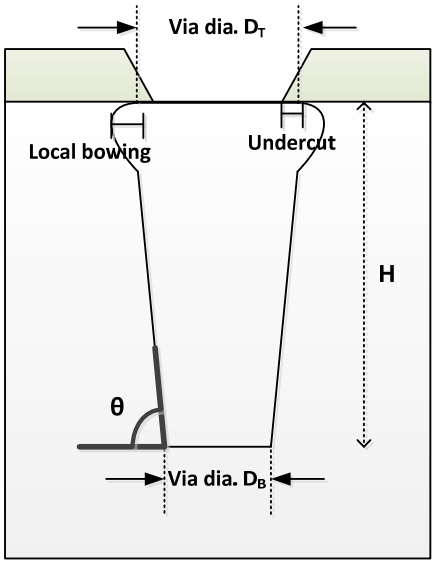


Fig 3.4 Schematic illustrating the via parameter definition

A. Characterization of 1st etch process

The first via etch step is done to 60 ~ 70 % of the via depth. The first etch step defines the size of the bottom of the via. In case of 1st etch performed by non-BOSCH process. The gases used for first etch step is mainly SF_6 and O_2. There is a high tendency towards isotropic etching due to SF_6 and O_2 gas chemistry which generates lot of reactive F-radicals [12]. The vertical via formation can be achieved by adding Ar gas as a reactive precursors which pushed deep into the via results in a more controlled etch profile. To understand the general characteristics of this etch, several experiments were performed. The process parameters in this study are varied using the following range:

- ICP power: 800 ~ 1500 W
- SF_6 flow rate: 65 ~ 100 sccm
- O_2 flow rate: 20 ~ 65 sccm
- Bias voltage: 80 ~ 240 V
- Pressure: 15 ~ 35 mTorr

In the following sections, the effect of percentage of oxygen in the gas mixture, chamber pressure, ICP power, and bias power on etch rate, via profile, sidewall morphology, and selectivity are discussed.

Effect of the percentage of oxygen in the gas mixture

The percentage of oxygen in the SF_6/O_2 gas mixture plays a crucial role in defining via profile. To investigate this effect, the flow of oxygen was varied while keeping other parameters constant. The process parameters were: Ar flow of 65 sccm; pressure of 25 mTorr; power of 1200 W; and bias voltage of 120 V. substrate temperature of -5 °C; etch time of 20 min. The percentage of oxygen in the gas flow mixtures was varied as shown in Fig 3.5. Changing the percentage of oxygen in the gas mixture from 20 % to 50 % reduces the etch rate from 5.8 to 0.9 μm/min. By increasing the amount of oxygen, passivation of via sidewall is increased and tapering can be achieved. However, increasing the percentage of oxygen in the gas mixture leads to some reduction in the etch rate. In case of the percentage of oxygen in the gas flow less than 20 %, nearly straight sidewall was obtained. This results shows that the oxygen reacted with the silicon and SF_5^+ and forms protecting Si_xO_y and $Si_xO_yF_z$ layers on the via sidewalls and on the via bottom [18]. Furthermore, O* radicals will also passivate the silicon surface with the growth of a $Si_xO_yF_z$ film related to reduction in etch rate. The vertical profile of the via is believe that the etching is entirely isotropic as it depends exclusively on the chemical reaction between the F* ions and the exposed silicon with the absence of O_2 in the plasma [19, 20]. As the O_2/SF_6+O_2 gas ratio is increased, the vertical etch rate is first increased because of a higher F atom density and then decreases because of a growing $Si_xO_yF_z$ film and further F atom dilution [13]. Fig 3.6 shows the bottom of 50 mm diameter via etched at varying O_2 flow rate. It is clearly visible from the images that vias etched with lower oxygen ratio were smoother than the vias etched with higher oxygen ratio.

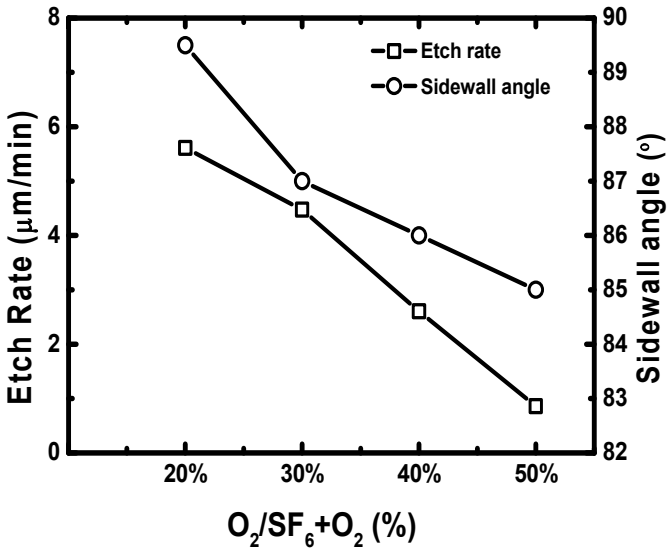


Fig 3.5 Variation of etch rate and via sidewall angle as a function of the amount of oxygen in SF_6/O_2 gas mixture

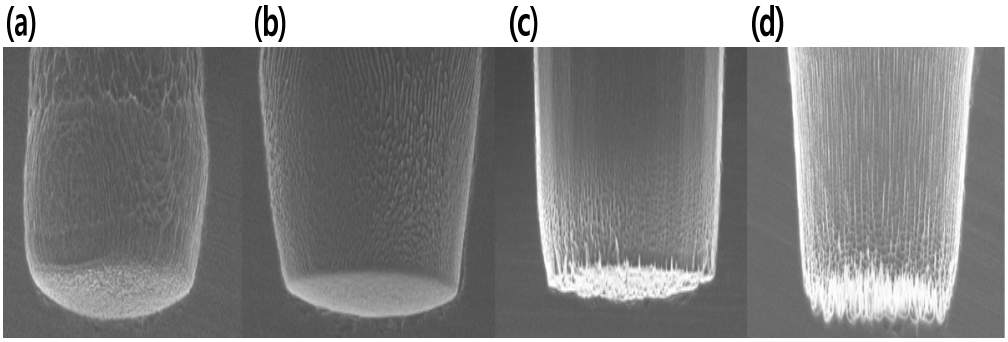


Fig 3.6 Effect of the amount of oxygen in SF_6/O_2 gas mixture on the bottom surface roughness (a) 20 %, (b) 30 %, (c) 40 %, and (d) 50 %

Effect of the ICP power

In my study, Wax was used to attach fabricated device (piece of wafer) to a carrier wafer for the via-hole etching process. It should be noted that materials was not allowed in CVD system. For these reason, photoresist was available masking material for etching process.

In order to raise the selectivity (Si/Photoresist), it was necessary to either raise the Si etching rate, and/or lower the photoresist etching rate. In addition to the ICP power, bias power, the process pressure and gas flow was another parameter that contributed to the etching rates of the Si and etch mask material. When we investigated the relationship between ICP power and selectivity, it became clear that raising the ICP power significantly decreased the etch selectivity. However, the effect of changing ICP power does not have a large impact on sidewall slope. This parameter was investigated by varying values from 800 to 1500 W using a photoresist mask with other parameters are fixed: pressure 25 mTorr; temperature -5°C; bias voltage 120 V; SF_6 flow rate 85 sccm, O_2 flow rate 60 sccm; Ar flow rate 65 sccm and etch time 20 min. Silicon etch rate and mask selectivity as a function of ICP power is shown in Figure 3.7. Mask selectivity as a function of ICP power are 18, 15, 13, and 12 for ICP power of 800, 100, 1200, 1500 W, respectively. For photoresist mask, selectivity is found to decrease with increasing ICP power.

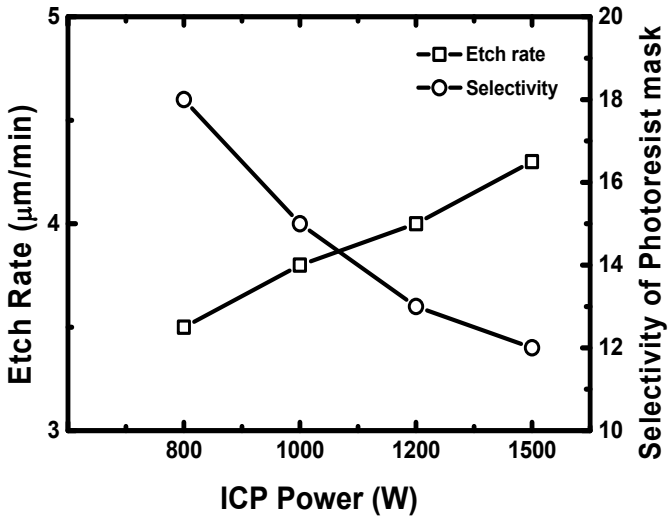


Fig 3.7 Variation of etch rate and selectivity of Photoresist mask as a function of ICP power

We optimized the Si etching process parameters on both sidewall profile and silicon etch rate. The recipe for etching the desired via is shown in Table 3.1. Adjusting the ICP power, bias power, process pressure, and gas flow rate, allowed us to achieve desirable etching features with smooth sidewalls in shown Fig 3.8. To control the taper angle, a two-step etching procedure was proposed.

Table 3.1 Process parameters used to 1st etch tapered vias

Process parameters	Values
Chamber pressure (mTorr)	25
ICP power (W)	1200
DC bias (V)	120
SF_6 flow rate (sccm)	85
O_2 flow rate (sccm)	60
Ar flow rate (sccm)	65
Etch time	20 min

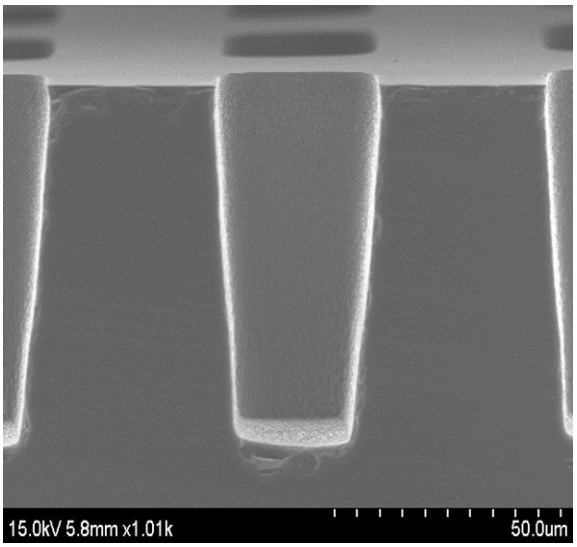


Fig 3.8 SEM image of 70 μm via formation by etch process

B. Characterization of 2nd etch process

The objective of the 2nd etch process is to produce a taper the sidewall profile. At the 2nd etch step, the required via depth and taper angle are achieved. After completing the first etch step, the etch mask is fully stripped and cleaned. The sample is then subjected to a global isotropic etch process. In this etch step, an isotropic etch plasma which is rich in free fluorine radicals. The neutral free radical, which tends to diffuse freely in all directions, causes the etch rates to be more at the top and gradually lesser at the bottom of the deep silicon vias thus giving a tapered via profile [12, 21]. Proper gas ratio and chamber pressures are needed to maintain the required taper angle. It is important to establish a uniform and stable plasma etching process in order to achieve good via to via repeatability within a chip. As shown in Fig. 3.10(a) showing 21 vias in a row, the two-step etch process produces via to via repeatability within a chip. The main advantage of this two-step approach is to provide straight via sidewall and eliminated the top undercut as shown Fig 3.10(b).

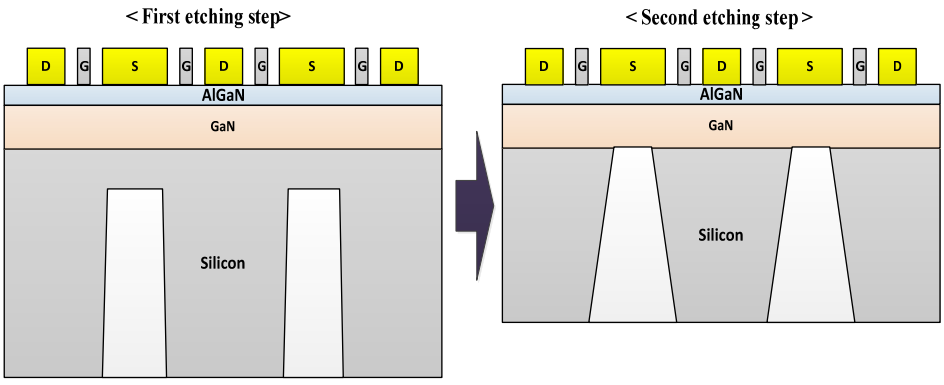


Fig 3.9 Schematic illustration of two-step etch process

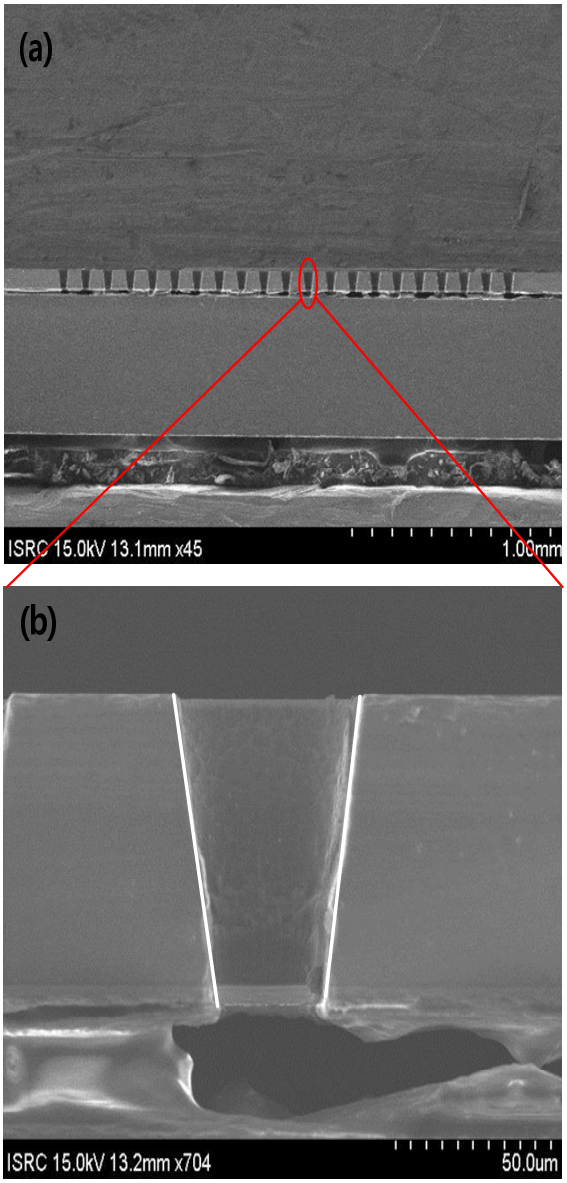


Fig 3.10 SEM image of (a) via to via repeatability (b) via tapered by global isotropic etch process

3.2.3 GaN Etch Process

Tapered via holes were fabricated from the backside of the silicon substrate and stopping on the GaN layer. Then GaN layer was etched away by inductively coupled plasma etching to expose the metal contacts. The wafer already has front-side metallization and therefore the dry etching process of GaN layer must have reasonable selectivity for the silicon over the metal contact as shown Fig 4.6. The difficulty of the dry etching process is that the mask material, typically metal such as Ni is not sufficiently robust to withstand via etch [22, 23]. The etching process must have low damage and selective etching of one material over another. This is critical especially to control accurately stop on the source region for metal contacts. The following will details the etching performance with high selectivity using Cl_2/Ar plasma.

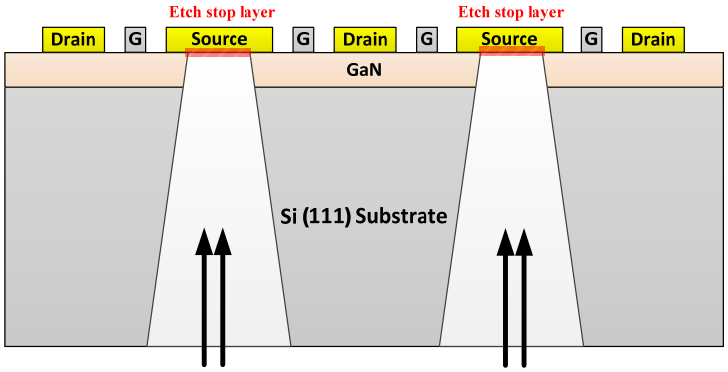


Fig 3.11 Schematic of via holes in silicon substrate

The GaN layer was etched by using inductively coupled plasma from the backside of the silicon. A silicon substrate was used hard mask during the etching process. ICP plasma parameters used in this study were: Cl_2 flow of 12 sccm, Ar flow of 8 sccm, ICP power of 1000 W and a chamber pressure of 5 mTorr. Chlorine plasmas are commonly used because $GaCl_3$ is the most volatile etching product. Due to the strong bond energy of GaN, etching also requires high ion bombardment energy, which can be improved by adding argon to the plasma with a rather high bias voltage [24, 25]. The following are dedicated to the influence of plasma parameters on the etch rate and selectivity with nickel layer. Fig 3.12 presents the etch rates as function of bias power. GaN etch rate reaches 225 nm/min for a bias power of 150 W. When the bias power increases, sputtering induces a higher etch rate with decreasing selectivity. As a consequence, a two-step etching procedure was required to obtain high Ni mask selectivity for deep etching. During the first etching, the 90 % of GaN layer was removed by high power dry etching. Then remainder of it was etched away by low bias power plasma. SEM cross sections for a 1 μm deep GaN via etched using a 2 step optimized process stopping on the metal contact layer are shown in Fig 3.13.

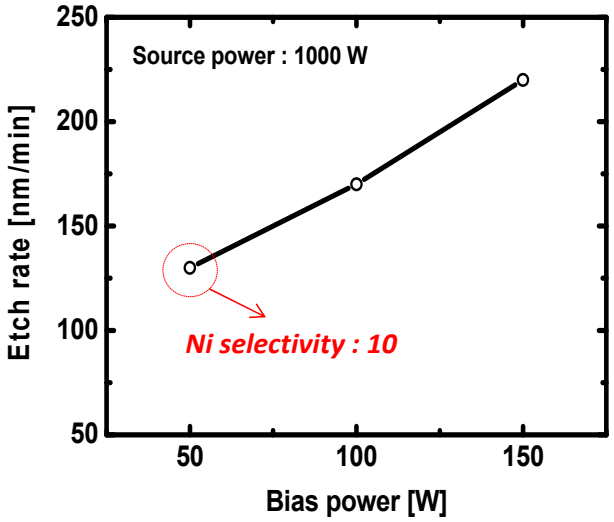


Fig 3.12 Etch rate of GaN and GaN:Ni selectivity as a function of bias power

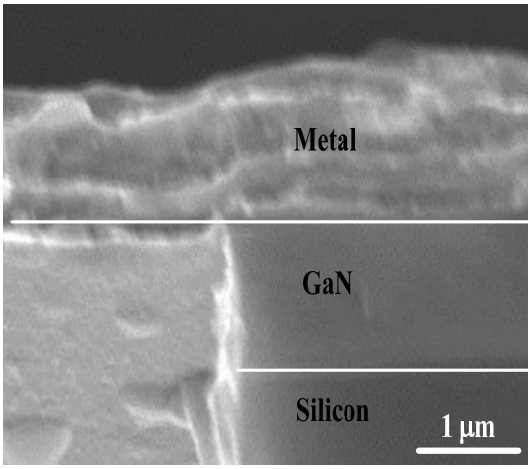


Fig 3.13 SEM images of via etched to the GaN layer

3.2.4 Au Electroplating

Generally, soft gold plating is used in the electronics industry, especially for semiconductor devices [26, 27]. After the etching process is finished, the backside is covered with a thin Ti/Au seed layer which serves to carry the electroplating current. For plating, a gold bath was used which is based in a gold cyanide complex. Contact from source pad to bottom of the substrate can be formed by electroplating 8 μm of gold using a current density of 4 mA/cm^2. The source electrical resistance of the fabricated source via was within the range of 10-13 mΩ. The tapered via etching process has been developed for achieving good sidewall coverage for gold seed metal layer in Fig 3.14. The backside was metalized and electrically connected to the source fingers on the front side.

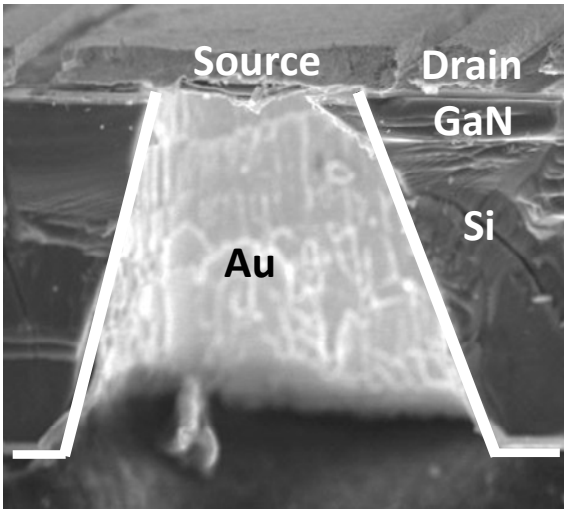


Fig 3.14 SEM images of cross section of via with gold plating

3.3 Back-Side Process Flows

The epitaxial layers grown on silicon (111) substrate consisted of a 20 Å GaN capping layer, a 100 Å $Al_{0.30}GaN$ barrier layer, a 1 μm GaN buffer layer, and AlN/GaN transition layers from top to bottom. A SiN_x pre-passivation layer was deposited at 350 °C using inductively coupled plasma chemical vapor deposition (ICP-CVD) with the intention of protecting the clean GaN surface during ohmic annealing. The ohmic contacts were formed by using a Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm) metal stack, followed by 800 °C for 30 sec in N_2 ambient. Device isolation was carried out by inductively coupled plasma (ICP) etching, utilizing BCl_3/Cl_2 gas. T-shape gate with 0.2 μm gate lengths was obtained by electron beam lithography and Ni/Au metallization. The device with individually grounded source finger vias consisted of a 25 x 25 mm^2 via on each source electrode. After source via etching process, samples were metallized by Ti/Au sputtering and Au electroplating. Figure 3.15 shows backside process flow of GaN HEMT on silicon substrate. The fabrication process can be summarized as follows:

A. The silicon substrate is grounded and polished to 100 μm to reduce thermal resistance.

B. Photo-resist (AZ4330) was coated at 2000 rpm for 40sec and baking 110 °C for 2min to protect front side. After that, samples are mounted onto 4 inch carrier wafer by using Wax.

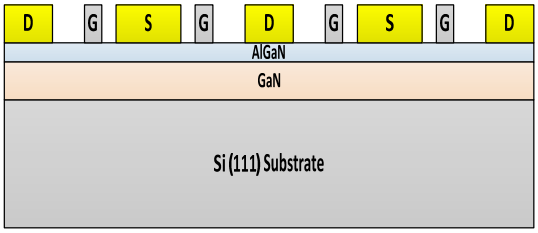
C. Via pattern was formed on the silicon surface with about 25 μm via diameter. A GaN buffer layer was used as stop layer during the silicon etching process.

D. The GaN layer was etched by using inductively coupled plasma from the backside of the silicon. A silicon substrate was used hard mask during the etching process.

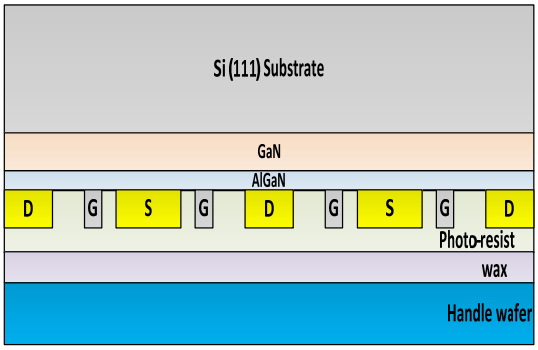
E. Ti/Au seed layer on the backside was deposited by sputtering to form gold metal via and gold was electroplated.

F. We detached a handle wafer from the front side.

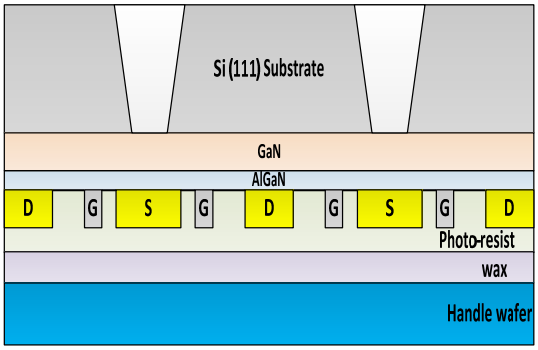
(a) Backside grinding and CMP process



(b) Photo-resist coating and it attached on handle wafer with wax



(c) Deep ICP Si dry etching process



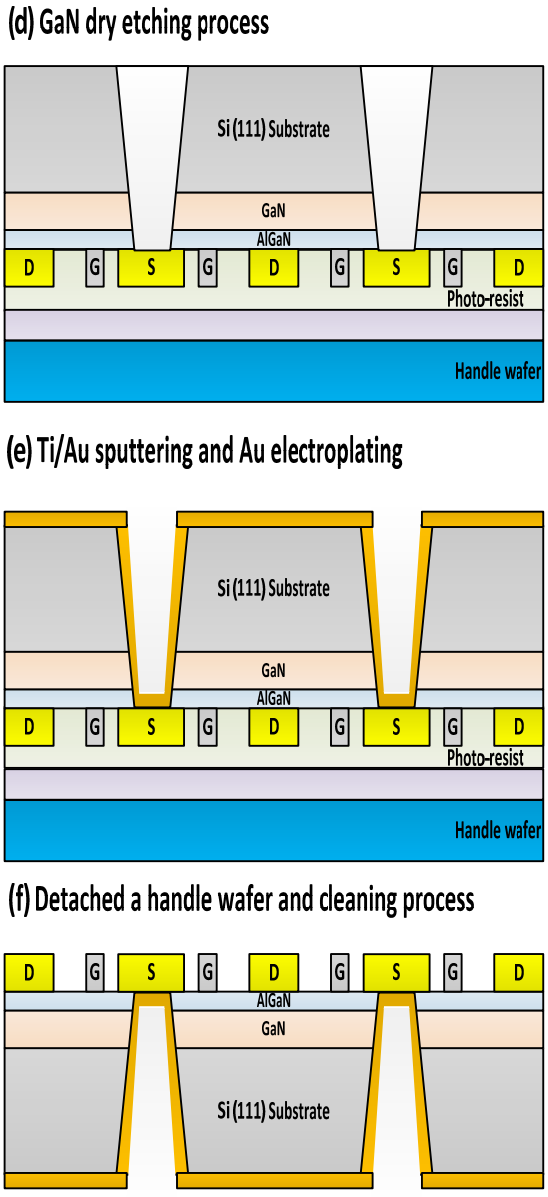


Fig 3.15 Back-side process flow of the AlGaN/GaN HEMT-on-Si (111) wafer

3.3.1 Individual Source Via

In this section the layout concept based on individual source vias (ISV) is introduced and investigated for GaN HEMT devices. Interconnection of various cells by air bridges and their source pads grounded through via holes or wire bonding, gives rise to source inductance is shown Fig 3.16 (a). This has a significant effect in lowering gain. Fig 3.16 (b) is preferred to individual through substrate source via (ISV) configuration because it reduces parasitic source inductance of large gate periphery device and allows use of a larger size cell to realize compact chips. The device performance, in terms of gain, is a function of the source inductance,

$$MAG = \left(\frac{\omega_T}{\omega}\right) \cdot \frac{1}{4g_{ds}\left(R_{in}+\frac{1}{2}\omega_T L_s\right)+4\omega_T C_{gd}(R_{in}+\omega_T L_s)}$$

Fig 3.17 shows the simulated MAG versus frequency for different source inductance settings. Use of individually grounded source vias lowers the source inductance resulting in higher gain. In mm-wave frequencies, this effect becomes even more significant [40-43] . The single-chip amplifier was designed using the ISV configuration for applications in X-band. The single-chip amplifier was designed for applications in X-band.

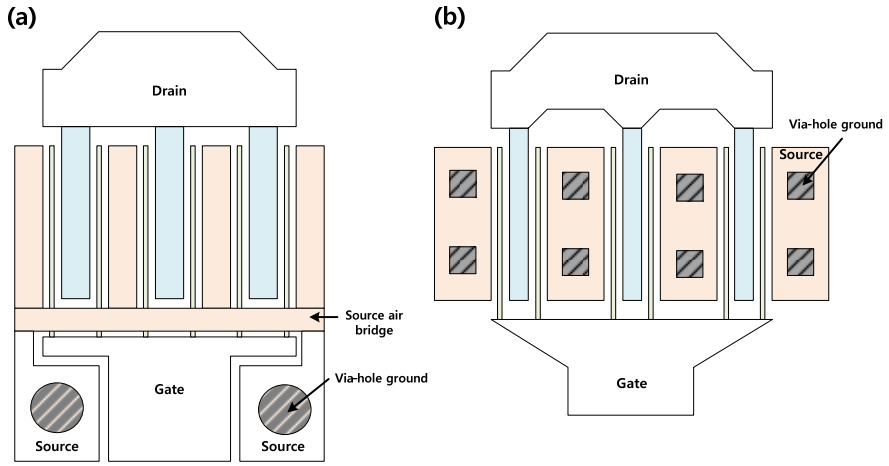


Fig 3.16 Schematic of a unit cell. Source grounding (a) end vias and (b) individual vias

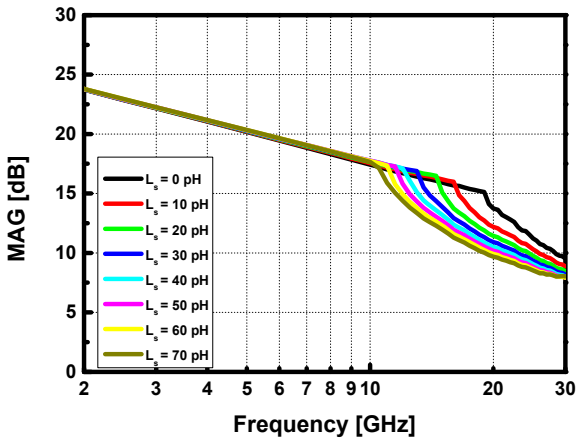


Fig 3.17 Simulated MAG over frequency with additional source inductance

3.3.2 Au-Sn Eutectic Solder Die Attach

High-power semiconductor devices must be mounted using a die-attach material that can handle the temperature generated by the chip to the substrate. Die-attach materials, which connect the die and device to rest of system, play a vital role in ensuring the system performance and reliability [44]. For die-attach material, a careful selection of materials to minimize mismatch in coefficients of thermal expansion (CTE) is critical, due to the significant temperature range of operation and the stiffness of die attach materials that are capable of withstanding such temperatures [45]. Among the high temperature application die attach materials which have been studied thus far include gold-tin (Au-Sn), gold-germanium (Au-Ge), gold-silicon (Au-Si), silver glass, silver-indium (AgIn), high lead (Pb) solutions, and nanoscale silver (Ag) [46]. For GaN-on-Si HEMTs, eutectic AuSn has been widely adopted as the die-attachment technique. Generally 80 wt. % Au, 20 wt. % Sn solder is widely used in the market because of its advantages, such as high reliability die attach, high strength, high corrosion resistance, no thermal fatigue, and allows soldering in fluxless processes [47-49]. This technique was optimized and adapted for HEMTs on AlGa/GaN. The detailed process technology is described in appendix. The fabricated device was mounted on a Cu metal block with Au-Sn eutectic die-attach for heat sinking.

3.3.3 Thermal Resistance Measurement

The HEMT performance deterioration could be observed at elevated temperature. Elevated operating temperatures can lead to increased degradation and failure rates, and a reduction in performance such as output power. An accurate method of measuring device temperatures is essential for optimizing thermal management [50]. To take into account thermal effects and to estimate channel temperature in high power AlGaN/GaN HEMTs several measurement methods have been investigated in literature [51]. They are optical temperature-measurement techniques such as infrared thermal imaging and micro Raman spectroscopy and electrical measurement such as DC/Pulsed characteristics are often used but they have several limitations [52]. The channel temperature of a HEMT was evaluated from temperature dependent transfer characteristics. In order to confirm the effect of the die attachment method, we have measured die attached devices.

Method for estimation of channel temperature as followed [51]

A. Pulsed I-V characteristics(V_{GS} = 0 V) from zero power quiescent point (V_{DS}=V_{GS}=0) at different base-plate temperature (25 °C ~ 120 °C)
B. Extracted pulsed I_{Dmax} and R_{on} a function of base-plate temperature T_a
C. Pulsed I-V characteristics(V_{GS}=0V) from various quiescent point (V_{GS} = 0 V, V_{DS}= 1-10 V) with nonzero power dissipation (P_D = 1.2 – 7 W/mm)
D. Extracted pulsed I_{Dmax} and R_{on} from different bias points with different power

It should mention that these parameters are pulsed values that are different from dc values. The device used in this measurement that gate periphery was 3.6 mm with a unit gate width of 200 μm. Pulse duration and the period were 200 ns and 1 ms, respectively. The devices is placed on the prober chuck of which the temperature is set to 25 °C to 120 °C. We define I_{Dmax} as I_D at V_{DS} = 5 V and V_{GS} = 1.5 V and R_{ON} as the drain-to-source resistance in the linear region at V_{GS} = 1.5 V. Fig 3.18 (a) shows pulsed I-V characteristics (V_{GS} = 0 V) from zero power quiescent point (V_{DS} = V_G = 0 V) at different base-plate temperature (25°C ~ 120 °C). Fig 3.18 (b) shows very clearly I_{Dmax} decreases and R_{ON} increases as the temperature increases. Fig 3.19 (a) shows Pulsed I-V characteristics (V_{GS} = 0 V) from various quiescent point (V_{GS} = 0 V, V_{DS} = 2-10 V) with nonzero power dissipation (P_D = 1.2 – 8.1 W/mm). Fig 3.19 (b) shows Extracted pulsed I_{Dmax} and R_{on} from different bias points with different power dissipation.

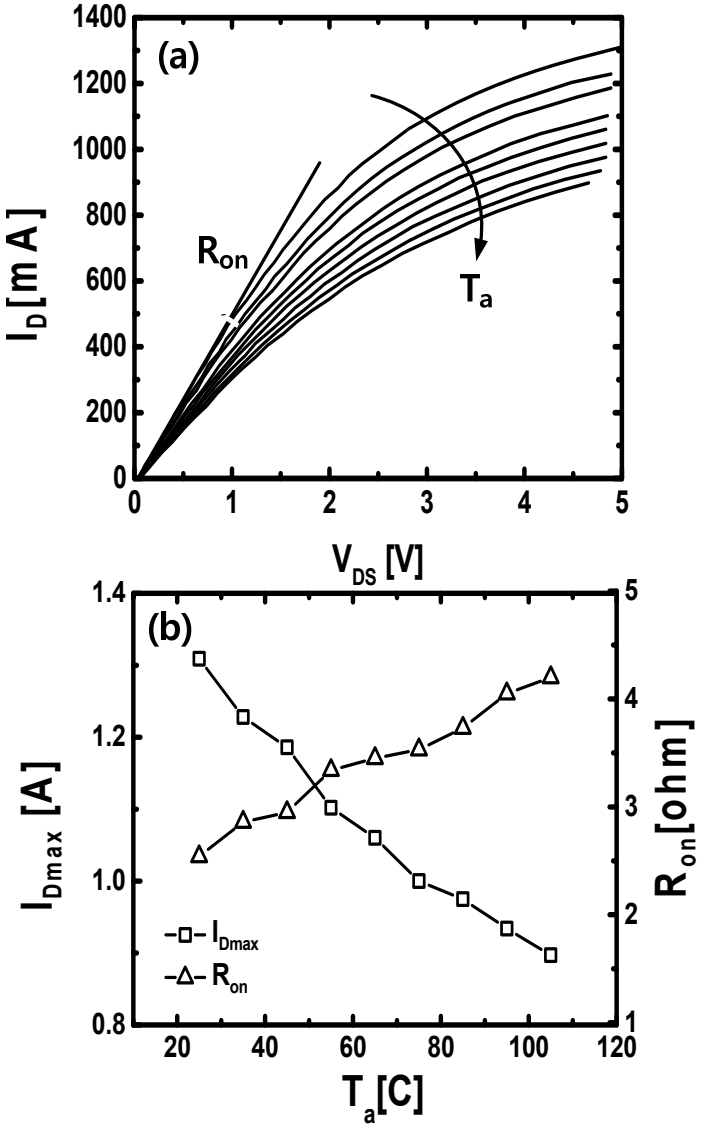


Fig 3.18 (a)Pulsed I-V characteristics (V_{GS}=0V) from zero power quiescent point (V_{DS}=V_{GS}=0) at different base-plate temperature (25°C ~ 120 °C), (b) Extracted pulsed I_{Dmax} and R_{on} as function of base-plate temperature (25°C ~ 120 °C)

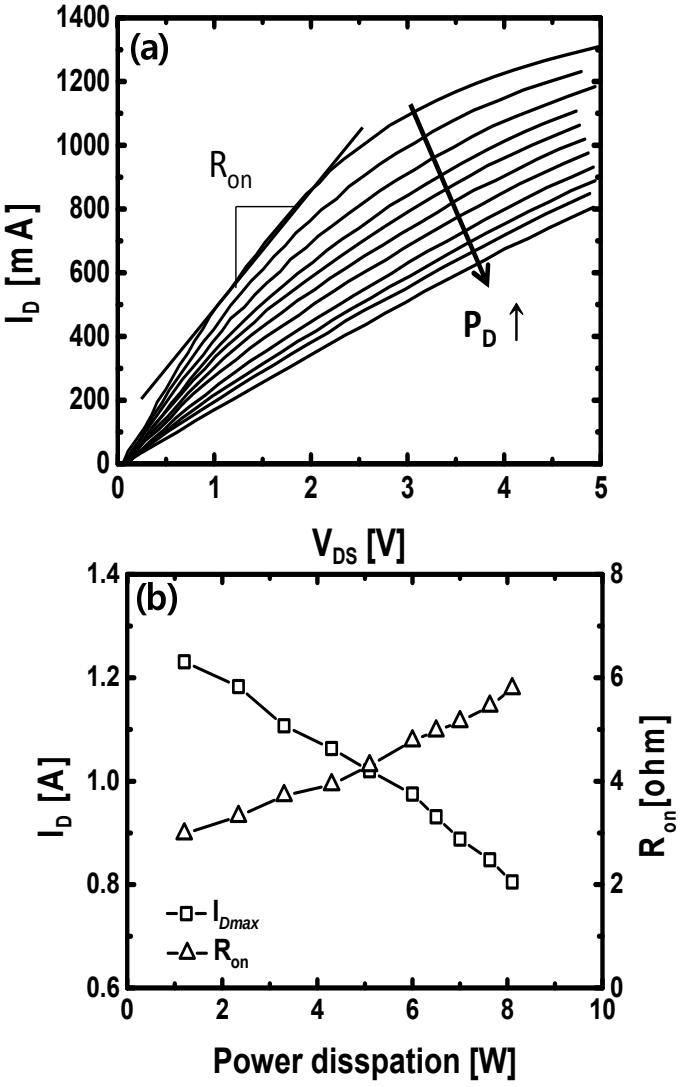


Fig 3.19 (a) Pulsed I-V characteristics (V_{GS} = 0 V) from various quiescent point (V_{GS} = 0 V, V_{DS} = 2-10 V) with nonzero power dissipation (P_D = 1.2 – 8.1 W/mm), (b) Extracted pulsed I_{Dmax} and R_{on} from different bias points with different power dissipation

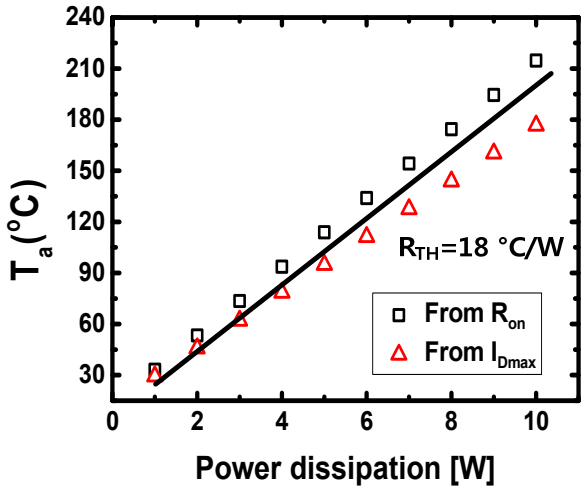


Fig 3.20 Estimated channel temperature from data in Figs. 4.26 and 4.27 as a function of power dissipation. (□) data obtained through I_{Dmax} measurement. (Δ) data obtained through R_{ON} measurement

From the slope of the measurements obtained in Fig 3.18 and 3.19, the thermal resistance has been extracted giving a value is 18 °C/W. This allows selections of the right die attach material for the targeted applications. However, it should point out that various methods for estimating thermal resistance can be make different results from reality.

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Chapter 4

AlGaN/GaN HEMTs for RF applications

4.1 Introduction

GaN-based high electron mobility transistors (HEMTs) have great potential in high power microwave application due to their superior material properties, such as high breakdown field, high electron mobility and high carrier density. This is of particular interest also for power amplifiers in X-band for satellite transmitters or radar applications. Semi-insulating SiC substrate is the most successfully used for demonstration of high-power GaN-based HEMT because of its very high thermal conductivity compared to Silicon. GaN HEMTs on Si substrate become an alternative approach because of its low cost and mass production capability [1]. So far, RF performance of 5.1 W/mm at 10 GHz, and 7 W/mm at 10 GHz are already reported in GaN-on-Si devices [2, 3]. However, many impressive power densities have been reported from small-periphery GaN-on-Si HEMTs. In general, the large-periphery power density at X band is still low, which is greatly limited by the current collapse and heating effect. This chapter will give a device fabrication process for high

frequency applications. To begin with, device layout and conventional fabrication process which we used in this work are outlined. Key process technologies that limit GaN transistor performance are also discussed.

4.2 Advantages of AlGaN/GaN HEMTs for RF Power Devices

Advantages of the High Electron Mobility Transistors (HEMTs) fabricated in the AlGaN/GaN material system for high frequency, high power applications are a large critical breakdown electric field ($\sim 3 \times 10^6\ V/cm$), a sheet charge density in excess of $1 \times 10^{13}\ cm^{-2}$, and saturation velocity of $1.5 \times 10^7\ cm/s$. The high breakdown fields due to the wide bandgaps of GaN and AlGaN enable the use of higher drain biases than can typically be used in the GaAs/AlGaAs system. The operation at high voltage due to its high breakdown electric field not only reduces the need for voltage conversion, but also provides the potential to obtain high efficiency, which is a critical parameter for amplifiers. A large conduction band offset at the AlGaN/GaN hetero-interface and strain-induced charge result in very high sheet carrier densities which are also higher than is achievable in practical III–As HEMT's [4-6]. The high electron mobility and carrier concentration results in a high current density and a low channel resistance are desirable for high RF current. These unique combinations of material characteristics make very attractive candidate for fabrication

of high-power and high-frequency electronic devices. Figure 4.1 offers the theoretical maximum power limit of Si, GaAs, and GaN versus frequency. It is apparent that the output power and frequency range of GaN devices is significantly higher than silicon, GaAs devices.

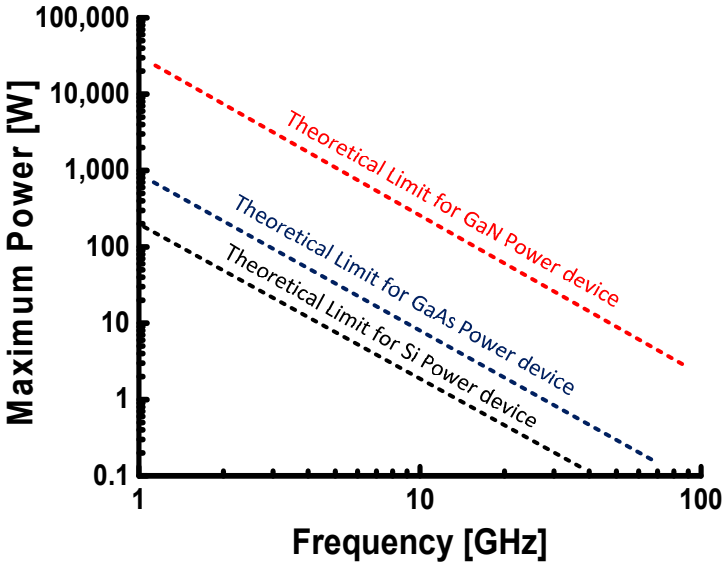


Fig 4.1 The theoretical maximum power limit of Si, GaAs, and GaN versus frequency

The power performance of a solid-state device can be predicted by the Johnson's Figure of Merit $\text{JFOM} = (E_c v_s/2\pi)^2$ and the Baliga's Figure of Merit $\text{BHFFFOM} = \varepsilon_r \varepsilon_0 \mu E_G^3$, where E_c is the critical breakdown field, v_s is the saturation velocity, μ is mobility, E_G is the BG energy of the semiconductor, ε_0 is the permittivity of free space and ε_r is the relative permittivity of the semiconductor [7, 8]. Figure 2.3 shows the Johnson's Figure of Merit and Baliga's Figure of Merit calculated to compare the power-frequency limits of Si, SiC, and GaN [9].

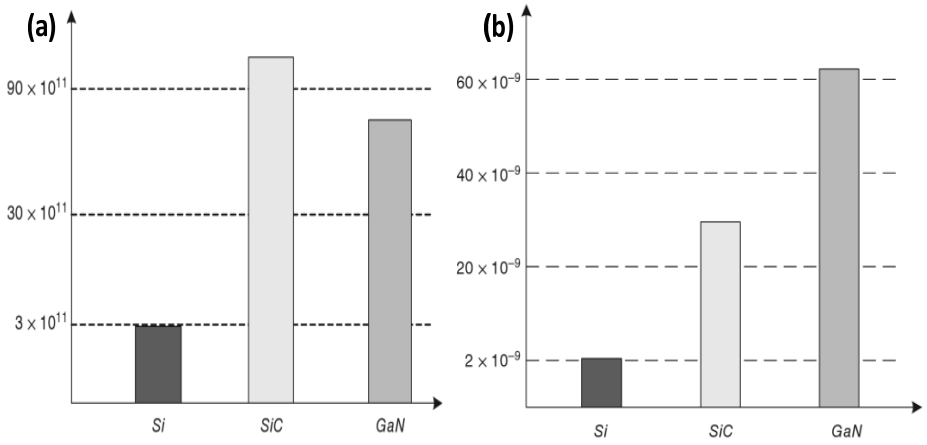


Fig 4.2 Comparison of (a) Johnson's figure-of-merit (JFOM), (b) Baliga's figure-of-merit (BFOM) for Si, SiC, and GaN [9].

4.3 RF Performance Limitations

The potential of AlGaN/GaN HEMT's for microwave power has been demonstrated power data of 1.1 W/mm at 2 GHz in 1996 at first [10]. Extensive research has been studied; a tremendous improvement has been in device performance achieved over last two decades. The main obstacle is a discrepancy between the measurement power and predicted output power. The reduction in output power from its expected value is caused by a decrease of maximum drain current and an increase of knee voltage. It is believed to be a trap-related phenomenon called RF dispersion where surface or bulk traps contribute.

4.3.1 Surface State

It is well known that spontaneous and piezoelectric polarization effects lead to charge sheets of opposite polarity at the top and bottom surfaces of the AlGaN layer in an AlGaN/GaN heterostructure [11]. Ibbetson [12] showed that the existence of such a polarization dipole alone is not sufficient for a 2DEG to form in the GaN channel. A positive sheet charge can arise from ionized donor states at the surface as was shown in [5, 12, 13]. As the thickness of the AlGaN layer increase, the donor energy reaches the Fermi level. Electrons are then able to transfer from occupied surface states to empty conduction band states at the interface, creating the 2DEG and leaving behind positive surface charge in Figure 4.3. Until all the surface states are

empty, the Fermi level then remains essentially at the donor energy but more and more electrons transfer with increasing barrier thickness. The 2DEG exists as long as the AlGaN barrier is thick enough to allow the valence band to reach the Fermi level at the surface. Electrons can then transfer from the AlGaN valence band to the GaN conduction band, leaving behind a surface hole gas [12]. It is obvious that the donor-like surface states are a source of 2DEG in AlGaN/GaN interface.

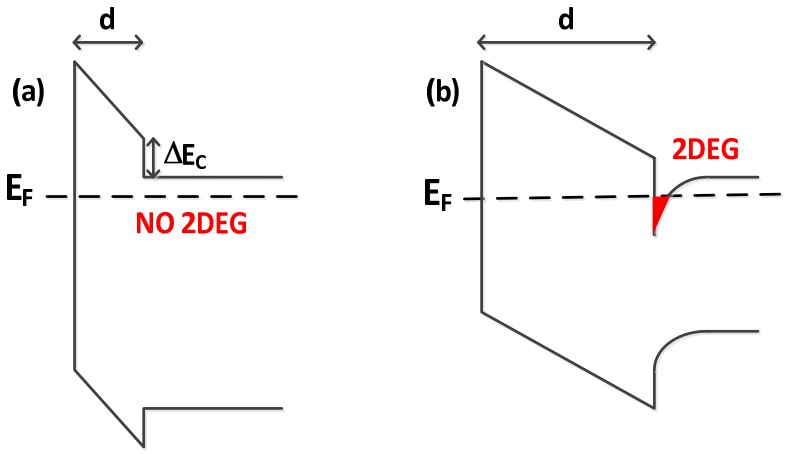


Fig 4.3 Schematic band diagram illustrating the surface donor model with the undoped AlGaN barrier thickness (a) less than, and (b) greater than the critical thickness for the formation of the 2DEG. The barrier thickness, d [12].

4.3.2 Current Collapse Phenomenon

A defect-related phenomenon of particular concern is generally referred as "frequency dispersion", "current collapse", "gate/drain lag" or "current slump" as these effect reduces the output power achievable by the device. Fig 4.4 shows the schematic comparison DC I-V characteristics and pulsed I-V characteristics. It is observed that reduced output power from its expected value is caused by a decrease of maximum drain current and an increase of knee voltage. Current collapse occurs when high drain-source voltage is applied to the gate edge on the drain side which can inject electrons into surface states between gate and drain. Consequently, the electrons from the channel are trapped. When the device is turned-on, those trapped electrons interrupt current pass through the channel resulting in higher on-resistance and low saturated drain-source current in Fig 4.5.

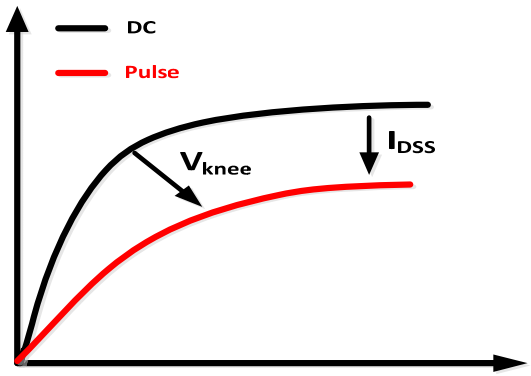


Fig 4.4 Schematic comparison of DC I-V characteristics and dynamic I-V characteristics

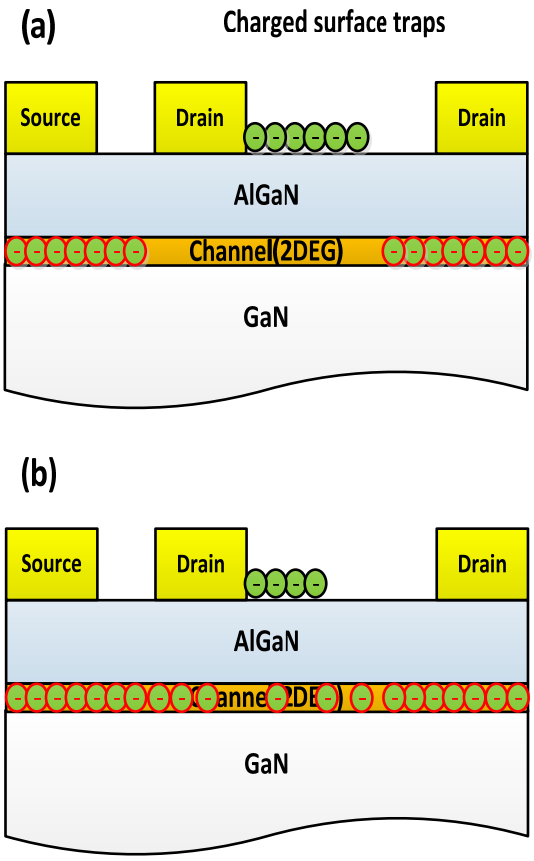


Fig 4.5 Traps phenomenon in a device when it is (a) turned-off (b) and turned-on

The carriers in the two-dimensional electron gas can be lost either to the surface states on the cap layer or trapping centers in the resistive buffer underlying the active channel [14]. The first, and most intensively studied, is due to surface effects associated with localized and reversible charge trapping in defects located near the corner of the gate, resulting in a "virtual gate" which reduces the current handling of the channel and leads to "knee walkout" [15-17]. If there exists negative charge on the surface, the surface potential is made negative, depleting the channel of electrons and leading to extension of the gate depletion region. Hence, the effect of surface negative charge is to act like a negatively biased metal gate as shown in Fig. 4.6 [5]. The potential on the metal gate is controlled by the applied gate bias while the potential on the second gate, V_{VG}, is controlled by the total amount of trapped charge in the gate drain access region. This second gate is referred to as the virtual gate. The output drain current is now controlled by the mechanism that supplies charge to, and removes charge from the virtual gate, in addition to the applied gate bias [5].

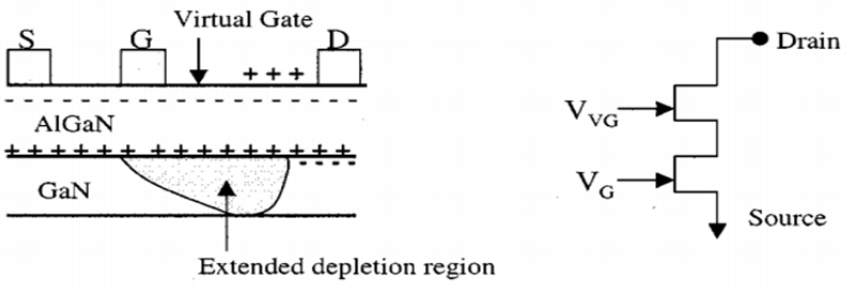


Fig 4.6 Model of the device showing the location of the virtual gate and schematic representation of the device including the virtual gate [5]

To control these surface issues effectively, systematic investigation of the properties of defect-related surface states has been performed. Even though some improvements were achieved by various approaches such as surface passivation, surface preparation, and plasma treatment, still it remains controversial. The surface passivation with SiN_x dielectric layer has been widely adopted as an effective passivation material to suppress the trapping effects due to Si to incorporate as a shallow donor at the AlGaN surface in sufficiently large quantities to replace the surface donor [18]. On the other hand, oxide-based high-k dielectrics such as Al_2O_3[19, 20], Gd_2O_3[14], and HfO_2 [21] have been deployed as the passivation layer. Also, it is important to control the condition of the surface before deposition of the passivation layer. Some recent work shows that pre-passivation plasma treatment such as N_2 [22], NH_3[23], and H_2 is effective ways in suppressing surface-related dispersion effects. An increasing number of papers had been proposed with various methods to reduce the surface-related effect. However, the different HEMT material and processing-related aspects is still lacking. The second mechanism is charge trapping in deep levels within the semi-insulating buffer Buffer-related current collapse due to hot-carrier injection into the buffer followed by trapping in deep levels [24]. The GaN buffer was originally rendered insulating using intrinsic growth defects, and this approach has continued to deliver outstanding device performance [25]. In this case, charge trapping in compensated intrinsic deep donors and acceptors can result in current collapse which varies with geometry, buffer doping, and trap energy level [26-28].

4.4 Device Fabrication

Device fabrication was carried out in the Inter-University Research Center, Seoul National University. The following will outline the process to take surface preparation through to the complete working device stage in shown Fig 4.8. The details were as follow:

A. Surface cleaning for device fabrication

The samples are initially immersed in a glass beaker of acetone and placed into an ultra-sonic bath for 30 minutes. The acetone is then removed by placing the sample into methanol and isopropyl alcohol for 15 minutes in order. The surface cleaned with a mixture H_2SO_4/H_2O_2 (SPM cleaning) after solvent cleaning. After that samples are dips for 10 minutes in 10:1 diluted HF followed by rinse deionized water and dried with nitrogen. This procedure ensures that any contaminants are removed.

B. SiN_x surface passivation

The SiN_x passivation is generally used as the surface passivation film for high frequency applications. A 120 nm SiN_x pre-passivation layer was deposited at 350 °C using inductive coupled plasma chemical vapor deposition (ICP-CVD) with the intention of protecting the clean GaN surface during ohmic annealing [29]. The film was deposited using a SiH_4-N_2-Ar gas mixture and its deposition rate was 5 nm/min.

C. Ohmic formation

After the ohmic contact areas were patterned, the SiN_x layer was etched away prior to metallization. A low-damage, SF_6 based dry etching process was developed using an RIE system with the RF power of 10 W and the pressure of 100 mT. The etch rate was 100 Å/sec. The ohmic metal scheme used for samples was Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm). Then a rapid thermal annealing process was performed at 780 ^{o}C for 30 sec. The contacts resistance (R_c) of fabricated TLM pattern was 0.4 Ω·mm. Fig 3.2 shows a representative high resolution TEM micrograph of the metal/GaN interfacial layer which evident of TiN layer.

D. E-beam marker

The Ti/Pt alignment marker definition is carried out using E-beam lithography which can withstand annealing to beyond 800 ^{o}C. It is still necessary smooth surface morphology and edge acuity in e-beam lithography process.

E. Mesa isolation

The MESA isolation was carried out using low-damage Cl_2/BCl_3-based inductively coupled plasma reactive ion etching with a source RF power of 350 W, a bias RF power of 10 W, and a chamber pressure of 5 mTorr. The GaN etch rate was 5 Å/sec.

F. Gate metallization

A Ni/Au Schottky gates have been defined by e-beam lithography.

G. 2nd passivation & Source field plate

The source field plate is the most common types used in RF applications resulted in increasing the gate and drain breakdown voltage and reducing the gate-to-drain capacitance. After gate metallization, samples were passivated with 200 nm layer of ICP-CDN SiN_x at 190 ^oC. The contact windows were opened by fluorine based dry etching. The field-plate connected to the source terminal was defined. Ni/Au-based field plate metallization was performed and extended by 1 μm out over the gate to the gate-to-drain region as illustrated in Fig 4.7.

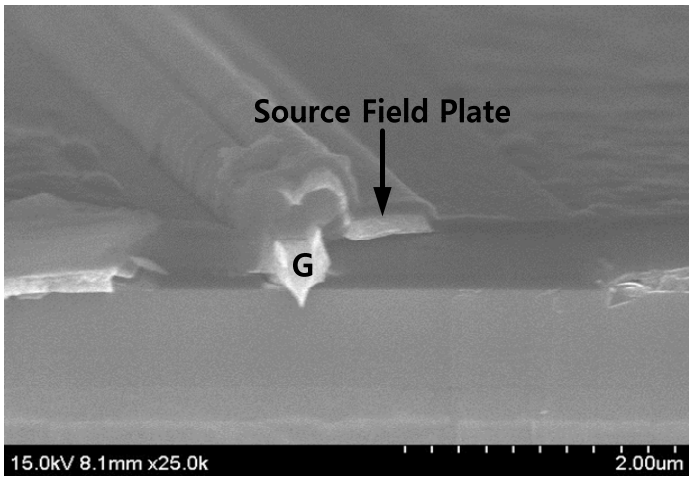
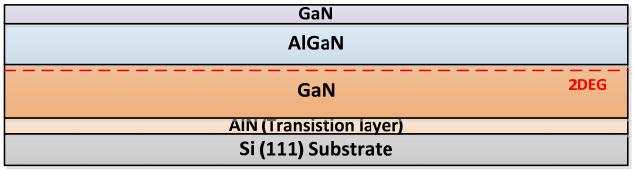


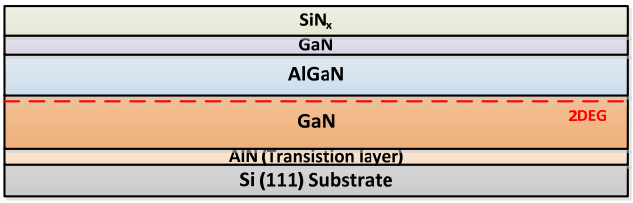
Fig 4.7 Cross sectional SEM micrographs of source field plate structure

I. Au-plated air-bridge process

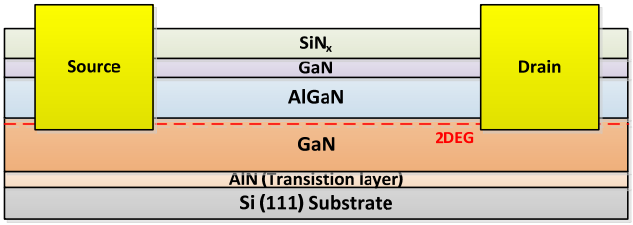
A standard Au-plated air bridge process was used to complete multi-fingered FETs.



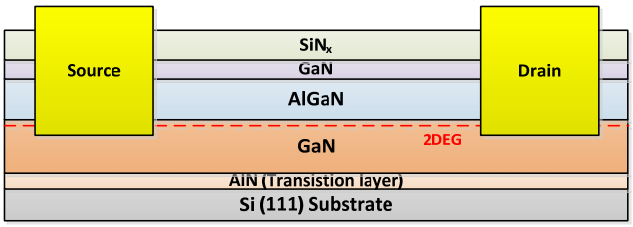
(a) Surface cleaning for device fabrication



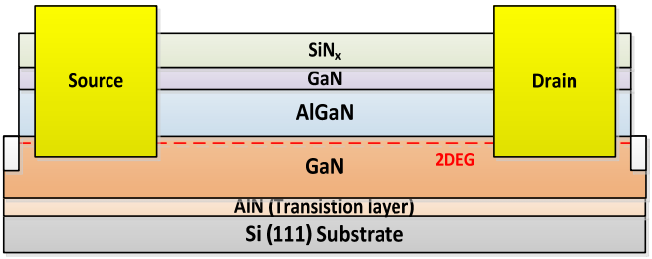
(b) SiN_x passivation



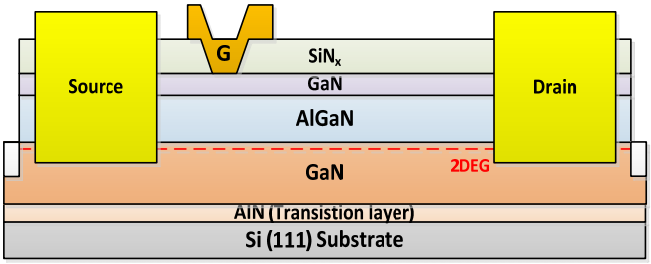
(c) Ohmic formation



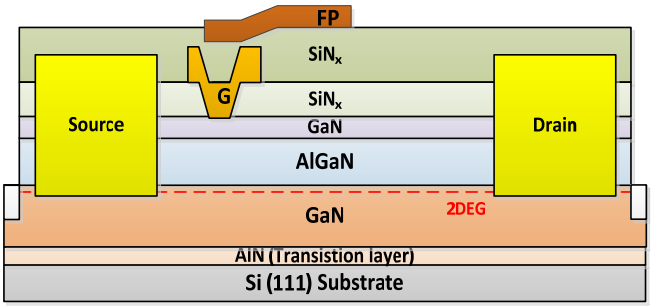
(d) E-beam lithography (for marker)



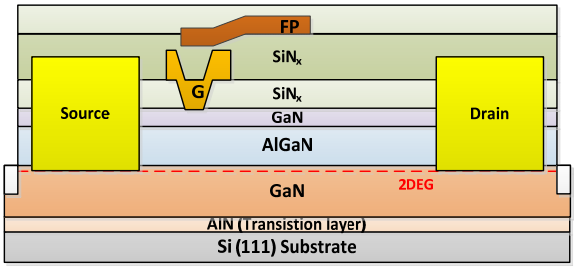
(e) Mesa isolation



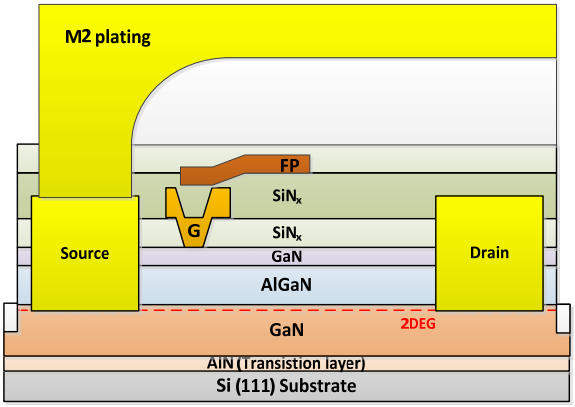
(f) Gate Metallization



(g) 2nd passivation and source field plate



(h) 3rd passivation



(i) Air-bridge & M2 plating

Fig 4.8: Device process (a) Surface cleaning for device fabrication, (b) SiN_x passivation, (c) Ohmic formation, (d) E-beam lithography for marker, (e) Mesa isolation, (f) Gate metallization, (g) 2nd passivation and source field plate, (h) 3rd passivation for multi-finger connection, and (i) Air-bridge and gold plating

4.4.1 Device Layout

All device data presented in this chapter consists of GaN HEMTs grown silicon substrate. The device layouts investigated are from 0.2-mm gate periphery to 3.6 mm gate periphery transistors. The device has a 0.25 μm gate length with a source–gate spacing of 1 μm and a gate–drain spacing of 2.5 μm. The 3.6 mm gate periphery device includes 18 fingers, each having a 200 μm gate-width. The multiple fingers are connected using a plated air-bridge process consisting of 3 μm thick gold. A photograph of the 0.2 mm GaN transistor layout is shown in Fig 4.9.

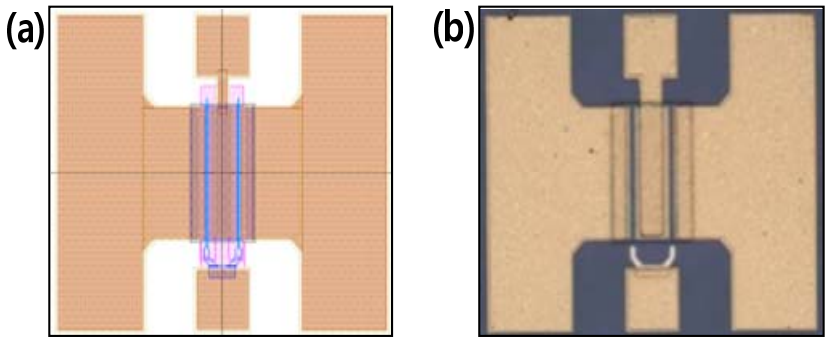


Fig.4.9 (a) Layout of the 0.2 mm GaN HEMT, (b) optical image of the device

4.4.2 Slant Gate Process

Various techniques have been developed to improve the RF performance of the GaN HEMTs. One of key technologies is maximized the breakdown voltage by engineering the electric field near the gate on the drain side. To solve the problem, field plates were developed and widely used, with the tradeoff of increased parasitic capacitance [30, 31]. Without significantly increasing the parasitic capacitance, the shaping of the dielectric during the recess process to create a slant field plate has the advantage of defining a gate with an integrated field plate optimized for high-voltage applications with a single lithography step [31]. The epitaxial layers grown on silicon (111) substrate consisted of a 20 Å GaN capping layer, a 100 Å $Al_{0.30}GaN$ barrier layer, a 1 μm GaN buffer layer, and AlN/GaN transition layers from top to bottom. For the device fabrication, 120 nm-thick SiN_x layer was deposited by inductively coupled plasma chemical vapor deposition (ICPCVD) for device passivation. Device isolation was carried out by inductively coupled plasma (ICP) etching, utilizing BCl_3/Cl_2 gas. The ohmic contacts were formed by using a Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm) metal stack, followed by 800 °C for 30 sec in N_2 ambient. The gate was patterned by E-beam lithography. The device under investigation has a gate width of 2 x 100 μm and a lithography gate length of 0.3 μm. The actual gate footprint length was 0.25 μm. The gate-to-source spacing is 0.5 μm, and the gate-to-drain spacing is 2.5 μm. A field plate structure in conjunction with a sloped gate profile was fabricated in this work using a sequence of plasma etching steps to

effectively suppress the high electric field at the gate corner. SiN_x film was etched away by using a SF_6 reactive ion etch (RIE). The gas flow rate was 100 sccm for SF_6 only. The plasma bias was 10 V and the chamber pressure was 100 mTorr. Increasing chamber pressure enables curved sloping walls are formed. The etch rate of the SiNx below overhang is lower than the etch rate of the SiN_x exposed to the direct flux. The shape of trench wall could be controlled by varying the pressure in the RIE and the over-etch time. Scanning electron microscopy (SEM) images of the SiN_x sidewall prior to gate deposition is shown Fig 4.10. Finally, gate metal stack of Ni/Au (40/360 nm) was evaporated in Fig 4.11.

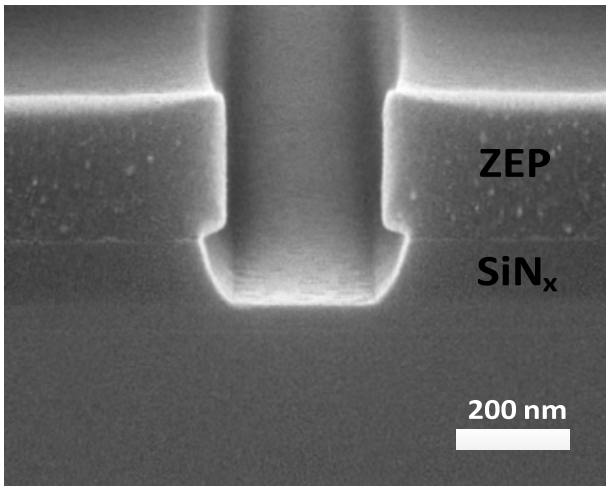


Fig 4.10 Cross section SEM images of the SiN_x sidewall prior to gate deposition

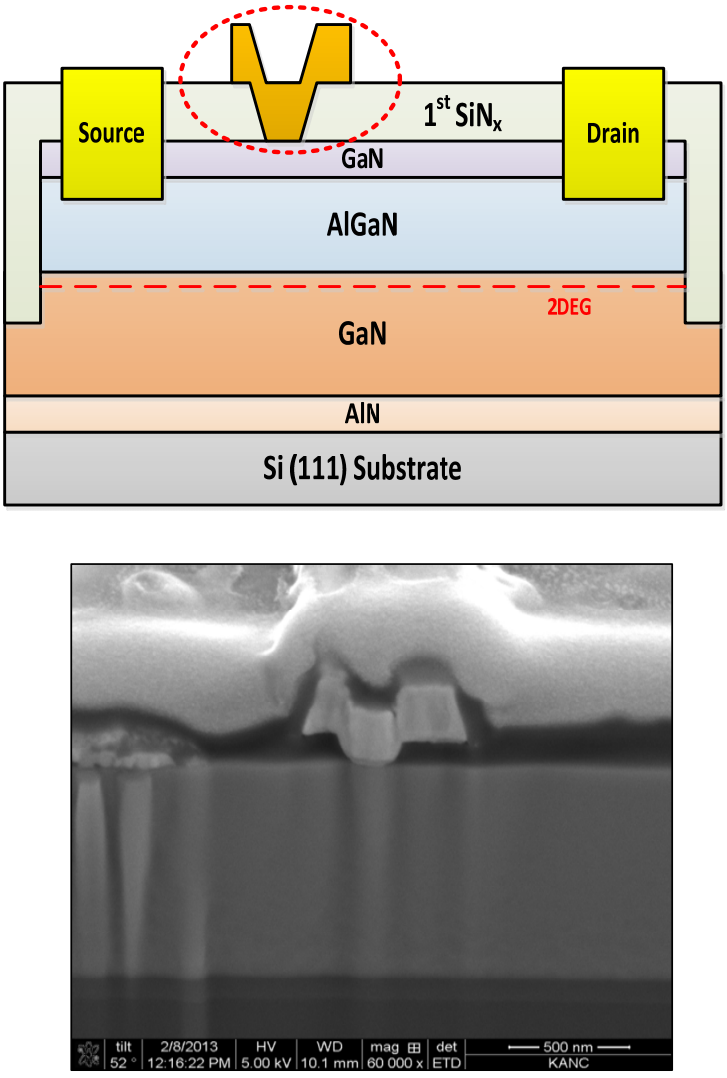


Fig 4.11 Schematic and Cross section SEM images of 0.25 μm gate AlGaN/GaN HEMTs

4.4.2 Fluorine Plasma Treatment Process

To achieve high performance in GaN microwave applications, current collapse must be minimized since it degrades DC and RF performance. A suitable surface treatment and surface passivation process can solve the problem. The surface properties can be affecting by high temperature or plasma damage during the fabrication process. Various plasma treatments are widely used in AlGaN/GaN HEMT processing to effectively enhanced high-frequency performance [23, 32, 33]. The fluorine plasma treatment can provide negative fixed charges which can effectively raise the energy band in the sample surface, suppressing the trapping and de-trapping process [34, 35]. Although a number of previous studies have been made on F^- plasma treatments, no detail studies have been reported on the effect of F^- plasma treatment prior to surface passivation. In this section, we reported the beneficial effects of using SF_6 plasma among the various surface treatments to mitigate current collapse. We focus to identify how critical are exposure time used during the SF_6 plasma discharge affect the GaN-based surface, in relation to electrical characterization of HEMT devices and the electrical properties of the 2DEG by Hall measurements. The device fabrication started with a 100-nm-thick SiN_x pre-passivation layer deposition which deposited at 350 °C using inductively coupled plasma chemical vapor deposition (ICP-CVD). The sample was annealed in nitrogen at 820 °C for 30 sec to form the ohmic contact. Device isolation was carried out by inductively coupled plasma (ICP) etching, utilizing BCl_3/Cl_2 gas. The SiN_x which was deposited for the protection of the active

area from high temperature annealing was removed by SF_6 plasma in an RIE system. The additional SF_6 plasma treatment step was performed before SiN_x passivation. In order to treat the sensitive GaN surface, the dielectric over-etch exposure of the GaN surface to a SF_6 discharge were performed. The processes are made of two steps that are the main etch step and the over etch step. After high temperature annealing process, each device was exposed to SF_6 plasma at room temperature followed by the SiN_x deposition. The SF_6 plasma power was fixed 10 W where minimum stable plasma is obtained. The SF_6 plasma discharge duration was increased from 0 to 10 min. The samples were exposed to fluoride plasma under different treatment time shown in Table 4.1. The data in Table 4.1 show that a brief SF_6-plasma treatment process has negligible influence on the 2DEG density and mobility.

Table 4.1 Dependence of hall measurement results on SF_6 plasma treatment time

F^- treatment time (min)	R_{sh} (Ω/sq)	n_{2DEG} (cm^{-2})	(Cm^2/Vs)	R_{on} (Ω·mm)
0	471	1.01×10^{13}	1310	5
2	449	1.11×10^{13}	1290	4.8
5	435	0.95×10^{13}	1380	5.2
10	370	0.76×10^{13}	1740	5.3

These soft surface treatments only lead to a change of the surface potential while the other parameters are not affected. In contrast, if the sample is exposed to low power in SF_6 plasma for over 300 sec, lowering the 2DEG density and increasing the on resistance were observed. These results indicated that the SF_6 plasma time plays a role to control the surface potential influencing interface states and shallow traps. The AES-depth profile from the surface to AlGaN/GaN to investigated the permeation probability of F^- ions during plasma treatment process in Fig. 4.12 (a). The fluoride atoms were distributed near the GaN surface within the 7 nm. Most of them controlled by soft etching condition was detected at the surface of AlGaN layer which not to invade the channel. The presence of fluorine near the surface of GaN layer plays the major role in enhancing the device performance. In order to investigate the influence of SF_6 plasma treatment in the trapping of charges in HEMT devices, current collapse measurement were carried out. The source-to-gate distance, gate length, and gate-to-drain distance were 3, 2, and 3 μm, respectively. As shown in Fig. 4.13 (a) and 4.13 (b) pulsed output characteristics measured for devices with and without SF_6 plasma treatment, respectively. Pulsed characteristics at different quiescent bias point are compared to a 2 x 100 μm^2. For these measurements, the gate quiescent bias point was kept constant while the drain sweeps voltage up to 40V. Pulse duration and the period were 200 ns and 1 ms respectively. It is evident that the current showed a large decrease, as well as knee voltage walk-out for the untreated device whereas minor degree of collapse was observed for treated sample.

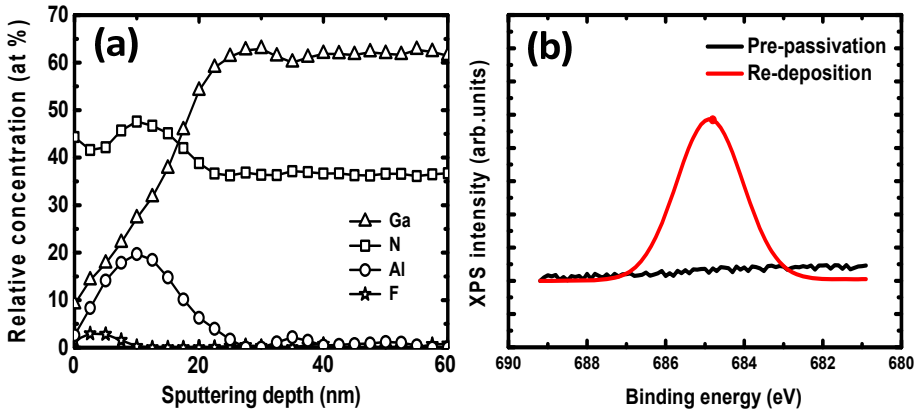


Fig.4.12 (a) AES measurement of the device with exposure SF_6 plasma at the RF power 10 W. (b) XPS spectra of F1s photoelectrons for the GaN surface with and without exposure to SF_6 plasma, respectively

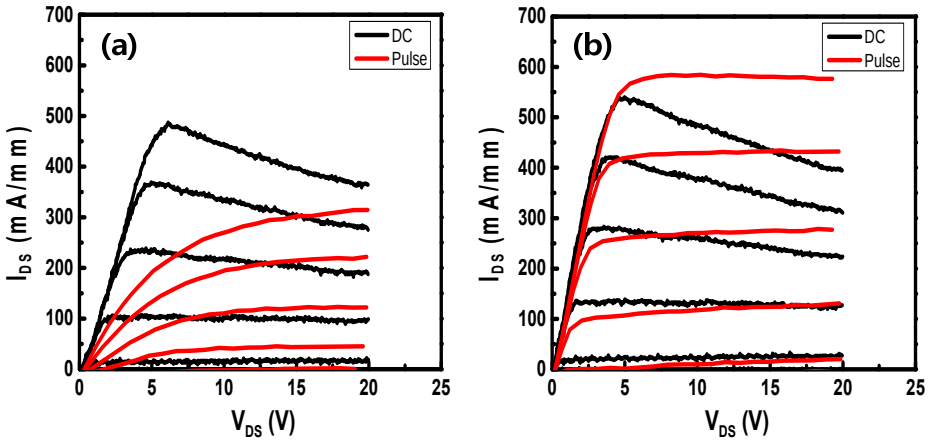


Fig.4.13. Pulsed output characteristics measured for devices (a) without and (b) with SF_6 plasma treatment

4.5 Device Characterization

In this section, the DC, small signal, pulsed and large signal characteristics of the AlGaN/GaN HEMTs on silicon substrate which have been used for experiments in the remainder of the thesis are shown.

4.5.1 DC and Small Signal Performance

The epitaxial structures of the GaN HEMTs are shown in Fig. 4.14. The epitaxial layers grown on silicon (111) substrate consisted of a 20 Å GaN capping layer, a 100 Å $Al_{0.30}GaN$ barrier layer, a 1 μm GaN buffer layer, and AlN/GaN transition layers from top to bottom. A sheet resistance of 290 Ω/sq and carrier and mobility of 1800 $cm^2/V{\cdot}s$ were measured. The HEMTs are 100 μm wide, with a gate length of 0.25 μm; L_{GD} = 2.5 μm, L_{GS} = 1 μm.

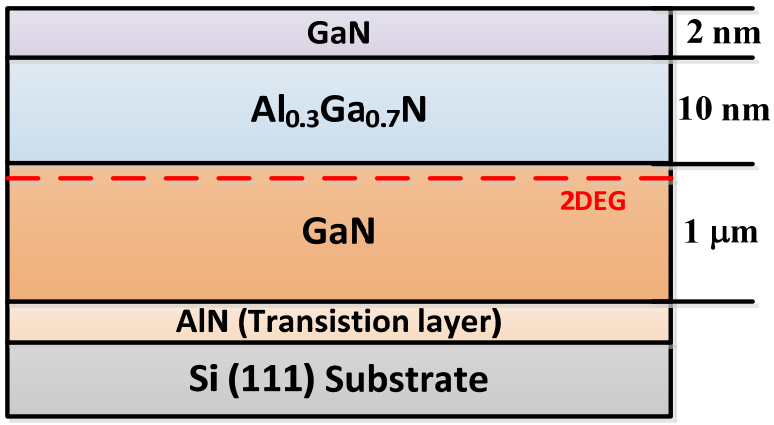


Fig 4.14 Epitaxial structure of HEMTs

On-wafer dc performances were performed using an HP4155 semiconductor parameter analyzer. Fig 4.15 shows the DC *I-V* characteristic for fabricated devices. The device exhibits high drain current and good pinch-off characteristics. The maximum drain current I_{MAX} = 900 mA/mm at gate bias of 0V and a drain bias of 5 V. The knee voltage was less than 4 V at gate-biases up to 0 V, which is attributed to the excellent ohmic contact. The dc transfer characteristics at a drain bias of 5 V are shown in Fig. 4.16. A peak extrinsic transconductance (g_m) of 350 mS/mm was measured. By defining the threshold voltage as the gate bias intercept of the extrapolation of at the point of peak transconductance, the threshold voltage of the device was determined to be -2.6 V.

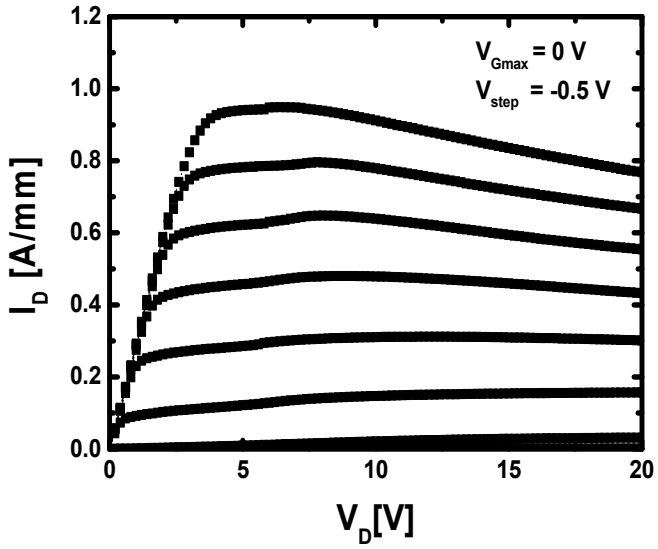


Fig 4.15 DC *I-V* characteristics of $Al_{0.3}Ga_{0.7}N$/GaN HEMT with a gate length of 0.25 μm and a gate width of 100 μm

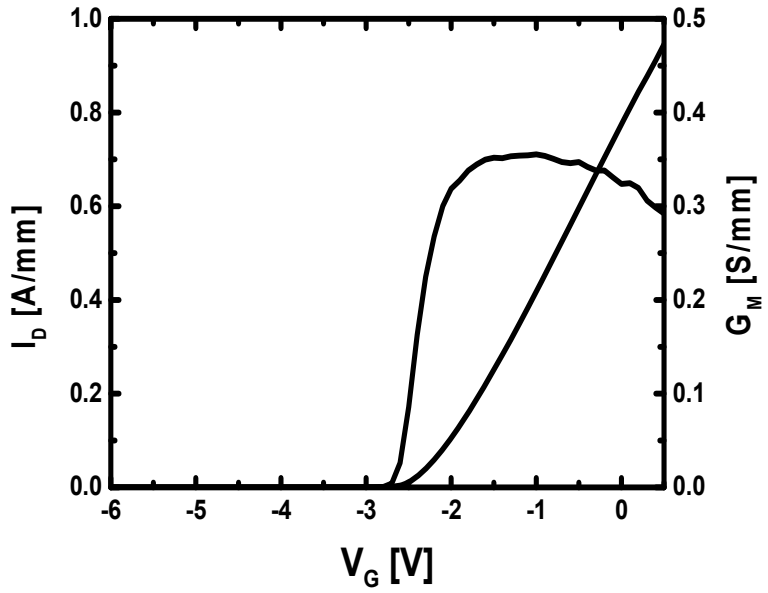


Fig 4.16 DC transfer characteristics of $Al_{0.3}Ga_{0.7}N$/GaN HEMT with a gate length of 0.25 μm and a gate width of 100 μm

Fig 4.17 shows typical small-signal RF characteristics measured from on-wafer S-parameter measurement. On wafer open and short patterns were used to subtract the effect of parasitic pad capacitances and inductances from the measured S-parameters [36]. A f_T = 28 GHz and f_{max} = 66GHz values were obtained by the extrapolation of $|h_{21}|$ and MSG/MAG using a -20 dB/decade slope at V_{DS} = 15 V and V_{GS} = -2.1 V. In Fig 4.18 the fabricated device with source field plate shows slight improvement in power gain and f_{max} that result from the reduced the gate-to-drain capacitance. For comparison, the extracted intrinsic parameters and calculated f_T/f_{max} is shown Table 4.2

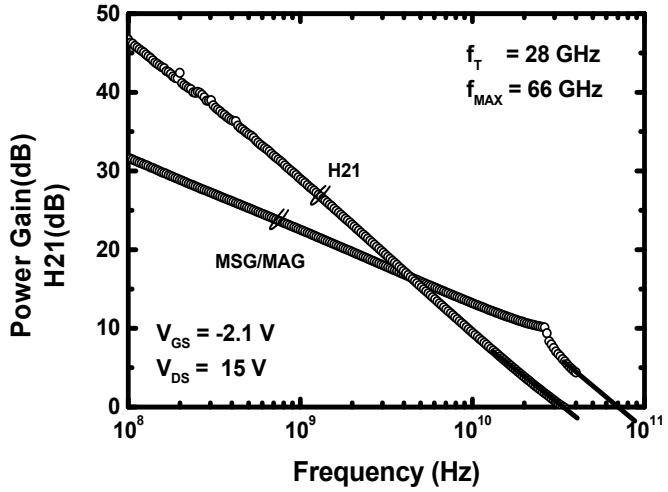


Fig 4.17 RF performance of 250-nm-gate-length HEMT showing f_T = 28 GHz and f_{max} = 66 GHz

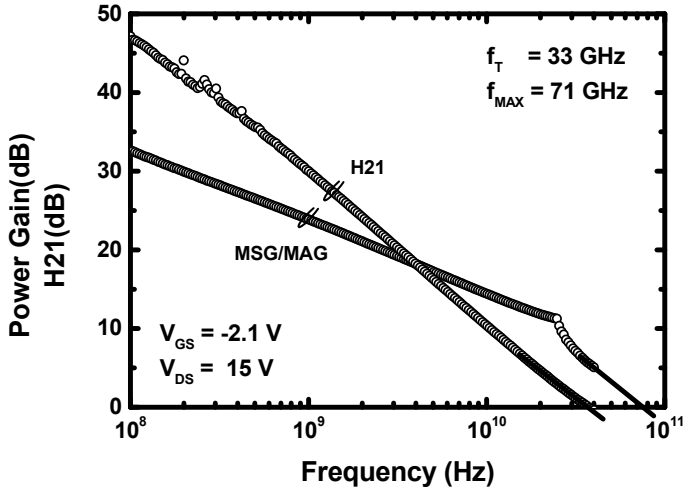


Fig 4.18 RF performance of 250-nm-gate-length HEMT with source field plate showing f_T = 33 GHz and f_{max} = 71 GHz

Table 4.2 Measured and calculated device intrinsic parameters of AlGaN/GaN HEMT with and without source field plate

	w/o SFP	with SFP
f_T (GHz)	29	33
f_{max} (GHz)	66	71
C_{gd} (fF/mm)	215	142
C_{gs} (fF/mm)	1227	1013
C_{gd}/C_{gs}(fF/mm)	0.176	0.140
C_{ds}(fF/mm)	469	270
Gain (dB) @ 10GHz	13.16	14.39

4.5.2 Pulse Characteristics

The data in this section is based on pulsed I-V measurement. The pulsed I-V characteristics were performed on an Accent DIVA pulse system. This system has the capability to pulse both the gate and drain voltages simultaneously, so that the pulsed "off" state can be any voltage [37]. Pulsed characteristics at different quiescent bias point are compared to a 0.2 x 100 μm^2 in Fig. 4.19. Pulse duration and the period were 200 ns and 1 ms respectively. A comparison between the quiescent bias point at V_{DS0} = 0 V, V_{GS0} = -8 V and V_{DS0} = 30 V, V_{GS0} = -8 V permits analyzing trapping effect.

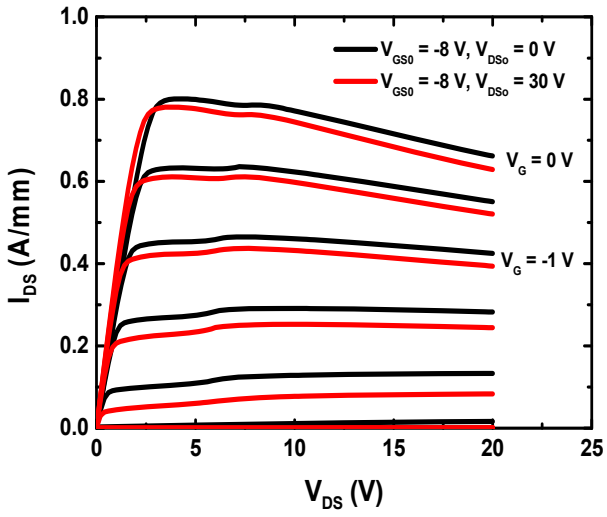


Fig 4.19 Pulsed I_D-V_{DS} characteristics of GaN-on-Si HEMT for SF_6 plasma treatment device with different quiescent bias point: V_{GS0} = -8 V, V_{DS0} = 0 V is compared to V_{GS0} = -8 V, V_{DS0} = 30 V

A drop of less than 5 % regarding the maximum drain current is noted at V_{DS} = 30 V. SF_6 plasma treatment processes as mentioned above have been optimized to reduce trapping phenomenon which originated from the surface. It was found that the proposed process in conjunction with a field plate structure was a very effective way to reduce the trapping problem. Almost no drain lag effect appears due to the benefit of the optimized passivation process.

4.5.3 Large Signal Performance

On-wafer measurements were performed on a microwaves load-pull system at 9.3 GHz and a drain bias of 25 V, using 50 Ω microwave probes. A power sweep for a 0.2 mm HEMT is plotted in Fig 3.16. The device shows power density of 6.32 W/mm, PAE of 54 % and drain efficiency of 67.9 %. The high linear gain of 13 dB is substantial compared to all other AlGaN/GaN HEMT's on silicon substrate reported at X-band.

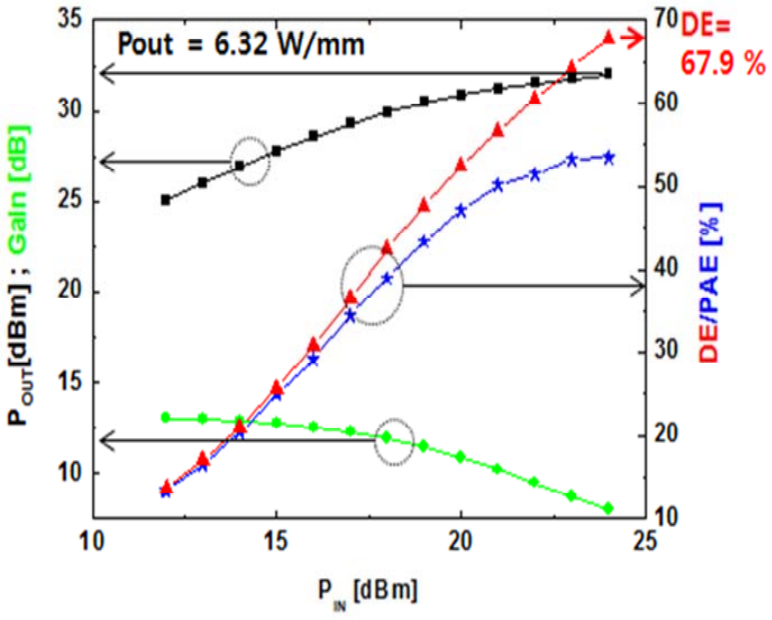


Fig 4.20 A 9.3 GHz CW power sweep for a 0.2 mm AlGaN/GaN HEMT on silicon substrate. The device was biased at V_{DS} = 25 V, and V_{GS} = -1.5 V

RF power measurement s of large devices was also performed on wafer at 9.3 GHz. Figure 4.21 shows the microwave power characteristics of 1.2 mm HEMT (6 x 200 μm) gate periphery with L_g = 0.25, L_{gs} = 1, and L_{gd} = 2.5 μm at 9.3 GHz. The bias points were V_{DS} = 25 V and V_{GS} = -2.5 V under class AB operation. The saturated power level was 35.4 dBm (3.46 W), the power added efficiency (PAE) was 31.7 %, and the linear power gain was 10.7 dB.

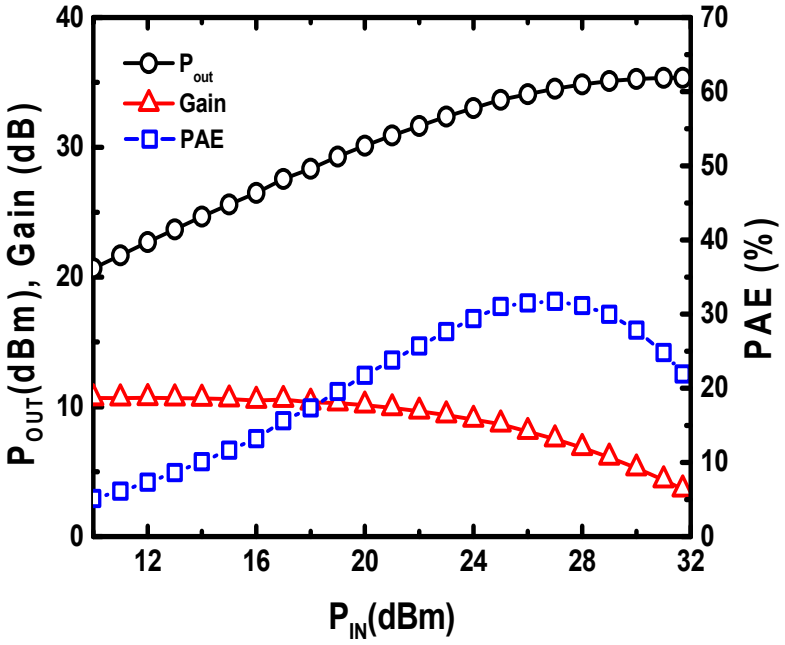


Fig 4.21 Output Power, gain and power-added efficiency for a 1.2 mm AlGaN/GaN HEMT as a function of input power under CW operation at 9.3 GHz

Figure 4.22 shows the microwave power characteristics of 2.4 mm HEMT (12 x 200 μm) gate periphery at 9.3 GHz. The bias points were V_{DS} = 20 V and V_{GS} = -2.5 V under class AB operation. The saturated power level was 37.4 dBm (5.5 W), the power added efficiency (PAE) was 33.6 %, and the linear power gain was 9.4 dB. The output performances of larger periphery device on silicon substrate are limited by thermal effects. In order to solve the thermal issues it is crucial to have the optimized device layout, substrate, and backend processing.

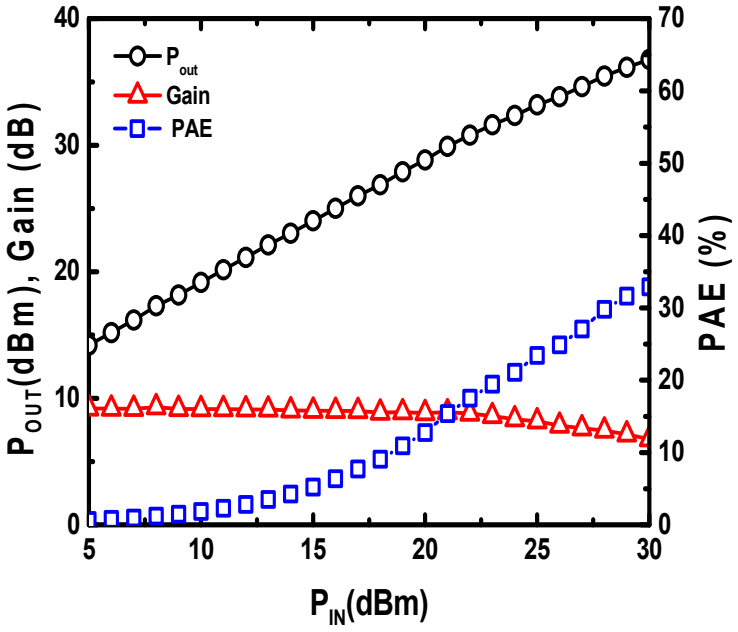


Fig 4.22 Output Power, gain and power-added efficiency for a 2.4 mm AlGaN/GaN HEMT as a function of input power under CW operation at 9.3 GHz

4.6 Wide Periphery Devices

Gallium nitride (GaN) grown on silicon (Si) substrates is a very promising technology for microwave applications. It combines the low cost and ease of manufacturing associated with large diameter Si substrates and the demonstrated high power density and high efficiency offered by AlGaN/GaN devices [38]. In previous section, we demonstrate high power densities of 6.32 W/mm and 54 % power added efficiency (PAE) for AlGaN/GaN HEMTs on silicon substrate at 9 GHz. Many impressive power densities have been reported from small-periphery GaN-on-Si HEMTs [2, 3]. In general, the large-periphery power density at X band is still considered low, which is greatly limited by the heating effect [39]. In previous section, the output power characteristics of AlGaN/GaN HEMTs with 0.25, 1.2, 2.4 mm total gate width was discussed. However, power performance of the large device is limited by thermal effect. These results gave us the information we required to try and resolve the issues which cause low power density of large periphery GaN-on-Si HEMTs. This section will present high-power performance of AlGaN/GaN devices fabricated on high resistivity silicon substrate at 8 GHz. It combines optimized device fabrications as mentioned chapter 3, 4 and device package, the single-cell HEMTs device of 3.6-mm gate width achieved output power density of 8.1 W/mm with output power level of 30 W.

4.6.3 Large Signal Performance

A Maury Microwave load pull system was used to measure the output power at 8 GHz as shown in Fig 4.23.

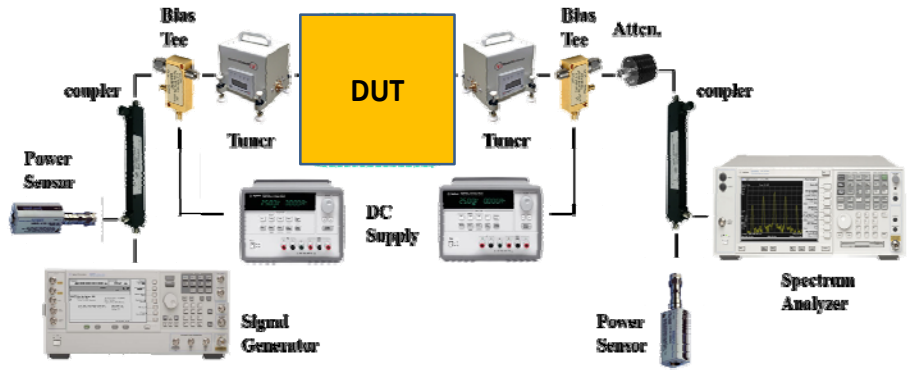


Fig 4.23 Load-pull measurement system setup

The characteristics of small periphery device were already mentioned above. The large size devices show almost same performance with those of 0.25 mm devices. The silicon substrate was grounded and polished to 60 μm to reduce thermal resistance. As mentioned previous section, the tapered via etching process was applied. It provided very low inductance grounding to the source connection. The backside was metalized and electrically connected to the source fingers on the front side. Matching network consisted in gate and drain of the transistor was designed for avoiding low frequency oscillation. Besides delivering bias to the active devices, the bias paths are also used to prevent potential instabilities resulting from a coupling of the various active

devices through the bias path [53]. Fig 4.25(a) shows matching network which was designed on R4350 PCB substrate. The 3.6-mm chip was mounted on a Cu metal block with Au-Sn eutectic die-attach for heat sinking and interconnected to the matching circuit with Au wire bonding in shown Fig 4.25(b).

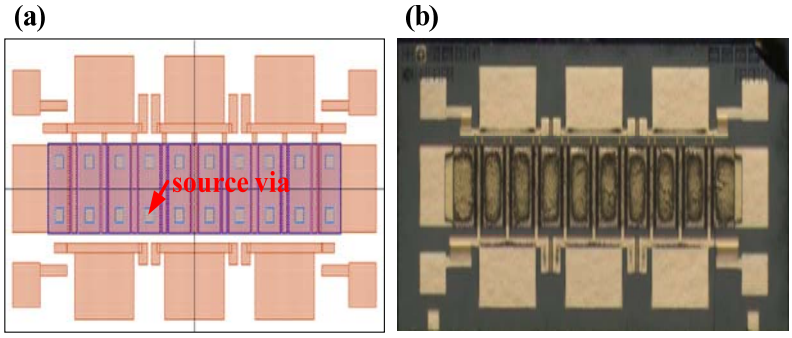


Fig 4.24 Photograph of AlGaN/GaN HEMT chip (a) device layout (b) fabricated device

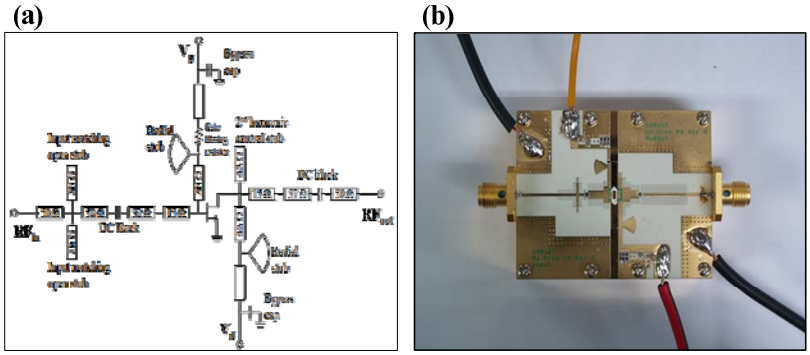


Fig 4.25 (a) schematic of matching circuit and (b) photograph of test-fixture with mounted device

The temperature of the metal block was kept at approximately 25 ^{0}C during the power measurements. Fig 4.26 shows the operating drain voltage dependency of saturated output power, power added efficiency and gain at 8 GHz. It is noticed that the output power increase with power added efficiency.

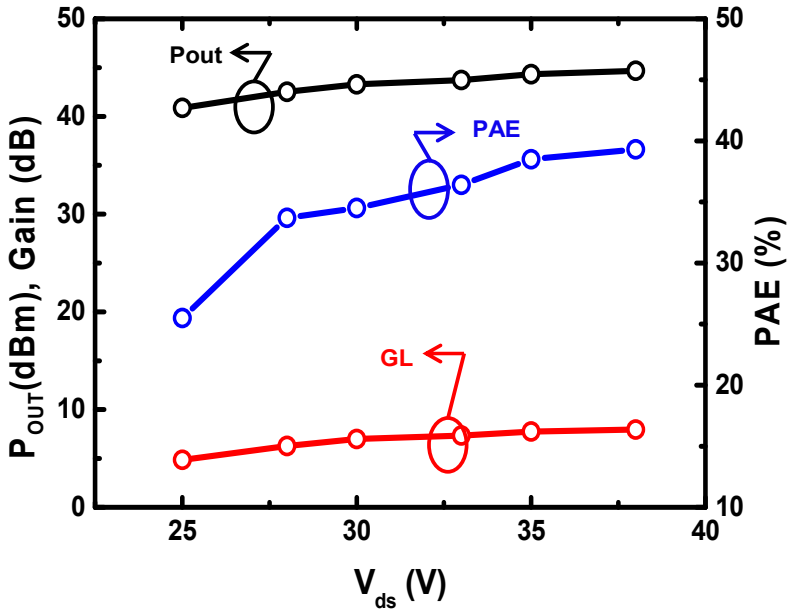


Fig 4.26 Operating voltage dependence of saturated output power, power-added efficiency and gain under pulsed operation at 8 GHz. *W*g = 3.6 mm

Fig 4.27 shows the operating drain voltage dependency of RF output power density at 8 GHz measured. The load-pull tuning was optimized for maximum output power. At a drain bias of 38 V, the device had an output power density of 8.1 W/mm and an associated PAE of 39.3%. The output power density continued to increase with drain bias which indicates a good dispersion control in the device. Moreover, substrate thinning and ISV process could definitely improve the thermal dissipation of the device.

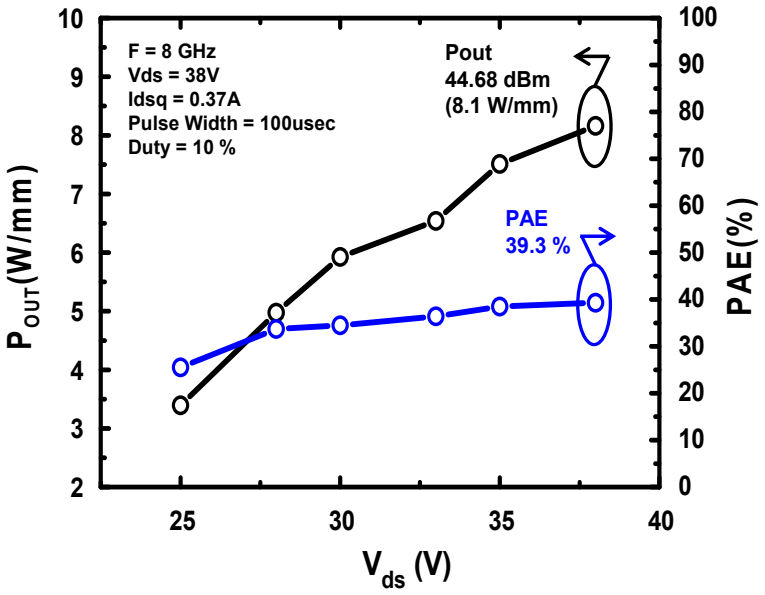


Fig 4.27 Operating voltage dependence of power density and power-added efficiency under pulsed operation at 8 GHz

Fig 4.28 shows the microwave power characteristics of a single chip of 3.6 mm gate periphery at 8 GHz. The bias points were V_{DS} = 38 V and V_{GS} = -1.8 V under class AB operation. The saturated power level was 44.68 dBm (29.4 W), the power added efficiency (PAE) was 39.3 %, and the linear power gain was 8 dB under the pulsed condition of 100 μs pulse width and 10 % duty cycles.

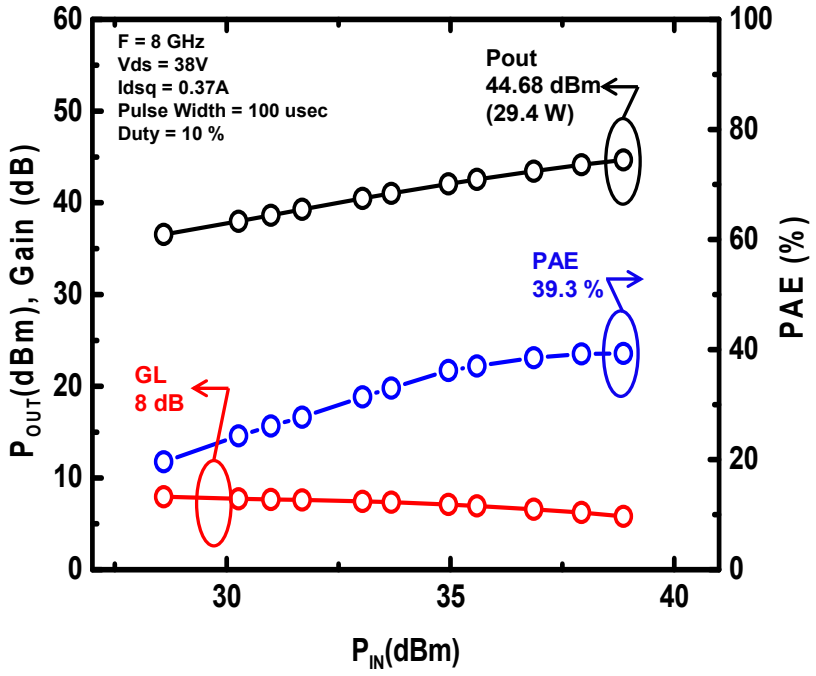


Fig.4.28 Output Power, gain and power-added efficiency for a packaged AlGaN/GaN HEMT as a function of input power under pulsed operation at 8 GHz

4.7 Summary

This chapter has given an insight into how AlGaN/GaN device fabricate and key process technologies are when it comes to producing high frequency HEMT designs. This research will mainly focus on the current collapse of the devices. It is clear that the most common approaches to engineering electric field distribution are to employ filed plate structure. SF_6 plasma treatment processes have been optimized to reduce trapping phenomenon which originated from the surface. It was found that the proposed process in conjunction with a field plate structure was a very effective way to reduce the trapping problem. However, power performance of the large device is limited by thermal effect. These results gave us the information we required to try and resolve the issues which cause low power density of large periphery GaN-on-Si HEMTs. To solve this issue, backend process with individually grounded source via formation was proposed. Optimized backend process would improve overall device performance by reducing thermal effect. Based upon it, GaN HEMT amplifier with single chip of 3.6 mm gate periphery has been successfully developed. It exhibits very high power density of 8.1 W/mm with 29.4 W output power under V_{DS} = 38 V pulse operating condition.

4.7 Reference

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Chapter 5

AlGaN/GaN HEMTs for Power applications

5.1 Introduction

This chapter will give development and optimization of the recessed GaN MIS-HEMT technology. Enhancement mode devices are also attracting a great interest as they allow simplistic circuity and safe operation. However, in spite of the excellent results achieved in depletion-mode devices, the performance of enhancement-mode devices is still modest [1]. It is difficult to obtain E-mode operation with a low on-resistance and a high breakdown voltage. The basic fabrication principles for both D-mode and E-mode devices for a very similar process but the gate process are quite different. A gate recess technique will be crucial to realize an enhancement-mode operation and improve the transfer characteristics. These processes will be detailed description given. The results in chapter 3 showed that excellent results in depletion mode (D-mode) AlGaN/GaN high electron mobility transistors (HEMTs) with the inclusion of fluoride plasma treatment beneath the active area. It was assumed that the consequence of this would be a minor change in

the dynamic access resistance which related to current collapse phenomenon.

5.2 Advantages of AlGaN/GaN HEMTs for Power Switching Devices

Wide bandgap semiconductors such as GaN and SiC serve high breakdown strength which enables high breakdown voltages together with low on-state resistance in the power switching transistors [2]. The performance is expected to overcome the limitation in conventional Si-based power devices, which would make the switching systems very efficient [3]. Figure 2.8 shows comparison of specific of R_{on} for Si, SiC, and GaN versus breakdown voltage which indicate the superior properties of GaN devices [4].

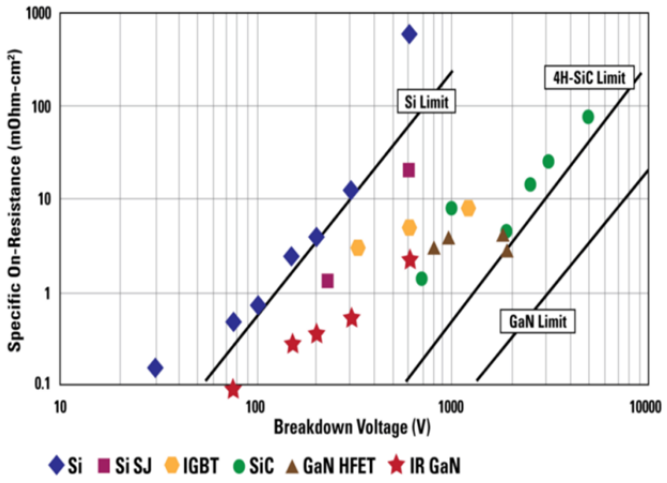


Fig 5.1 Comparison of R_{on} for Si, SiC, and GaN versus breakdown voltage [5]

5.2.1 Enhancement-mode Operation

Most AlGaN/GaN HEMTs show normally-on operation because the 2DEG exists under the gate at a gate bias voltage of 0 V as mentioned previously. For power electronics applications, however, normally off operation is required to simplify the design of driving circuits and safe operation [6]. Several techniques for the normally-off operation of the AlGaN/GaN HEMTs have been reported such as using a thin AlGaN barrier layer [7, 8], a recessed gate structure [9, 10], a fluoride-based plasma treatment [11], and a p-type gate structure [12]. The most popular and efficient method is to reduce the barrier layer thickness under the gate. The channel can be easily depleted under the gate for normally-off operation due to the reduced 2DEG density, but the devices suffer from reduced drain currents and high on-resistances since the low density 2DEG is across the entire source-drain region [13]. The selective thinning of the AlGaN layer can be realized by ICP dry etching, resulting in a recessed-gate structure. With a deep-enough gate-recess etching, the 2DEG can be completely depleted at zero gate bias and E-mode HEMTs are formed. However, the ICP dry etching technique has a low etch selectivity between nitride-based materials resulted in the non-uniformity in the recess-etching depth, and consequently the uniformity in threshold voltage is poor. Moreover, the damages and associated defects caused by the ICP-dry etching lead to an increase in gate leakage, and in surface roughness. To avoid this, the control of the threshold voltage was realized through a modulation of energy band by F^- ions implanted in the AlGaN/GaN heterostructure

during the plasma treatment. The fluorine ions have a strong electronegativity and are negatively charged, effectively raising the potential in the AlGaN barrier and the 2DEG channel. As a result, the V_{th} can be shifted to positive values, and E-mode HEMTs can be fabricated [11]. For practical application, the E-mode device with fluorine treatment has reliability and stability issues. Another method is encapsulating the AlGaN barrier with a p-type GaN layer at the gate. A negative spatial charge is induced at the interface between the AlGaN barrier and GaN cap layers by piezoelectric polarization. The p-doping and negative spatial charge reduces the sheet carrier density of the channel under the gate [14].

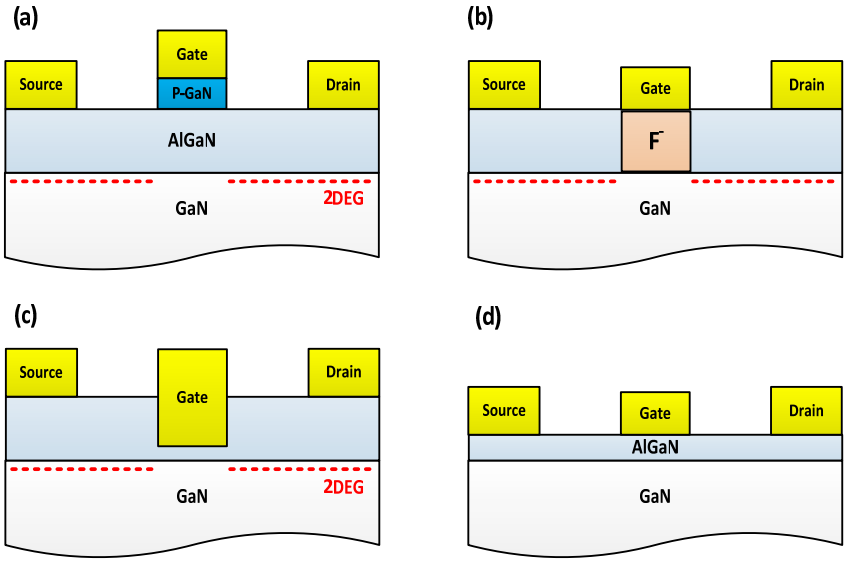


Fig 5.2 Various approach to fabricate E-mode AlGaN/GaN HEMTs : (a) p-type gate structure, (b) a fluoride-based plasma treatment, (c) a recessed gate structure, (d) thin AlGaN barrier layer

5.5.2 High Breakdown Voltage

The key operating parameters for power switching device is the off-state breakdown voltage (V_{BD}). The common definition of breakdown given is the time gate leakage current reach 1 mA/mm. Many groups demonstrated physical mechanism responsible for breakdown in GaN HEMTs. The most common theory which explains breakdown is impact ionization in the channel that usually occurs near the gate edge on the drain side. The electrons injected from the gate gains enough energy at the gate-drain region of high electric field cause impact ionization. Tan *et al*. proposed a surface-hopping conduction mechanism. This mechanism induced an increase the gate-drain leakage result in charge trapping and leakage processes. Fig 5.3 shows off-state breakdown mechanism. Also a buffer-related breakdown have been suggested by several research groups [15]. By improvement of processing technologies and the employment of new device structures, off-state breakdown characteristics have been effectively improved in GaN-based HEMTs. It is generally accepted that fabricated HEMTs with field plate structure achieving a high breakdown voltage due to the electric field between drain and gate can be more uniformly spread [4, 16, 17].

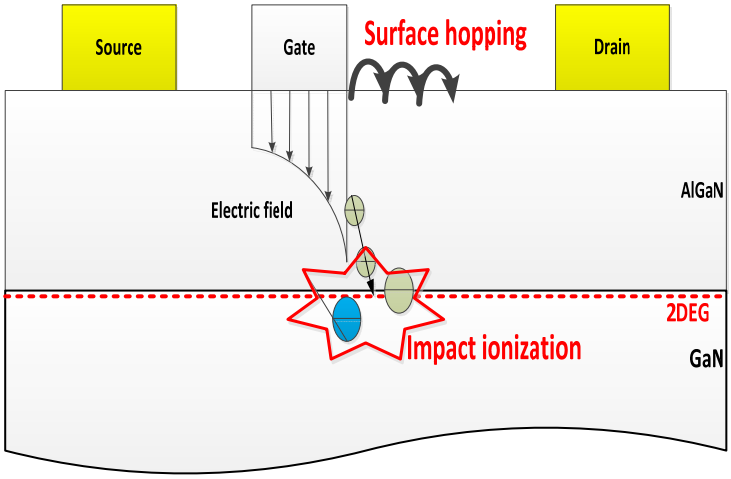


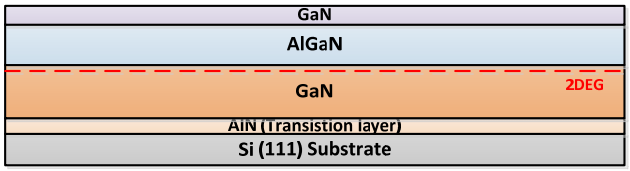
Fig 5.3 Off-state breakdown mechanisms in GaN HEMTs [18]

5.3 Device Fabrication

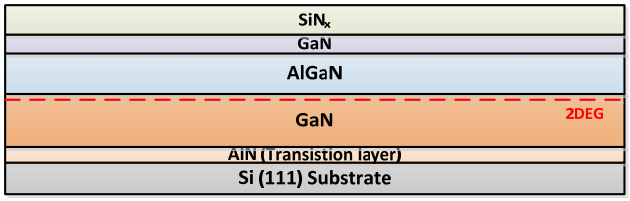
Device fabrication was carried out in the Inter-University Research Center, Seoul National University. The following will outline the process to take surface preparation through to the complete working device stage in shown Fig 5.4. The details were as same as previously mentioned in chapter 2 except a gate process.

The epitaxial layers grown on silicon (111) substrate consisted of a 40 Å GaN capping layer, a 200 Å $Al_{0.24}GaN$ barrier layer, a 3.9 μm GaN carbon-doped buffer layer, and AlN/GaN transition layers from top to bottom. Sheet resistance of 530 Ω/sq and carrier mobility of 1800 $cm^2/V \cdot s$ were measured. A SiN_x pre-passivation layer was deposited at 350 °C using inductively coupled plasma chemical vapor deposition (ICP-CVD). The ohmic contacts were formed by using a Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm) metal stack, followed by 800 °C for 30 sec in N_2 ambient. The ohmic contact resistance was 0.6 Ω-mm measured by transfer length method. Device isolation was carried out by inductively coupled plasma (ICP) etching, utilizing BCl_3/Cl_2 gas. A new 2000 Å SiN_x passivation layer was subsequently re-deposited by ICP-CVD at 350°C which also serves as the ICP etching mask. The first lithography defined the foot of the gate. Then, the gate was transferred to the thick SiN_x layer with SF_6 –based dry etch. Over etch at 8 V was performed to assure avoiding the fluoride ions into AlGaN barrier. The gate recess was carried out using a low-damage Cl_2/BCl_3-based RIE where the target etch depth was remains AlGaN barrier layer in order to improve the transfer characteristics. A Ni/Au multilayer was deposited for

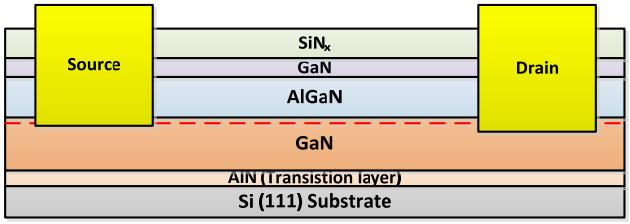
the gate contact.



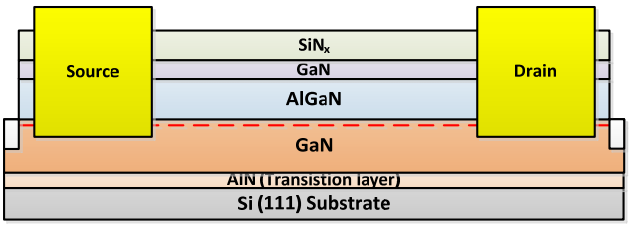
(a) Surface cleaning for device fabrication



(b) SiN_x passivation



(c) Ohmic formation



(d) Mesa isolation

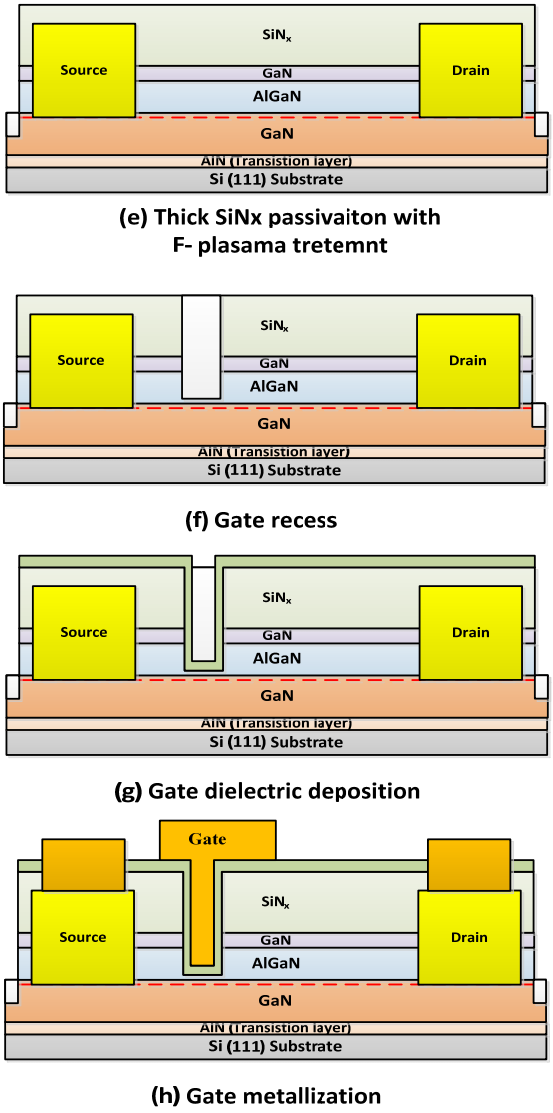


Fig 5.4: Device process (a) Surface cleaning for device fabrication, (b) SiN_x passivation, (c) Ohmic formation, (d) Mesa isolation, (e) Thick SiN_x passivation with F^- plasma treatment, (f) Gate recess, (g) Gate dielectric deposition, and (h) Gate metallization

5.3.1 Gate Recess Process

In this section, the effect of the gate recessing on device characteristics is described. As shown in the section 5.2.1, several techniques for the normally-off operation of the AlGaN/GaN HEMTs have been reported. Among them, selective thinning of the AlGaN layer was the most effectiv way which can be realized by ICP dry etching. However, general observations show that the recess process itself increases the surface roughness [19, 20] or that it introduces damage into the barrier [21, 22], both possibly causing a drop in electron mobility μ_n in the 2DEG [23]. Inductively coupled plasma-RIE (ICP-RIE) tool which obtain a high density plasma with low DC bias at the same time can be demonstrate the full potential of the recess process [24]. However, the controllability of the recess depth and dry-etching-induced plasma damage are still the major challenges in obtaining high performance E-mode GaN HEMTs [25, 26]. Many works have been demonstrated normally-off operation by complete removal of barrier layer in the gate area in order to use a MOSFET structure [27-33]. Completely recessing the AlGaN barrier not only reduces the carrier concentration under the gate region but also brings the interface under the gate dielectric close to the channel [34]. The partial recessing the AlGaN barrier in association with opimization of the gate recess technique is discussed in the following.

Gate recess etch is performed the active region of device thus requiring low damage process to ensure optimum device performance. Low damge etching can be achieved by decreasing the ion energy. However, this can decrease the uniformity of the etch or minimize the utility of the etch. Therfore, etch processes should address several issues such as surface morpholoty, uniformity, and low damage which result in device performance. The epitaxial layers grown on silicon (111) substrate consisted of a 40 Å GaN capping layer, a 200 Å $Al_{0.24}GaN$ barrier layer, a 3.9 μm GaN carbon-doped buffer layer, and AlN/GaN transition layers from top to bottom. The gate recess structure was patterned by photolithograpy using AZ5214 photoresist. The patterned structure were exposed to Cl_2/BCl_3 plasma. The standard ICP etch paramters used in for the damage study were 2 sccm of BCl_3, 18 sccm of Cl_2, and 5 mTorr pressure kept fixed while ICP power and bias power was used variable. During the etching, the ICP power was varied from 100 to 300 W at a constant bias power of 5W. In addition, the ICP power of 200 W was kept constant during varying bias power 1 to 5 W. The etch step height and surface roughness were studied using AFM operated in contact mode after photoresist was removed. The etch-induced damage of an inductively coupled plasma (ICP) etch system was investicated on electrical performance of recessed GaN MIS-HEMTs. Fig 5.5 shows the effect of dc bias along with the corresponding GaN etch rate. Under the ICP power of 200 W, GaN layer was not etched which is not acceptable in ICP etching conditions.

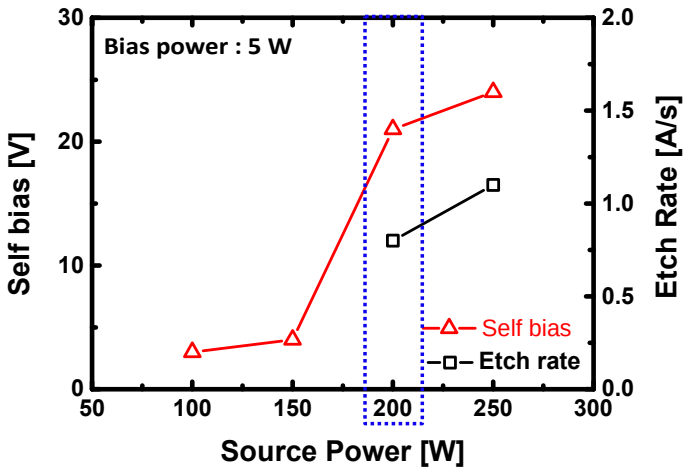


Fig 5.5 Etch rate and dc bias voltage of GaN as a function of ICP power

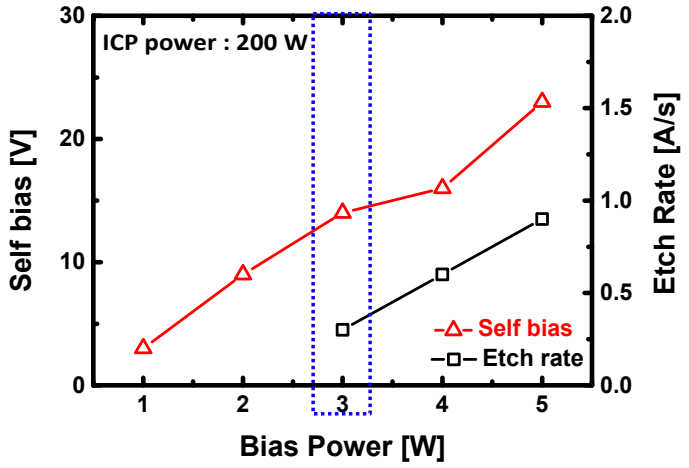


Fig 5.6 Etch rate and dc bias voltage of GaN as a function of Bias power

The ICP power of 200 W was kept constant. The effect of bias power on the etch rate was studied as shown Fig 5.6. The etch rate decreased as the dc bias is decreased from 25 to 13 V. Etch rate of 0.26 Å/sec was obatained using a ICP power of 200 W and a bias power of 3 W. Under a low self bias contitions, the etched surface was smooth as shown Fig 5.7. The surface morphology of unetched GaN surface and etched layer was examined by atomic force microscopy (AFM). The unetched surface has an average root mean square roughness of 30 Å, while the etched surface has almost same value of it. This fact indicated that there is no roughness introduced by this etching process.

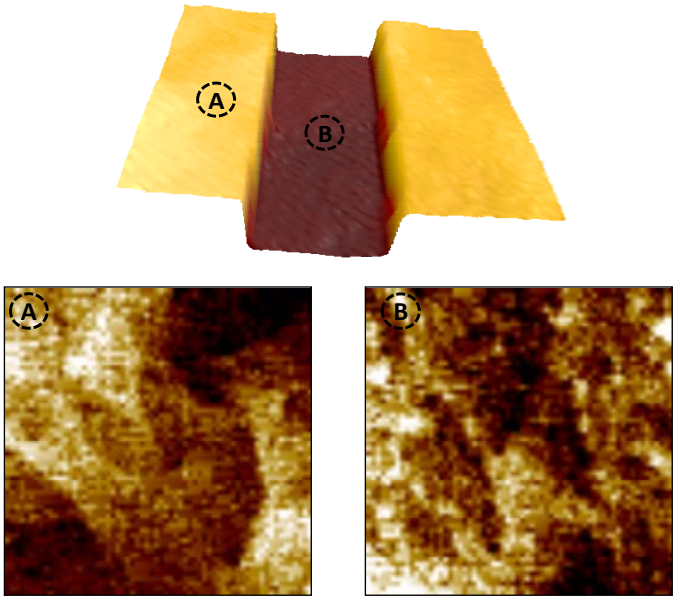


Fig 5.7 AFM images of unetched(left) and etched(right) GaN surfaces

To date, there has been a lots of work on the sysmetic characterization of ICP-RIE plasma induced damage on GaN surfaces [21, 35-39]. Among the various parameters of etching conditions, bias voltage was found to be the most significant cause of variation in plasma-induced damages to the GaN surface [40]. Etching damage have also been investicated by using fabricated recessed MIS-HEMTs. Fig 5.8 shows the schematic cross-sectional view of the device. The device feature a gate length of 2 μm, a gate-source distance of 3 μm, and a gate-drain distnace of 15 μm. The gate recess was carried out to complete remove the AlGaN barrier layer. After that a 30-nm SiN_x dielectric layer is deposited. Finally, gate metal and interconnections are formed by photolithography and Ni/Au metal was evaporated.

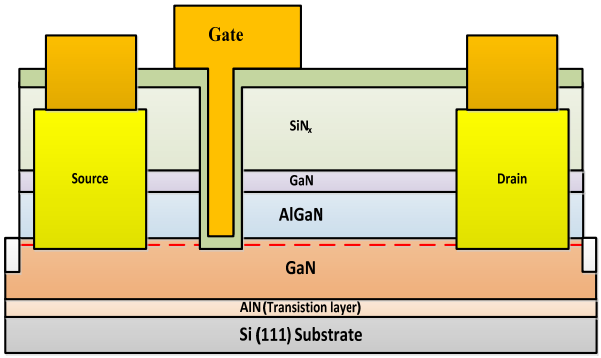


Fig 5.8 Schematic cross-section of AlGaN/GaN recessed MIS-HEMT

Transfer characteristics measured in order to investicate the influence of etching induced-damage on characteristics of the E-mode MIS-HEMT are shown in linear scale in Fig 5.9. With recess etching with high self bias, the drain current decrease by 45 % and the maximum transconductance decrease by 40 %. Therefore, the increasing the bias voltage would tend to increase the plasma-induced damge.

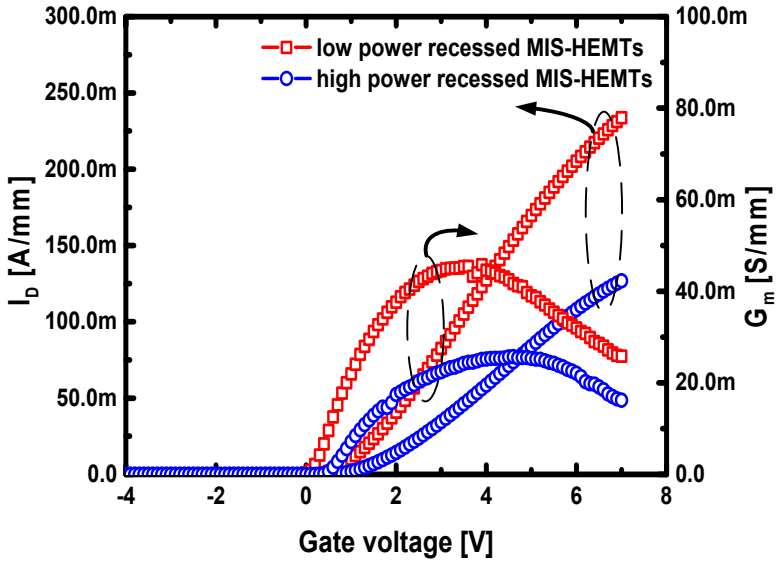


Fig 5.9 Transfer characteristics of normally-off AlGaN/GaN recessed MIS-HEMT measured at V_{DS} = 10 V. The gate region was etched with self bias of 14 V (square), and self bias of 24 V (circle)

5.3.1.1 Partial Gate Recess

E-mode HEMTs have been fabricated using recessed-gate structre for AlGaN/GaN material systems. In previous section, fabricated reseceed MIS-HEMTs using low power ICP-RIE etching process was described. Even though, etching induced damage during the fabrication process of recessed gate was minimized, the maximum transconductanc and the drain current were still lower than that of standard D-mode HEMTs. In this section, we will discuss the optimization of recessed AlGaN-barrier thickness which to be able to fully deplete the 2-dimentional electron gas. The interface roughness/state and electrical characteristics is evaluated in recess gate transistos with different recess depths. The schematic of the device with different recessed gate depth are shown in Fig 5.10.

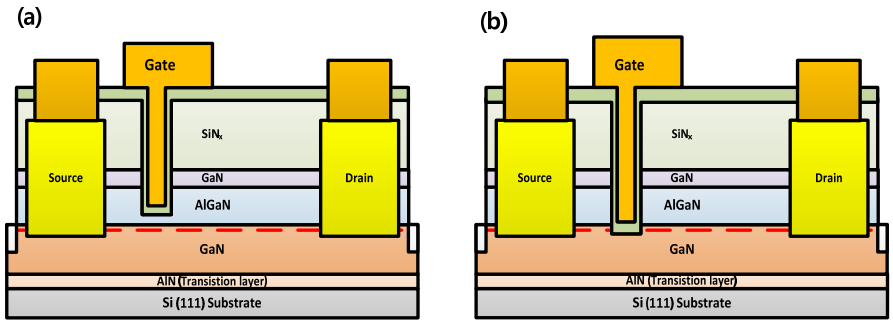


Fig 5.10 Schematic cross-section of recessed gate MIS-HEMT with 2 nm remaining AlGaN barrier (a) and 2 nm etch depth into the GaN channel

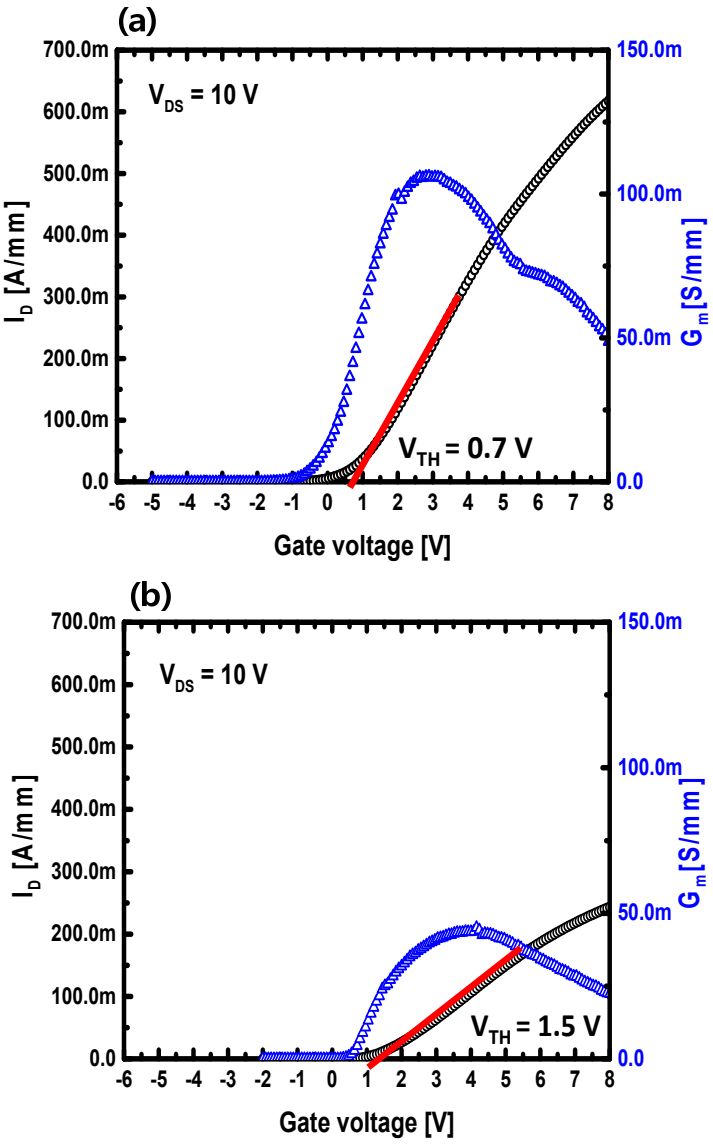


Fig 5.11 Measured transfer curves in linear scale (a) 2 nm remaining AlGaN barrier and (b) 2 nm etch depth into the GaN channel

Fig 5.11 (a) shows transfer characteristics for devices with a 2 nm reamining AlGaN barrier. The maximum drain current density and the maximum transconductance were 620 mA/mm at V_{GS} = 8 V and 110 mS/mm. Fig 5.11 (b) shows transfer characteristics for devices with 2 nm etch depth into the GaN channel. The maximum drain current density and the maximum transconductance were 250 mA/mm at V_{GS} = 8 V and 50 mS/mm. A fully recessed MIS-HEMT shows extremely lower current and transconductance compare with partially recessed MIS-HEMT. The specific on-resistance calculated from linear region of output curves is 0.45 $m\Omega \cdot cm^2$ for partial recessed device and 4.15 $m\Omega \cdot cm^2$ for fully recessed device as shown in Fig 5.12. No remarkable change in the gate leakage current was observed. The gate recess recipe as aforementioned was used for both devices. Even though a higher threshold voltage of 1.5 V is obtained for fully recessed device, much more current drop and transconductance degradation was observed. Fig 5.15 shows the experiment C-V characteristics of recessed MIS-HEMT with partial recess (black line), and fully recess (red line). The threshold voltage shift to positive slightly when recess depth was closed to the channel. The hysteresis for the partially recessed MIS-HEMT and fully receesed MIS-HEMT are 0.08 and 0.27 V, respectively. Completely recessing the AlGaN barrier layer reduces the carrier concentration under the gate region result in have much lower mobility due to the plasma induced damage. Moreover, scattering effect may impact access region in a device where the gate dielectric layer located at GaN channel without AlGaN barrier layer.

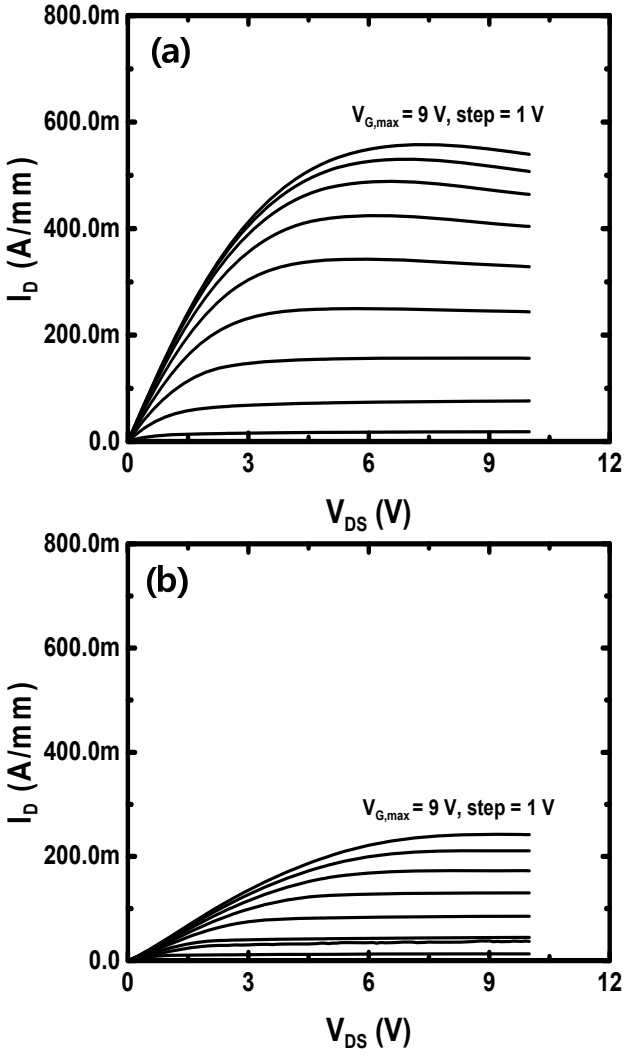


Fig 5.12 *I-V* characteristics (a) 2 nm remaining AlGaN barrier and (b) 2 nm etch depth into the GaN channel

The impact of the interface properties and the quality of the gate dielectrics is extensively evaluated in recessed gate transistors with different gate dielectric layers. In order to characterize the interface properties of the gate region where the gate dielectric layer located at GaN channel with and without AlGaN barrier layer, samples are passivated with a thin ICP-CVD SiN_x layer. To reveal the effect of existence of AlGaN barrier on interface properties, frequency-dependent capacitance-voltage characteristics were performed on SiN_x/AlGaN/GaN and SiN_x/GaN MOS capacitors, and the results are plotted in Fig. 5.13. From 4 kHz to 100 kHz, the SiN_x/AlGaN/GaN MOSCAP exhibits smaller frequency dispersion compared to the SiN_x/GaN MOS MOSCAP, suggesting an improved interface with low interface trap density. To investicate the effect of quality of dielectrics, samples are passivated with a thin PEALD SiN_x layer. Again, the device with a PEALD SiN_x gate dielectics shows less frequency dispersion in both cases in Fig 5.14. A better quality gate dielectric can reduced the electron scattering. Based on the aforementioned characterizations, the electrons can be easily transferred from the channel to the interface between the gate dielectric and GaN channel without AlGaN barrier in which case the screening becomes less effective. When the gate dielectric interface is very close to the GaN channel, the scattering effect plays a huge role. Fig 5.16 shows the extracted field-effect mobility in the MIS channel of a FAT-FET with 100 μm long gate length. The maximum value of μ_{FE} of partially receesed MIS -HEMT and fully receesed MIS-HEMT are 170 and 80 $cm^2/V{\cdot}s$, respectively.

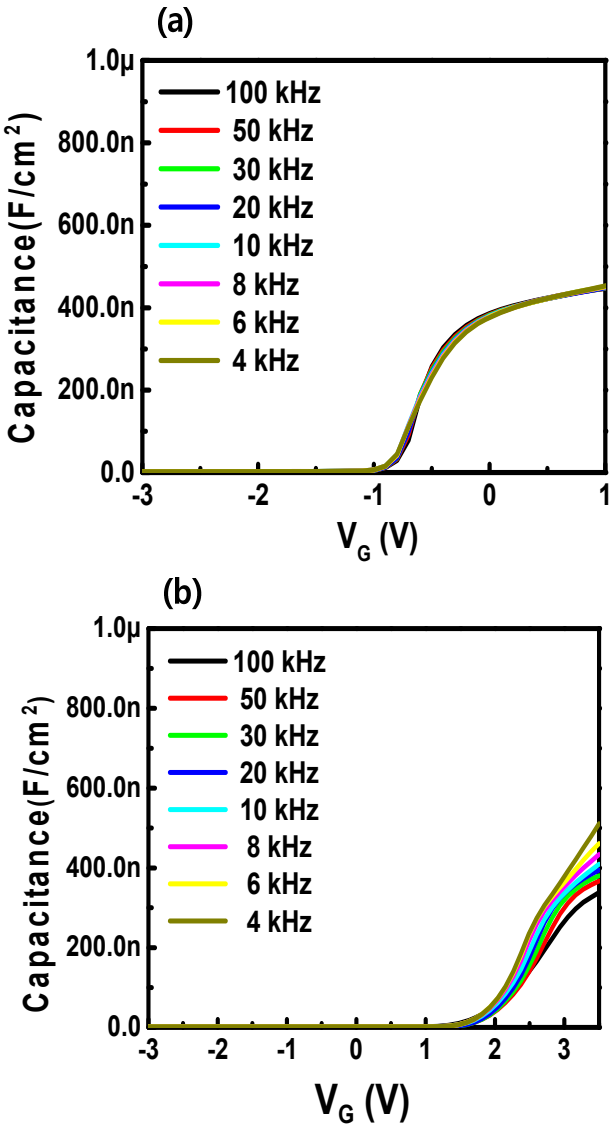


Fig 5. 13 Frequency-dependent C-V characteristics of (a) SiN_x/AlGaN/GaN and (b) SiN_x/GaN MOSCAP with ICP-CVD SiN_x. The sweeping rate is 0.1 V/s

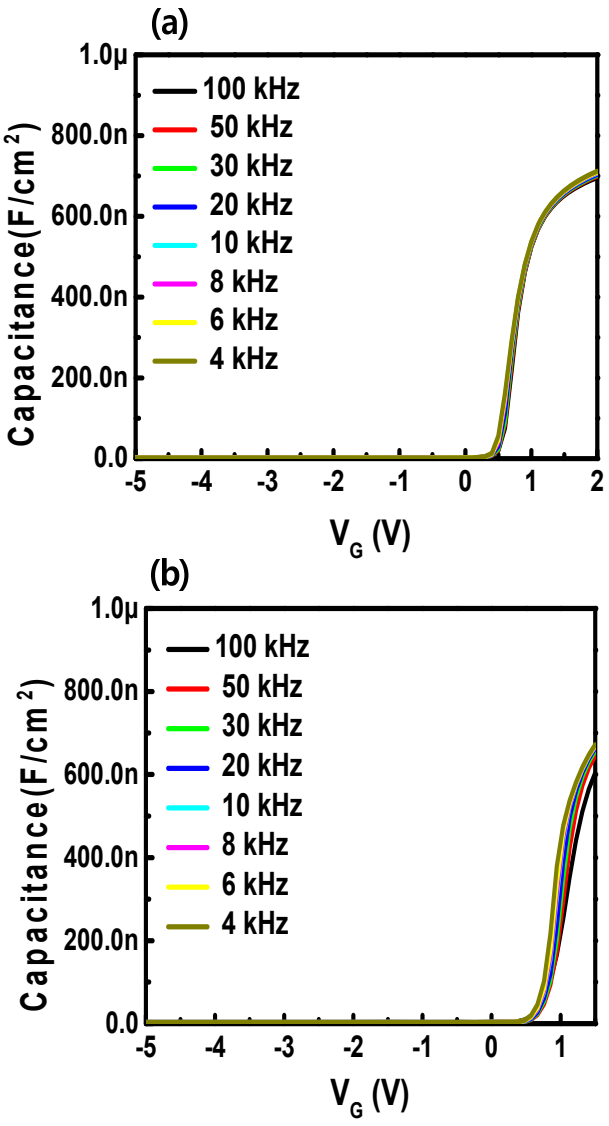


Fig 5. 14 Frequency-dependent C-V characteristics of (a) SiN_x/AlGaN/GaN and (b) SiN_x/GaN MOSCAP with PEALD SiN_x. The sweeping rate is 0.1 V/s

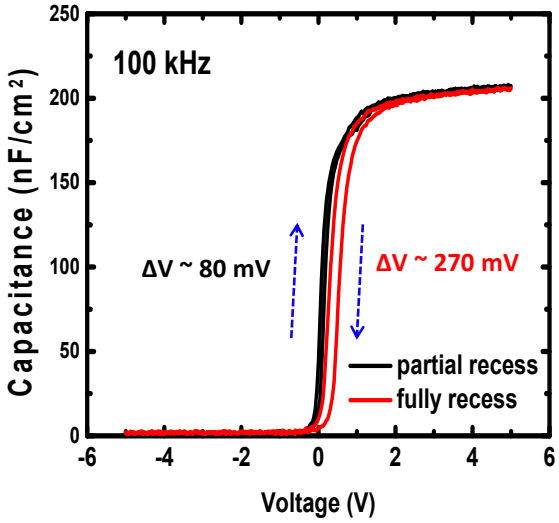


Fig 5.15 Measured C-V characteristics of recessed MIS-HEMT

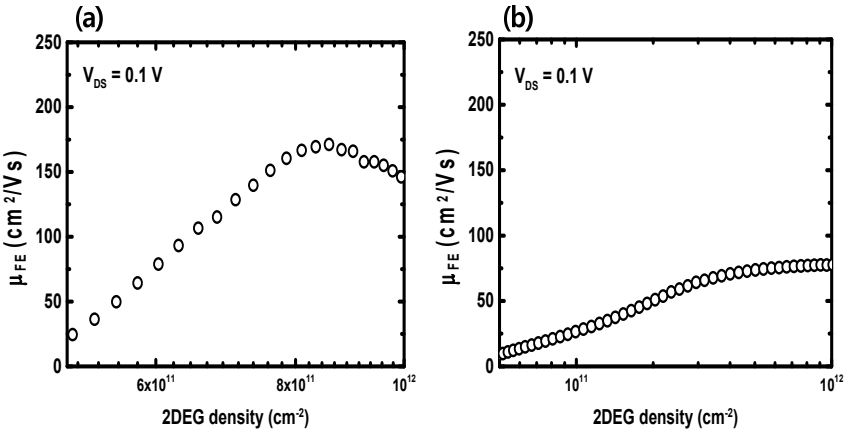


Fig 5.16 The field-effect mobility in the channel of a FAT-FET with 100 mm long gate width (a) partially receesed MIS-HEMT, (b) fully recessed MIS-HEMT

5.3.2 Plasma Enhanced ALD SiN_x Film

The quality of gate dielectric in MIS-HEMT brings substantial impact in E-mode power devices. The presence of a high density of positive fixed charge is one of main issues. The positive fixed charges at the interface of dielectric on GaN not only prevents normally off operation by causing negative voltage shift of the threshold voltage but also increases gate leakage current by increasing the electron tunneling probability [34, 41, 42]. A recessed gate process is commonly used to achieve normally-off operation. Then, the quality of the gate dielectric becomes the important factor. Atomic layer deposition (ALD) has been proven to be the superior technique for depositing highly conformal films with an excellent thickness control [43, 44]. Many groups has been used Al_2O_3 deposited by ALD as the gate dielectric in AlGaN/GaN MIS-HEMTs because of its high conduction-band offset, high dielectric constant, and high breakdown filed [45, 46]. On the other hand, silicon nitride has been a commonly used passivation film for suppressing the current collapse phenomena in GaN HEMTs due to its good interface properties. Plasma enhanced chemical vapor deposition (PECVD) which has highly conformal dielectric coatings with precise thickness control has been recently used [47]. In this study, we used a high-quality PEALD-SiN_x dielectric film deposition process using a conventional ICP-CVD system, which was applied in fabrication of normally-off recessed-gate AlGaN/GaN-on-Si MISHEMTs.

PEALD SiN_x was grown using conventional inductively-coupled plasma chemical vapor deposition (ICP-CVD) system with SiH_4 and N_2 as precursors for Si and N, respectively, where the first step was N_2 plasma treatment. Deposition conditions and resulting SiN_x film characteristics are summarized in Table 5.1 [48].

Table 5.1 Deposition conditions and properties of PEALD SiN_x film [48]

	PEALD deposition	
	N_2 plasma	SiH_4 adsorption
RF power (W)	600	0
Pressure (mTorr)	60	70
Gas Flow (sccm)	N_2/Ar (50/10)	SiH_4/N_2 (25/75)
Chuck temperature (℃)	400	400
Deposition rate	0.5 Å/cycle	
Refractive index at λ =632 nm	1.872	
Dielectric constant	7.07	
Breakdown field (MV/cm)	11.2	

5.4 Characterization for Normally-off GaN Transistors

In this chapter, we report the E-mode SiN_x/GaN MIS-HEMTs with a two-step Si_3N_4 process which features a thin layer of PEALD SiN_x under the gate and a thick layer of SiN_x in the access region. The fluoride plasma treatment technique as mentioned in section 4.4.2 is adapted to reduce the trapping phenomenon. The partial gate recess technique is used to convert the device from D-mode to E-mode.

5.4.1 DC Characteristics

The epitaxial layers used in this chapter is grown on silicon (111) substrate consisted of a 40 Å GaN capping layer, a 200 Å $Al_{0.24}GaN$ barrier layer, a 3.9 μm GaN carbon-doped buffer layer, and AlN/GaN transition layers from top to bottom. Sheet resistance of 454 Ω/sq and carrier mobility of 1800 $cm^2/V{\cdot}s$ were measured. The fabrication process is illustrated in Fig 5.4. A SiN_x pre-passivation layer was deposited at 350 °C using inductively coupled plasma chemical vapor deposition (ICP-CVD). The ohmic contacts were formed by using a Si/Ti/Al/Mo/Au (=5/20/60/35/50 nm) metal stack, followed by 800 °C for 30 sec in N_2 ambient. Device isolation was carried out by inductively coupled plasma (ICP) etching, utilizing BCl_3/Cl_2 gas. A new 2000 Å SiN_x passivation layer was subsequently re-deposited by ICP-CVD at 350°C. The AlGaN layer under the gate region was etched to remaining AlGaN barrier of 2 nm. Prior to gate dielectric deposition, the wafer was

cleaned using a sulfuric peroxide mixture, and diluted HF. A 6 nm SiN_x interfacial layer was deposited with plasma enhanced atomic layer deposition (PEALD) followed by in-situ 24 nm inductively coupled plasma-chemical vapor deposition (ICP-CVD) SiN_x deposition. Subsequently, RTA was carried out at 500 °C for 5 min in N_2 was performed to improve the quality of the SiN_x layer. Finally, Ni/Au gate metal and probing pad are formed by photolithography and E-beam evaporation after source/drain opening. As shown Fig 5.17, the source-to-gate distance, gate length, and gate-to-drain distance were 2, 2, and 3 μm, respectively. A 1 μm gate overhang region formed the field plate.

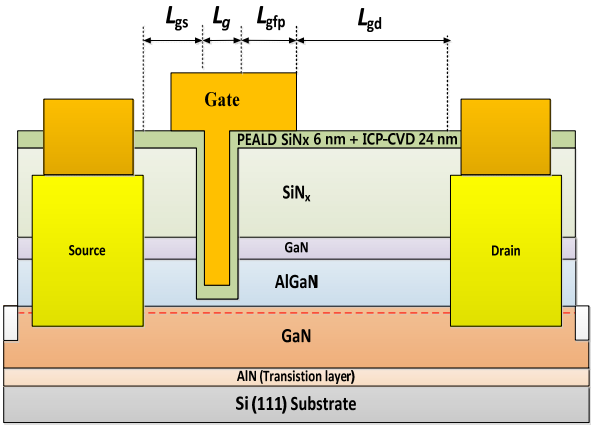


Fig 5.17 Schematic cross section of an E-mode SiN_x/GaN MIS-HEMTs

The DC output characteristics of the E-mode MIS-HEMTs are plotted in Fig 5.18. The devices exhibit a peak current density of 550 mA/mm and an on resistance of 0.45 mΩ·cm^2 (extracted around V_{DS} = 1 V) at V_{GS} = 9 V. It can be seen that the gate forward bias limit of AlGaN/GaN HEMTs has been improved from 1 V (conventional E-mode) to 9 V using metal-insulator-semiconductor structure. Fig 5.19 shows that gate leakage current of E-mode MIS-HEMTS is also plotted. It can be seen that the gate current remains as low as pA at forward bias 8 V. Fig 5.20 shows the transfer characteristics operated at V_{DS} = 10 V. The maximum transconductance was 110 mS/mm. The pinched-off voltage is 0.7 V from linear extrapolation of drain current.

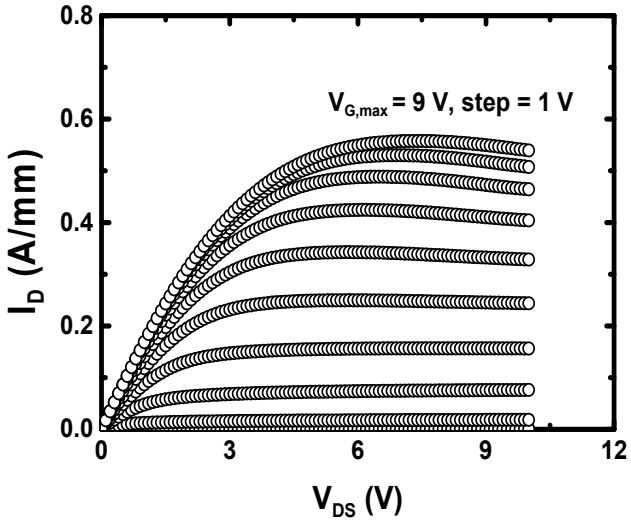


Fig 5.18 I_{DS}-V_{DS} characteristics of SiN_x/GaN MIS-HEMTs with 2 μm gate length and 100 μm gate width

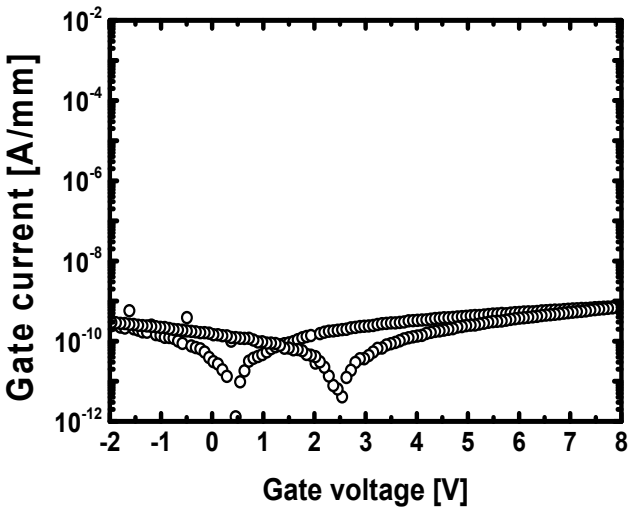


Fig 5.19 Gate leakage characteristics of SiN_x/GaN MIS-HEMTs

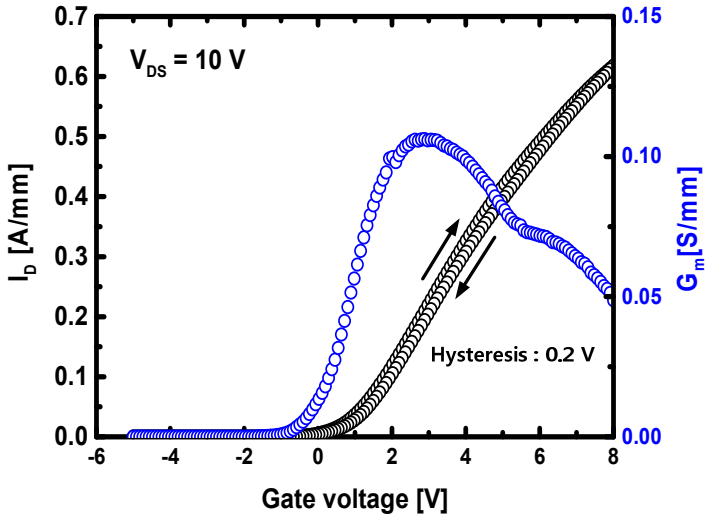


Fig 5.20 Transfer characteristics of SiN_x/GaN MIS-HEMTs in linear scale. The transfer curves are measured at V_D = 10 V

5.4.2 Breakdown Voltage Characteristics

The air which surrounds the fabricated device during the breakdown voltage measurements was suspected to be triggering the breakdown beyond a certain drain voltage. The test device was immersed in the inert liquid called Flourinert to withstand higher BV on drain side. The BV is defined as the V_{ds} at which an I_{ds} of 1 mA/mm was observed at a constant Vg = Vs = 0 V. The device with L_{gd} = 10 µm exhibited a high BV of 1.1 kV. The BV almost exhibits a linear increase with L_{gd} up to 10 µm with increasing specific on resistance.

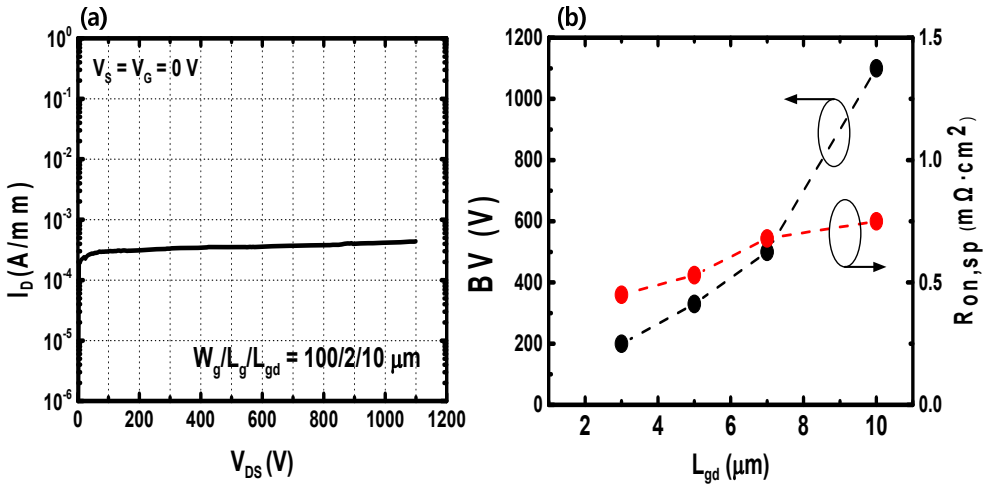


Fig 5.21 (a) Three terminal breakdown voltage characteristics of SiN_x/GaN MIS-HEMT (b) Breakdown voltage and specific on-resistance of SiN_x/GaN MIS-HEMT with increasing L_{gd} spacing

Fig. 5.22 shows the benchmark $R_{ON,sp}$ versus BV with previous reports based on various approaches of E-mode GaN power devices [3, 27, 49-57]. The specific on resistance $R_{on,sp}$ is as low as 0.75 mΩ·cm^2 for gate-drain separation (L_{gd}) of 10 μm. The area (A) considered whole active area. The off-state breakdown voltage is as high as 1100 V. Our result reflects the advantages of the unique combination of partial gate recess technique and the PEALD SiN_x gate dielectric layer.

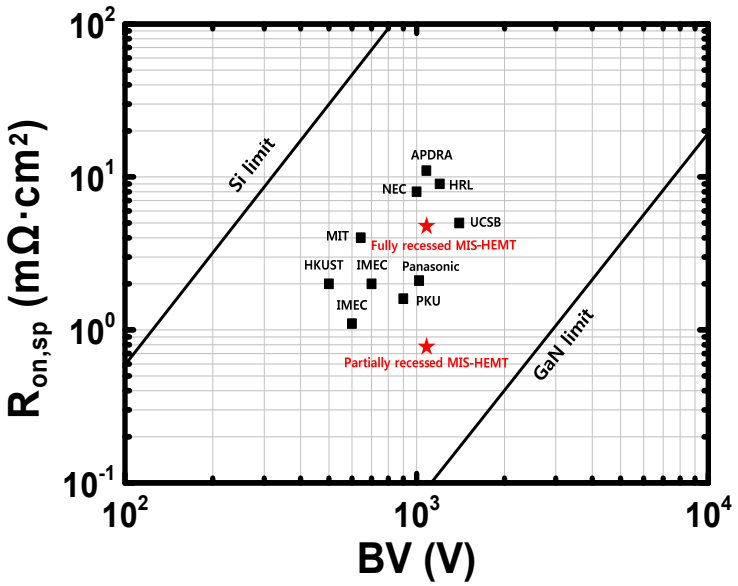


Fig 5.22 Benchmarking of breakdown voltage versus specific on-resistance of E-mode GaN transistors. Solid line represents the theoretical limits of Si and GaN

5.4.3 Dynamic R_{on} Characteristics

The control of the dynamic on-resistance is one of key issues for GaN-on-Si FETs power switching devices. The dynamic R_{on} was characterized by measuring the R_{on} after the device was switched from the OFF-state to the ON-state. A hard switching test configuration in on-wafer measurement was used as illustrated in Fig. 5.23. The switching frequency was 100 KHz with a 50 % duty cycle. The off-state V_{DD} stress bias started from 20V and was increased to 260 V by 20 V steps. The load resistor was adjusting to have same driving current at different V_{DD} values. The conventional device exhibits large increase in dynamic $R_{DS(on)}$ which implies a significant trapping phenomenon during the switching operation. Fig 5.24 shows that the conventional process sample had dynamic Ron degradation while the GaN FET with fluorine plasma treated had slightly degradation of dynamic R_{on} characteristics. It is clearly seen that the improved dynamic $R_{DS(on)}$ characteristics were achieved by fluorine plasma treatment process as discussed in section 4.4.2. The dynamic on-resistance ($R_{ds(on)}$) was increased by 1.2 times when V_{dd} was 200 V. Further optimization of the field plate improves the dynamic R_{on} characteristics.

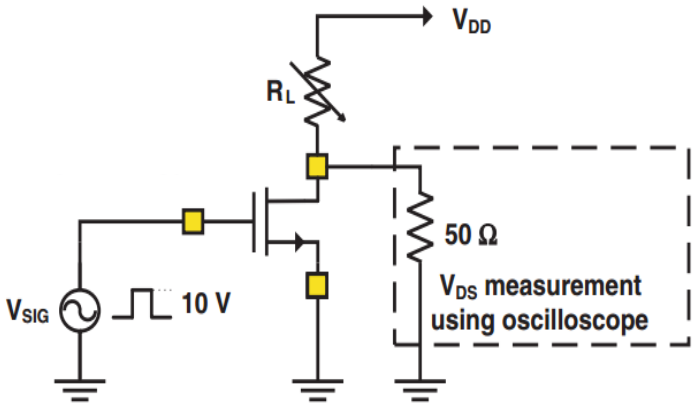


Fig 5.23 The schematic of hard switching test circuit in on-wafer measurement [58]

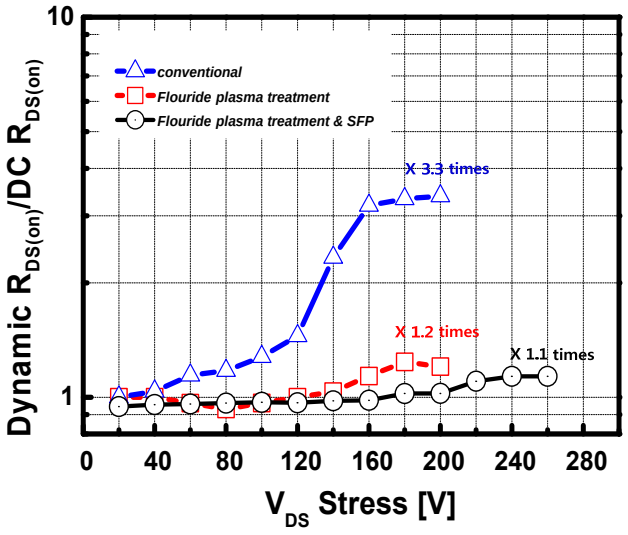


Fig 5.24 Process-dependent dynamic on-resistance characteristics of fabricated recessed MIS-HEMTs

5.5 Summary

In this chapter, the fabrication and characterization of the enhancement-mode MIS-HEMTs which employ PEALD SiN_x as a gate dielectric is demonstrated. The influence of impact access region in a device where the gate dielectric layer located at GaN channel with and without AlGaN barrier layer was studied. The developed gate ethcing process provides an opportunity to contol the thickness of AlGaN barrier prior to the formation of Si_3N_4 layer. Maximum drain current and on-resistacnce comparisons between recessed MIS-HEMTs with thin AlGaN barrier and without were given. The results indictated that the thin AlGaN barrier layer helped to improve the maximum drain current and reducing transconductance degradation. The improvement can be attributed to lower plasma induced damage and reducing scattering effect.The fabricated device exhibit a peak current density of 550 mA/mm and an on resistance of 0.45 $m\Omega \cdot cm^2$ (extracted around V_{DS} = 1 V) at V_{GS} = 9 V. The off-state breakdown voltage is as high as 1100 V.

5.6 Reference

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Chapter 6

Conclusions and Future Works

The overwhelming focus of this work was to create AlGaN/GaN HEMTs which could gain the maximum potential through the straight forward fabrication. It is important to get closer to theoretical value because GaN based devices has been attractive in high power/frequency electronic applications. This work can be divided into two parts, namely D-mode AlGaN/GaN schottky HEMTs on silicon substrate for high power devices in X-band operation and E-mode Si_3N_4/AlGaN/GaN metal-insulator-semiconductor heterostructure field-effect transistors (MIS-HEMTs) for power switching devices.

Initial efforts were aimed at reducing trapping phenomenon which related to reducing the output power from its expected value. SF_6 plasma treatment processes have been optimized to reduce trapping phenomenon which originated from the surface. In order to investigate the influence of SF_6 plasma treatment in the trapping of charges in HEMT devices, current collapse measurement were carried out. It is

evident that the current showed a large decrease, as well as knee voltage walk-out for the untreated device whereas minor degree of collapse was observed for treated sample. It is clear that the most common approaches to engineering electric field distribution are to employ filed plate structure. It was found that the proposed process in conjunction with a field plate structure was a very effective way to reduce the trapping problem. Take advantage of this technology, the two-gate-finger HEMTs demonstrated significant improvement in the output power density and power added efficiency. The fabricated device shows power density of 6.32 W/mm, PAE of 54 % and drain efficiency of 67.9 %. The high linear gain of 13 dB is substantial compared to all other AlGaN/GaN HEMT's on silicon substrate reported at X-band. The large-periphery HEMT with a total gate width of 2.4 mm exhibits the saturated power level was 37.4 dBm (5.5 W), the power added efficiency (PAE) was 33.6 %, and the linear power gain was 9.4 dB. The output performances of larger periphery device on silicon substrate are limited by thermal effects. To solve the thermal issues, a novel backend processing was proposed.

The individual through substrate source via (ISV) configuration was proposed to reduce the parasitic source inductance of large gate periphery device and allows use of a larger size cell to realize compact chips. To utilize the individually grounded source finger vias, source via profile should be change vertical profile to taper shape. The tapered silicon via etch process consists of two silicon etching steps. The 1st etching step is a high etch-rate silicon etching process is performed deep silicon vias

of required depth followed by photoresist stripping by oxygen plasma. The 2nd etching step is designed to control the taper angle of the via through the global isotropic etch. To examine the profile of the etched vias, visualization of the via profiles using scanning electron microscopy (SEM) is used. The tapered via etching process has been developed for achieving good sidewall coverage for gold seed metal layer. Optimized backend process would improve overall device performance by reducing thermal effect. Based upon it, GaN HEMT amplifier with single chip of 3.6 mm gate periphery has been successfully developed. It exhibits very high power density of 8.1 W/mm with 29.4 W output power under V_{DS} = 38 V pulse operating condition.

At last, Enhancement mode (E-mode) device is developed based on partially recess gate etching technique. It is difficult to obtain E-mode operation with a low on-resistance and a high breakdown voltage. To reduce the on resistance and enhance the drain current density, partially recessed MIS-HEMTs are investigated. The low damage gate recess process is developed to reduce the plasma etching-induced damage. To examine the plasma induced damage, XPS analysis was performed. It shows that no noticeable difference between as-grown GaN surface and etched GaN surface. The surface morphology of unetched GaN surface and etched layer was examined by atomic force microscopy (AFM). The unetched surface has an average root mean square roughness of 30 Å, while the etched surface has almost same value of it. It is suggested that there is no additional damage by etching process. The gate

recess was carried out using a low-damage Cl_2/BCl_3-based RIE where the target etch depth was remains AlGaN barrier layer in order to improve the transfer characteristics.

The occurring degradation of the mobility due to plasma etching-induced damage and scattering effect were effectively removed by partial gate recess technique. Completely recessing the AlGaN barrier layer reduces the carrier concentration under the gate region result in have much lower mobility due to the plasma induced damage. Moreover, scattering effect may impact access region in a device where the gate dielectric layer located at GaN channel without AlGaN barrier layer.

Appendix A

Fabrication Process of AlGaN/GaN HEMT

1. **Si_3N_4 pre-passivation**
    a. Acetone ultrasonic clean, 10 minutes
    b. IPA ultrasonic clean, 10 minutes
    c. D.I water rinse, 5 minutes
    d. Blow dry with N_2 gun
    e. Dip in SPM for 10 minutes at 120 °C
    f. D.I water rinse, 20 minutes
    g. Dip in SPM for Diluted HF (1:10) for 15 minutes
    h. D.I water rinse, 1 minutes
    i. The 1st Si_3N_4 Deposition
        - $SiH_4/N_2/Ar$: 2.8/9/90 sccm, 35 mTorr, 200 W, 350 °C

2. **Mesa Isolation**
    a. Acetone ultrasonic clean, 10 minutes
    b. IPA ultrasonic clean, 10 minutes
    c. Dehydration bake, 150 °C, 10 minutes on hot plate
    d. Apply AZ 5214, spin at 4000 rpm for 40 seconds
    e. Soft bake, 90 °C for 2 minute on hot plate
    f. Expose for 4.5 seconds
    g. Develop in AZ300 for 40 seconds
    h. Oxygen plasma Descum

i. Si_3N_4 etch

- SF_6: 30 sccm, 100 mTorr, 20 W

j. GaN etch

- BCl_3/Cl_2: 2/18 sccm, 5 mTorr, 350/10 W

k. Solvent cleaning to remove residue photoresist

3. Ohmic formation

a. Acetone ultrasonic clean, 10 minutes

b. IPA ultrasonic clean, 10 minutes

c. Dehydration bake, 120 °C, 10 minutes on hot plate

d. Apply AZ 5214, spin at 4000 rpm for 40 seconds

e. Soft bake, 95 °C for 1 minute on hot plate

f. Expose for 4.5 seconds

g. Hard bake, 115 °C for 2 minute on hot plate

h. Develop in AZ300 (6:1) for 40 seconds

i. Oxygen plasma Descum

j. Si_3N_4 etch

- SF_6: 30 sccm, 100 mTorr, 10 W

k. Recess etching

- BCl_3/Cl_2: 2/18 sccm, 5 mTorr, 200/3 W

l. Dip in HCl (1:3) for 1 minutes

m. D.I water rinse, 1 minutes

n. Deposit multiple metal layers :

Material	Thickness	Deposition Rate
Si	50 Å	0.8 Å/sec
Ti	200 Å	1Å/sec
Al	800 Å	1.5 Å/sec
Mo	350 Å	1 Å/sec
Au	500 Å	3 Å/sec

o. Soak wafer in Acetone until metal becomes loos and falls off

p. Annealing

- Anneal the wafer at 780 °C for 1 minutes

4. E-beam marker

a. Acetone ultrasonic clean, 10 minutes

b. IPA ultrasonic clean, 10 minutes

c. Dehydration bake, 120 °C, 10 minutes on hot plate

d. Apply PMGI, spin at 4000 rpm for 40 seconds

e. Soft bake, 160 °C for 5 minute on hot plate

f. Apply ZEP(1:1), spin at 2500 rpm for 40 seconds

g. Soft bake, 160 °C for 5 minute on hot plate

h. Electro-beam exposure

- Dose : 120 uC/cm^2 , step : 16 nm

i. Develop in MEK:MIBK (2:3) for 120 seconds

j. IPA rinse, 30 seconds

k. Develop in AZ300 for 45 seconds

l. Oxygen plasma Descum

m. Deposit Ti/Pt metal layers

n. Soak wafer in remove PG until metal becomes loose and falls off

o. Rinse with Acetone/IPA

p. Blow dry with N_2 gun

5. Gate foot formation

a. Acetone ultrasonic clean, 10 minutes

b. IPA ultrasonic clean, 10 minutes

c. Dehydration bake, 120 °C, 10 minutes on hot plate

d. Apply ZEP(1:1), spin at 2500 rpm for 40 seconds

e. Soft bake, 160 °C for 5 minute on hot plate

f. Electro-beam exposure

- Dose : 1000 uC/cm^2 , step : 16 nm

g. Develop in MEK:MIBK (1:1) for 90 seconds

h. IPA rinse, 30 seconds

i. Si_3N_4 etch

- SF_6: 30 sccm, 100 mTorr, 10 W

j. Solvent cleaning to remove residue photoresist

6. Gate metallization

a. Acetone clean, 10 minutes

b. IPA clean, 10 minutes

c. Dehydration bake, 120 °C, 10 minutes on hot plate

d. Apply PMGI, spin at 4000 rpm for 40 seconds

e. Soft bake, 160 °C for 5 minute on hot plate

f. Apply ZEP(1:1), spin at 2500 rpm for 40 seconds

g. Soft bake, 160 °C for 5 minute on hot plate

h. E-beam lithography

- Dose : 120 uC/cm^2 , step : 16 nm

i. Develop in MEK:MIBK (2:3) for 90 seconds

j. IPA rinse, 20 seconds

k. Develop in AZ300 for 45 seconds

l. Oxygen plasma Descum

m. Deposit metal Ni/Au of 40/360 nm

n. Soak wafer in remove PG until metal becomes loose and falls off

o. Rinse with Acetone/IPA

p. Blow dry with N_2 gun

7. Pad Contacts

a. Acetone ultrasonic clean, 10 minutes

b. IPA ultrasonic clean, 10 minutes

c. Dehydration bake, 120 °C, 10 minutes on hot plate

d. Apply AZ 5214, spin at 4000 rpm for 40 seconds

e. Soft bake, 95 °C for 1 minute on hot plate

f. Expose for 4.5 seconds

g. Hard bake, 115 °C for 2 minute on hot plate

h. Develop in AZ300 (6:1) for 40 seconds

i. Oxygen plasma Descum

j. Deposit metal Ni/Au of 40/360 nm

k. Lift off in Acetone

l. Rinse with Acetone/IPA

8. Air-bridge technology (copolymer)

a. Cleaning in Acetone and IPA, blow with dry N_2

b. Dehydration bake, 120 °C, 10 minutes on hot plate

c. Apply 1st Copolymer (MMA), spin at 1500 rpm for 80 seconds

d. Soft bake, 150 °C for 90 seconds on hot plate

e. Apply 2nd Copolymer (MMA), spin at 1500 rpm for 80 seconds

f. Soft bake, 150 °C for 90 seconds on hot plate

g. Apply 3rd Copolymer (MMA), spin at 1500 rpm for 80 seconds

h. Soft bake, 150 °C for 90 seconds on hot plate

i. Apply AZ 4330, spin at 3000 rpm for 40 seconds

j. Soft bake, 95 °C for 90 seconds on hot plate

k. Expose for 15 seconds

l. Develop in AZ300 for 100 seconds

m. Copolymer etching

   - O_2: 50 sccm, 100 mTorr, 100 W

n. Hard bake, 70 °C for 3 minutes on hot plate

o. Solvent cleaning to remove residue photoresist

p. Copolymer flowing, 225 °C for 4 minutes in the oven

q. Apply AZ 4620, spin at 3000 rpm for 60 seconds

r. Soft bake, 100 °C for 500 seconds on hot plate

s. Expose for 50 seconds

t. Develop in AZ300 for 3 minutes

u. Seed metal sputtering Ti/Au of 50/200 nm

v. Au plating of 4 μm

w. Seed metal etching

Appendix B

Fabrication Process of AlGaN/GaN MIS-HEMT

1. **Si_3N_4 pre-passivation**
2. **Mesa Isolation**
3. **Ohmic formation**
4. **E-mode Gate Electrodes Definition**
   a. Solvent cleaning
   b. SF_6 Plasma Used to Etch Si_3N_4 and Treat GaN surface
   c. Thick Si_3N_4 layer deposition
   d. Photoresist coating
   e. Photoresist Exposure and Development
   f. Oxygen Plasma Descum
   g. Si_3N_4 Layer etching by SF_6 plasma
   h. Solvent Cleaning to remove residue photoresist
   i. Acid treatment
      - Dip in SPM for 15 minutes at 60 °C
      - D.I water rinse, 20 minutes
   j. Gate recess etching
   k. Gate insulator deposition

l. Source/drain window open

m. Photoresist coating

n. Photoresist Exposure and Development

o. Oxygen Plasma Descum

p. Deposit metal Ni/Au of 40/200 nm

q. Lift off in Acetone

r. Rinse with Acetone/IPA

5. Air-bridge technology (BCB)

a. Cleaning in Acetone and IPA, blow with dry N_2

b. Dehydration bake, 120 °C, 10 minutes on hot plate

c. Si_3N_4 film deposition for adhesion

d. Apply BCB63, spin at 5000 rpm for 90 seconds

e. Post bake, 120 °C for 90 seconds on hot plate

f. Curing, 250 °C for 60 minutes in the BCB oven

g. Si_3N_4 film deposition for adhesion

h. Apply AZ 4620, spin at 2000 rpm for 60 seconds

i. Soft bake, 100 °C for 2 minutes on hot plate

j. Expose for 50 seconds

k. Develop in AZ300 for 3 minutes

l. BCB etching

m. Solvent (EKC) cleaning to remove residue photoresist

n. Seed metal sputtering Cr/Au of 20/200 nm

o. Apply AZ 4620, spin at 2000 rpm for 60 seconds

p. Soft bake, 100 °C for 10 minutes on hot plate

q. Expose for 50 seconds

r. Develop in AZ300 for 3 minutes

s. Au plating of 10 μm

t. Seed metal etching

초 록

최근, 여러 가지 화합물 반도체 물질 중에서 고항복전계, 고전류밀도, 고전자이동도의 고유 물질적 특성을 갖는 aluminum gallium nitride (AlGaN)/gallium nitride (GaN) 이종접합구조 기반의 소자가 활발하게 연구가 진행되고 있다. 이런 특성들은 고전력, 고주파 특성을 가지는 RF 소자뿐만 아니라 전력 반도체로 적합하다고 할 수 있다. 하지만, 우수한 물질적 특성에도 불구하고 소자 제작 공정에 따른 전기적 특성 저하를 개선시키기 위한 노력이 필요하다. 본 논문에서는 X-band에서 동작하는 우수한 성능의 RF 소자 및 전력 반도체 소자의 특성을 개선 시키기 위한 공정 기반의 연구를 진행하였다. 일반적으로 RF용 전력반도체의 경우 대부분 열적 특성이 우수한 SiC 기판의 연구를 진행하고 있다. 하지만, 높은 가격과 기존의 실리콘 기반의 반도체 공정 설비와의 호환성 등을 고려할 경우 실리콘 기판에서 성장한 GaN 소자의 연구의 중요성이 매우 높다.

먼저, RF 소자의 전력 특성을 저하의 주요 원인이 되는 표면 트랩을 억제하기 위한 연구로 플라즈마 처리를 이용한 공정 기법을 제안하였다. 가스 유량, 압력, 그리고 처리 시간 등에 따른 조건을 최적화함으로써 전하

트랩핑 현상을 최소화 하였다. 이를 분석하기 위해 펄스를 이용한 측정과 노이즈 특성을 통해 개선점을 찾을 수 있었다. 뿐만 아니라, 소스 필드 플레이트 구조 및 slant 구조의 게이트를 형성함으로써 우수한 RF 특성을 얻을 수 있었다. 개선된 제작 공정을 통해 실리콘 기판에 제작된 소자에서는 9.3 GHz의 동작주파수에서 6.32 W/mm 의 전력 밀도와 54.5 % 효율을 얻을 수 있었다. 하지만, 높은 전력을 얻기 위하여 대 면적 소자를 적용할 경우 1.2 mm 소자의 경우 6.32 W/mm 의 전력 밀도를 가지고 2.4 mm 소자의 경우 2.3 W/mm 의 전력 밀도 특성을 보여준다. 이는 기존의 전하 트랩핑 현상에 따른 효과가 아닌 소자의 열화를 방지하기 위한 추가적인 공정이 필요한 것으로 생각된다.

특히, 출력 파워를 증가시키기 위해 대면적 소자를 제작할 경우에는 소자 동작 시 발생하는 열을 효과적으로 분산시키고 패키징시 발생하는 추가적인 소스 인덕턱스를 줄이는 것이 중요하다. 상대적으로 열전도도가 나쁜 실리콘 기판에서 특성을 개선시키기 위하여 개별 비아 홀 구조를 적용하였다. 일반적으로 여러 개의 소스 단을 한곳으로 묶어서 소스 패드에 비아 홀 구조를 적용하는 것이 아니라 각각의 소스 메탈에 직접 비아 홀을 적용하는 구조를 적용하였다. 이를 위해 Taper 형태의 소스 비아 홀 공정을 개발하였다. 소자의 높은 주파수 특성을 유지하면서 비아 홀 공정을 적용

하기 위하여 two-step 에칭 프로세스를 개발하여 소자에 적용하였다. 각각의 소스 메탈에 직접 비아 홀을 적용함으로써 소자 동작 시 발생하는 열을 효과적으로 줄일 수 있을 뿐 아니라 추가적으로 생기는 소스 인덕턴스를 줄일 수 있었다. 또한, 개별 비아 홀 공정은 소스 메탈을 연결 시키기 위한 에어브릿지 공정을 사용하지 않게 되어 소자의 안정도 특성에도 개선을 가져올 수 있다. 개발된 백사이드 공정을 적용하여 제작된 3.6 mm 소자의 경우 8 GHz의 동작주파수에서 8.31 W/mm 의 전력 밀도와 29.4 W 의 최대 전력을 얻을 수 있었다. 이는 기존의 제작 공정을 통해 제작된 소자 대비 300 % 이상의 출력 밀도의 증가를 얻은 것이다. 이를 통하여 소자 크기 증가에 따른 발열 문제와 트랩 효과가 소자의 특성을 제한하는 것임을 분석하였다.

일반적으로 제작한 GaN 소자의 경우 depletion-mode 로 동작하지만, 전력 반도체로 안정적으로 사용하기 위해서는 Enhancement-mode 동작이 요구된다. E-mode 동작을 구현하기 위해 다양한 방법들이 연구되고 있고 그 중에서도 recessed MIS 구조가 가장 많이 사용되는 구조이다. 하지만, 게이트 영역 에칭 시 발생하는 데미지와 절연 막과 에피 사이에 존재하는 트랩핑 현상은 여전히 해결되어야 될 문제점으로 남아있다. 특히, 낮은 온 저항과 높은 전류 밀도를 얻기 위해서는 매우 중요하다.

이를 해결하기 위한 AlGaN barrier를 부분적으로 남기는 식각 공정을 이용한 recessed-MIS 구조를 제안하였다. 게이트 영역 식각 시 발생하는 데미지를 최소화 하기 위하여 식각 조건을 최적화 하였으며, XPS 분석을 통해 그 결과를 확인하였다. 분석 결과 Ga, N peak 값이 식각 전 후에 차이가 없는 것을 확인 할 수 있었다. 또한, 에칭 전후에 AFM 측정을 통하여 표면의 roughness 가 변화되지 않는 것을 확인할 수 있었다. 이를 통해 개발된 식각공정에서 추가적인 데미지가 발생하지 않는 것을 확인하였다. 이런 개선된 식각 공정을 이용하여 제작된 소자의 경우 4.15 $m\Omega \cdot cm^2$ 의 높은 온 저항과 250 mA/mm 의 낮은 전력 밀도 특성을 보여주었다. 반대로, AlGaN barrier를 부분적으로 남기는 식각 공정을 이용한 소자의 경우 0.45 $m\Omega \cdot cm^2$ 의 낮은 온 저항과 600 mA/mm 의 높은 전력 밀도 특성을 보였다. 이런 특성을 분석하기 위하여 주파수에 따른 C-V 특성 및 FAT-FET 구조를 이용한 mobility를 분석하였다. AlGaN barrier를 모두 식각한 구조에서는 frequency-dispersion 이 상대적으로 심하게 발생하였으며, 계면전하밀도를 추출한 결과 개발된 구조에서 보다 $2.27x10^{12}\ cm^{-2}$ 높은 값을 가지는 것을 확인 할 수 있었다. 이를 통해 낮은 전력밀도를 가지는 것을 확인할 수 있었다. 전류 이동도 특성에서도 약 2.5 배 낮은 값을 가지는 것을 확인하였다. 최종적으로 제작된 소자는

0.75 mΩ · ㎠ 의 낮은 온 저항과 1000 V 이상의 항복전압 특성을 보여 주었다.

주요어: AlGaN/GaN 이종접합, 전력 밀도, X-band, 증폭기, 개별 소스 비아 홀 (ISV), 플라즈마 표면처리, 전력소자, 온-저항, 항복 전압, 실리콘 질화막 (SiN_x)

학 번 : 2011-30970

Research Achievements

- International Journals

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[2] **Min-Seong Lee**, Il-Hwan Hwang, Woojin Choi, Ho-Young Cha and Kwang-Seok Seo, “Effect of fabrication process on dynamic resistance of SiN_x/GaN MIS-HEMTs,” Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD), Jeju, Korea, June 29-July 1, 2015.

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Patents

[1] Republic of Korea

"Forming method for passivation film and manufacturing method for AlGaN/GaN HFET including the forming method"

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(Application) 10-2013-0094477, 2013, (Registration) 10-1455283, 2014

Awards and Honors

[1] The 4th Conference on Korea Society of Optoelectronics – Best poster, 2014.