Ph.D. DISSERTATION

Nano-structured RRAM for Ultra High Density and Low Power RRAM

초고집적 및 저전력 동작을 위한
나노 구조의 저항변화 메모리

BY

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이 논문을 공학박사 학위논문으로 제출함

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2016 년 2 월

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ABSTRACT

The IT industry has grown explosively since the emergence of a variety of mobile devices that make us handle information anytime and anywhere. The demand of large-capacity information storage device has increased with this trend. Currently, the development of the three-dimensional stacked NAND flash memory is nestled into the mainstream of a large-capacity memory. On the other hand, in order to achieve excellent memory performance of much faster, less power consumption, and higher density, the research of new memories are being actively conducted as an alternative to the NAND flash memory. Among these m emories, RRAM has attracted much attention as one of the most promising candidates that may replace the conventional memory due to its simple stru cture, good scalability, high-speed operation, and low energy consumption. In spite of the above-mentioned advantages, RRAM suffers from high reset current, poor reliability such as large variation in set/reset voltages and LRS/HRS resistances. It is struggling to be commercialized. In this thesis, a study was

carried out to solve the problems through a structural change of RRAM.

In the introduction, the basic structure and operation principle of RRAM is described. Especially, advantage of nitride-based RRAM with Si bottom electrode is also described. And, the methods to solve the issues of RRAM are introduced. Searching for the optimal combination of material and applying additional treatment to the device can improve the memory characteristics. Structural approach to improve performance can be a method for fundamentally to solve the problem fundamentally.

First, the basic bipolar resistive switching characterstics and the conduction mechanism are analyzed in large size cell of silicon nitride-based RRAM with Si bottom electrode.

Then, the cross-point array of the RRAM that is based on these materials is demostrated for the first time. In the fabricated cross-point RRAM cell, analysis of active area scaling effect is performed. It is found that the switching voltage increases with the scaling down of the active area.

In order to reduce the switching voltage and improve the memory performance, a new device structure having a nano-cone shaped silicon is proposed and is applied to the cross-point array of RRAM for the first time. By using simulation tool, it is verified that the electric field concentration effect occurs at the sharp point of nano-cone and the electric field is concentrated locally. These results imply that the position occuring resistive switching phenomenon is confined at the end of nano-cone and reduced switching voltage and uniform switching behavior can be achieved.

Finally, the feasibility of low power operation in the proposed device is successfully verified by the fabrication and the measurement.

Keywords: RRAM, Si_3N_4, Si, cross-point RRAM, nano-cone, electric field concentration effect

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Chapter 1

Introduction

1.1 IT and Memory Industry

The technological challenges for the future IT industry evolution are Internet of Things (IoT), cloud computing, and big data. In these technologies, dealing with a lot of information and storing very large amounts of data are important. Figure 1.1 shows that the amount of global digital information doubles every two years and is expected to reach 40 zeta bytes in 2020, which means approximately 5.3 terabytes of data per capita [1].

In an ideal computer there would only be one memory that is the main memory. That memory would be instantaneously accessible, allow permanent storage, require minimal energy, and be compact and cheap. Unfortunately, there is no technology that offers all those features. Because there is no ideal memory, real world constraints force computer engineers to use multiple different technologies, using each for the kind of thing it is best suited for. These different technologies form the memory hierarchy that is a series of layers from small and

fast to large and slow.

Figure 1.2 shows the memory hierarchy. The hierarchy of memory comprises three major layers: SRAM is used for on-chip cache memory. DRAM is used for main memory and mass storage is provided by flash and hard disk drives.

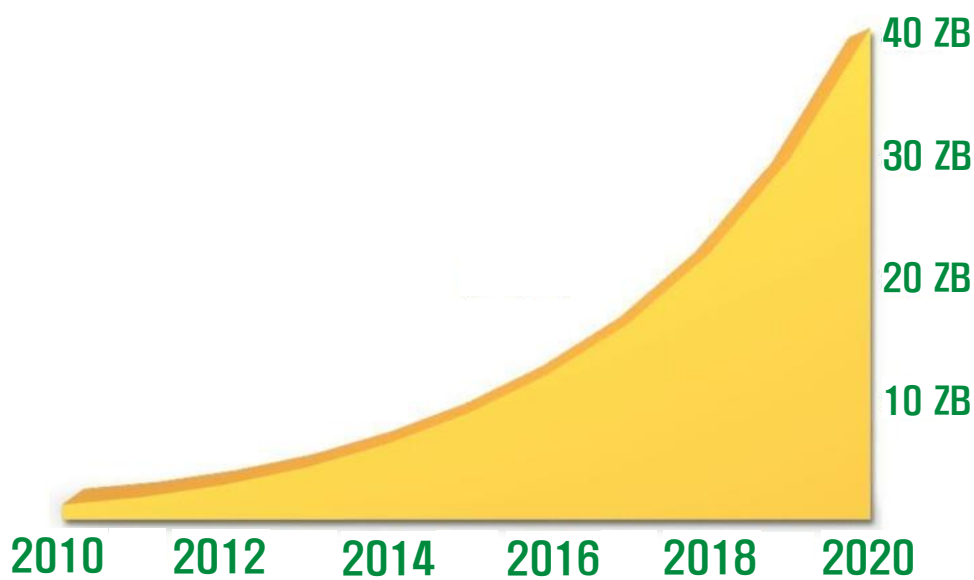


Fig. 1.1 Amount of digital information on the globe [1].

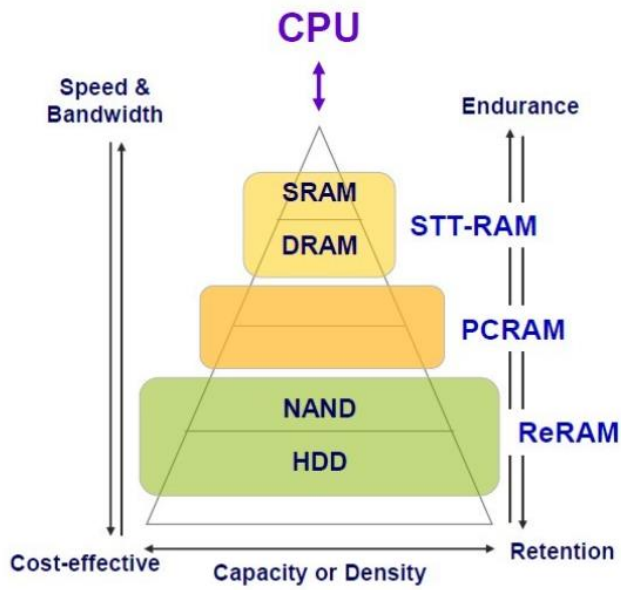


Fig. 1.2 Memory hierarchy in a computer system.

Table 1.1 shows comparison of access time between strorage types [2]. Accessing data in SSD and HDD are much slower than that of RAM and cache. The computer's performance is affected by this memory bottleneck. The movement of data between the CPU and the memory slows down. The increased processing times, in turn, lead to slow computer operations. Therefore, the memory speed has to be fast so as to facilitate efficient data processing.

Table 1.1 Comparison of access time between storage types.

Storage type	Access time	Relative access time
L1 cache	0.5 ns	Blink of an eye
L2 cache	7 ns	4 seconds
1MB from RAM	0.25 ms	5 days
1MB from SSD	1 ms	23 days
HDD seek	10 ms	231 days
1MB from HDD	20 ms	1.25 years

On the other hand, due to the explosive growth of the mobile market over the past five years, the demand for more memory capacity is inevitably ongoing task. Until recently, charge-based memory technologies such as flash memory and dynamic random access memory (DRAM) have dominated the memory market. Even though they have suffered from the difficulty in further scaling, sustainable development will be expected thanks to 3D integration and multi-level-cell (MLC) [3-5].

1.2 RRAM Technology

1.2.1 Evolution of RRAM Technology

In the last decade, emerging non-volatile memory devices such as Phase Change RAM (PCRAM), Magnetic RAM (MRAM), and Resistive RAM (RRAM) have been intensively explored as potential replacements for current memory technologies. Among these memories, RRAM has attracted much attention as one of the most promising candidates that may replace the conventional memory due to its simple structure, good scalability, high-speed operation, and low energy consumption [6-8]. Figure 1.3 shows the storage capacity and switching speed of RRAM among the conventional and new memories. The storage capacity of RRAM is chasing that of NAND flash memroy with frightening speed and the switching speed of RRAM is quite close to the level of DRAM.

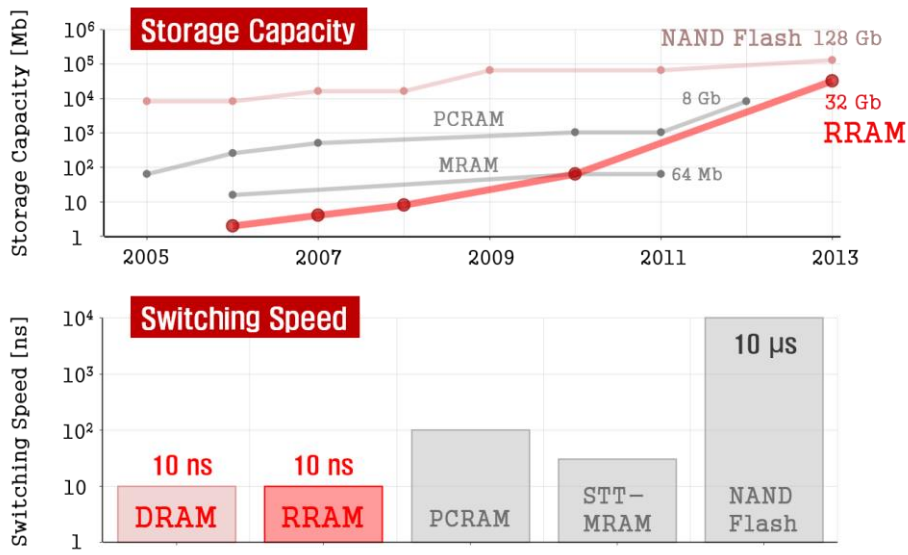


Fig. 1.3 Storage capacity and switching speed of RRAM among the conventional and new memories.

1.2.2 Basic Operation of RRAM

As shown in Fig. 1.4, RRAM consists of a simple metal-insulator-metal (MIM) structure. Although transition metal oxides such as TaO_2, HfO_2, etc. are widely used as resistive switching material of RRAM stack, optimized RRAM stack is still debatable due to uniformity problem. It is because conduction and resistive switching mechanisms is unclear [9, 10]. In order to improve the memory performance, the understanding of switching and conduction properties is essential.

Figure 1.5 illustrates the basic operation of RRAM. By applying an appropriate voltage across the electrodes, the resistive switching layer can be switched between a high-resistance state (HRS) and a low-resistance state (LRS). These two states can represent the logic values 1 and 0, respectively. As fabricated, the RRAM device has a pristine state, in which the resistance is usually very high. First, a forming voltage is applied to the switching layer, bringing it into LRS (the forming process). In order to avoid a permanent breakdown of the device, the

compliance current is usually limited. Then, reversible resistive switching occurs repeatedly while the device switches from LRS to HRS (the reset process) and HRS to LRS (the set process). The formation and rupture of a conducting filament is propsed to explain the resistive switching mechanism.

The resistive switching behavior of the RRAM device is classified as unipolar (nonpolar) and bipolar [11]. For unipolar (nonpolar) switching, resistive switching is independent of the polarity of voltage and is induced by the magnitude of voltage (Fig. 1.6(a)). For bipolar switching, one polarity is used to switch from HRS to LRS, and the opposite polarity is used to switch back into HRS in Fig. 1.6(b).

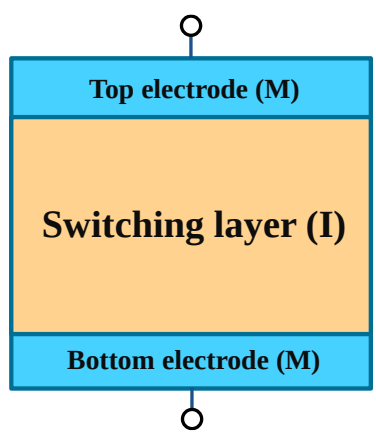


Fig. 1.4 Basic RRAM cell structure consisting of metal-insulator-metal (MIM).

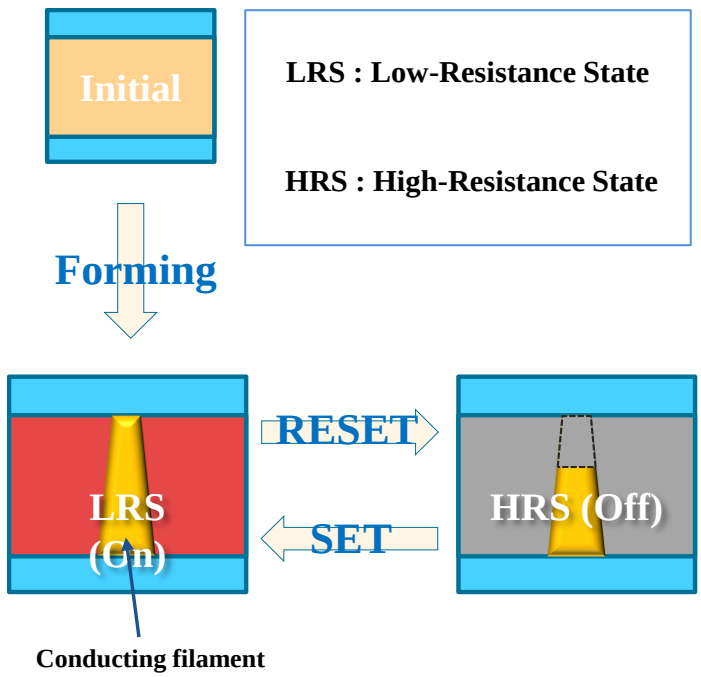


Fig. 1.5 Basic operation of RRAM: forming, reset, and set.

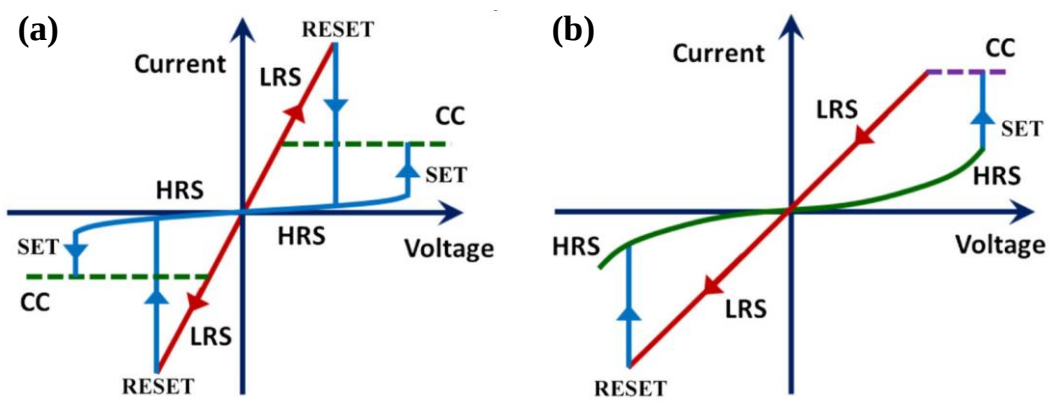


Fig. 1.6 Switching modes of the RRAM devices: *I-V* curves for (a) unipolar (nonpolar) and (b) bipolar resistive switching characteristics [11].

1.2.3 Challenges and Opportunities of RRAM

In spite of feasibility studies showing superior characteristics of RRAM such as simple structure, good scalability, strong endurance, high-speed operation, and low energy consumption, the issues to be solved for commercializion of RRAM still remain.

Poor yield and reproducibility are critical issues. Due to randomness of resistive switching behavior and overshoot current, variation of LRS/HRS resistance values exists even under the same switching voltage and compliance current [12, 13]. It causes uniformity and endurance problems. In addition, an unintended sneak current through other cells in cross-point array causes a misreading [14]. It limits the size of a cross-point array and leads to increased power consumption.

In recent years, many researches have been carried out to address these problems. In terms of material engineering, multi-layer structure is proposed to improve the performance [15, 16]. By inserting the AlO barrier layer, excellent memory performances are demonstrated. Reset current is reduced and on/off ratio is increased. Also, thin Ti

layer as the reactive buffer layer plays a role of oxygen gettering layer. Large amount of oxygen atoms diffuse from HfO_2 layer to the Ti overlayer, resulting in the formation of HfO_x/TiO_x bilayer. As a results, low reset current, high of/off ratio, fast switching speed, strong endurance, and reliable data retention are demonstrated.

Resistive switching characteristics can be improved using additional treatment and process [17-19]. N_2 RTA treatment induces more crystalline phases in ZnO film and rearranges and/or recover the oxygen vacancies. It is beneficial for the resistance switching. In addition, ozone treatment significantly improves the resistive switching uniformity of $HfAlO_2$ based RRAM. It is related to the changes in compositional and structural properties of the $HfAlO_2$ film. Also, implantation of Ti ions into ZrO_2 can improve the switching behavior. The doped Ti impurites not only provide oxygen vacancies but may also the role of a seed for forming conducting filaments.

Modifying the structure of RRAM device is the other approach [20-21]. By reducing the contact area at switching material and top electrode interface, irregular switching can be decreased significantly. It reveals that controlling the amount of conducting filament branch is necessary to achieve the stable resistive switching. By adopting the structure

with electric field enhancement effect, forming voltage can be reduced. Reduced forming voltage leads to reduction of the operating current, which in turn brings the low power operation. For next generation high density nonvolatile memory application, 3D stacked RRAM architecture and multi-level cell operation are inevitable [22].

For high densty RRAM with excellent resistive switching characteristics, it is important to combine the mateiral engineering, process optimization and structural approach in an RRAM cell.

1.3 Nitride –based RRAM with Si Bottom Electrode

Among the materials that exhibit a resistive switching behavior, the RRAM devices using transition metal oxides (TMOs) as a resistive switching material have been mainly reported. In TMO-based RRAMs, the movement of oxygen vacancy plays a crucial role in resistive switching. Although many studies that control the oxygen vacancy have been conducted, the optimum material combination is still debatable.

Recently, nitride-based RRAM devices have been extensively reported owing to their excellent compatibility to complementary metal oxide semiconductor (CMOS) processing [23-25]. Among them, Si_3N_4-based RRAM having a lot of traps in the Si_3N_4 layer playing a role as vacancies exhibit improved resistive switching characteristics including strong endurance, long retention, high on/off ratio, and fast switching speed [26, 27]. Moreover, it is reported that the RRAM with heavily doped silicon as a bottom electrode is fully compatible with CMOS fabrication processes [28, 29]. Engineering its material stack has raised the

prospect of achieving practical platforms for future low-cost nonvolatile memory applications.

1.4 Motivation and Thesis Organization

In this thesis, silicon nano-cone RRAM with a silicon nitride switching layer is investigated for the promising RRAM technology. Chapters will be presented as follows.

In Chapter 2, we investigate *I-V* characteristics and conduction mechanism of the silicon nitride (Si_3N_4)-based RRAM device with Ti/Si_3N_4/p-Si stack for its high compatibility with CMOS processing.

In Chapter 3, in order to investigate the area scaling effect, the cross-point RRAM with Ti/Si_3N_4/p-Si stack is fabricated and measured. Fabrication method of the proposed cross-point RRAM is introduced. Experimental results during the fabrication are presented. We also discuss the area scaling effect on electrical parameters such as switching voltage, current, and resistance.

In Chapter 4, in order to improve the switching characteristics, the nano-cone RRAM is proposed. The merit of the proposed structure will be introduced. To verify the merit of the device, TCAD simulation is performed. Fabrication method and experimental results are presented. Especially, silicon anisotropic wet etching process using TMAH is

described in detail. Resistive switching characteristics of the nano-cone RRAM will be discussed in comparison with the RRAM using conventional flat bottom electrode,

In the end, the conclusion is provided in Chapter 5.

Chapter 2

Basic Characteristics of Nitride-based RRAM with Si Bottom Electrode

2.1 Fabrication Results

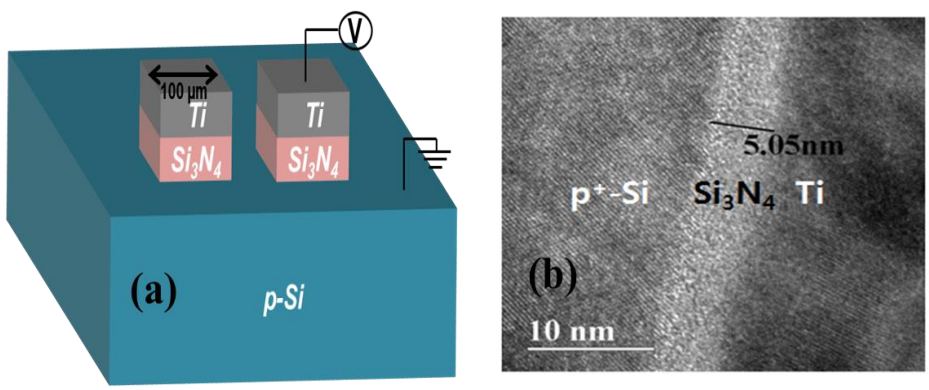


Fig. 2.1 Device configuration. (a) A schematic diagram and (b) transmission electron microscope (TEM) image of Ti/Si_3N_4/p-Si stacked RRAM cells.

Figure 2.1(a) shows the schematic diagram of fabricated Ti/Si_3N_4/p-Si RRAM cell. Fabrication process is as follows. First, 10 nm sacrificial oxide was grown by using dry oxidation. Then, in order to form the heavily doped p-Si

bottom electrode, BF_2 was implanted into the Si wafer at a dose of $10^{15}/cm^2$ and at implantation energy of 40 keV. Then, rapid thermal annealing was performed at 1000 ℃ for 10 sec. After sacrificial oxide strip, Si_3N_4 film with 5 nm thickness was deposited as a resistive switching material, using low pressure chemical vapor deposition (LPCVD). As shown in Fig. 2.1(b), 5 nm thick silicon nitride was uniformly deposited. In order to form the top electrode, a 100 nm thick titanium layer was deposited by sputter and patterned by using a photolithography and etching. The diameter of top electrode is 100 μm.

Our device has simple metal - insulator - semiconductor (MIS) structure with titanium (Ti) top electrode and p-type doped silicon (p-Si) bottom electrode. CMOS-friendly metal is adopted instead of noble metals such as platinum or ruthenium. Such a combination of memory stack materials can be easily adopted to 3D RRAM structure for high density memory application. For measurement, we applied positive or negative bias to the top electrode in the *I-V* sweep mode while the bottom electrode was grounded.

2.2 Measurement Results

2.2.1 Resistive Switching Characteristics

Figure 2.2 shows the typical bipolar resistive switching characteristics of Ti/Si_3N_4/p-Si RRAM. The set and reset processes occur under positive and negative biases, respectively. And the device has low reset current of 100 μA and forming-free behavior due to thin silicon nitride layer.

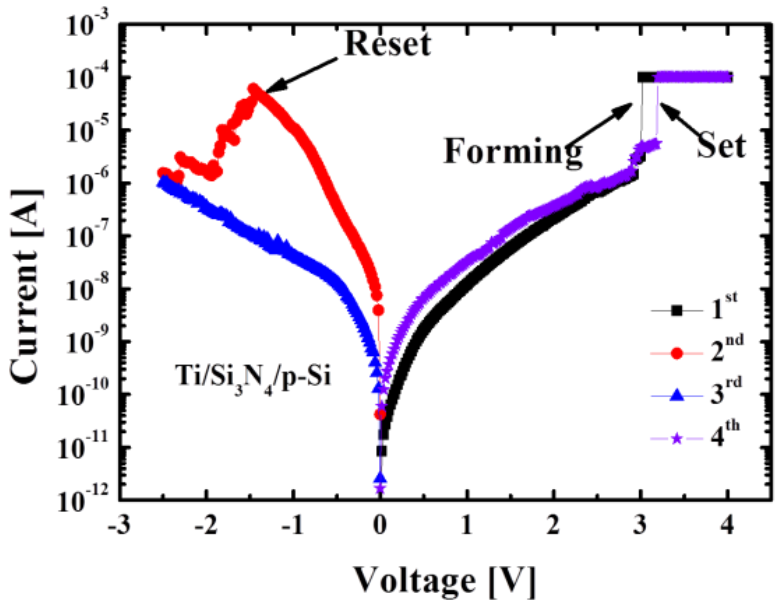


Fig. 2.2 Measured *I-V* curves of $Ti/Si_3N_4/p\text{-}Si$ stacked RRAM device showing bipolar resistive switching behaviors.

2.2.2 Conduction Mechanism

Recently, nitride-based RRAMs have been introduced to improve the endurance and switching speed. However, the research on the conduction mechanism of nitride-based RRAMs has been rarely performed.

In order to investigate the conduction mechanism, *I-V* fitting is performed. *I-V* fitting is the basic step of analyzing the conduction mechanism. We first consider two conduction mechanisms, since they share the $V^{1/2}$ dependence of current or conductance. Equation (1) and (2) indicate the Schottky emission and Poole-Frenkel (PF) models, respectively [30, 31].

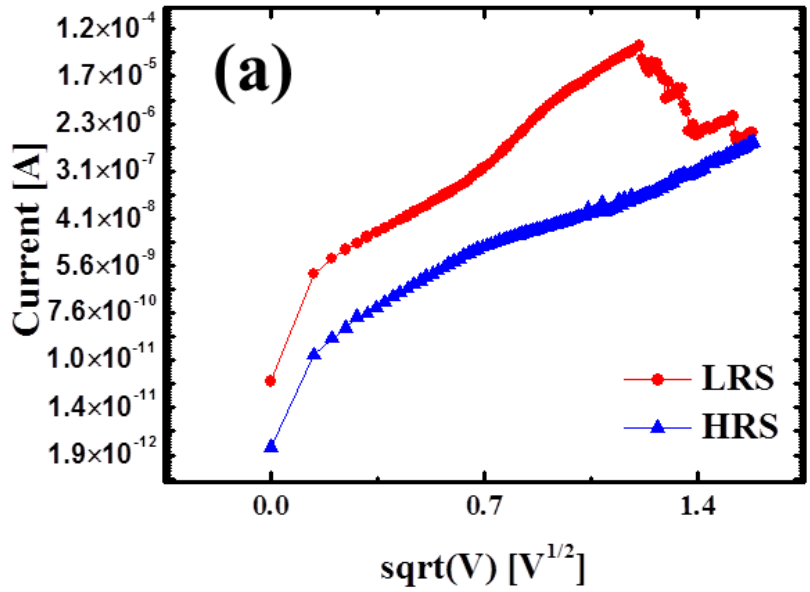
$$I = A^* T^2 exp(\beta_{Sc} V^{\frac{1}{2}}) exp(-q\emptyset_B / k_B T) \qquad (1)$$

$$I \propto V exp(\frac{\sqrt{\frac{q^3 V}{\pi \varepsilon L}} - E_t}{k_B T}) \qquad (2)$$

where A^* is the effective Richardson constant, T is the temperature, β_{Sc} is the

Schottky field lowering constant, V is the applied bias, q is the electron charge, Φ_B is the Schottky barrier height, k_B is the Boltzmann constant, ε is the dielectric constant, L is the thickness of insulator, and E_t is the energy barrier in zero applied electric field that an electron must cross to move from one atom to another in the crystal.

Both models are possible conduction mechanisms in an RRAM stack. If the conduction follows Schottky emission model, the natural logarithm of current should be proportional to the square-root of voltage. And if natural logarithm of conductance is proportional to the square-root of voltage, PF model is the possible conduction mechanism. Figure 2.3 shows the plot of current and conductance as a function of $V^{1/2}$, for Schottky emission and PF models, respectively. Although both models are expressed with an exponential function, the y-axis is plotted in the common logarithm instead of the natural logarithm because we judge whether the *I-V* curve are fitted with a straight line. In low resistance state (LRS), *I-V* curves do not seem to agree with any of the two models. In the high resistance state (HRS), however, they appear to follow both models.



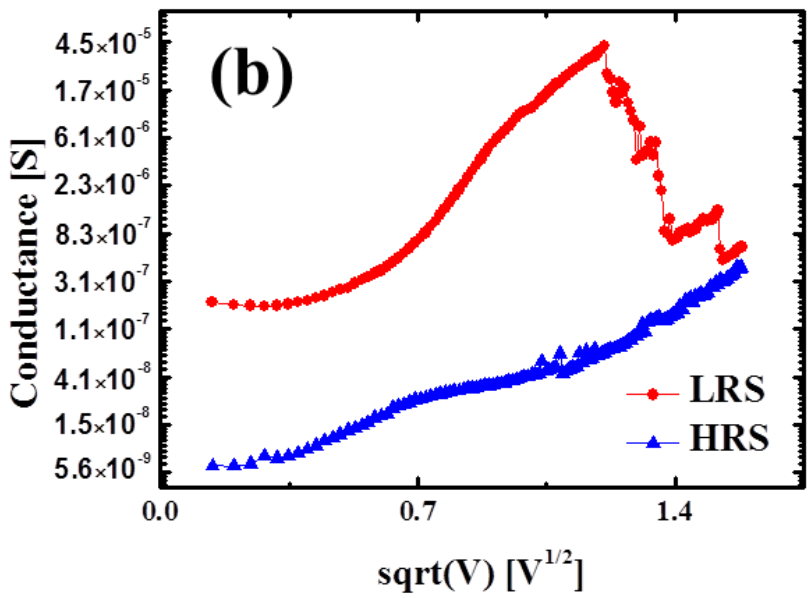


Fig. 2.3 Plots of (a) current (Schottky emission model) and (b) conductance (Poole-Frenkel model) as a function of the square-root of voltage.

For more detailed analysis, temperature dependence on current in HRS is investigated by varying the temperature from 25 ℃ to 150 ℃. We found that the HRS current has a weak dependence on the temperature as shown in Fig. 2.4. Therefore, we can rule out the possibility of Schottky emission.

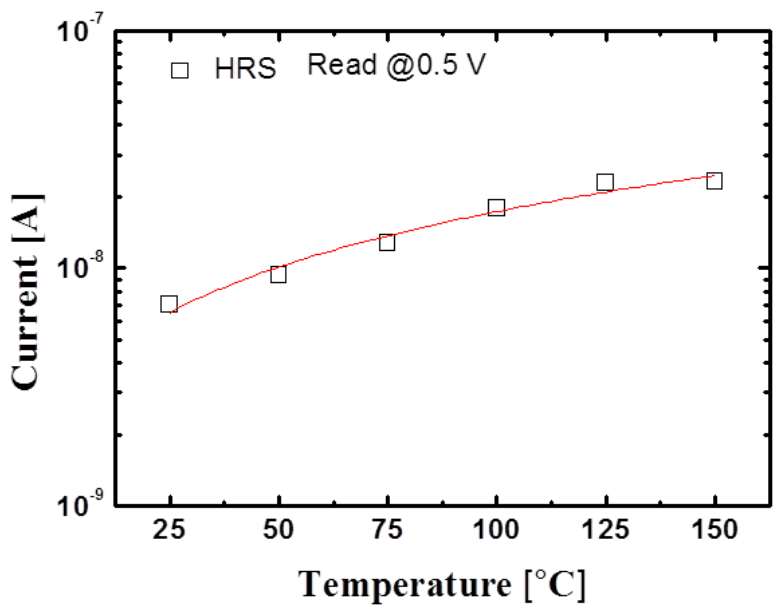


Fig. 2.4 Temperature dependence on the HRS current.

As shown in Fig. 2.5(a), we plot ln(I/V) vs. $1/k_BT$ curve to extract activation energy (E_a) for PF model fitting [32]. The activation energy at each bias is the slope in Fig. 2.5(a) divided by factor of log(e) for PF model fitting. From the activation energies, trap energy level can be extracted by extrapolating from the E_a vs. $V^{1/2}$ plot in Fig. 2.5(b). The values of trap energy (E_t) in positive and negative biases are 0.14 and 0.16 eV, respectively. And the dielectric constant of Si_3N_4 which is related to the slope of Fig. 2.5 (b) can be calculated by using Eq. (3).

$$\text{Slope} \sim \sqrt{\frac{q^3}{\pi \varepsilon L}} \qquad (3)$$

where ε and L mean the dielectric constant and thickness of Si_3N_4, respectively, in this experiment.

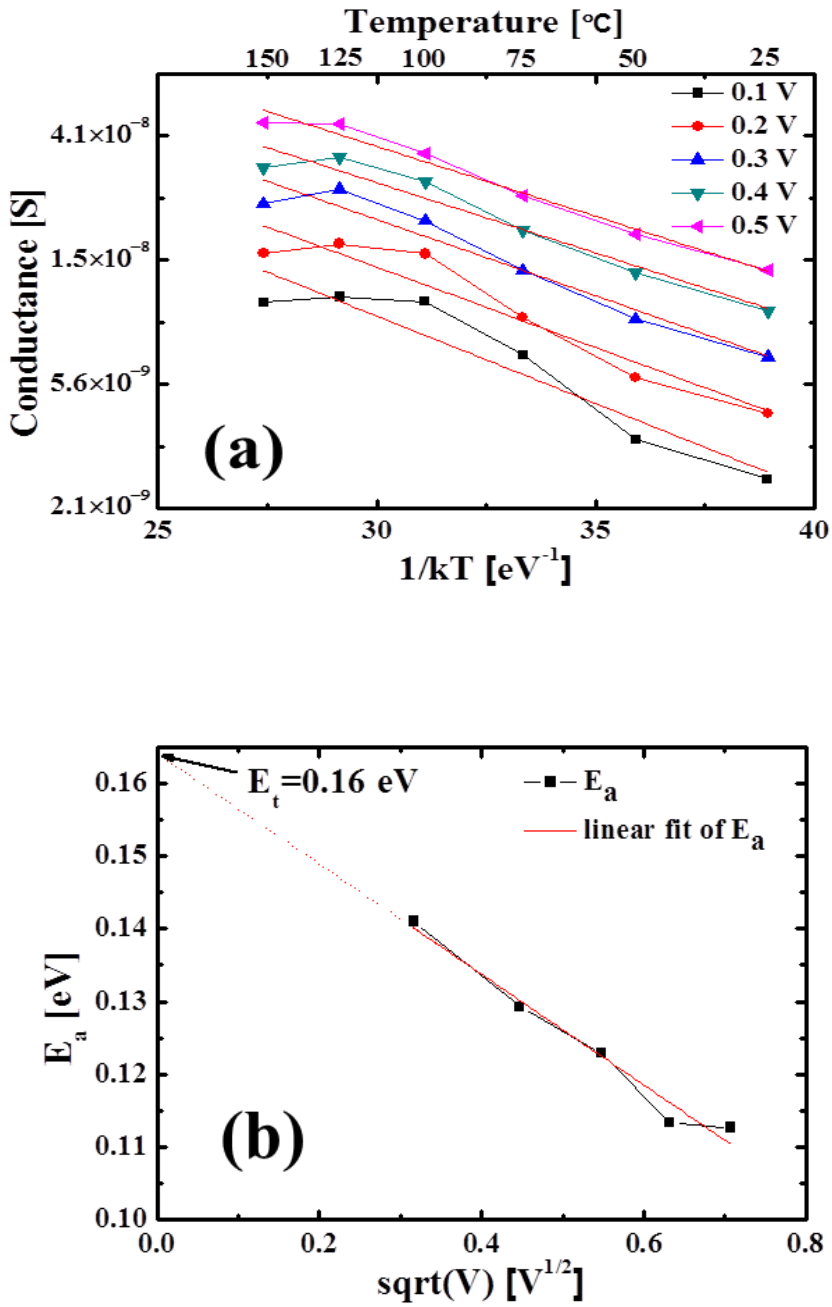


Fig. 2.5 Plots of (a) conductance as a function of temperature to extract activation energy and (b) activation energy as a function of read voltage to extract the trap energy level.

The value of the extracted dielectric constant is about 100, which is much higher than the known dielectric constant of about 7 for Si_3N_4. This discrepancy indicates that PF model is not the conduction mechanism in HRS [32].

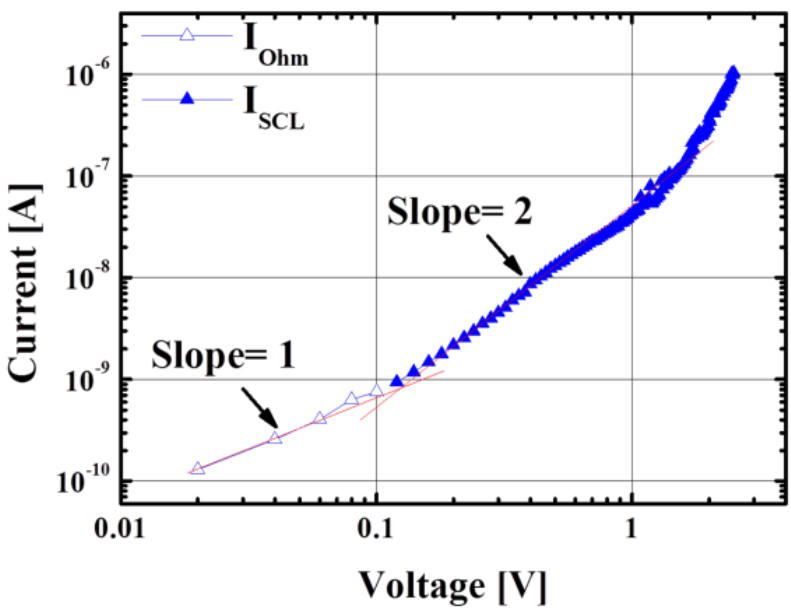


Fig. 2.6 SCLC fitting result in HRS.

Figure 2.6 shows the full log plot of *I-V* curve and the fitting results with space-charge-limited conduction (SCLC) in HRS. In low voltage region ($V < 0.1$ V), *I-V* relationship follows the Ohm's law and the slope is ~1. As the voltage

increases, the *I-V* relationship follows the Child's square law and the slope changes from 1 to 2 in SCL region. The current in SCL region can be expressed as Eq. (4) [33].

$$I = 10^{-13}\left[\frac{V^2(\mu_0\theta)\varepsilon}{L^3}\right] \quad (4)$$

Where $\theta = \frac{N_c}{N_t}e^{-\frac{E}{k_BT}}$ is the fraction of free charge, N_c is the number of states in the bottom k_BT slice of the conduction band, N_t is the shallow trap density occupying a single energy level, and μ_0 is the drift mobility of free carriers. *I-V* fitting results and the weak dependence of current on temperature support the hypothesis that SCLC is the dominant conduction mechanism in HRS [34-36]. As indicated in Fig. 2.7, in case of the insulator with trap-free or shallow traps, the conduction follows this model.

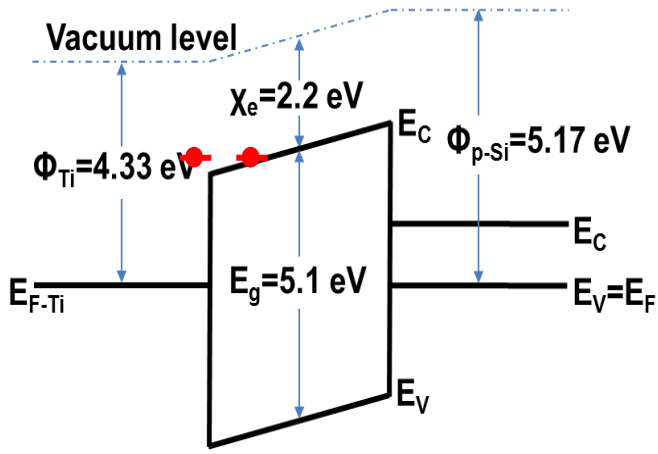


Fig. 2.7 Band diagram showing trap distribution in HRS.

Figure 2.8 shows the fitting results about SCLC in LRS. In contrast with HRS, *I-V* relationship is not well fitted with Child's square law. Instead, it is well fitted with the exponential function in SCL region. This is probably because that traps with deep energy level are generated by strong electric field during set process and distributed uniformly in energy below the conduction band as illustrated in Fig. 2.9 [33]. Therefore, the current depends exponentially on the applied voltage. In this region, the current can be given by Eq. (5) [33].

$$I = 10^{-13}\left(\frac{V\mu_0\varepsilon}{L^2}\right)\left(\frac{qn_{c0}}{C}\right)e^{\alpha V} \qquad (5)$$

where n_{c0} is the initial, thermal equilibrium concentration of free carriers, $\alpha = \frac{C}{n_t L q k_B T}$, n_t is the number of traps per cm^3 per unit range in energy, and C is the capacitance of device.

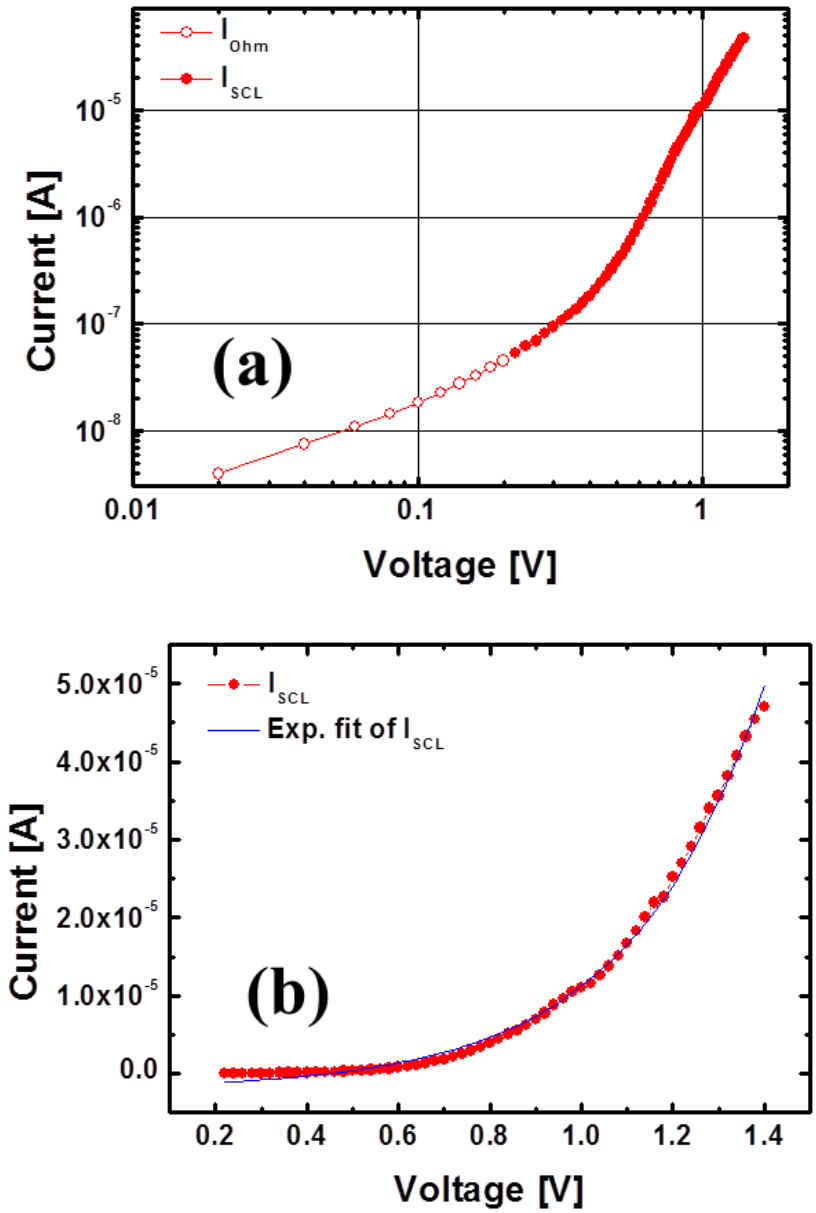


Fig. 2.8 Current characteristics modeling. (a) SCLC fitting result in the LRS and (b) exponential function fitting in the SCL region.

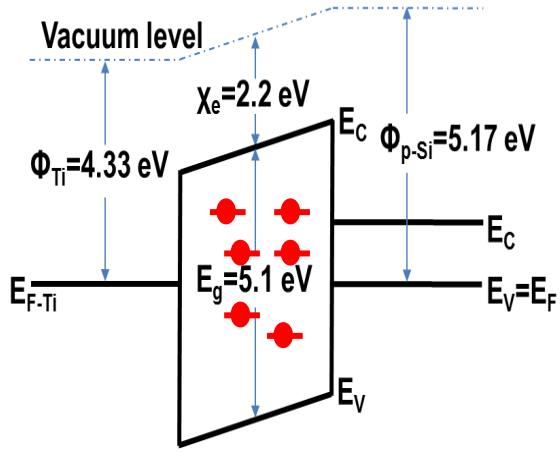


Fig. 2.9 Band diagram showing trap distribution in the LRS.

The property of different *I-V* relationship between LRS and HRS has advantage of the resistance switching performance. While HRS follows the Child's square law, LRS follows the exponential relationship due to the effect of generated traps. It leads to high on/off resistance ratio of 10^3.

Chapter 3

Area Scaling Characteristics of Cross-point RRAM

3.1 Fabrication Results

3.1.1 Process Flow

Figure 3.1 shows the process flow of cross-point RRAM. At first, silicon (Si) region is defined by the mix-and-match lithography process and patterned through dry etch process in bit line (BL) direction. Silicon nitride (Si_3N_4) is used as etch hard mask because Si_3N_4 plays a role as CMP stopper in the following process. In order to isolate the cells from each other, silicon dioxide (SiO_2) is deposited to fill the trenches by high density plasma chemical vapor deposition (HDPCVD) and removed using chemical-mechanical planarization (CMP). These processes are similar to conventional shallow trench isolation (STI) process. After removal of Si_3N_4 used as CMP stopper, ion implantation is conducted to form the heavily

doped p^+-Si region as bottom electrode (BE). Then, Si_3N_4 for switching layer (SL) and titanium (Ti) for top electrode (TE) are sequentially deposited on the p^+-Si. In the same manner as silicon patterning, TE/SL are also defined in word line (WL) direction. The active area in a cell is rectangular shape, which is created by crossing between WL and BL. Finally, conventional back end of line (BEOL) process is performed. Oxide deposition and contact hole etch is conducted. Metal deposition and patterning is consecutively conducted for electrical contact. TE and BE pads are connected to Ti and heavily doped p^+-Si region.

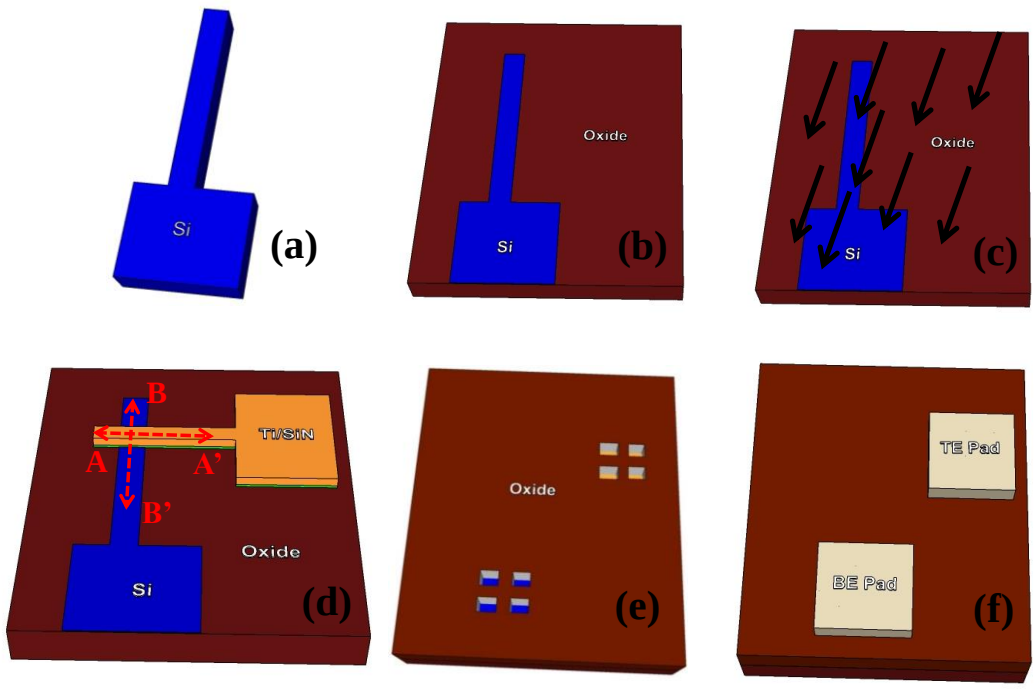


Fig. 3.1 Process flow for the cross-point RRAM:

(a) Silicon patterning by photo or e-beam lithography and etch (BL direction).

(b) Isolation region formation by oxide deposition and CMP process.

(c) Ion implantation for formation of heavily doped p^+-Si region.

(d) Switching layer (Si_3N_4) and top electrode (Ti) deposition and patterning (WL direction).

(e) Oxide deposition and contact hole etch.

(f) Metal deposition and patterning for contact.

3.1.2 Key Process Steps

By oxidizing the Si substrate, Si fin width can be further reduced than the lithographically defined dimension as shown in Fig. 3.2. Figure 3.2(a) shows the schematic cross sectional view of the patterned Si by lithography and etch processes. The Si fin width is determined by lithographic limitation. Figure 3.2(b), on the other hand, shows the schematic view of the laterally reduced Si after oxidation process. By consuming the both sides of the patterned Si, the extremely narrow Si fin width can be obtained beyond limitation of lithography process. In this experiment, in order to decide the oxidation condition, two principles should be considered. First, the thickness of pure silicon consumed in the oxidation process is 45 % of the final oxide thickness. The other is that oxide growth rate has dependence on crystal orientation. In (100) type Si wafer, the side of Si fin is in (110) plane. The oxide growth is faster on (110) oriented surfaces than on (100) oriented due to differences in the surface density of silicon atoms on the various crystal faces [37]. Figure 3.3 shows the SEM images of oxidized Si fin (a) before

HF dipping and (b) after HF dipping to remove the grown oxide. It is verified that the Si fin can be successfully reduced by oxidation process. As shown in Fig. 3.4, average 24 nm Si is consumed and the minimum width of Si fin is 12 nm. Sub-10 nm Si fin can be expected through more precise control of oxidation process.

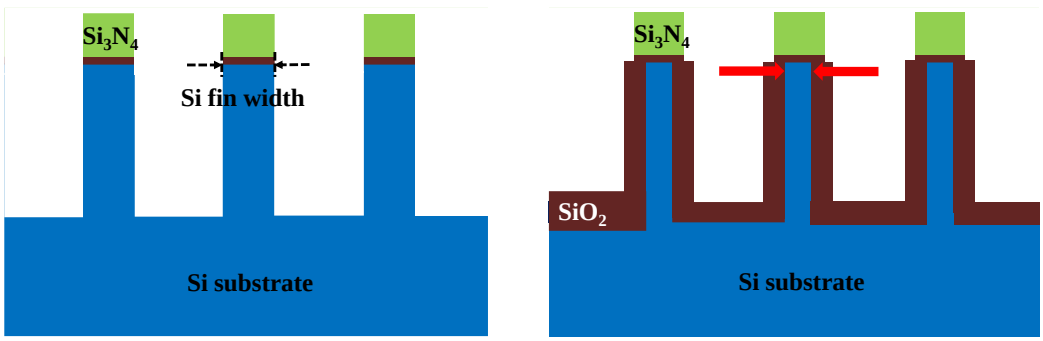


Fig. 3.2 Illustrations to explain the Si fin width reduction method. (a) Before and (b) after the thermal oxidation of Si fins.

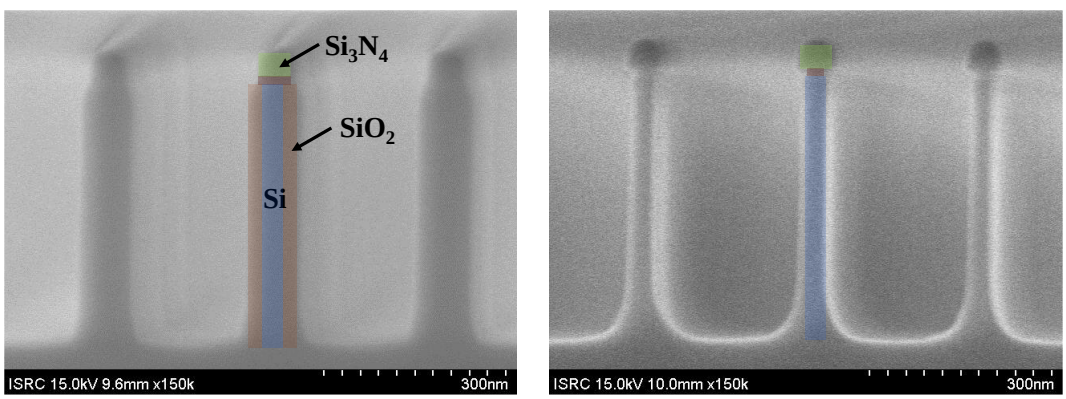


Fig. 3.3 SEM images of (a) oxidized Si fin and (b) Si fin after HF dipping (layout size = 70 nm).

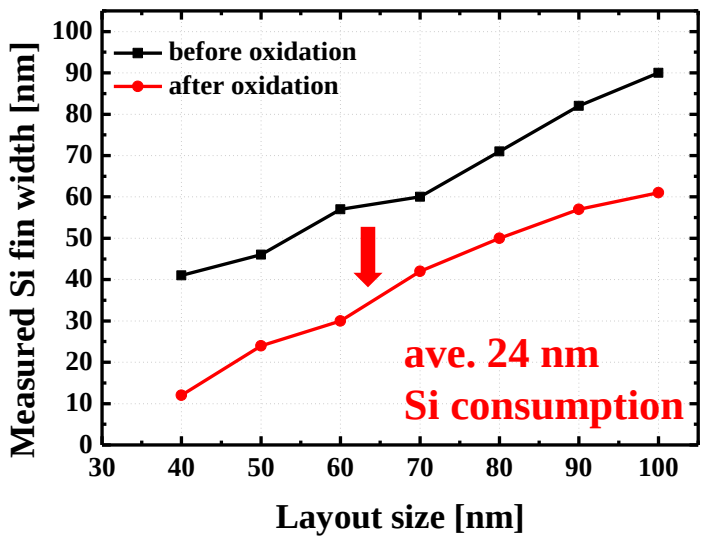


Fig. 3.4 Measured Si fin width as a function of layout dimension.

Figure 3.5 shows SEM image of cross-sectional view of the Si fin after the first step of CMP using oxide slurry. About 30 nm thick SiO_2 on Si_3N_4 remains. The remaining SiO_2 on Si_3N_4 is polished off during the second step of CMP using ceria slurry which has high selectivity over Si_3N_4. The Si_3N_4 of CMP stopper is removed by wet etch process using H_3PO_4.

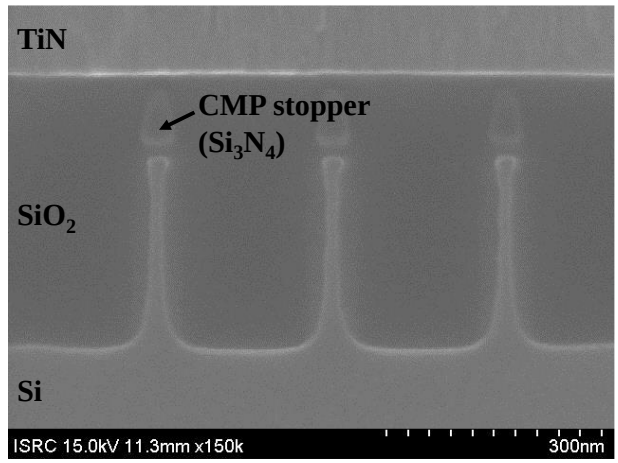


Fig. 3.5 SEM image of the Si fin after CMP using oxide slurry (layout size= 40 nm).

Figure 3.6 shows TEM image of B-B' cut of Fig. 3.1(d). As shown in Fig. 3.6, it is observed that the color of point 2 is different from that of point 1. It means that the two materials are not the same. In order to detect the composition elements of both materials, energy dispersive spectrometry (EDS) analysis is used. Figure 3.7 shows EDS spectrums at (a) point 1 and (b) point 2 of Fig. 3.6. While only titanium is detected at point 1, oxygen is additionally detected with titanium at point 2. From EDS data, we verify that both sides of titanium is oxidized by O_2 plasma during photoresist ashing process. The oxidized titanium plays the same role as the oxidized Si of bottom electrode.

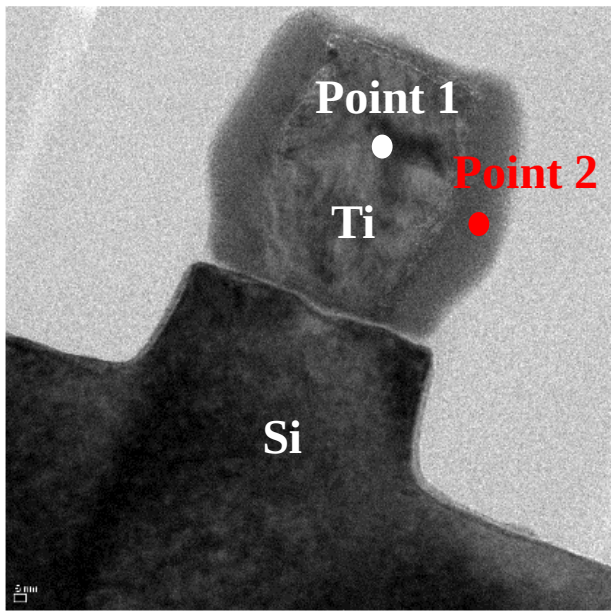


Fig. 3.6 TEM image of B-B' cut in Fig. 3.1(d).

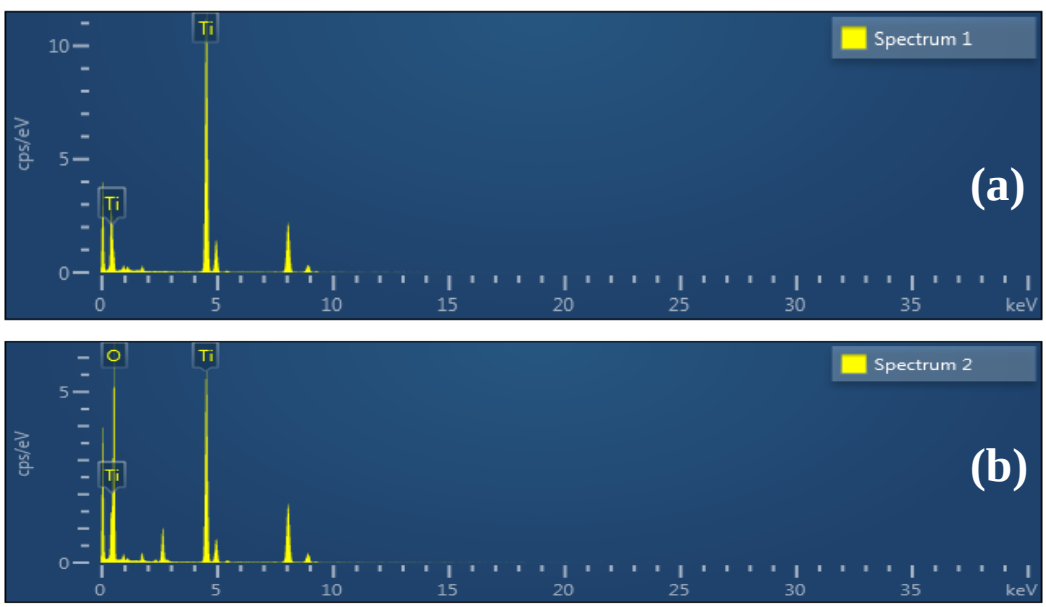


Fig. 3.7 EDS spectra at (a) point 1 and (b) point 2 in Fig. 3.6.

Figure 3.8 shows the cross-sectional view of Fig. 3.1(d). The region where the Ti top and Si bottom electrodes intersect each other means active region occurring resistive switching phenomenon. Therefore, the active area of the fabricated device is defined as the product of width of in Fig. 3.8(a) and width of Ti in Fig. 3.8(b). Table 4.1 shows measured values of the widths of p^+-Si and widths of Ti from TEM images and calculated values of the active area. The widths are defined by e-beam lithography. Table 4.2 shows the layout dimensions of the widths which are defined by photolithography. The active areas of the devices fabricated by photolithography are defined by the product of layout dimension because the widths is relatively large compared to the widths defined by e-beam lithography.

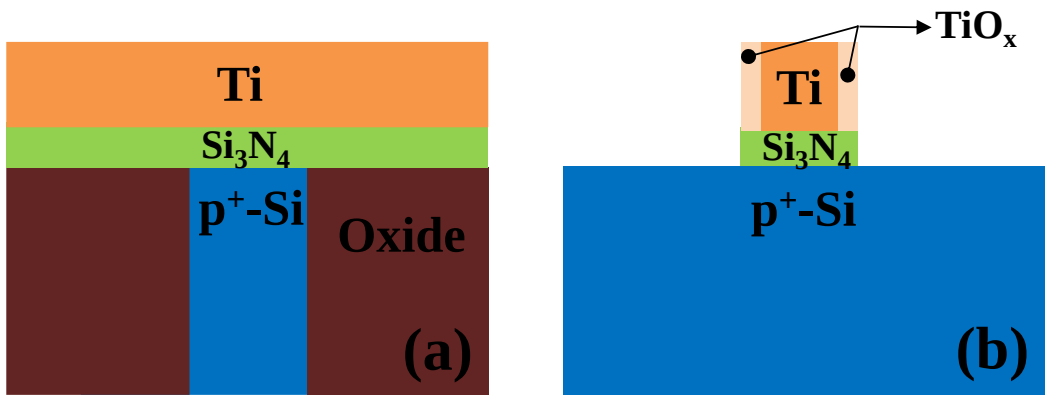


Fig. 3.8 Cross-sectional views in Fig. 3.1(d) along (a) A-A' and (b) B-B' cutlines.

Table 4.1 Measured values of the width of p^+-Si and width of Ti from TEM images and calculated values of the active area. The widths are defined by e-beam lithography.

Layout dimension [nm]	**60**	**70**	**80**	**90**	**100**	**300**
Width of p^+ Si [nm]	**43**	**46**	**58**	**72**	**78**	**257**
Width of Ti [nm]	**73**	**75**	**88**	**100**	**102**	**297**
Active area [nm^2]	**$3.139*10^3$**	**$3.45*10^3$**	**$5.104*10^3$**	**$7.2*10^3$**	**$7.956*10^3$**	**$7.633*10^4$**
Active area [μm^2]	**$3.139*10^{-3}$**	**$3.45*10^{-3}$**	**$5.104*10^{-3}$**	**$7.2*10^{-3}$**	**$7.956*10^{-3}$**	**$7.633*10^{-2}$**

Table 4.2 Layout dimensions and calculated values of the active area. The widths are defined by photolithography.

Layout dimension [µm]	**0.5**	**1**	**3**	**5**	**10**
Active area [nm^2]	**$2.5*10^5$**	**10^6**	**$9*10^6$**	**$2.5*10^7$**	**10^8**
Active area [μm^2]	**$2.5*10^{-1}$**	**1**	**9**	**$2.5*10^1$**	**10^2**

3.2 Measurement Results

Figure 3.9 shows the typical *I-V* curves of Ti/Si_3N_4/p-Si stacked cross-point RRAM device showing bipolar resistive switching behavior. While the forming-less characteristics is observed in large cell size, forming voltage is higher than set voltage in small cell size.

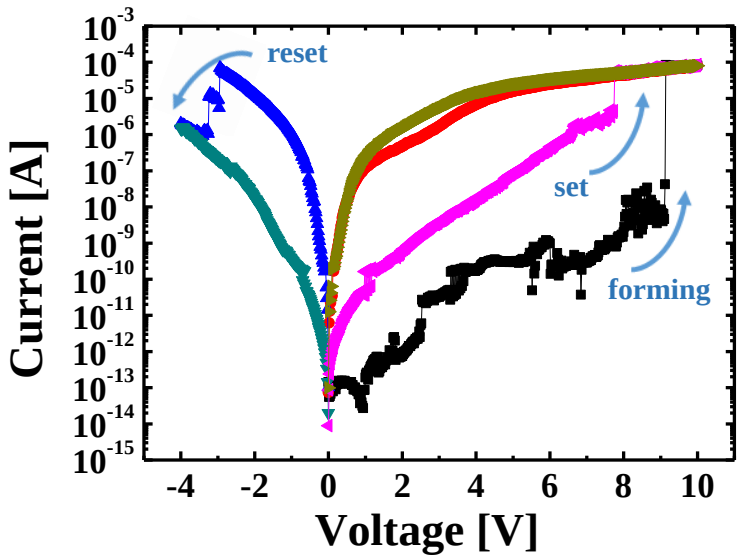


Fig. 3.9 Typical *I-V* curves of Ti/Si_3N_4/p-Si stacked cross-point RRAM device showing bipolar resistive switching behavior (layout dimension = 60 nm).

Figure 3.10 shows the double logarithmic plot of *I*-*V* characteristics of highly scaled cross-point RRAM device. Here, the SCLC conduction is observed in both HRS and LRS states. In low voltage region ($V < V_{tr}$), the *I*-*V* curve follows Ohm's law ($I \sim V$), which implies that the density of thermally generated free carriers inside the nitride film is higher than that of the injected carriers [38]. Transition voltage (V_{tr}) is the minimum voltage required for the transition. In this region, the carrier transit time is longer than the dielectric relaxation time, which means that the injected carriers redistribute themselves in the electrically quasi-neutral nitride film. In the high-voltage region of $V > V_{tr}$, the injected excess carriers become dominant over the thermally generated carriers. When strong injection is present, the injected carriers do not redistribute themselves anymore, get trapped, and space charges are revealed. At V_{TFL}, the current rapidly jumps from its low trap-limited value to the high trap-free SCL current. Trap-filled-limited voltage (V_{TFL}) is defined as the voltage required to fill the traps. In case of very high injection, all the traps are filled and the conduction becomes the space-charge-limited (Child's law). In the space-charge-limited region, the slope is larger than 2 since the nitride

film is not a perfectly trap-free layer.

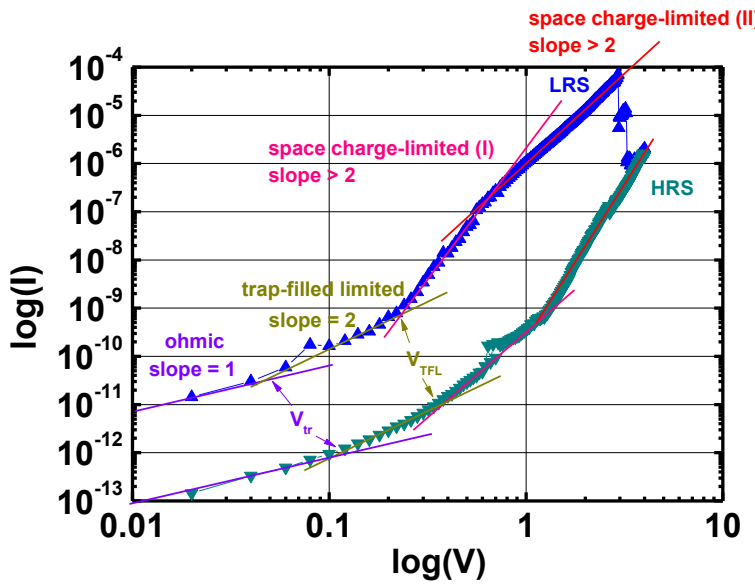


Fig. 3.10 Double logarithmic plot of *I-V* characteristics for scaled cross-point RRAM device, showing the SCLC conduction in both HRS and LRS.

In order to investigate the effect of area scaling on the switching parameters, we measure 50 cells of each device area. Current compliance is fixed at 100 μA. Fig. 3.11(a) shows the forming voltage scaling trends as a function of cell area. As the cell area decreases, the forming voltage increases [39-44]. It is evident that the possibility of generating the conductive filaments formed by nitride-related defects decreases with decreasing active area under uniformly applied electric field. The nitride-related defects are Si and N dangling bonds [45, 46]. In as-deposited nitride film, dangling bonds exist and are also created by illumination, heat, and electric field [45-49]. Forming voltage is closely related with the initial resistance of pristine cell as shown in Fig. 3.11(b). This forming voltage scaling trend is undesirable for low power operation. In order to reduce or even eliminate the forming process, two approaches exist. It is claimed that reducing the thickness of switching layer is one. Another solution is to create "local enhancement" where structural modification enables higher electric field in smaller devices to preferentially trigger forming in localized regions.

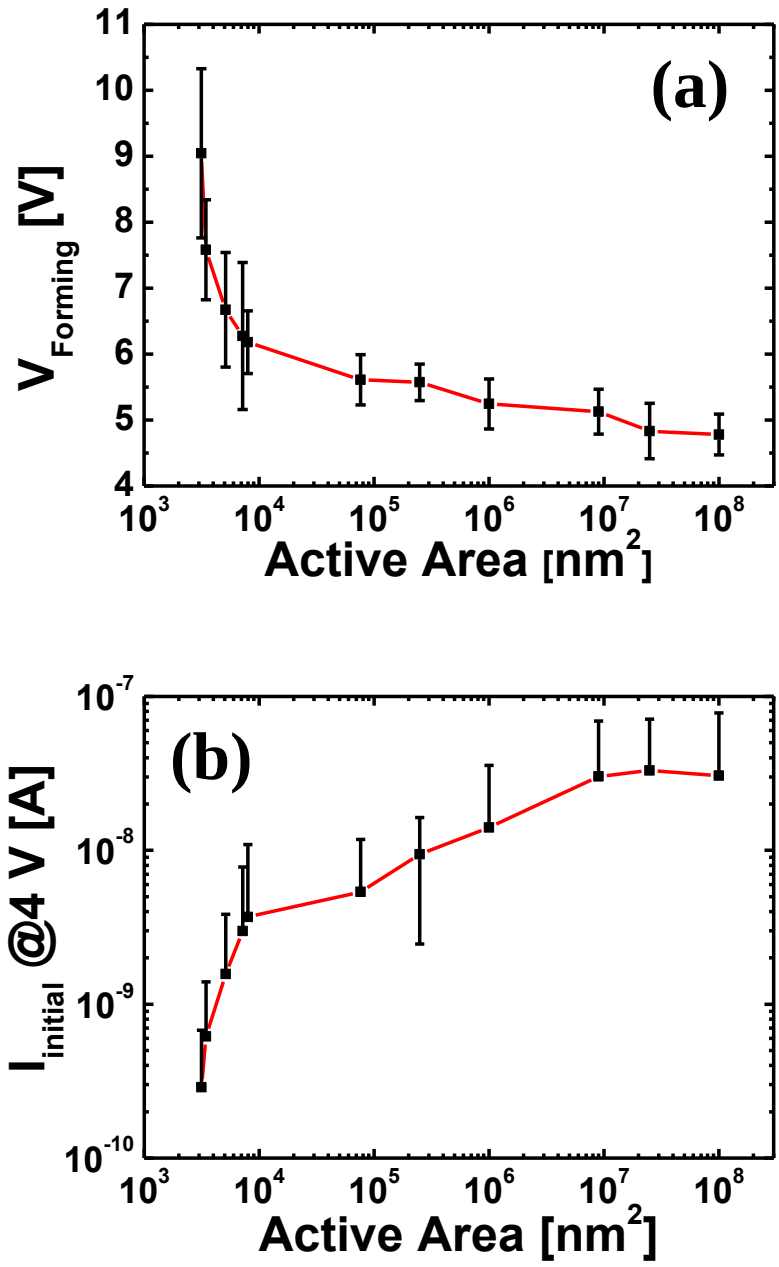


Fig. 3.11 (a) Forming voltage and (b) initial current trends as a function of device area.

Figure 3.12(a) shows the set voltage scaling trends as a function of cell area. As the cell area decreases, the set voltage increases [39, 40, and 42]. The scaling trends of forming voltage and set voltage appear the same. This trend is not consistent with Ref. [43] which claims that the change of set voltage is negligible. It means that the remaining conducting filament is a dominant source for formation of conductive filament path during set operation. In our device, nitride-related defects are still dominant sources which is dependent on device area. The set voltage is closely related with the HRS resistance as shown in Fig. 3.12(b).

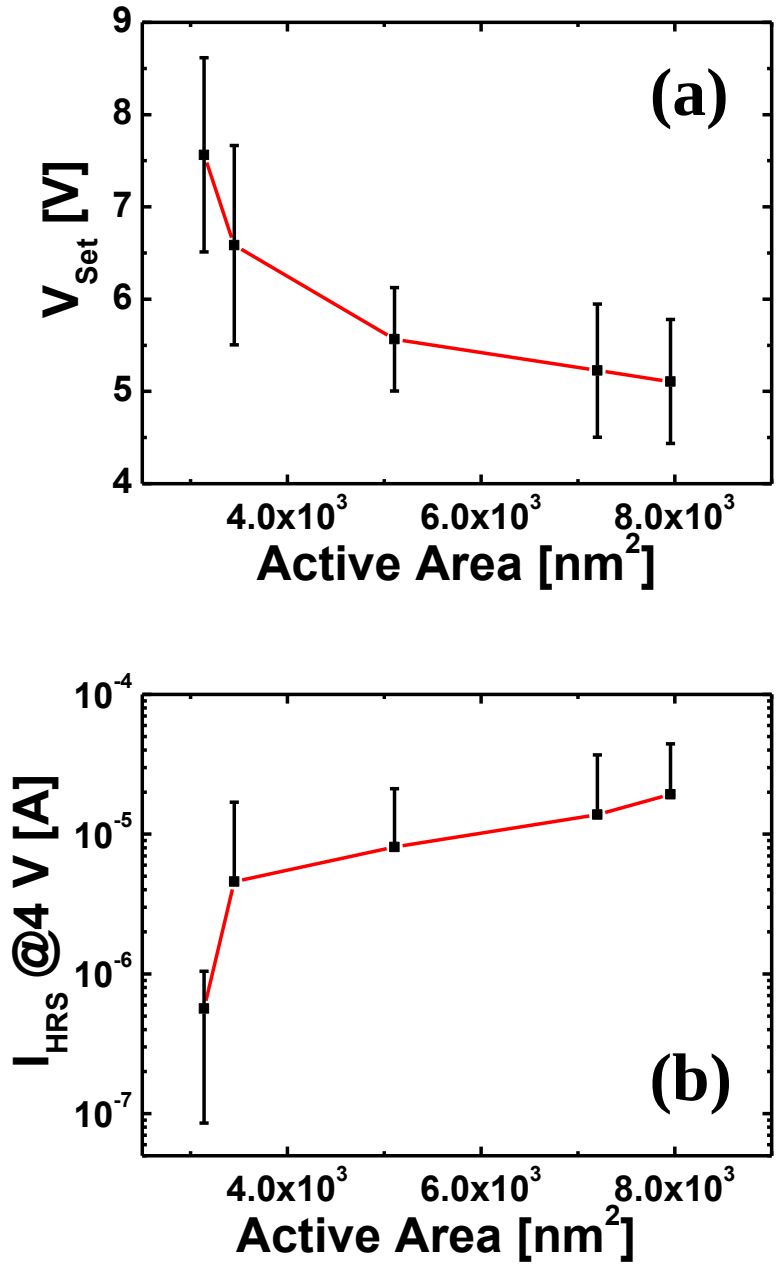


Fig. 3.12 (a) Set voltage and (b) HRS current trends as a function of device area.

Figure 3.13(a) shows the reset voltage scaling trends as a function of cell area. Although there is weak dependence on the device area, the reset voltage also slightly increases as the active area increases and significantly increases in smallest size. Figure 3.13(b) shows reset current scaling trends as a function of cell area. As the cell size decreases, reset current decreases. Figure 3.14 shows the reset current scaling trend as a function of active area at (a) 10 μA and (b) 1 μA of compliance current, respectively. In all compliance condition, the same scaling trends are observed. Figure 3.15 shows the relationship between the compliance current and the reset current with the various active areas. It is known that by changing the compliance current, the reset current can be tuned. While nearly 1:1 relation between the compliance current and reset current has been reported [50], the reset current is saturated due to current overshoot during set operation in these devices. The current overshoot is caused by parasitic capacitance and can be suppressed by connecting the series transistor or resistor with an RRAM cell internally [50, 51].

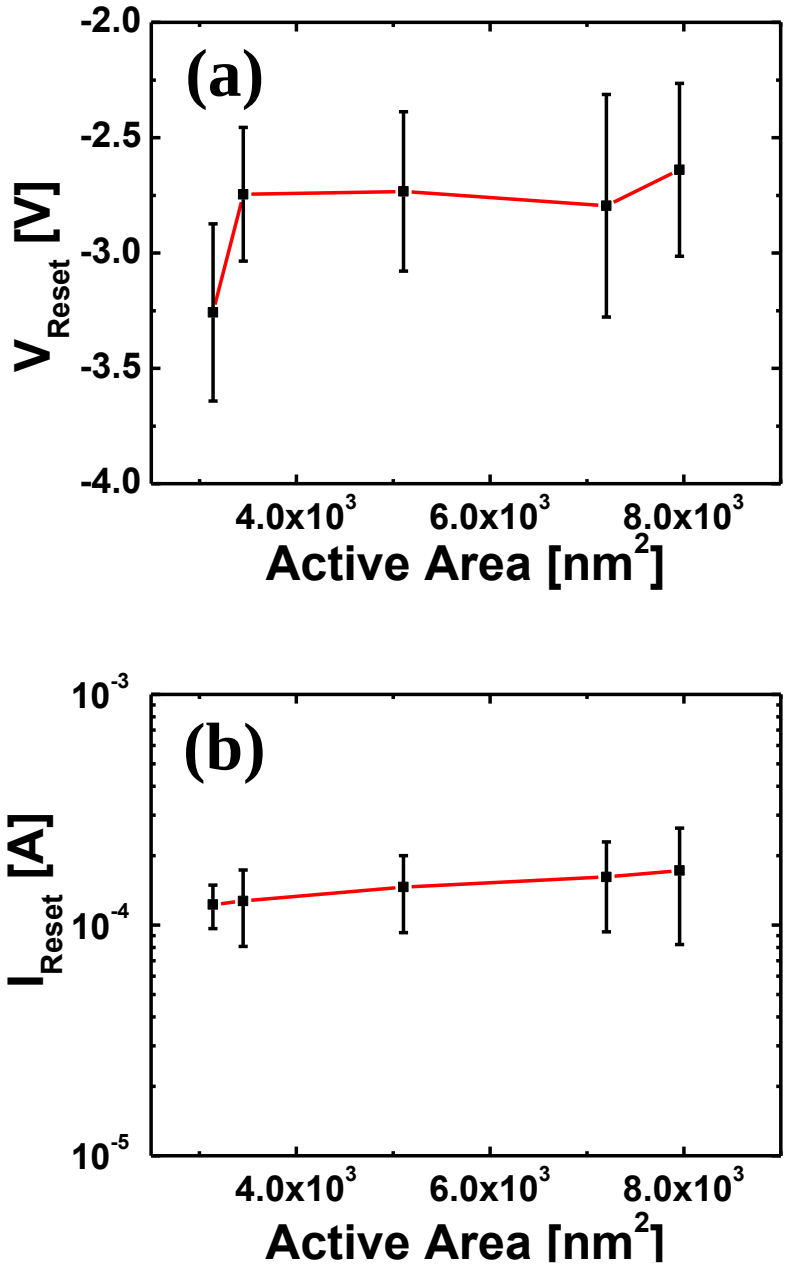


Fig. 3.13 (a) Reset voltage and (b) reset current trends as a function of device area.

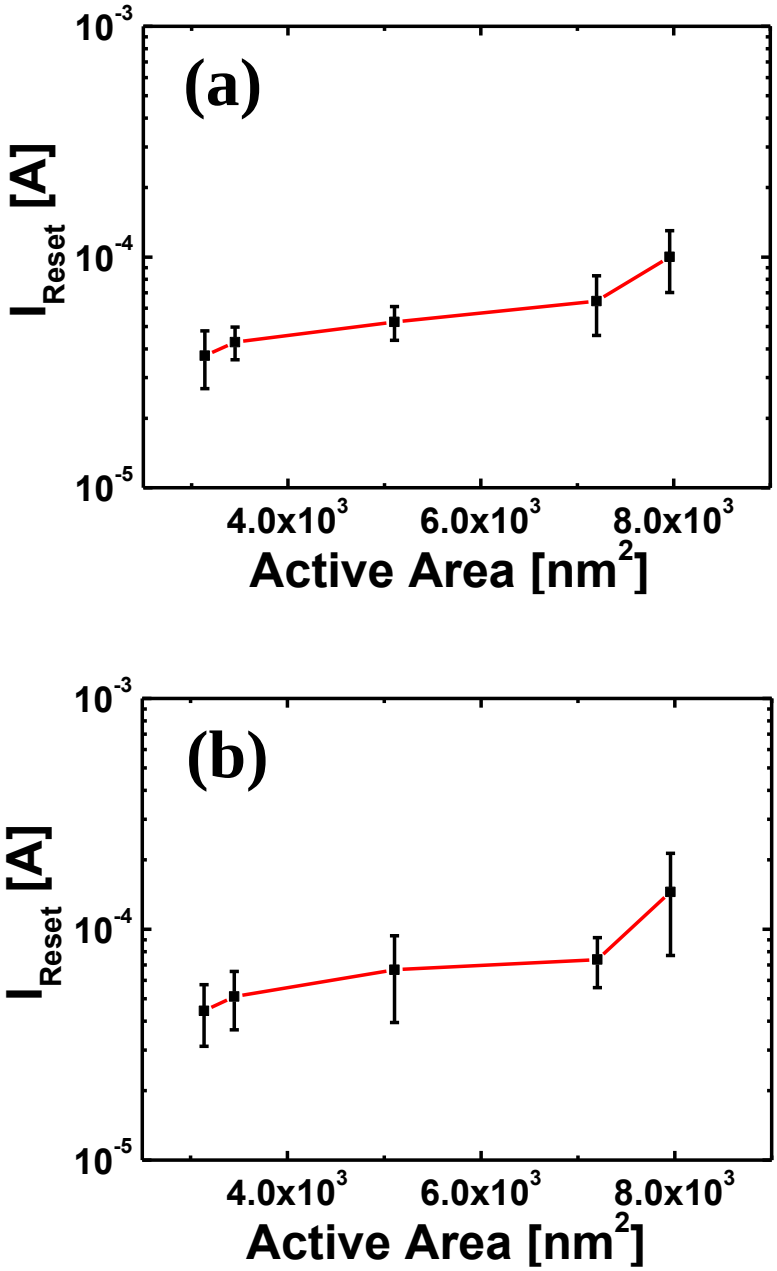


Fig. 3.14 Reset current as a function of device area. (a) Compliance current = 10 μA. (b) Compliance current = 1 μA.

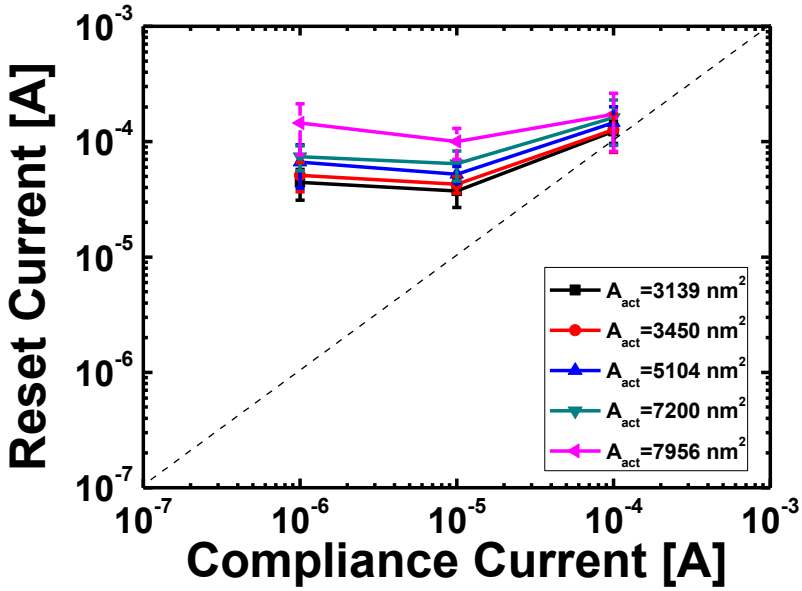


Fig. 3.15 Relationship between the compliance current and the reset current.

Figure 3.16 shows the retention properties of HRS and LRS at 0.2 V and 85 °C in the scaled RRAM cell. While HRS exhibits little degradation, LRS resistance becomes higher during baking time of 10^4 sec.

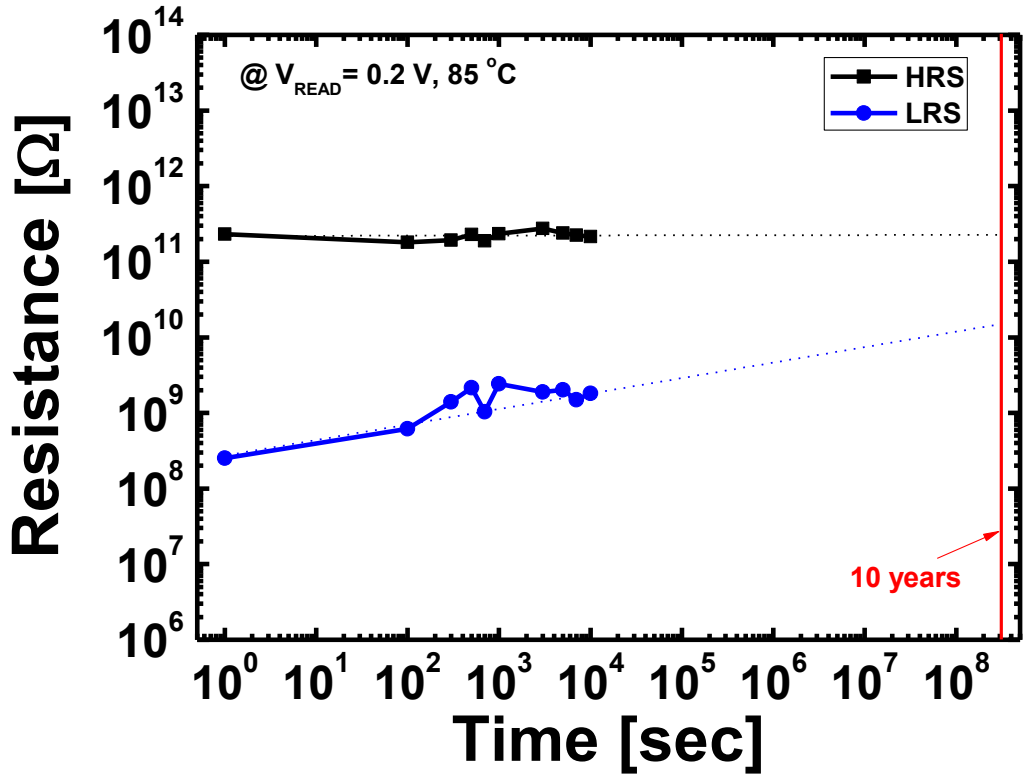


Fig. 3.16 Retention properties of the scaled RRAM cell at 0.2 V and 85 °C (layout dimension = 70 nm).

Chapter 4

Nanostructured RRAM

4.1 Nano-cone RRAM

Figure 4.1 shows the schematic diagram of nano-cone RRAM array for the proposed structure. Its unit cell has a simple MIS structure with metal top electrode (TE), switching layer (SL), and silicon (Si) bottom electrode (BE). Due to the cone shape of Si BE, electric field concentration effect is generated, which helps to achieve a low power operation. As shown in close-up drawing of Fig. 4.1, the location of conductive filament (CF) formation is determined by the size of the cone tip regardless of the size of top electrode.

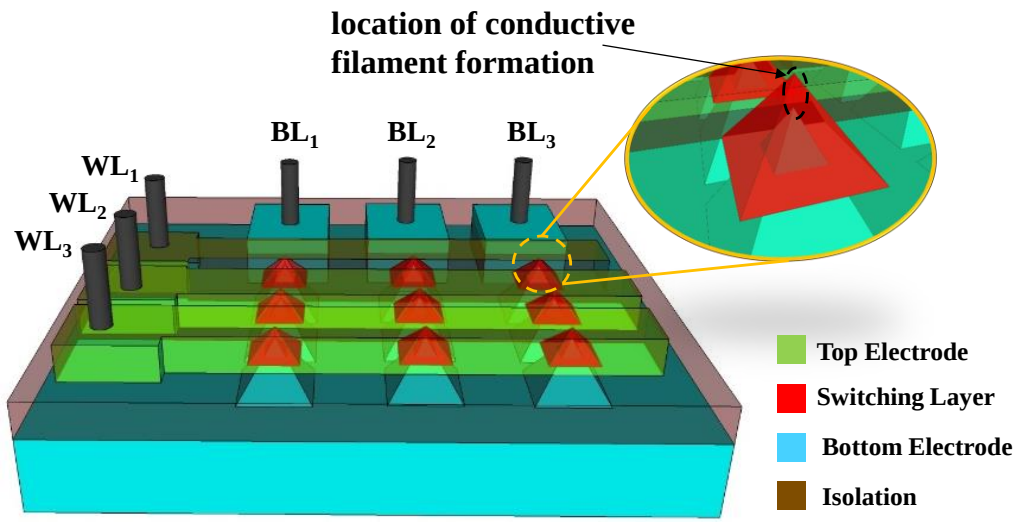
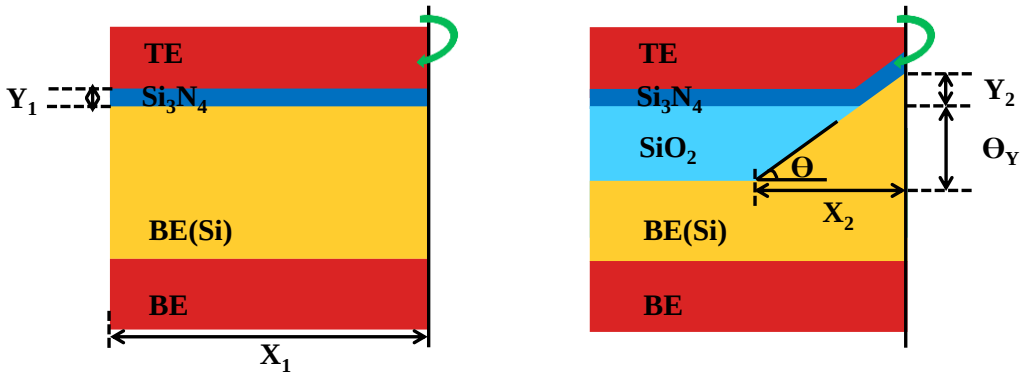


Fig. 4.1 Schematic drawing of the proposed nano- cone RRAM array and close-up drawings of unit cells in the nano-cone RRAM.

4.2 Simulation Results

In order to verify the main feature of the proposed structure, we investigate the electric field concentration effect using SILVACO^{TM} simulation tool. Figure 4.2 illustrates the simulation structures in cylindrical coordinates for 3-dimensional simulation. Table 4.1 indicates the simulation parameter values for conventional and nano-cone structures. The same voltage (1 V) and switching layer thickness (Y_1) is applied to both structures for fair comparison to evaluate the electric field concentration effect. In the nano-cone structures, angle (Θ) is changed by varying the height (Θ_Y). The height of nano-cone tip (Y_2) exposed above silicon oxide layer is fixed.



(a) (b)

Fig. 4.2 Schematics of the (a) conventional (without slope) and (b) nano-cone (with intended slope) structures for evaluating the electric field concentration effects.

Table 4.1 Simulation parameter values for conventional and nano-cone structures.

	X_1 (fixed)	X_2 (fixed)	Y_1 (fixed)	Y_2 (fixed)	Angle (Θ)
Conventional	500 nm	400 nm	10 nm	60 nm	-
Spilt 1					50°
Split 2					60°
Split 3					70°
Split 4					80°

Figures 4.3(a) through (f) show (a) structure of the simulated nano-cone RRAM and (b) electric field contour of conventional RRAM and (c)-(f) electric field contours of nano-cone RRAM varying angle of nano-cone at 1 V on the top electrode. Compared with the uniform electric field distribution in the conventional structure, stronger electric fields near the sharp points are observed in the nano-cone structures. This tendency becomes more prominent as the nano-cone structure has a steeper angle. In the nano-cone RRAM, however, the location of maximum electric field is not exactly at the end of the tip. The peak is located at 1~2 nm distance from the end of the tip. This is due to the field effect induced by the depletion region of the doped Si. Figure 4.4(a) shows the hole concentration contour of the nano-cone RRAM with an angle of 70°. At the end of tip, the concentration of hole is very low, which is the formation of depletion region. Figure 4.4(b) shows the potential along the A-A' direction. Since the potential drop across the depletion region is high, the electric field in switching layer is low at the end of tip. As a result, the location of maximum electric field shift is deviated from the end of tip. Figure 4.5 shows the maximum electric field

as a function of angle. The maximum electric field increases as the tip angle increases. The structure with angle of 70° has stronger electric field of more than 5 times of conventional one. The reason why the structure with an angle of 70° was examined is that the angle obtained from the actual device fabrication was 70°. Due to the localization of strong electric field, the nitride-related defects are more readily generated at the end of tip. In turn, it leads to higher formation probability of conductive filaments. Therefore, it is expected that the switching voltages can be reduced and switching area can be effectively confined to a small region by using the proposed structure due to the highly localized field concentration.

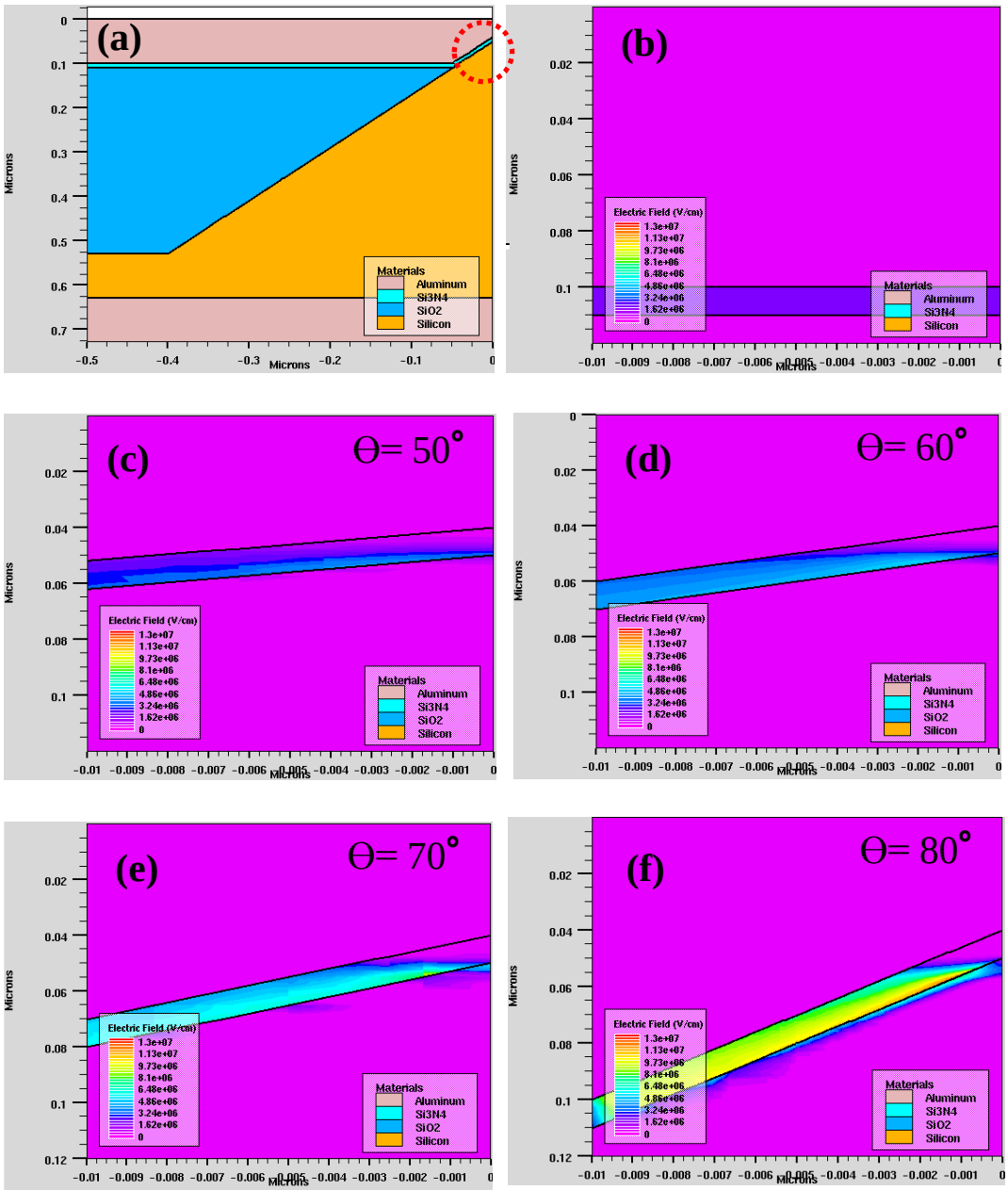


Fig. 4.3 Simulated structures. (a) Nano-cone RRAM. Electric field contour of (b) conventional RRAM and (c)-(f) nano-cone RRAM with different cone angles at 1 V on top electrode metal.

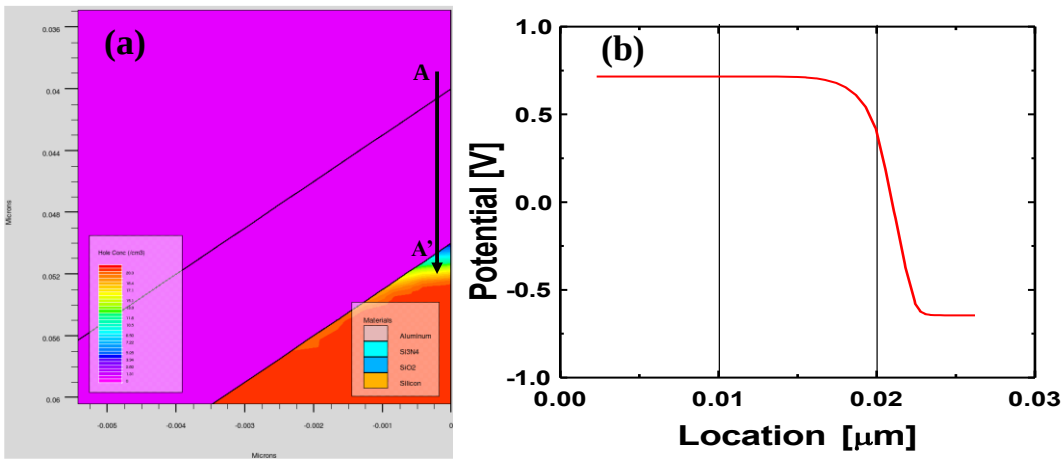


Fig. 4.4 Confirmation of the depletion region. (a) Hole concentration contour and (b) potential along the A-A' cutline in the nano-cone RRAM device with a cone angle of 70°.

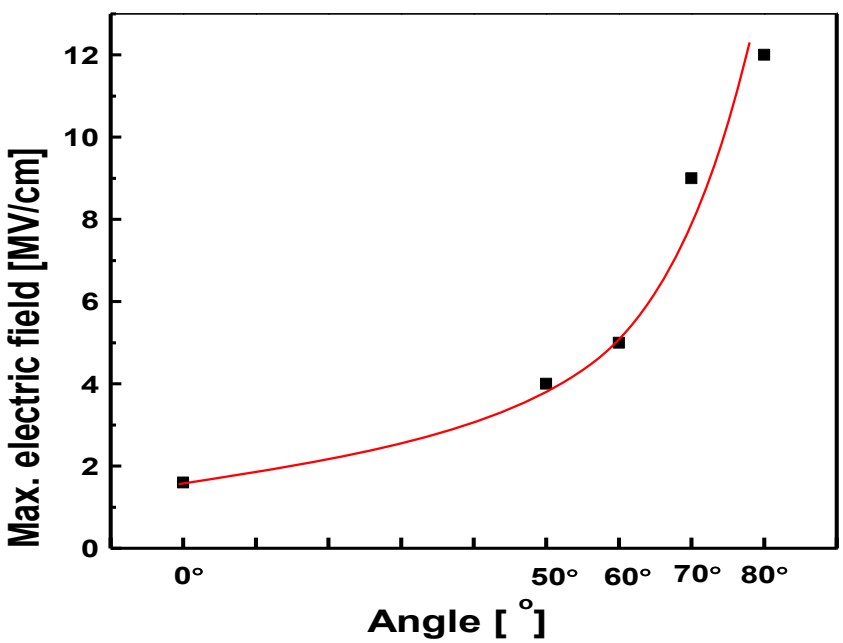


Fig. 4.5 Maximum electric field as a function of cone angle.

4.3 Fabrication Results

4.3.1 Process Flow

The fabrication process of the proposed nano-cone RRAM array is fully compatible with the conventional CMOS process as described in Fig. 4.6(a)~(j). Bulk Si wafer is used (Fig. 4.6(a)). At first, the silicon region is defined by the lithography process and patterned through dry etch process in bit-line (BL) direction (Fig. 4.6(b)). In order to isolate the cells from each other, silicon dioxide (SiO_2) is deposited to fill the trenches by high density plasma chemical vapor deposition (HDPCVD) and removed using chemical-mechanical planarization (CMP) (Fig. 4.6(c)). These processes are similar to conventional shallow trench isolation (STI) process. In order to form the nano-cone, the deposition and patterning of hard mask (SiO_2) is conducted for each cell (Fig. 4.6(d)). Anisotropic wet etch is conducted by using TMAH (Fig. 4.6(e)). Then, ion implantation is conducted to form the heavily doped p^+-Si region (Fig. 4.6(f)). To

expose only the tip of the cone SiO_2 deposition, CMP, and SiO_2 wet etch proceeds step by step (Fig. 4.6(g)). SL and TE are sequentially deposited on the p^+-Si cone and patterned along word-line (WL) direction (Fig. 4.6(h)). Finally, back end of line (BEOL) process is performed. Before the deposition of inter-layer dielectric (ILD) material, the oxide on the Si should be etched (Fig. 4.6(i)). After ILD oxide deposition, contact hole etch is conducted (Fig. 4.6(j)). Metal deposition and patterning is consecutively conducted for electrical contact (Fig. 4.6(k)).

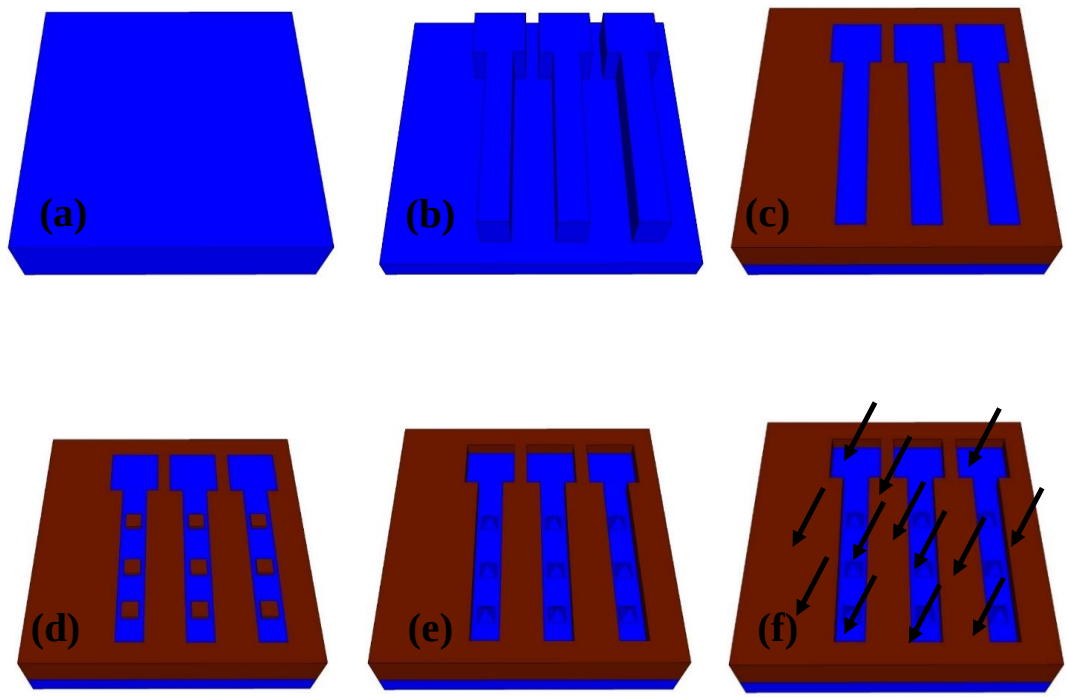


Fig. 4.6 Process flows for nano-cone RRAM:

(a) Bulk Si wafer preparation.

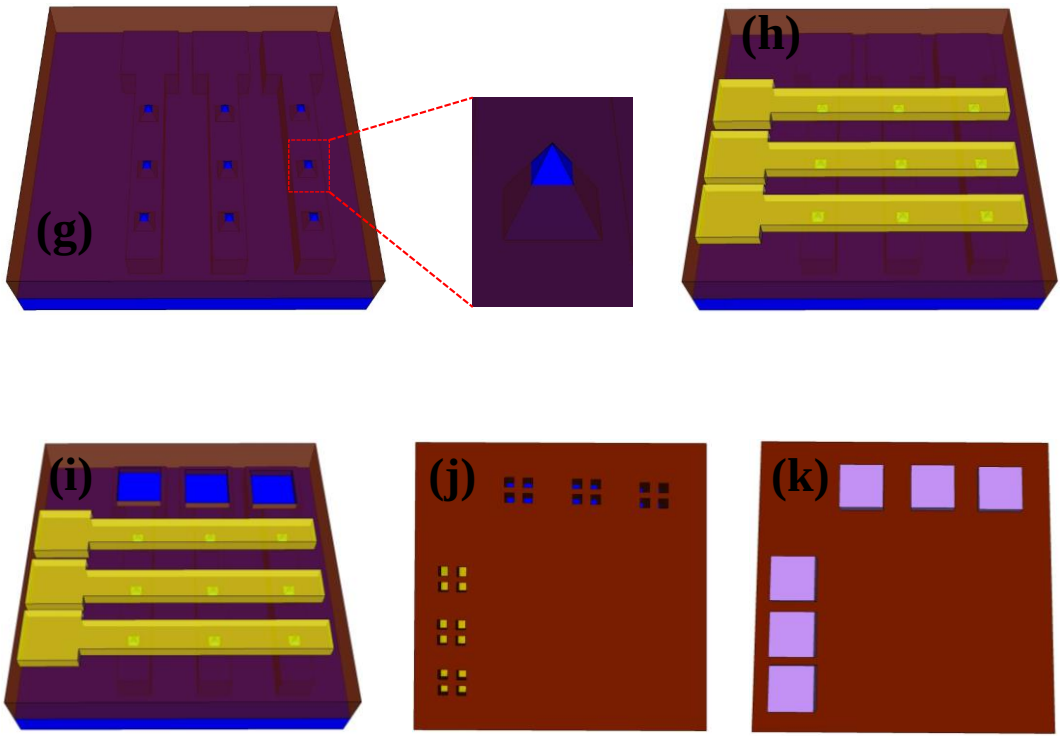
(b) Si bit-line patterning.

(c) Isolation region formation.

(d) SiO_2 hard mask patterning.

(e) Nano-cone formation.

(f) Ion implantation for heavily doped p^+-Si.



(g) Reduction of cone tip size.

(h) SL and TE deposition and metal word-line patterning.

(i) Oxide etch for Si opening.

(j) Contact hole formation.

(k) Pad formation.

4.3.2 Anisotropic Wet Etch

In order to form Si nano-cone, anisotropic wet etching is conducted. It is well known that Si etch rate has dependence on crystal orientation [52, 53]. Etch rates on (100) and (110) oriented surfaces are 37 and 68 times faster than that on (111) oriented. Table 4.2 shows the etch rates of Si(100), Si(110), Si(111), Si_3N_4, and SiO_2 using 25 % TMAH solution at 80 ℃. Because the etch rate of SiO_2 is much slower than that of Si, SiO_2 is used as a hard mask for wet etch. After patterning the oxide upon Si, the oxide prevents the surface of Si from being etched as shown in Fig. 4.7(b).

Table 4.2 Etch rates of Si(100), Si(110), Si(111), Si_3N_4, and SiO_2 using TMAH solution at 80 ℃.

Etch rate ratio		Etch rate		
(100)/(111)	(110)/(111)	(100)	Si_3N_4	SiO_2
37	68	0.3~1 μm/min	<1 Å/min	2 Å/min

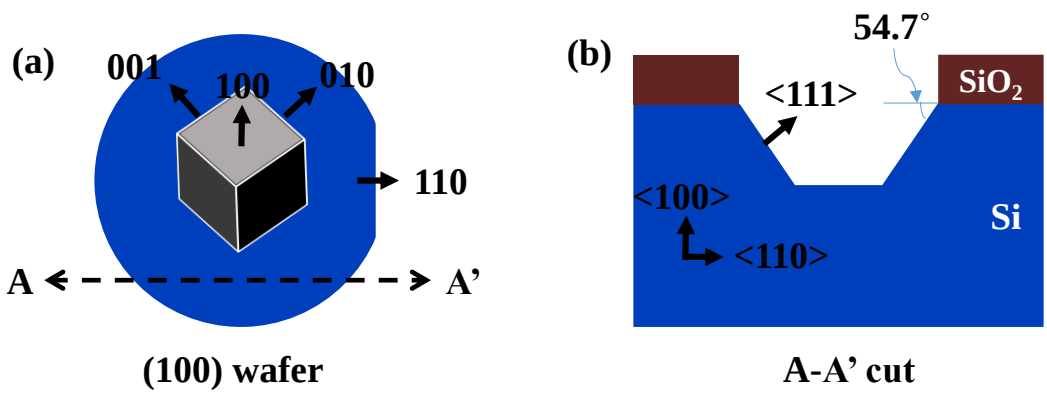


Fig. 4.7 (a) Crystal orientation of (100) Si wafer and (b) AA' cut image of Fig. 4.7(a) after Si wet etch with SiO_2 hard mask using TMAH solution.

Wet etch test sample is fabricated as described in Fig 4.8. After oxide dry etch, the SC1 + HF cleaning should be conducted for residue removal [54]. Figure 4.9 shows the top-view SEM images after Si wet etch (a) without SC1 + HF cleaning and (b) with SC1 + HF cleaning. Figure 4.10 shows the experimental setup for Si wet etch. 400 ml of 25 % TMAH solution is poured into the tray on the hot plate. After 20 minutes, we check the temperature of the solution with a thermometer. Then, the sample is submerged into the solution during specific wet etch time.

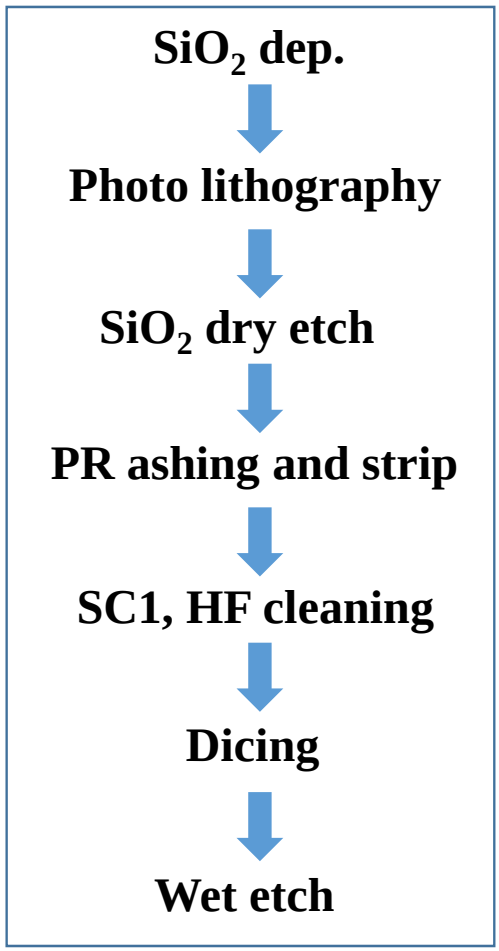


Fig. 4.8 Process flow for test sample fabrication.

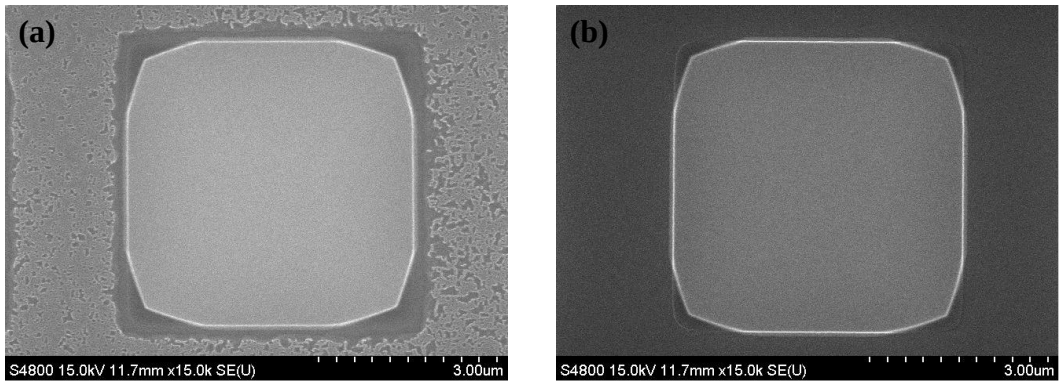


Fig. 4.9 Top-view SEM images after Si wet etch (a) without SC1+HF cleaning and (b) with SC1+HF cleaning.

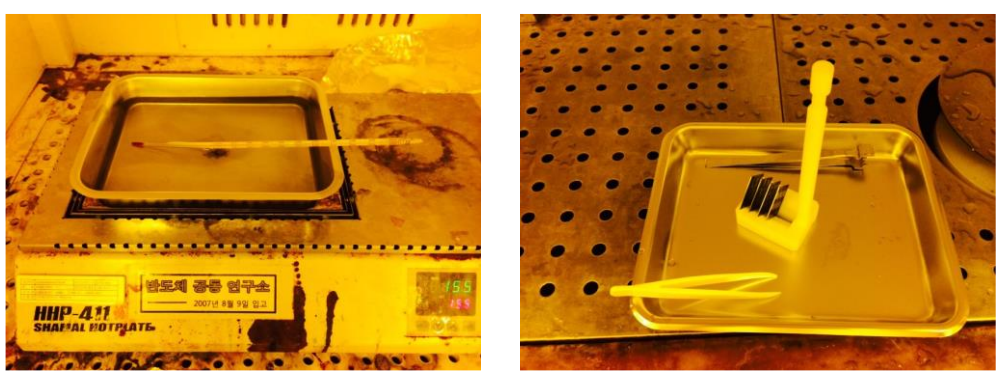


Fig. 4.10 Experimental setup for Si wet etch.

Figure 4.11 shows the etch tendency to progress in accordance with time. The slope is almost maintained with little change since the etching proceeds in the lateral direction along the crystal plane as shown in cross-sectional views of SEM images. Initially, octagonal silicon surface is formed. Over time, the shape turn into rhombic as shown in top views of SEM images. This is because Si wet etch is conducted at corner as well as side (Fig. 4.12). At corner, the etch rate in (411) plane is the fastest. As shown in Fig. 4.13, it is verified that the simulation results are quite the same as the experimental results which are obtained by Si anisotropic wet etch process with oxide hard mask. The simulation is conducted by using MATLAB tool [55]. Figure 4.14(a) shows nano-cone arrays which are successfully formed. As shown in enlarged TEM image of nano-cone tip (Fig. 4.14(b)), it is confirmed to be less than 10 nm level. A more sophisticated wet etch process can reduce the tip size further [56].

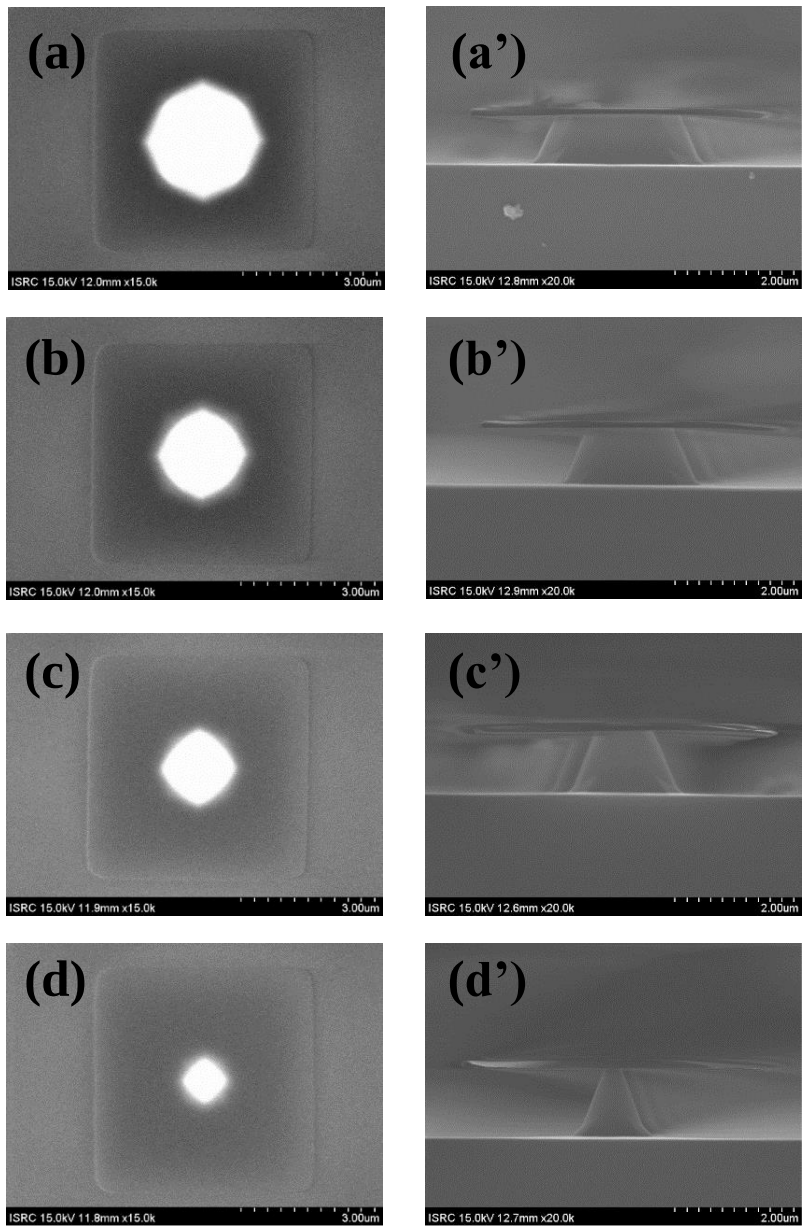


Fig. 4.11 (a)~(d) Top views and (a')~(d') cross-sectional views of SEM images of wet etch tendency to progress with time. (a) and (a') 2 min and 50 sec. (b) and (b') 3 min and 10 sec. (c) and (c') 3 min and 30 sec. (d) and (d') 3 min 50 min.

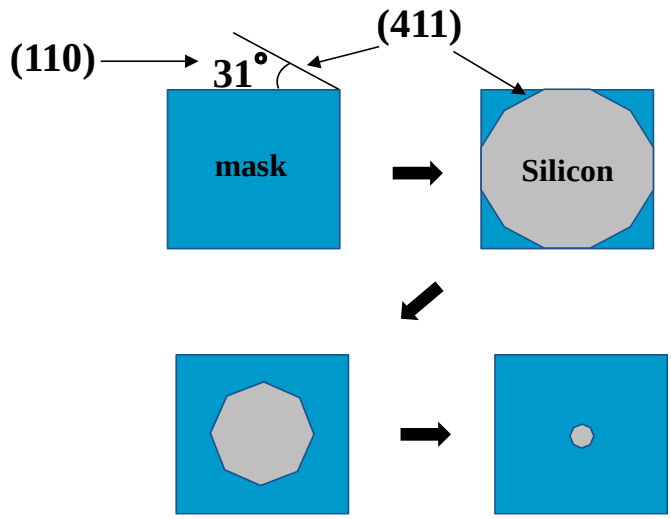


Fig. 4.12 Illustration of top views for explaining corner etch of (411) plane.

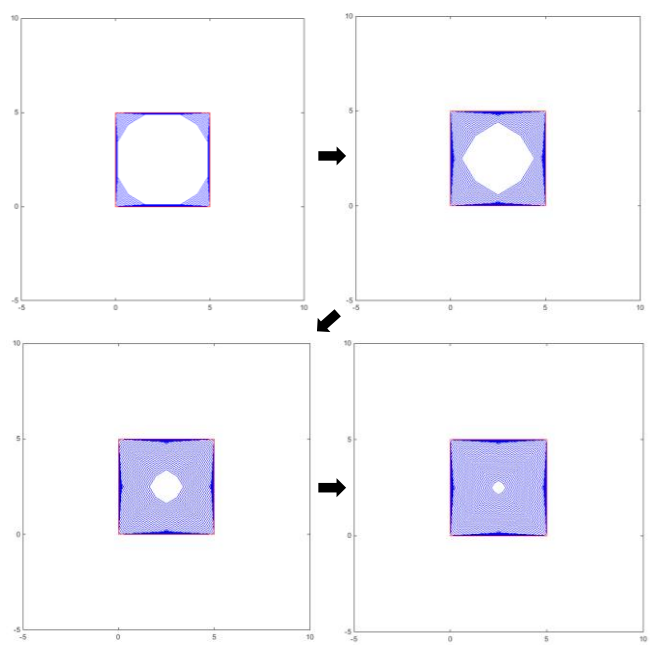


Fig. 4.13 Top views of wet etch simulation results.

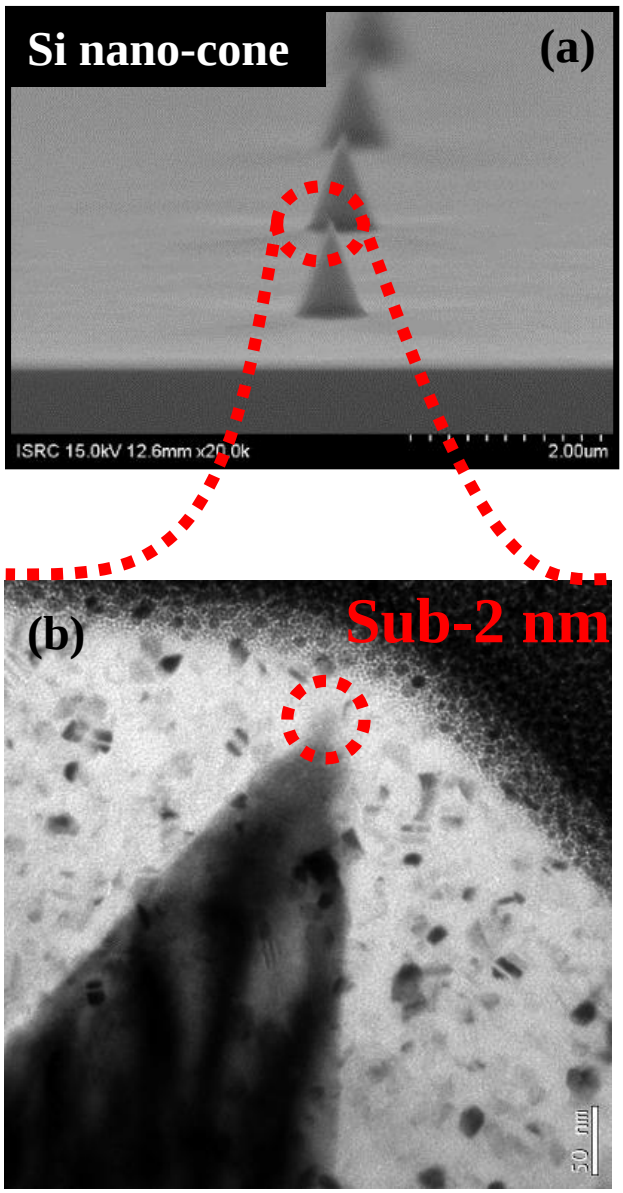


Fig. 4.14 Electron images from the fabricated nano-tips. (a) SEM images of Si nano-cone arrays. (b) Enlarged TEM image of nano-cone tip.

After formation of Si nano-cone, oxide hard mask is automatically removed without any additional process. Because the tip of Si nano-cone cannot be protected anymore, the height and slope of nano-cone decrease as the wet etch progress. In order to reduce the variation of wet etch and sustain the steep slope of Si nano-cone, there is a need to reduce the etch rate of Si. Figure 4.15 shows etch rate of Si(100) as a function of solution temperature. As the TMAH solution temperature decreases, the etch rate of Si(100) decreases. Compared to the etch rate at 80 ℃, the etch rate decreases more than 6 times at 40 ℃.

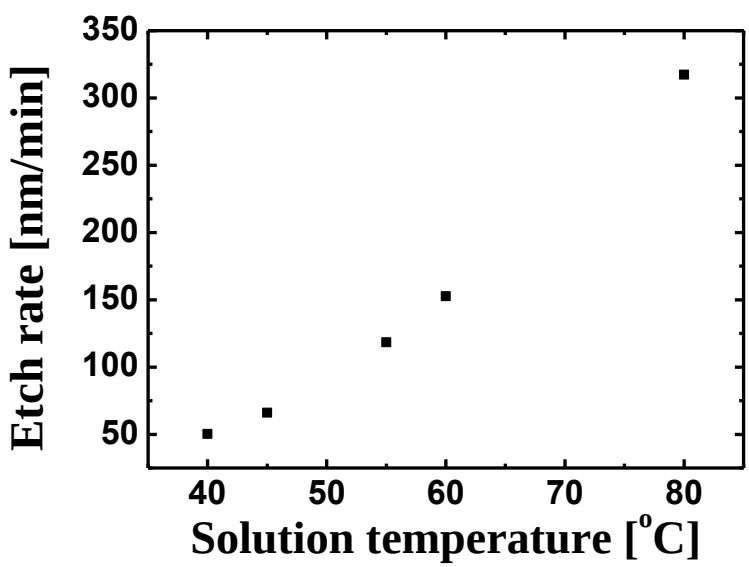


Fig. 4.15 Etch rate of Si(100) as a function of solution temperature.

4.4 Measurement Results

Figure 4.16 shows the typical *I-V* curves of Ti/Si_3N_4/p-Si stacked nano-cone RRAM device showing bipolar resistive switching behavior. Compared with the scaled cross-point RRAM, switching voltages such as forming, set, and reset voltages are reduced drastically.

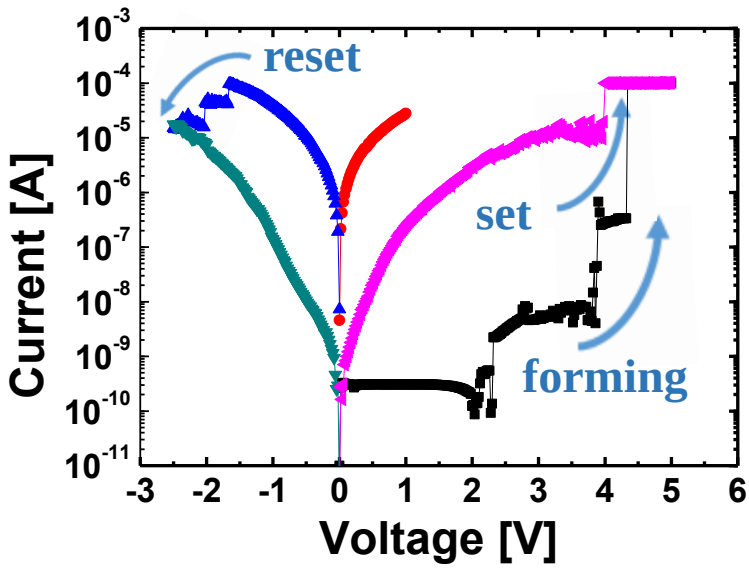


Fig. 4.16 Typical *I-V* curves of Ti/Si_3N_4/p-Si stacked nano-cone RRAM device showing bipolar resistive switching behavior.

Figure 4.17 shows the double logarithmic plot of *I*-*V* characteristics for nano-cone RRAM device, showing the SCLC conduction. In HRS, Ohmic ($V < V_{tr}$), trap filled-limited ($V_{tr} < V < V_{TFL}$), and space-charge-limited ($V > V_{TFL}$) regions are distinguishably observed. In LRS, the space-charge-limited region is not observed since the reset operation takes place at the voltage below the V_{TFL}.

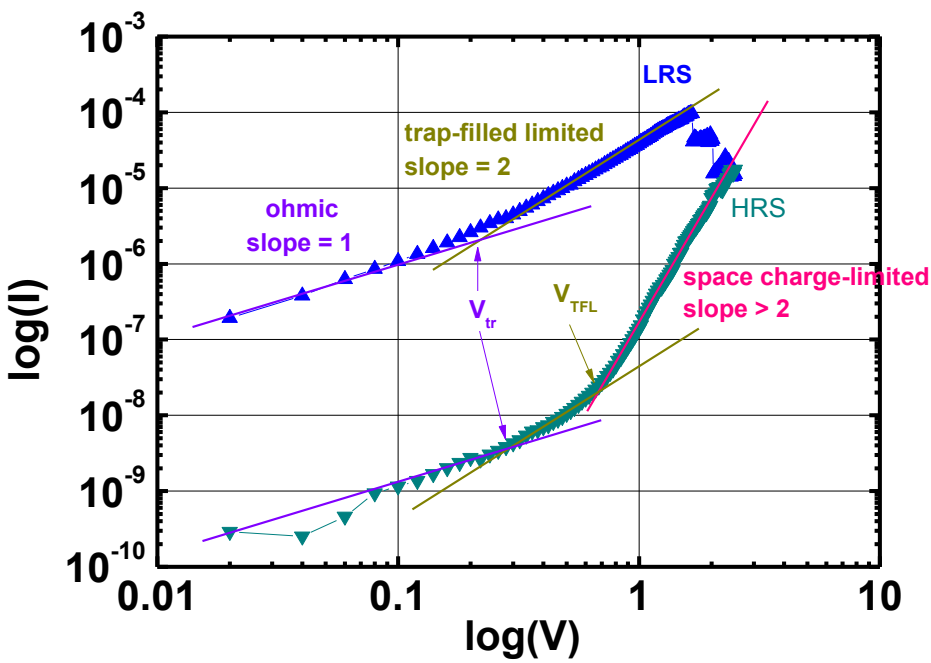


Fig. 4.17 Double logarithmic plot of *I*-*V* characteristics of the nano-cone RRAM device.

Figure 4.18 shows scaling trends of various switching parameters as a function of active area for the comparison between nano-cone RRAM and scaled cross-point RRAM. The active area of nano-cone RRAM is estimated to be about 10 nm^2 because the resistive switching occurs at the tip of nano-cone. In nano-cone RRAM, all switching voltages are dramatically reduced as shown in Fig. 4.18(a)~(c). By enhancing the electric field at the tip of nano-cone, low voltage operation can be achieved. In most cells, the reset current is nearly 100 μA which is governed by compliance current of 100 μA as shown in Fig. 4.18(d).

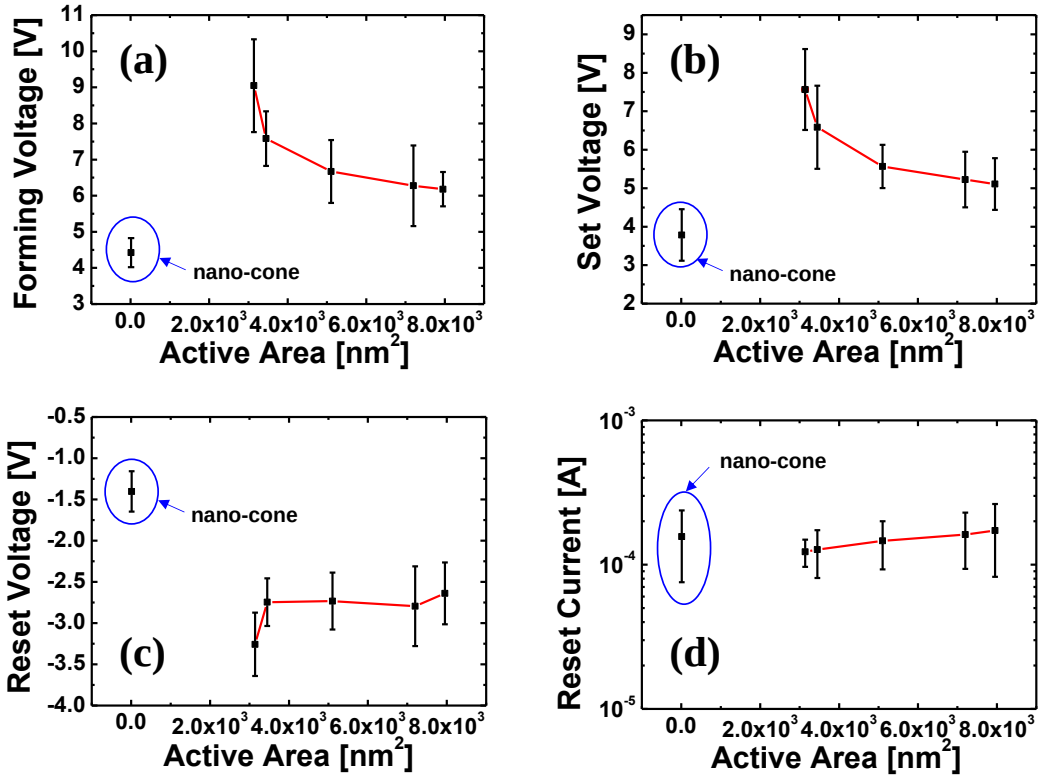


Fig. 4.18 The comparison between nano-cone RRAM and scaled cross-point RRAM. Scaling trends of various switching parameters as a function of active area. (a) Forming voltage, (b) set voltage, (c) reset voltage, and (d) reset current.

Chapter 5

Conclusions

In summary, the conduction mechanism in RRAM stack with thin Si_3N_4 resistive switching layer is investigated from *I-V* fitting and temperature measurement. We ruled out the possibility of Schottky emission and Poole-Frenkel models because these conduction models are not fitted with the experimental data. We found that trap controlled SCLC is the most probable conduction mechanism in Ti/Si_3N_4/p-Si RRAM cell. In this regard, the different *I-V* relationship between low resistance state and high resistance state in space charge region may occur due to the distribution of the nitride-related traps.

Also, we fabricate a cross-point RRAM cell, which consists of a silicon nitride-based RRAM with MIS structure. Fabrication method of the proposed RRAM array is introduced. Also, experimental results during the fabrication are presented. It is confirmed that the forming and set voltages increase as the active area of the RRAM device shrinks.

Finally, in order to improve the resistive switching characteristics, we propose the nanostructured RRAM cells, which are called nano-cone RRAM. Due to electric field concentration effect of area of nano-size, low switching voltage operation can be achieved. The proposed RRAM cell structure is expected to be a promising candidate for low power memory applications.

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초 록

다양한 모바일 기기들의 출현으로 인하여 언제 어디에서나 정보를 다룰 수 있는 환경이 조성되면서 IT 산업은 폭발적으로 성장하고 있다. 이러한 흐름에서 대용량 정보저장 장치의 수요도 함께 증가하고 있으며, 현재 3 차원 적층형 낸드 플래시 메모리의 개발이 대용량 메모리의 주류로 자리잡고 있다. 한편으로, 3 차원 적층형 낸드 플래시 메모리의 대안으로 더 빠르고, 전력을 덜 소모하고, 더 높은 집적도를 가지는 새로운 메모리에 대한 연구가 활발히 진행 중이며, 그 중에서도 저항 변화 메모리 (RRAM)가 낸드 플래시 메모리를 대체할 수 있는 후보로 각광받고 있다. 하지만, 저항 변화 메모리는 앞서 언급한 가능성에도 불구하고 높은 리셋 전류, 저항 및 동작 전압의 넓은 산포 등의 문제가 여전히 존재하여 상용화하는데 어려움을 겪고 있다. 이에 본 논문에서는 저항 변화 메모리의 구조적인 변화를 통하여 문제점을 해결하는 연구를 수행하였다.

서론에서는 저항 변화 메모리의 기본 구조와 동작 방법에 대해서 설명하

였다. 특히, 하부 전극으로 실리콘을 사용한 질화막 기반의 저항변화 메모리의 장점에 대하여 설명하였다. 그리고, 저항 변화 메모리가 갖고 있는 문제점들을 해결하기 위하여 제시되었던 방법들을 조사하였다. 우수한 특성을 보이기 위하여 최적의 물질 조합을 찾고 특수한 처리를 통하여 메모리 성능을 향상시키기 위한 시도들을 소개하였으며, 구조적인 접근을 통한 성능 향상이 근본적으로 문제를 해결하는 방법이 될 수 있는 가능성을 보였다.

먼저, 본 논문에서 실리콘을 하부 전극으로 하고 저항 변화 물질로 질화막을 사용하는 저항 변화 메모리의 기본적인 양극성 저항 변화 동작 특성 및 전류 전도 메커니즘을 분석하였고, 이 물질들을 기반으로 하는 교차형 어레이 저항 변화 메모리 소자를 최초로 제작하였다. 교차형 저항 변화 메모리 소자에서 소자의 면적에 따른 특성 변화에 대하여 분석하였으며, 소자의 면적이 점점 작아질수록 동작 전압이 커지는 문제점을 발견하였다.

따라서, 하부 전극으로 사용하는 실리콘을 습식식각으로 가공하여 나노 콘 형태를 갖는 새로운 소자 구조를 제안하였으며, 이를 교차형 어레이에 적용한 저항 변화 메모리 소자를 최초로 제작하였다. 시뮬레이션을 통하여 뾰족한 모

양의 실리콘 하부 전극에서 발생되는 전기장 집중 효과를 검증하였으며, 나노 콘의 끝 부분에서 전기장이 가장 세고 국부적으로 모이는 것을 확인하였다. 이는 제안한 소자에서 저항 변화가 발생하는 위치가 전기장이 가장 센 뾰족한 부분에 국한되며, 집중된 전기장을 통해 낮은 전압에서 저항 변화 동작이 발생될 것이라는 것을 예측할 수 있다.

마지막으로, 제안한 소자의 제작 및 측정을 통하여 낮은 전압에서의 저항 변화 현상을 성공적으로 검증하였다.

주요어: 저항 변화 메모리, 질화막, 실리콘, 교차형 저항변화 메모리, 나노 콘, 전기장 집중 효과

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