공학박사 학위논문

Self-Assembled Interface and Materials Engineering for Solution Processed ZnO Thin Film Transistors

용액형 산화아연 반도체 박막 트랜지스터를 위한 자기 조립 계면과 소재 공정에 관한 연구

2015년 8월

서울대학교 대학원

융합과학부 나노융합전공

김 경 준

Self-Assembled Interface and Materials Engineering for Solution Processed ZnO Thin Film Transistors

지도교수 김 연 상

이 논문을 공학박사 학위논문으로 제출함

2015년 7월

서울대학교 대학원

융합과학부 나노융합전공

김 경 준

김경준의 박사학위논문을 인준함

2015년 8월

위 원 장 車國憲

부 위 원 장 김 연 상 (인)

위 원 朴元哲 (인)

위 원 송 윤 수 (인)

위 원 明 在 哲 (인)

Abstract

Self-Assembled Interface and Materials Engineering for Solution Processed ZnO Thin Film Transistors

Kyongjun Kim

Program in Nano science and Technology

The Graduate School

Seoul National University

Flexible and transparent devices have attracted attention as innovative equipment that has the potential to drive the future of the information technology industry. In particular, solution processed flexible transparent thin film transistors (FTTFTs) have emerged as next generation transistors because of their applicability in an advanced process for the creation of printed transparent electronic devices. To achieve the FTTFTs, zinc oxide (ZnO) has received increasing interest as a solution-processed inorganic semiconductor, because it has high optical transparency as a wide bandgap (Eg=3.3 eV) compound semiconductor, relatively good electrical performance, and

low-temperature solution processability. However, there remain challenging problems for patterning, doping materials, and interface engineering in solution processed ZnO.

First, as the solution-processed ZnO films have a porous structure and given that ZnO reacts easily with both acidic and alkaline solvents as an amphoteric oxide, there are substantial difficulties when it comes to applying these ZnO films in conventional lithography processes. So, I demonstrated a direct patterning method with a toluene - methanol mixture to develop uniform patterned ZnO thin films with ammine-hydroxo zinc solution using a pre-patterned PMMA layer.

In addition, various metal-alloy zinc oxides, such as indium zinc oxide (IZO) and indium gallium zinc oxide (IGZO) that are still solution processable, have been introduced with good electrical performances. But it becomes a serious issue of indium (In) usage, which is becoming more expensive and scarce and thus strategic. We have developed simple alkali metals (such as Li, Na) doping method in ammonia - ZnO precursor solution, which shows excellent field effect mobility of 7.34 $cm^2V^{-1}s^{-1}$. Furthermore, in order to maximize electrical performance, a solution-processed ionic amorphous Al_2O_3 dielectric layer was using with a low temperature annealing process at 350 °C. Especially, the integrated Li - ZnO/Al_2O_3 TFTs was exhibited high field-effect mobilities of 46.9 $cm^2V^{-1}s^{-1}$.

Finally, I demonstrated a self-assembled inorganic layer (SAIL), which was fabricated by a photo-induced transformation technique of

a self-assembled PDMS mono-layer, to control the interface between a solution-processed ZnO semiconductor and polymer dielectric layers. In particular, I showed experimentally and theoretically that the SAIL between the inorganic semiconductor and the organic dielectric layer remarkably suppressed the flat band voltage (V_{FB}) shift. Also, through the adoption interface engineering into ZnO/SAIL/PVP TFTs, they showed a good flexibility and suppressive effect of interfacial traps between inorganic and organic compounds are derived by interface dipole. Also, I developed a new direct patterning method, drop-casting with a new developing method, through the combination of an aqueous ammonia - ZnO process with the doping of Na ions and surface engineering for high n-type semiconducting performance with good operational stability at low temperature as low as 100 °C.

To sum up, I have developed solution-processed alkali metals doped ZnO, solution-processed ionic Al_2O_3 dielectric layer, and new selective patterning method for the FTTFTs to achieve high-performance and low-temperature solution-processed ZnO thin film transistors. Furthermore, SAIL was effectively suppressed the shifting of flat band voltage (V_{FB}) in flexible TTFTs. These methods are easy and simple and can be applied to various fields as electronic devices.

Keywords : solution-processed zinc oxide, ionic Al_2O_3, thin film transistors (TFTs), alkali metal doping, patterning, interface engineering

Student Number : 2009-22459

Contents

List of Tables and Figures

Figure 2.6. The schematic proposed by Nomura et al. The model of crystaline and amorphous oxide semiconductor has (n-1)d10ns0 (n > 4) electron configuration explaining the high field effect mobility of amorphous phase.(adapted from 2.[1])

Figure 3.1. Schematic description of overall fabrication process(the patterned TTFT): (a) ITO-PET substrate; (b) Spin coated PVP on the ITO-PET substrate; (c) Spin coated 10 wt% PMMA on the ITO-PET substrate by 3000 rpm; (d) Stencil mask assist on PMMA layer; (e) Patterned PMMA on the ITO-PET substrate after exposure of UVO 1h; (f) Patterned ZnO on the PVP dielectric layer.

Figure 4.1. Schematic description of overall fabrication process: (a) SiO_2 substrate;(b) Spin-coated PMMA on the SiO_2 substrate; (c) Shadow mask over PMMA layer; (d) Patterned PMMA layer on the SiO_2 substrate; (e) Patterned ZnO on the SiO_2 substrate; (f) Thin film transistor with bottom gate and top contact.

Figure 4.2. Problems of ammonia based solution; (a) droping the solution on glass substrate ;(b) drying the solution on glass; (c) Tilted FE-SEM image of the matted ZnO paticles(Θ = 60°).

Figure 4.3. Cases of Optical microscopy images and SEM micrograph of patterned ZnO on a SiO_2 substrate. (a), (b) and (c) Cases of developing by toluene before the ZnO solution has dried up. (d), (e) and (f) Cases of developing by toluene after the ZnO solution has dried up solution. (g), (h) and (i) Cases of developing by toluene & methanol mixture (methanol 20 %) before the ZnO solution has dried up.

Figure 4.4. (a) The pre-patterned substrate by selective PMMA bond breakage. (b) Patterned ZnO thin films on a SiO2substrate.(c) The optical image of completed 60 TFTs by one run. Al source and drain electrodes with around 100nm thickness, 1000 μm wide with a 60 μm gap are deposited on the patterned semiconductors. (d) and (e) Cross section SEM micrograph of the patterned ZnO film. (f) A 3D AFM image of the patterned ZnO film.

Figure 4.5. Nanocrystallinity of the patterned ZnO thin film sintered at the temperature range 200 - 300 °C. High resolution X-ray diffraction (HRXRD) data of a wurtzite ZnO powder obtained through drying of the zinc-ammine precursor solution. HRXRD data were collected using a Bruker D8 Discover diffractometer (Germany) with Cu Kα radiation.

Figure 4.6. (a) The average field effect mobility of TFTs as one run at 200 °C. (b) The average field effect mobility of TFTs as one run at 300 °C.

Figure 4.7. Typical electrical characteristics for patterned ZnO-TFT with W/L ratio of 20. (a) and (b): Output and transfer curves at 200 °C. (c) and (d): Output and transfer curves at 300 °C.

Figure 4.8. Transfer curve for patterned ZnO-TFT with stable gate leakage current at 200 °C. (W/L = 20)

Figure 4.9. (a): Schematic illustration of a flexible TTFT; (b): optical image of patterned ZnO-TFT on ITO-PET; (c): Al source and drain electrodes deposited on the patterned ZnO; (d), (e): output curve and transfer curve for a patterned ZnO TFT on a PVP

ionic Al_2O_3 dielectrics were analyzed by TOF-SIMS. (e) The XPS depth profile of 350 °C annealed Al_2O_3 film. The insets indicate N1s and C1s peaks.

Figure 5.5. Leakage current density of (a) 350 °C and (b) 500 °C annealed amorphous Al_2O_3 dielectric with thickness of 242 nm and 200nm, respectively. Their values are 4.1×10^{-6}A/cm^2 and 4.6×10^{-9} A/cm^2 at 1 MV/cm, respectively.

Figure 5.6. The transmittance of ionic amorphous Al_2O_3 dielectric layers on quartz glass under UV-visible range photons. (200nm~700nm)

Figure 5.7. (a) Output curve, (b) transfer curve, and (c) count clock wise-hysteresis with 10 times sweep of Li-ZnO TFTs on ionic amorphous Al_2O_3 dielectric layer. (d) Output curve, (e) transfer curve and (f)counter clockwise-hysteresis with 10 times sweep of In-ZnOTFTs on ionic amorphous Al_2O_3 dielectric layer. The annealing temperature of ionic amorphous Al_2O_3 dielectric layer was 350 °C.

Figure 5.8. (a) Output curve of TFTs consisted of 350 °C annealed Li-ZnO semiconductor film on 500 °C annealed Al_2O_3 dielectric layer with the sweep of 10V steps on gate voltage from 0V to 50V. (b) Transfer curve of Li-ZnO/Al_2O_3 TFT with drain current of 30V. (c) Clockwise hysteresis of Li-ZnO/Al_2O_3 TFT. (d) Output curve of 350 °C annealed In-ZnO on 500 °C annealed Al_2O_3 dielectric layer with sweep of 10V steps on gate voltage from 0V to 50V. (e) Transfer curve of In-ZnO/Al_2O_3 TFT with drain current of 30V. (f) Clockwise hysteresis of In-ZnO/Al_2O_3 TFT.

Figure 5.9. Frequency vs capacitance of 500 °C annealed Al_2O_3 dielectric layer with thickness of 215 nm.

Figure 5.10. Frequency vs. capacitance of 350 °C annealed ionic Al_2O_3 dielectric layer with various film thickness designed by spin-coating counts.

Figure 5.11. The capacitance of 350 °C annealed Al_2O_3 film with MIM structure of Au/Al_2O_3/p++-Si at (a) 15, 30, 60, (b)80, 100, 120, and 150 °C thermal treatment conditions. Measured capacitance values of 350 °C annealed Al_2O_3 film under 40 RH% at 30 °C express brown color. (c) Relative impedance spectroscopic datas of 350 °C annealed Al_2O_3 film corresponding to thermal treatment conditions with fit data using equivalent circuit 1. Symbols show the observed resistance(Z‘) and reactance (Z“), and solid lines show the nonlinear least-squares fitting results by each equivalent circuit modeling. The capacitance of 500 °C annealed Al_2O_3 film with MIM structure of Aul/Al_2O_3/p++-Si at (d) 15, 30, 60,(e) 80, 100, 120, and 150°C thermal treatment conditions. Measured capacitance values of 500 °C annealed Al_2O_3 film under 40 RH% at 30 °C express brown color. (f) Relative impedance spectroscopic datas of 500 °C annealed Al_2O_3 film corresponding to thermal treatment conditions with fit data using equivalent circuit 2.

Figure 5.12. The water adsorption, desorption, and recovery characteristics of (a) 350 °C and (b) 500 °C annealed Al_2O_3films were monitored by FT-IR in ambient conditions. The peak in range of 3000-3500 cm^{-1} represents adsorbed water. To measure the water desorption behavior, 150 °C thermal treatment was conducted for 5

min and immediately measured FT-IR. The ellipsometric porosimetry measurement of (c) 350 °C and (d) 500 °C annealed Al_2O_3 films were carried out to observe the water adsorption and desorption characteristics. There fractive index of 350 °C and 500 °C annealed Al_2O_3 films were 1.542 and 1.668, respectively, at 550nm. There fractive index of water is 1.335. By using the difference between two values, water adsorption and desorption characteristics were shown.

Figure 6.1. Schematic description and HR-TEM (High-resolution transmission electron micrograph) images of solution processed oxide semiconductor on polymer dielectric layer (a) The illustration of hybrid ZnO/PVP TFT structure (b) self-assembled inorganic layer (SAIL) on PVP dielectric layer (c) HR-TEM images of solution-processed zinc oxide semiconductor on polymer dielectric layer with SAIL (d) enlarged HR-TEM image of the stacked layers.

Figure 6.2. HR-TEM images of solution processed oxide semiconductor on polymer dielectric layer were shown. (a) The poly crystalline ZnO was well deposited on the highly cross linked PVP dielectric layer as 629nm. (b) The flexible gate & substrate was fabricated with 20 nm ITO on the hard coated polyester (PET) film.

Figure 6.3. (a) Cross-sectional HR-TEM image of solution processed ZnO semiconductor on polymer dielectric layer were shown. (b) The ZnO shows crystalline FFT-SAED patterns.

Figure 6.4. (a) Contact angle change after UVO exposure on natural PVP (b) AFM image of surface of spin-coated ZnO on PVP, which facilitated UVO exposure. (c) Transfer curve of the ZnO/PVP TFT

without interface engineering (d) change in contact angle after UVO exposure on SAIL grafted PVP (e) AFM image of surface of spin-coated ZnO on SAIL grafted PVP, which facilitated UVO exposure (f) Transfer curve of the ZnO/SAIL/PVP TFT with interface engineering.

Figure 6.5. 3D views of AFM images: (a) 3D view of ZnO thin film on PVP without interface engineering (RMS=5.33 nm), (b) 3D view of intrinsic ZnO thin film on PVP with interface engineering (RMS= 2.92 nm)

Figure 6.6. Voltage-dependent capacitance of both the SAIL coated PVP and the intrinsic PVP at 100 kHz.

Figure 6.7. Hysteresis and repeated transfer characteristics of SAIL grafted ZnO/PVP TFT with W/L ratio of 20 (g) Hysteresis-transfer curves of SAIL grafted ZnO/PVP TFT after sintering at 200 °C (h) Repeating transfer curves of SAIL grafted ZnO/PVP TFT 20 times after sintering at 200 °C

Figure 6.8. Cross-sectional SEM images of polymer dielectric layers were shown. (a) The spin coated PVP has 598 nm at 2000 rpm. (b) The spin coated TPC has 137 nm at 2000 rpm. (c) The spin coated double dielectric layer has 615 nm that TPC was spin coated at 2000 rpm on the spin coated PVP at 2000 rpm.

Figure 6.9. Typical electrical characteristics of 200 °C annealed ZnO/ 200 °C annealed PVP and TPC TFTs with W/L ratio of 20 (a) Output curve with 12V steps of gate voltage from 0V to 60V. (b) Transfer curve with drain current of 60V.

Figure 6.10. The transfer curves were fit with simulation using the explicit analytic model for nanocrystalline ZnO TFTs. (a) The measured hysteresis test of SAIL grafted ZnO/polymer TFT was compared with simulation of SAIL grafted TFT. (b) The measured hysteresis test of ZnO/polymer TFT without interface engineering was compared with the simulation of ZnO/polymer TFT.

Figure 6.11. The changes in on - off current (a), field effect mobility (b), and threshold voltage (c) were measured as flexible devices during compressive and tensile bending. The bending radius was determined from flat condition to 20~10 mm compressive and tensile bending by the bend support plates.

Figure 6.12. Optical spectroscopy images: (a) the ITO PET before bending; (b) the ITO PET after bending. (C) The ZnO/SAIL/PVP TFT was shown reliable flexibility without any delamination after bending.

Figure 7.1. Schematic description of the solvent reaction between methanol and the ammonia-ZnO precursor solution: (a) aqueous zinc ammonia complexes form by resolving in ammonia water, (b) changes of the ZnO precursor solution after the decrease in the pH via methanol, (c) $Zn(OH)_2$ formation by a continual pH decrease and methanol absorption of the residuals of ammonia and water, (d) ZnO formation by the thermal decomposition of $Zn(OH)_2$.

Figure 7.2. Optical microscopy images were magnified by a factor of 40. Cross-section and tilted(Θ = 45°) FE-SEM microscopy images of patterned ZnO on a SiO_2 substrate. a - c) Drying of the solution in

the air without methanol. d-f) Direct sintering of the solution in the air without methanol. g-i) developing of the solution with de-ionized water.

Figure 7.3. Schematic description of a PDMS layer coated onto the surface of the substrate: (a) PDMS coated onto a SiO_2 substrate,(b) UVO exposure through a shadow mask to generate selective hydrophilic regions.

Figure 7.4. Schematic description of the overall fabrication process: (a) PDMS thin layer coated onto a SiO_2 substrate, (b) selective photo induced transformation of the PDMS layer through a shadow mask by UVO exposure,(c) selective hydrophilic regions onto hydrophobic regions,(d) dropping of the ZnO precursor solution onto the substrate, (e) casting of the ZnO precursor solution from the substrate,(f) dipping in methanol with sonication, (g) uniformly patterned ZnO semiconductors on the SiO_2 substrate,(h) fabrication of a thin film transistor with bottom gate and top contact.

Figure 7.5. (a) Images of selective hydrophilic regions on the substrate, (b) an image of patterned ZnO semiconductors on the substrate, (c) optical microscopy images magnified by a factor of 40, (d) a cross-section image of patterned ZnO films imaged by a field emission scanning

electron microscope (FE-SEM) on a SiO_2 substrate, (e) a tilted (Θ = 45°) FE-SEM image of the upper surface as observed to probe the macroscopic crystalline formation.

Figure 7.6. The optical microscopy(OM) images of various ZnO thin

films, which fabricated by one run; (a) and (b) OM images of patterned ZnO thin films magnified by a factor of 40; (c) Enlarged OM image of side part of the patterned ZnO thin film magnified by a factor of 500.; (d) and (e) OM images to show the part of the gap between patterned ZnO thin films magnified by a factor of 40; (f) Enlarged OM image of side part of the patterned ZnO thin film magnified by a factor of 500.

Figure 7.7. Top views and 3D views of AFM images: (a) The sobel transform image of intrinsic ZnO thin film (RMS=1.261 nm), (b) 3D view of intrinsic ZnO thin film, (c) The sobel transform image of Na-doped ZnO thin film (RMS=1.121 nm), (d) 3D view of Na-doped ZnO thin film.

Figure 7.8. The oxygen (O) 1s peaks of the intrinsic/doped ZnO film in the temperature range of 100 - 300 °C sintering on a SiO_2 substrate, as measured by X-ray photo electron spectroscopy(XPS): (a) XPS O1s peaks of a patterned intrinsic ZnO TFT in the temperature range of 100 - 300 °C, (b) XPS O1s peaks of a patterned Na-doped ZnO TFT in the temperature range of 100 - 300 °C.

Figure 7.9. Analysis of the relative oxygen intensity (1s) and mobility changes of intrinsic/doped ZnO film transistors in the sintering temperature range of 100 - 300 °C on a SiO_2 substrate:(a) Relative mobility changes, (b) relative comparison of the oxygen intensity (1s) related to oxide lattices in the XPS data, (c) relative increment of the oxygen intensity (1s) related to oxide vacancies in the XPS data.

Abbreviations

TFT Thin film transistor

FET Field effect transistor

TTFT Transparent thin film transistor

FTTFT Flexible transparent thin film transistor

Al Aluminium

In indium

Ga gallium

T tin

Zn Zinc

ZnO Zinc oxide

InO indium oxide

IGZO indium gallium zinc oxide

IZO indium zinc oxide

ZTO zinc tin oxide

Al_2O_3 Aluminum oxide

LiOH Lithium hydroxide

UVO Ultraviolet ozone

IPA Isopropyl alcohol

PVP poly(4-vinylphenol)

c-PVP cross-linked poly(4-vinylphenol)

PMMA poly(methyl methacrylate)

PDMS poly(dimethylsiloxane)

SAIL self-assembled inorganic layer

TPC TiO_2-polymer composite

APTES 3-(aminopropyltriethoxysilane)

PGMEA propylene glycol monomethyl ether acetate

IPA isopropyl alcohol

UVO ultraviolet-ozone

DI de-ionized

S/D source and drain

I_{on} on-current

I_{off} off-current

V_D drain voltage

V_T threshold voltage

C capacitance

R resistance

SS subthreshold swing

CBB conduction band bottom

AM active matrix flat

FPD flat panel display

OLED organic light emitting diode

ESL etch stopper layer

BCE back channel etch

FHD full high definition

MIM Metal-Insulator-Metal

LC liquid crystal

LTPS low temperature poly-silicon

PET polyethylene terephthalate

PEN polyethylene naphthalate

PES polyethersulfone

PC poly carbonate

PI polyimide

TSOs transparent semiconducting oxides

Chapter 1. Introduction

The transparent thin-film transistor (TTFT) has grown in importance in the display industry because flexible and transparent displays are drawing attention as the next-generation display component. In order to achieve the TTFT, the development of transparent semiconducting materials have been intensively researched. Of prime importance is zinc oxide (ZnO), a material with extensive application in the industry. ZnO is a wide bandgap (Eg=3.3 eV) compound semiconductor with a large exciton binding energy (60 meV).[1] It has a wide range of electrical properties through doping.[2-5] Therefore, ZnO has been applied to gas sensors,[6] conducting films,[7,8] luminescent materials,[9] and transparent electrodes.[10-12] Recently, solution processed ZnO has seized the limelight and pointed toward a significant integration as the active channel in the TFT, unlike silicon-based electronics.[13,14]

In Chapter Ⅱ, literature review and theories about metal oxide based TFT are described to understand these studies with detailed depiction of device structures, operation, materials property, trends and issues. Especially, impotance of patterning, doping, and interface engineering are considered in this Chapter.

In Chapter Ⅲ, all detailed experimental used in this dissertation, such as material synthesis, patterning, device fabrication and characterization, are described to comprehend the process.

In chapter Ⅳ, I propose a patterning method using binary solvent

mixture and unconventional lift off method for the solution processed ZnO.[15] The major driving force behind solution-processed zinc oxide film research is its prospective use in printing for electronics. Since patterning that prevents current leakage and crosstalk noise is essential when fabricating TTFTs, the need for sophisticated patterning methods is critical. When patterning solution-processed ZnO thin films, several points require careful consideration. In general, as these thin films have a porous structure, conventional patterning based on photolithography causes loss of film performance. In addition, as controlling the drying process is very subtle and cumbersome, it is difficult to fabricate ZnO semiconductor films with robust fidelity through selective printing or patterning. Therefore, we have developed a simple selective patterning method using a substrate pre-patterned through bond breakage of poly(methyl methacrylate) (PMMA), as well as a new developing method using a toluene-methanol mixture as a binary solvent mixture.

In chapter Ⅴ, semiconductor and gate dielectric are essential in the building of TFTs. In order to promote the potential of solution processed metal oxide TFTs, the considerable effort for high performance gate dielectrics, as well as that for metal oxide semiconductors, is indispensable. For these reasons, several alternative dielectrics with solution processability and high electrical performance, such as ion gel, self-assembled layer, polymer electrolyte, perovskite materials, have been introduced. In particular, the ion gel dielectrics showed remarkable performance in TFTs. However, ion gel dielectrics

don't show a good compatibility with metal oxide semiconductor. In addition, they are quite fragile in high temperature processes and hinder the further deposition process. Herein, we introduce the simple solution process for the high electrical performance TFTs with a low temperature annealing process as maximum as 350 °C using the combination of nitrate ion (NO_3^-) coordinated amorphous Al_2O_3 dielectrics and ZnO-based semiconductors.[16] The proton mobile ion, such as hydrogen ion (H^+) from chemisorbed water, in solution-processed ionic Al_2O_3 dielectric induce remarkably a high capacitance by formation of electrical double layer. These ionic amorphous Al_2O_3 dielectrics show a good potential as switching TFTs device in advanced displays.

In chapter Ⅵ, In order to achieve the stable FTTFTs, solution processes of organic and inorganic compounds have received significant attention. Above all, an integration of ZnO semiconductor and organic dielectrics is most suitable composition of thin film transistor to enhance flexibility with high electrical performance. However, interfacial traps between inorganic and organic compounds are derived by interface dipole, which affected flat band shift. Thus, I developed a self-assembled inorganic layer (SAIL) via the photo-induced transformation of a mono poly(dimethylsiloxane) (PDMS) layer as an interface engineering.[17] Especially, flat band shift was effectively suppressed by SAIL process that was proved by an analytic model of nanocrystalline ZnO-based TFTs with the flat-band voltage (V_{FB}) shift.

In chapter Ⅶ, I introduce a new direct patterning method as an application of interface engineering, drop-casting with a new developing method, through the combination of the aqueous ammonia-ZnO process with the doping of Na ions and interface engineering for high n-type semiconducting performance with good operational stability at low temperature.[18] In particular, the effective decomposition and removal of the residual ammonia compounds using methanol had successfully effect on both intrinsic and Na doped ZnO precursor processes for TFT and they showed the extensive possibility of ammonia based metal oxide precursor solutions. In this method, the Na doped ZnO TTFTs showed good operational stability even at the process of low temperature sintering. In ambient conditions, the patterned Na doped ZnO TTFT exhibited high electron mobility μ = 1.84 $cm^2v^{-1}s^{-1}$ with excellent device operational stability and scant hysteresis with sintering at 300°C. This method is not only simple as compared with photolithography and inkjet printing, but is also a sophisticated patterning process with good fidelity for solution-processed ZnO TFT. Moreover, as the proposed method can be extended to the plastic substrates on a large scale because of the low temperature development process of ammonia-ZnO precursor using methnol and continuous patterning at ambient conditions.

Finally, in chapter Ⅷ, the overall conclusion of this dissertation is presented.

1.1 References

[1] U. Ozgur, Ya. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. J. Cho , and H. Morkoc, Appl. Phys. Rev. 2005, 98, 041301.

[2] K. Ip, G.T. Thaler, Hyucksoo Yang, Sang Youn Han, Yuanjie Li, D.P. Norton, S.J. Pearton, Soowhan Jang, F. Ren, Journal of Crystal Growth. 2006, 287,149 - 156.

[3] Myung-Gil Kim, Hyun Sung Kim, Young-Geun Ha, Jiaqing He, Mercouri G. Kanatzidis, Antonio Facchetti, and Tobin J. Marks, J. Am. Chem. Soc. 2010, 132, 10352 - 10364.

[4] A. Tsukazaki, A. Ohtomo, T. Onuma, M. Ohtani,T. Makino, M. Sumiya, K. Ohtani, S. F. Chichibu, S. fuke, Y. Segawa, H. Ohno, H. Koinuma, and M. Kawasaki, nature materials. 2005, 4 , January.

[5] Z. Jin, T. Fukumura, M. Kawasaki, K. Ando, H. Saito, T. Sekiguchi, Y. Z. Yoo, M. Murakami, Y. Matsumoto, T. Hasegawa, and H. Koinuma, Appl. Phys. Lett. 2001, 78, 24.

[6] Q. Wan, Q. H. Li, Y. J. Chen, T. H. Wang, X. L. He, J. P. Li, C. L. Lin, Appl. Phys. Lett. 2004, 84, 18.

[7] X. Jiang, L. Wong, M. K. Fung, and S. T. Lee, Appl. Phys. Lett. 2003, 83, 9.

[8] T. Minami, T. Miyata, and T. Yamamoto, J. Vac. Sci. Technol. 1999, A 17.4.

[9] B. Lin, Z. Fu, and Y. Jia, Appl. Phys. Lett. 2001, 79, 7.

[10] X. W. Sun, and J. X. Wang, Nano Lett. 2008, 8, 7.

[11] H. Rensmo, K. Keis, H. Lindstrom, S. Sol1dergren, A. Solbrand,

A. Hagfeldt, and S.-E. Lindquist, J. Phys. Chem. B. **1997**, 101, 2598-2601.

[12] J. Meyer, P. Görrn, S. Hamwi, H.-H. Johannes, T. Riedl, and W. Kowalsky, Appl. Phys. Lett. **2008**, 93, 073308.

[13] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature. **2004**, 432 , 25.

[14] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. **2008**, 130, 51.

[15] K. Kim, S. Park, J. B. Seon, K. H. Lim, K. Char, K. Shin and Y. S. Kim, Adv. Funct. Mater. **2011**, 21, 3546.

[16] J. H. Park, K. Kim, Y. B. Yoo, S. Y. Park, K. H. Lim, K. H. Lee, H. K. Baik and Y. S. Kim, J. Mater. Chem. C, **2013**, 1, 7166.

[17] K. Kim, E. Lee, J. Kim, S. Y. Park, K.-H. Lim, C. Shin, Y. S. Kim, J. Mater. Chem. C, **2013** , 1 , 7742.

[18] K. Kim, S. Park, K. H. Lim, C. H. Shin and Y. S. Kim, J. Mater. Chem., **2012**, 22, 23120.

Chapter 2. Literature review and Theories

2.1 Thin Film Transistors: Definition and its theories

TFT(thin film transistor) is general field effect transistor that is created by connecting semiconductor layer on the dielectric layer. TFT is consist of gate, semiconductor, dielectric layer, source and drain(S/D) electrodes, which is used for switching device in display. Drain current between source and drain electrodes is controlled to on-current (I_{on}) or off-current (I_{off}) for switching of pixel.(**Figure 2.1**) Nevertheless, TFT being applied to sensor, memory device, and optical device, the main realm of TFT is switching device in active matrix(AM) flat panel display (FPD). Each TFTs in the AM FPD are operated to modulate on/off, and change brightness of pixel. Conventionally, amorphous silicon(a-si) based TFT have widely used in the AM FPD. However, the oxide based TFT is emerged as next generation TFT by its optical transparency and high electrical conductivity. The detailed explanation of developing TFT issues will be discussed in following chapter.

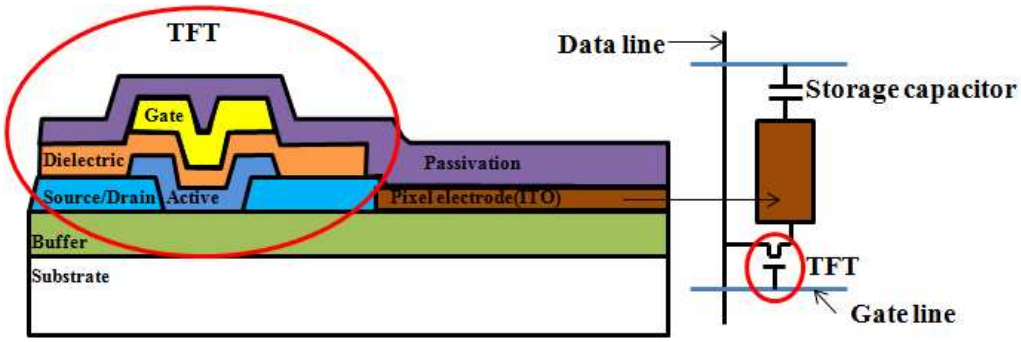


Figure 2.1. Cross sectional diagram of TFT used in LCD flat panel display and it's a circuit diagram.

2.1.1 Structure of Thin Film Transistor

The most common oxide TFT structures are represented in **Figure 2.2**. Depending on whether the S/D are on the same side or on opposite sides of the semiconductor, the structures are identified as coplanar and staggered. In addition, the top- and bottom gated structures, which are desided as whether the gate electrode is at the top or bottom of the dielectric layer. In a device structure of top gated TFT (top gate: staggered and top gate: self align), overlap between S/D and dielectric is minimized size of S/D due to possibility of pre-pattern formation of electrodes. It is issued by needs of high definition display using oxide TFT.

To achieve high definition and large area display, the oxide thin film transistor is needed to minimize RC delay in a circuit. R is resistance of data/gate electrodes and C is parastic capacitance. The electrical signal produced potential drop when the electric signal passed TFT as amount of multiply R by C. C is decided by capacitance of dielectric layer and overlap capacitance between S/D electrodes. The less resistance of data/gate electrodes and the smaller parastic capacitance in TFT are best in minimization of RC delay. Because TFT depends on the overlap degree between gate and S/D electrodes and capacitance of gate insulator film, the less overlap between electrodes and the smaller cap of gate insulator are the most desired.

The etch stopper layer (ESL) TFT is far more unique structure than bottom gate(staggered): back channel etch(BCE) of TFT. Because oxide semiconductor is easily degraded by developing process

in wet or dry photolithography. So, the ESL effectively protect the damage of oxide material. This structure has been briskly used in full high definition (FHD) AM organic light emitting diode (OLED) display due to stable electrical performance of oxide TFT.

However additional mask process that is caused by ESL pattern formation is more required in ESL TFT and according to the **Figure 2.2**, overlap is the largest structure between gate electrode and S/D electrodes. Nevertheless, the oxide TFT structure has been studied for many years the ESL structured TFT has obtained best electrical reliability. The case of driving oxide TFT of OLED has more competitive in electrical characteristics and cost reduction than low temperature poly-silicon (LTPS) TFT if the simplicity of the process and accessibility of large area fabrication are satisfied. Although the structures of self aligned oxide TFT and LTPS TFT are similar, the case of self alighed oxide TFT are many advantages in what is lower temperature process than LTPS TFT and having super structure in a strong stability. Also, doping activation process of semiconductor in memory device is rarely needed for the self alighed oxide TFT. The metal electrodes deposition process in oxide TFT needs only verification of technology as the process is not stable. First and most importantly, despite the identical structure is BCE structure for LC-FPD, oxide TFT is needed to present superior electrical characteristics than a-Si TFT. The high electrical performance is because of possibility of fine pattering and an appropriated structure to reduce parastic capacitance. But higher

electrical performance than ESL TFT cannot be shown and active channel layer is exposed during S/D patterning process. Consequently development for minimizing damage of oxide semiconductor is actually required. In most cases, developing solvents of photolithography are H_2O_2 based etchant, however, the basic solvents are easily dissolved the ZnO based semiconductor layer. For these reasons, consideration of several new patterning methods for the oxide TFT have emerged over the past few years.

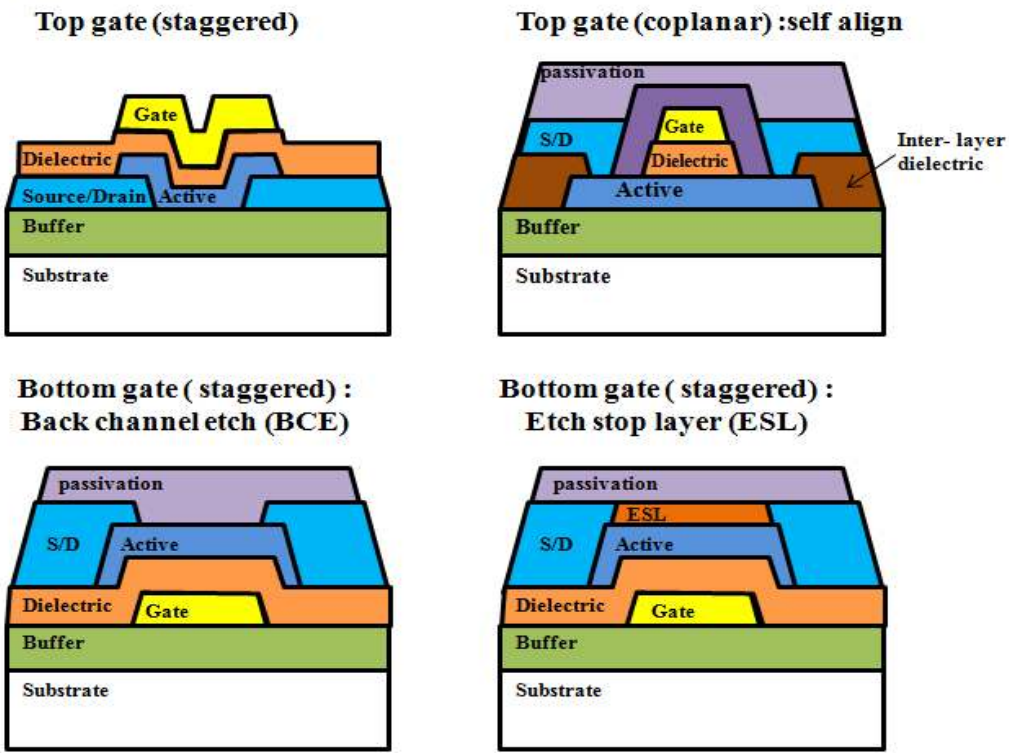


Figure 2.2. Typical device structures of oxide TFTs.

2.1.2 Operation of Thin Film Transistor

The working principles of TFT depend on the current flowing between source and drain electrodes. The current is called “Drain current (I_D)”. Dielectric layer is inserted between semiconductor and gate electrode as a gate insulator, which induced charges at the interface between semiconductor and dielectric layer by modulating gate bias. **Figure 2.3** represented simple N-type semiconductor based TFT structure with the central elements, which are gate/drain voltage(V_G and V_D) and charge polarities. Under threshold gate voltage (V_T), the depletion layer is formed near the interface that means being rarely mobile charge carriers as off state.($V_G < V_T$) On the other hand, charge carriers accumulated at the interface between semiconductor and dielectric layer when positive gate voltage is pulsed over V_T.($V_G \geq V_T$) Applying positive drain voltage (V_D), it leads I_D flow as on state. At higher V_G than V_D, the saturation of I_D is derived from the depletion of semiconductor near the drain region, which is called “pinch-off”. $C_{GS,overlap}$ and $C_{GD,overlap}$ are parasitic capacitance, which induced by capacitive effect of dielectric layer between gate and source/drain electrodes. To reduce the parasitic capacitance, the TFT is minimized overlap distance as gate to source or drain electrodes. Reducing the parasitic capacitance can improve the driving speed of the device. The parameters of operation are given a detailed account at Chapter 2.1.3.

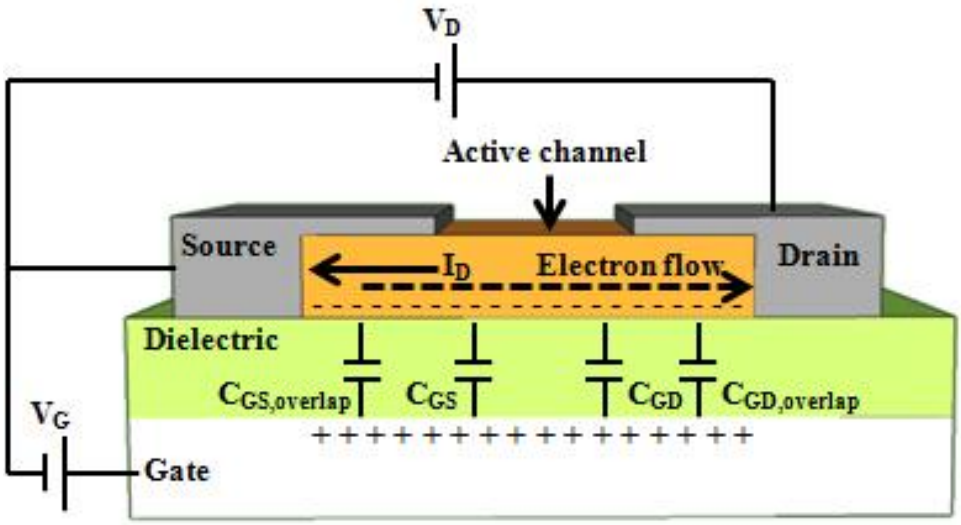


Figure 2.3. Schematic illustration of the elements in operating TFT.

2.1.3 Parameters of Thin Film Transistor

Generally, the electrical characteristics of TFT are evaluated from field effect transistor (FET) theory. Between threshold voltage and pinch-off regime, which is linear regime, for $V_D<V_G-V_T$, the I_D is described by Equation 1.

$$I_D = \frac{W}{L}\mu_{lin} C_i\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right] \quad (1)$$

where I_D and V_D are the drain current and drain voltage, between source and drain electrodes; W is the device width; and L is the channel length; V_G is the voltage between the gate and source reference electrode; V_T is the saturation threshold voltage; μis the device field effect mobility; C_i is the gate dielectric capacitance per unit area; μ is the channel mobility. Also, the W, L is determined by width and length between source and drain electrodes in **Figure 2.4.** From post pinch-off, which is saturation regime, for $V_D>V_G-V_T$, the I_D is described by Equation 2.

$$I_D = \frac{W}{2L}\mu_{sat} C_i(V_G - V_T)^2 \quad (2)$$

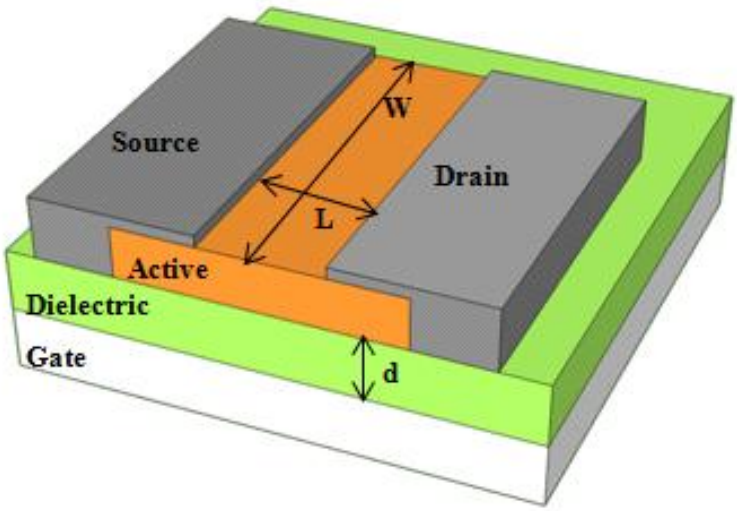


Figure 4. Schematic depiction of TFT structure.

While this expression may not provide quantitative agreement with TFT devices that deviate substantially from one or more of the relevant model assumptions, it nonetheless comprises a useful qualitative basis for understanding the key elements of TFT operation.

In order to determine the electrical performances of TFT, field effect mobility, on/off current ratio, subthreshold swing, capacitance of dielectric layer, and carrier concentration are significantly featured using output and transfer characteristics.(**Figure 2.5**) The mobility(μ_{sat}) in the saturation region was calculated from the following Equation 3 and 4, which is derived from Equation 2.

$$I_D^2 = \sqrt{\frac{W}{2L}\mu_{sat}C_i}(V_G - V_{th}) \quad (3)$$

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right) \quad (4)$$

To calculate the exact value, the transfer characteristic is deeply considered like **Figure 2.5(b)**. Also, on-off current ratio can be derived from the transfer characteristic, which is by plotting log I_D versus V_G.(**Figure 2.5(b)**) subthreshold swing(SS) represented the inverse of the maximum slop of the transfer characteristic, it indicates the required V_G to increase I_D by one decade. The SS is

described by Equation 5.

$$S = \frac{\partial V_D}{\partial(\log_{10} I_D)} \quad (5)$$

The capacitance of dielectric layer is expressed by Equation 6.

$$C = \epsilon_0 k \frac{A}{d} = \epsilon_0 \epsilon_r \frac{A}{d} \quad (6)$$

Where the C is the capacitance; ε_0 is the electric constant ($\varepsilon_0 \simeq 8.854\times10^{-12}$ F m^{-1}); ε_r is the relative static permittivity, which can be called as dielectric constant as k; A is the area of the active channel layer; d is the thickness of the dielectric layer (Figure 4). From the parameters, $I_{D,sat}$ can be maximized by reducing L, higher μ of TFT, and maximizing C.

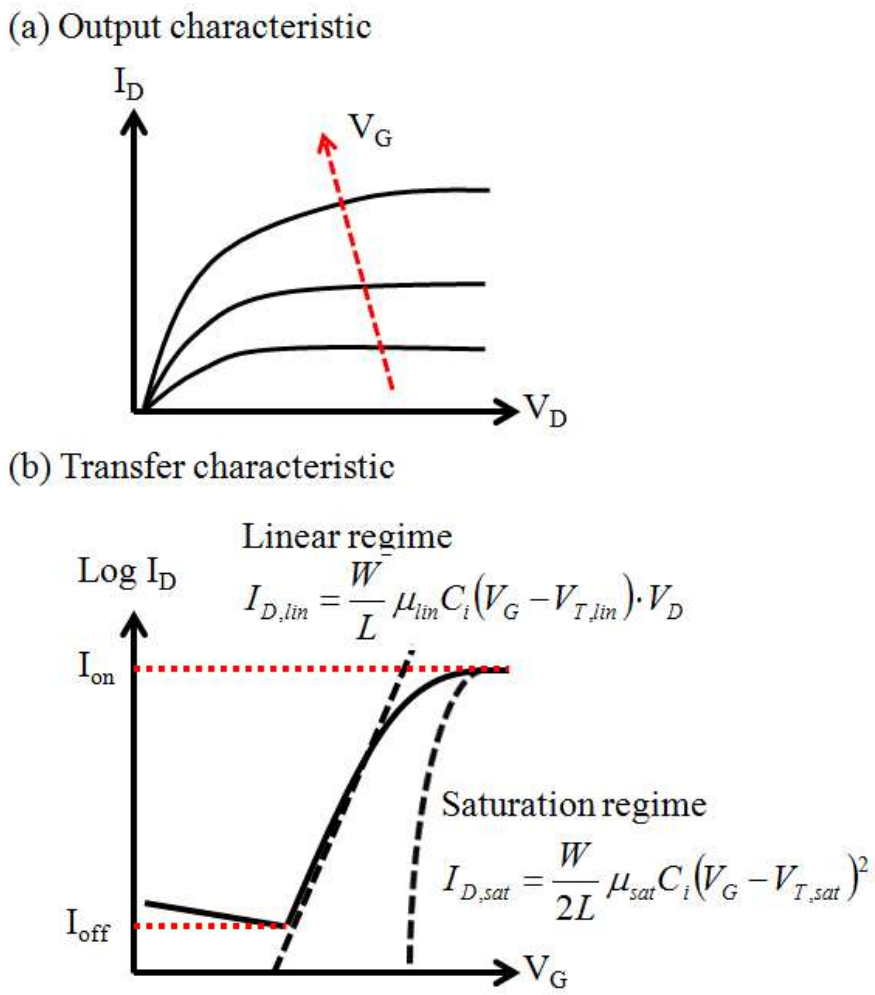


Figure 2.5. Common (a) output and (b) transfer characteristics of operating oxide TFTs.

2.2 Trends and issues of Thin Film Transistor

The transparent device is spreading rapidly to the whole industry expecting of changing the display. For instance, ultra-mobile PCs, smart windows, transparent tablets, and paper-thin displays are notable examples using that technology. In particular, one anticipated application is the smart window. The smart window could transmit visual information onto the windshields of automobiles and airplanes. The use of transparent window displays has no limitation in space and visibility. Therefore, the transparent device has the potential to drive the future of the IT industry. From a technological standpoint, advances in transparent devices mean an increase the beam transmittance to enhance aperture ratio. Higher transmittance of the thin film transistor (TFT) allows penetration of back light and improves power consumption efficiency. In addition, as operation of high-precision fine pixel is needed in order to achieve high definition display, oxide semiconductor based TFT is highly favoured in fabricating TFT by remarkable electrical property. In general, the oxide material has high optical transparency in the visible range and high electrical conductivity. Thus, the oxide TFT can be applied to transparent TFT using its wide band gap (E_G > 3 eV), it leads to transparent property in visible range.

In the issue of flexible TFT, the methods can be achieved using two tries using transfer and direct deposition on the flexible substrate. The flexible substrate is widely used by plastic substrates. The most representative flexible substrate is polyethylene

terephthalate (PET), polyethylene-naphthalate (PEN), polyether-sulfone (PES), poly carbonate(PC), and polyimide(PI). Although the PI being yellow color in visible range unlike other transparent plastic substrate, it has the highest glass transition temperature (T_G > 350 °C) among those plastic substrate. In this reason, the PI is widely used to fabricate only flexible TFT. However PES or PET can be applied to transparent and flexible TFT under 200 °C process temperature. So, the transparent and flexible TFT has needs to develop with plastic subatrate engineering, appropriate patterning for oxide materials, and low temperature process.

2.3 Oxide materials for Thin Film Transistor

2.3.1 Semiconductor materials

Recently, many researcher has been studied on N-type semiconducting oxides (TSOs). Specially, zinc oxide(ZnO) and indium oxide(InO) have been researched as binary compounds in transparent electronics. Also, indium gallium zinc oxide (IGZO), indium zinc oxide (IZO), and zinc tin oxide(ZTO) are extremely researched as ternary and quaternary compounds, which offer amorphous structure and excellent optical and electrical properties with relatively low temperature process. Generally, TSOs has ion bond property. Ionic amorphous oxide semiconductor occurred under appropriate carrier concentration toward band transport mechanism not hopping mechanism. Conduction band bottom (CBB) of oxide semiconductor consists of peripheral ns-orbital which is bigger as 50~100% than ion self-radius. Therefore, because overlap among s-orbital of ions is easy electron transport in CBB is simple.(**Figure 2.6**) Because of symmetry of spherical and big ns-orbital feature, overlap degree of s-orbital is not strongly affected by oxygen-metal-oxygen bond angle.

This amorphous oxide semiconductor holds p-block positive ion that has $(n-1)d^{10}ns^{0}$ ($n > 4$) electronic configuration, In^{3+} ($[Kr]4d^{10}5s^{0}$, n=5) in IGZO is a representative example. For more information, electronic configuration of Ga^{3+} and Zn^{2+} is $[Ar]3d^{10}4s^{0}$ (n=4). Transparent amorphous oxide semiconductor showing similar field effect mobility

in $(n-1)d^{10}ns^0$ electronic configuration crystaline is applied to a case in $n > 4$ positive ion. Thus, In^{3+} ion affected better in conductive property than Ga^{3+} and Zn^{2+} ion in amorphous phase of IGZO. Although the In is the best conductive material in oxide TFT, the attempt to avoid rare earth material is needed to suppress mass of resource.

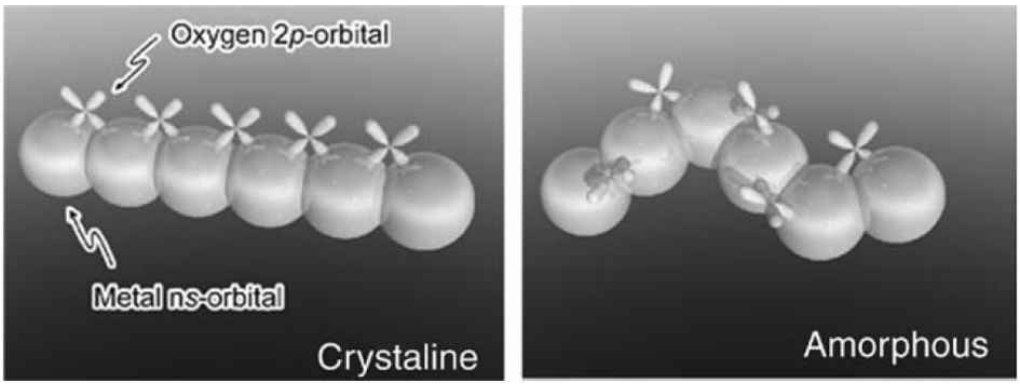


Figure 2.6. The schematic proposed by Nomura et al. The model of crystaline and amorphous oxide semiconductor has (n-1)d10ns0 (n > 4) electron configuration explaining the high field effect mobility of amorphous phase.(adapted from [1])

2.3.2 Insulator materials

The insulator materials is very important to provide active channel interface with semiconductor, which called “dielectric layer” in TFT. So, high quality surface of dielectric layer is required in BCE and ESL structures. In order to promote the potential of metal oxide TFTs, the considerable effort for high k and wide band gap of gate dielectrics, as well as the high electrical property for metal oxide semiconductors, is pivotal. The properties of typical metal oxide materials is indicated in **Table 2.1**. SiO_2(k=3.9) has been extensively used in gate dielectric layer for metal oxide TFTs due to large band gap(8.9eV) and small defect density.[2] Also, SiO_2 is amorphous phase, which effectively prevents the leakage current arising from defects in dielectric structure and carrier tunneling induced by crystalline grain boundary.[3] However, SiO_2 has an intrinsic limitation for the low charge carrier inducement in semiconductor layer by intrinsic low dielectric constant. The perovskite materials, $BaTiO_3$,[4] $PbTiO_3$,[5] and $SrTiO_3$,[6] have disadvantages as the high temperature process for crystalline structure formation and leakage paths through grain boundary. Also, universal binary oxide dielectrics have propensities to crystallize easily and produce grain boundaries, which contribute to form electrical leakage paths and increase gate leakage currents. For these reasons, amorphous inorganic materials, such as HfO_2, Y_2O_3, ZrO_2, and Al_2O_3[7-10], have been recently reported as solution-processed dielectric materials for the high electrical performance of TFT. That being said, the oxide dielectrics induce lower field effect mobility than

vacuum-deposited dielectrics in TFTs. Thus, more research is necessary to develop the dielectric material compound to generate high capacitance with low leakage current and film quality.

Table 2.1. Dielectric constant and band gap property of typical binary oxide dielectric.[11]

Oxide	Dielectric constant	Band gap(eV)
SiO_2	4	8.9
Al_2O_3	9	8.7
HfO_2	25	5.7
TiO_2	80	3.0

2.4 Solution processed zinc oxide TFT

Solution processed thin-film transistors (TFTs) have emerged as next-generation transistors because of their applicability in an advanced process for the creation of printed transparent electronic devices. Various metal-alloy zinc oxides, such as IZO, ZTO and IGZO that are still solution processable, have been introduced with good electrical performances. But it becomes a serious issue of indium (In) usage, which is becoming more expensive and scarce and thus strategic.

Also, to promote the potential of ZnO-based TTFTs with solution processability strongly, a low-temperature process is essential. Although some remarkable reports have been introduced,[12-13] they have an intrinsic problem in that they use a metal oxide precursor with carbonyl and chloride ligand group. The carbonyl ligand groups are completely decomposed at temperatures close to 310 °C; the chloride ligand group absolutely decomposed over 400 °C. These ligand choice hinders the low-temperature process of the metal oxide semiconductor.[14]

Therefore, the ammonia based ZnO precursor solution seized a limelight for metal oxide semiconductor, which is regarded as the most promising active channel material for the future development of flexible TTFT.

The chemical formula of ammonia based ZnO precursor solution is described in following formula.[15,16]

$$ZnO + 4NH_3(aq) + 2H^+(aq) \rightarrow Zn(NH_3)_4^{2+}(aq) + H_2O(l)$$

$$H_2O(l) \rightarrow H^+(aq) + OH^-(aq)$$

$$Zn(NH_3)_4^{2+}(aq) + n\ OH^-(aq) \rightarrow [Zn(NH_3)x\ OHx]x$$

$$[Zn(NH_3)x\ OHx]x \rightarrow ZnO + x\ NH_3 + H_2O(g)$$

Since ammonia and water have high volatility, the precursor solution can be formed easily ZnO at low temperature process as 150 ℃. As this method can be successfully applied to a low temperature process as low as 150 ℃, the method can be adapted as an advanced process for the fabrication of printed transparent electronic devices in the near future.

2.6 Importance of interface engineering

Non-conventional lithography methods such as inkjet printing is an desirable alternative to fabricate TFT using precursor solution. However, while inkjet printing shows relatively good performance in the patterning process, there are a number of issues that includes interface engineering for the yield of dropping solution on plastic substrate for flexible TFT. Because plastic substrate has very low surface energy and rough surface. In order to increase fidelity, the interface engineering is essential process to adapt on the polymer surface.

Additionally, typical oxide dielectric materials have been evaluated as suitable in metal oxide TFT. However, inorganic oxide dielectrics are fragile and inconsistence in the flexible TFT.[17] Also, metal oxide gate dielectrics require high temperature annealing above 400 °C for the sol-gel process, which cannot be applied to plastic substrates.[18]

Unlike inorganic dielectrics, organic dielectrics are suitable for fabrication on plastic substrates because they have good ductility and low-temperature solution processability below 200 °C.[19] That being said, although many researchers have attempted to use high performance gate dielectrics, such as ion gel and a polymer dielectric layer,[20-21] interface problems between the metal oxide semiconductor and the organic dielectric layer have hindered the stable and high performance of TFT fabrication.[22] Interface dipoles induce flat band shift by the interface trap between organic and inorganic materials.[23] Also, interface dipoles usually occur between inorganic and organic

compounds, which induces hysteresis and reduces the effectiveness of charge inducement. In addition, to achieve flexible integrated electronic devices using solution-processed inorganic and polymer materials, interface energy should be controlled using interface engineering by considering the wettability of each. For these reasons, interface engineering for solution processed oxide TFTs with organic dielectric is essential to suppress interface traps. Also, it needs for the process compatibility in coating process with metal oxide semiconductor and organic dielectric solution precursors. This issue is important in all solution-processed ZnO-based TFTs fabrication with organic dielectric.

2.7 References

[1] H. Hosono, Thin Solid Films **2007**, 515, 6000.

[2] S. Jeong, J. Lee, S. S. Lee, S. Oh, H. H. Lee, Y. Seo, B. Ryu, Y. Choi, J. Mater. Chem. **2011**, 21, 17066.

[3] P. K. Nayak, M. N. Hedhili, D. Cha, H. N. Alshareef, Appl. Phys. Lett. **2012**, 100, 202106.

[4] H.Han, D. Ghosh, J. L. Jones, J. C. Nico, J. Am. Ceram. Soc. **2012**, 9, 1.

[5] Y. S. Yoon, W. N. Kang, S. S. Yom, T. W. Kim, M. Jung, H. J. Kim, T. H. Park, H. K. Na, Appl. Phys. Lett. **1993**, 63, 1104.

[6] F. M. Pontes, E. J. H. Lee, E. R. Leite, E. Longo, J. Mater. Science. **2000**, 35, 4783.

[7] Y. Aoki, T. Kunitake, A. Nakao. Chem. Mater. **2005**, 17, 450.

[8] G. Adamopoulos, S. Thomas, D. D. C. Bradley, M. A. McLachlan, T. D. Anthopoulos, Appl. Phys. Lett. **2011**, 98, 123503.

[9] G. Adamopoulos, S. Thomas, P. H. Wöbkenberg, D. D. C. Bradley, M. A. McLachlan, T. D. Anthopoulos, Adv. Mater. **2011**, 23, 1894.

[10] D. X. Xia, J. B. Xu, J. Phys. D: Appl. Phys. **2010**, 43, 442001.

[11] J. Roberton, Rep. Prog. Phys. **2006**, 69,327.; Wang, L.; Yoon, M.-H.; Lu, G.; Yang, Y.; Facchetti, A.; Marks, T. J. Nat. Mater. **2006**, 5, 893.; Ponce Ortiz, R.; Facchetti, A.; Marks, T. J. Chem. Rev. **2010**, 110, 205.

[12] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, Nat. Mater. **2011**, 10, 45.

[13] M. G. Kim, M. G. Kanatzidis, A. Facchetti and T. J. Marks, Nat.

Mater. 2011, 10, 382.

[14] S. O. Beng, L. Chensha, L. Yuning, W. Yiliang and L. Rafik, J. Am. Chem. Soc. 2007, 129, 2750.

[15] B. Zhao, C.-L. Wang, Y.-W. Chen, and H.-L. Chen, Mater. Chem. Phys. 2010, 121, 1.

[16] J. J. Richardson and F. F. Lange, Cryst. Growth Des. 2009, 9, 2570.

[17] S. H. Chae, W. J. Yu, J. J. Bae, D. L. Duong, D. Parello, H. Y. Jeong, Q. H. Ta, T. H. Ly, Q. A. Lu, M. Yun, X. Duan and Y. H. Lee, Nat. Mater. 2013, 12, 403.

[18] V. ZardettoT. M. BrownA. RealeA. Di CarloJ.Polym.Sci. Part B:Polym. Phys. 2011, 49638.

[19] I.G. Hill, A. Rajagopal and A. Kahn, Appl. Phys. Lett. 1998, 73, 662.

[20] H. Bong, W. H. Lee, D. Y. Lee, B. J. Kim, J. H. Cho and K. Cho, Appl. Phys. Lett. 2010, 96, 192115.

[21] K. Lee, J. Kim, S. Im, C. Kim, H. Baik, Appl. Phys. Lett. 2006, 89, 133507

[22] K. Lee, G, Ko, G. H. Lee, G. B. Han, M. M. Sung, Appl. Phys. Lett. 2010, 97, 082110.

[23] N. Koch, Chem Phys Chem, 2007, 8, 1438.

Chapter 3. Experimental Procedure

3.1 Materials

Preparation of ZnO solution: This method of ZnO solution followed a previously reported method.[1,2] We dissolved 0.5 M zinc nitrate hexahydrate ($Zn(NO_3)_2 \cdot 6H_2O$) [AlfaAesar, 99.9%] in 15 ml de-ionized(DI) water. A 10 ml DI-water solution of 2.5 M sodium hydroxide(NaOH) (Duksan Pure Chemicals Co.,Ltd.) was added drop by drop to the zinc nitrate solution while stirring at 600 rpm for 10min. After a while, white zinc hydroxide was formed by precipitation, and the solution was centrifuged four times with DI water at 5000 rpm for 5 min. During all four centrifugation processes, Na^+ and NO_3^- were eliminated by washing with DI-water. The final centrifuged zinc hydroxide was dissolved in 20 ml ammonium hydroxide(aq) (AlfaAesar,99.9%) with 25 ml DI-water.

Preparation of alkali metal doped ZnO solution[3,5]: For Li-ZnO solution, 0.001 mole of the zinc oxide (ZnO) [Sigma Aldrich, 99.99%] was dissolved into 12 ml of ammonium hydroxide (aq) [Alfa Aesar, 25 wt% NH_3 in water,99.99%]. The as-prepared solution was put in refrigerator for 5 hours to increase of the solubility of ZnO. For the Li doped ZnO solution, the 0.1 ml of 1 M Lithium hydroxide (LiOH) [Duksan Pure Chemicals Co., Ltd.]/deionized (DI) water solution was added by a drop to the 12ml of ZnO precursor solution, which was 10 mol%. The Li-doped ZnO solution was vertically stirred for 3

minutes. For the Na doped ZnO solution, the 0.1 ml of 0.1 M sodium hydroxide (NaOH) [Duksan Pure Chemicals Co., Ltd.]/deionized (DI) water solution was added by a drop to the 12ml of ZnO precursor solution, which was 1 mol%. The Na-doped ZnO solution was vertically stirred for 3 minutes.

Polymer dielectric precursor solution[2,4]: To obtain the polymer dielectric precursor solution, 10-wt% PVP solution was prepared from poly(4-vinylphenol) (MW = 25,000, Sigma-Aldrich) and poly(melamine-co-formaldehyde) methylated/butylated (Mn = 637, Aldrich) as a cross-linker in propylene glycol monomethyl ether acetate (PGMEA) (MW = 132.16, Fluka) (2:1:17, w/w), with vigorous stirring. In addition, to synthesize the TiO
2 precursor and PVP composite solution (TPC), 5-wt% PVP solution was prepared with poly(melamine-co-formaldehyde) methylated /butylated and PGMEA (2 : 1 : 37, w/w). The 5-wt% PVP solution was stirred vigorously for 24 h at room temperature. The TiO_2 precursor was obtained from titanium (IV) butoxide (MW = 340.32, Sigma-Aldrich) and acetyl acetone (MW = 100.12, Fluka) at a molar ratio of 1:2. The 5 wt% PVP solution and TiO_2 precursor were mixed at a ratio of 9:1 (w/w) with stirring. In order to make uniform gelatin without the aggregation of the PVP solution and the TiO_2 precursor, the solution was stirred under low temperature (2 ºC) to suppress rapid cross-link. Finally, the gelatin was dissolved in ethanol (MW = 46.07, DAE JUNG) in the ratio of 1:1 (w/w).

IZO precursor solution synthesis[3]: For IZO solution, 0.1 M $In(NO_3)_3 \cdot H_2O$[Sigma Aldrich, 99.999%]and 0.1M $Zn(NO_3)6H_2O$ [Sigma Aldrich, 99%] were dissolved in 2-methoxy ethanol with equivalent molar ratio of ethylene glycol (EG) [Sigma Aldrich, 99.8%]. Solutions were stirred vigorously for 24 hours.

Al_2O_3 precursor solution synthesis: Al_2O_3 solution was prepared by adding 0.3 M $Al_2O_3 \cdot 9H_2O$[Sigma Aldrich, 98%] in 2-methoxy ethanol [Sigma Aldrich, 99.8%] with 6.67 M hydrogen peroxide (H_2O_2) [Sigma Aldrich, 30 wt% in H_2O].

3.2 Patterning methods of ZnO semiconductors

Fabrication of patterned TTFT using binary solvent mixture[2]: SiO_2 substrate was cleaned in an ultrasonic bath with detergent, acetone, and isopropyl alcohol (IPA) prior to processing. A 10 wt% PMMA (Mw~100,000) solution was dissolved in toluene overnight, then spin-coated onto the 200 nm thermally grown SiO_2 on a highly p-doped Si substrate at 3000 rpm for 30seconds. Selectively exposed PMMA regions were irradiated with ultraviolet-ozone (UVO, λ = 185 and 254 nm, 100 mW/cm^2) through a shadow mask for one hour to make pre-pattern. When the UVO irradiation had created a patterned area through breakage of PMMA bonds, de-ionized (DI) water rinsing left the SiO_2 surface selectively exposed. Each revealed region had an area of 550 μm x 1200 μm. For uniform coating with the ammine-hydroxo zinc solution, the overall PMMA layer was exposed to UVO irradiation for 5 minutes. The prepared ammine-hydroxo zinc solution was spin-coated onto the pre-patterned substrate in a double step (5 seconds at 500 rpm and 30 seconds at 1000 rpm). After that, the spin-coated substrate was immediately dipped into a toluene-methanol mixture (4:1, v/v) for 5 minutes and then rinsed it with isopropyl alcohol (IPA) and DI-water.

Fabrication of patterned TTFT using interface engineering[5]: The overall fabrication of the device is illustrated schematically in Figure 1. The substrate was cleaned in an ultrasonic bath with acetone and isopropyl alcohol (IPA). The aminosilane grafting on the surface of

the SiO_2 wafer was realized by treatment for the reactive hydroxyl group on the surface of the SiO_2 wafer through ultra violet ozone (UVO, λ = 185 and 254nm, 100 $mWcm^{-2}$) exposure for 30 minutes, followed by immersion in a 0.5 wt% aqueous solution of 3-(amino propyl triethoxysilane) (APTES, Sigma Aldrich, USA) for 10 min. After washing the unreacted APTES with deionized (DI) water, the amino group was reacted with monoglycidyl ether - terminated PDMS (number-average molecular weight 5000 g mol - 1, Sigma Aldrich, USA) by heating at 80°C for 1 hour. After heating, the PDMS coated substrate was immersed in isopropyl alcohol and sonicated for 1 minute to remove the unreacted PDMS. A shadow mask was laid on the substrate and UVO irradiated onto selective regions for 40 minutes. Then, the shadow mask was removed. The prepared ZnO solution was dropped onto the pre-patterned substrate using wettability control and casted from the substrate. The substrate was then dipped in methanol for 1 min with sonication. The patterned ZnO films were revealed after rinsing with IPA and DI-water. The substrate was heated to a range of 100 ~ 300 °C to sinter the ZnO films. Aluminium (Al) source and drain electrodes, thickness ~ 100 nm, width 1000 μm, and gap length 50 μm, were then deposited on the patterned ZnO semiconductor films by thermal evaporation.

3.3 Interface Engineering

Interface engineering via self-assembled inorganic layer (SAIL):[4] Amino silane grafting on the surface of the SiO_2 wafer was realized by treatment for the reactive hydroxyl group on the surface of the SiO_2 wafer through exposure to ultraviolet ozone(UVO, λ = 185 and 254 nm, 100 $mWcm^{-2}$) for 30 minutes, followed by immersion in a 0.5 wt% aqueous solution of 3-(amino propyl triethoxy silane)(APTES, Sigma Aldrich, USA) for 10 min. After washing the unreacted APTES with deionized (DI) water, the amino group was reacted with monoglycidyl ether - terminated PDMS (number-average molecular weight 5000 g mol - 1, Sigma Aldrich, USA) by heating at 80 °C for 1 hour. After heating, the PDMS coated substrate was immersed in isopropyl alcohol (IPA) and sonicated for 1 min to remove the unreacted PDMS. The PDMS-coated substrate was rinsed again by IPA and then blown by nitrogen gas.

3.4 TFT Fabrication

Fabrication of patterned flexible TTFT[2]: The overall fabrication of the device is illustrated schematically in Figure 3.1. The 10 wt% PVP solution was prepared from poly(4-vinylphenol) and poly(melamine-co-formaldehyde) methylated/butylated in propylene glycol monomethyl ether acetate (PGMEA) (2:1:17, m/m). The PVP solution was spin-coated (30 seconds at 1000 rpm) onto the ITO-PET [Mirae Innovation & Technology], which was used as the gate electrode and substrate. The substrate was heated at 200 °C for 1 hr. The thickness of the PVP was 672 nm. The PMMA was spin-coated onto the PVP layer. (30 seconds at 3000 rpm) A shadow mask was laid on the PMMA layer, and UVO irradiated onto selective PMMA regions for 1 hr. The shadow mask was then removed and the pre-patterned substrate rinsed in DI-water. UVO was irradiated onto the overall PMMA layer for 5 min. The prepared ZnO solution was spin-coated onto the patterned substrate in a double step (5 s at 500 rpm and 30 s at 1000 rpm). The substrate was then dipped in a toluene-methanol mixture (4:1, v/v) for 5 min. The patterned ZnO was revealed after rinsing with IPA and DI-water. The substrate was heated to 200 °C to sinter the ZnO. Al source and drain electrodes (100 nm Al), 1000 μm wide with a 60 μm gap, were then deposited on the patterned semiconductor by thermal evaporation.

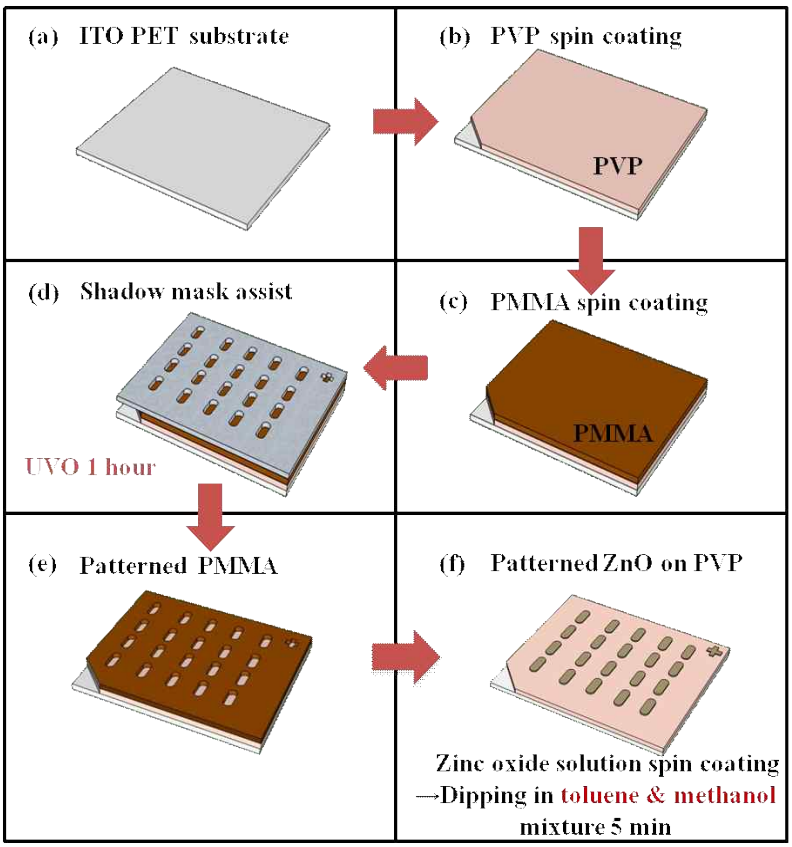


Figure 3.1. Schematic description of overall fabrication process(the patterned TTFT): (a) ITO-PET substrate; (b) Spin coated PVP on the ITO-PET substrate; (c) Spin coated 10 wt% PMMA on the ITO-PET substrate by 3000 rpm; (d) Stencil mask assist on PMMA layer; (e) Patterned PMMA on the ITO-PET substrate after exposure of UVO 1h; (f) Patterned ZnO on the PVP dielectric layer.

Integrated ZnO based oxide TFT Film fabrication[3]: Al_2O_3 film was spin-coated on heavily boron-doped silicon with 3000 rpm for 20s and softbaked at 240 °C for 5min. To get desired film thickness, we carried out multi-coating and finally hard baked at 350 °C and 500 °C. The 350 °C and 500 °C annealed film thickness were measured spectroscopic ellipsometry (SEMG-Vis1000: Nano-view) and cross section TEM, and their thicknesses were 242nm and 200nm, respectively. For InZnO TFT, InZnO film was spin-coated on Al_2O_3 film with 4000 rpm for 20s and annealed 350 °C for 2 hours. For Li-ZnO TFT, Li-ZnO film was spin-coated on Al_2O_3 film with 3000 rpm for 30s and annealed 300 °C for 1 hour.

Metal-Insulator-Metal (MIM) device fabrication[3]: To evaluate capacitance with various frequency and leakage current density of 350 °C and 500 °C annealed Al_2O_3 film, we fabricated MIM capacitor on Si^{++} substrate with circular Al electrode through thermally evaporation. The area of the circular Al was 0.17 mm^2. Capacitance of Al_2O_3 film was measured various frequencies from 20 Hz to 1 MHz.

Fabrication of the ZnO/SAIL/PVP TFT[4]: The prepared PVP solution was spin-coated (30 seconds at 1000 rpm) onto the ITO-PET [Mirae Innovation & Technology], which was used as the gate electrode and substrate. The substrate was heated at 200 °C for 1 hour. The thickness of the PVP was 672 nm. The SAIL process

was treated on the highly cross linked PVP. Then, the prepared ZnO solution was spin coated on SAIL grafted c-PVP, which is treated above interface engineering. After heating at 200 °C for 1 hour, Aluminium (Al) source and drain electrodes, thickness ~ 100 nm, width 1000 μm, and gap length 50 μm, were then deposited on the ZnO semiconductor by thermal evaporation.

3.5 Characterization

Observation of the ZnO thin films: The thickness of both intrinsic ZnO and alkali metal-doped ZnO was characterized by a field emission scanning electron microscope (FE-SEM; S-4800: Hitachi) and an atomic force microscope (AFM; XE100: PSIA). The crystalline phase of the ZnO thin film were characterized by high resolution transmission electron micrograph (HR-TEM; JEM-2100F: JEOL(Japan)). The transmittance of ZnO was measured by a UV-visible spectrometer (Lambda 35: Perkinelmer). The thickness of the polymer thin film was measured (ST2000-DLXn, K-MAC). The deposited films and ZnO powder were characterized by measurement of X-ray diffraction (XRD, Bruker D8 Discover: Germany). The deposited intrinsic/Na doped ZnO films were characterized by measurement of X-ray Photoemission Spectroscopy (XPS; Sigma Prove : ThermoVG (U.K)). The current-voltage measurements were executed under ambient conditions using an Agilent 4155B semiconductor parameter analyzer.

Thermal behavior analysis of Al_2O_3 solution: Al_2O_3 powder was made by evaporating solvent in 80 °C convection oven for 8 hours. Thermo gravimetry differential thermal analysis (TG-DTA; Seiko Exstar 6000: SEICO) was performed with increasing temperature of 8 °C/min upto 600 °C. The thickness and crystalline phase of the Li-ZnO and InZnO thin film were characterized by high resolution transmission electron micrograph (HR-TEM; JEM-2100F:

JEOL(Japan)). The detailed elemental information was characterized by time-of-flight secondary ion mass spectrometry (TOF-SIMS; ION-TOF, Germany).

3.6 References

[1] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. **2008**, 130, 51.

[2] K. Kim, S. Park, J. B. Seon, K. H. Lim, K. Char, K. Shin and Y. S. Kim, Adv. Funct. Mater. **2011**, 21, 3546.

[3] J. H. Park, K. Kim, Y. B. Yoo, S. Y. Park, K. H. Lim, K. H. Lee, H. K. Baik and Y. S. Kim, J. Mater. Chem. C, **2013**, 1, 7166.

[4] K. Kim, E. Lee, J. Kim, S. Y. Park, K.-H. Lim, C. Shin, Y. S. Kim, J. Mater. Chem. C, **2013** , 1 , 7742.

[5] K. Kim, S. Park, K. H. Lim, C. H. Shin and Y. S. Kim, J. Mater. Chem., **2012**, 22, 23120.

Chapter 4. Polymer pre-pattern and binary solvent developing for ZnO based TFT

4.1 Introduction

The patterning of electronic devices is essential to avoid crosstalk noise and current leakage in the TFT.[1,2] When patterning of solution-processed ZnO thin films, several points need careful consideration. In general, TFTs are patterned by photolithography after deposition of the overall substrate. However, this method is not suitable for the patterning of solution-processed ZnO thin films. As these thin films have a porous structure, the photoresist stripper spreads through the film during developing, lowering semiconducting performance and degrading the interface between the active layer and the gate insulator.[3] Moreover, because of the softness of the material, it is easily damaged by plasma during dry etching while patterning.[4] Protecting it from damage during etching requires cumbersome processes such as applying an etch stopper or a protective layer.[5-7] For these reasons, most previous results of solution-processed ZnO thin films were reported solely with non-patterned films.[8-10] Recently, transistors isolated by mechanical scribing have been reported, because patterning is essential to show the good performance of solution-processed ZnO TTFTs.[11] However, as neither mechanical scribing nor standard wetchemical etching are ideal, new patterning methods are needed for solution-processed ZnO TTFTs.

In the solution-based processing of ZnO thin films, the

ammine-hydroxo zinc solution is applicable in a low temperature process because of the outstanding volatility of the ammine, which combines with the zinc hydroxide. However, the ammonia-based solution makes it difficult to control thickness and morphology accurately. As controlling the drying process in solution-processed ZnO thin films is very subtle and cumbersome, it is difficult to fabricate ZnO semiconductor films of robust fidelity with selective printing or patterning. For example, in the inkjet printing process, the ink droplets follow an erratic migration route from the nozzle, making thickness difficult to control. Also, the uneven drying process induces the matting of particles, wavy patterns, and the coffee-ring effect, degrading the performance of the semiconductor film. Moreover, inkjet printing in general produces low-resolution patterning. For high-resolution inkjet printing, a patterned hydrophobic region is essential to the process.[12] For these reasons, several new patterning methods for the oxide TFT have emerged over the past few years.

To this end, we have developed a simple patterning method for TTFTs using solution-processed ZnO films as semiconductors. To achieve this, we used a pre-patterned substrate fabricated by selective decomposition of poly(methyl methacrylate) (PMMA), and introduced a new developing method with a binary solvent mixture, which has the potential to control solution-processed ZnO thin-film patterns without defects such as the coffee-ring effect, particle matting, or wavy lines.

4.2 Simple fabrication method for the selective patterned ZnO TFT

The overall fabrication of the device is illustrated schematically in Figure 4.1. The substrate was cleaned in an ultrasonic bath with detergent, acetone, and isopropyl alcohol (IPA) prior to processing. A 10 wt% PMMA (Mw~100,000) solution was dissolved in toluene overnight, then spin-coated onto the 200 nm thermally grown SiO_2 on a highly p-doped Si substrate at 3000 rpm for 30 seconds (Figure 4.1b). Selectively exposed PMMA regions were irradiated with ultraviolet-ozone (UVO, λ = 185 and 254 nm, 100 mW/cm^2) throug ha shadow mask for one hour (Figure 4.1c). When the UVO irradiation had created a patterned area through breakage of PMMA bonds, de-ionized (DI) water rinsing left the SiO_2 surface selectively exposed (Figure 4.1d). Each revealed region had an area of 550 μm x 1200 μm. For uniform coating with the ammine-hydroxo zinc solution, we again exposed the overall PMMA layer to UVO irradiation for 5 minutes. The prepared ammine-hydroxo zinc solution (see chapter 3.1) was spin-coated onto the pre-patterned substrate in a double step (5 seconds at 500 rpm and 30 seconds at 1000 rpm). After that, we immediately dipped the spin-coated substrate into a toluene-methanol mixture (4:1, v/v) for 5 minutes and then rinsed it with isopropyl alcohol (IPA) and DI-water, respectively (Figure 4.1e).

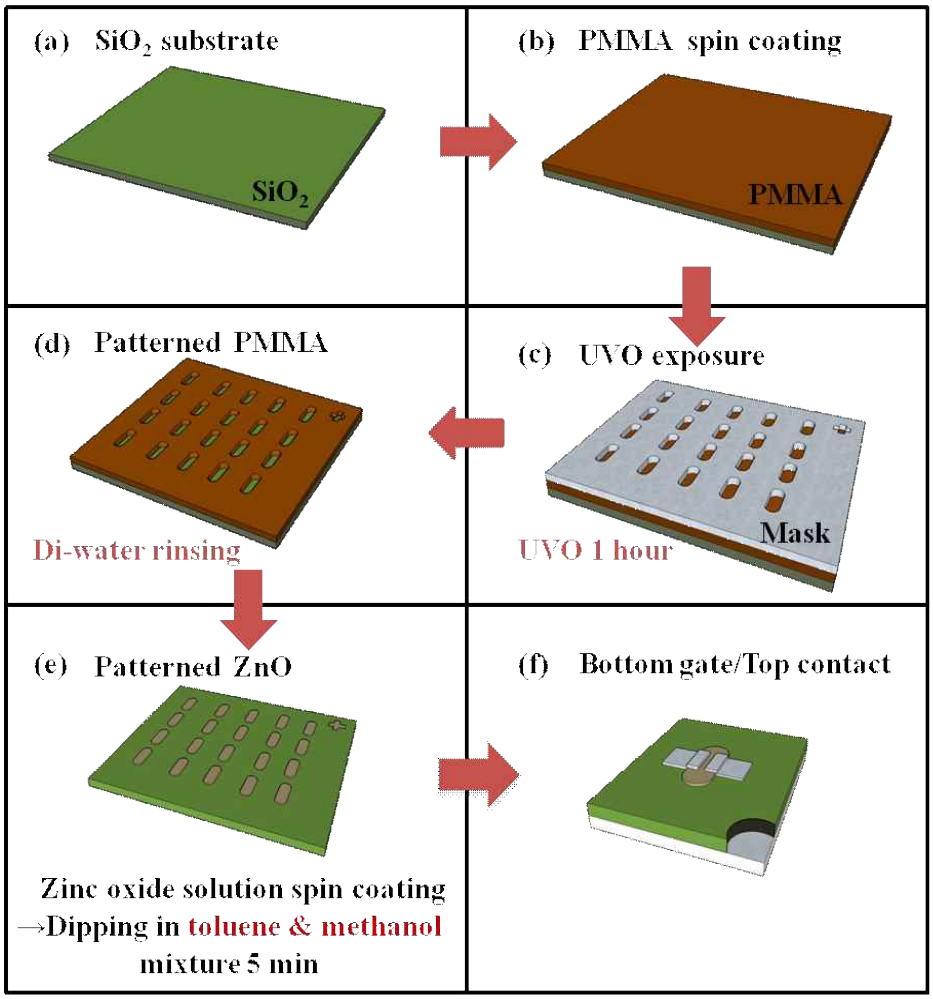


Figure 4.1. Schematic description of overall fabrication process: (a) SiO_2 substrate;(b) Spin-coated PMMA on the SiO_2 substrate; (c) Shadow mask over PMMA layer; (d) Patterned PMMA layer on the SiO_2 substrate; (e) Patterned ZnO on the SiO_2 substrate; (f) Thin film transistor with bottom gate and top contact.

As the residual PMMA layer was eliminated in the toluene-methanol mixture along with the debris on the PMMA layer, neat, uniform, and defect-free patterns were fabricated. For sintering, the film on the substrate was heated to 200 °C or 300 °C respectively, so that the patterned ZnO thin film could function as an n-type semiconductor. Al source and drain electrodes, about 100 nm thick, 1000 μm wide, and with a 60 μm gap, were thermally evaporated onto the patterned semiconductors. Highly doped p-type Si was used as the bottom gate electrode (Figure 4.1f).

With this method, the malfunction ratio of the TTFT based on the ZnO thin-film micro-patterns was extremely low. As mentioned, poor control of the drying process in solution-processed ZnO thin films tends to prevent robust fidelity in ZnO semiconductor films. The uneven drying of an ammonia-based solution leads to nucleation/aggregation of particles and induces extremly porous or wavy patterns during ZnO thin-film fabrication. However, with this process, through the merits of a pre-patterned substrate and a binary solvent mixture, the patterns were created successfully without defects. In addition, several dozen ZnO semiconductor film patterns can be fabricated on the substrate with robust fidelity through this patterning process.

4.3 Binary solvent mixture: toluene - methanol mixture

In this work, we introduce a binary solvent mixture, a toluene-methanol mixture, as a new developing solvent. When ammonia based solution is dried, ammonium carbamate, which is induced with the reaction with carbon dioxide in air, is formed on the surface and blocks the water evaporation.[13] However, ammonia in ZnO solution continuously evaporates and then the ZnO is precipitated abruptly by pH decrease (Figure 4.2).[14] That is the reason we have used binary solvent mixture including methanol to prevent ammonium carbanate and extract water without the abrupt evaporation of ammonia to form uniform pattern. To show the performance of the binary solvent mixture, we prepared three samples: the first sample was dipped in toluene when the ZnO solution pattern on the substrate was still wet, after spin-coating with an ammine-hydroxo zinc solution; a second sample was dipped in toluene after air drying the ZnO solution pattern on the substrate after spin-coating; and a third sample was dipped in a toluene-methanol mixture with a wet ZnO solution pattern on the substrate after spin-coating. In the first sample, when it was dipped in toluene before the ZnO solution had dried, toluene blocked generation of ammonium carbamate. But polar ZnO solution was isolated in the non-polar toluene. Also, this toluene can't extract water in ZnO. In clearing bank structure using toluene, polar ZnO solution did not maintain selective areas because ZnO aqueous solution was shrunk by surface tension on the evaporation of

non-polar toluene. So it causes the defects of an unclear pattern (Figure 4.3a - 4.3c). In the second sample, it was dipped in toluene after the ZnO solution had dried. There are generated ammonium carbamates on the surface, which causes matted ZnO particles and wavy lines (Figure 4.3d - 4.3f). The water of solution was isolated by film of ammonium carbamates, it aggregated within film of ammonium carbamates. Also, in evaporation, as ammonia more fast evaporated than water in ZnO films, it induced the abrupt precipitation of ZnO and created the matted ZnO particles. In the third sample, developed with the toluene-methanol (4:1 v/v) mixture before the ZnO solution had dried, the ZnO thin film shows clear divisions and edges as directly patterned semiconductors without any defects (Figure 4.3g - 4.3i).

In this study, the toluene-methanol mixture was introduced as the developing solvent. As this binary toluene-methanol mixture, composed with both hydrophobic and hydrophilic solvents, they had a good potential to remove a wide range of contaminants in a single step.[15,16] Therefore, our introduced solvent that used simply binary solvent mixture has azeotropic solvent effect and acts water extraction effectively. Thus, uniform and clearly patterned ZnO thin films were produced with good fidelity.

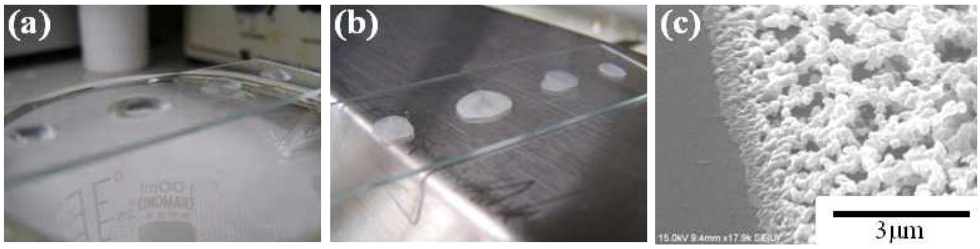


Figure 4.2. Problems of ammonia based solution; (a) droping the solution on glass substrate ;(b) drying the solution on glass; (c) Tilted FE-SEM image of the matted ZnO paticles(Θ = 60°).

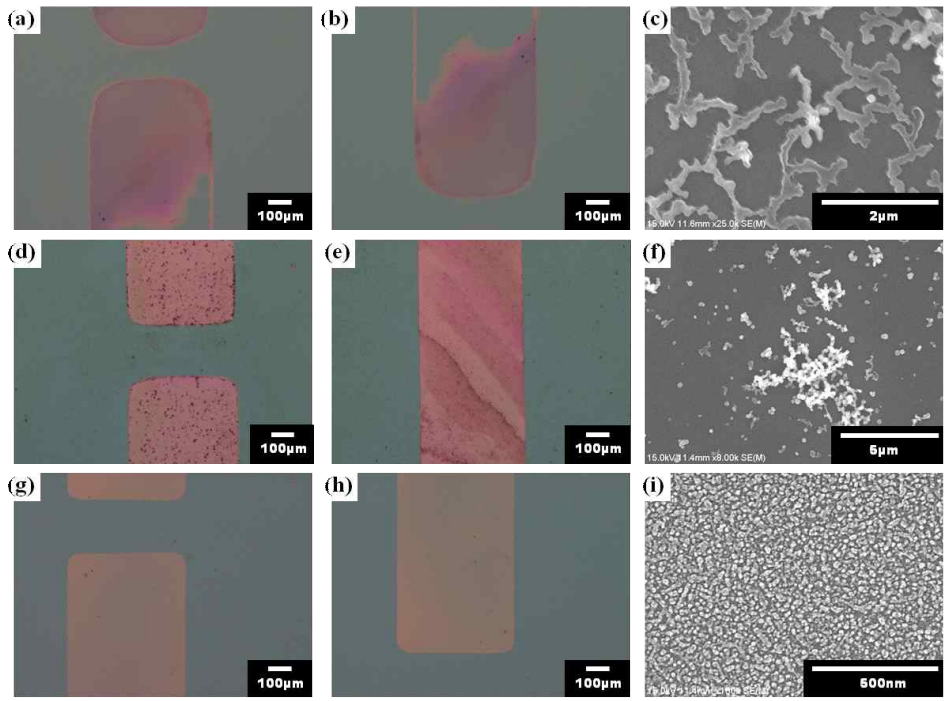


Figure 4.3. Cases of Optical microscopy images and SEM micrograph of patterned ZnO on a SiO_2 substrate. (a), (b) and (c) Cases of developing by toluene before the ZnO solution has dried up. (d), (e) and (f) Cases of developing by toluene after the ZnO solution has dried up solution. (g), (h) and (i) Cases of developing by toluene & methanol mixture (methanol 20 %) before the ZnO solution has dried up.

4.4 Bond breakage of PMMA : Pre-patterned substrates

The shadow-mask assisted process has good potential for the wide-scale manufacturing of electronic devices. This technique can be easily fabricated the selective area depending on the mask pattern size. Recent developments in the fabrication of shadow mask could reduce the minimum size up to around 10 micrometer level.[17] In addition, the breakage of PMMA bonds is well known in the field of block copolymer lithography.[18] Under UVO irradiation, the carbon-carbon bond is easily broken by strikes from the reactive hydroxyl functional groups. We used PMMA bond breakage to manufacture pre-patterned substrates. Figure 3a shows the pre-patterned PMMA layer. It is used as an appropriate patterning method for selective deposition of the solution-processed ZnO (zinc oxide), avoiding the problems of the standard etching process. Due to the selective exposure of regions, the patterned ZnO films can be deposited on any substrate. Figure 4.4b shows the patterned ZnO films. Sixty TFTs were fabricated on a 200 nm thick SiO_2 layer, thermally grown on a Si substrate, in a 2 cm x 2 cm area, which can be produced in one run (Figure 4.4c). The cross-sectional FE-SEM images and 3D atomic force microscopy (AFM) image of the ZnO thin film shows the uniform pattern with a 52 - 75 nm thickness range (Figure 4.4d - f). The effect of the binary solvent mixture and pre-patterned PMMA layer was confirmed by the uniform deposition of the thin films.

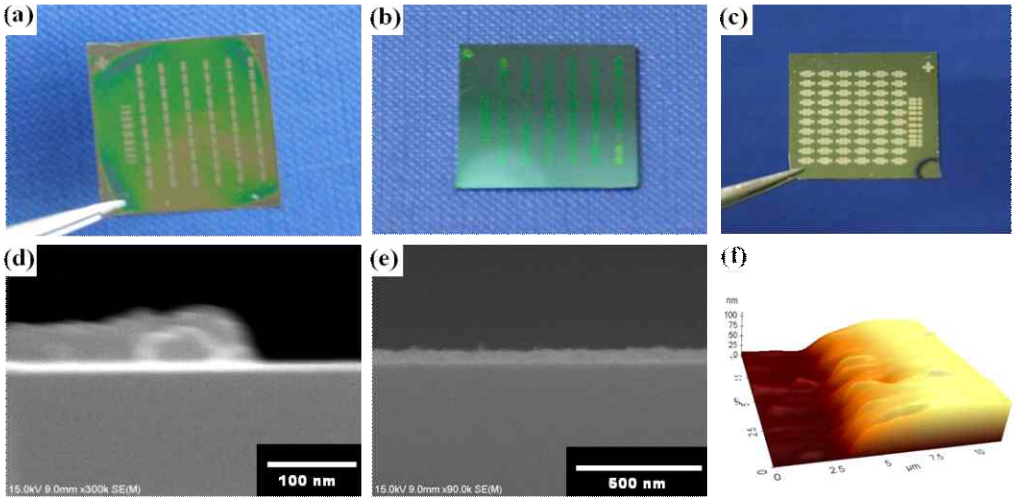


Figure 4.4. (a) The pre-patterned substrate by selective PMMA bond breakage. (b) Patterned ZnO thin films on a SiO_2 substrate.(c) The optical image of completed 60 TFTs by one run. Al source and drain electrodes with around 100nm thickness, 1000 μm wide with a 60 μm gap are deposited on the patterned semiconductors. (d) and (e) Cross section SEM micrograph of the patterned ZnO film. (f) A 3D AFM image of the patterned ZnO film.

In photolithography, as solution-processed ZnO thin films have a porous structure, the photoresist stripper passes throughout the thin film during developing and causes loss of electrical performance.[3,19] In this reason, we introduced pre-patterning using the PMMA layer to pattern solution-processed ZnO films. The PMMA layer could be selectively removed by UVO exposure through a shadow mask pattern and complete removal was easy using the binary solvent mixture. The PMMA patterns provided the regions for selective deposition of the solution-processed ZnO films and could be removed without damaging the material properties of the ZnO. XRD analysis of completed ZnO patterns indicated a ZnO thin-film formation without any adverse effects from the solvent or PMMA (Figure 4.5). In XRD analysis of powder, peaks at 2Θ = 31, 34, 36, 47 and 56 correspond to (100), (002) ,(101), (102) and (110) directions of ZnO hexagonal structure. These indicate that ZnO powder has a hexagonal wurtzite structure. In XRD analysis of ZnO thin film, in general, only the (002) peak of the ZnO thin film can be shown at high temperature processing over 600 °C.[20]The high (002) peak of the ZnO thin film indicates the good crystallization of thin film phase. However, with our system, the (002) peak of the ZnO thin film was sharply shown at low temperature processing (~200 °C). We believe that the binary solvent mixture effectively extracted solvent from ZnO precursor solution to generate the ZnO thin film with high quality below 200 °C.

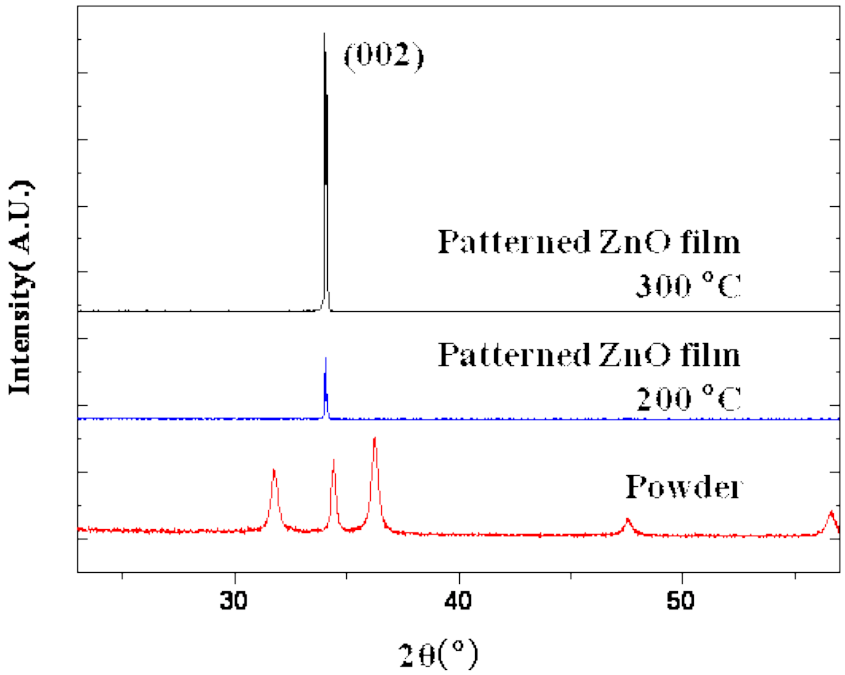


Figure 4.5. Nanocrystallinity of the patterned ZnO thin film sintered at the temperature range 200 - 300 °C. High resolution X-ray diffraction (HRXRD) data of a wurtzite ZnO powder obtained through drying of the zinc-ammine precursor solution. HRXRD data were collected using a Bruker D8 Discover diffractometer (Germany) with Cu Kα radiation.

4.5 Electrical characteristics

From analysis of the transfer curves using Equation (4), this device has the average mobility μ=0.12 $cm^2v^{-1}s^{-1}$ at 200 °C. Over 90 % of TFTs fabricated in a single time run operated well and exhibited uniform electrical characteristics (Figure 4.6). The output curve and transfer curves of a representative TFT are presented in Figure 4.7a, and the mobility calculated from Figure 5b, μ = 0.16 $cm^2v^{-1}s^{-1}$, V_{th} = 7.3 V and on/off current ratio = 10^7 at V_D = 40 V after 200 °C sintering. The output curve and transfer curve of our patterned TFT, with a 300 °C annealing process at ambient conditions, are presented in Figure 4.7c and d. Calculating the mobility from Figure 5d, μ = 0.80 $cm^2v^{-1}s^{-1}$; V_{th} = 11.1 V; and the on/off current ratio >10^7at V_D = 40 V. We summarized the average electrical characteristics of the 60 patterned ZnO TFTs on the SiO_2/Si substrate in Table 4.1. Mobility increased more than five times when the sintering temperature increased from 200 to 300 °C. Generally, increasing the sintering temperature of solution-processed ZnO enhances the electrical performance of the ZnO TFTs.

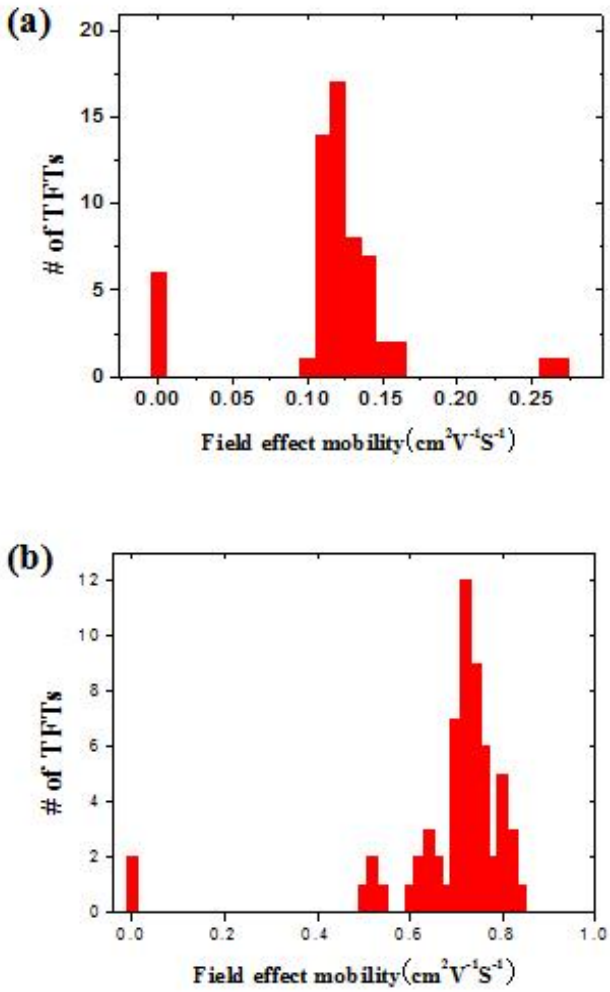


Figure 4.6. (a) The average field effect mobility of TFTs as one run at 200°C. (b) The average field effect mobility of TFTs as one run at 300°C.

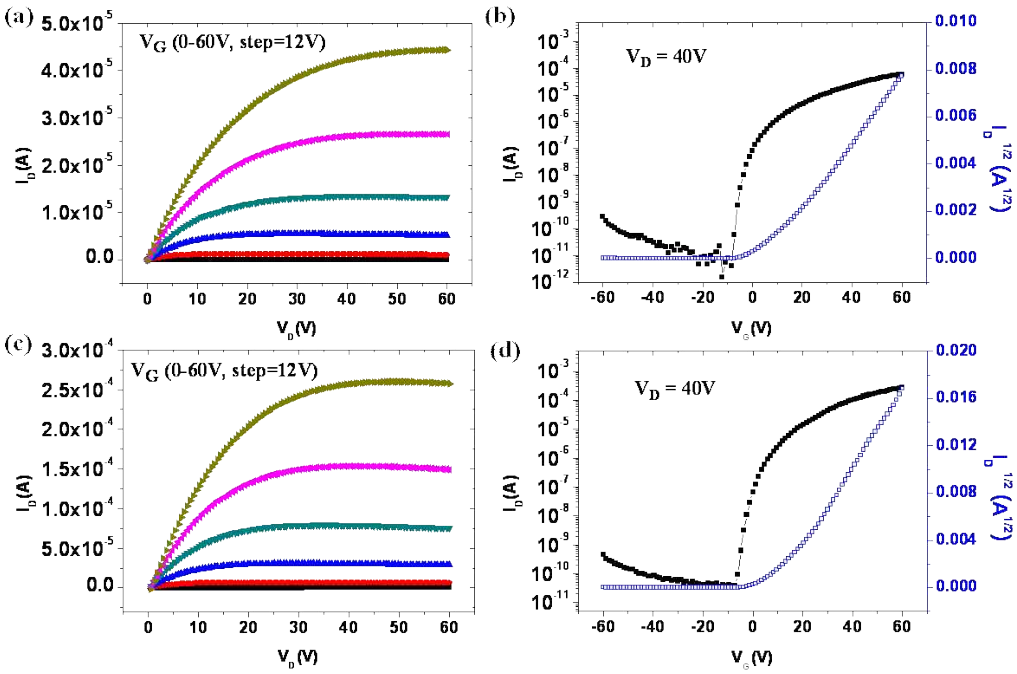


Figure 4.7. Typical electrical characteristics for patterned ZnO-TFT with W/L ratio of 20. (a) and (b): Output and transfer curves at 200 °C. (c) and (d): Output and transfer curves at 300 °C.

Table 4.1. Electrical properties of patternd ZnO TFT on SiO_2 (operating voltage: 40 V). All devices are fabricated under ambient conditions. (This summarized information is the average of each 60 patterned TFTs by one run)

Anneal(°C)	V_{th}	$\mu(cm^2v^{-1}s^{-1})$	I_{on}/I_{off}
200	7.3	0.12	10^7
300	6.5	0.71	10^7~10^8

As these ZnO patterns prevented cross-talk noise and completely blocked current leakage in the patterned semiconductors, the electrical characteristics showed the intrinsic performance of ZnO thin film TFTs and needed no additional etching process to isolate the TFT (Figure 4.8). The gate leakage current was shown under 10^{-9}A. Also, the mobility (0.80 $cm^2v^{-1}s^{-1}$ at 300 °C) of this product was higher than the previously reported mobility (0.05-0.2 $cm^2v^{-1}s^{-1}$ at 300 °C[21], which is patterned solution-processed IGZO TFT by conventional photolithography) of patterned ZnO TFTs using solution-processed intrinsic ZnO semiconductors. This improvement is attributed to the minimization of performance degradation by our patterning method.

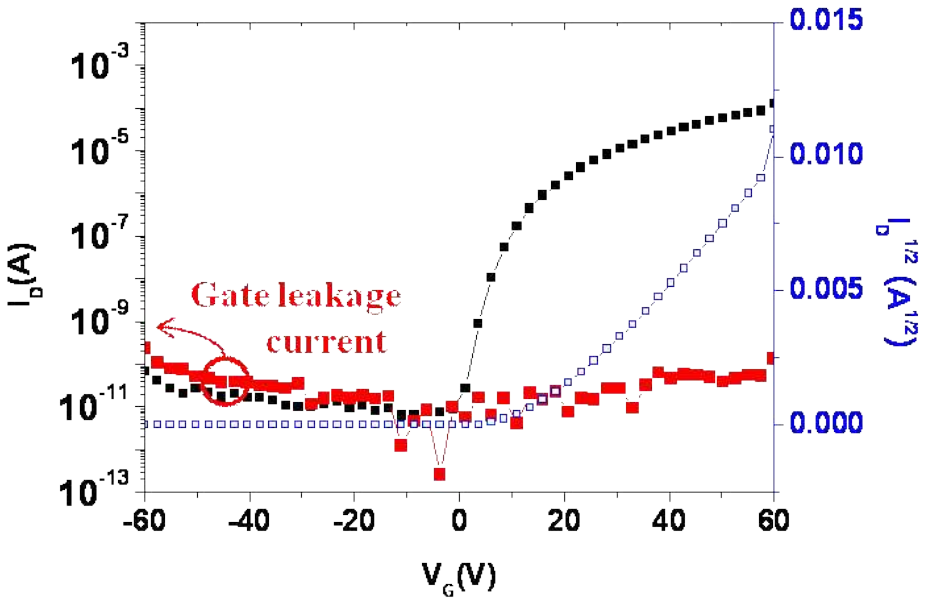


Figure 4.8. Transfer curve for patterned ZnO-TFT with stable gate leakage current at 200 °C. (W/L = 20)

Table 2. Electrical properties of patterned ZnO TFT on SiO_2 (operating voltage: 40 V). All devices are fabricated under ambient conditions. (This summarized information is the average of each 60 patterned TFTs by one run)

Anneal(°C)	V_{th}	$\mu(cm^2v^{-1}s^{-1})$	I_{on}/I_{off}
200	7.3	0.12	10^7
300	6.5	0.71	10^7~10^8

4.6 Flexible TTFT with polymer dielectric layer

Presently, the critical temperature of the plastic substrate for the flexible TTFT is around 200 °C. However, as the technology of the flexible substrate has developed, the critical temperature has been increased gradually to allow sintering at 300 °C. For this reason, we presented the average electric characteristics at 300 °C sintering. The flexible transparent display has many advantages over a panel display, in that it can be produced more cheaply. Low weight, high impact resistance, and a high degree of design are key advantages of producing an electronic device with a flexible substrate. Generally, as plastic substrates for flexible TTFTs have been limited by thermal degradation with a high-temperature process, low-temperature processing is essential for the solution-processed ZnO TFT. As semiconductor fabrication using an ammine-hydroxo zinc solution is applicable to a low-temperature process because of the outstanding volatility of the ammine which combines with the zinc hydroxide, we applied our method to ZnO flexible TTFT fabrication. Cross-linked poly(4-vinylphenol) (PVP) was used as the polymer dielectric layer (Figure 4.9a). Also, we made the patterned ZnO semiconductor with a 200 °C annealing process under ambient conditions, introducing the above method to the flexible TTFT (Figure 4.9b and 4.9c). The output curve and transfer curve of the TFT are presented as follows: the mobility, calculated from Figure 4.9e, μ = 0.13 $cm^2v^{-1}s^{-1}$, V_{th} = 2.5 V, and an on/off current ratio = 10^4 at V_D = 20 V can be seen in Figure 4.9d and 4.9e.

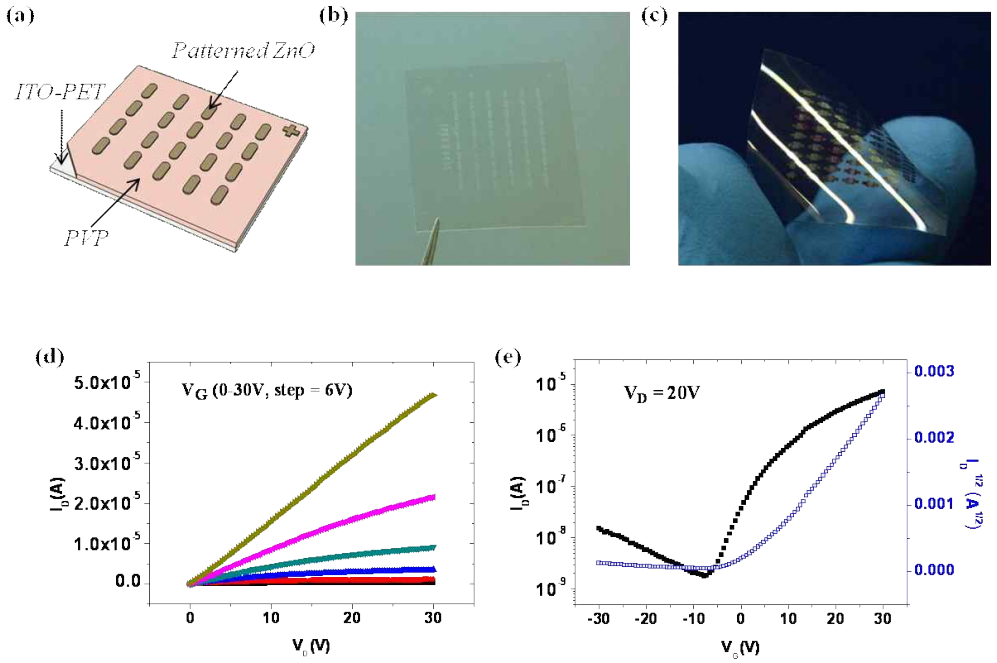


Figure 4.9. (a): Schematic illustration of a flexible TTFT; (b): optical image of patterned ZnO-TFT on ITO-PET; (c): Al source and drain electrodes deposited on the patterned ZnO; (d), (e): output curve and transfer curve for a patterned ZnO TFT on a PVP dielectric layer at 200 °C. (W/L = 20)

Also, we measured the changes of on-off current, mobility and flexible threshold voltage as flexible device during forward and backward bending (Figure 4.10). When the flexible TTFT bent to forward, the patterned ZnO semiconductor layer was compressed and the mobility and on current were increased at this compression state. Otherwise, when the flexible TTFT bent to backward, compressed ZnO layer was released and the on-off current and mobility were decreased. In overall changes of Figure 4.10a-c, the flexible patterned TTFT is the reliably available device without failure.

These electrical characteristics of the flexible TTFT were achieved in the patterned ZnO on the polymer dielectric layer in an all-soluble process except for the electrodes. Generally, the polymer dielectric layer caused a decrease in on/off ratio and threshold voltage because of the low capacitance of the polymer dielectric layer. Also, a little hysteresis was generated by polymer dielectric layer (see supporting information, Figure S6). However, we believe this can be solved using an advanced hybrid material as a dielectric. [22,23] The transmittance of the solution-processed ZnO on the PVP layer, obtained under UV-visible range photons (300 - 800 nm), is shown in Figure 4.11. The transmission spectrum of the patterned ZnO thin film on the PVP layer indicates that it is optically transparent; more than 85% transmittance was observed in most visible-light regions.

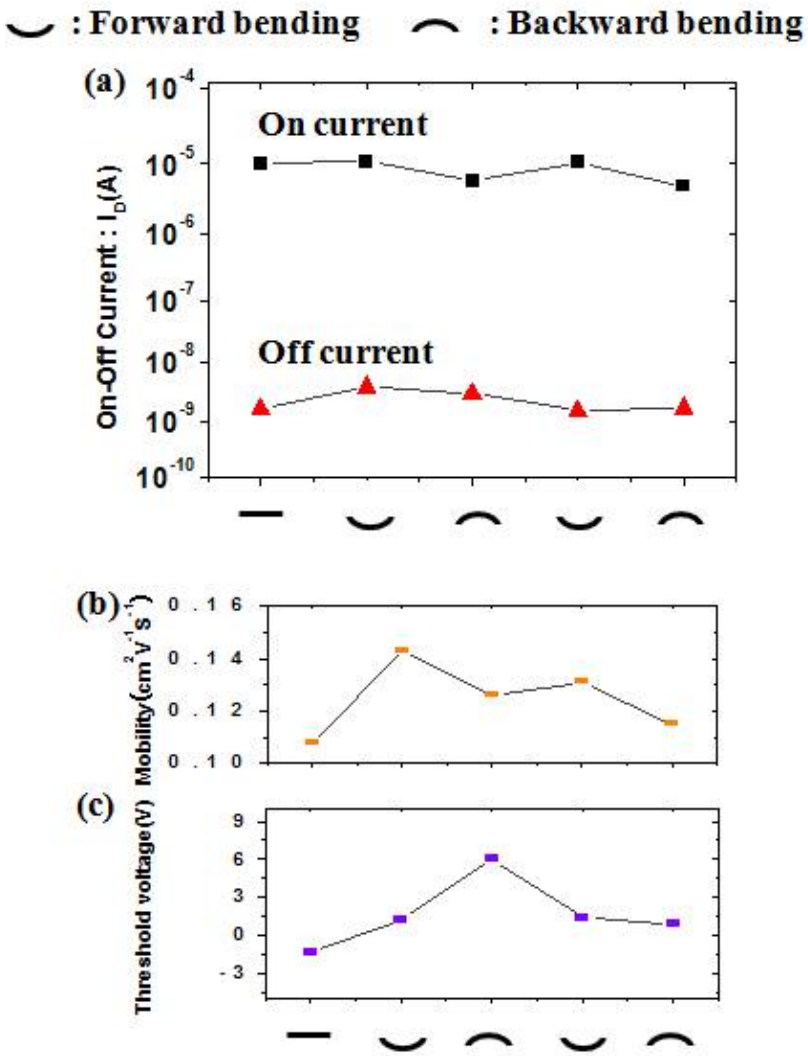


Figure 4.10. Forward and backward bending test data of patterned ZnO on flexible substrate with 10mm bending radius; (a) On-off current; (b) Field effect mobility; (c) Threshold voltage.

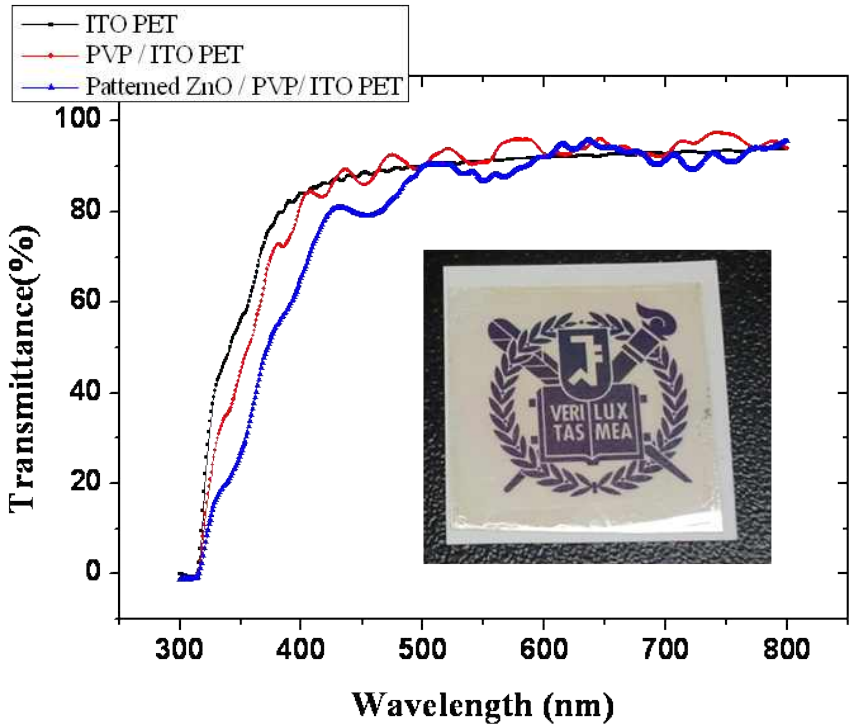


Figure 4.11. The transmittance of patterned ZnO films on ITO-PET as obtained under UV-visible range photons. (300 nm ~ 800 nm)

4.7 References

[1] J. Chang, and H. Sirringhaus, Adv. Mater. **2009**, 21, 2530 - 2535.

[2] P. Gorrn, F. Ghaffari, T. Riedl, and W. Kowalsky, Solid-State Electronics. **2009**, 53, 329 - 331.

[3] H. S. Shin, G. H. Kim, W. H. Jeong, B. D. Ahn, and H. J. Kim, Jpn. J. Appl. Phys. **2010**, 49, 03CB01.

[4] U. Ozgur, Ya. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. J. Cho , and H. Morkoc, Appl. Phys. Rev. **2005**, 98, 041301.

[5] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K.Jeong, Y. G. Mo, and H. D. Kim, Appl. Phys. Lett. **2007**, 90, 212114.

[6] S.Yoon, S.K.Park, C.Hwang, H.Y.Chu and K.I.Cho, Electrochem. Solid-State Lett. **2008**, 11, 2, J15-J18.

[7] S. H. K. Park, D. H. Cho, C. S. Hwang, S. Yang, M. K. Ryu, C. W. Byun, S. M. Yoon, W. S. Cheong, K. I. Cho, and J. H. Jeon, ETRI J. **2009**, 31, 653.

[8] K. Song, J. Noh, T. Jun, Y. Jung, H. Kang and J. Moon, Adv. Mater. **2010**, 22, 4308 - 4312.

[9] B. S. Ong, C. Li, Y. Li, Y. Wu and R. Loutfy, J. Am. Chem. Soc. **2007**, 129, 2750-2751.

[10] S. Jeong, Y. Ha, J. Moon, A. Facchetti and T. J. Marks, Adv. Mater. **2010**, 22, 1346 - 1350

[11] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, Nature Materials, **2011**, 10,

45 - 50.

[12] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, Science. 2000, 290, 2123.

[13] Licari, J.J. 2003. Coating Materials for Electronic Applications: Polymers, Pro-cesses, Reliability, Testing. Noyes Publications, William Andrew Publishing, New York.

[14] C. Chiang, K. S. Shores, M. Freindorf, T. Furlani, R. L. DeLeon, and J. F. Garvey, J. Phys. Chem. A. 2008, 112, 11559 - 11565.

[15] U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern, and H. Klauk et al, Adv. Mater. 2010, 22, 982 - 985.

[16] S. Jeong, G. Xia, B. H. Kim, D. O. Shin, S. Kwon, S. Kang, and S. O. Kim, Adv. Mater. 2008, 20, 1898 - 1904.

[17] C. Kim, J. Park, S. Kim, I. Song, S. Kim, Y. Park, E. Lee, B. Anass and J. Park, Electrochemical and Solid-State Letters. 2009, 12, 4, H95-H97.

[18] S. K. Park, Y. Kim and J. Han, J. Phys. D: Appl. Phys. 2009, 42, 125102.

[19] J. Kim, S. H. Lim, and Y. S. Kim, J. Am. Chem. Soc. 2010, 132, 42, 14721 - 14723.

[20] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. 2008, 130, 51.

[21] J. H. Cho, J. Lee, Y. Xia, B. S. Kim, Y. He, M. J. Renn, T. P. Lodge and C. D. Frisbie, Nature Materials. 2008, 7, 900.

[22] J. Kim, S. H. Lim, and Y. S. Kim, J. Am. Chem. Soc. 2010, 132,

14721.

[23] J. H. Cho, J. Lee, Y. Xia, B. S. Kim, Y. He, M. J. Renn, T. P. Lodge and C. D. Frisbie, Nat. Mater. 2008, 7, 900.

Chapter 5. Doping mechanism and integration for high electrical performance of inorganic TFT

5.1 Introduction

In the building of TFTs, semiconductor and gate dielectric are essential. Zinc oxide (ZnO) is gaining increasing interest as a solution-processed inorganic semiconductor, because it has high optical transparency as a wide bandgap (E_g= 3.3 eV) compound semiconductor, relatively good electrical performance, and low-temperature solution processability. The general form of solution processed ZnO is amorphous ZnO, the overlap of ns-orbital of metal oxide make conduction band to have high electrical property. This amorphous oxide semiconductor holds p-block positive ion that has (n-1)d10ns0 (n > 4) electronic configuration, such as In^{3+} ([Kr]4d105s0, n=5) in IGZO, which more effected the conductive property in N type doped ZnO than intrinsic ZnO. Thus, most researcher used doped ZnO to fabricate TFT, such as Indium zinc oxide(IZO), indium gallium zinc oxide(IGZO), zinc tin oxide(ZTO). Although the In leads to have high field effect mobility, However, this material has cost effective problem as rare earth material. Also, conventional solution processed doping method limited to fabricate flexible and transparent TFT by high annealing temperature as 400~500 °C. This is down to conventional sol-gel method using zinc acetate or zinc chloride that has high decomposition temperature over 400 °C to form ZnO. Thus, these defects are overcome with zinc ammonia complex that is ammonia based precursor solution. Since

ammonia has high volatility, the precursor solution can be formed easily ZnO at low temperature process.[1] Furthermore, the appropriate doping method for ammonia based ZnO precursor solution can be increased electrical property using alkali metal doping without high cost of synthetic rare earth material.

In order to promote the potential of solution-processed metal oxide TFTs, a considerable effort towards high performance gate dielectrics, as well as that for metal oxide semiconductors, is essential. In general, SiO_2 (dielectric constant 3.9) has been widely used in gate dielectrics for metal oxide TFTs because of its large band gap (8.9 eV) and small defect density.[2] In addition, SiO_2 is amorphous phase, which effectively prevents leakage current arising from structure defects and carrier tunneling induced by crystalline grain boundaries.[3] However, SiO_2 has an intrinsic limitation for high carrier induction in the semiconductor layer because of its intrinsically low dielectric constant. For these reasons, several alternative dielectrics with solution processability and high performance, such as ion gel,[4] self-assembled layer,[5] polymer electrolyte,[6] perovskite materials,[7-9] and sol - gel ionic crystalline alumina,[10] have been introduced. In particular, the ion gel dielectrics showed remarkable performance in TFTs. However, ion gel dielectrics do not show good compatibility with metal oxide semiconductors.[11,12] In addition, they are quite fragile in high temperature processes and hinder the further deposition process. Recently, Pal et al.[10] reported the crystalline sodium beta-alumina, which has a high dielectric constant and can

induce low-voltage, high performance TFT operation. However, in spite of a good performance, these are intrinsically crystalline structures and suffered from a relatively low on/off current ratio.[13] Also, the crystalline sodium beta-alumina requires a high temperature process (750 °C) for crystalline formation, which hinders the industrial applications for active matrix displays.

To address these issues, a simple solution process is herein introduced for high electrical performance TFTs with a low temperature annealing process at a maximum of 350 °C using the combination of nitrate ion (NO_3) coordinated amorphous Al_2O_3 dielectrics and ZnO-based semiconductors. In particular, we newly introduce the chemisorbed water effect of the amorphous ionic Al_2O_3 dielectrics with solution and low temperature processability for high-performance metal-oxide thin film transistors. We examined the electrical properties of water chemisorbed amorphous ionic Al_2O_3 dielectrics on the TFT performance through the solution-processed polycrystalline Li - ZnO[1] and amorphous In - ZnO[14] channel layers.

5.2 Alkali metal doping for solution-processed ZnO

For the N-type doping using alkali metal, the defect chemistry was accounted with Li in ZnO.[15,16] Na defect mechanism in the ZnO is very similar to the case of Li as a kind of the alkali metal.

$$Na \rightarrow Na_i^+ + e^- \quad \text{(Interstitial)} \quad (1)$$

$$Na \rightarrow Na'_{zn} + h^+ \quad \text{(Substitutional)} \quad (2)$$

The Li and Na defect mechanism could be demonstrated to both the interstitial doping of alkali metal ion and the substitutional doping, that alkali metal have potentials into the 4-fold coordinated O atoms in ZnO crystal structure by Equation (1 & 2). However, alkali metal easily formed the interstitial defects more than the substitutional exchange of Zn in the ZnO matrix. Because the energy of alkali metal substitution exchange is higher than the energy of alkali metal interstitial doping like the case of Li defect mechanism.[17] It means that the interstitial doping is superior on alkali metal doping in ZnO at low temperature as N-type doping.

N doping mechanism and ammonia ZnO precursor solution can make higher filed effect mobility and on/off current ratio.[1] Transfer characteristics of both intrinsic and doping TFT are fabricated at 300 °C and shown in Figure 5.1. The μ_{sat} of intrinsic ZnO and Li-ZnO TFTs on the SiO_2 dielectric with 300 °C annealing corresponding are 1.1 $cm^2V^{-1}s^{-1}$ and 7.5 $cm^2V^{-1}s^{-1}$, respectively. The Li ion doping effect sufficiently raised 7 times of the electrical property from intrinsic ZnO with higher on/off current ratio. N-type doping without In is possible using several alkali metal precursor in order to increase

electrical property like the results of previously reported our group paper[1].

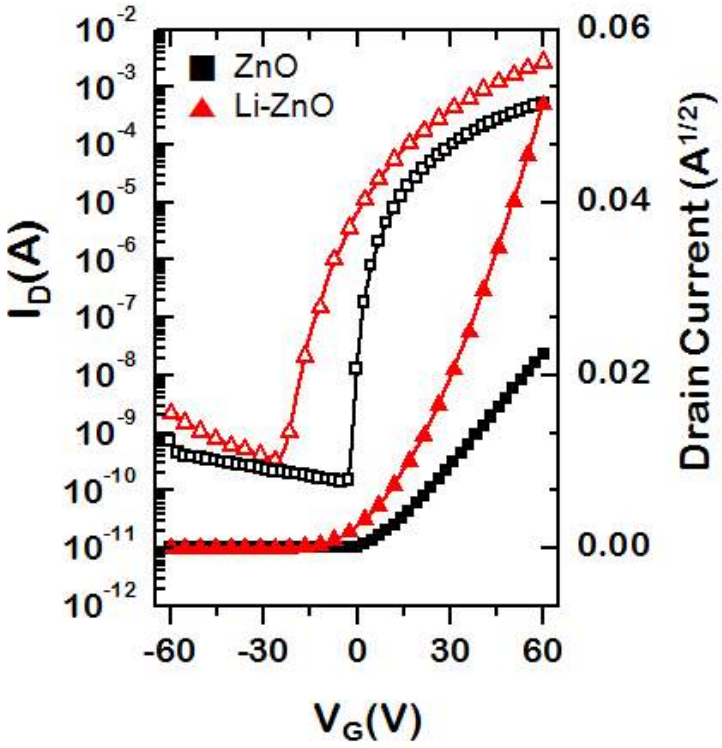


Figure 5.1. Transfer curves of ZnO-TFT and Li-ZnO TFT on SiO_2 dielectric layer at 300 °C. (W/L = 20)

5.3 Ionic amorphous dielectric layer for ZnO TFTs

In order to verify the good performance of solution-processed amorphous ionic Al_2O_3 dielectrics, the solution-processed polycrystalline Li-ZnO and amorphous In-ZnO semiconductor layer were fabricated on the amorphous ionic Al_2O_3 dielectric layer with annealing at 300 °C for 1hour as the bottom gate & top electrode structured TFTs.(Figure 5.2a) The thickness of Al_2O_3 dielectric layer by the consecutive 10 times spin-coating was observed as 242 nm by the high resolution transmission electron micrograph (HR-TEM). (Figure 5.3) To control the thickness of Al_2O_3 dielectric layer, we conducted the consecutive spin-coating process, which the one spin-coating step was consisted with the spin-coating with precursor at 3000 rpm and then soft baking at 240 °C for 3 min. The both polycrystalline Li-ZnO semiconductor layer and the amorphous In-ZnO semiconductor layer were well fabricated on the amorphous Al_2O_3 dielectric layer(Figure 5.2b and 5.2c). After annealing at 300°C for 1 hour, the thickness of polycrystalline Li-ZnO layer was shown as 6.07 nm and that of amorphous In-ZnO layer was shown as 11.28 nm by the HR-TEM. (NO_3^-) was formed, which was proved by FT-IR, detection of negative ion using TOF-SIMS, and XPS depth profile (Figure 5.4b-e). As remaining NO_3^- ions were induced more electrostatic attraction with water, the water adsorption effect was effectively activated in our ionic Al_2O_3 layer. The existence of ions was characterized through the analysis of TG-DTA, FT-IR, TOF-SIMS, and XPS depth profile (Figure 5.4a-e). In the TG-DTA

of ionic Al_2O_3 dielectric layer, weight loss percent was gradually decreased(Figure 5.4a). The gradual weight loss was originated from evaporation of solvent, decomposition of nitrate groups, and dehydroxylation reaction.

To know the formation of solution-processed Al_2O_3 film, we measured the FT-IR as a function of annealed temperature. The hydroxyl groups or adsorption water was assigned to 3000-3500 cm^{-1}.[18] The peaks at 2939, 2886, and 2836 cm^{-1} indicate C - H stretching vibrations.[24] The peaks in the range of 1200-1700 cm^{-1} design at nitrate deformation vibration.[19] The solvent associated peaks in range of 700-1100 cm^{-1}, which area tributed to carbonate species.[20] The solvent related peaks were decreased up to 300 °C and fully eliminated at 350 °C. The nitrate groups and hydroxyl species were still remained until 350 °C. Therefore, the 350 °C annealed Al_2O_3 film has small amounts of hydroxyl and nitrate groups; meanwhile the 500 °C annealed Al_2O_3 film contains no hydroxyl and nitrate groups because of its high decomposition temperature.

To compare the existence of ions in the 350°C and 500°C annealed Al_2O_3 film, the TOF-SIMS is measured (Figure 5.4c-d). In the analyses of TOF-SIMS, the NO^{3-} ions were accurately detected in the Al_2O_3 dielectric layer with 350 °C annealing (Figure 5.4c). This means that the small amount of NO^{3-} existed in the ionic Al_2O_3 dielectric layer with 350 °C. The NO^{3-} ions-embedded in Al_2O_3 layer completely disappeared and transformed to intrinsic Al_2O_3 after high

temperature annealing process at over 500 °C (Figure 5.4c-d). Contrary to the case of the NO^{3-} ions, the intensity of Al^{3+} ions and O^{2-} ions were approximately equal between TOF-SIMS data of the Al_2O_3 dielectric layer with either 350 °C annealing or with 500 °C annealing(Figure 5.4c-d). In comparing the data of TOF-SIMS of 350 °C annealed Al_2O_3 layer and the data of TOF-SIMS of 500 °C annealed Al_2O_3 layer, we observed that the NO^{3-} ions embedded in ionic Al_2O_3 dielectric proportionally interrelated with H^+. The electrostatic adsorbed water molecules on hydroxyl groups in Al_2O_3 film form selectrical double layers and attracts more charge carriers at semiconductor/dielectric interface resulting in high performance characteristics by additional effect of NO^{3-} ions.

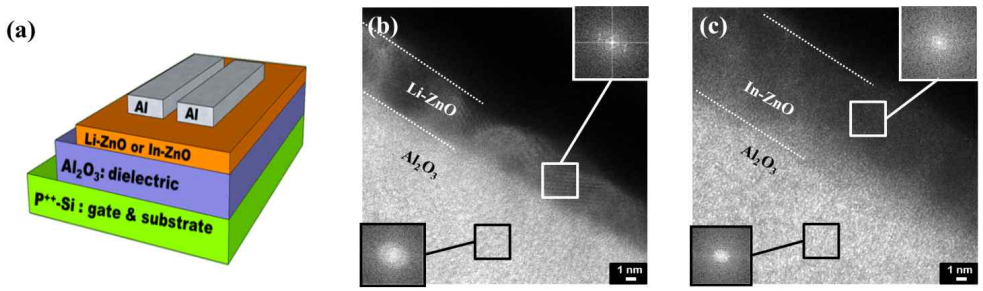


Figure 5.2. (a) Simple illustration of the bottom gate & top contact thin film transistor was shown. (b) The polycrystalline structure of Li-ZnO semiconductor films and (c) the amorphous structure of In-ZnO semiconductor films were well fabricated on the amorphous of Al_2O_3 dielectric layer that were shown by HR-TEM. All films were annealed at 350 °C.

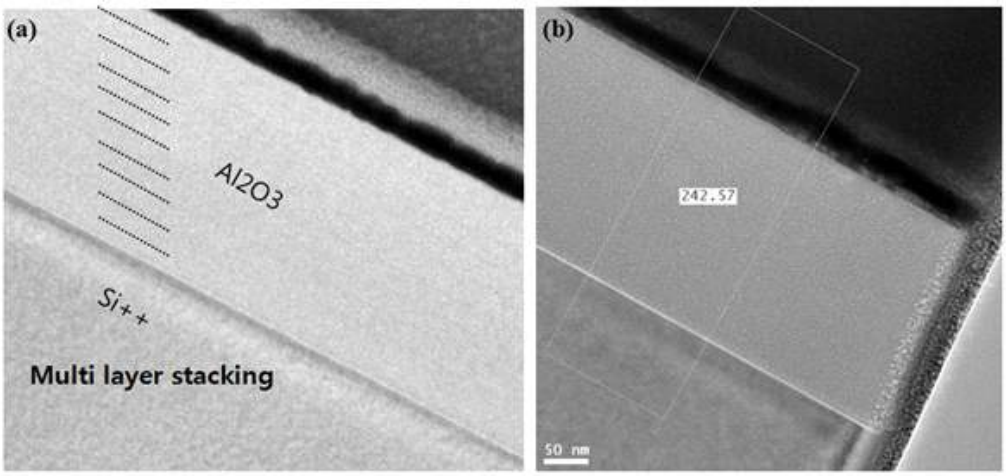
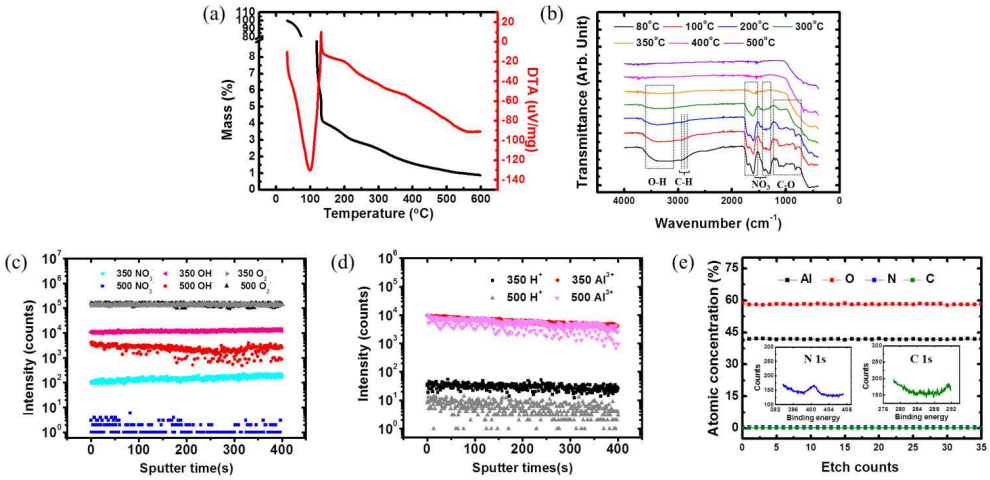


Figure 5.3. The HR-TEM images of solution processed ionic amorphous Al_2O_3 dielectric layer were shown. (a) The 10 times coated ionic amorphous Al_2O_3 layer was fabricated on the heavily boron doped Si wafer and (b) the thickness of amorphous ionic Al_2O_3 layer was 242.57 nm.



Ficture 5.4. (a) Thermogravimetric differential thermal analysis (TG-DTA) of the ionic Al_2O_3 dielectric layer was analyzed from 0°C to 600 °C. (b) FT-IR measurement of Al_2O_3 film as a function of temperature. The black dot indicates molecules vibration. (c) The existence of negative ions and (d) The existence of positive ions in ionic Al_2O_3 dielectrics were analyzed by TOF-SIMS. (e) The XPS depth profile of 350 °C annealed Al_2O_3 film. The insets indicate N1s and C1s peaks.

5.4 Electrical characteristics of integrated metal oxide TFT

In the study of the potential of solution-processed amorphous ionic Al_2O_3 dielectrics toward high performance dielectrics, we investigated the current-voltage characteristics from the simple electrode-insulator-electrode structure, Al/amorphous ionic Al_2O_3/p++-Si wafer. The thickness of the Al_2O_3 dielectric layer with 350 °C and 500 °C annealing conditions were 242 nm and 215 nm (Figure 5.3b). They effectively blocked a leakage current, and their leakage current densities of Al_2O_3 dielectric layer with 350 °C and 500 °C annealing conditions were 4.1×10^{-6} A/cm^2 and 4.6×10^{-9} A/cm^2 at 1 MV/cm, respectively (Figure 5.5). These results showed that a solution-processed ionic amorphous Al_2O_3 dielectric layer is suitable in use of gate dielectric layer. Also, the ionic amorphous Al_2O_3 dielectric layers were shown that it is optically transparent over 95% transmittance in most visible-light regions so that it can be applied to transparent display (Figure 5.6).

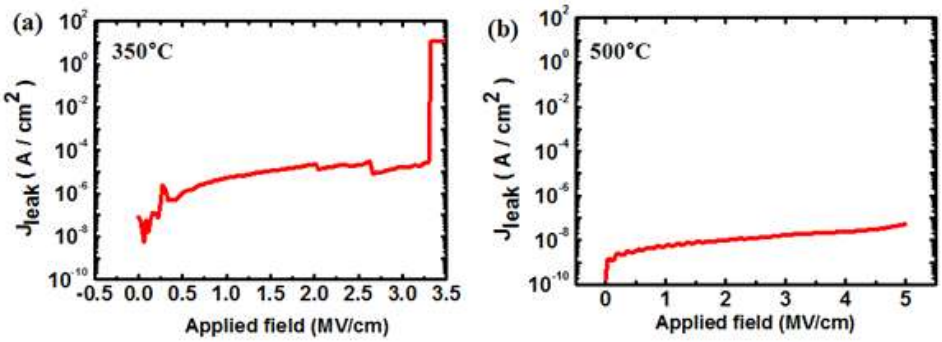


Figure 5.5. Leakage current density of (a) 350 °C and (b) 500 °C annealed amorphous Al_2O_3 dielectric with thickness of 242 nm and 200 nm, respectively. Their values are 4.1×10^{-6}A/cm^2 and 4.6×10^{-9} A/cm^2 at 1 MV/cm, respectively.

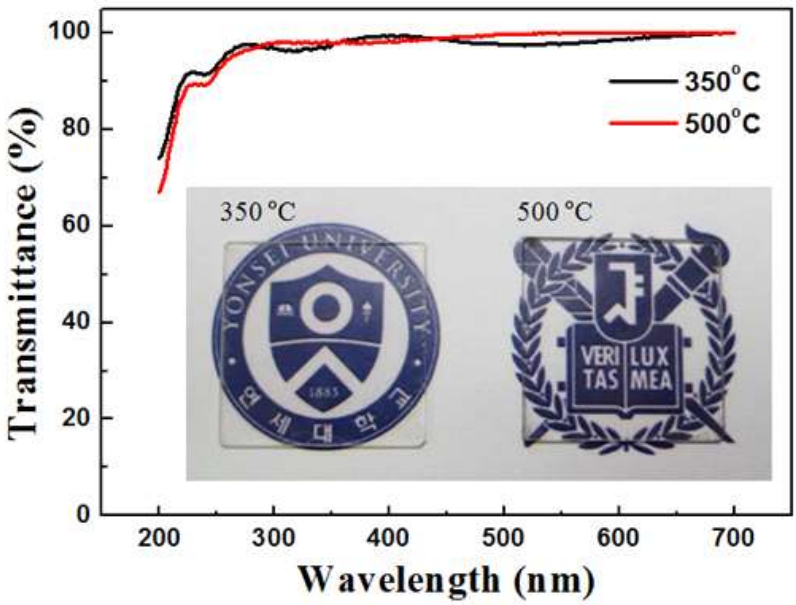


Figure 5.6. The transmittance of ionic amorphous Al_2O_3 dielectric layers on quartz glass under UV-visible range photons.(200 nm~700 nm)

To evaluate the nitrate ion embedded Al_2O_3 thin film as high performance gate dielectric, bottom gate top contact structure TFT was fabricated with poly crystalline Li-ZnO and amorphous In-ZnO channel layer. The simple illustration of the TFT structure was shown in figure 5a. In order to verify the good performance of solution-processed amorphous ionic Al_2O_3 dielectrics, the solution-processed polycrystalline Li-ZnO[1] and amorphous In-ZnO[14] semiconductor layer were fabricated on the amorphous ionic Al_2O_3 dielectric layer with annealing at 350 °C. Both the poly crystalline Li-ZnO semiconductor layer and the amorphous In-ZnO semiconductor layer were well fabricated on the amorphous Al_2O_3 dielectric layer(Figure 5.2b-c). The thickness of the polycrystalline Li-ZnO layer was shown as 6.07 nm and that of the amorphous In-ZnO layer was shown as 11.28 nm.

Electrical characteristics of Li-ZnO TFTs and In-ZnO TFTs on ionic Al_2O_3 dielectric with a 350 °C annealing condition were shown in Figure 5.7. Figure 5.7a-c shows the electrical properties of polycrystalline Li-ZnO TFTs, and figure 6d-f shows the electrical properties of amorphous In-ZnO TFTs. To avoid overestimation of mobility, we adopted the capacitance value at 20 Hz. If we apply the lowest capacitance value at 1 MHz, the calculated mobility values of both TFTs are over 200 $cm^2V^{-1}s^{-1}$, which is preposterous value. Therefore, we selected the capacitance value of 350°C and 500 °C annealed Al_2O_3 film at 20Hz.

In polycrystalline Li-ZnO TFTs, output curves with gate voltage

(V_G) that was varied from 0 to 10 V in step of 2 V showed a good saturation behavior with maximum drain current of 3.4 mA at Vg = 10V (Figure 5.7a). Transfer curve with drain current (V_D) of 10 V informed the saturation mobility (μ_{sat}) of 46.9 $cm^2V^{-1}s^{-1}$, which were calculated with the capacitance of 143.7 nF/cm^2 at 20 Hz frequency, at hreshold voltage of 0.2 V, and an on/off current ratio ($I_{on/off}$) of over 10^5 (Figure 5.7b). The hysteresis of V_{th} was ~1.41V at the sweeping speed of ~4V/s and showed a counter-clock wise direction (Figure 5.7d). On consecutive 10 times hysteresis tests, the electrical characteristics were stable. In case of amorphous In-ZnO TFTs, their electrical characteristics were investigated on the conditions of V_G and V_D, which were varied between 0 and 5 V in step of 1 V. In Figure 5.7d-e, they showed a good saturation behavior with maximum drain current of 1 mA at Vg = 5 V. Also, the threshold voltage was 0.2 V and I_{on}/I_{off} was over 10^4. The calculated μ_{sat} was 44.2 $cm^2V^{-1}s^{-1}$ with capacitance of 143.7 nF/cm^2 at 20 Hz frequency. On consecutive 10 times hysteresis tests, the hysteresis of V_{th} was ~0.69 V at the sweeping speed of ~ 4 V/s and showed a counter-clockwise direction (Figure 5.7f).

Both kinds of TFTs showed the dramatically enhanced field effect mobility with low V_{th} of 1±0.5 V. Also, they showed stable, durable, and reproducible performance. These enhanced electrical performances were induced by the H^+ ions in ionic Al_2O_3 dielectric layers. Because of the high dielectric performance induced by high dielectric constant of water, the ionic amorphous Al_2O_3 dielectric layers remarkably

elevated the field effect mobility of metal oxide TFTs. Furthermore, the addition of H_2O_2 in the precursor effectively suppressed the oxygen vacancies in dielectric layers, which work as the electron traps or pass, and considerably promoted the response of the Al_2O_3 dielectric layer.

There were the small hysteresis shifts of V_{th} in round-operations, because the H^+ ions from adsorbed water in Al_2O_3 dielectric layers caused the counter-clockwise hysteresis. In spite of the small hysteresis shifts of V_{th}, they cannot cheapen the remarkable electrical performance of ionic embedded Al_2O_3 dielectrics, because these small values can be faithfully controlled through the integrated circuit design for active matrix. 30 On the other hands, in case of Li-ZnO and In-ZnO TFT on 500 °C annealed Al_2O_3 dielectric layers, the field effect mobilities were considerably reduced and the hysteresis disappeared in both cases because of the disappearance of NO_3^- ion coordinated effect in Al_2O_3 dielectric layers (Figure 5.8). Moreover, the hysteresis direction changed to clockwise direction and it revealed that the 500 °C annealed Al_2O_3 did not contained mobileions, which lead to counter-clockwise hysteresis direction.[6,21] The capacitance frequency characteristics of 500 °C annealed Al_2O_3 dielectric is shown in Figure 5.9. The obtained capacitance was uniform, and its value was 28 ± 0.686 nF/cm^2 in the whole range of frequencies. The μ_{sat} of Li-ZnO and In-ZnO TFTs on the Al_2O_3 dielectric with 500 °C annealing corresponding to the capacitance value at 20 Hz are 3.4 $cm^2V^{-1}s^{-1}$ and 2.34 $cm^2V^{-1}s^{-1}$, respectively. The electrical

characteristics of the polycrystalline Li-ZnO and amorphous In-ZnO TFT on the 350 °C and 500 °C annealed Al_2O_3 dielectric were summarized in Table 5.1.

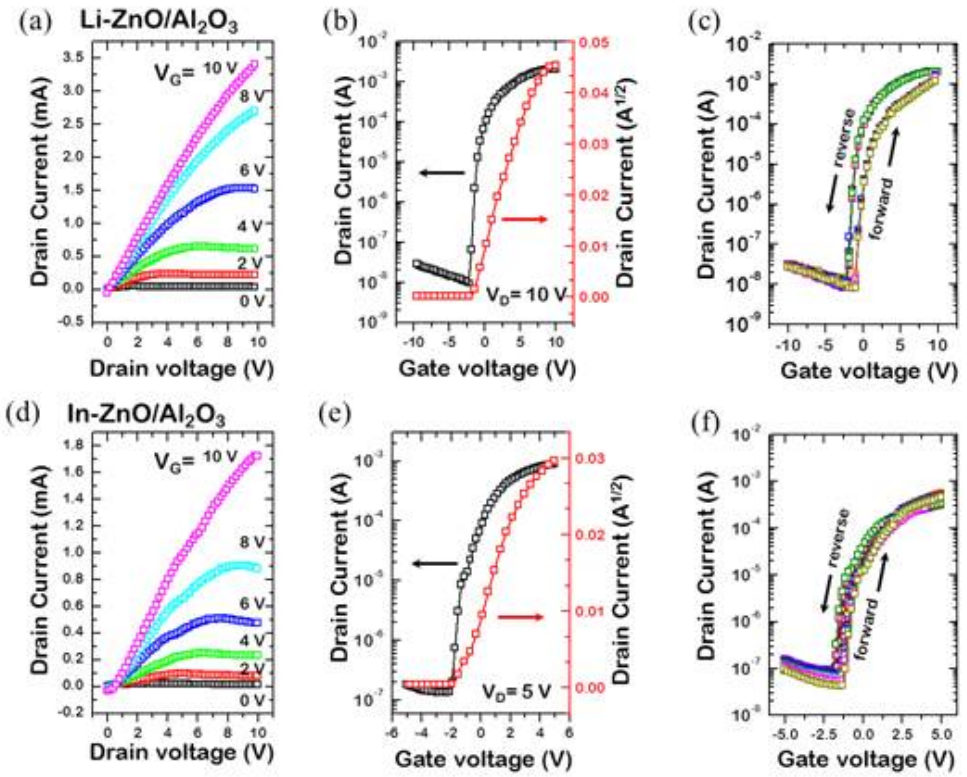


Figure 5.7. (a) Output curve, (b) transfer curve, and (c) count clock wise-hysteresis with 10 times sweep of Li-ZnO TFTs on ionic amorphous Al_2O_3 dielectric layer. (d) Output curve, (e) transfer curve and (f)counter clockwise-hysteresis with 10 times sweep of In-ZnO TFTs on ionic amorphous Al_2O_3 dielectric layer. The annealing temperature of ionic amorphous Al_2O_3 dielectric layer was 350 ˚C.

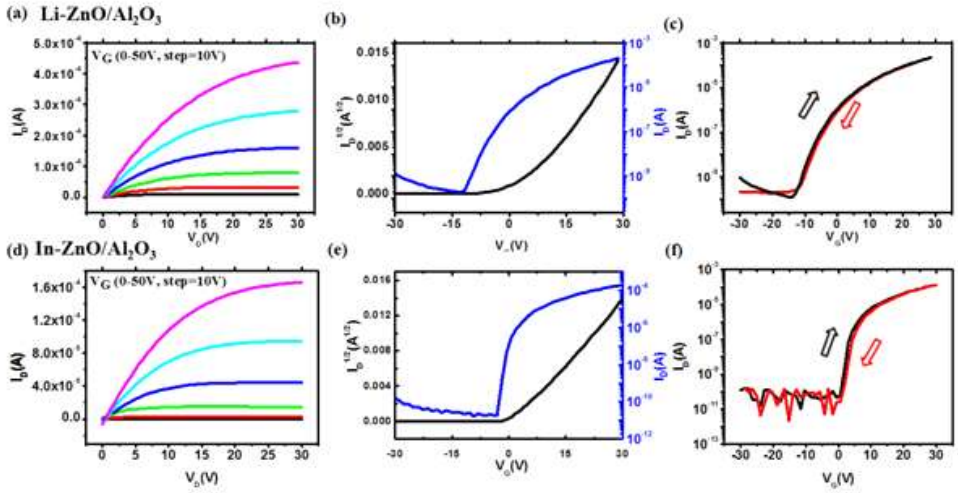


Figure 5.8. (a) Output curve of TFTs consisted of 350 °C annealed Li-ZnO semiconductor film on 500 °C annealed Al_2O_3 dielectric layer with the sweep of 10V steps on gate voltage from 0V to 50V. (b) Transfer curve of Li-ZnO/Al_2O_3 TFT with drain current of 30V. (c) Clockwise hysteresis of Li-ZnO/Al_2O_3 TFT. (d) Output curve of 350 °C annealed In-ZnO on 500 °C annealed Al_2O_3 dielectric layer with sweep of 10V steps on gate voltage from 0V to 50V. (e) Transfer curve of In-ZnO/Al_2O_3 TFT with drain current of 30V. (f) Clockwise hysteresis of In-ZnO/Al_2O_3 TFT.

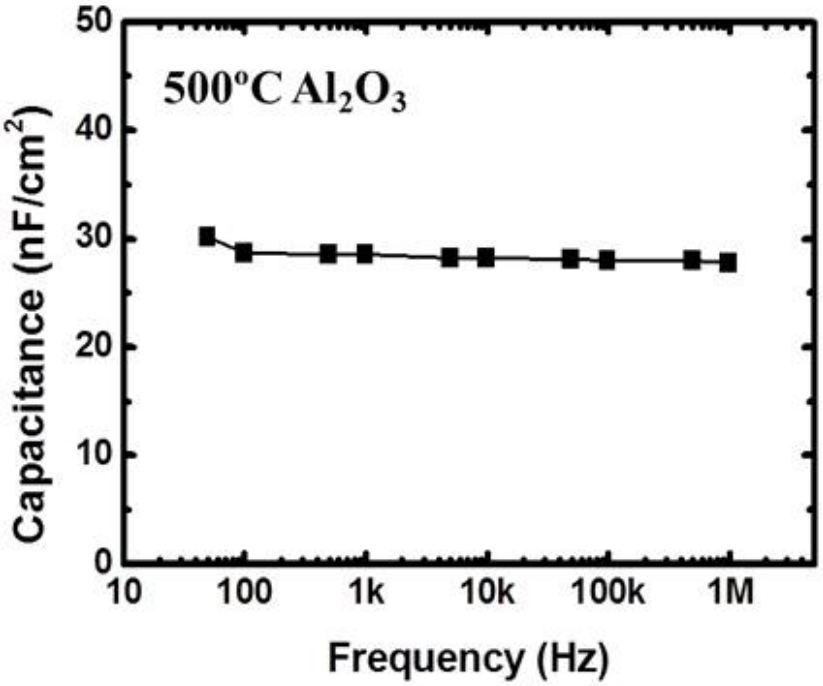


Figure 5.9. Frequency vs capacitance of 500 °C annealed Al_2O_3 dielectric layer with thickness of 215 nm.

Table 5.1. Summarized the capacitance of 350 °C and 500 °C annealed Al_2O_3 thin film at 20Hz and TFT performance parameters with Li-ZnO and In-ZnO channel layers. The mobility was calculated by using the capacitance value at 20Hz.

Dielectric Temperature (°C)	Capacitance At 20Hz (nF/cm^2)	Channel Material	Mobility (cm^2/Vs)	V_{th} (V)	I_{on}/I_{off}	S.S (V/dec)
350	143.7	Li-ZnO	46.9	0.2	4.64×10^5	0.264
		In-ZnO	44.2	0.2	3.17×10^4	0.344
500	36.2	Li-ZnO	3.4	6.43	2.34×10^6	2.469
		In-ZnO	2.34	2.29	1.18×10^7	0.722

5.5 water adsorption effects of ionic amorphous dielectric

To investigate in detail the dielectric behaviors of solution-processed ionic amorphous Al_2O_3 dielectric, we measured the frequency vs. capacitance characteristics with the variation of film thickness - spin coating count (Figure 5.10). Thickness of 2, 4, 6, 8, and 10 times coated Al_2O_3 films with 350 °C annealing condition were 53.1, 105.5, 163.6, 210, and 242 nm, respectively. The capacitance was changed reversely with the variation of thickness. For example, 2 and 10 times coated ionic implanted Al_2O_3 films show capacitance of 209 nF/cm^2 and 143.7 nF/cm^2, respectively, at 20 Hz. Furthermore, they showed a high value of capacitance at a low frequency operation and a low value of capacitance at high frequency operation. In general, the capacitance of conventional dielectric films shows a constant value regardless of frequency. However, the solution-processed ionic amorphous Al_2O_3 dielectrics showed the frequency dependent dielectric behaviors like the ion gel dielectric layer.[12] These variations were induced from mobile proton of H^+ in Al_2O_3 dielectrics. The H^+ ions in Al_2O_3 film easily formed the electrical double layers(EDL) and remarkably enhanced the dielectric constant of Al_2O_3 dielectric films.[22]

From the results of capacitance and impedance analysis in Figure 5.11, we verified that the Al_2O_3 thin film contained positive or negative mobile ions such as proton or nitrate groups. To clarify major mobile ions for the enhancement of electrical performance,

capacitance - frequency measurement of 350 °C annealed Al_2O_3 thin film was investigated under various heating condition with 20 % relative humidity (RH) and the results are shown in Figure 5.11a-c. The capacitance of Al_2O_3 film measured under the heating condition at 15 ˚C showed the capacitance of 97.3 nF/cm^2 at 20Hz(Figure 3a). As the heating condition increased up to 60 °C, the capacitance at 20 Hz gradually increased from 97.3 nF/cm^2 to 174.8 nF/cm^2(Figure 5.11a). This capacitance increment may be originated from enhanced ion conductivity by nitrate ion coordinated water adsorption effect. Additionally, capacitance of Al_2O_3 film at 20 Hz gradually decreases from 174.8 nF/cm^2 to 39.3 nF/cm^2 as thermal treatment temperature increases from 60 ˚C to 150 ˚C, respectively (Figure 5.11b). In case of the thermal treatment condition at 150 °C, interestingly, the capacitance value of Al_2O_3 film showed almost constant about 29.4 nF/cm^2 with standard deviation of 4.819 nF/cm^2 in Figure 5.11b. Through the results of capacitance - frequency (Hz) measurements under various thermal treatments, we can conclude that water is negative mobile ions such as proton or nitrate groups. To clarify major mobile ions for the enhancement of electrical performance, capacitance - frequency measurement of 350 °C annealed Al_2O_3 thin film was investigated under various heating condition with 20 % relative humidity (RH) and the results are shown in figure 3a-c. The capacitance of Al_2O_3 film measured under the heating condition at 15 °C showed the capacitance of 97.3 nF/cm^2 at 20Hz(Figure 5.11a). As the heating condition increased up to 60 °C, the capacitance at 20 Hz

gradually increased from 97.3 nF/cm^2 to 174.8 nF/cm^2(Figure 5.11a). This capacitance increment may be originated from enhanced ion conductivity by nitrate ion coordinated water adsorption effect. Additionally, capacitance of Al_2O_3 film at 20 Hz gradually decreases from 174.8 nF/cm^2 to 39.3 nF/cm^2 as thermal treatment temperature increases from 60 °C to 150 °C, respectively (Figure 5.11b). In case of the thermal treatment condition at 150 °C, interestingly, the capacitance value of Al_2O_3 film showed almost constant about 29.4 nF/cm^2 with standard deviation of 4.819 nF/cm^2 in Figure 5.11b. Through the results of capacitance - frequency (Hz) measurements under various thermal treatments, we can conclude that water is they showed a constant capacitance value about 28.4 nF/cm^2 with standard deviation of 0.694 nF/cm^2 at 15°C~150°C (Figure 3d-e). It reveals that the 500 °C annealed Al_2O_3 film doesn't have water adsorbed effect in ambient air condition due to elimination of nitrate ionin Al_2O_3 layer. However, the capacitance of 500 °C annealed Al_2O_3 film at 40% RH shows high capacitance value from 120 nF/cm^2 to 27 nF/cm^2 in whole frequency region (Figure 3d). This phenomenon is similar characteristic with intrinsic Al_2O_3, which can be affected by water adsorption over 40 %RH.[23] The value of capacitance of 500 °C annealed Al_2O_3 film under 40% RH is smaller than 350 °C annealed Al_2O_3 film because of dense structures with small porosity and the absence of the NO^{3-} ions in 500 °C annealed Al_2O_3 layer. From the analyses of capacitances under various thermal treatment conditions, I can conclude that the NO^{3-} ions in 350 °C annealed Al_2O_3 film assist

the adsorption of water molecules by electrostatic force[24] and the EDL formation by H^+ ions resulting in high capacitance at low frequency.

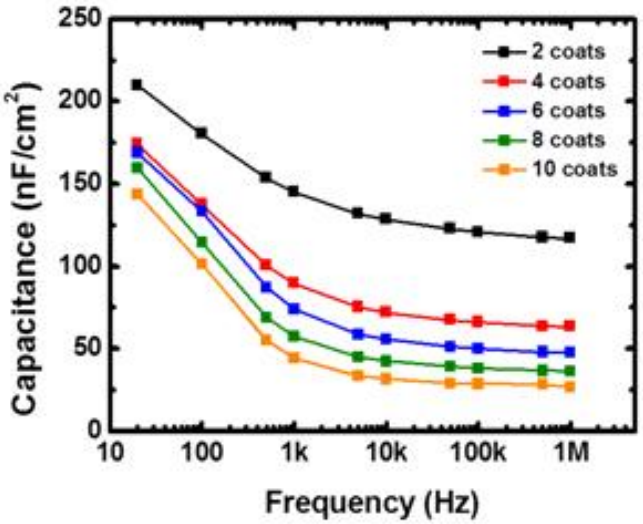


Figure 5.10. Frequency vs. capacitance of 350 °C annealed ionic Al_2O_3 dielectric layer with various film thickness designed by spin-coating counts.

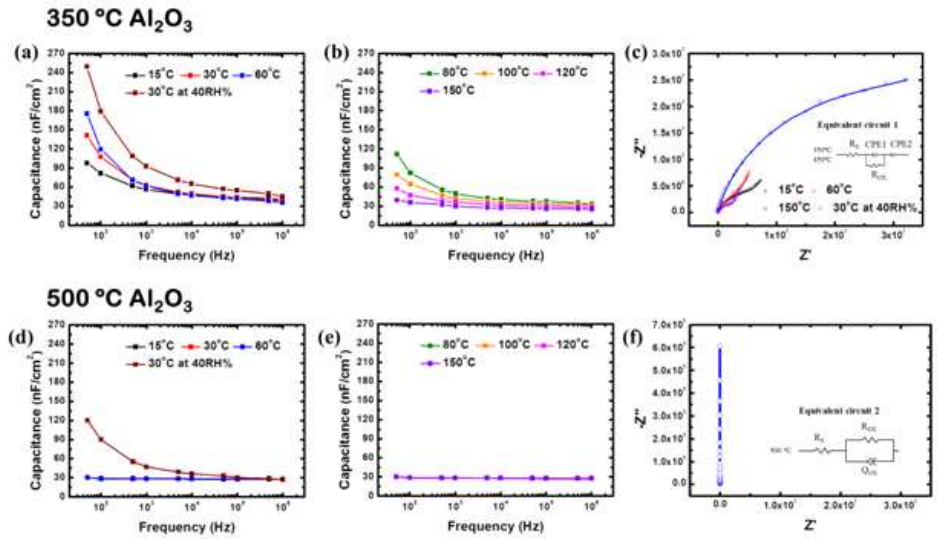


Figure 5.11. The capacitance of 350 °C annealed Al_2O_3 film with MIM structure of Au/Al_2O_3/p++-Si at (a) 15, 30, 60, (b)80, 100, 120,and 150ºC thermal treatment conditions. Measured capacitance values of 350 °C annealed Al_2O_3 film under 40 RH% at 30 °C express brown color. (c) Relative impedance spectroscopic datas of 350 °C annealed Al_2O_3 film corresponding to thermal treatment conditions with fit data using equivalent circuit 1. Symbols show the observed resistance(Z') and reactance (Z"), and solid lines show the nonlinear least-squares fitting results by each equivalent circuit modeling. The capacitance of 500 °C annealed Al_2O_3 film with MIM structure of Aul/Al_2O_3/p++-Si at (d) 15, 30, 60,(e) 80, 100, 120, and 150°C thermal treatment conditions. Measured capacitance values of 500 °C annealed Al_2O_3 film under 40 RH% at 30 °C express brown color. (f) Relative impedance spectroscopic datas of 500 °C annealed Al_2O_3 film corresponding to thermal treatment conditions with fit data using equivalent circuit 2.

However, these analyses showed indirect evidence of water adsorption effect. Thus we directly monitored water adsorption and desorption phenomenon on the Al_2O_3 film by FT-IR and spectroscopic ellipsometry. Figure 5.12a-b show the FT-IR results of water adsorption and desorption on the 350 °C and 500 °C annealed Al_2O_3 film. The 3000-3500 cm^{-1} indicates the adsorbed water stretching vibrations.[25] 350 °C annealed Al_2O_3 film has small amount of adsorbed water (Figure 4a). To evaluate water desorption characteristics, 350 °C annealed Al_2O_3 thin film placed on the 150 °C set hot plate for 5 min and immediately measured FT-IR. After 150 °C thermal treatment, there is no water adsorption related peaks and it reveals that adsorbed water was desorbed. After measuring FT-IR, the sample stored in ambient condition for 10 min and re-measured. It also has small amount of water adsorption peaks. Water molecules can be easily adsorbed with the help of hydroxyl and nitrate groups in 350 °C annealed Al_2O_3 film. On the other hand, 500 °C annealed Al_2O_3 film shows different behaviors. The same measurement was conducted and the result was shown in Figure 5.12b. The 500 °C annealed Al_2O_3 film shows rarely water adsorption related peaks regardless of 150 °C thermal treatment and recovery measurement because of lack of hydroxyl and nitrate groups. From the result of water adsorption and desorption experiments, we conclude that the adsorbed species on the 350 °C annealed Al_2O_3 film are water molecules and it leads to high capacitance value at low frequency.

The refractive index (n) of water is 1.335, which is smaller than 350

°C annealed Al_2O_3 film (n=1.542, at 550nm, figure 4c). By utilizing the difference between two values, adsorption and desorption characteristics of water can be known. Thus we performed ellipsometric porosimetry measurement and the results were shown in Figure 5.12c,d. Then value of 350 °C annealed Al_2O_3 film is 1.542, which is lower than bulk Al_2O_3 value (n=1.771). After 150 °C thermal treatment for 10 min, the n value is abruptly decreased from 1.542 to 1.502 because of water desorption. Moreover, we monitored the recovery behavior by multiple sweeping measurements. As the sweeping count increases, the n value is recovered its initial state. The restoration time is only 2 min. In contrast, the n value of 500 °C annealed Al_2O_3 film is 1.668, which is higher than 350 °C annealed Al_2O_3 film. It means that 500 °C annealed Al_2O_3 film is dense by eliminating hydroxyl and nitrate groups. Then value of 500 °C annealed Al_2O_3 film is nearly constant regardless of 150 °C thermal treatment for 10 min. This result reveals that the water adsorption characteristic is rarely observed in 500 °C annealed Al_2O_3film. Through FT-IR measurement under 150 °C thermal treatment, the water adsorption and desorption behavior are confirmed and monitored by FT-IR and ellipsometric porosimetry measurement.

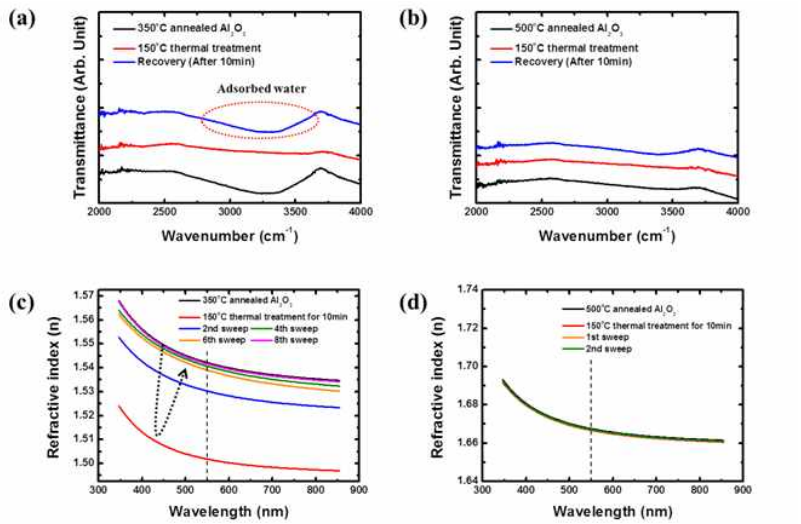


Figure 5.12. The water adsorption, desorption, and recovery characteristics of (a) 350 °C and (b) 500 °C annealed Al_2O_3films were monitored by FT-IR in ambient conditions. The peak in range of 3000-3500 cm^{-1} represents adsorbed water. To measure the water desorption behavior, 150 °C thermal treatment was conducted for 5 min and immediately measured FT-IR. The ellipsometric porosimetry measurement of (c) 350 °C and (d) 500 °C annealed Al_2O_3 films were carried out to observe the water adsorption and desorption characteristics. There fractive index of 350 °C and 500 °C annealed Al_2O_3 films were 1.542 and 1.668, respectively, at 550nm. There fractive index of water is 1.335. By using the difference between two values, water adsorption and desorption characteristics were shown.

5.6 References

[1] S. Y. Park, B. J. Kim, K. Kim, M. S. Kang, K. Lim, T. I. Lee,J. M. Myoung, H. K. Baik, J. H. Cho and Y. S. Kim, Adv. Mater., 2012, 24, 834.

[2] E. P. O'Reilly and J. Robertson, Phys. Rev. B, 1983, 27, 3780.

[3] M. Furuta, T. Nakanishi, M. Kimura, T. Hiramatsu, T. Matsuda, H. Furuta, T. Kawaharamura, C. Li and T. Hirao, Electrochem. Solid-State Lett., 2010, 13, H101.

[4] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge and C. D. Frisbie, Nat. Mater., 2008, 7, 900.

[5] S. A. Dibenedetto, A. Facchetti, M. A. Ratner and T. J. Marks, Adv. Mater., 2009, 21, 1407.

[6] M. J. Panzer and C. D. Frisbe, J. Am. Chem. Soc., 2007, 129, 6599.

[7] H. Han, D. Ghosh, J. L. Jones and J. C. Nino, J. Am. Ceram. Soc., 2012, 9, 1.

[8] Y. S. Yoon, W. N. Kang, S. S. Yom, T. W. Kim, M. Jung, H. J. Kim, T. H. Park and H. K. Na, Appl. Phys. Lett., 1993, 63, 1104.

[9] F. M. Pontes, E. J. H. Lee, E. R. Leite and E. Longo, J. Mater. Sci., 2000, 35, 4783.

[10] B. N. Pal, B. M. Dhar, K. C. See and H. E. Katz, Nat. Mater., 2009, 8, 898.

[11] K. H. Lee, M. S. Kang, S. Zhang, Y. Gu, T. P. Lodge and C. D. Frisbie, Adv. Mater., 2012, 24, 4457.

[12] H. Bong, W. H. Lee, D. Y. Lee, B. J. Kim, J. H. Cho and K. Cho, Appl. Phys. Lett., 2010, 96, 192115.

[13] J. Zhang, Y. Fu, C. Wang, P. Chen, Z. Liu, W. Wei, C. Wu, M. E. Thompson and C. Zhou, Nano Lett., 2011, 11, 4852.

[14] J. H. Park, Y. B. Yoo, K. H. Lee, W. S. Jang, J. Y. Oh, S. S. Chae and H. K. Baik, ACS Appl. Mater. Interfaces, 2013, 5, 410.

[15]G. Srinivasan, R. T. R. Kumar and J. Kumar, J. Sol-Gel Sci. Techn., **2007**, 43, 171-177.

[16]P. Bonasewicz, W. Hirschwald and G. Neumann, J. Electrochem. Soc., **1986**, 133, 2270-2278.

[17].J. R. Duclere, M. Novotny, A. Meaney, R. O'Haire, E. McGlynn, M. O. Henry and J. P. Mosnier, Superlattice Microst., **2005**, 38, 397-405.

[18] A. Baranauskas, D. Jasaitis and A. Kareiva, Vib. Spectrosc., **2002**, 28, 263.

[19] K. Nakamoto, Infrared and Raman Spectra of Inorganic and Coordination Compounds, John Willey & Sons, New York, 5th edn, 1997.

[20] L. Djoudi, M. Omari and N. Madoui, EPJ Web Conf., 2012, 29,16.

[21] J. Liu, D. B. Buchholz, J. W. Hennek, R. P. H. Chang, A. Facchett and T. J. Marks, J. Am. Chem. Soc., 2010, 132, 11934.

[22] L. Q. Zhu, J. Sun, G. D. Wu, H. L. Zhang and Q. Wan, Nanoscale, 2013, 5, 1980.

[23] A. Baranauskas, D. Jasaitis and A. Kareiva, Vib. Spectrosc.,

2002, 28, 263.
[24] K. Nakamoto, Infrared and Raman Spectra of Inorganic and Coordination Compounds, John Willey & Sons, New York, 5th edn, 1997.
[25] H. Han, D. Ghosh, J. L. Jones and J. C. Nino, J. Am. Ceram. Soc., 2012, 9, 1.

Chapter 6. Interface engineering for suppression of flat-band voltage shift in ZnO semiconductor /polymer dielectric thin film transistor

6.1 Introduction

To achieve a flexible thin film transistor (FTFT) using solution-processed ZnO, the dielectric layer is also considered for flexibility and good insulating properties.[1-2] Typical oxide dielectric materials have been evaluated as suitable in ZnO semiconductors; however, inorganic oxide dielectrics are fragile, which has to be thick to enhance insulating property.[3] In addition, metal oxide gate dielectrics require high temperature annealing above 400°C for the sol-gel process, which cannot be applied to plastic substrates.[4]

Unlike inorganic dielectrics, organic dielectrics are suitable for fabrication on plastic substrates because they have good ductility and low-temperature solution processability below 200 °C.[5] However, although many researchers have attempted to use high performance gate dielectrics, such as iongel and a polymer dielectric layer,[6-7] interface problems between the metal oxide semiconductor and the organic dielectric layer have hindered the stable and high performance of TFT fabrication.[8] Interface dipoles usually occur between inorganic and organic compounds, which induces hysteresis and reduces the effectiveness of charge inducement. Interface dipoles induce flat band shift by the interface trap between organic and inorganic materials.[9] In addition, to achieve flexible integrated electronic devices using solution-processed inorganic and polymer

materials, interface energy should be controlled using interface engineering by considering the wettability of each. Interface engineering for solution processed oxide TFTs is essential to suppress interface traps and apply in fabrication on any flexible materials that require a solution process. This issue is very important in all solution-processed ZnO-based TFTs fabricated with organic dielectric layer.

Hence, a self-assembled inorganic layer (SAIL) via the photo-induced transformation of a mono poly(dimethylsiloxane) (PDMS) layer is introduced to suppress the interface traps and flat band shift in low temperature, flexible and solution-processed metal oxide TFTs, including poly(4-vinylphenol) (PVP) dielectrics and solution-processed ZnO semiconductors. They exhibited good electrical performance and flexibility with on/off current ratios of more than 10^{-6} in TFTs with an annealing process as high as 200 °C. In addition, because of the good wetting ability of its high surface energy, the SAIL process is an appropriate interface to integrate various electronic precursor solutions without changing surface morphology.

6.2 Fabrication method for a self-assembled inorganic layer (SAIL)

The schematic of a flexible TFT structure including the SAIL process is illustrated in Figure 6.1a. For the formation of the polymer dielectric layer, 10 wt% PVP is dissolved overnight in propylene glycol monomethyl ether acetate (PGMEA) with melamine-co-formaldehyde as a cross-linker, and then spin-coated onto indium tin oxide-coated polyester (ITO-PET) substrate at 1000 rpm for 30 s. After annealing at 200 °C for 1 hour, highly cross-linked PVP (c-PVP) was formed at 629 nm thickness on the ITO-PET substrate (Figure 6.2). With regard to the interface engineering, the coating method of the ultra-thin PDMS layer was introduced in our previously report.[10] The reactive hydroxyl group was grafted on the surface of c-PVP through exposure to ultraviolet ozone (UVO, λ = 185 and 254 nm, 100 $mWcm^{-2}$) for 30 minutes. This was followed by immersion in a 0.5 wt% aqueous solution of 3-(amino propyl triethoxy silane)(APTES) for amino-silane grafting. The ultra-thin PDMS layer was formed by dropping monoglycidyl ether terminated poly(dimethylsiloxane) on the amino-silane grafted on c-PVP. The PDMS monolayer was then bound on amino-silane grafted on c-PVP layer by epoxy-amine reaction heated at 80 °C for 1 hour. For transformation from the PDMS monolayer to SAIL, the PDMS thin layer grafted on c-PVP was treated by UVO for 40 minutes. Next, the SAIL grafted on c-PVP composed with hydrophilic SiO_2 thin layer below 10nm was fabricated, as shown in Figure 6.1b.

Thus, although the prepared ZnO solution was a hydrophilic property, it was well spin-coated onto the SAIL grafted on c-PVP. Hence, hydrophilic inorganic semiconductor solution can be used in the solution-integrated process in the SAIL process regardless of any hydrophobic dielectric layers. The details of synthesis and process of flexible TFTs are described in the Experimental section. The high-resolution transmission electron micrograph (HR-TEM) images of solution-processed ZnO semiconductor on polymer dielectric layer are shown in Figure 6.1c-d. For measurement of HR-TEM, a thin poly (methyl methacrylate) (PMMA) layer was spin-coated on ZnO thin films to avoid penetration of platinum (Pt). The thickness of SAIL was measured at 8.59 nm, and the polycrystalline ZnO semiconductor was well formed at 5.21 nm [11] (Figure 6.3).

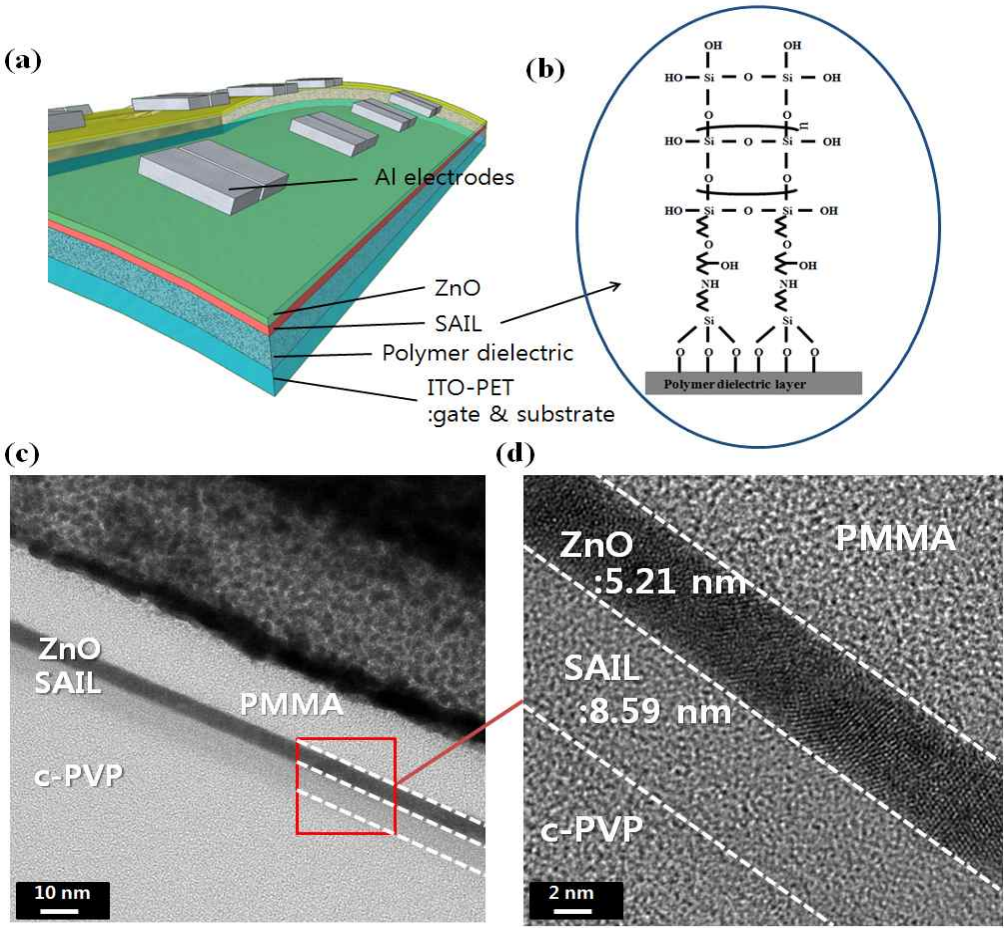


Figure 6.1. Schematic description and HR-TEM (High-resolution transmission electron micrograph) images of solution processed oxide semiconductor on polymer dielectric layer (a) The illustration of hybrid ZnO/PVP TFT structure (b) self-assembled inorganic layer (SAIL) on PVP dielectric layer (c) HR-TEM images of solution-processed zinc oxide semiconductor on polymer dielectric layer with SAIL (d) enlarged HR-TEM image of the stacked layers.

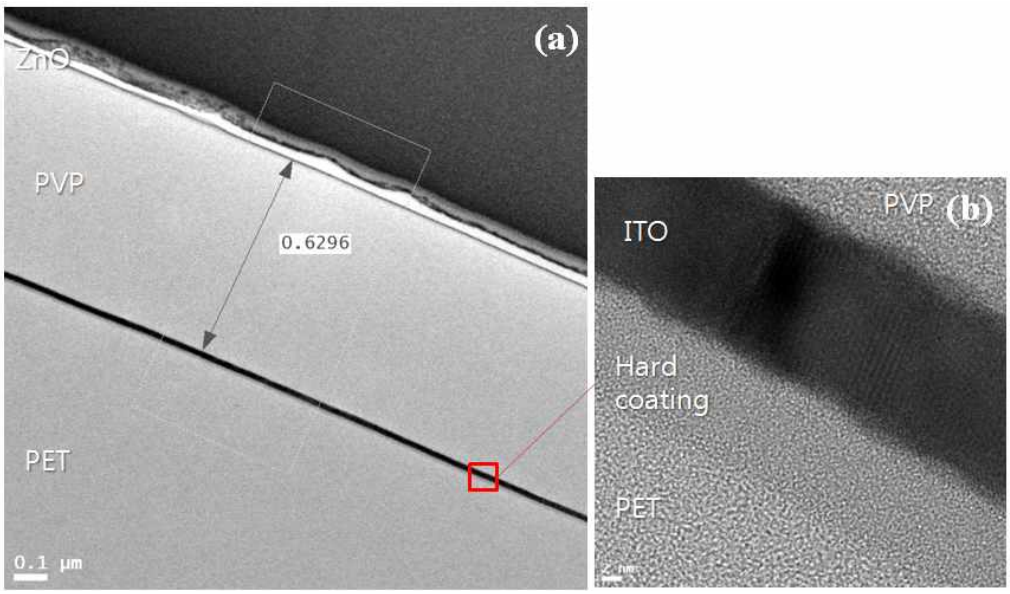


Figure 6.2. HR-TEM images of solution processed oxide semiconductor on polymer dielectric layer were shown. (a) The poly crystalline ZnO was well deposited on the highly cross linked PVP dielectric layer as 629nm. (b) The flexible gate & substrate was fabricated with 20 nm ITO on the hard coated polyester (PET) film.

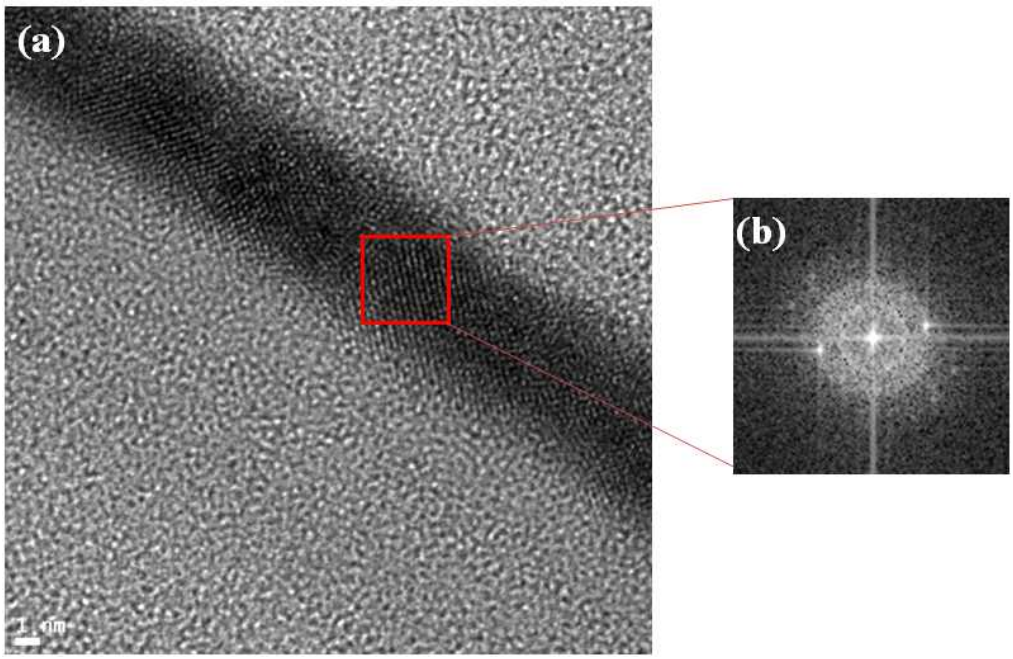


Figure 6.3. (a) Cross-sectional HR-TEM image of solution processed ZnO semiconductor on polymer dielectric layer were shown. (b) The ZnO shows crystalline FFT-SAED patterns.

6.3 The interface engineering effect with stable electrical performance by SAIL

To show the performance of the flexible TFTs, including SAIL, we prepared two samples: the first sample was irradiated by UVO for 40 minutes on natural c-PVP (Figure 6.4a); and the second sample was irradiated by UVO for 40 minutes on the PDMS thin layer grafted on c-PVP for SAIL (Figure 6.4d). The contact angle of SAIL grafted on c-PVP showed a higher surface energy than that of UVO-irradiated c-PVP. In a comparison of the ZnO spin coated samples onto SAIL grafted on c-PVP and the UVO irradiated c-PVP by atomic force microscopy (AFM), the ZnO layer showed island growth by insufficient interface energy in UVO irradiated c-PVP (Figure 6.4b). Otherwise, the formation of the ZnO layer on the SAIL grafted c-PVP was uniform, with no voids (Figure 6.4e). The root mean square (RMS) roughness of ZnO thin film on natural PVP was measured at 5.33 nm, and that of ZnO on SAIL grafted c-PVP was decreased to 2.92 nm (Figure 6.5). Although the ZnO/PVP TFT exhibited failure (Figure 6.4c), the ZnO/SAIL/PVP TFT showed good electrical performance. The ZnO/SAIL/PVP TFT transfer curve with drain current (V_D) of 40V informed the saturation field-effect mobility (μ_{sat}) of 0.05 cm^2/Vs, which were calculated with the capacitance of 20.5 nF/cm^2 at 100 kHz frequency (Figure 6.6), a threshold voltage of 0.2V, and an on/off current ratio (Ion/off) of more than 10^{-6} (Figure 6.4f). Because the solution-processed ZnO was compactly deposited on the SAIL/PVP, the field effect mobility of ZnO/SAIL/PVP TFTs was

as good as that of ZnO/PVP TFTs fabricated by high quality deposition, such as atomic layer deposition (ALD), which showed similar field-effect mobility, 0.075 $cm^2v^{-1}s^{-1}$, as the bottom-gate and top-contact ZnO/PVP TFTs on ITO-PET substrate.[12]

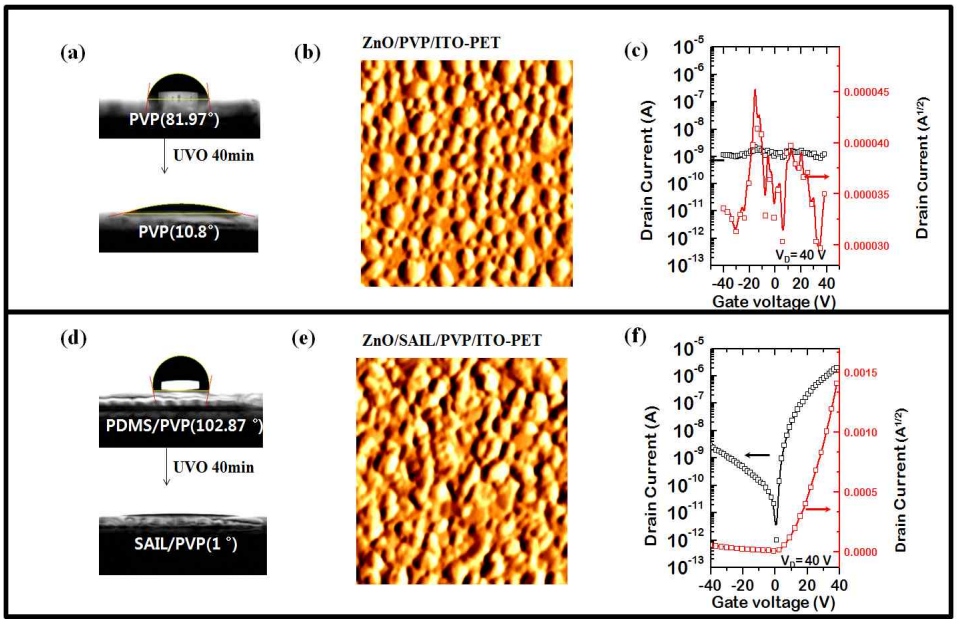


Figure 6.4. (a) Contact angle change after UVO exposure on natural PVP (b) AFM image of surface of spin-coated ZnO on PVP, which facilitated UVO exposure. (c) Transfer curve of the ZnO/PVP TFT without interface engineering (d) change in contact angle after UVO exposure on SAIL grafted PVP (e) AFM image of surface of spin-coated ZnO on SAIL grafted PVP, which facilitated UVO exposure (f) Transfer curve of the ZnO/SAIL/PVP TFT with interface engineering.

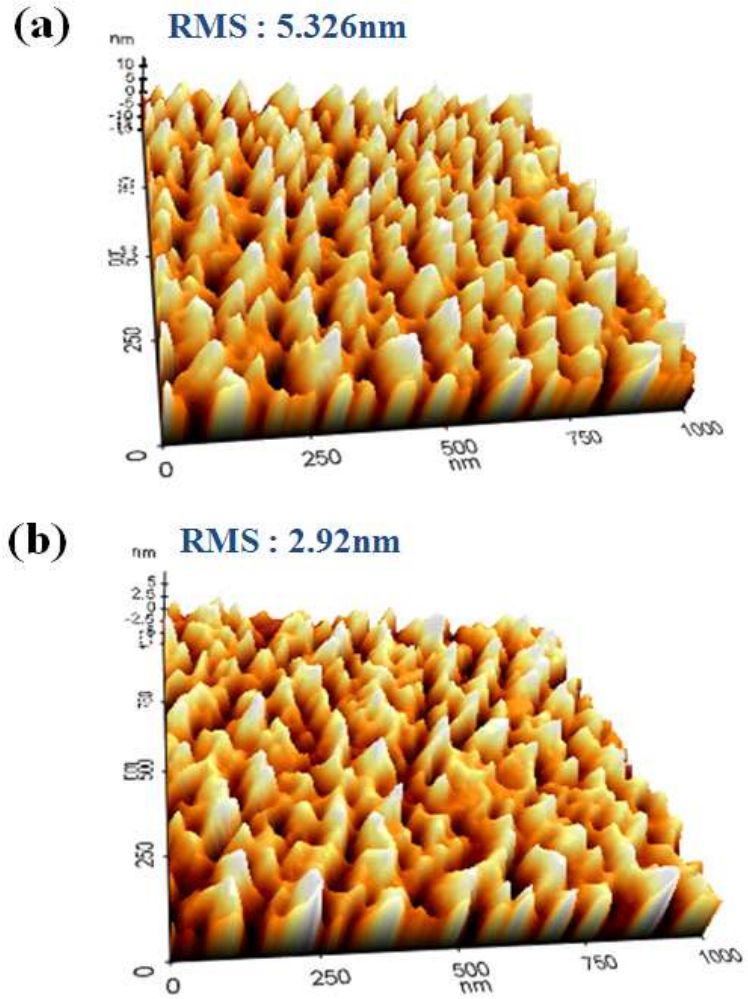


Figure 6.5. 3D views of AFM images: (a) 3D view of ZnO thin film on PVP without interface engineering (RMS=5.33 nm), (b) 3D view of intrinsic ZnO thin film on PVP with interface engineering (RMS= 2.92 nm)

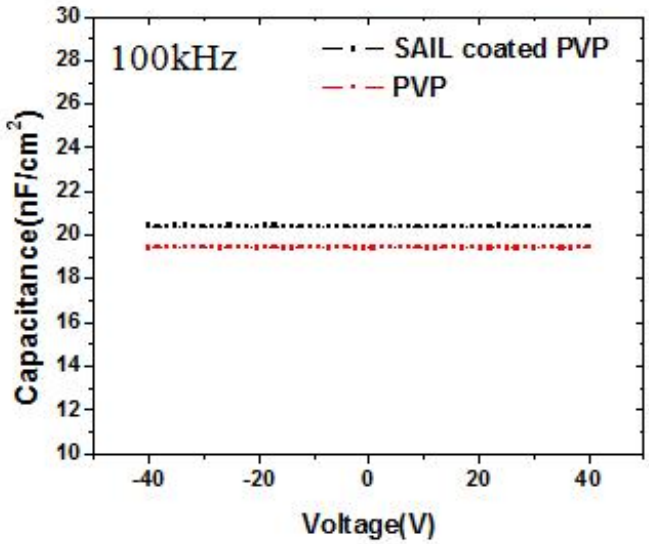


Figure 6.6. Voltage-dependent capacitance of both the SAIL coated PVP and the intrinsic PVP at 100 kHz.

The hysteresis and repeated transfer characteristics of ZnO/SAIL/PVP TFT are shown in Figure 6.7. The transfer tests were measured with drain current of 40V. Using interface engineering, the hysteresis-transfer curves of ZnO/SAIL/PVP TFT exhibited well in forward and reverse gate voltage sweep with scant hysteresis (Figure 6.7a). Moreover, the repeating transfer curves of the ZnO/SAIL/PVP TFT operated well 20 times without any threshold voltage shift (Figure 6.7b). In the poor interface between the polymer dielectric and metal oxide semiconductor, the polymer dielectrics degraded the electrical performance of metal oxide TFTs because of their low capacitance. The field-effect mobility induced by the low capacitance of the polymer dielectric can be increased using advanced hybrid dielectric materials, such as double dielectric layer with TiO_2-polymer composite(TPC)[13] and PVP. In this study, we adopted the TiO_2-polymer composite (TPC) and PVP double layer as dielectric material used in flexible ZnO TFTs. The details of the synthesis of TPC and PVP are introduced in the Experimental section.

The TPC precursor solution was spin-coated at 2000 rpm on the ITO-PET, which was measured at 135 nm by SEM (Figure 6.8b). After heating at 200 °C for 1 hour, the 10-wt% PVP solution was spin-coated at 2000 rpm on the TPC/ITO-PET. The integrated thickness of TPC and PVP was measured at 615 nm (Figure 6.8c). Then, the SAIL process was treated on the highly cross linked PVP

as an interface engineering. The aqueous amine ZnO precursor solution was spin coated on SAIL grafted c-PVP/TPC. After heating at 200 °C for 1 hour, Aluminium (Al) source and drain electrodes were deposited by thermal evaporation with width (W)/ length (L) ratio of 20. The output curves of the ZnO/SAIL/PVP/TPC TFT showed a good electrical saturation behavior from 0 to 60 V in steps of 12 gate voltage (V_G) with maximum drain current of 0.027 mA at V_G = 60 V in Figure 6.9a. Also, the TFT has enhanced field-effect mobility with 0.28 $cm^2v^{-1}s^{-1}$ with an on/off current ratio of more than 10^{-6} in Figure 6.9b. The enhanced electrical performance means that the capacitance performance of the dielectric layer greatly affected the electrical performance of TFTs, which shows good potential as a double dielectric layer, including high K dielectrics. The electrical characteristics of ZnO/SAIL/PVP and ZnO SAIL/PVP/TPC flexible TFTs are summarized in Table 6.1.

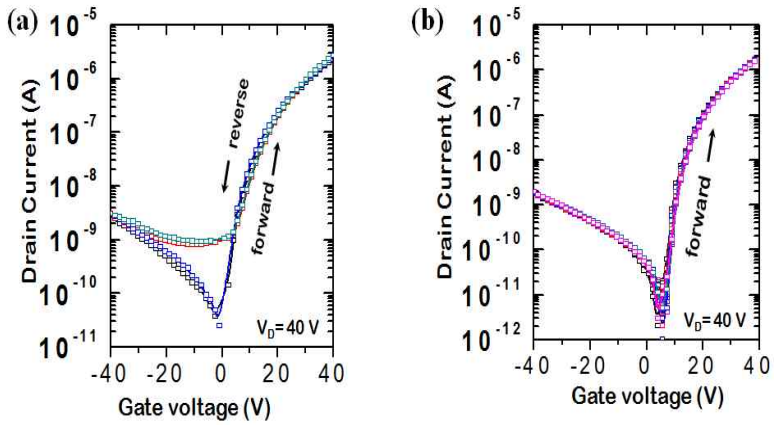


Figure 6.7. Hysteresis and repeated transfer characteristics of SAIL grafted ZnO/PVP TFT with W/L ratio of 20 (g) Hysteresis-transfer curves of SAIL grafted ZnO/PVP TFT after sintering at 200 °C (h) Repeating transfer curves of SAIL grafted ZnO/PVP TFT 20 times after sintering at 200 °C.

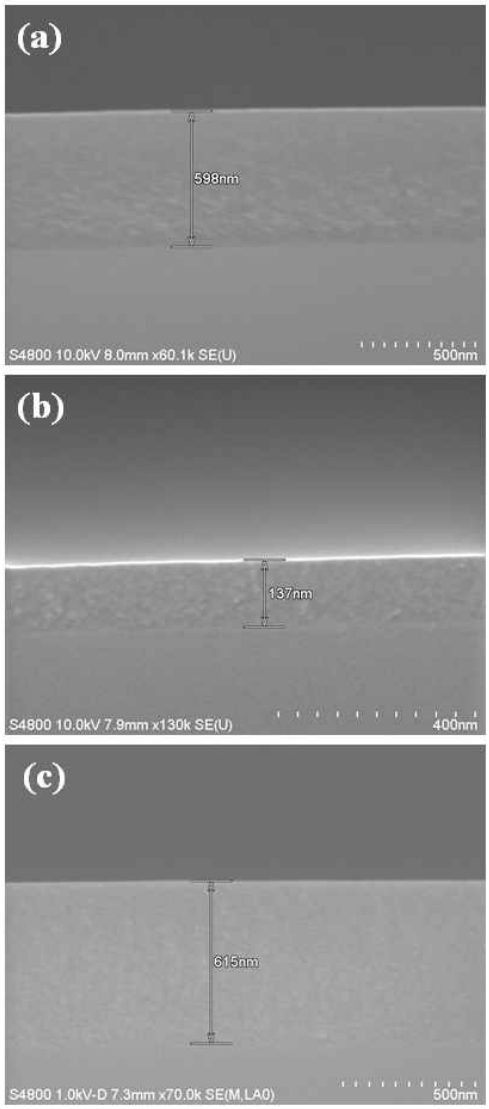


Figure 6.8. Cross-sectional SEM images of polymer dielectric layers were shown. (a) The spin coated PVP has 598 nm at 2000 rpm. (b) The spin coated TPC has 137 nm at 2000 rpm. (c) The spin coated double dielectric layer has 615 nm that TPC was spin coated at 2000 rpm on the spin coated PVP at 2000 rpm.

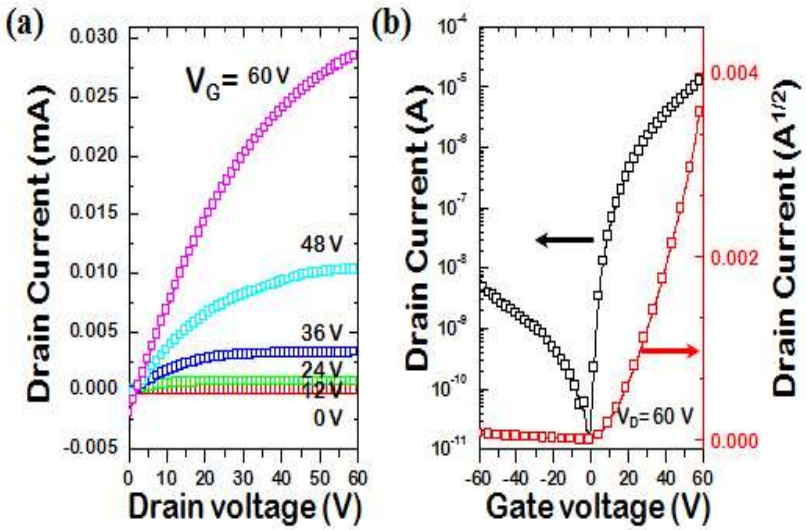


Figure 6.9. Typical electrical characteristics of 200℃ annealed ZnO/200℃ annealed PVP and TPC TFTs with W/L ratio of 20 (a) Output curve with 12V steps of gate voltage from 0V to 60V. (b) Transfer curve with drain current of 60V.

Table 6.1. Summarized electrical properties of 200 °C annealed ZnO/SAIL/polymer dielectrics TFT.

Sintering Temp.(°C)	Material	$\mu(cm^2v^{-1}s^{-1})$	$V_{on}(V)$	I_{on}/I_{off}
200	ZnO/SAIL/PVP	0.05	0.87	~10^6
200	ZnO/SAIL/PVP+TPC	0.28	-1.14	~10^6

6.4 Analytic model for suppression of flat band shift

To investigate how SAIL affected the electrical properties of the TFTs, we analyzed the hysteresis of the transfer characteristics using an analytic model specific to nanocrystalline ZnO-based TFTs.[14] The model assumes that the charge carrier transport in the channel of the device is limited by the localized-carrier trapping states below the conduction band edges of the ZnO.[15] As the localized states we only consider the tail trap states, and a single exponential density of states is applied for the tail trap states.[15] The mathematical details and physical manipulations are well explained and described in a previously reported analytic model.[14] The drain current (I_D) for the ZnO-based TFTs can be given by

$$I_D = \frac{W}{L}\beta\left[\left(V_G - V_{FB} - \varphi_{sS}\right)^{\gamma} + \frac{v_{th}\gamma^2}{(\gamma-1)}\left(V_G - V_{FB} - \varphi_{sS}\right)^{\gamma-1}\right]$$
$$-\frac{W}{L}\beta\left[\left(V_G - V_{FB} - \varphi_{sD}\right)^{\gamma} + \frac{v_{th}\gamma^2}{(\gamma-1)}\left(V_G - V_{FB} - \varphi_{sD}\right)^{\gamma-1}\right] \qquad (1)$$

where,

$$\varphi_{sS} = V_G - V_{FB} - v_{th}\gamma W_0\left[\frac{\eta}{v_{th}\gamma}\exp\left(\frac{V_G - V_{FB} - V_S}{v_{th}\gamma}\right)\right] ,$$

$$\varphi_{sD} = V_G - V_{FB} - v_{th}\gamma W_0\left[\frac{\eta}{v_{th}\gamma}\exp\left(\frac{V_G - V_{FB} - V_D}{v_{th}\gamma}\right)\right] ,$$

$$\beta = \sigma_0 \frac{\varepsilon_0 \varepsilon_s}{C_i} v_{th} \left(\frac{1}{\gamma - 1} \right) \left[\frac{C_i^2 \sin(2\pi / \gamma)}{2\pi N_t q \varepsilon_s v_{th}} \right] \quad ,$$

$$\eta = \frac{\sqrt{q \varepsilon_0 \varepsilon_s n_0 v_{th} \gamma}}{C_i} \quad ,$$

$$v_{th} = \frac{k_B T}{q} \quad ,$$

$$\gamma = \frac{2T_0}{T}$$

q is the electron charge, kB is the Boltzmann constant, ε_0 is the electrical permittivity in vacuum, and W_0 represents the principal branch of the Lambert Function. The descriptions of the other variables are depicted in Table 6.2. The values of parameters used for the analytic model are chosen to represent a typical ZnO-based TFT.[14] The measured transfer characteristics of the devices were fitted with varying 'fitting parameters' depicted in Table 6.2 using equation (1) via the interior point method.

With regard to the hysteresis curves, "forward sweep" refers to the gate voltage swept from a negative to positive bias; "backward sweep" refers to the opposite. As shown in Figure 6.10a, the I_D-V_G curve of the ZnO/SAIL/PVP TFT for the forward sweep was well matched by the analytic model with the flat-band voltage (V_{FB}) of 0.009 V, which insensitively varied in the case of the backward sweep (V_{FB} = 0.499), while other device parameter remained stable (Table 6.3). The negligible shift of V_{FB} may suggest that the accumulated electrons in the channel for the region of 0 V < V_G <

30 V cannot change the electronic structure of the device at the equilibrium condition (meaning V_G = 0 V).

In order to verify the effect of SAIL, we fabricated ZnO/PVP TFTs as reference devices and compared their electrical performances. Because ZnO film is incompletely deposited onto the pristine PVP surface using conventional spin-coating methods, as shown in Figure 6.4b-c, I used the poly (methyl methacrylate) (PMMA) pre-pattern[16] to fabricate the ZnO layer on the PVP surface (see the Chapter 3.2). The hysteresis of the control ZnO/PVP TFT device was in remarked contrast to that of the ZnO/SAIL/PVP TFT. Furthermore, the fitted V_{FB} of the control TFT device largely shifted from -2.798 V (forward sweep) to 6.014 V (backward sweep), as shown in Figure 6.10b. The electronic structure at the equilibrium condition for the control ZnO/PVP TFTs was significantly changed under the device operation range (0 V < V_G < 30 V). These results indicated that SAIL could efficiently block the penetration of the accumulated electrons in the channel into the PVP layer, resulting in highly attenuated hysteresis of the transfer characteristics of the ZnO/SAIL/PVP device.

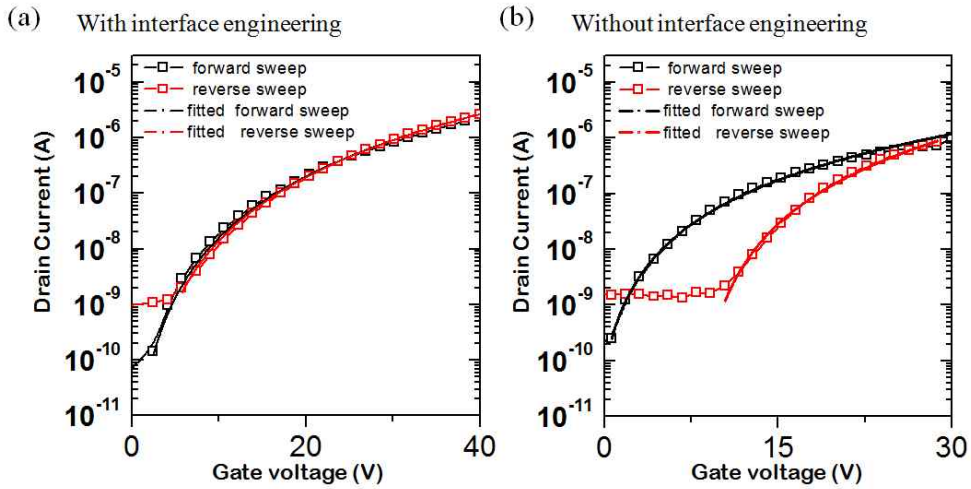


Figure 6.10. The transfer curves were fit with simulation using the explicit analytic model for nanocrystalline ZnO TFTs. (a) The measured hysteresis test of SAIL grafted ZnO/polymer TFT was compared with simulation of SAIL grafted TFT. (b) The measured hysteresis test of ZnO/polymer TFT without interface engineering was compared with the simulation of ZnO/polymer TFT.

Table 6.2. Definition of variables used for the analytic model.

Variables	Definition	Values	Units
W	Width of the channel	1000	μm
L	Length of the channel	50	μm
V_G	Gate bias voltage	-	
V_D	Voltage at the drain electrode	30	V
V_S	Voltage at the source electrode	0	V
C_i	Capacitance of the gate-insulator per unit area	9.00	nF cm^{-2}
ε_s	Relative electrical permittivity in ZnO	7.5	-
n_0	Charge-carrier number of ZnO per unit volume	10^{19}	cm^{-3}
T	Temperature of the device	298	K
V_{FB}	Flat-band voltage	Fitting parameter	V
T_0	Trap characteristic temperature	Fitting parameter	K
N_t	Total number of trap state per unit volume at T	Fitting parameter	cm^{-3}
σ_0	Conductivity of ZnO at infinite temperature	Fitting parameter	S cm^{-1}

Table 6.3. Values of fitting parameters used for Figure 6.10.

	ZnO/SAIL/PVP TFT		ZnO/PVP TFT		Units
	Forward	Backward	Forward	Backward	
V_{FB}	0.009	0.499	-2.742	6.014	V
T_0	553	553	550	552	K
N_t	$2.95*10^{19}$	$2.94*10^{19}$	$2.53*10^{19}$	$2.10*10^{19}$	cm^{-3}
σ_0	2.23	2.35	2.25	2.99	S cm^{-1}

6.5 Flexible bending test of ZnO/SAIL/PVP TFTs

The designed flexible ZnO/SAIL/PVP TFT can enhance the properties of aperture ratio, high impact resistance, low weight over the conventional panel display. Also, it can be produced more cheaply with unbreakable characteristic to produce an electronic device with a cheapest plastic substrate, such as PET. Thus, the ZnO/SAIL/PVP TFT was fabricated on ITO-PET below 200 °C to avoid thermal degradation. To show the flexibility, we also measured the changes in on - off current, field effect mobility, and threshold voltage of flexible ZnO/SAIL/PVP TFTs during compressive and tensile bending (Figure 6.11). When the flexible TFT, ZnO/SAIL/PVP TFT, was in compressive bending, the ZnO semiconductor layer did not crack in the bending radius range from 20 mm to 10 mm, which was proved by the maintenance of the on-current, field-effect mobility, and threshold voltage (Figure 6.11a-c). Although the off-current is slightly increased than before bending, on-current maintained well on compressive and tensile bending. Otherwise, in tensile bending, mobility and on current decreased sharply at a 10 mm bending radius of the tensile state, which means that the tensile stress was greater than compressive stress in ZnO/SAIL/PVP TFT. However, in overall changes, this flexible TFT was the most reliably available device, without any failures in bending up to a 10-mm bending radius. A small amount of electrical degradation was caused by ITO crack at the bottom gate without delamination and exfoliation of the dielectric layers (Figure 6.12). These electrical characteristics of the flexible

TFT were achieved in the all-solution process, except for the Al electrode deposition. The ZnO/SAIL/PVP TFT was successfully operated as a flexible device without any shift in V_{FB} or formation of interface dipole.

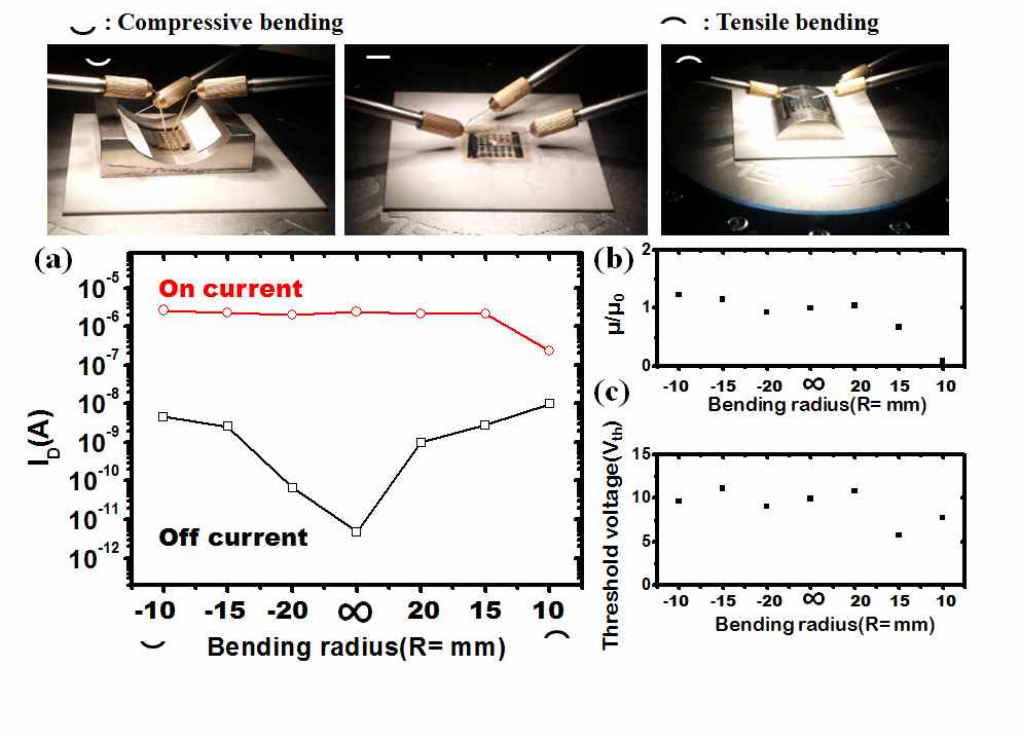


Figure 6.11. The changes in on - off current (a), field effect mobility (b), and threshold voltage (c) were measured as flexible devices during compressive and tensile bending. The bending radius was determined from flat condition to 20~10 mm compressive and tensile bending by the bend support plates.

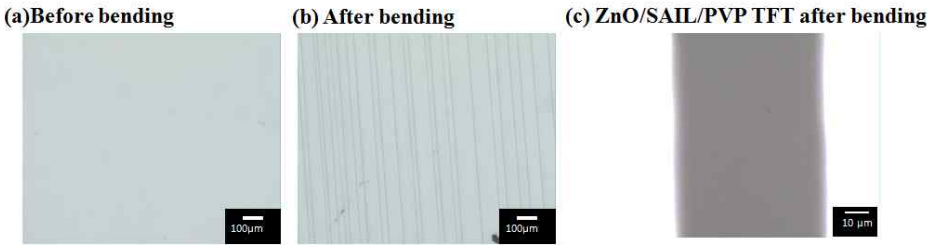


Figure 6.12. Optical spectroscopy images: (a) the ITO PET before bending; (b) the ITO PET after bending. (C) The ZnO/SAIL/PVP TFT was shown reliable flexibility without any delamination after bending.

6.6 References

[1] J. Liu, D. B. Buchholz, R. P. H. Chang, A. Facchetti and T. J. Marks, Adv. Mater. **2010**, 22, 2333.

[2] T. Sekitani, U. Zschieschang, H. Klauk and T. Someya, Nat. Mater. **2010**, 9, 1015.

[3] S. H. Chae, W. J. Yu, J. J. Bae, D. L. Duong, D. Parello, H. Y. Jeong, Q. H. Ta, T. H. Ly, Q. A. Lu, M. Yun, X. Duan and Y. H. Lee, Nat. Mater. **2013**, 12, 403.

[4] V. ZardettoT. M. BrownA. RealeA. Di CarloJ.Polym.Sci. Part B:Polym. Phys. **2011**, 49638.

[5] I.G. Hill, A. Rajagopal and A. Kahn, Appl. Phys. Lett. **1998**, 73, 662.

[6] H. Bong, W. H. Lee, D. Y. Lee, B. J. Kim, J. H. Cho and K. Cho, Appl. Phys. Lett. **2010**, 96, 192115.

[7] K. Lee, J. Kim, S. Im, C. Kim, H. Baik, Appl. Phys. Lett. **2006**, 89, 133507

[8] K. Lee, G, Ko, G. H. Lee, G. B. Han, M. M. Sung, Appl. Phys. Lett. **2010**, 97, 082110.

[9] N. Koch, ChemPhysChem, **2007**, 8, 1438.

[10] M. J. Lee, N. Y. Lee, J. R. Lim, J. B. Kim, M. Kim, H. K. Baik and Y. S. Kim, Adv. Mater. **2006**, 18, 3115.

[11] S. Y. Park, K. Kim, K.-H. Lee, B. J. Kim, E. Lee, J. H. Cho and Y. S. Kim, J. Mater. Chem. C, **2013**, 1, 1383.

[12] J. W. Yang, G. W. Huung, H. W. Lee, J. Park, J. R. Koo, H. S. Jung, E. S. Cho, S. J. Kwon and Y. K. Kim, Mol. Cryst. Liq. Cryst.

2011, 550, 205.

[13] J. Kim, S. H. Lim, and Y. S. Kim, J. Am. Chem. Soc. **2010**, 132, 42, 14721.

[14] F. J. Garcia-Sanchez, and A. Ortiz-Conde, IEEE Trans. Electron Devices, **2012**, 59, 46-50.

[15] P. Servati, A. Nathan, and G. A. Amaratunga, Phys. Rev. B, **2006**, 74, 245210.

[16] K. Kim, S. Park, J. B. Seon, K. H. Lim, K. Char, K. Shin and Y. S. Kim, Adv. Funct. Mater. **2011**, 21, 3546.

Chapter 7. Patterning by surface engineering

7.1 Introduction

To promote strongly the potential of ZnO-based TTFTs with solution processability, a low-temperature and fast drying process are essential to achieve printed electronics on the large substrate. Although some remarkable reports have been introduced,[1-2] they have an intrinsic problem in that they use a metal oxide precursor with a carbonyl ligand group. The carbonyl ligand groups are completely decomposed at temperatures close to 310 °C, and this hinders the low-temperature process of the metal oxide semiconductor.[3] Although the temperature of the ZnO semiconductor process is too high to be applied directly to a flexible device on a plastic substrate, ZnO is regarded as the most promising active channel material for the future development of TTFTs.[4]

In TFTs, the semiconductor patterning process is essential to prevent current leakage and cross-talk noise in devices. As the solution-processed ZnO films have a porous structure and given that ZnO reacts easily with both acidic and alkaline solvents as an amphoteric oxide,[5] there are substantial difficulties when it comes to applying these ZnO films in conventional lithography processes, such as wet developing and stripping in photolithography.[6-7] In addition, plasma etching for pattern development damages ZnO films due to the excessive oxygen vacancies induced by the plasma treatment.[8-9] As the alternatives, non-conventional lithography methods such as inkjet printing are feasible for fabricating patterned ZnO films.

However, while inkjet printing shows good performance in the patterning process, there are some issues that remain to be solved, such as the bank structures for fine patterns[10] and the complicated care during the drying process for neat and uniform patterns. Moreover, inkjet printing with ZnO precursor solutions easily induces wavy, porous and non-uniform patterns in the drying step. Recently, several successful results have been introduced for the patterning with ZnO ink.[11,12] However, they still required cumbersome processes such as a hot substrate and sequential post-annealing. Also, on low-temperature sintering under ~300 °C, these previously reported results showed very low field effect mobility in a TFT.[11]

Hence, we introduced a new direct developing method known as drop-casting for use with both intrinsic and Na doped ZnO precursor solutions. In this study, through a combination of an aqueous ammonia-ZnO process with the doping of Na ions for high n-type semiconducting performance and residual ammonia extraction in ZnO films using methanol which was combined with the direct patterning method of drop-casting with surface engineering via the photoinduced transformation of poly(dimethylsiloxane) (PDMS), we fabricated the patterned intrinsic and Na doped ZnO TTFTs with high performance and good stability after sintering process at a maximum process temperature as low as 300 °C. Moreover, this patterning process didn't require any cumbersome steps such as a vacuum process, inert gas conditions, and a high-temperature annealing process.

7.2 Low-temperature process through ligand extraction by methanol

For a low-temperature and fast drying process, we introduced a simple developing method to remove the residual ligands of the ZnO precursor using methanol. In general, as the carbon functional groups in a precursor require a relatively high-temperature sintering process for the removal of carbonyl groups, we introduced an ammonia-aqueous ZnO precursor for a low-temperature process. Also, in order to prevent wavy and matted patterns, we used methanol in the developing process. The mechanism of the conversion from the ammonia-aqueous ZnO precursor solution to ZnO semiconductor films was demonstrated in Figure 7.1. First, the ZnO powder was easily dissolved in aqueous ammonia, which generated zinc ammonia complexes ($Zn(NH_3)_4^{2+}$) and hydroxide ion (OH^-)(Figure 7.1a).[13] For the easy decomposition of zinc ammonia complexes ($Zn(NH_3)_4^{2+}$), the excess methanol was added and then ($Zn(NH_3)_4^{2+}$) transformed Zn^{2+} and NH^{4+} ions via the decrease in the pH (Figure 7.1b).[14] In the low-pH state, zinc hydroxide ($Zn(OH)_2$) is generated from the reaction between Zn^{2+} and OH^-. The $Zn(OH)_2$ does not dissolve in methanol; otherwise, ammonia can dissolve in methanol and can be effectively extracted from the $Zn(OH)_2$ film patterns (Figure 7.1c). $Zn(OH)_2$ was easily decomposed at about 100 °C and become ZnO(Scheme 1d). Also, the small amount of residual ammonia or methanol in the ZnO films was easily removed by evaporation in annealing on a hot plate.

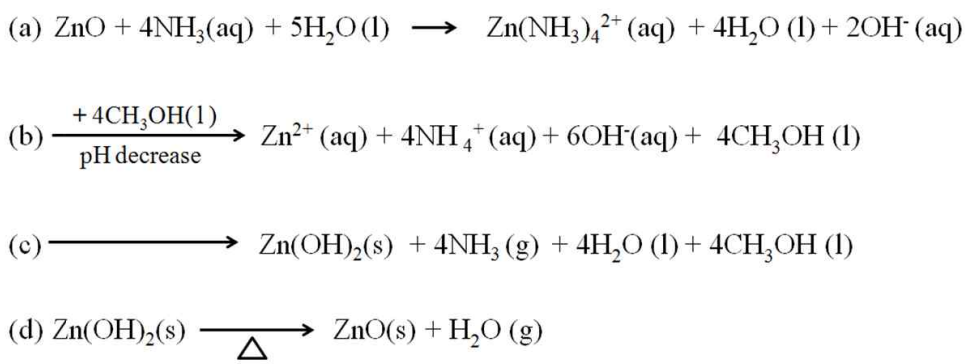


Figure 7.1. Schematic description of the solvent reaction between methanol and the ammonia-ZnO precursor solution: (a) aqueous zinc ammonia complexes form by resolving in ammonia water, (b) changes of the ZnO precursor solution after the decrease in the pH via methanol, (c) $Zn(OH)_2$ formation by a continual pH decrease and methanol absorption of the residuals of ammonia and water, (d) ZnO formation by the thermal decomposition of $Zn(OH)_2$.

7.3 Patterning: surface engineering using selective photoinduced transformation

For the patterning of transparent semiconductor thin film with a ZnO precursor solution, an unconventional patterning method is required due to unique properties of the ZnO films. As ZnO film made using a precursor solution has a porous structure and easily reacts to both acidic and alkaline solvents, the electrical performance becomes degraded when wet etching and developing the film during photolithography. In addition, when an ammonia-aqueous ZnO precursor solution dried in air, ammonium carbamate was formed on the surface of the ammonia-based solution in seconds due to the reaction with carbon dioxide in air, which induced defects in the ZnO films [15] (Figure 7.2a-c). When ZnO precursor solutions were sintered directly on a hot plate under ambient conditions, irregular aggregations of ZnO came about due to instances of momentary solidification (Figure 7.2d-f). When developing with water, Zn ions dissolved in the water and disrupted the formation of dense films of ZnO (Figure 7.2g-i). Otherwise, when using a methanol dipping and developing method, the methanol prevents ZnO film patterns from irregular aggregation as a proper developing solvent.[16]As the methanol hindered the formation of ammonium carbamate and effectively extracts the ammonia ligand from the ZnO precursor, it induced the dense and neat films of ZnO.

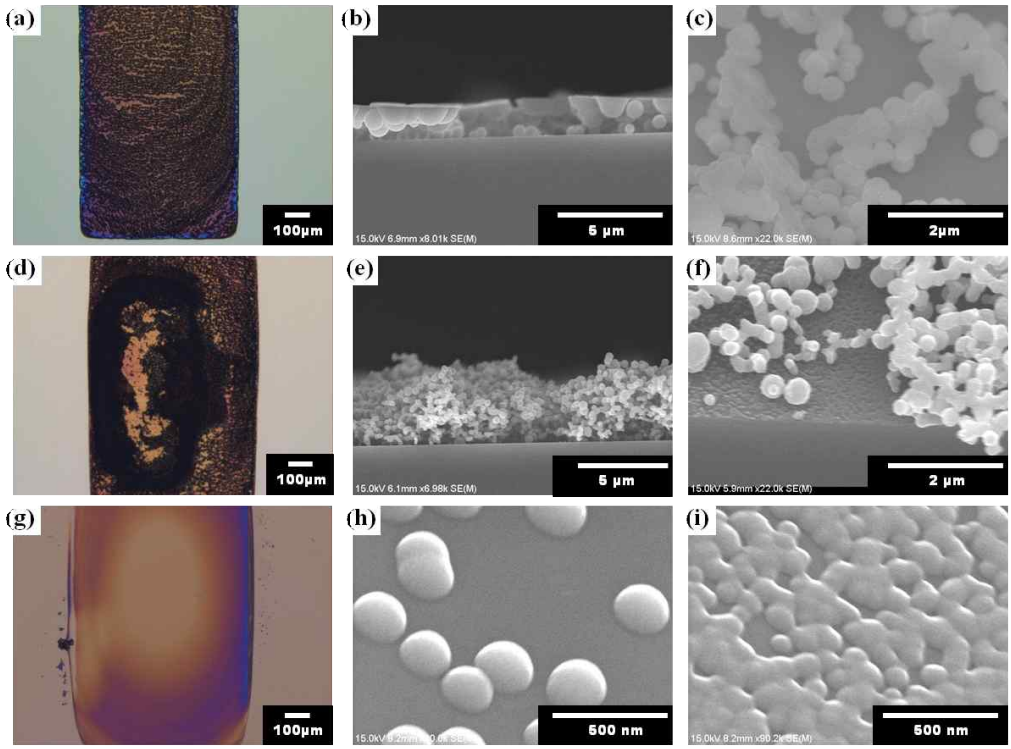


Figure 7.2. Optical microscopy images were magnified by a factor of 40. Cross-section and tilted(Θ = 45°) FE-SEM microscopy images of patterned ZnO on a SiO_2 substrate. a - c) Drying of the solution in the air without methanol. d-f) Direct sintering of the solution in the air without methanol. g-i) developing of the solution with de-ionized water.

Using the above mechanisms, we developed a simple patterning method, termed drop-casting, through selective control of the surface. For patterning through the drop and casting method, we coated a thin PDMS layer onto a substrate and generated selective hydrophilic patterns by means of a UV ozone treatment through a shadow mask. The mechanism of the PDMS coating and selective photoinduced transformation technique was demonstrated in Figure 7.3. The coating method of the PDMS thin layer was introduced in our previously report.[17] To create selective hydrophilic regions through UVO treatment, a clean silicon dioxide (SiO_2) should be coated with mono glycidyl ether - terminated poly-dimethyl siloxane (PDMS) to cover the entire substrate with a hydrophobic self-assembled monolayer (Figure 7.3a). The details of the PDMS monolayer coating were demonstrated in the experimental. To make the selective hydrophilic and hydrophobic surface properties onto a substrate, it was irradiated with UVO (λ = 185 and 254 nm, 100 mW/cm^2) through a shadow mask for 40 minutes to obtain selective hydrophilic regions(Figure 7.3b). The reactive hydroxyl functional group broke the side-carbon bonding of PDMS and then hydrophilic SiO_2 on the surface of the substrate was generated by decomposition.

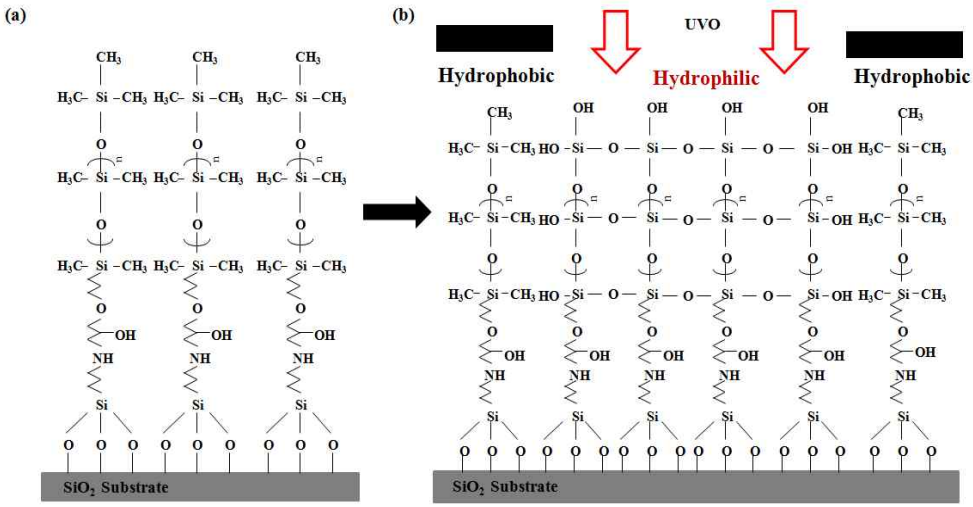


Figure 7.3. Schematic description of a PDMS layer coated onto the surface of the substrate: (a) PDMS coated onto a SiO_2 substrate,(b) UVO exposure through a shadow mask to generate selective hydrophilic regions.

The overall fabrication steps of the TTFT device are illustrated schematically in Figure 7.4. The prepared substrate, PDMS monolayer - coated SiO_2(Figure 7.4a), was selectively exposed to UVO through a shadow mask (Figure 7.4b). Through a photo-induced transformation technique, a hydrophilic region was selectively generated onto hydrophobic regions (Figure 7.4c). As noted above, this could easily be filled selectively with an ammonia-aqueous ZnO precursor solution by means of drop and casting (Figure 7.4d-e). Each hydrophilic region, with an area of 550 μm x 1200 μm, was then filled with the ammonia-aqueous ZnO precursor solution (see the Figure 7.5a). The substrate, selectively filled with the ZnO precursor, was then dipped in methanol under sonication (Figure 7.4f). The methanol effectively blocked the sudden precipitation that caused by the decrease in the pH through the abrupt evaporation of ammonia. Also, it suppressed the side reaction between the ambient carbon dioxide gas and the ammonia hydroxide (NH_4OH) in the solution while also effectively extracting the ligands of the ZnO precursor. As a result, neat and uniform ZnO film patterns were easily obtained. Images of the uniform patterns of the ZnO thin film captured with both a camera and an optical microscope were shown in Figure 7.5b-c; the patterned ZnO semiconductors were fabricated without any matted ZnO particles or wavy patterns. To show the fidelity of the patterned ZnO thin films in our method, various images of the patterned ZnO thin films by optical microscopy were shown in Figure 7.6. Cross-sectional and tilted field-emission scanning electron

microscopy (FE-SEM) images of the ZnO film patterns also showed the good performance of this process. The thickness was monitored and was found to range from 105 to 120 nm (Figure 7.5d - e). Also, the morphology of patterned intrinsic ZnO film and Na doped ZnO film were analyzed using atomic force microscopy (AFM) (Figure 7.7). Figure 7.7a-d showed two-dimensional and three-dimensional AFM images of the micro-patterned intrinsic ZnO and Na doped ZnO thin film. The scanning area was 2 × 2 μm^2 as well. The root mean square(RMS) roughness of Na doped ZnO thin film was measured as 1.121 nm and decreased by 0.14 nm in comparison with that of intrinsic ZnO thin film (Figure 7.7). I think that this variation was in the range of experimental error.

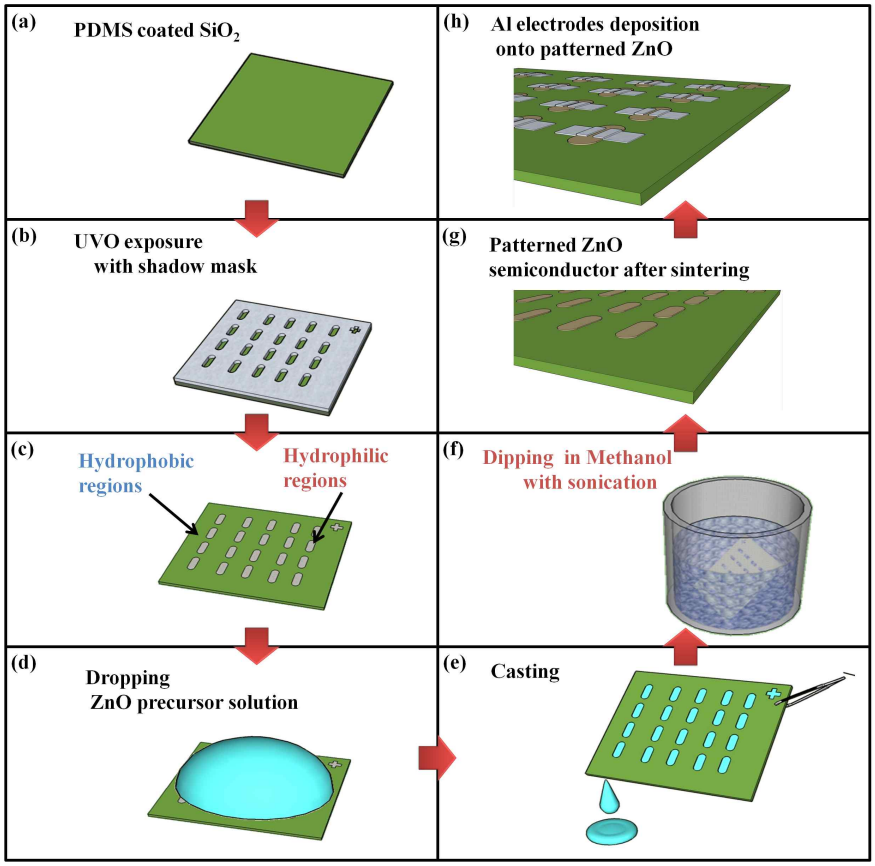


Figure 7.4. Schematic description of the overall fabrication process: (a) PDMS thin layer coated onto a SiO_2 substrate, (b) selective photo induced transformation of the PDMS layer through a shadow mask by UVO exposure,(c) selective hydrophilic regions onto hydrophobic regions,(d) dropping of the ZnO precursor solution onto the substrate, (e) casting of the ZnO precursor solution from the substrate,(f) dipping in methanol with sonication, (g) uniformly patterned ZnO semiconductors on the SiO_2 substrate,(h) fabrication of a thin film transistor with bottom gate and top contact.

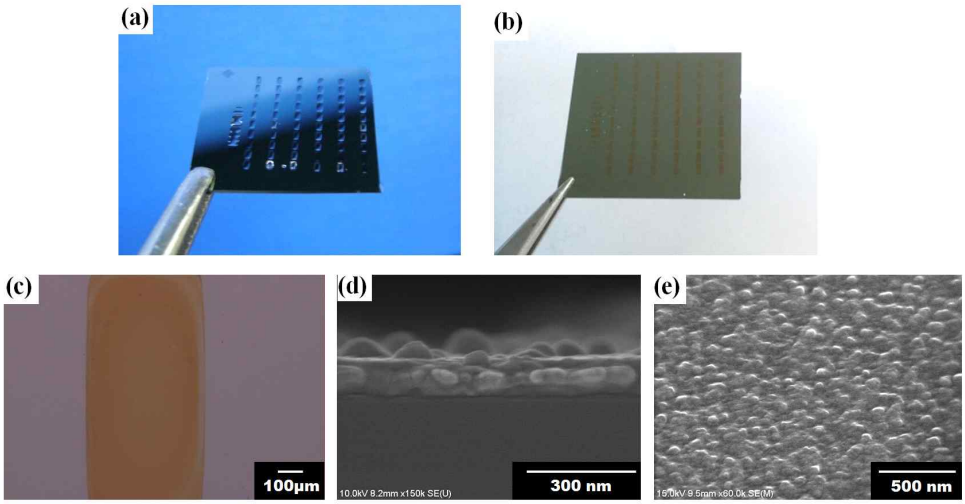


Figure 7.5. (a) Images of selective hydrophilic regions on the substrate, (b) an image of patterned ZnO semiconductors on the substrate, (c) optical microscopy images magnified by a factor of 40, (d) a cross-section image of patterned ZnO films imaged by a field emission scanning electron microscope (FE-SEM) on a SiO_2 substrate, (e) a tilted (Θ = 45°) FE-SEM image of the upper surface as observed to probe the macroscopic crystalline formation.

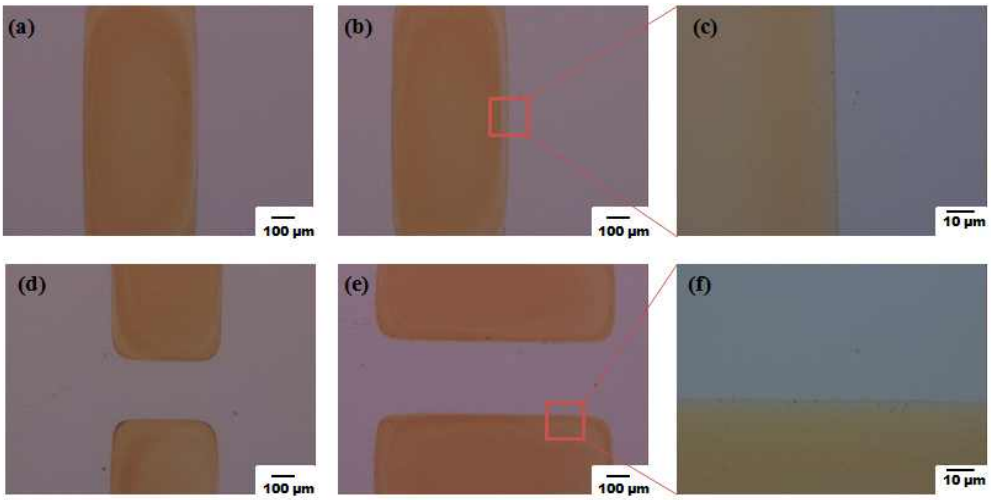


Figure 7.6. The optical microscopy(OM) images of various ZnO thin films, which fabricated by one run; (a) and (b) OM images of patterned ZnO thin films magnified by a factor of 40; (c) Enlarged OM image of side part of the patterned ZnO thin film magnified by a factor of 500; (d) and (e) OM images to show the part of the gap between patterned ZnO thin films magnified by a factor of 40; (f) Enlarged OM image of side part of the patterned ZnO thin film magnified by a factor of 500.

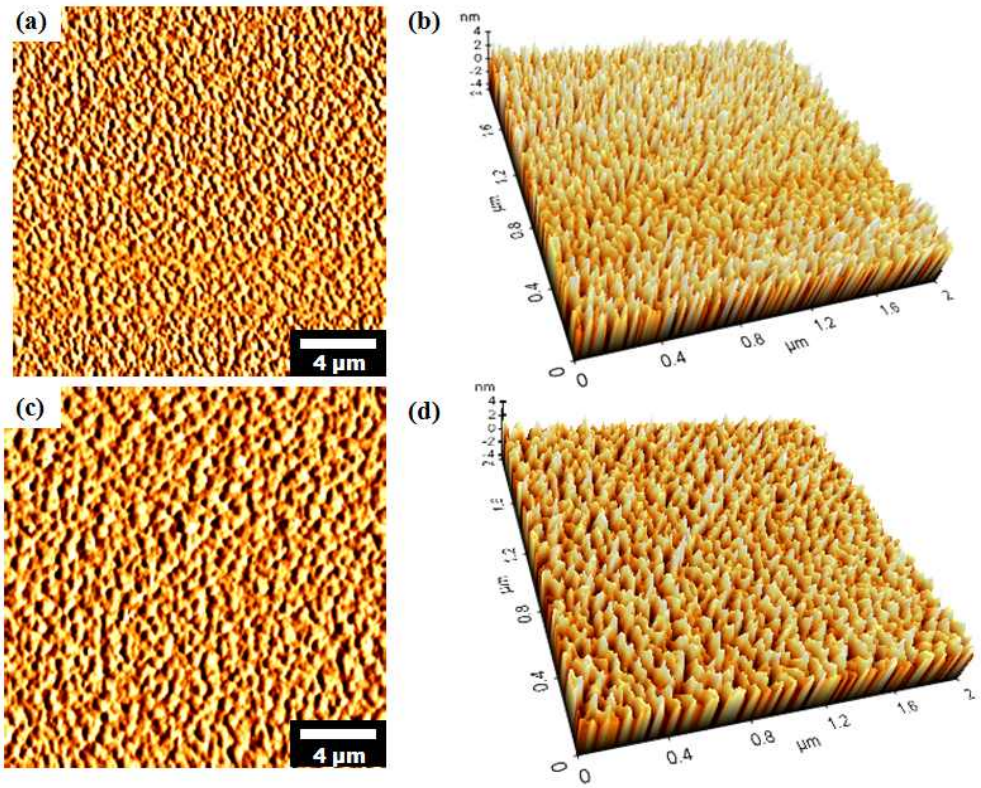


Figure 7.7. Top views and 3D views of AFM images: (a) The sobel transform image of intrinsic ZnO thin film (RMS=1.261 nm), (b) 3D view of intrinsic ZnO thin film, (c) The sobel transform image of Na-doped ZnO thin film (RMS=1.121 nm), (d) 3D view of Na-doped ZnO thin film.

7.4 Analysis of Na doped ZnO by X-ray photoelectron spectroscopy (XPS)

In this study, a Na doped ZnO precursor solution is used in the proposed patterning method for high performance TTFTs. Our group previously reported alkali metal doping with Li, Na, K, and Rb in a ZnO precursor solution for high performance ZnO TFT.[18] Specially, we focused on a Na doping in ZnO precursor solution. Even though Na has been rarely researched as N-type dopant, Na is the one of among the most cheapest and common elements and has enough potential to avoid the problem of a scarcity of resources. In the case of the low temperature sintering, Na ions locate in ZnO crystal structure as interstitial sites (electron donors) rather than substitutional sites (acceptors),[19] and they cause defects such as oxygen vacancies in the ZnO matrix due to a lack of stoichiometry.[20]

The relationships between oxygen vacancies, metal oxide, and hydroxide in the ZnO semiconductor were shown in terms of the 1s oxygen peaks of the XPS (Figure 7.8). The four Gaussian sub-peaks of XPS data were centered at ~529.9, ~531.1, ~532.1 and ~533.3 eV (Figure 7.8a). The peak at ~529.9 eV could be assigned to oxide in oxide lattices (M-O),[21] and the peak at ~531.1 eV denoted the oxygen vacancies in the oxide lattices (Ovac).[22] The peak at ~532.1 eV could be assigned to the oxide in hydroxide (-OH), which includes absorbed oxygen on the surface of the ZnO thin films as - CO_3, H_2O and O_2.[23] The high energy level band at ~533.3 eV was assumed to be silicon dioxide (SiO_2)/Si substrate[24]; they were

selectively exposed by this patterning method. For the Na-doped ZnO, the peaks were shifted by 0.3 eV as a result of the doping(Figure 7.8b).[25] However, oxygen bound peak of Na atoms (Na-O) could not be detected from XPS, because the state of Na was interstitial doping ($Na \rightarrow Na_i^+ + e^-$) in ZnO. The detailed explanation of Na interstitial doping was demonstrated in the Chapter 5.2.1.

Generally, the mobility of ZnO is affected by the correlation between oxygen lattices (M-O) and oxygen vacancies (Ovac). To maximize the field effect mobility, n-doped ZnO semiconductors require both the proper amount of oxygen vacancies exceeding that of intrinsic ZnO semiconductors for percolation conduction induced by the high concentration of free electrons and the reduction of trap sites which is represented by the increase of amount of metal oxide lattices (M-O) (Figure 7.9a-c).[26] However, the correlation between oxide lattice(M-O) and Ovac is somewhat controversial. The previous report demonstrated that the increment of M-O in the ZnO crystal structure induced by the sintering at high temperatures is required for high performance ZnO TFT devices. The high temperature sintering is essential for the removal of the oxygen vacancies that produce potential wells as trap sites, which hinder the free movement of electrons.[22,27] On the contrary to above phenomenon, the increase of oxygen vacancies also can enhance the electrical performance of devices.[21] The oxide sublattice (Oox) in the ZnO crystal structure transformed to O_2 gas by high sintering temperature, which creates a doubly charged oxygen vacancy (Vo) in the ZnO crystal structure

with two free electrons. The increment of free electron induced by oxygen vacancy can enhance the carrier transport by filling the trap states at high carrier concentration, which is percolation conduction theory.[21,27] The oxygen vacancy makes the trap states, which degrade the carrier transport, as well as has potential to generate two free electrons as carriers, which enhance the carrier transport.

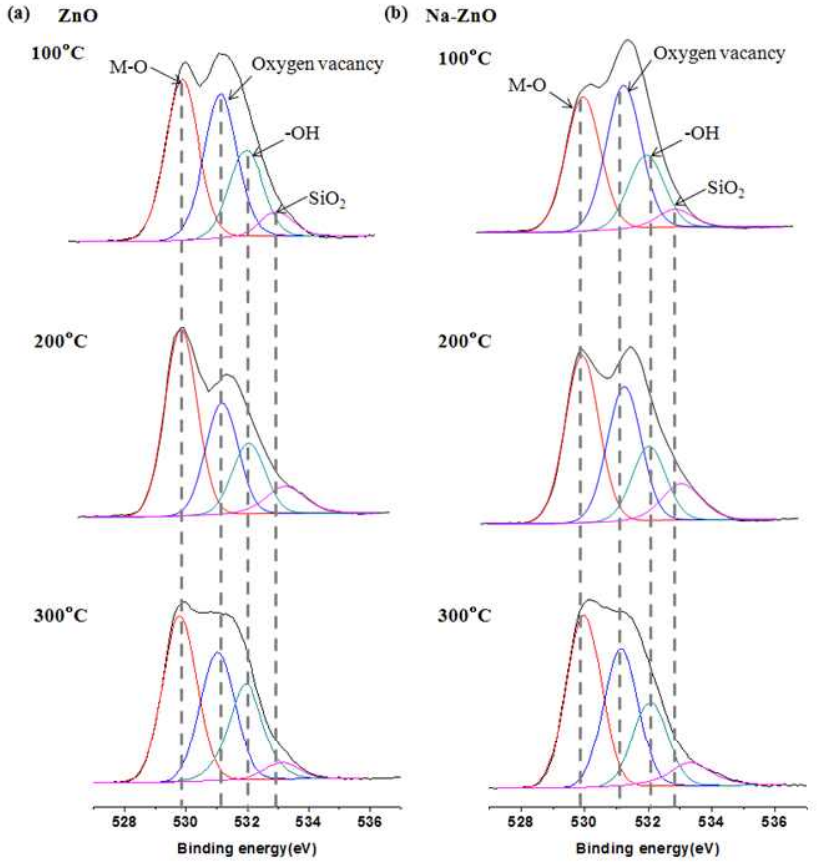


Figure 7.8. The oxygen (O) 1s peaks of the intrinsic/doped ZnO film in the temperature range of 100 - 300 °C sintering on a SiO_2 substrate, as measured by X-ray photo electron spectroscopy (XPS): (a) XPS O1s peaks of a patterned intrinsic ZnO TFT in the temperature range of 100 - 300 °C, (b) XPS O1s peaks of a patterned Na-doped ZnO TFT in the temperature range of 100 - 300 °C.

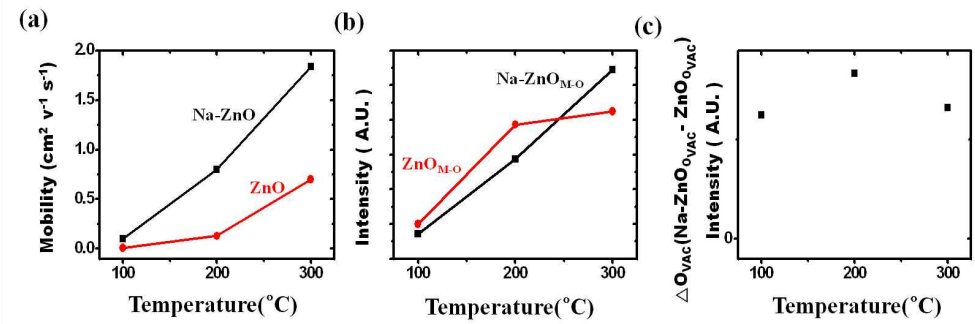


Figure 7.9. Analysis of the relative oxygen intensity (1s) and mobility changes of intrinsic/doped ZnO film transistors in the sintering temperature range of 100 - 300 °C on a SiO_2 substrate:(a) Relative mobility changes, (b) relative comparison of the oxygen intensity (1s) related to oxide lattices in the XPS data, (c) relative increment of the oxygen intensity (1s) related to oxide vacancies in the XPS data.

In this study, the field effect mobility of Na-doped ZnO TFT was explained the enhancement considering both effects - the variation of oxygen vacancy amount and oxide lattice amount - through the comprehensive analysis of XPS data (Figure 7.9). In the sintering range from 100 °C to 300 °C, the mobility was increased depending on the sintering temperature in all cases of the intrinsic and Na-doped ZnO TTFTs (Figure 7.9a). In the range from 100 °C to 200 °C, although the intensity of the oxide lattices (M-O) in the XPS data of the intrinsic ZnO TTFTs was slightly higher than that of the Na doped ZnO TTFTs (Figure 7.9b), the mobility of the Na-doped ZnO TTFTs, from 0.10 $cm^2v^{-1}s^{-1}$ to 0.80 $cm^2v^{-1}s^{-1}$, increased more rapidly than the increment of the mobility of the intrinsic ZnO TTFTs, from 0.01 $cm^2v^{-1}s^{-1}$ to 0.13 $cm^2v^{-1}s^{-1}$ (Figure 7.9a), because there were more free electrons from interstitial doping and oxygen vacancies. In these conditions, the amount of oxygen vacancy in Na doped ZnO was more than that in the intrinsic ZnO (Figure 7.9c). Also, in the range of 200 °C to 300 °C, the mobility of the Na-doped ZnO TTFTs, from 0.80 $cm^2v^{-1}s^{-1}$ to 1.84 $cm^2v^{-1}s^{-1}$, increased more rapidly than the increment of mobility of the intrinsic ZnO TTFTs, from 0.13 $cm^2v^{-1}s^{-1}$ to 0.70 $cm^2v^{-1}s^{-1}$ (Figure 7.9a). In this case, the increment of the oxygen lattices in the Na-doped ZnO TTFTs was higher than that of the intrinsic ZnO TTFTs (Figure 7.9b). The relative intensity, the intensity of oxygen vacancies in Na doped ZnO semiconductor minus the intensity of the oxygen vacancies in the ZnO semiconductor ($\triangle O_{VAC}$), of the oxygen vacancies in the

Na-doped ZnO semiconductor films as fabricated by this method was always higher than that of the intrinsic ZnO films when sintered from 100 °C to 300 °C (Figure 7.9c). In these reasons, the results suggested that Na ions acted as electron donors in the ZnO interstitial sites and caused a lack of stoichiometry, which effectively induced oxygen vacancies. The free electrons induced from interstitial doping and oxygen vacancies promoted the carrier transport by percolation conduction over the trap states even though the oxygen vacancies produced potential trap wells. Additionally, the increment of oxygen lattices, which are represented by XPS peak of metal oxide (M-O) bond, decreased the trap states in ZnO films and this effect promoted effectively the carrier transport.

7.5 Electrical characteristics

To show the potential of this patterning and developing method, I demonstrated the electrical performance of a solution-processed ZnO film TTFT with a low-temperature sintering process in the range of 100 ~ 300 °C. As plastic substrates for flexible devices restrict the temperature of the thermal process to less than 300 °C, a low-temperature process is essential to fabricate flexible devices on a plastic substrate.

The output curves and transfer curves of TTFTs after sintering at 100 °C, 200 °C and 300 °C were presented in Figure 7.10 respectively. The hysteresis and repeated transfer characteristics of the ZnO TTFTs as fabricated by this method with sintering in the range of 100 ~ 300 °C were presented in Figure 7.11. In this study, the ZnO TTFTs showed a highly saturated current as n-type TFTs that can be adapted for application in electronic-switching components (Figure 7.10a-c). In order to show the performance difference between the intrinsic ZnO TTFTs and the Na-doped ZnO TTFTs, we fabricated TTFTs with intrinsic ZnO patterns and with Na-doped ZnO patterns. From an analysis of the transfer curve of the intrinsic ZnO TTFTs after sintering at 100 °C, a mobility μ = 0.01 $cm^2v^{-1}s^{-1}$ with a threshold voltage V_{th} = 9.78V (Figure 7.12) were noted. For the Na-doped ZnO TTFTs after sintering at 100 °C, the mobility increased dramatically by 10 times compared to the intrinsic ZnO TTFTs, with μ = 0.10 $cm^2v^{-1}s^{-1}$ at a threshold voltage V_{th} = 14.6 V with a low hysteresis voltage(Figures 5d and 6a). After four

hysteresis tests, the hysteresis voltage declined to 0.75V. Furthermore, despite the low-temperature sintering process, the patterned Na-doped ZnO TTFTs showed good operational stability with identical transfer characteristics even after 20 repeated operations (Figure 7.11d). In the case of the Na-doped ZnO TTFTs after sintering at 200 °C, the mobility increased to μ = 0.80 $cm^2v^{-1}s^{-1}$ with a threshold voltage V_{th} = 17.56 V and the hysteresis voltage was negligible (Figure 7.10e and 7.11b). Also, good operational stability was shown during 20 repeated operations (Figure 7.11e). In the case of the Na-doped ZnO TTFTs after sintering at 300 °C, they showed a mobility of μ = 1.84 $cm^2v^{-1}s^{-1}$ at a threshold voltage V_{th} = 14.7 V with a very low hysteresis voltage (Figure 7.10f and 7.11c). They showed also good operational stability during the 20 repeated operations (Figure 7.11f). The on-off ratio of the TTFTs increased depending on the increase of the sintering temperature. Thus, the patterning technique onto photoinduced hydrophilic regions using drop and casting and the developing technique of the ammonia-ZnO precursor solution using methanol were successfully applied for the fabrication of Na-doped ZnO TTFTs, which exhibited excellent operational stability and high electrical performance without any leakage current. Consequently, the patterned ZnO films completely blocked cross-talk noise and current leakage without any significant charge trapping. We also fabricated the micopattened Li-doped ZnO TTFTs using the proposed method in this study. In the case of the Li-doped ZnO TTFTs after sintering at 100 °C, the mobility increased by 2 times in comparison with that of

Na-doped ZnO TTFTs. (Figure 7.13a and Figure 7.13b) After four hysteresis tests, the hysteresis voltage declined to 1.6 V. (Figure 7.13c) These results showed that various alkali metal doped ZnO TTFT can be successfully fabricated by our patterning method.

I summarize the electrical characteristics of each ZnO TTFT patterned on a SiO_2/Si substrate in Table 7.1. All of the devices were measured at the same drain voltage (V_D=60V). One significant point was that the patterned Na-doped ZnO TTFTs sintering at 100 °C showed reliable operation with a mobility μ = 0.10 $cm^2v^{-1}s^{-1}$. This signified that the proposed method could be applicable for flexible e-paper[28] or with radio frequency identification (RFID)[29-30] on plastic substrates with direct patterning due to the low decomposition temperature of the ammonia-ZnO aqueous precursor and the unique utilization of methanol for neat and dense ZnO film patterns. Furthermore, this patterning method confirmed good operational stability and very low hysteresis (Figure 7.11); thus, it has good potential toward future printed electronics.

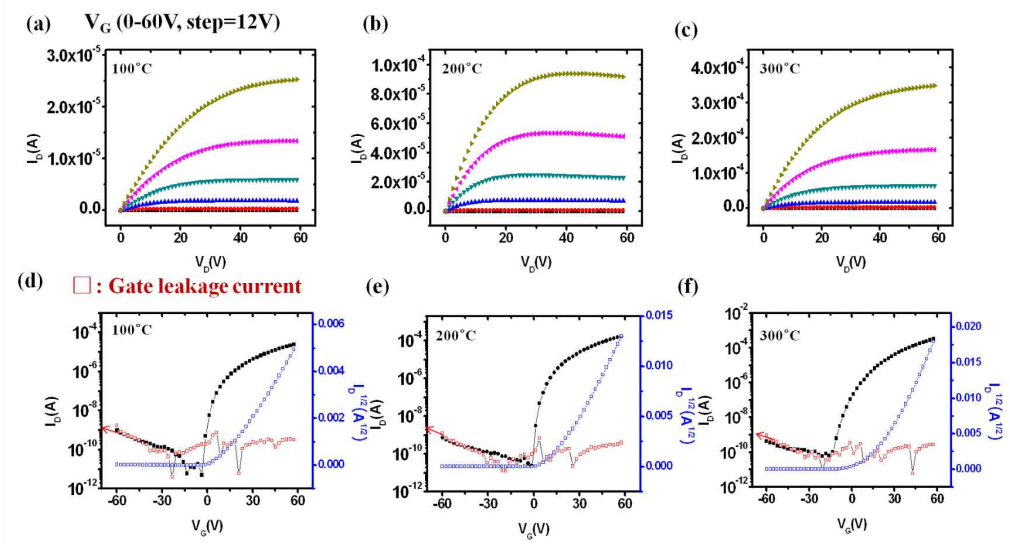


Figure 7.10. Output curves of patterned Na doped ZnO TFT after sinterring at (a) 100 °C; (b) 200 °C; (c) 300 °C. Transfer curves of patterned Na doped ZnO TFT after sinterring at (d) 100 °C; (e) 200 °C; (f) 300 °C.

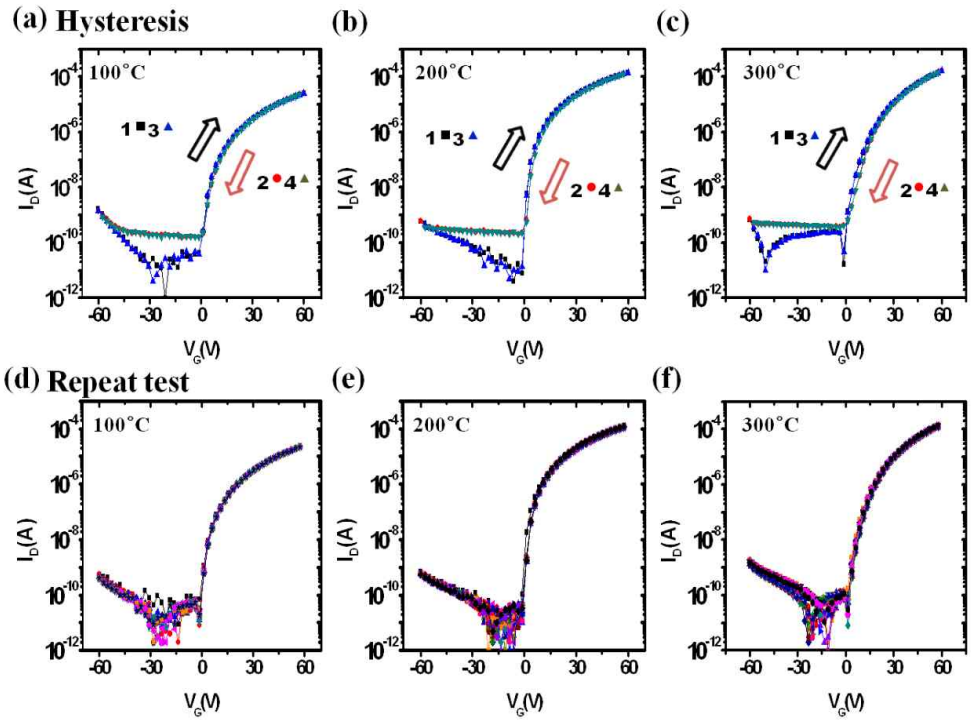


Figure 7.11. Hysteresis and repeated transfer characteristics of Na-doped ZnO TFT in the range of 100 ~ 300 °C sinterring with a W/L ratio of 20. (a), (b), and (c): The hysteresis-transfer curves of Na-doped ZnO TFT after sintering at 100, 200, and 300 °C. (d), (e), and (f): The repeating transfer curves of Na-doped ZnO TFT by 20 times after sintering at 100, 200, and 300 °C.

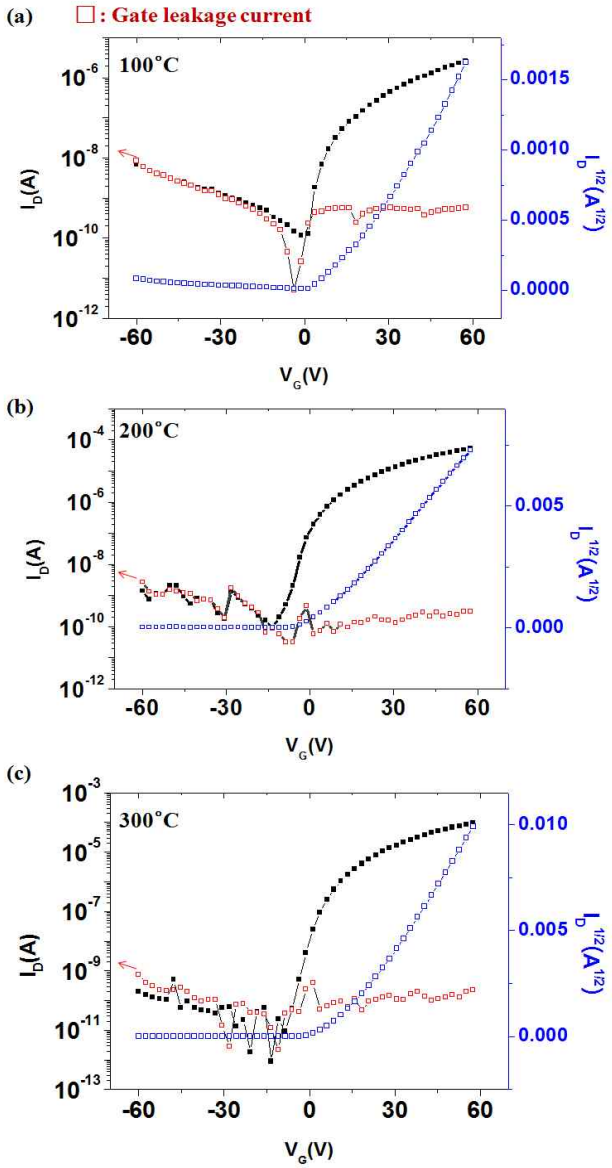


Figure 7.12. Transfer curves of the patterned intrinsic ZnO TFT after sintering at (a) 100 °C; (b) 200 °C; (c) 300 °C.

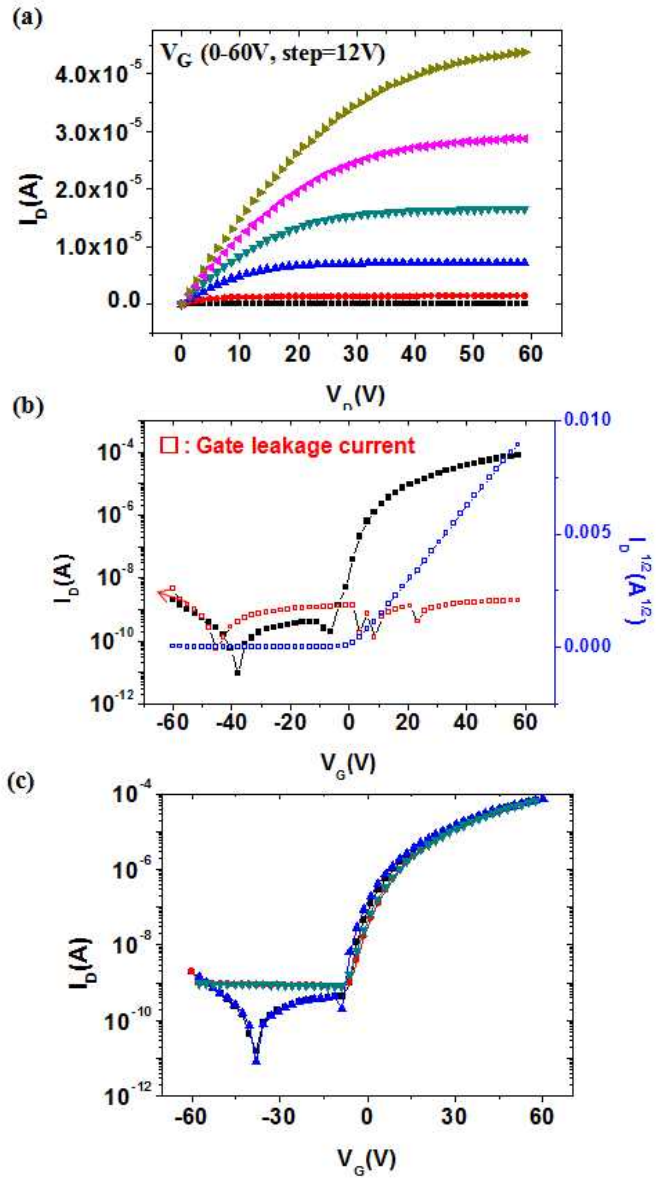


Figure 7.13. (a) Output curve of patterned Li doped ZnO TFT after annealing at 100 °C. (b) Transfer curve of patterned Na doped ZnO TFT after annealing at 100 °C. (c) The hysteresis-transfer curves of Na-doped ZnO TFT after annealing at 100 °C with a W/L ratio of 20.

Table 7.1. Electrical properties of the patterned intrinsic/Na doped ZnO TFT on SiO_2. (The operating voltage: 60 V)

Sintering Temp.(°C)	Material	$\mu(cm^2v^{-1}s^{-1})$	I_{on}/I_{off}
100	ZnO	0.01	1.9×10^4
	Na-ZnO	0.10	4.6×10^6
200	ZnO	0.13	6.4×10^5
	Na-ZnO	0.80	6.6×10^6
300	ZnO	0.70	6.1×10^6
	Na-ZnO	1.84	1.1×10^7

7.6 References

[1] K. K. Banger, Y. Yamashita, K. Mori, R. L. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, Nat. Mater. 2011, 10, 45.

[2] M. G. Kim, M. G. Kanatzidis, A. Facchetti and T. J. Marks, Nat. Mater. **2011**, 10, 382.

[3] S. O. Beng, L. Chensha, L. Yuning, W. Yiliang and L. Rafik, J. Am. Chem. Soc. **2007**, 129, 2750.

[4] S. T. Meyers, J. T. Anderson, C. M. Hung, J. Thompson, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc. **2008**, 130, 51.

[5] N. YamamotoH. MakinoS. OsoneA. UjiharaT. ItoH. HokariT. MaruyamaT. YamamotoThin Solid Films **2012**, 520, 4131.

[6] H. S. Shin, G. H. Kim, W. H. Jeong, B. D. Ahn, and H. J. Kim, Jpn. J. Appl. Phys. **2010**, 49, 03CB01.

[7] S. H. K. Park, C. S. Hwang, H. Y. Jeong, H. Y. Chu, and K. I. Cho, Electrochem. Solid-State Lett. **2008**, 11, H10

[8] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J. S. Park, J. K.Jeong, Y. G. Mo, and H. D. Kim, Appl. Phys. Lett. **2007**, 90, 212114.

[9] S. H. K. Park, D. H. Cho, C. S. Hwang, S. Yang, M. K. Ryu, C. W. Byun, S. M. Yoon, W. S. Cheong, K. I. Cho, and J. H. Jeon, ETRI J. **2009**, 31, 653.

[10] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P. Woo, Science. **2000**, 290, 2123.

[11] S. Dasgupta, R. Kruk, N. Mechau and H. Hahn, ACS nano **2011**, 5, 12, 9628.

[12] D. Kim, Y. Jeong, K. Song, S. K. Park, G. Cao and J. Moon, Langmuir 2009, 25, 18, 11149.

[13] B. Zhao, C.-L. Wang, Y.-W. Chen, and H.-L. Chen, Mater. Chem. Phys. 2010, 121, 1.

[14] J. J. Richardson and F. F. Lange, Cryst. Growth Des. 2009, 9, 2570.

[15] M. George, and R. G. Weiss, Langmuir 2002, 18, 7124.

[16] K. Kim, S. Park, J. B. Seon, K. H. Lim, K. Char, K. Shin and Y. S. Kim, Adv. Funct. Mater. 2011, 21, 3546.

[17] M. J. Lee, N. Y. Lee, J. R. Lim, J. B. Kim, M. Kim, H. K. Baik and Y. S. Kim, Adv. Mater. 2006, 18, 3115.

[18]S. Park, B. J. Kim, K. Kim, M. S. Kang, K. H. Lim, J. H. Cho, and Y. S. Kim, Ad4v. Mater. 2012, 24, 834.

[19] C. H. Park, S. B. Zhang, and S. H Wei, Phys. Rev. B. 2002, 66, 073202.

[20] B. Yaglioglu, H. Y. Yeom, R. Beresford, and D. C. Paine, Appl. Phys. Lett. 2006, 89, 062103.

[21] S. Jeong, Y. G. Ha, J. Moon, A. Facchetti and T. J. Marks, Adv. Mater. 2010, 22, 1346.

[22] H. Bong, W. H. Lee, D. Y, Lee, B. J. Kim, J. H. Cho and K. Cho, Appl. Phys. Lett. 2010, 96, 192115.

[23] G. H. Kim, H. S. Shin, B. D. Ahn, K. H. Kim, W. J. Park, and H. J. Kim, J. Electrochem. Soc. 2009,156,1, H7 - H9.

[24] S. M. Mukhopadhyay and S. H. Garofalini, J. Non-Cryst. Solids 1990, 126, 202.

[25] K. Yoshino, T. Hata, T. Kakeno, H. Komaki, M. Yoneta, Y. Akaki, and T. Ikari, Phys. Status Solidi C, 2003, 2, 626.

[26] T. Kamiya, K. Nomura and H. Hosono, J. Disp. Technol. 2009, 5, 273.

[27] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature. 2004, 432, 25.

[28] J.-K. Lee, Y.-S. Lim, C.-H. Park, Y-.I. Park, C-.D. Kim and Y.-K. Hwang, IEEE Electron Dev. Lett. 2010, 31, 8.

[29] C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters and D. M. de Leeuw, Appl. Phys. Lett. 1998 , 73 , 108.

[30] B. S. Ong, Y. L. Wu, Y. N. Li, P. Liu and H. L. Pan, Chem. Eur. J. 2008, 14, 4766.

Chapter 8. Conclusion

In conclusion, I have demonstrated a patterning method with binary solvent, solution-processed alkali metals doped ZnO, solution-processed ionic Al_2O_3 dielectric layer, interface engineering and new selective patterning method for the FTTFTs to achieve high-performance and low-temperature solution processed ZnO thin film transistors.

First and foremost, the direct patterning method with a toluene-methanol mixture develop uniformly and clearly patterned ZnO thin films with an ammine-hydroxo zinc solution using a pre-patterned PMMA layer. In view of the reported etching damage, uniform solution-processed ZnO thin films have been produced to avoid loss of electrical performance. In particular, the bifunctional property of the toluene-methanol mixture effectively controlled the ZnO thin film patterns without any defects. The toluene-methanol solvent mixture removed the extra PMMA layer from the pre-patterned substrate after deposition and simultaneously extracted water from the wet ZnO film. The ZnO patterns were completely isolated, which blocked current leakage without cumbersome processes such as a mechanical scribing or chemical etching, and showed higher performance than the previously reported mobility of a patterned intrinsic ZnO semiconductor. From a solution-processed patterned ZnO TFT with annealing at 300 °C under ambient conditions, we obtained an average mobility of 0.71 $cm^2v^{-1}s^{-1}$ with on/off current ratios $>10^7$. This simple patterning method is also easy

to apply on any flexible substrate. The patterning method was successfully adapted to fabricate a patterned flexible TTFT including a polymer dielectric layer.

Second, the solution-processed ionic amorphous Al_2O_3 dielectrics for the high electrical performance metal oxide TFTs with alow annealing process as maximum as 350 °C. When the ionic Al_2O_3 dielectric was examined on the solution-processed poly crystalline Li-ZnO TFTs and amorphous In-ZnO semiconductor TFTs with the annealing process at 350 °C, they exhibited the field-effect mobilities with 46.9 $cm^2v^{-1}s^{-1}$ in Li-ZnO TFTs and 44.2 $cm^2v^{-1}s^{-1}$ in In-ZnOTFTs with on/off current ratio of more than 10^{-5}. Moreover, nitrate ions in 350 °C annealed Al_2O_3 film facilitate the adsoption of water molecules by electrostatic force and the electrical double layer formation by H^+ mobile ions leading to high capacitance. These ionic amorphous Al_2O_3 dielectrics success fully meet the various needs of next generation high-performance TFTs, such as low-cost, solution-processability, and a relatively low-temperature process, and show good potential toward switching TFTs in advanced displays.

Finally, self-assembled inorganic layer (SAIL) was fabricated by photo-induced transformation technique of a self-assembled PDMS mono layer to control interface between a solution-processed ZnO semiconductor and polymer dielectric layers. In particular, the SAIL between the inorganic and organic layers remarkably suppressed the flat band shift that was proved by V_{FB} of analytic model for nano-crystalline ZnO-based TFTs. The V_{FB} shift was successfully

analyzed the hysteresis of the transfer characteristics of both interface engineered TFTs and non-interface engineered TFTs using the analytic model. Obviously, V_{FB} shift = 0.49 V of the ZnO/SAIL/PVP TFT was much smaller than V_{FB} shift = 8.81 V of the non-interface engineered ZnO/PVP TFT. These results showed that that the SAIL process between ZnO and polymer successfully suppressed the interface trap, which caused V_{FB} - shifting and electrical hysteresis behavior. Also, ZnO/SAIL/PVP/TPC TFT showed a field-effect mobility of 0.28 $cm^2 \cdot V-1 \cdot s-1$and an on/off current ratio of more than 10^{-6} in a low temperature process as high as 200 °C, which has nearly quadrupled in comparison with a field-effect mobility of ZnO/SAIL/PVP TFT. It was caused by an advanced hybrid material, such as TPC, that the electrical performance can be enhanced by high K dielectric materials. Furthermore, as we successfully fabricated the FTTFT and showed flexibility in the bending radius range from 20 mm to 10 mm, the SAIL process is not only very valuable interface engineering process, which can be applied in various hybrid electrical devices. Furthermore, interface engineered patterning method was proposed as direct patterning method with removal of the residual ammonia ligands in a ZnO precursor by methanol as interface engineering's application. The methanol blocked the formation of ammonium carbamate and effectively controlled the patterning with the aqueous ammonia-ZnO precursor solution. In particular, because the ammonia-ZnO precursor could be transformed easily to $Zn(OH)_2$ on the substrate by the ligand extraction of

methanol and the $Zn(OH)_2$ films were easily sintered to ZnO films at alow temperature, uniform Na-doped ZnO TTFTs were successfully achieved with very low temperature annealing and showed good operational stability, μ = 0.1 $cm^2v^{-1}s^{-1}$ and I_{on}/I_{off} = 4.6 x 10^6, even after sintering at temperatures as low as 100°C. Under ambient conditions, the patterned Na-doped ZnO TTFTs exhibited a high electron mobility μ = 1.84 $cm^2v^{-1}s^{-1}$ with excellent operational stability and low hysteresis with sintering at 300°C. This method is not only simple as compared to photolithography and ink jet printing but is also a sophisticated patterning process with good fidelity for solution processed ZnO films.

In this regard, the proposed Interface & materials methods show good process fidelity with greatly enhanced in electrical properties of solution processed ZnO TFT, I believe it has tremendous potential to fabricate future oriented electronic devices. The Interface & materials methods are cut out for the flexible TTFT and can be applied to various fields as electronic devices continue to develop and expand.

Appendix

List of publications

1. SCI journal

[1] 1st author

1. **Kyongjun Kim**, Siyun Park, Jong-Baek Seon, Keon-Hee Lim, Kookheon Char, Kyusoon Shin, and Youn Sang Kim, "Patterning of Flexible Transparent Thin-Film Transistors with Solution-Processed ZnO Using the Binary Solvent Mixture", Adv. Funct. Mater. **2011**, 21, 3546.

2. **Kyongjun Kim**, Si Yun Park, Keon-Hee Lim, ChaeHo Shin, Jae-Min Myoung and Youn Sang Kim, "Low temperature and solution-processed Na-doped zinc oxide transparent thin film transistors with reliable electrical performance using methanol developing and surface engineering", J. Mater. Chem., **2012**, 22, 23120.

3. **Kyongjun Kim**, Jee Ho Park, Young Bum Yoo, Si Yun Park, Keon-Hee Lim, Keun Ho Lee, Hong Koo Baik and Youn Sang Kim, "Water adsorption effects of nitrate ion coordinated Al2O3 dielectric for high performance metal-oxide thin film transistor", J. Mater. Chem. C, **2013**, 1, 7166.

4. **Kyongjun Kim**, Eungkyu Lee, Joohee kim, Si Yun Park, Keon-Hee Lim, ChaeHo Shin and Youn Sang Kim, "Interface

engineering for suppression of flat-band voltage shift in a solution-processed ZnO/polymer dielectric thin film transistor", J. Mater. Chem. C, **2013**, 1, 7742.

[2] Co-author

5. Si Yun Park, Beom Joon Kim, **Kyongjun Kim**, Moon Sung Kang, Keon-Hee Lim, Tae Il Lee, Jae M. Myoung, Hong Koo Baik, Jeong Ho Cho, and Youn Sang Kim, "Low-Temperature, Solution-Processed and Alkali Metal Doped ZnO for High-Performance Thin-Film Transistors", Adv. Mater. **2012**, 24, 834.

6. Sung Yun Chung, Sunyoung Kim, Ju-Hyuck Lee, **Kyongjun Kim**, Sang-Woo Kim, Chong-Yun Kang, Seok-Jin Yoon, and Youn Sang Kim, "All-Solution-Processed Flexible Thin Film Piezoelectric Nanogenerator", Adv. Mater. **2012**, 24, 6022

7. Keon-Hee Lim, **Kyongjun Kim**, Seonjo Kim, Si Yun Park, Hyungjun Kim, and Youn Sang Kim, "UV-Visible Spectroscopic Analysis of Electrical Properties in Alkali Metal-Doped Amorphous Zinc Tin Oxide Thin-Film Transistors", Adv. Mater. **2013**, 25, 2994.

8. Si Yun Park, **Kyongjun Kim**, Keon-Hee Lim, Beom joon Kim, Eungkyu Lee, Jeong Ho Cho, and Youn Sang Kim, "The Structural, Optical and Electrical Characterization of High- Performance, Low-Temperature and Solution-Processed Alkali Metal-Doped ZnO

TFTs", Journal of Materials Chemistry C, **2013,** 1, 1383.

9. Kieun Seong, **Kyongjun Kim**, Si Yun Park and Youn Sang Kim, "Micro-patterned ZnO semiconductors for high performance thin film transistors via chemical imprinting with a PDMS stamp", Chem. Comm. **2013**, 49, 2783.

10. Si Yun Park, **Kyongjun Kim**, Keon-Hee Lim, Eungkyu Lee, Seonjo Kim, Hyungjun Kim and Youn Sang Kim, "Alkali Earth Metal Dopants for High Performance and Aqueous-derived ZnO TFTs", RSC Advances, **2013,** 3, 21339.

11. ChaeHo Shin, **Kyongjun Kim**, JeongHoi Kim, Wooseok Ko, Yusin Yang, SangKil Lee, ChungSam Jun and Youn Sang Kim, "Fast, exact, and non-destructive diagnoses of contact failures in nano-scale semiconductor device using in-line conductive AFM", Scientific reports, **2013**, 3, Article number: 2088

12. Jieun Ko, Joohee Kim, Si Yun Park, Eungkyu Lee, **Kyongjun Kim**, Keon-Hee Lim and Youn Sang Kim, "Solution-Processed Amorphous Hafnium-Lanthanum Oxide Gate Insulator for Oxide Thin- Film Transistors", Journal of Materials Chemistry C, **2014,** 2, 1050.

13. Si Yun Park, Sunyoung Kim, Jeeyoung Yoo, Keon-Hee Lim,

Eungkyu Lee, **Kyongjun Kim**, Joohee Kim and Youn Sang Kim, "Aqueous zinc ammine complex for solution-processed ZnO semiconductors in thin film transistors", RSC Advances, **2014,** 4, 11295.

14. Eungkyu Lee, Jieun Ko, Keon-Hee Lim, **Kyongjun Kim**, Si Yun Park, Jae M. Myoung and Youn Sang Kim, "Gate Capacitance-Dependent Field-Effect Mobility in Solution Processed Oxide Semiconductor Thin-Film Transistors", Adv. Funct. Mater. **2014,** 24, 4689.

15. Jieun Ko, Su Jeong Lee, **Kyongjun Kim**, EungKyu Lee, Keon-Hee Lim, Jae-Min Myoung, Jeeyoung Yoo and Youn Sang Kim, "A Robust Ionic Liquid-Polymer Gate Insulator for High-Performance Flexible Thin Film Transistors", Journal of Materials Chemistry C, **2015,** 3, 4239.

2. International Conference

[1] 1st author

1. **Kyongjun Kim**, Si Yun Park, SeungChul Yew, and Youn Sang Kim, **2011**, "Patterning of flexible transparent thin film transistors with solution-processed ZnO using binary solvent mixture" 2011 MRS(Materials Research Society) Spring Meeting & Exhibit, San Francisco, USA, April 29, -oral

2. **Kyongjun Kim**, **2011**, “A simple patterning method of solution-processed ZnO thin film for flexible transparent thin film transistors”, International Conference on Advanced Electromaterials (ICAE), Jejudo, Republic of Korea, Nonember 10. -oral

[2] Co-author

3. ChaeHo Shin, **Kyongjun Kim**, and Youn Sang Kim, **2010**, “Nanoparticle alignment and nanoscale stamp manufacture by atomic force microscopy indentation”, IEEE NANO 2010 - Joint Symposium with NANO KOREA 2010, Ilsan-si, Gyeonggi Province, Republic of Korea, August 20 -poster

4. Min Jung Lee, Jihyun Lee, **Kyongjun Kim**, Si Yun Park, and Youn Sang Kim, **2010**, “Pressure-assisted metal printing with an anti-adhesive rigiflex stamp”, IEEE NANO 2010 - Joint Symposium with NANO KOREA 2010, Ilsan-si, Gyeonggi Province, Republic of Korea, August 20 - poster

5. Min Jung Lee, Jihyun Lee, **Kyongjun Kim**, Si Yun Park, and Youn Sang Kim, **2010**, “Crack-free metal transfer with a rigiflex stamp by a pressure-assisted printing”, The International Chemical Congress of Pacific Basin Societies (Pacific Chem 2010), Hawaii, USA, December 18. -poster

6. Joohee Kim, **Kyongjun Kim**, SeungChul Yew, Dae Man Han, Si Yun Park, Sung Yun Chung, Jihyun Lee, and Youn Sang Kim, **2010**, "OTFTs with TiO_2-polymer composite gate insulator for low operating voltage", The International Chemical Congress of Pacific Basin Societies (Pacific Chem 2010), Hawaii, USA, December 18. -poster

7. ChaeHo Shin, **Kyongjun Kim**, Byeong-Hyeok Sohn, Zheong G. Khim and Youn Sang Kim, **2010**, "Nanopaticle Alignment and Nanoscale Stamp Manufacture by Atomic Force Microscopy Indentation", The 12th International Scanning Probe Microscopy Conference, Sapporo, Hokkaido, Japan, May 10-May 12

8. Si Yun Park, **Kyongjun Kim**, Keon-Hee Lim, and Youn Sang Kim, **2012**, "Low Temperature, Solution-processed and Alkali Metal Doped ZnO for High Performance Thin Film Transistors", MRS(Materials Research Society) Spring Meeting & Exhibit, San Francisco, USA, April 11. - oral

9. Keon-Hee Lim, **Kyongjun Kim**, Si Yun Park, and Youn Sang Kim, **2012**, "High-Mobility, Solution-Processed Alkali Metal Doped Amorphous Zinc TIN Oxide Thin Film Transistor", iMiD (The 12th International Meeting on Information Display), Daegu, Republic of Korea, August 28. - oral

10. Jieun Ko, **Kyongjun Kim**, Si Yun Park, and Youn Sang Kim, **2013**, “Solution Processed Hafnium-lanthanum Oxide Gate Insulator for ZnO Thin Film Transistors”, MRS Spring Meeting & Exhibit, San Francisco, USA, 2013, April 1-April5 - oral

11. Si Yun Park, **Kyongjun Kim**, Jieun Ko, Jae-Min Myoung, and Youn Sang Kim, **2013**, “The Optical analysis of Low-Temperature and Solution-Processed Alkali Metal-Doped ZnO TFTs”, MRS(Materials Research Society) Spring Meeting & Exhibit, San Francisco, USA, April 1-April 5. -poster

3. Domestic Conference

[1] 1st author

1. **Kyongjun Kim**, Joohee Kim, SeungChul Yew, Si Yun Park, Jihyun Lee, Sung Yun Chung, and Youn Sang Kim, **2010**, “A simple patterning method of solution-processed ZnO thin film for transparent thin fillm transistors”, 2010 한국고분자학회 추계 학술대회, Daegu, Republic of Korea, October 8. - poster

2. **Kyongjun Kim**, Si Yun Park, Joohee Kim, SeungChul Yew, and Youn Sang Kim, **2011**, “Selective micro patterns of the solution-processed ZnO developed by azeotrocpic solvent for the transparent thin film transistor”, The 1st Conference on Pioneering Convergence Technologies, Suwon-si, Gyeonggi Province, Republic of

Korea, February 15. -oral

[2] Co-author

3. Joohee Kim, Min Jung Lee, Sung Hee Lim, **Kyongjun Kim**, Haekyu Jang, and Youn Sang Kim, **2009**, "Free-standing film electronics using photo-cross linking layer-by-layer assembly", 한국고분자학회 추계 학술대회, Daegu, Republic of Korea, October 8. - poster

4. Joohee Kim, **Kyongjun Kim**, Haekyu Jang, Min Jung Lee, Sung Hee Lim, and Youn Sang Kim, **2009**, "Patchable organic transistors using photo-crosslinking layer-by-layer assembly", Ilsan-si, Gyeonggi Province, Republic of Korea, 한국화학공학회 추계 학술대회, October 23. - poster

5. Sung Hee Lim, Min Jung Lee, Joohee Kim, **Kyongjun Kim**, SeungChul Yew, Si Yun Park, Jihyun Lee, Sung Yun Chung, Dae Man Han, and Youn Sang Kim, **2010**, "Water- soluble polymer dielectric toward high performance organic thin film transistor", 2010 한국고분자학회 춘계 학술대회, Daejeon, Republic of Korea, April 9. - poster

6. Joohee Kim, **Kyongjun Kim**, SeungChul Yew, Si Yun Park, Jihyun Lee, Sung Yun Chung, Hanju Jo, and Youn Sang Kim, **2010**, "The OTFTs including Soluble-based TiO_2-PVP composite gate insulator

for low operating voltage", 한국화학공학회 추계 학술대회, Busan, Republic of Korea, October 20. - poster

7. Youn Sang Kim, Joohee Kim, Jihyun Lee, and **Kyongjun Kim**, **2010**, "Ultra-thin PDMS coating and Its applications for Various Organic Devices", 한국고분자학회 추계 학술대회, Daegu, Republic of Korea, October 7. -oral

8. Sung Yun Chung, **Kyongjun Kim**, Hanju Jo, Keon-Hee Lim, Jieun Ko, and Youn Sang Kim, **2011**, "ZnO nanorod Arrays Integrated Piezoelectric Nanogengerator Using Aqueous Solution Method", 2011 춘계 한국공업화학회, Jejudo, Republic of Korea, May 13. - poster

9. Kieun Seong, **Kyongjun Kim**, **2012**, "Simple patterning of thin ZnO semiconductor film using soft lithography", The 2nd Conference on Pioneering Convergence Technologies, Suwon-si, Gyeonggi Province, Republic of Korea, February 4. - oral

10. Keon-Hee Lim, **Kyongjun Kim**, Si Yun Park, Joohee Kim, Eungkyu Lee, Jieun Ko, Yong Keon Ahn, and Youn Sang Kim, **2013**, "Characterization of Alkali Metals-Doped Oxide Thin Film Transistor using UV-visible Spectroscopy Analysis", 한국전기전자재료학회 하계 학술대회, June 19-June 21. -oral

11. Youn Sang Kim, **Kyongjun Kim**, Si Yun Park, and Sung Yun

Chung, 2013, “Solution-processed ZnO metal oxide semiconductor for various functional devices”, 한국물리학회 봄 학술논문발표회 및 제89회 정기총회, Daejeon, Republic of Korea, April 24-April 25. -oral

요 약 (국문초록)

용액형 산화아연 반도체 박막 트랜지스터를 위한 자기 조립 계면과 소재 공정에 관한 연구

본 연구에서는 플라스틱 기판위에서 투명 플렉시블 구동 소자를 구현할 수 있도록 저온 소성 가능한 용액형 박막 트랜지스터 개발을 위하여 용액형 산화아연 반도체 전구체 및 도핑 방법과 패터닝, 그리고 산화 알루미나 절연체와 효율적인 계면 공정을 개발하였다.

우선 산화아연은 양친성 물질이며 다공성 구조로써 기존의 포토리소그래피에서의 공정 중 강 염기성 포토 레지스트 스트리퍼(photo resist stripper) 용매에 의하여 계면에서 침투된 용매에 의하여 성능 저하를 유발하게 된다. 따라서 저온 소성 가능한 아연 아민 착제를 활용하여 기존 포토리소그래피를 사용하지 않고 폴리머 뱅크(bank) 구조를 이용하여 선구조 형성 후 산화 아연 아민 착제가 표면에서 암모니엄 카보네이트를 형성하는 것을 막고 깔끔한 패턴으로 형성하고자 메탄올과 톨루엔을 1:4 부피 비율로 합성한 binary solvent mixture를 통하여 lift-off 방식을 만들었다. 이를 통해 기존의 아연산화물 패턴 형성 시 사용되었던 강염기 및 산성의 용매를 사용하지 않고 유기 용매를 통한 균일한 용액형 패턴 형성 방법을 만들었다.

다음으로 저온형 공정을 위한 산화 아연 아민 착제 반응을 이용한 새로운 알칼리 금속 도핑된 용액형 ZnO 기반의 금속산화물 반도체 소재와 이러한 용액형 반도체의 성능을 극대화 할 수 있는 고 성능의 용액형 산화 알루미나 절연체를 개발하였다. 350 °C의 저온에서 형성된 산화 알루미나 절연체와 산화 아연 반도체를 통합 소자를 개발하여 46.9 cm^2/Vs의 굉장히 높은 전계 효과 이동도를 구현하였다. 그리고 이러한 고성능

은 각 온도와 습도 상황에서 측정하여 규명하였을 때 흡수된 물의 이온 효과에 의하여 고 정전용량이 형성되었음을 규명하였다.

마지막으로 플렉시블 소자로의 활용이 유리한 유기 절연체와 고 이동도의 산화 아연 반도체가 접합될 때 발생하는 플랫 밴드 전압 변화를 유발하는 계면 트랩을 효과적으로 제어할 계면을 무기 자기 조립 박막 형성 방법을 통해 개발하였다. 균일하게 형성된 PDMS 코팅을 한 후 ultraviolet ozone(UVO) 광 변화를 통하여 모노 실리카 계면으로 개질된 계면 형성 방법을 개발하였다. 이는 유기물과 무기물의 접합시의 계면 트랩에서 야기되는 계면 쌍극자(interface dipole)에 의한 플랫 밴드 전압 변화를 효과적으로 제어하였다. 또한 이의 활용으로 계면 공정 형성 방법을 적용하여 패터닝 기술을 개발하였다. 부분적으로 습윤성을 변화시켜 친수성과 소수성 계면을 선택적으로 패터닝하여 수용성 산화 아연 전구체 용액을 드롭-캐스팅(drop-casting)과 함께 메탄올의 반응을 통하여 100 °C의 저온 용액 공정에서도 안정적 소자 구현이 가능한 패터닝 방법을 개발하였다.

결론으로, 본 연구에서는 새로운 용액형 산화 아연 반도체 및 산화 알루미나 절연체 전구체 제조와 도핑 방법, 그리고 이를 효과적으로 사용하기 위한 패터닝 방법을 개발하였다. 그리고 유무기를 통합한 트랜지스터를 개발하기 위해서 무기 계면 자기 조립 박막을 개발하고 이의 효과적인 계면 트랩 억제를 이루었다. 이 기술들은 저온 용액 소성 방법으로써 고해상도 디스플레이 및 투명, 플렉서블 디스플레이에서의 구동 소자로의 충분한 가능성을 보여주었다.

주요어 : 용액형 산화 아연 반도체, 박막트랜지스터, 패터닝, 산화 알루미나 절연체, 알칼리 메탈 도핑, 계면 공정

학 번 : 2009-22459