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공학박사 학위논문

Hybrid Gate Insulators Fabricated by Solution Process for High Performance of Organic Thin Film Transistors

고성능 유기 전자소자를 위한 용액 공정 기반의 하이브리드 게이트 절연막에 관한 연구

2016 년 8 월

서울대학교 대학원

융합과학부 나노융합전공

김 주 희

Hybrid Gate Insulators Fabricated by Solution Process for High Performance of Organic Thin Film Transistors

지도교수 김 연 상

이 논문을 공학박사 학위논문으로 제출함

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Abstract

Hybrid Gate Insulators Fabricated by Solution Process for High Performance of Organic Thin Film Transistors

Joohee Kim

Program in Nano science and Technology

The Graduate School

Seoul National University

Organic thin film transistors (OTFTs) have attracted attention for next generation device, which shows transparent and flexible property. The main elements of OTFTs are semiconductor, gate insulator, and electrodes. To obtain the feature of flexible and transparent for OTFTs, the elements of them have to be composed of organic based materials or amorphous materials. Up to date, OTFTs

used organic materials mainly show a research tendency which was focused on high performance of organic semiconductor. Organic semiconductors need generally high operating voltage because those indicate intrinsically low field-effect mobility due to their driving system caused by hoping of electrons through $\pi-\pi$ intermolecular interactions between adjacent molecules. In this reason, in order to improve the performance of OTFTs, the gate insulators indicating high k property and low off current be required and have to be studied alongside organic semiconductors.

In this study, we focused the researches of gate insulators for inducing the conducting channel of semiconductor. Many researchers have tried to improve gate insulators for OTFTs by using organic materials, such as various polymers. Nevertheless, the organic based gate insulators have still several challenges, which are high leakage current and low dielectric constant (k). Whereas, metal oxides as high k materials, such as TiO_2, Ta_2O_5, and HfO_2, exhibits high leakage current due to polycrystalline formation tendency and narrow band gap as insulator. Here are the suggestions of polymer-metal oxide

composite and metalorganic compound as gate insulators. They show flexible and transparent properties of polymer as well as increased dielectric constant due to high k materials.

First, we have introduced the TiO_2–PVP composite (TPC) gate insulator to overcome the problems discussed above. The TPC is composed of a TiO_2 precursor (titanium (IV) butoxide and acetyl acetone) and poly (4–vinylphenol) (PVP) solution (PVP, poly (melamine–*co*–formaldehyde) methylated/butylated and propylene glycol methyl ether acetate (PGMEA) solvent). As this TPC gate insulator can easily be deposited by a simple solution process and exhibits a considerably low surface energy, it generates a smooth and hydrophobic surface that allows the uniform vertically oriented growth of small semiconductor molecules and closely packed grains between crystal domains. Also, the TiO_2 precursor induces an increased dielectric constant compared with the dielectric constant of pristine PVP. As this enhanced dielectric property leads to the increased drain current at a low operating gate bias voltage, the OTFTs including the TPC gate insulator could be successfully

operated at gate bias voltage of V_G = −3 V. Furthermore, this homogeneous TiO_2−PVP composite solution is stable in ambient conditions, and it was easily applied in the fabrication of OTFTs. As a result, the OTFTs with a TPC gate insulator exhibited the better transistor performance with an increased on/off ratio, improved mobility, and low subthreshold voltage at a low operating gate bias voltage compared to the performance of OTFTs that include a pristine PVP gate insulator.

Second, we suggest the flexible inorganic−organic hybrid gate insulator materials fabricated by sol−gel process, which can lead into not only the improved field−effect mobility but also the operation at low gate bias voltage in the pentacene based−OTFTs. This gate insulator was composed with two layers; one is the charge−accumulation inducing layer made with Tetraethyl orthosilicate (TEOS), (3−Glycidoxypropyl) trimethoxysilane (GLYMO), and titanium acetylacetone precursor, the other is the electron−trap blocking layer made with aqueous potassium hydroxide and SiO_X solution. These double−coated gate insulators successfully showed

the capability of the solution process at the low temperature annealing as maximum as 175 ℃ and the operation of the pentacene based-OTFTs at the low gate bias voltage (V_G = ±5 V). The electron-trap blocking layer efficiently obstructs the space-charge electret induced by the electrons which was injected from a gate electrode during the operation of pentacene based-OTFTs. Thus, the hysteresis originated from -OH groups could be successfully decreased.

As a result, they indicated the improved dielectric constant with ~ 5.2 and induced the advanced field-effect mobility with 2.59 cm^2/Vs at V_G = -20 V and 1.08 cm^2/Vs at V_G = ±5 V in the pentacene based-OTFTs. Furthermore, to observe flexibility of the double-coated gate insulator, we conducted the bending test of its thin film and pentacene based-OTFTs up to enduring maximum curvature of bending distance 5 mm.

Keyword : organic thin film transistors, gate insulator, high *k* materials, hybrid materials, sol-gel process, hysteresis

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List of Abbreviations

AFM	Atomic force microscope
BCB	Bensocyclobutene
CYTOP	Poly (perfluorobutenylvinylether)
GLYMO	(3-Glycidoxypropyl) trimethoxysilane
HOMO	Highest molecular orbital
LUMO	Lowest molecular orbital
MIBK	Methyl isobuthylketone
MIM	Metal-insulator-metal
OMBD	Organic Molecular beam deposition
OTFTs	Organic thin film transistors
P3HT	Poly(3-hexylthiophene)
PAA	Poly (acrylic acid)
PET	Polyethylene terephthalate
PGMEA	Propylene glycol methyl ether acetate
PMMA	Poly (methyl-methacrylate)
PS	Poly styrene
PVA	Poly (vinyl alcohol)
PVP	Poly (4-vinylphenol)
SAM	Self-assembled monolayer
SEM	Scanning electron microscope
TEOS	Tetraethyl orthosilicate

TIPS (6, 13-(Bis(triisopropylsilyethynyl)

TPC Titanium oxide-poly (4-vinylphenol) composite

UVO Ultra-violet ozone

XRD X-ray diffraction

Chapter 1. Introduction

1.1 Introduction

Organic thin film transistors (OTFTs) have a tremendous potential for next generation devices, such as flexible mobile display [1], e-paper [2], and large area billboard [3], because OTFTs show remarkable flexibility, transparency and low-cost effective. To present the above mentioned properties, the two essential elements, such as semiconductor and gate dielectric, of transistors have to be made up transparent and flexible ingredients found in organic materials.

OTFTs used organic materials mainly show a research tendency which was focused on high performance of organic semiconductor. In the past two decades, a lot of researches have been done to improve the performance of valid organic semiconducting materials for flexible OTFTs such as pentacene [4], rubrene [5], poly (3-hexylthiophene) (P3HT) [6], 6, 13-(Bis(triisopropylsilyethynyl) (TIPS) pentacene [7].

However, organic semiconductors need high operating voltage because those indicate intrinsically low field-effect mobility due to their driving system caused by hoping of electrons through $\pi-\pi$

intermolecular interactions between adjacent molecules. [8] Applications fabricated by using organic materials are indeed required to operating in low voltage region (≤ ±5 V) for low power consumption and maintaining durability of devices. To overcome these disadvantages of organic devices, the research of gate dielectric needs for the amicable generation of conducting channel in interface of gate dielectric and semiconductor as well as the studies of organic active materials.

Generally, polymer materials are used for gate dielectric of OTFTs, which are typically poly (methyl-methacrylate) (PMMA) [9], poly styrene (PS) [10], poly (4-vinylphenol) (PVP) [11], and poly (perfluorobutenylvinylether) (CYTOP) [12]. These polymers are naturally superior flexibility and transparency but relatively lower dielectric constant than inorganic material, namely metal oxide. The transistors constituted to polymer materials as gate dielectric are necessary for high voltage for working and show the property of low field-effect mobility. On the contrary, the gate dielectric made from metal oxide is conventionally known as high dielectric constant and superior stability in high operating voltage although its thin film type shows very rigid and brittle properties. Also, metal oxide gate dielectric is formed by high cost deposition process due to

cumbersome vacuum equipment while the organic gate dielectric is fabricated by a simple and cost-effective solution process.

Therefore, to improve flexible polymer gate dielectric, the advantages of metal oxide were started to apply for organic materials by using simply mixing method and solution process. Previous studies were reported about polymer and metal oxide nanoparticles composite dielectric for avoiding the weak points of organic materials and introducing the strong points of inorganic materials. However, in the previous reports, the gate dielectric made from mixture of polymers and TiO_2 precursor still possessed the limitation of device performance because the intrinsic inferior dielectric constant of organic matrix determines dominantly the total capacitance of composite material. [13, 14]

In this research, to surmount the limitations of metal oxide-nanoparticles and polymer mixture, the titanium oxide-poly (4-vinylphenol) composite (TPC) dielectric elicited by binding of intermolecular was formed for OTFTs with low voltage operation (–3 V). [15] The TPC is composed of a TiO_2 precursor (titanium (IV) butoxide and acetyl acetone) and poly (4-vinylphenol) (PVP) solution (PVP, poly (melamine-*co*-formaldehyde) methylated/butylated and propylene glycol methyl ether acetate

(PGMEA) solvent). This TPC composite dielectric layer has a low leakage current similar to PVP polymer dielectrics due to dense chemical structure formed by cross-linking reaction between the polymer and TiO_2 precursor. Our OTFTs included with TPC as gate dielectric were well operated at low voltage region (-3 V) and showed enhanced performance than the device with pristine PVP gate dielectric. Also, to resolve the various drawbacks related with composite dielectric materials, we newly suggest the flexible inorganic-organic hybrid gate dielectric materials fabricated by sol-gel process, which can lead into not only the improved field-effect mobility but also the operation at low voltage range in OTFTs operation. Our gate dielectric layer consisted of two layers; one is the charge accumulation layer made with Tetraethyl orthosilicate (TEOS), (3-Glycidoxypropyl) trimethoxysilane (GLYMO), and titanium acetylacetone precursor, the other is the electron-trap blocking layer made with aqueous potassium hydroxide and SiO_X solution. The OTFTs with double-coated gate dielectric indicated high flexibility and transparency as well as superior performance. [16]

1.2 Reference

[1] Flexible Flat Panel Display Technology. G. P. Crawford, *Wiley-SID*, 2005, Ch 1.

[2] Particle display technologies become e-Paper. T. Z. Kosc, *Optics & Photonics News*, 2005, 18 p.

[3] I.-J. Chung, I. Kang, *Mol. Cryst. Liq. Cryst*, 2009, *507*, 1.

[4] S. J. Jo, C. S. Kim, M. J. Lee, J. B. Kim, S. Y. Ryu, J. H. Noh, K. Ihm, H. K. Baik, Y. S. Kim, *Adv. Mater.* 2008, *20*, 1146.

[5] V. C. Sunder, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willett, T. Someya, M. E. Gershenson, J. A. Rogers, *Sciene.* 2004, *303*, 1644.

[6] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, D. M. de Leeuw, *Nature*. 1999, *401*, 685.

[7] D. H. Kim, D. Y. Lee, H. S. Lee, W. H. Lee, Y. H. Kim, J. I. Han, K. Cho, *Adv. Mater.* 2007, *19*, 678.

[8] Introduction to Organic Electronic and Optoelectronic Materials and Devices. S.-S. Sun, L. R. Dalton, CRC Press, 2008, ch 10.

[9] H. S. Byun, Y.-X. Xu, C. K. Song, *Thin Solid Films*. 2005, *493*, 278.

[10] Y. Lu, W. H. Lee, W. S. Lee, Y. Jang, K. Cho, *Appl. Phys. Lett.* 2009, *94*, 113303.

[11] F. D. Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, *Appl. Phys. Lett*. 2005, *86*, 203505.

[12] X. Cheng, M. Caironi, Y.-Y. Noh, J. Wang, C. Newman, H. Yan, A. Facchetti, H. Sirringhaus, *Chem. Mater.* 2010, *22*, 1559.

[13] F.-C. Chen, C.-W. Chu, J. He, Y. Tang, *Appl. Phys. Lett*. 2004, *85*, 3295.

[14] A. Maliakal, H. Katz, P. M. Cotts, S. Subramoney, P. Mirau, *J. Am. Chem. Soc.* 2005, *127*, 14655.

[15] J. Kim, S. H. Lim, Y. S. Kim, *J. Am. Chem. Soc.* 2010, *132*, 14721.

[16] J. Kim, Y. S. Kim, *preparing*, 2013.

Chapter 2. Literature review

2.1 Organic thin film transistor

2.1.1 Thin film transistor architecture

OTFTs structure is composed of electrodes (gate, source and drain), dielectric, and semiconductor, which have to be appropriately located in device. The source and drain electrodes are contacted with the semiconductor while the gate electrode is separated with semiconductor due to gate dielectric.

As shown in Figure 2.1, the structures of OTFTs indicate four-case according to its operating mode and fabrication condition. Because organic semiconductor is very vulnerable to follow-up process, its deposition process is implemented after gate dielectric forming. The fabricated OTFTs show bottom-gate structure, which is depicted in two alternatives according to position of source and drain electrodes. Source and drain electrodes are either deposited before or after the semiconductor layer, which named bottom-contact and top-contact, respectively.

In case of the bottom-contact, the channel feature of source and drain electrodes can be patterned by microlithography process if gate dielectric is made from inorganic material such as silicon dioxide. While, in case of the top-contact, the channel length is dependent on pattern size of shadow mask with substantial loss resolution, contact resistance has reported to be lower in top-contact than bottom-contact.

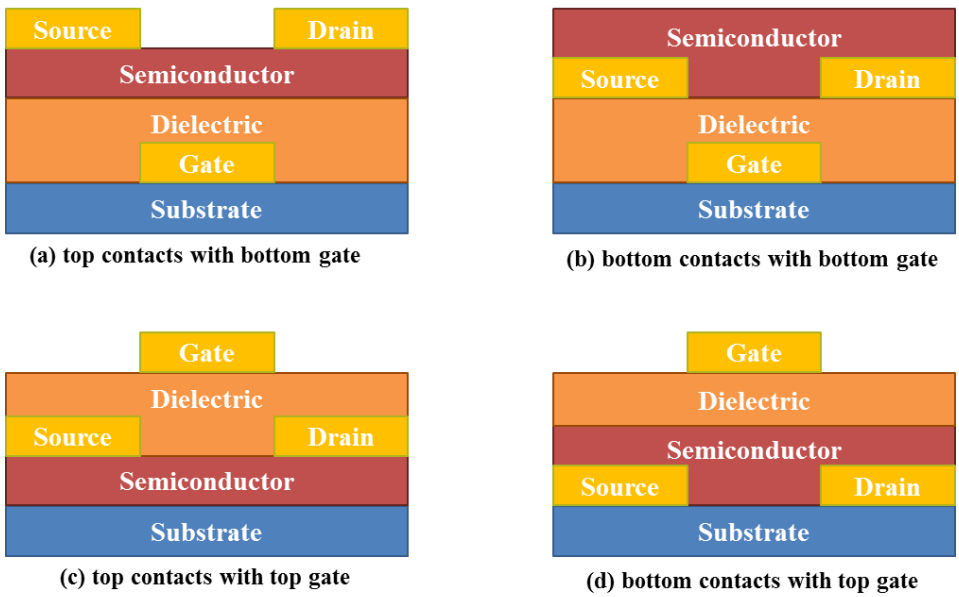


Figure 2.1 The schematic view of four architectures of OTFTs in cross-section (a) top contacts with bottom gate, (b) bottom contacts with bottom gate, (c) top contacts with top gate, and (d) bottom contacts with top gate.

2.1.2 Operating principle of OTFTs [1-3]

Operating mode of OTFTs is defined to n-type or p-type according to charge flow which is called by either electrons or holes in the OTFT conducting channel. The Fermi level of Au, as source and drain electrodes, is close to the highest molecular orbital (HOMO) level of organic semiconductor, such as pentacene, so there the barrier height is low. When conducting channel is formed at the interface of semiconductor-gate dielectric and drain voltage is pulsed, the holes, namely positive charges, injected from Au, source electrode, are easily accepted at the conducting channel of pentacene. The operating type of this OTFT is called to p-type because the positive charges, holes, is smoothly injected to conducting channel of semiconductor than negative charges, electrons.

On the other hand, the lowest molecular orbital (LUMO) level of pentacene is quite far away from the Fermi level of Au and the drain current can show very low leakage current at off state of OTFTs. This concept shows difference that the operation type of field-effect transistors is changed according to doping materials in conventional semiconductor.

Usually, when a voltage is applied to gate, an equal charge at semiconductor close to dielectric is generated as conducting channel.

As gate voltage is gradually increased, the positive carriers, holes, are mounted up at conducting channel of p-type OTFTs. Conductance of channel is increased according to drain voltage if gate voltage is enough to make conducting channel and constant. Also, as it is generated in proportional to gate voltage, the drain current is not increased despite drain voltage applied above that of conducting channel formation. At this point, it is called 'pinch off' and the channel current starts to be saturated irrespective of drain bias. This region is defined by the saturation region.

2.1.3 Analysis and parameter of OTFTs

The performance of OTFTs is estimated by using diverse parameters, such as field-effect mobility (m), on-off ratio, threshold voltage (V_T), and sub-threshold swing (SS). The characteristic, transfer and output curve as shown in Figure 2.2, of OTFTs is measured by current-voltage apparatus, which is employed at equation (2.2) to fine the parameters of OTFTs.

Generally, the operation of OTFTs is categorized to two regions by linear increase or saturation of drain current which indicate at $V_D << (V_G - V_T)$ and $V_D > (V_G - V_T)$, respectively. Each value of drain current is as followed:

$$\text{Linear region: } I_D = (W/L)\mu C\,(V_G - V_T - V_D/2)\,V_D \qquad (2.1)$$

$$\text{Saturation region: } I_D = (W/2L)\mu C\,(V_G - V_T)^2 \qquad (2.2)$$

Where I_D is the drain current, μ is the field-effect mobility, W is the channel width, L is the channel length, C is the capacitance per unit area of the dielectric layer, V_T is the threshold voltage, V_D is the drain voltage, and V_G is the gate voltage.

The field-effect mobility (μ) shows how charge carriers fast move in conducting channel depending on increasing drain current. It can be obtained through the tangential line extracted with $I_D^{1/2} - V_D$ curve. The slope value of tangential line is equal to $(W\mu C / 2L)^{1/2}$ induced from equation (2.2) and then the field-effect mobility can be easily elicited from $(W\mu C / 2L)^{1/2}$.

The on-off ratio is estimated by the differential of the highest drain current and lowest drain current when the bias was applied at gate electrode. It is the critical factor of transistors performances and indicates the quality as switching device. The on-off ratio is secured

from transfer curve by plotting the drain current (I_D) versus gate voltage (V_G).

Threshold voltage of transistor means the value of the gate−source voltage when the conducting channel just starts to connect the source and drain electrodes of the transistor, allowing significant current to flow. It can be obtained by extracting the transfer curve by plotting $I_D^{1/2}$ versus V_G in the saturation region, extrapolating to $I_D = 0$.

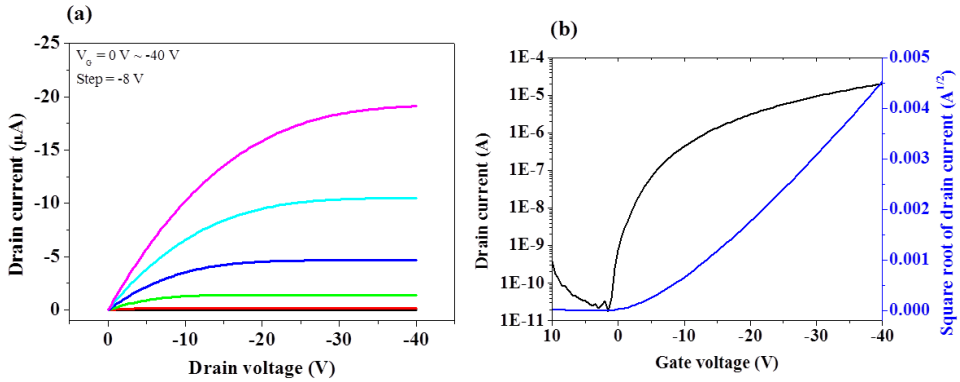


Figure 2.2 The output curve (a) and the transfer curve (b) of OTFTs.

2.2 Gate dielectrics

2.2.1 Introduction of gate dielectrics

In typical OTFTs, the dielectric layer is sited between the gate electrode and the organic semiconductor. This structure has two interfaces, which are important consideration as an appropriate dielectric material is selected. The gate electrode-gate dielectric interface must be considered of preventing static charge or dynamic charge injection into gate dielectric because they are the origin of adverse effects on threshold voltage (V_T) as a function of time. The gate dielectric-organic semiconductor interface is very important as well as the gate electrode-gate dielectric interface. The conducting channel is created at this interface. The property of conducting channel is determined by interface roughness, surface energy, and charges at this interface. [4] The organic semiconductor is grown and deposited on top of the gate dielectric, which can induce the arrangement of organic semiconductor molecules. The structure of arranged organic semiconductor molecules is really crucial factor about the performance of OTFT. [5] As a gate dielectric material is chosen for OTFT, the diverse requisites, such as interface, leakage, dielectric constant, processibility, stability, and reliability, must be controlled. The high dielectric constant is very vital, considering the

low field-effect mobility (typically, < 1 cm^2/Vs) of organic semiconductor as OTFT is operated. [6] The low leakage current is desirable to reduce the consumption of electrical power because the device can be worked at low gate bias voltage of $V_G = \pm 5$ V. [7] The simple process of dielectric has an advantage in profitability of commercial device. In this reason, the low-cost solution process for gate dielectric fabrication is valuable if it can be applied at printing method, such as ink-jet, gravure, or offset printing. [8] In addition, the stability and a minimum hysteresis of gate dielectric are essential requirements. Until now, to develop the desirable gate dielectric materials at OTFT, a number of researches have been studied. The many various dielectrics, such as inorganic, organic, and hybrid materials, have been searched for the goal, which is low leakage current and high dielectric constant.

2.2.2 The Type of gate dielectrics

2.2.2.1 Polymer dielectrics

The polymer dielectric shows superior flexibility suited at bendable device and can be fabricated by using low-cost solution process. Also, the polymer dielectric made by solution process is easily reproducible and indicates the useful surface to arrange the organic semiconductor.

The diverse polymer dielectrics, as shown in Figure 2.3, are complied with the value of Table 2.1. The polystyrene (PS) [9] and poly (methyl methacrylate) (PMMA) [10] as a gate dielectric were studied by researchers because they can easily be controlled. However, they indicate the low dielectric constant, which is not able to induce the good performance of OTFT. The poly (vinyl alcohol) (PVA) [6], Poly (acrylic acid) (PAA) [11] and poly (vinyl phenol) (PVP) [12] are well known as polymer dielectric for OTFT. They are cured by cross-linking system with assistance of using agent such as melamine-co-formaldehyde (PVP cross-linker) and ethylene glycol (PAA cross-linker). They show the excellent insulating property, which is caused from forming a dense thin film by the highly cross-linking of hydroxyl groups. The highly thin dielectric makes to increase capacitance value according to Eq (2.3)

$$C = (\varepsilon_0 k) A/d \qquad (2.3)$$

where C is the measured capacitance, A is the area of the capacitor, ε_0 is the permittivity of free space, k is the permittivity of dielectric material (dielectric constant), and d is the thickness of dielectric material, although the dielectric constant is pretty low. Also, the PVA

and PAA as water soluble polymers have the potential for being deposited onto an organic semiconductor to generate a top gate dielectric, because the water soluble polymers cannot dissolve the organic solvent based the semiconductor. [13] The divinyl-tetramethyl-disiloxane-bis(bensocyclobutene) (BCB precursor) [14] as a high capacitance material was applied at a gate dielectric of OTFT. This polymer is generated by the alkene unit in a $4\pi+2\pi$ Diels-Alder reaction to form the network polymer. The BCB polymer film as thin as 50 nm could show excellent breakdown voltage (> 3 MV/cm) and low leakage current (< 10^{-6} A/cm^2). The capacitance of BCB polymer thin film was measured to C = 47 nF/cm^2 despite the low dielectric constant (k = 2.65) owing to the highly thin BCB polymer layer.

In this reason, to overcome low dielectric constant of polymer dielectric and obtain high performance of OTFT, it must be fabricated as not only very thin film (< 100 nm) but also high uniform or amorphous property for low leakage current. Still, as thin polymer film was only used for gate dielectric, the limitations, such as high leakage current and low dielectric constant, exist. Therefore, inorganic materials indicating amorphous and high dielectric constant was suggested to control polymer demerits as a gate dielectric

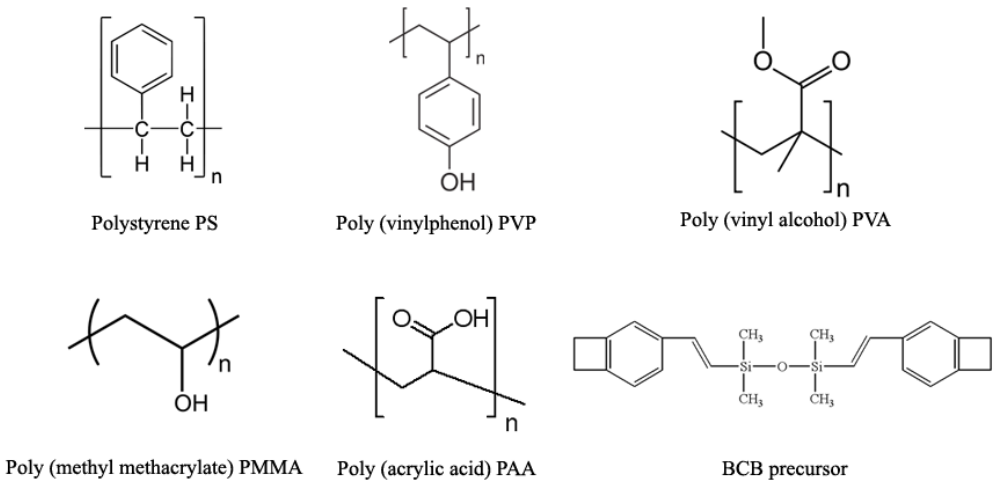


Figure 2.3 Polymers and polymer precursor used for as a gate dielectric in OTFTs.

Table 2.1 Dielectric properties for polymers.

Dielectric Materials	Dielectric constant	Minimum Thickness (nm)	Capacitance (C (nF/cm^2))	Leakage (A/cm^2)	Ref
PS	2.6	122	19	10^{-4}-10^{-7}	9
PMMA	3.5	160	19.5	-	10
PVA	10	500	17.8	-	6
PVP	6.4	450	7.4	10^{-7}	12
PAA	3.2	400	7	10^{-6}-10^{-9}	11
BCB	2.65	50	47	~10^{-5}	14

2.2.2.2 Inorganic dielectrics

Generally, in order to work transistors, the requirements of dielectric material are low interface state density, thermodynamic stability, and high breakdown voltage. The silicon dioxide is typical inorganic dielectric material in the transistors and presents superior insulating properties due to its wide band gap (8.9 eV). The SiO_2 dielectric exhibits the stable performance of transistors and is useful for initial evaluation of a number of new organic semiconductor materials. [15] Despite these merits of SiO_2 dielectric, it is difficult to apply in OTFTs because of its low dielectric constant (k = 3.9) and pretty brittle property.

So far, the many researchers have studied to improve the low dielectric constant of SiO_2 by using alternative material, high dielectric constant metal oxide. For example, as shown in Table 2.2, the TiO_2 (~80 depending on crystal structure) well known as high dielectric constant material can be employed to improve the performance of OTFTs. There was report of the enhancement of the field-effect mobility according to the dielectric constant increase. [16] Also, to obtain the low electrical power consumption, the high dielectric constant materials are surely essential element for flexible and mobile devices. However, the high dielectric constant material,

such as TiO_2, tends to form the leakage current path and is inappropriate as a dielectric. In order to complement the drawback of the high dielectric constant materials, the diverse efforts have been implemented. These methods are the nanocomposite of the metal oxide and polymer [17] and the layering of self-assembled monolayer (SAM) or polymer to prevent the leakage current [18].

Table 2.2 Dielectric properties for common inorganics. [1]

Dielectric materials	Dielectric constant	Minimum thickness (nm)	Capacitance (C (nF/cm^2))	Leakage current (A/cm^2)	Ref
SiO_2	3.9	300	0.01	10^{-7}	7
TiO_2	80	8-12	6-34	High	7
Al_2O_3	9	4.8	1.7	10^{-8}	7
Ta_2O_5	26	5-6	4-5	< 1	7

2.2.2.3 Polymer–Metal oxide composite dielectrics

A number of dielectric materials indicating high dielectric constant and flexible properties have been researched for advanced device.

These were researched for developing flexible high dielectric constant material, which is the dielectrics of nanocomposite type using PVP and TiO_2 nanoparticle. As shown in Figure 2.4, OTFT with the mixed PVP and TiO_2 nanoparticles as gate dielectric exhibits bottom–gate and top–contact of source and drain.

Although the nanocomposite, which is mixed with TiO_2 nanoparticles and PVP, dielectric was applied at OTFTs, the performance of the OTFTs was not improved and they were only worked at high voltage region V_G = −40 V. [19] Table 2.3 shows the performances of OTFTs according to diverse TiO_2 mixture ratio in PVP for gate dielectric. The more TiO_2 nanoparticles are increased in PVP, the more its capacitance is improved. Nevertheless, the field–effect mobility of OTFTs including PVP and TiO_2 nanocomposite gate dielectric was a little improved. The composite method mixing metal oxide nanoparticles and polymer precursor exhibits a fatal drawback, which is the adverse effect of organic semiconductor alignment due to rough dielectric surface.

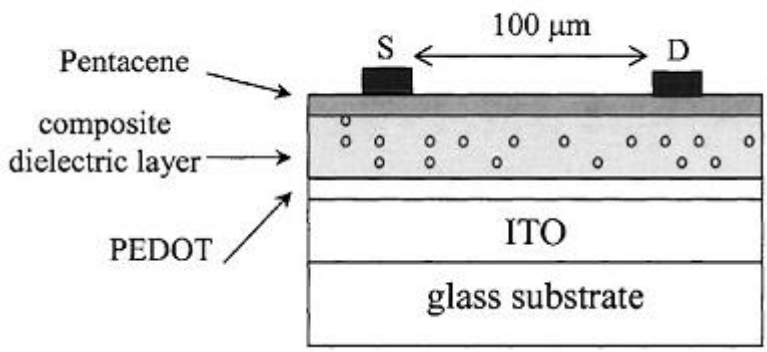


Figure 2.4 The device structure of the organic transistor. [19]

Table 2.3 Electrical parameters of the OTFTs including mixture of PVP and TiO_2 nanoparticles as a gate dielectric. [19]

Conc. of TiO_2 nanoparticles (wt%)	Thickness (nm)	Dielectric constant	Mobility (cm^2/Vs)	Threshold voltage (V)	On-off ratio
0 (w/o PEDOT)	600	3.5	0.23	-7.5	10^3
0	630	3.9	0.20	-7.8	10^4
3	700	4.4	0.25	-7.5	10^3
5	700	5.1	0.24	-7.2	10^3
7	700	5.4	0.24	-7.0	10^3

Maliakal et al. suggested the homogeneous nanocomposite dielectric material, which is fabricated by using polystyrene coated TiO_2 nanoparticles (TiO_2-PS), as shown in Figure 2.5(a). This method is able to make the uniform nanocomposite solution and obtain the smooth dielectric surface. [20] To measure the performance of OTFTs, the applied structure of OTFTs is bottom gate and top contact shown in Figure 2.5(b). Despite the forming smooth and uniform dielectric surface of TiO_2-PS, the performance of OTFTs including TiO_2-PS gate dielectric was narrowly improved (Figure 2.5(c)). The homogeneous TiO_2-PS gate dielectric is not interconnected thin film by cross-linking system. It means the high possibility of leakage current generation due to the grain boundaries between TiO_2-PS materials. Therefore the drain current can be decreased at low operating gate voltage because the thickness of the TiO_2-PS gate dielectric should be thickened to prevent leakage current. We propose two methods to achieve the flexibility of organic material and the high dielectric constant of metal oxide for new dielectric applied in next generation device.

First, as inducing the cross-linking of PVP and TiO_2 precursor (Figure 2.6), this nanocomposite of PVP and TiO_2 molecules is made from combining hydroxyl groups. It means that the dielectric shows

very smooth surface and can lead the perpendicular alignment of organic semiconductor, pentacene, on the dielectric surface. We suppose that the dense chemical structure of TiO_2-PVP composite (TPC) is caused by the alkoxy group of the PVP cross-linker, poly (melamine-*co*-formaldehyde) methylated/butylated, reacted with the hydroxyl group of the PVP and the ligands of the TiO_2 precursor. [21]

Second, the silicon-based inorganic-organic hybrid material, which has the flexibility due to the carbon chain of GLYMO, was used as a dielectric. The dielectric material was fabricated by sol-gel process, which goes through the hydrolysis and condensation reactions. Generally, the hydroxyl groups are created during the chemical reaction of sol-gel process and lead to hysteresis as adverse effect in switching device. Thus, in this study, the double-coated gate dielectric composed of inorganic-organic hybrid material and solution-based $SiOH_X$ was fabricated for the efficient working and minimized hysteresis of device.

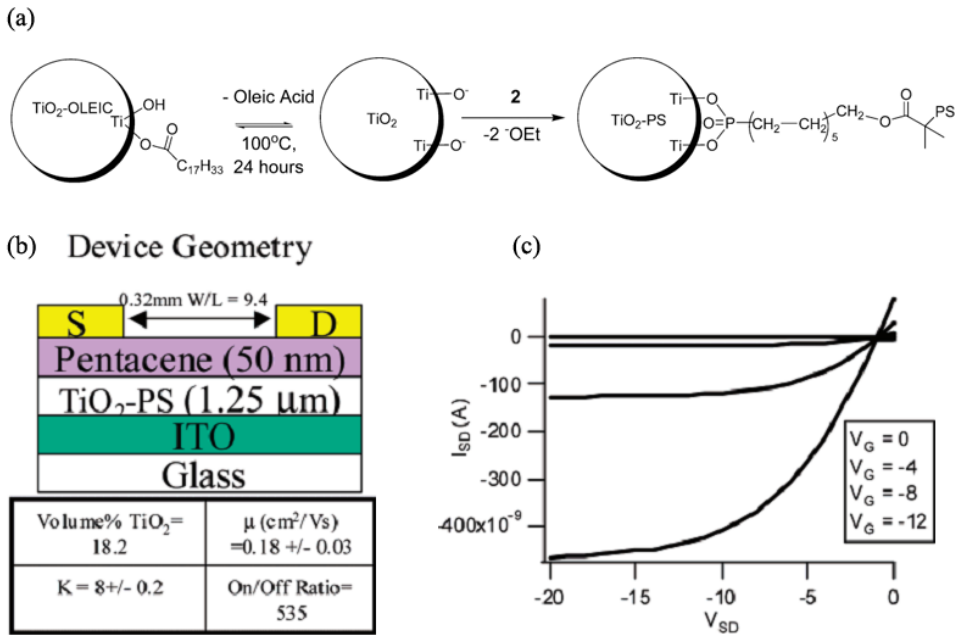


Figure 2.5 (a) Polystyrene Coated Titanium Dioxide (TiO_2–PS) (PMDETA = Pentamethyl diethylenetriamine) (b) Device geometry and (c) transistor characteristics for pentacene TFT using 20 mol% TiO_2–PS as gate dielectric. [20]

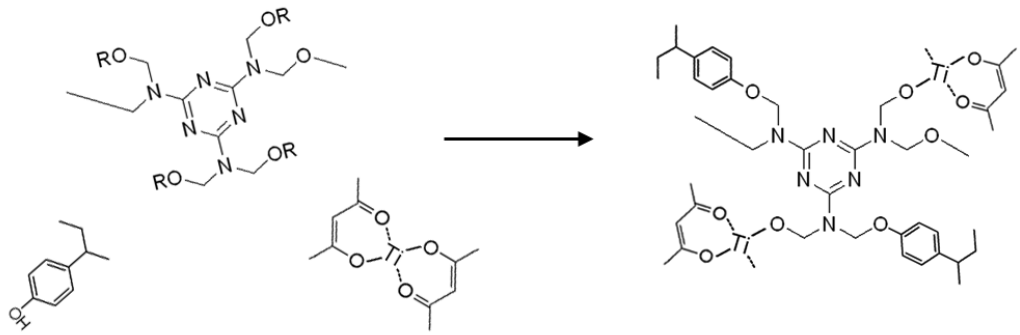


Figure 2.6 The cross-linking reaction of TPC dielectric including with PVP, TiO_2 precursor, and poly (melamine-co-formaldehyde). [21]

2.3 Sol-gel chemistry

2.3.1 Introduction of sol-gel chemistry

Sol-gel method is widely used synthetic technique in the preparation of bulk metal oxides (e.g., ceramic, glasses, films, and fibers). To make various metal oxide products, the appropriated procedure of sol-gel method is essential. They are categorized by aqueous sol-gel chemistry and nonaqueous sol-gel chemistry.

The aqueous sol-gel method is verified as the conversion of a precursor into inorganic solid through inorganic polymerization reactions triggered by water. Commonly, the metal salt (chloride, nitrate, sulfate) or metal organic compound (generally metal-oxygen-carbon bond), such as alkoxide, are used for the precursor or starting materials. A number of metal alkoxides, utilized in aqueous sol-gel method, can easily react with water and be used in commercial industry. Although aqueous sol-gel method has the merit, it has much less been researched due to the high reactivity of transition metal alkoxides.

The aqueous sol-gel chemistry is rather complicated due to the high reactivity of the metal oxide precursor for water. Also, the water as ligand and solvent has to be strictly controlled, such as hydrolysis and condensation rate of the metal oxide precursor (pH, temperature,

method of mixing, rate of oxidation, the nature and concentration of anions) to give good reproducibility of the synthesis protocol. [22]

The nonaqueous sol–gel chemistry is expressed by non–hydrolytic method. Generally, organic solvent under exclusion of water is used in the nonaqueous sol–gel method, which can overcome some of the major limitations of aqueous sol–gel systems. [23] This reaction system leads the powerful and versatile alternative because the organic components contribute to the diverse roles (e.g., solvent, organic ligand of precursor molecule, surfactants, or *in situ* formed organic condensation products). They work as oxygen–supplier for the oxide formation and powerfully affect the particle size and shape as well as the surface properties owing to their coordination nature. In addition, the oxygen carbon shows the moderate reactivity and leads to slower reaction rates.

2.3.2 Reaction mechanism [24]

Generally, the sol–gel method is composed of the preparation of a homogeneous solution, conversion of the homogenous solution into a sol, aging, shaping and hardening (or sintering) as shown in Figure 2.7. [25] These products are fabricated by sol–gel reaction, which can be defined as hydrolysis and condensation reaction (Scheme

2.1).The hydrolysis induce a dispersion of colloidal particles in the liquid, followed by condensation results in a gel, which is rigidly interconnected between particles and develops porous inorganic networking. [26]

During the hydrolysis reaction, –OR groups of metal oxide precursor is substituted with –OH groups by nucleophilic attack of the oxygen atom of water under release of alcohol and the generation of metal hydroxide. Condensation reaction arises between hydroxylated metal ingredients induce M–O–M bonds and oxolation (release of water), whereas the reaction between a hydroxide and alkoxide induce M–O–M bonds and alkoxolation (release of an alcohol).

The sol–gel reaction is very tricky and fast to control the reaction rate because a several factors, such as electronegativity of the metal atom, its ability to increase the coordination number, steric hindrance of the alkoxy group, and on the molecular structure of the metal alkoxides (monomeric or oligomeric), influence on it exhibit. In this reason, the complex multi metal oxides fabricated by sol–gel method are prone to lose control its composition and homogeneity. To overcome these problems, as mentioned above, the answer is to slow the reaction rate by forming chelating ligands in metal precursor and modify the reactivity of the precursor. [22]

Although the sol-gel method is difficult to control the reaction rate and the uniformity of products, it has the merit of obtaining the products of diverse shape [27, 28] and the application possibility in various fields, such as the sensor device [29], magnetic resonance imaging of biomedical [30], and dyesensitized solar cell [31].

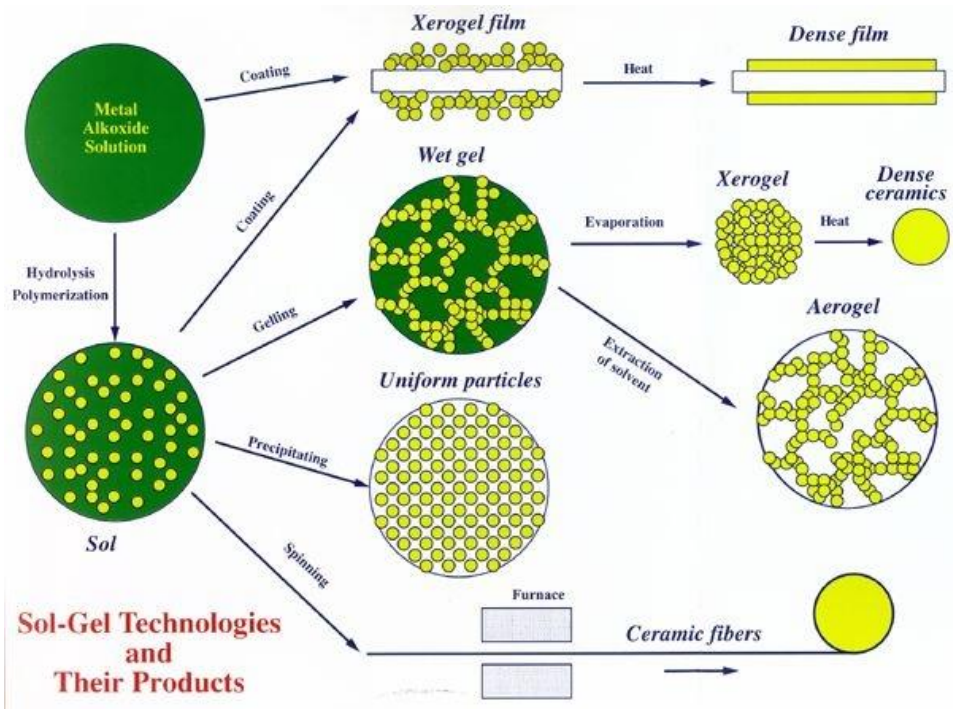


Figure 2.7 Steps in the sol–gel method to control the final morphology of the product. [25]

$$\equiv M-OR + H_2O \longrightarrow \equiv M-OH + ROH \quad (2.4)$$

$$\equiv M-OR + HO-M\equiv \longrightarrow \equiv M-O-M\equiv + H_2O \quad (2.5)$$

$$\equiv M-OR + HO-M\equiv \longrightarrow \equiv M-O-M\equiv + ROH \quad (2.6)$$

Scheme 2.1 Main reactions in the sol-gel process using metal alkoxide. Hydrolysis (Eq. 2.4) and condensation, including oxolation (Eq. 2.5) and alkoxolation (Eq. 2.6). [24]

In this study, we fabricated the thin film for the appropriate gate dielectric to OTFTs by using sol-gel method. The thin film composed of tetraethyl orthosilicate (TEOS), (3-Glycidoxypropyl) trimethoxysilane (GLYMO), and titanium acetylacetone precursor was built up of the networking of metal organic compound (metal-oxygen-carbon bond) via sol-gel reaction.

While TEOS and GLYMO become hydrated by water, titanium (IV) butoxide is formed to complex with acetylacetonate anion. Both oxygen atoms of acetylacetone bind to the metal to form a six-membered chelate ring. This titanium acetylacetone complex can easily be networked with other precursors, such as polymer or metal based precursor, by cross-linking between –OH groups of precursors.

Therefore, the three metal precursors, TEOS, GLYMO, and titanium acetylacetone complex, can be fabricated as gate dielectric by forming metal organic compound (metal-oxygen-carbon bond) thin film.

2.3.3 Requirement for the gate dielectric of OTFTs fabricated by sol-gel process

There are some essential factors as materials are made for gate dielectric to employ at OTFTs. The gate dielectric in OTFTs must be able to induce enough conducting channel of semiconductor at settled gate bias voltage and obstruct the leakage current flowing from source electrode to gate electrode. To induce sufficient conducting channel of semiconductor at low gate bias voltage (V_G < ±5 V), the high dielectric constant material is imperative for gate dielectric of OTFTs. In addition, the gate dielectric maintaining low leakage current or off-state current can quickly lead to the saturation of drain current even at low drain voltage. To keep low leakage current of gate dielectric, films have to show amorphous and dense property and exhibits no pores or cracks.

Because of requirements for the gate dielectric of OTFTs, diverse methods and materials have been suggested to apply at device. The solution process, such as sol-gel method, is used for gate dielectric fabrication as simple and low cost manufacturing. The compatible materials for gate dielectric commonly are known as metal oxide, which is SiO_2, Al_2O_3, Y_2O_3, or HfO_2. Generally, the metal oxides fabricated via solution process, are inclined to crystalize at low

process temperature, generating grain boundaries that contribute to reinforcing impurity inter-diffusion and high leakage currents. [32]

There are important to note that metal oxides with high dielectric constant show small band gaps, and binary oxides with low dielectric constant indicate wide band gaps. As metal oxide is employed at gate dielectric, wide band gap-binary oxide is desirable due to breakdown field scale with the magnitude of the band gap. Furthermore, the gate dielectric has to get flexible and transparent property for the next generation device, for example smart window [33], patchable display [34], and e-paper [35].

For preparing flexibility of gate dielectric, polymer materials are ordinarily used by solution process but need high operating voltage of OTFTs due to their low dielectric constant. In this reason, to make balance between the advantages of metal oxide and polymer, metal precursor fabricated by sol-gel process must have affinity with polymer solution. The hydrated metal oxide precursor by hydrolysis of sol-gel reaction can fully linked with hydroxyl groups in polymer. And then, the superior flexibility and improved dielectric constant shows in metal oxide and polymer compound thin film, which is suited for gate dielectric of OTFTs.

In alternative method for gate dielectric material fabrication, it can be made from metal oxide precursors by using sol-gel process. The metal oxide thin film is built via hydrolysis and condensation of sol-gel reaction, and then its rigid chemical structure can easily be cracked by external stress. To remove this demerit, a metal oxide precursor including carbon chains is added in the metal oxide precursor solution. [36] The flexible metal oxide thin film can be applied at gate dielectric of OTFTs, indicating higher dielectric constant in comparison with polymer.

2.4. Reference

[1] Z. Bao, J. Locklin, in: *Organic Field-Effect Transistors*, 1st ed. CRC, Boca Raton FL 2007.

[2] C.-A. Di, Y. Liu, G. Yu, D. Zhu, *Accounts of Chemical Research* 2009, *42*, 1573.

[3] C.-K. Song, *Polymer Science and Technology* 2003, *14*, 22.

[4] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, *Chem. Mater.* 2004, *16*, 4543.

[5] R. Schroeder, L. A. Majewski, M. Grell, *Adv. Mater.* 2005, *17*, 1795.

[6] A. Facchetti, M.-H. Yoon, T. J. Marks, *Adv. Mater.* 2005, *17*, 1705.

[7] G. D. Wilk, R. M. Wallace, J. M. Anthony, *J. Appl. Phys.* 2001, *89*, 5243.

[8] H. Klauk, Organic electronics: materials, Manufacturing and Applications. *WILEY-VCH*, 2006.

[9] M.-H. Yoon, H. Yan, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc.* 2005, *127*, 10388.

[10] C. D. Dimitrakopoulos, B. K. Furman, T. Graham, S. Hegde, S. Purushothaman, *Synth. Met.* 1998, *92*, 47.

[11] S. H. Lim, J. Kim, Y. S. Kim, *Chem. Commun*. 2010, *46*, 3961.

[12] J. Lee, D. K. Hwang, J.-M. Choi, K. Lee, J. H. Kim, S, Im, J. H. Park, E. Kim, *Appl. Phys. Lett.* 2005, *87*, 023504.

[13] R. Parashkov, E. Becker, G. Ginev, T. Riedl, H.-H. Johannes, W. Kowalsky, *J. Appl. Phys.* 2004, *95*, 1594.

[14] L.-L. Chua, P. K. H. Ho, H. Sirringhaus, R. H. Friend, *Appl. Phys. Lett.* 2004, *84*, 3400.

[15] S. R. Forrest, *Nature.* 2004, *428*, 911.

[16] Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, K. Cho, *Appl. Phys. Lett.* 2005, *87*, 152105.

[17] A. Maliakal, H. Katz, P. M. Cotts, S. Subramoney, P. Mirau, *J. Am. Chem. Soc.* 2005, *127*, 14655.

[18] L. A. Majewski, R. Schroeder, M. Grell, *Adv. Mater.* 2005, *17*, 192.

[19] F.-C. Chen, C.-W. Chu, J. He, Y. Yang, *Appl. Phys. Lett.* 2004, *85*, 3295.

[20] M. J. Panzer, C. D. Frisbie, *J. Am. Chem. Soc.* 2005, *127*, 6960.

[21] J. Kim, S. H. Lim, Y. S. Kim, *J. Am. Chem. Soc.* 2010, *132*, 14721.

[22] J. Livage, M. Henry, C. Sanchez, *Prog. Solid State Chem.* 1988, *18*, 259.

[23] D. Pinna, M. Niederberger, *Angew. Chem. Int. Ed.* 2008, *47*, 5292.

[24] C. J. Brinker, G. W. Scherer, *Sol-Gel Science.* Academic press, Inc, 1990.

[25] M. Niederberger, N. Pinna, in: Metal Oxide Nanoparticles in Organic Solvents, Springer-Verlag London Limited 2009.

[26] R. C. Mehrotra, A. Singh, *Prog. Inorg. Chem.* 1997, *46*, 239.

[27] I. Djerdj, D. Sheptyakov, F. Gozzo, D. Arcon, R. Nesper, M. Niederberger, *J. Am. Chem. Soc.* 2008, *130*, 11364.

[28] X. Zhong, R. Xie, L. Sun, I. Lieberwirth, W. Knoll, *J. Phys. Chem. B.* 2006, *110*, 2.

[29] M. Cao, I. Djerdj, M. Antonietti, M. Niederberger, *Chem. Mater.* 2007, *19*, 5830.

[30] Y. W. Jun, J. S. Lee, J. Cheon, *Angew. Chem. Int. Ed.* 2008, *47*, 5122.

[31] Q. Zhang, T. Chou, B. Russo, S. Jenekhe, G. Cao, *Angew. Chem. Int. Ed.* 2008, *47*, 2402.

[32] J. Robertson, *Rep. Prog. Phys.* 2006, *69*, 327.

[33] G. P. Crawford, *John Wiley & Sons, Ltd.* 2005.

[34] J. Park, J. Kim, S. Lee, J. Bang, B. J. Kim, Y. S. Kim, J. Cho, *J. Mater. Chem.* 2009, *19*, 4488.

[35] T. Z. Kosc, *Optics & Photonics News.* 2005,18.

[36] J. Kim, M. Kim, M. J. Lee, J. S. Lee, K. Shin, Y. S. Kim, *Adv. Mater.* 2009, *21*, 4050.

Chapter 3. Experimental procedure

3.1 Experimental apparatus

3.1.1 Organic molecular beam deposition system

Organic Molecular beam deposition (OMBD) system is used for the formation of pentacene thin film, as shown in Figure 3.1. An effusion cell is situated at the left edge of the chamber. A p.i.d controlled as power supplier is connected via electrically insulating feedthrough to the effusion cell. A diffusion pump is used to empty the OMBD system to a based pressure of 3×10^{-6} Torr. The low vacuum pressure, 760 Torr ~ 10^{-3} Torr, was tracked by using a thermocouple gauge and the high vacuum pressure, 10^{-3} ~ 10^{-6}, was watched by using an ion gauge. The increasing thickness of pentacene film is in-situ identified by a quart crystal monitor located near the substrate holder. The aiming deposition rate was accurately controlled in range of 0.4 Å/s ~ 0.5 Å/s.

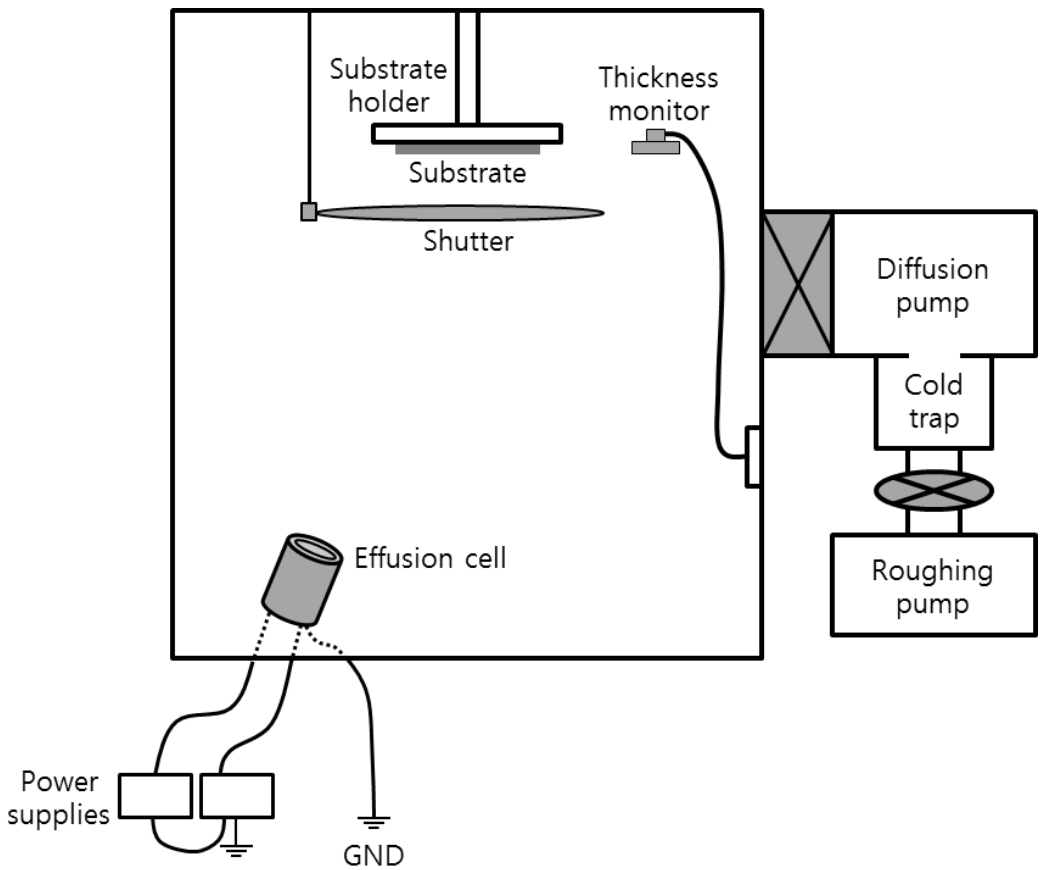


Figure 3.1 Schematic illustration of organic molecular beam deposition system.

3.1.2 Thermal evaporation system

Figure 3.2 shows thermal evaporation system, which is employed for the deposition of a metal, such as Au thin film. A tungsten boat, which is linked at an ac power supplier, is sited at the center of the chamber. The deposition rate of the metal is controlled by current flow to the tungsten boat from an ac power supplier. The low vacuum pressure, 760 torr ~ 10^{-3}, was tracked by using a thermocouple gauge and the high vacuum pressure, 10^{-3} ~ 10^{-6}, was watched by using an ion gauge. The increasing thickness of Au thin film is in-situ identified by a quart crystal monitor located near the substrate holder. The aiming deposition rate was accurately controlled in range of 4 Å/s ~ 5 Å/s.

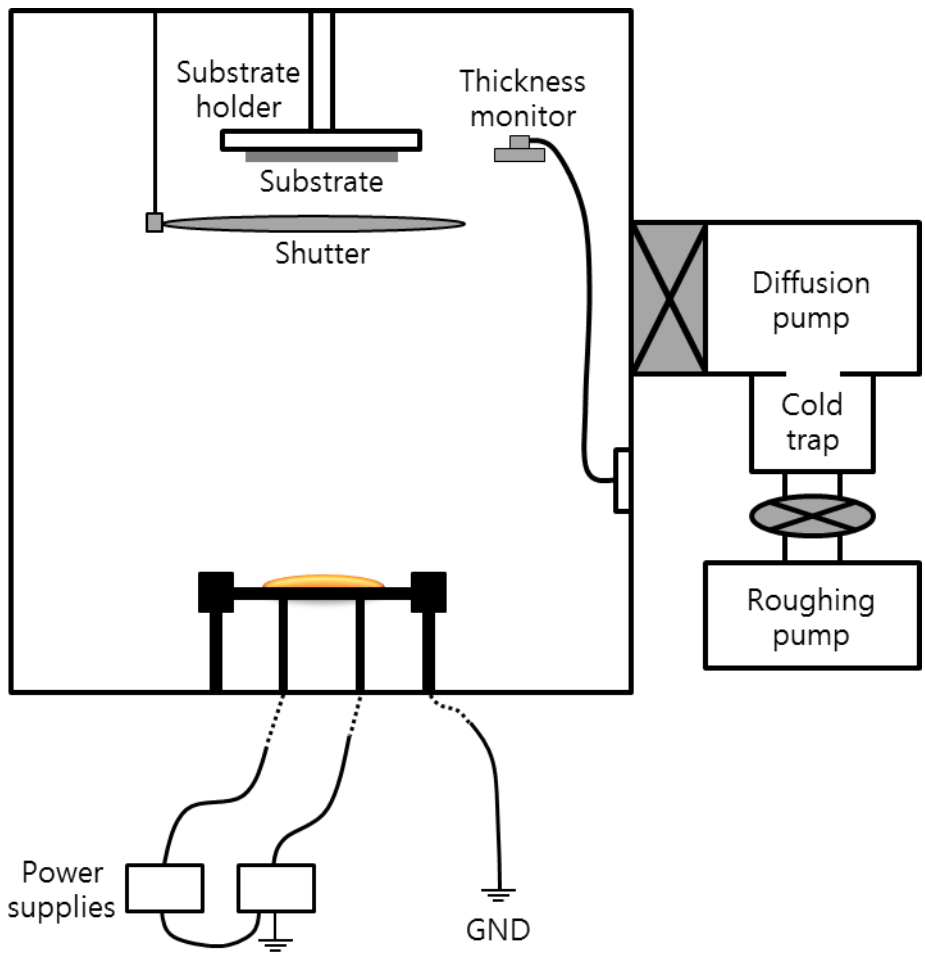


Figure 3.2 Schematic illustration of thermal evaporation system.

3.2 Characterization methods

3.2.1 Current-voltage (I-V) measurement

The current-voltage curves of OTFTs were measured by using an Agilent 4155B semiconductor parameter analyzer (MS TECH, Korea). The measurement environment was under ambient in a dark shield box.

3.2.2 Capacitance-voltage measurement

The capacitance-voltage curves of MIM (metal-insulator-metal) structure were carried out under air environment using as Agilent 4284A 1 KHz precision LCR meter.

3.2.3 Atomic force microscope (AFM)

All electrical measurements were taken in dark ambient conditions. An atomic force microscope (XE-100, PSIA) was used to investigate the surface morphology.

3.2.4 Scanning electron microscope (SEM)

The thickness of all the double-coated gate fielectric was measured by using a field emission scanning electron microscope (FE-SEM) (Hitachi S-4800).

3.2.5 X-ray diffraction (XRD)

X-ray diffraction (XRD) was measured to verify the amorphous property of metalorganic materials used as charge-accumulation inducing layer.

3.2.6 Contact angle and surface energy measurement

The contact angles were measured by using a Phoenix 150 surface angle analyzer (Surface Electro Optics, Korea) and analyzed with Image XP 5.9 software. A droplet of deionized water and diiodomethane were dropped on the surface, right after the images were captured by a CCD camera.

3.2.7 Thickness profiler (K-MAC, ST2000-DLXn)

To estimate the thickness of the TiO_2-PVP composite thin film, Thickness profiler (K-MAC, ST2000-DLXn) was measured by the difference of reflectance between thin films.

3.2.8 Bending tester (Z-tec)

The bending tester (Z-tec) was conducted to investigate the flexibility of the double-coated gate dielectric and OTFTs including it.

3.3. Reference

[1] J. Kim, M. Kim, M. J. Lee, J. S. Lee, K. Shin, Y. S. Kim, *Adv. Mater.* 2009, *21*, 4050.

[2] J. Kim, S. H. Lim, Y. S. Kim, *J. Am. Chem. Soc.* 2010, *132*, 14721.

[3] S. Y. Chung, S. Kim, J.-H. Lee, K. Kim, S.-W. Kim, C.-Y. Kang, S.-J. Yoon, Y. S. Kim, *Adv. Mater.* 2012, *24*, 6022.

Chapter 4. Solution-based TiO_2-PVP composite gate insulator for low operating voltage of OTFTs

4.1 Introduction

Organic thin film transistors (OTFTs), which are appropriate for flexible and lightweight devices compared with traditional inorganic electronics, have considerable potential for printable electronics. [1] Also, OTFT-based electronics are very attractive because they are simple and cost efficient with a high throughput of solution processing and the printing method. However, there are several challenges regarding OTFTs, such as a high operating voltage induced by the low charge carrier mobility of organic semiconductors and the low dielectric property of the organic gate dielectric. [2] The low operating voltage is essential for various OTFTs applications, such as portable displays, [3] smart cards, [4] and radio frequency identification tags. [5] Furthermore, patchable electronics [6] such as smart patches [7] and smart textiles [8] must be operated at low voltages because they are worn on the human body. To be worked at low voltage, OTFTs must have an organic insulator with a high dielectric constant. In previous research, various polymer dielectric materials, such as poly (4-vinyl phenol) (PVP), [9] poly

(methylmethacrylate) (PMMA), [10] poly (styrene) (PS), [11] poly (perfluorobutenylvinylether) (CYTOP), [12] and poly (acrylic acid) (PAA) [13] have been studied by many research groups. However, polymer materials are not appropriate for use in low voltage applications due to their low dielectric constant (k). In order to overcome this problem, various nanocomposite dielectrics, including inorganic nanoparticles with a high dielectric constant (k), have been studied. [14−16] However, nanocomposite dielectrics in OTFTs have not been shown to have a surface that allows well−aligned organic semiconductor growth, resulting in a low on/off ratio and low carrier mobility in the low voltage range. Furthermore, according to the increase of inorganic particles in nanocomposite materials, the dielectric layer shows high leakage currents because high k materials can generate a high leakage current path. [17]

In OTFTs, the surface of the dielectric layer is important for effective performance because it allows for a conducting channel in the interface between the dielectric layer and semiconductors. In the case of deposition of small semiconductor molecules, such as pentacene, molecular orientation and grain morphology depend strongly on the surface roughness and energy of the underlying film. The low surface energy of the dielectric layer allows the vertical

growth of pentacene molecules. As the hole can easily be moved in the vertical direction of pentacene molecules, these vertical alignments of pentacene enhance mobility in OTFTs. [18] In order to decrease the high surface energy of the dielectric–semiconductor interface, the nanocomposite dielectric layer has been deposited by the polymer capping on inorganic materials. However, in this case, the transistors were not operated successfully in a low voltage range due to insufficient dielectric properties caused by polymer capping.

In chapter 4, we have introduced the TiO_2–PVP composite (TPC) gate insulator to overcome the problems discussed above. The TPC is composed of a TiO_2 precursor (titanium (IV) butoxide and acetyl acetone) and poly (4–vinylphenol) (PVP) solution (PVP, poly (melamine–*co*–formaldehyde) methylated/butylated and propylene glycol methyl ether acetate (PGMEA) solvent). As this TPC can simply be deposited by a simple solution process and exhibits a considerably low surface energy, it generates a smooth and hydrophobic surface that allows the uniform vertically oriented growth of small semiconductor molecules and closely packed grains between crystal domains. Also, the TiO_2 precursor induces an enhanced dielectric constant compared with it of pristine PVP. As this enhanced dielectric property leads to the increased drain current at a

low operating voltage, the OTFTs including this TPC gate insulator can successfully be operated at a low operating gate bias voltage. Furthermore, this homogeneous TiO_2–PVP composite solution is stable in ambient conditions, and it was readily applied in the fabrication of OTFTs. As a result, the OTFTs with a TPC exhibited the better transistor performance with an increased on/off ratio, increased mobility, and low subthreshold voltage at a gate bias voltage of V_G = −3 V in comparison with the performance of OTFTs that include a pristine PVP dielectric.

4.2 Results and discussions

4.2.1 Synthesis of the PVP solution (5 wt%), TiO_2 precursor and PVP composite solution

In order to synthesize the TiO_2 precursor and PVP (M_W = 25,000, Sigma–Aldrich) composite solution, PVP, poly (melamine–*co*–formaldehyde) methylated/butylated (M_n = 637, Aldrich), and propylene glycol methyl ether acetate (PGMEA) (M_W = 132.16, Fluka) were mixed in a weight ratio of 2 : 1 : 37. The cross–linked PVP solution was stirred for 24h at room temperature. The TiO_2 precursor was mixed from titanium (IV) butoxide (M_W = 340.32, Sigma–Aldrich) and acetyl acetone (M_W = 100.12, Fluka), at a molar ratio of 1:1. The

cross-linked PVP solution and TiO_2 precursor, at a ratio of 9:1 (w/w), were mixed by stirring until they formed a gelatin. In order to avoid the aggregation of PVP solution and TiO_2 precursor due to rapid cross link, the solution was stirred under low temperature (2 ℃). The gelatin was dissolved in ethanol (M_W = 46.07, DAE JUNG) at a ratio of 1:3 (w/w).

4.2.2 The Fabrication of OTFTs

The transistors were fabricated on ITO substrates (thickness: 120 nm, sheet resistance: 15 W/□). The ITO substrates were subjected to 10 min washes in trichloroethylene, acetone, and isopropyl alcohol, and then rinsed with distilled water before being dried with nitrogen. The TiO_2 precursor and PVP composite (TPC) solution was deposited on an ITO substrate as a bottom gate using spin casting at 3,500 rpm for 40 sec. The whole was then heated at 200 ℃ for 1 h. The TFTs device was designed as a top-contact electrode structure, as shown in Figure 4.1. The pentacene, the TFTs semiconductor was deposited by thermal evaporation in ~ 3×10^{-6} Torr (500 Å, 0.5 Å/s). The source and drain electrodes, Au, were deposited through a shadow

mask with a channel length (L) and width (W) of 100 μm and 1,000 μm, respectively, in ~ 3×10^{-6} Torr (1000 Å, 5 Å/s).

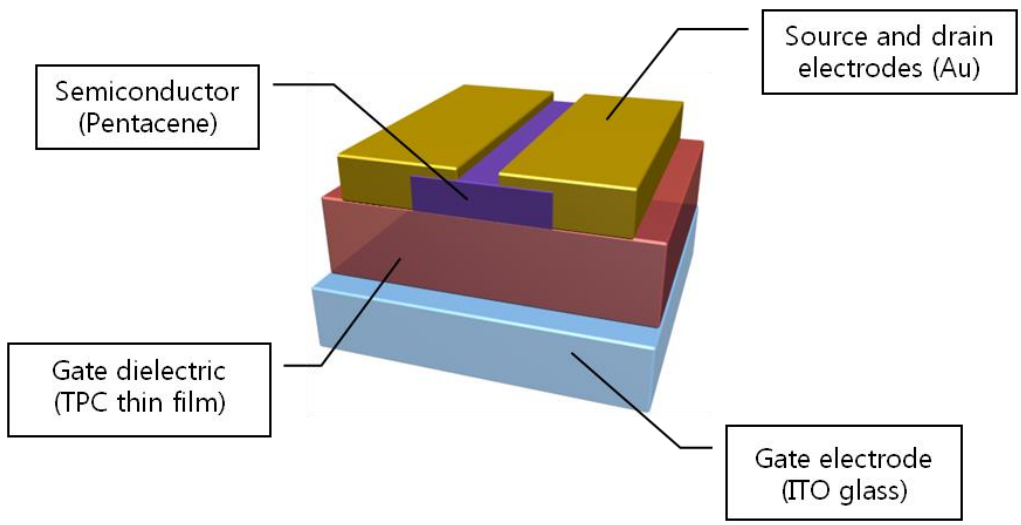


Figure 4.1 The organic transistor structure with TiO_2–PVP composite (TPC) thin film as a gate dielectric.

4.2.3 Solubility of TiO_2–PVP composite

The TiO_2 precursor and PVP composite solution showed reddish–orange color. A few minutes after being completely mixed, the TiO_2 precursor solution and the PVP solution for the TPC gate insulator turned into gelatin as a result of the cross–linking reaction of poly (melamine–*co*–formaldehyde) methylated/butylated (cross–linker) and the TiO_2 precursor. This gelatin was observed by the naked eye and was transparent with reddish–orange. Solvents, including hydroxyl group, can dissolve the gelatin resulting from the cross–linkable PVP solution and the TiO_2 precursor solution in order to make a homogeneous solution phase with low viscosity. We conducted dissolving tests for various solvents and the results are summarized in Figure 4.2. The TPC gelatin can be dissolved the ethanol and 2–propanol including hydroxyl group, as shown in Table 4.1, and was converted into homogeneous solution phase.

We used ethanol to transform the TPC gelatin to the transparent solution phase. As we introduced a complete solution phase composite including inorganic precursor that can be easily used in the spin–coating process, their surface properties show the extremely low surface roughness.

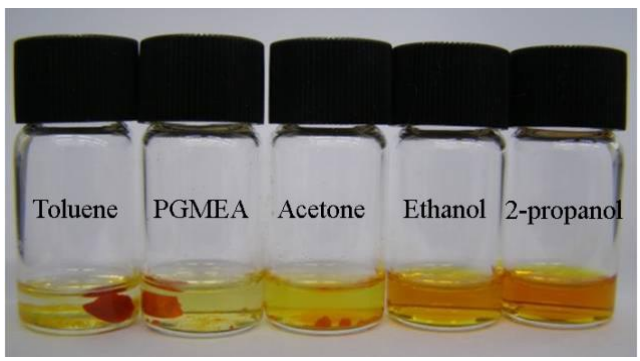
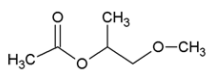
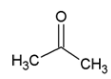
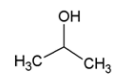
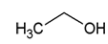


Figure 4.2 The solubility of TiO_2-PVP composite (TPC) gelatins according to diverse solvents.

Table 4.1 The chemical structures of solvents shown in Figure 4.1.

Materials without hydroxyl group			Materials with hydroxyl group	
				
Toluene	PGMEA	Acetone	2-propanol	Ethanol

4.2.4 Electrical characteristics of OTFTs

The leakage currents of TPC and PVP thin film as a gate insulator were measured by using current-voltage measurements, as shown in Figure 4.3(a). The leakage current value of the TPC gate insulator at ±5 V was ~ 10^{-7} A/cm^2, which is same as that of the pristine PVP gate insulator. The gate leakage currents of the TPC gate insulator were very low due to the dense chemical structure of TPC induced by cross-linking between poly (melamine-*co*-formaldehyde) methylated/butylated and titanium (IV) butoxide chemically reacted with acetyl acetone. We presume the alkoxyl group of the PVP cross-linker, poly (melamine-*co*-formaldehyde) methylated/butylated, reacted with the hydroxyl group of the PVP and the ligands of the TiO_2 precursor and that this chemical cross linking generated the dense structure. Although inorganic TiO_2 induces high leakage currents, [17] this TPC that include a TiO_2 precursor indicated a considerable low leakage current compared to the pristine PVP polymer due to the dense chemical structure generated from cross-linking of hydroxyl groups. Otherwise, the capacitance of the TPC thin film is higher than the pristine PVP because of the high *k* property of TiO_2 composited with PVP. Figure 4.3(b) shows the capacitance of the TPC and pristine PVP dielectric.

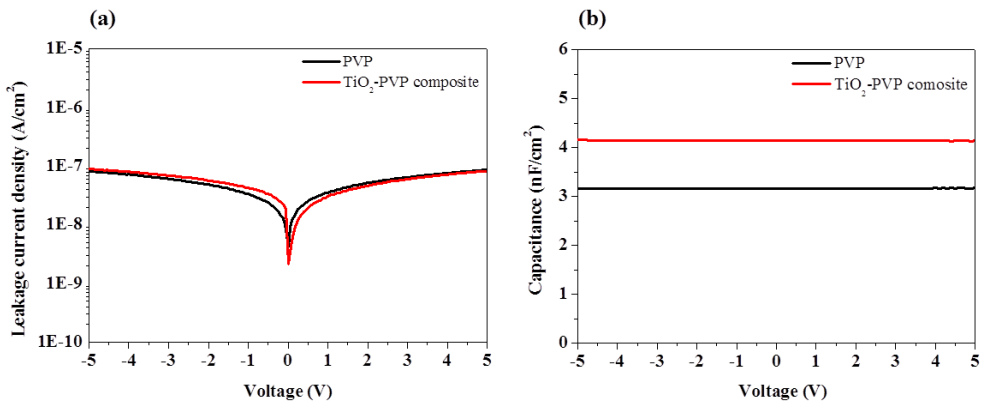


Figure 4.3 (a) The leakage current density and (b) the capacitance of the cross-linked PVP and TiO_2-PVP composite (TPC) dielectric. (MIM structure = Metal-Insulator-Metal, Operating voltage: ±5 V)

The performance of the transistor including the TPC and pristine PVP thin film as a gate insulator are indicated in Figure 4.4 at gate bias voltage V_G = −3 V. Although the dielectric constant (k = 5.2) of the TPC thin film is not a remarkably high value, this TPC gate insulator sufficiently improves the output drain current of OTFTs in a low−voltage range.

In order to compare the performance of OTFTs including PVP and TPC gate insulator, several parameters expressed in Table 4.2 were analyzed from the transfer curves of them. Especially, while the on/off ratio (Figure 4.4(b)) of the OTFTs with the PVP as a gate insulator was calculated to ~10^1, the TPC improved the device with it to ~10^3 as shown in Figure 4.4(d). In addition, the obtained field−effect mobility of OTFTs with a TPC gate insulator was 0.105 cm^2/Vs, while the field−effect mobility of OTFTs with a pristine PVP gate insulator was 0.036 cm^2/Vs.

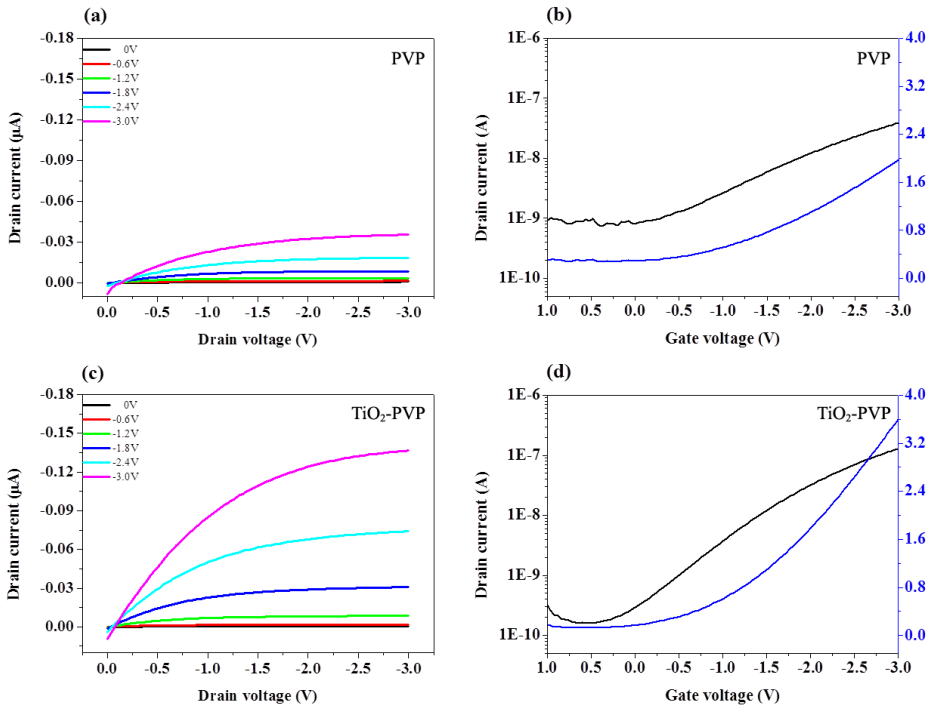


Figure 4.4 (a) Output and (b) transfer characteristics of OTFTs with pristine PVP thin film as a gate insulator. (c) Output and (d) transfer characteristics of OTFTs with TiO_2–PVP composite (TPC) thin film as a gate insulator. (channel length, 100 μm; channel width, 1,000 μm; source–drain bias voltage, −3 V)

Generally, field-effect mobility is dependent on the capacitance of the gate insulator as well as is affected by pentacene molecule alignment or morphology. In previous papers [17], field-effect mobility of OTFTs has improved as a result of changing the surface energy of the dielectric using surface treatments with self-assembled monolayer such as octadecyltrichlorosilane (OTS). The structures of TPC surface enhance the field-effect mobility of OTFTs as well as the vertical alignment of pentacene molecules induced by low surface energy.

Figure 4.5 displays the pentacene morphology according to the surface property of PVP and TPC dielectric. Figures 4.5(a) and (b) show the contact angles of PVP and TPC surfaces: the surface energy of the TPC composite layer was lower than that of the pristine PVP. The low surface energy of the TPC induced the vertical alignment and dense packing of pentacene, resulting in better performance of OTFTs. Figures 4.5(c) and (d) show the roughness of pristine PVP and TPC surface morphology and Figures 4.5(e) and (f) show the pentacene morphology deposited onto the pristine PVP and TPC surfaces, measured using atomic forced microscopy (AFM). The pentacene morphology on the pristine PVP surface exhibited a larger grain size and a broader void (black color) than those on the TPC

surface. The OTFTs including a PVP gate insulator indicated the lower mobility than TPC OTFTs. That was caused by the obstructed electron flow in the semiconductor channel due to voids and sparse packing in the pentacene morphology on PVP surface. The pentacene morphology on the TPC surface (Figure 4.5(f)) showed small, densely packed grains.

Also, it is well known that OTFTs with dielectrics that include inorganic nanoparticles have sometimes exhibited electrical instabilities, such as hysteresis, due to interface defects of nanoparticles. [19] In this research, as the TPC was cross-linked completely with both the TiO_2 precursor and PVP polymer, there was little hysteresis as shown in Figure 4.6. The performance of OTFTs with TPC gate insulator improved compared to that of OTFTs with a pristine PVP gate insulator, as a summarized in Table 4.2.

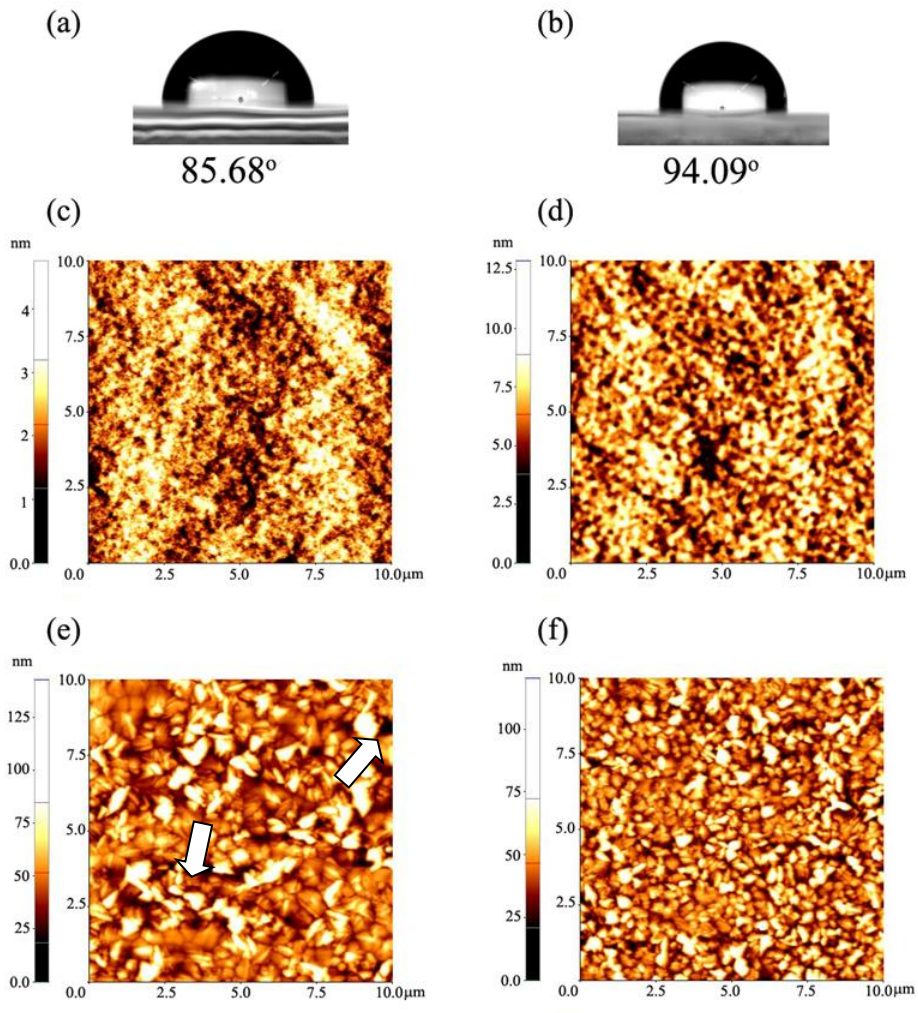


Figure 4.5 The contact angles of (a) pristine PVP and (b) TiO_2–PVP composite (TPC) surface. AFM images of (c) the pristine PVP (roughness rms: 0.514 nm) and (d) TPC surface (roughness rms: 1.303 nm) as a dielectric layer, (e) and (f) pentacene morphology onto the pristine PVP and TPC surface, respectively.

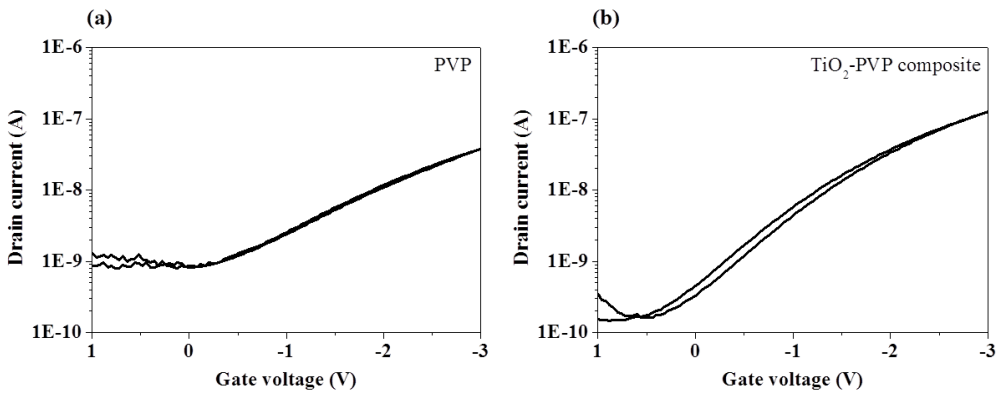


Figure 4.6 The hysteresis of OTFTs with (a) pristine PVP and (b) TiO_2–PVP composite (TPC) gate insulator.

Table 4.2 The electrical properties of cross-linked pristine PVP and TiO_2-PVP composite (TPC) film as a gate insulator, respectively (Operating voltage: -3V).

Dielectric materials	Mobility (cm^2/Vs)	Threshold Voltage (V_T)	On/off ratio	Subthreshold Swing (V/decade)	Thickness (nm)	Dielectric Constant
PVP	0.036	-0.5	5.2×10^1	1.65	110	3.9
TPC	0.105	-0.8	$\sim 10^3$	0.98	110	5.2

4.3 Conclusion

We introduced a composite polymer gate insulator (TPC) that included high *k* TiO_2 for OTFTs operated at low gate bias voltage. The dielectric properties of TPC, which is composed of PVP, a cross-linker, and a TiO_2 precursor, were enhanced due to the dense chemical structure of the polymer (PVP) and high *k* materials (TiO_2 precursor). This TPC gate insulator can simply be used in solution processes, such as spin casting and showed good stability in ambient conditions, air environments and moisture conditions. The TPC thin film as a gate insulator could sufficiently hinder leakage currents and successfully operate in low-voltage conditions, such as −3 V. Furthermore, the TPC gate insulator exhibited enhanced performance characteristics of OTFTs, such as on/off ratio, mobility, and subthreshold swing, compared with the pristine PVP gate insulator. Although this device shows low field-effect mobility because of intrinsic organic semiconductor limitation, it operated well at a low gate bias voltage with the considerable and remarkable performance. We conclude that the TPC, namely TiO_2-PVP composite, is quite promising as a gate insulator in advanced flexible OTFTs.

4.4 Reference

[1] S. R. Forrest, *Nature*. 2004, *428*, 911.

[2] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, *Science*. 2000, *290*, 2123.

[3] C. D. Sheraw, J. West, *et. al*, *Appl. Phys. Lett.* 2002, *80*, 1088.

[4] W. Fix, A. Ullmann, J. Ficker, W. Clemens, *Appl. Phys. Lett.* 2002, *81*, 1735.

[5] P. F. Baude, S. D. Theiss, *et. al*, *Appl. Phys. Lett.* 2003, *82*, 3964.

[6] J. Park, J. Kim, S. Lee, J. Bang, B. J. Kim, Y. S. Kim, J. Cho, *J. Mater. Chem.* 2009, *19*, 4488.

[7] T. Someya, T. Sakurai, *et. al*, *PNAS.* 2005, *102*, 12321.

[8] M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci, A. Bonfiglio, *Appl. Phys. Lett.* 2006, *89*, 143515.

[9] H. S. Byun, Y.-X. Xu, C. K. Song, *Thin Solid Films*. 2005, *493*, 278.

[10] F. D. Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, *Appl. Phys. Lett*. 2005, *86*, 203505.

[11] M.-H. Yoon, H. Yan, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc*. 2005, *127*, 10388.

[12] T. Umeda, D. Kumaki, S. Tokito, *Org. Electro*. 2008, *9*, 545.

[13] S. H. Lim, J. Kim, S.-g. Lee, Y. S. Kim, Chem. Comm. 2010, *46*, 3961.

[14] F.-C. Chen, C.-W. Chu, J. He, Y. Yang, J.-L. Lin, *Appl. Phys. Lett.* 2004, *85*, 3295.

[15] A. Maliakal, H. Katz, P. M. Cotts, S. Subramoney, P. Mirau, *J. Am. Chem. Soc.* 2005, *127*, 14655.

[16] C. Jung, A. Maliakal, A. Sidorenko, T. Siegrist, *Appl. Phys. Lett.* 2007, *90*, 062111.

[17] C.-H. Kim, J.-H. Bae, S.-D. Lee, J. S. Choi, *Mol. Cryst. Liq. Cryst*. 2007, *471*, 147.

[18] Y. D. Park, J. A. Lim, H. S. Lee, K. Cho, *Materialstoday*. 2007, *10*, 46.

[19] H. Faber, M. Burkhardt, A. Jedaa, D. Kalblein, H. Klauk, M. Halik, *Adv. Mater*. 2009, *21*, 3099.

Chapter 5. Double-coated gate dielectric for high performance OTFTs

5.1 Introduction

Organic thin film transistors (OTFTs) as the essential component of various next generation devices, such as flexible mobile display [1], e-paper [2] and smart card, have been acutely researched. [3] In the fabricating of OTFTs, the two essential components are the semiconductor and the gate insulator. In the past two decades, a lot of studies have been done to promote the performance of suitable organic semiconducting materials for flexible OTFTs such as pentacene [4], rubrene [5], poly(3-hexylthiophene) (P3HT) [6], 6, 13-(Bis(triisopropylsilyethynyl) (TIPS) pentacene [7]. On the other hand, the seeking for flexible and superior dielectric materials was not satisfactory in comparison with the researches of organic semiconductors. Because the electrical performance of OTFTs as the switching component for flexible electronics depends on the properties of both semiconductor and dielectric materials, the OTFTs including the poor gate insulating material, which has low dielectric constant and poor stability, have shown the inferior efficiency irrespective of the semiconductor intrinsic performance. To improve

the working of OTFTs, the high efficient semiconductor and gate insulator is essential and decisive factor.

As the polymer gate insulators exhibit considerable merits for flexible device owing to their excellent bendability, many research groups have investigated on various polymers as gate dielectric materials, which are the poly (4-vinyl phenol) (PVP) [8], poly (methylmethacrylate) (PMMA) [9], and poly (perfluorobutenylvinylether) (CYTOP) [10]. In spite of their useful characteristics, they in common suffer from a low field-effect mobility and high operating voltage due to the poor dielectric property of polymers. [11] For expanding the potential of OTFTs to advanced devices, besides the high field-effect mobility, the operation at low gate bias voltage (< ±5 V) is essential.

By contrast to polymer gate insulators, generally, the metal oxide dielectric materials have high dielectric constant and good electrical stability but show the rigid property and limited flexibility. [12] Also, their manufacturing methods need a high cost deposition process due to cumbersome vacuum equipment while the organic dielectric materials are fabricated by a simple and cost-effective solution process. For the above reasons, the various novel processes, such as the soluble inorganic-organic nanocomposite method [13, 14] and

sol-gel process [15], have been reported with the object of obtaining the sufficient flexibility, high dielectric constant and durability as gate dielectric materials. However, in simple inorganic-organic nanocomposite method, they have not shown the sufficient high performance in the pentacene based-OTFTs, because the intrinsic inferior dielectric constant of organic matrix determines dominantly the total capacitance of composite material. Otherwise, the metal oxide gate insulators fabricated by sol-gel process showed a high dielectric constant but they easily lost the flexibility due to their innate rigid property. Also, they suffer from the considerable hysteresis, which is caused by residual unreacted function sited such as –OH groups. In our previous report, to break through the limitations of metal oxide-nanoparticles and polymer mixture, the titanium oxide-poly (4-vinylphenol) composite (TPC) dielectric induced by intermolecular binding was developed for the pentacene based-OTFTs with low gate bias voltage V_G = –3 V. [16] However, the OTFTs including TPC gate insulator still showed a relatively low field-effect mobility and device stability.

Herein, to remedy the diverse drawbacks related with composite dielectric materials, we newly suggest the flexible inorganic-organic hybrid gate insulator materials fabricated by sol-gel process, which

can lead into not only the improved field-effect mobility but also the operation at low gate bias voltage in the pentacene based-OTFTs. This gate insulator was composed with two layers; one is the charge-accumulation inducing layer made with Tetraethyl orthosilicate (TEOS), (3-Glycidoxypropyl) trimethoxysilane (GLYMO), and titanium acetylacetone precursor, the other is the electron-trap blocking layer made with aqueous potassium hydroxide and SiO_X solution. These double-coated gate insulators successfully showed the capability of the solution process at the low temperature annealing as maximum as 175 ℃ and the operation of the pentacene based-OTFTs at the low gate bias voltage (V_G = -5 V). Also, they indicated the improved dielectric constant with ~ 5.2 and induced the good field-effect mobility with 2.59 cm^2/Vs at V_G = -20 V and 1.08 cm^2/Vs at V_G = -5 V in the pentacene based-OTFTs. Furthermore, the hysteresis originated from -OH groups could be successfully decreased, because the electron-trap blocking layer effectively prohibits the space-charge electret induced by the electrons which was injected from a gate electrode during the operation of pentacene based-OTFTs. To observe flexibility of the double-coated gate insulator, we conducted the bending test of its thin film and pentacene

based-OTFTs up to enduring maximum curvature of bending distance 5 mm.

5.2 Results and discussions

5.2.1 Fabrication of the aqueous potassium cation-SiO_X solution from solid silicon

The 1.12 g of potassium hydroxide (KOH) (Samchun chemicals) was diluted with the 10 mL of distilled water. After the potassium hydroxide was completely dissolved in distilled water, silicon pieces (Aldrich) was added in the aqueous KOH solution at molar ratio of 5:2 and this solution was maintained until form the condition of $SiOH_X$ gelation. The completely dissolved silicon in aqueous potassium hydroxide was diluted in distilled water at ratio of 1:1 (w/w) for deposition process.

5.2.2 Synthesis of the metalorganic compounds solution by sol-gel process

The metalorganic compounds, SiO_X and SiO_X-TiO_X, for charge-accumulation inducing layer are composed of three solutions. For solution one, 10 mmole of tetraethyl orthosilicate (TEOS) (Aldrich) was mixed with 40 mmole ethanol and 1 mmole hydrochloric acid in

40 mmole of distilled water, and then the solution was stirred for 60 min. For solution two, 10 mmole of (3-glycidoxypropyl) trimethoxysilane (GLYMO) (Aldrich) was mixed with 50 mmole of ethanol and 50 mmole, and the solution was stirred for 60 min. For solution three, 10 mmole of titanium tetrabutoxide (Aldrich) was added to 2, 4-pentanedione (Fluka, Milwaukee, WI, USA) at molar ratio of 1:2 and this solution was blended until it exhibits homogeneous yellow color.

The metalorganic compound SiO_X was made from solution one and two in the weight ratio of 7:3 before it is stirred for 25 hours at room temperature. Methyl isobuthylketone (MIBK) (Aldrich) as a solvent was added to the metalorganic compound SiO_X solution, at a ratio of 1:3 (w/w). In case of the metalorganic compound SiO_X-TiO_X solution, it was composed with solution one, two, and three at a ratio of 6:3:1 (w/w/w). This mixture was stirred and diluted with solvent MIBK in the same way as the metalorganic compound SiO_X solution.

5.2.3 The pentacene based-OTFTs fabrication

The transistors were fabricated on ITO/PET substrates (thickness: 120 nm, sheet resistance: ~ 15 KΩ/□) and designed as the bottom gate and top contact source and drain electrodes, as shown in Figure

5.1. The potassium cation−SiO_X (~ 220 nm), as the electrons−trap blocking layer, was deposited on ITO/PET substrates by using spin casting at 4,000 rpm for 40 sec after the ultra−violet ozone (UVO) treatment for 20 min (λ: 254 nm, Power: 100 mW/cm^2). The potassium cation−SiO_X was annealed at 150 ℃ for an hour in vacuum oven. In the next step, metalorganic compound layer formed by sol−gel process (~ 460 nm), as an charge accumulation layer, were deposited on pre−coated potassium cation−SiO_X layer in the spin casting way at 4,000 rpm for 40 sec. The thickness of double−coated gate insulator was measured by using field emission scanning electron microscope (FE−SEM) and indicates about 680 nm (Figure 5.2). These films were treated by heating at 175 ℃ for an hour in vacuum oven. The pentacene as a semiconductor was deposited through a shadow mask with rectangle shape (length: 1500 μm, breadth: 500 μm) by thermal evaporation at 3×10^{-6} Torr (thickness: 500 Å, rate: 0.4 Å/s). The source and drain electrodes, Au, were deposited through a shadow mask with a channel length (L) and width (W) of 150 μm and 1,000 μm, respectively, at 3×10^{-6} Torr (thickness: 700 Å, rate: 4 Å/s).

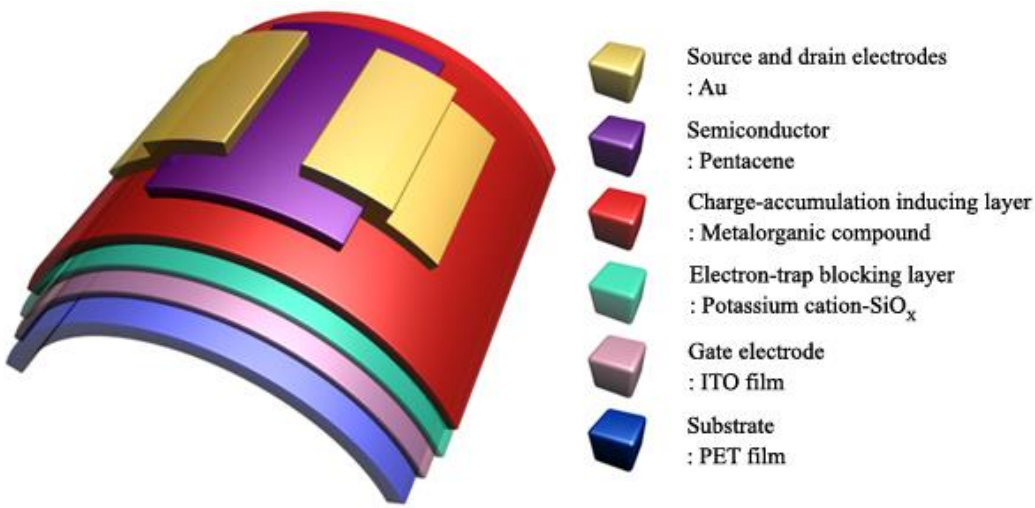


Figure 5.1 The structure of bendable the pentacene based-OTFT: bottom gate and top contact.

5.2.4 Electrical characteristics of OTFTs

The solution-processed double-coated gate insulator was composed with two layers as shown in the SEM images (a, b) of Figure 5.2. One is the electron-trap blocking layer for obstructing the penetration of electrons from a gate electrode and the other is charge-accumulation inducing layer for leading the conducting channel of a semiconductor in a pentacene based-OTFTs. In a precursor for the electron-trap blocking layer, the Si wafer slices were resolved in the aqueous potassium hydroxide (KOH) solution, which were made with the $SiOH_X$ gel by sol-gel reaction with silicon cation, Si^{4+}, and hydroxide ion, OH^-, as well as K^+ from the potassium hydroxide. The electron-trap blocking layer, which can be expressed with the potassium cation-SiO_X, was spin-coated on ITO film and then annealed at 150 ℃ for an hour. The charge-accumulation inducing layer, composed of SiO_X, TiO_X, and GLYMO, is formed as metalorganic compound having direct metal-oxygen-carbon linkages after spin-coated on the electron-trap blocking layer and then annealed at 175 ℃ for an hour.

To estimate the electrical properties of the double-coated gate insulator, such as leakage current density and capacitance, the measurement of current-voltage (I-V) and capacitance-voltage (C-

V) were performed on metal-insulator-metal (MIM, M = ITO, Au) structure. Figure 5.2(c) shows the stable leakage current density, < 10^{-6} A/cm^2, regardless of adding TiO_X in charge-accumulation inducing layer. The leakage current of inorganic based-gate insulator commonly arise by grain boundary of its polycrystalline or low band gap of high dielectric constant materials for example TiO_2. [17] This charge-accumulation inducing layer observed by X-ray diffraction (XRD) indicated amorphous and no grain boundary because the SiO_X, TiO_X, and GLYMO were made to network structure via condensation reaction in molecular level. Figure 5.3 exhibits that $2q$ Peaks of around 70° shown in metalorganic compounds are in agreement with crystalline Si peak from JCPDS(17-901). Any peak assumed as crystalline of metalorganic compounds was not observed. Therefore, the metalorganic compounds SiO_X and SiO_X-TiO_X fabricated by sol-gel process are extremely amorphous phase.

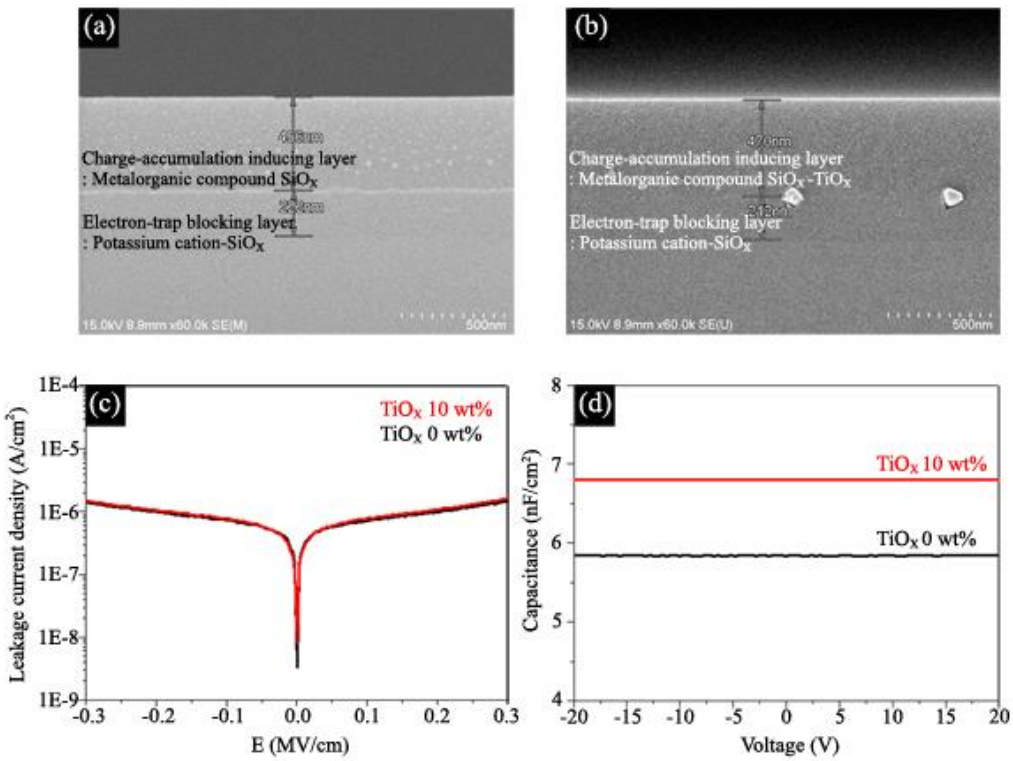


Figure 5.2 The cross-section SEM images of double-coated gate insulator stacked in the charge-accumulation inducing layer SiO_X (a) and SiO_X-TiO_X (b) on the electron-trap blocking layer. Leakage current density (c) and capacitance (at 100 kHz) (d) of the double-coated gate insulator composed of charge-accumulation inducing layer and electron-trap blocking layer.

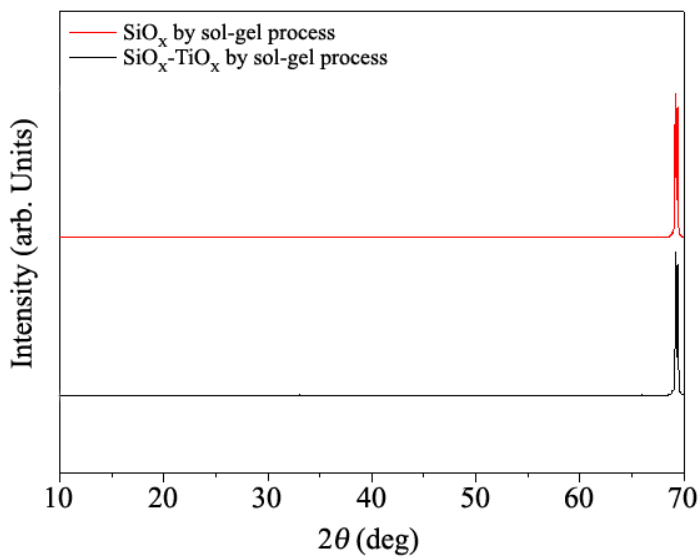


Figure 5.3 XRD data of metalorganic compounds SiO_X and SiO_X-TiO_X thin film.

Whereas, considering the capacitance of the double-coated gate insulator (Figure 5.2(d)), the capacitance of the gate insulator added with TiO_X 10 wt% was somewhat increased to 6.8 in comparison to it (5.8) without TiO_X.

Usually, a higher capacitance of gate insulator would allow greater charge inducing in the semiconductor layer of an OTFT in a given gate bias voltage, thus granting the possibility of operation at low gate bias voltage. [18] For this reason, the increased capacitance of the double-coated gate insulator can trigger the conducting channel of a semiconductor at the low gate bias voltage (< V_G = ±5 V). Therefore, this double-coated gate insulator could be engineered for low gate bias voltage (V_G = -5 V) as well as high gate bias voltage (V_G = -20 V) in accordance with TiO_X whether or not.

In order to demonstrate the performance of the solution-processed double-coated gate insulator, we fabricated the pentacene based-OTFTs with the bottom gate and top contact structure in Figure 5.1. Moreover, the electron-trap blocking layer in the double-coated gate insulator was removed to verify its feature obstructing the electrons injected from gate electrode to the charge-accumulation inducing layer. The thin film excluding the electron-trap blocking layer is expressed by the single-coated gate insulator. The pentacene

based-OTFTs with the single-coated gate insulator and the double-coated gate insulator were respectively estimated by current-voltage ($I-V$) measurement to obtain the device performance.

The performance of the pentacene based-OTFTs with the single-coated gate insulator (the charge-accumulation inducing layer SiO_X) and the double-coated gate insulator, which consisted of charge-accumulation inducing layer SiO_X and electron-trap blocking layer, were indicated in Figure 5.4. The two devices were measured at gate bias voltage V_G = -20 V. The pentacene based-OTFTs including the single-coated gate insulator showed the field-effect mobility of 0.86 cm^2/Vs via extracting square root of drain current-gate voltage curve in the saturation region of Figure 5.4(a). Meanwhile, the pentacene based-OTFTs with the double-coated gate insulator indicated the increased field-effect mobility, 2.59 cm^2/Vs, in the saturation region of transfer characteristic (Figure 5.4(b)). It means that the electron-trap blocking layer located on the gate electrode prevents electrons penetrated from gate electrode to charge-accumulation inducing layer. As the electron-trap blocking layer was excluded in the gate insulator, the electrons are trapped at -OH groups of charge-accumulation inducing layer. The trapped electrons disturb the forming of dipoles in charge-accumulation inducing layer, and it is

followed by the reducing of conducting channel generation in a semiconductor and low drain current.

The turn-on voltage shift could also be changed from ΔV_{on} = 4.50 V to ΔV_{on} = 1.75 V by inserting the electron-trap blocking layer between the charge-accumulation inducing layer and the gate electrode. The turn-on voltage shift is defined by hysteresis, which works for fatal drawback in a switching device. The electron-trap blocking layer in the double-coated gate insulator acts on hysteresis minimizing by preventing the electrons penetrating from gate electrode to gate insulator. Additionally, in the pentacene based-OTFTs, the surface property of gate insulator helps the alignment of a pentacene, which is directly related with the field-effect mobility of the pentacene based-OTFTs. [19] The upper layer of the double-coated gate insulator is the charge-accumulation inducing layer, which is regarded as leading the perpendicular alignment of a pentacene on this surface. The enhanced performance owing to well aligned pentacene molecules will concretely discuss in the section 5.2.7. The double-coated gate insulator is regarded as leading to the better performance of the pentacene based-OTFTs because each of its two layers contributes to property improvement of the device.

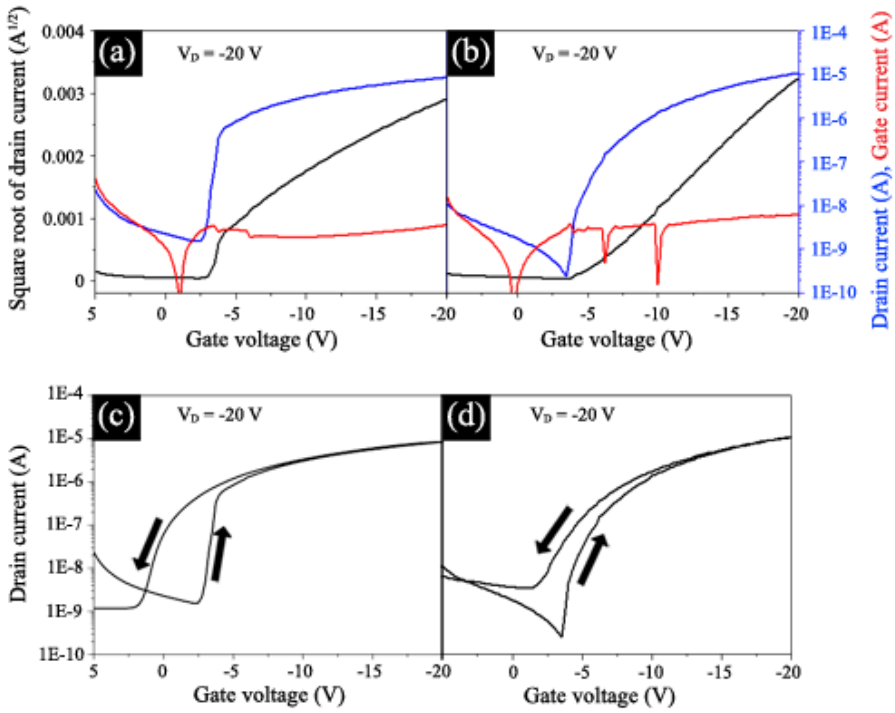


Figure 5.4 Transfer characteristics of the pentacene based-OTFT including the single-coated gate insulator (a) and the double-coated gate insulator (b) measured in ambient at V_G = -20 V. Hysteresis characteristics of the pentacene based-OTFT including the single-coated gate insulator (c) and the double-coated gate insulator (d) measured in ambient at V_G = -20 V.

5.2.5 Hysteresis generation: Bulk trap vs. Interfacial trap

Generally, hysteresis resulted from the charge trapping, which means that the charge carriers of semiconductor flowing in conducting channel are trapped at –OH groups of the top surface of gate insulator, at the interface between semiconductor and gate insulator. [20] Also, hysteresis can be developed by electrons injected from gate electrode because unreacted –OH groups inside the bulk of gate insulator make electrons trapping centers developing charge electrets. [21]

In our study, the high hysteresis is the feature indicated in the pentacene based-OTFTs including the charge-accumulation inducing layer as the single-coated gate insulator fabricated by sol-gel process. To investigate the root of the hysteresis, a pristine SiO_2 (100 nm) was situated underneath the charge-accumulation inducing layer and PαMS (20 nm) was deposited on the charge-accumulation inducing layer like the inset images of Figure 5.5. If the origin of the hysteresis was related to charge trapping at the interface between semiconductor and gate insulator, the pentacene based-OTFT including the bilayer gate insulator shown in the inset image of Figure 5.5(a) would not display the turn-on voltage shift of ΔV_{on} = 10 V, hysteresis, because PαMS [22] well known as insulating material

would prohibit the interaction of charge carrier and –OH groups on top of a gate insulator. On the contrary, in case of the charge-accumulation inducing layer on the pristine SiO_2, the turn-on voltage shift disappeared completely in the transfer characteristic of Figure 5.5(b). It exhibits no hysteresis of the device as the pristine SiO_2 prohibits that the electrons injected from gate electrode are trapped at the charge-accumulation inducing layer. Therefore, the hysteresis root of the pentacene based-OTFTs with the charge-accumulation inducing layer is manifested in electrons trapped inside the bulk of gate insulator not charge trapping at the interface between semiconductor and gate insulator.

To apply the simple solution-processible electron-trap blocking layer like as the pristine SiO_2 in the pentacene based-OTFTs, we adopted the solution based silicon oxide layer between the charge-accumulation inducing layer and the gate electrode. The electron-trap blocking layer was fabricated by silicon pieces dissolved in KOH solution and named as potassium cation-SiO_X. The hysteresis, turn-on voltage shift ΔV_{on}, described in Figure 5.4(c) was decreased from ΔV_{on} = 4.5 V to ΔV_{on} = 1.75 V (Figure 5.4(d)) by inserting the electron-trap blocking layer between the charge-accumulation inducing layer and the gate electrode. This means that the electron-

trap blocking layer prohibits the trap of electrons injected from gate electrode to the bulk of the gate insulator.

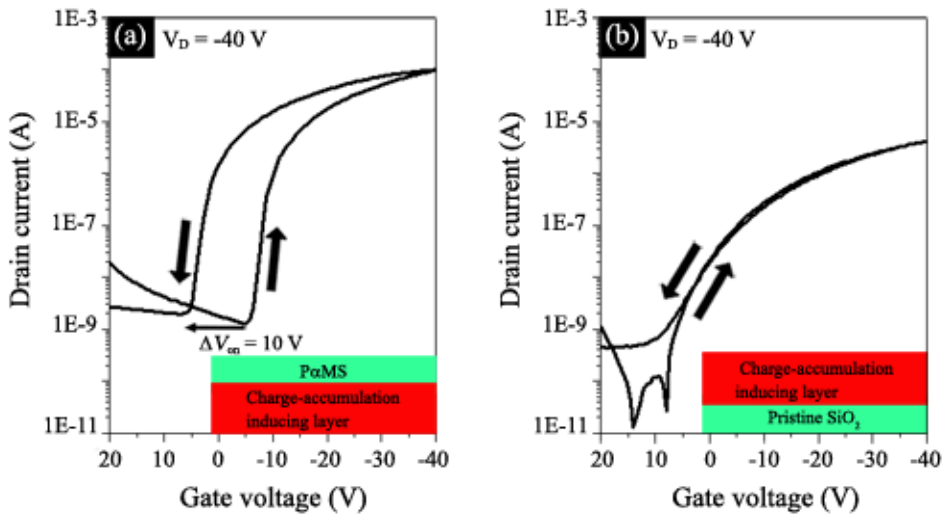


Figure 5.5 Hysteresis characteristics of the pentacene based-OTFTs including the PαMS/charge-accumulation inducing layer SiO_X-TiO_X* (a) and charge-accumulation inducing layer SiO_X-TiO_X/pristine SiO_2 of 100 nm (b) as the gate insulator, measured in ambient at V_G = -40 V.

[*] This charge-accumulation inducing layer SiO_X-TiO_X is composed of TEOS 68 wt% and GLYMO 30 wt%, and TiO_X precursor 2 wt%.

5.2.6 The TiO_X addition for controlling the gate bias voltage of the pentacene based-OTFTs

The charge-accumulation inducing layer could simply be manipulated for operating at low gate bias voltage of the pentacene based-OTFTs by adding high dielectric constant materials, such as TiO_X. To investigate the possibility of operating at the low gate bias voltage (V_G = -5 V), the pentacene based-OTFTs performance depending on components of the charge-accumulation inducing layer was measured at gate bias voltage of V_G = -5 V as shown in Figure 5.6. The output characteristic of Figure 5.6(a) illustrates the drain current of -0.2 μA at gate bias voltage of V_G = -5 V as the pentacene based-OTFT including the double-coated gate insulator without TiO_X was operated by $I-V$ measurement. Meanwhile, the drain current indicated in Figure 5.6(b) shows the increased to -0.6 μA at gate bias voltage of V_G = -5 V, because TiO_X was added in the charge-accumulation inducing layer belonging to the double-coated gate insulator. Similarly, the transfer characteristic in Figure 5.6(c) was obtained from the pentacene based-OTFT including the double-coated gate insulator without TiO_X and indicated the low field-effect mobility of 0.43 cm^2/Vs and negative shifted turn-on voltage.

According to TiO_X adding in the charge-accumulation inducing layer, the field-effect mobility of this device was improved to 1.08 cm^2/Vs and displayed the turn-on voltage of near zero, as shown in Figure 5.6(d). The increased dielectric constant of the double-coated gate insulator with TiO_X could induce the sufficient conducting channel of semiconductor at low gate bias voltage V_G = –5 V. As a result, even in low gate bias voltage, the pentacene based-OTFTs were successfully operated. In other words, according to the diverse component ratio of solution-processible metal oxide precursor, it shows the potential that the operating gate bias voltage of device can be controlled by manipulating metalorganic compound for the pentacene based-OTFTs. The metalorganic compound is component material of the charge-accumulation inducing layer.

We measured the performance of several devices according to diverse experimental conditions. To clarify the performance value of the pentacene based-OTFTs researched in this paper, Table 5.1 represents a list of parameters such as field-effect mobility, on-off ratio, threshold voltage, the capacitance, the dielectric constant and so on. Specially, the field-effect mobility of the pentacene based-OTFT including the double-coated gate insulator was dramatically increased as compared with it including the pristine SiO_2 gate insulator from

0.061 cm^2/Vs to 2.59 cm^2/Vs at gate bias voltage V_G = −20 V. The performance of OTFT including SiO_2 gate insulator was obtained from the transfer curve of Figure 5.7.

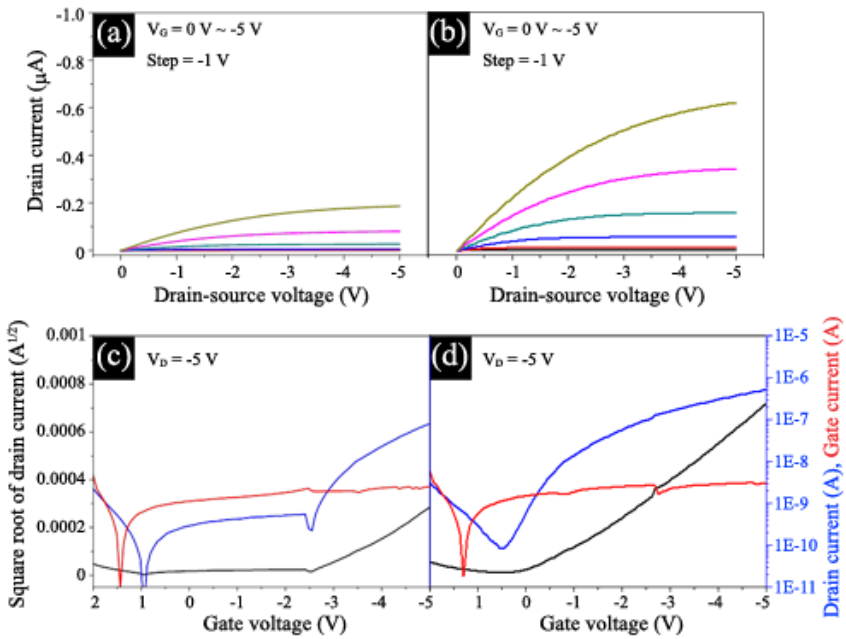


Figure 5.6 Output characteristics of the pentacene based-OTFTs including the double-coated gate insulator without TiO_X (a) and with TiO_X 10 wt% (b), measured in ambient at V_G = –5 V. Transfer characteristics of the pentacene based-OTFTs including the double-coated gate insulator without TiO_X (c) and with TiO_X 10 wt% (d), measured in ambient at V_G = –5 V.

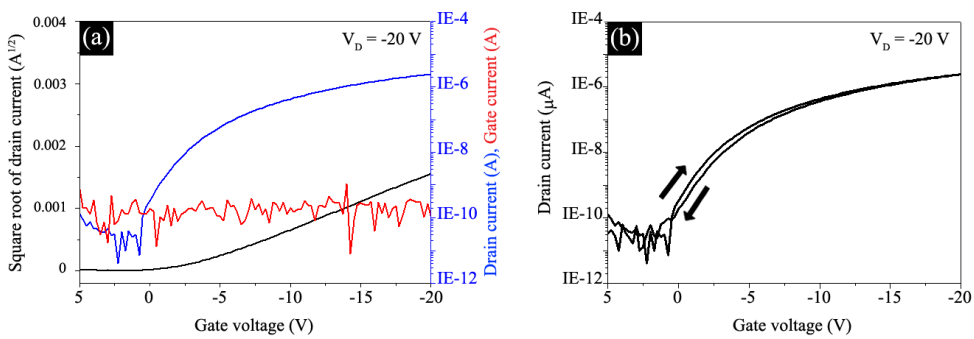


Figure 5.7 Transfer curve (a) and hysteresis curve (b) measured from the pentacene based-OTFT including the pristine SiO_2 as a gate insulator.

(The field-effect mobility: 0.061 cm^2/Vs, and on-off ratio: 10^5)

Table 5.1 The performance of the pentacene based-OTFTs included with the pristine SiO_2 gate insulator, the double-coated gate insulator[a], and the single-coated gate insulator[b]. Bending test of the pentacene based-OTFTs with the double-coated gate insulator.

Operating Voltage	Electron-trap blocking layer	Mobility (cm^2/Vs)	On-off ratio	V_{th} (V)	ΔV_{on} (V)	Thickness (nm)	Capacitance (nF/cm^2)	Dielectric constant	TiO_X ratio (wt%)
Pristine SiO_2 V_G = - 20 V	-	0.01	3.85 X 10^2	1.6	-	100	34.5	3.9	-
V_G = - 5 V	with	1.08	6.2 X 10^3	-0.4	0.35	~ 680	6.8	5.2	10
	with	0.55	3.5 X 10^2	-2.5	0.55	~ 680	5.8	4.4	0
V_G = - 20 V	with	2.01	8.5 X 10^3	-3.2	3.00	~ 680	6.8	5.2	10
	without	2.31	2.3 X 10^3	-5.7	> 10	470	7.2	3.8	10
V_G = - 20 V	with	2.59	4.4 X 10^4	-5.0	1.75	~ 680	5.8	4.4	0
	without	0.86	5.3 X 10^3	4.1	4.50	456	5.4	2.9	0
During bending[c] V_G = - 20 V	with	2.16	3.5 X 10^3	- 4.2	2.8	~ 680	5.9	4.4	0

[a] The double-coated gate insulator is composed of charge-accumulation inducing layer/electron-trap blocking layer. [b] The single-coated gate insulator is composed of charge-accumulation inducing layer. [c] Bending radius: 10 mm

5.2.7 The consideration about the improved field-effect mobility of the pentacene based-OTFTs including the double-coated gate insulator

In the previous research, it explained that the field-effect mobility has a dependency of the large crystalline size and high ordered align of pentacene in reference to XRD data. [23] To examine the reason of the field-effect mobility improving, we conducted the analysis of the pentacene crystalline on the gate insulators, which are the pristine SiO_2 and the double-coated gate insulators, and the surface properties of them.

According to XRD data of pentacene in Figure 5.8(a), the field-effect mobility of the pentacene based-OTFTs including the pristine SiO_2 would demonstrate the highest value amid the three types of the pentacene based-OTFTs. Instead, the crystalline size of pentacene (thickness: 50 nm) on the double-coated gate insulator, as shown in Figure 5.8(b, c), is similar to it on the pristine SiO_2 in Figure 5.8(d). As indicated in Table 5.1, the performance of the pentacene based-OTFTs including the double-coated gate insulators were increased, although the pentacene deposited on the charge-accumulation inducing layers exhibits lower (001) peak intensity than it on top of the pristine SiO_2.

As we scrutinized the XRD data of Figure 5.8(a), the first pentacene peak (001) at 2θ = 5.8° presents the "thin film phase", while the "triclinic bulk phase" peak (001′) is visible at 2θ = 6.2°. This diffraction angle of thin film phase means the interlayer spacing of the 15.4 Å, indicating that pentacene molecular structures in film thickness 50 nm were standing nearly perpendicular to the substrate. Practically, the thin film phase of pentacene initial growth (< 10 nm) is critical condition determining the performance of the pentacene based-OTFTs. The thin film phase is known to be transformed as film thickness increase to contain the triclinic bulk phase increase. The triclinic bulk phase tend to increase as the pentacene growth mode transition from thin film phase to bulk phase was happened due to interfacial surface energy mismatches. [24] In other words, the field-effect mobility of the pentacene based-OTFTs is under the control at the initial growth not bulk film of organic semiconductor such as pentacene.

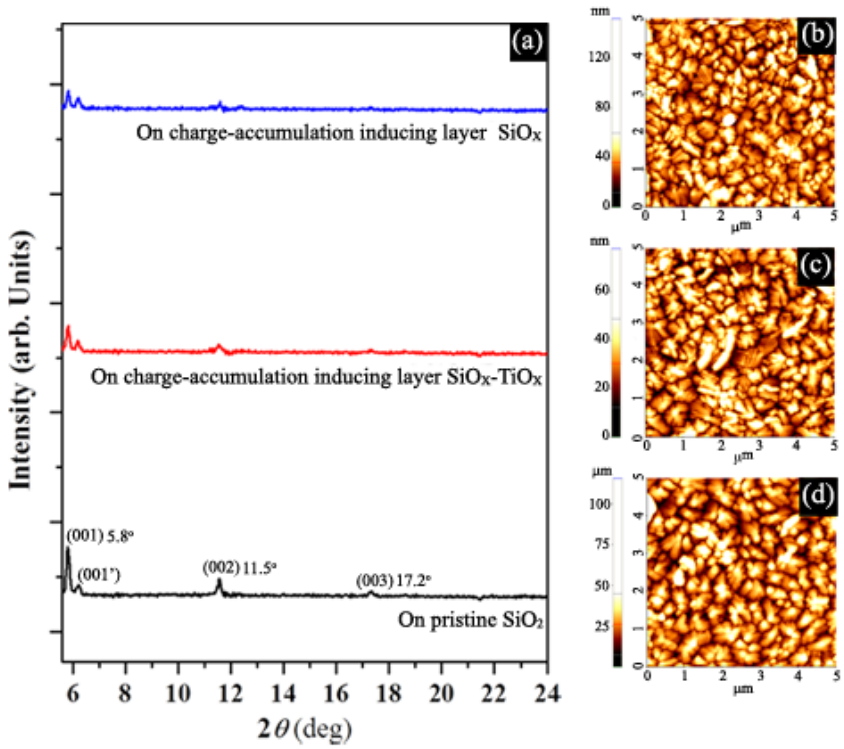


Figure 5.8 XRD data (a) of the pentacene deposited on the pristine SiO_2 and the charge-accumulation inducing layers. The pentacene morphology on the surface of the double-coated gate insulators which are charge-accumulation inducing layer SiO_X/electron-trap blocking layer (b) and charge-accumulation inducing layer SiO_X-TiO_X/electron-trap blocking layer (c) and pentacene morphology on the pristine SiO_2 (d). [Thickness of pentacene 50 nm]

Chou et al. reported that the orthorhombic phase in initial growth step can derive the improved performance of the pentacene based-OTFTs. [25] The orthorhombic phase can easily arises at the low surface energy value of 38 mJ/m^2 and thermodynamically stable at low film thickness(< 30 nm), which was suggested by Drummy et al. [26]

As mentioned above, the pentacene crystalline is controlled by the surface hydrophobicity and morphology of a gate insulator. To investigate the pentacene molecular alignment on the charge-accumulation inducing layer of the double-coated gate insulators, we measured the surface properties of them. Figure 5.9 shows the contact angles and the surface morphologies of the gate insulators, which are the pristine SiO_2 and the charge-accumulation inducing layers. The surface roughness of the pristine SiO_2 (Figure 5.9(a)) shows the best smoothness amid the three thin film surface in Figure 5.9. The surface of charge-accumulation inducing layers (Figure 5.9(b, c)) exhibits a little higher roughness than the pristine SiO_2. The higher roughness of charge-accumulation inducing layers is regarded as the origin of low intensity in pentacene (50 nm) XRD data. Thus, the initial growth of pentacene must be investigated to fine the

effect on field-effect mobility than the whole film growth of pentacene.

The surface free energy of these gate insulators was merely claculated via the contact angles (Figure 5.9(d, e, f)) in the different values as indicated in Table 5.2. The surface free energy of the charge-accumulation inducing layer made by sol-gel process was 34.5 mJ/m^2, matched in orthorhombic phase, while the pristine SiO_2 showed relatively high surface free energy, 53.5 mJ/m^2, suited in the triclinic phase as shown in Table 5.2. The low surface energy of the double-coated gate insulator well leads the orthorhombic phase at initial growth of pentacene, which helps to improve the field-effect mobility of the pentacene based-OTFTs.

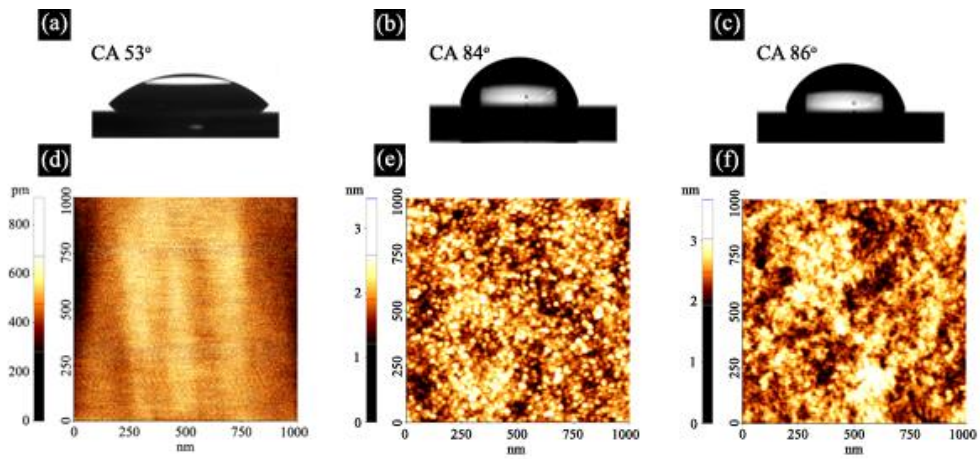


Figure 5.9 Contact angles and AFM images of the pristine SiO_2 (a, d), the charge-accumulation inducing layer SiO_X (b, e), and the charge-accumulation inducing layer SiO_X-TiO_X (c, f). Roughness: (d) 0.105 nm, (e) 0.402 nm, (f) 0.224 nm

Table 5.2 The surface properties of the pristine SiO_2 and the charge-accumulation inducing layers fabricated by sol-gel process.

Dielectric materials	Surface Roughness (nm)	Contact angle (deg)		g_s^{Pa} (mJ/m^2)	g_s^{Da} (mJ/m^2)	g_s^{a} (mJ/m^2)	SiO_X pre (wt%)	GLYMO pre (wt%)	TiO_X pre (wt%)
		Water	Diiodomethane						
Pristine SiO_2	0.105	53	39	18.3	35.2	53.5	-	-	-
SiO_X	0.402	84	53	4.1	30.4	34.5	70	30	0
SiO_X-TiO_X	0.224	85	52	3.6	31.0	34.6	60	30	10

5.2.8 The flexibility of the double-coated gate insulator

While the inorganic thin film made by sol-gel process indicates diverse advantages, such as simple fabrication by using solution process, it builds up rigid chemical bonding structures, followed by cracking on its surface. To avoid cracking of inorganic thin film, we added the GLYMO in the inorganic precursor solution. [27] The inorganic thin film was transformed to the metalorganic compound having direct metal-oxygen-carbon linkages, which gave the flexibility at the inorganic thin film. As a result, the double-coated gate insulator with GLYMO can help to represent sufficient flexibility of the pentacene based-OTFTs.

To examine the flexibility bounds and electrical durability of the double-coated gate insulator, we conducted the bending test of the pentacene based-OTFTs involving it. As shown in the inset image of Figure 5.10(a), the bending test was implemented with the curved pentacene based-OTFTs array on polyethylene terephthalate (PET) film. As the pentacene based-OTFTs were bended on the half column with radius 10 mm, the performance, such as field-effect mobility, on-off ratio, and hysteresis, were somewhat deteriorated from 2.595 cm^2/Vs to 2.160 cm^2/Vs, from 4.4×10^4 to 3.5×10^3, and from 1.75 V to 2.8 V, respectively. It means that pentacene molecules were

deformed by bending of the PET film with OTFTs array in the tensile direction, which would decrease $\pi-\pi$ overlaps of pentacene molecules. [28] Although the bended OTFTs indicated a little declined performance, they showed still low leakage current density as shown in Figure 5.10(b) . Furthermore, after the device was repeatedly curved by bending tester (Z-tec) with bending distance 5 mm, it displayed the tremendous performance degradation of transistors, as shown in Figure 5.10(c).

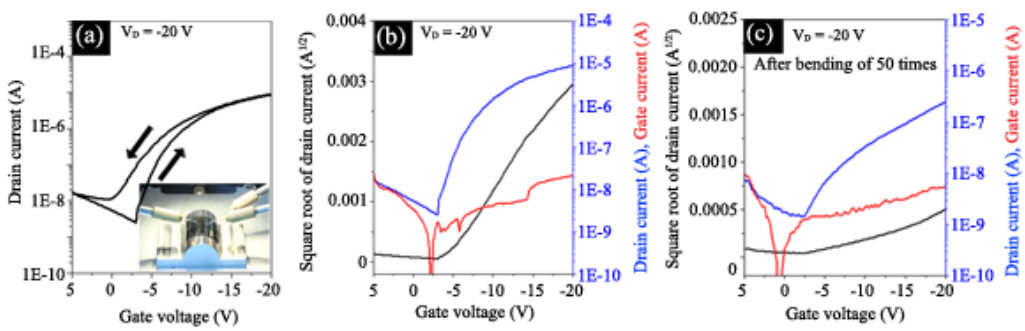


Figure 5.10 Hysteresis (a), transfer characteristics (b) of bended device and transfer characteristic (c) after 50 times bending of the pentacene based-OTFTs (bending distance: 5 mm), which contain the double-coated gate insulator, charge-accumulation inducing layer SiO_X/electron-trap blocking layer, measured in ambient at V_G = –20 V. Inset image of (a): Optical image of bending test with curvature radius of 10 mm

The reason why the performance of bending device rapidly declines is that an ITO film as gate electrode was cracked by continuative bending, as shown in Figure 5.11(a, b). Nonetheless the fine cracks (Figure 5.11(c)) appear on the double-coated thin film after the consecutive bending 50 times of the OTFTs, the gate voltage ($I_G - V_G$) property in Figure 5.10(c), namely insulator nature, was not degraded as $< 10^{-8}$ A. It explains that the fine cracks of the double-coated thin film would not be regarded to adverse effect in insulator property.

In addition, in order to investigate the electrical durability of the pentacene based-OTFTs including the double-coated gate insulator (without curvature of device), its performance were observed by using current-voltage ($I-V$) measurement. Figure 5.10 indicates that the performance of the pentacene based-OTFTs was slightly deteriorated during the consecutive stimulation test of 20 times without curving but not severe fail of the device.

The organic structure material of OTFT is commonly vulnerable to repetitive stress and readily destroyed. We implemented the repeat test of the OTFT including the double-coated gate insulator and, even at high gate bias voltage of $V_G = -20$ V, its function was maintained as Figure 5.12.

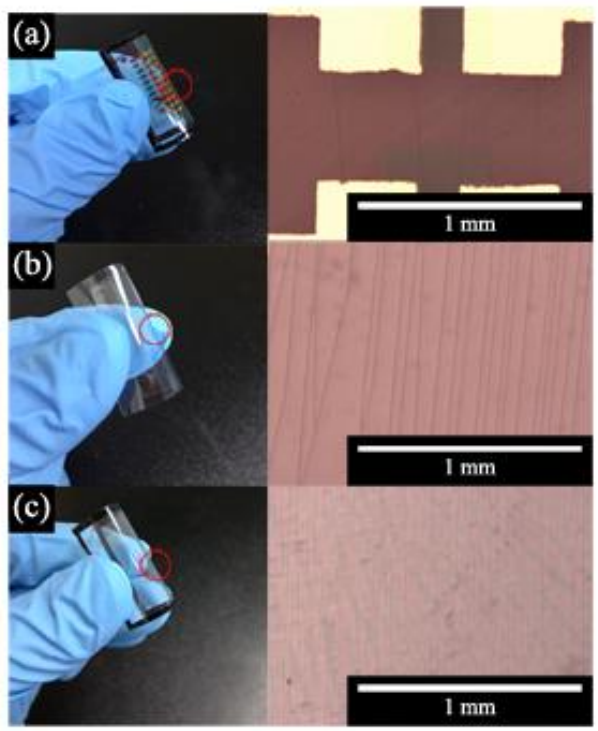


Figure 5.11 Optical images of the pentacene based-OTFTs surface (a), the ITO film surface (b), and the double-coated gate insulator, charge-accumulation inducing layer SiO_X/electron-trap blocking layer, surface (c) after consecutive bending of 50 times.

[Bending distance: 5 mm]

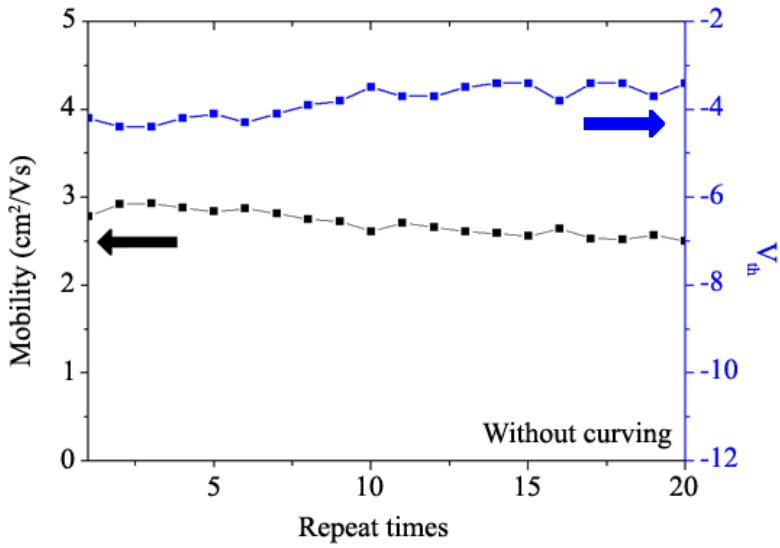


Figure 5.12 Repeat test (b) of the pentacene based-OTFTs contained with the double-coated gate insulator, charge-accumulation inducing layer SiO_X/electron-trap blocking layer, measured in ambient at operating gate bias voltage of V_G = –20 V.

5.3 Conclusion

We propose the flexible double-coated gate insulator, which is composed of the charge-accumulation inducing layer and the electron-trap blocking layer. It was fabricated by simple solution process and could be applied at bendable pentacene based-OTFTs. To harmonize the properties of organic and inorganic materials, the charge-accumulation inducing layer of the double-coated gate insulator was synthesized with inorganic based materials and crack protecting material GLYMO by sol-gel process. It was formed with flexible metal-oxygen-carbon structure, the metalorganic compound, which was able to be curved on ITO substrate. However, the charge-accumulation inducing layer is the origin of hysteresis due to unreacted –OH groups inside the layer. To minimize the hysteresis, the potassium cation-SiO_x layer was deposited by using solution process on top of the gate electrode for obstructing the electrons penetration from the gate electrode to the charge-accumulation inducing layer. In this reason, the potassium cation-SiO_X can be named by the electron-trap blocking layer.

In addition, the charge-accumulation inducing layer can simply be manipulated with the diverse high dielectric constant material. We tried to control the operating gate bias voltage of the pentacene

based-OTFTs by adding TiO_X in the charge-accumulation inducing layer. After that, the dielectric constant of the double-coated gate insulator was increased and the operating gate bias voltage of the pentacene based-OTFTs could be lowed at V_G = -5 V.

The double-coated gate insulator composed of the charge-accumulation inducing layer and the electron-trap blocking layer showed the merits of flexible organic materials and high quality inorganic material because they were properly combined with their pros features in molecular level. Finally, the pentacene based-OTFTs applied with the double-coated gate insulator exhibited the improved electrical property as well as the good flexibility of device.

5.4 Reference

[1] Flexible Flat Panel Display Technology. G. P. Crawford, Wiley-SID, 2005, Ch 1.

[2] Particle display technologies become e-Paper. T. Z. Kosc, Optics & Photonics News, 2005, 18 p.

[3] S. R. Forrest, *Nature*. 2004, *428*, 911.

[4] S. J. Jo, C. S. Kim, M. J. Lee, J. B. Kim, S. Y. Ryu, J. H. Noh, K. Ihm, H. K. Baik, Y. S. Kim, *Adv. Mater.* 2008, *20*, 1146.

[5] V. C. Sunder, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willett, T. Someya, M. E. Gershenson, J. A. Rogers, *Sciene.* 2004, *303*, 1644.

[6] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, D. M. de Leeuw, *Nature*. 1999, *401*, 685.

[7] D. H. Kim, D. Y. Lee, H. S. Lee, W. H. Lee, Y. H. Kim, J. I. Han, K. Cho, *Adv. Mater.* 2007, *19*, 678.

[8] H. S. Byun, Y.-X. Xu, C. K. Song, *Thin Solid Films*. 2005, *493*, 278.

[9] F. D. Angelis, S. Cipolloni, L. Mariucci, G. Fortunato, *Appl. Phys. Lett*. 2005, *86*, 203505.

[10] X. Cheng, M. Caironi, Y.-Y. Noh, J. Wang, C. Newman, H. Yan, A. Facchetti, H. Sirringhaus, *Chem. Mater.* 2010, *22*, 1559.

[11] J. Veres, S. Ogier, G. Lloyd, D. de Leeuw, *Chem. Mater.* 2004, *16*, 4543.

[12] R. G. Gordon, J. Becker, D. Hausmann, S. Suh, *Chem. Mater.* 2001, *13*, 2463.

[13] F.-C. Chen, C.-W. Chu, J. He, Y. Tang, *Appl. Phys. Lett.* 2004, *85*, 3295.

[14] A. Maliakal, H. Katz, P. M. Cotts, S. Subramoney, P. Mirau, *J. Am. Chem. Soc.* 2005, *127*, 14655.

[15] T. Cahyadi, H. S. Tan, S. G. Mhaisalker, P. S. Lee, F. Boey, *Appl. Phys. Lett.* 2007, *91*, 242107.

[16] J. Kim, S. H. Lim, Y. S. Kim, *J. Am. Chem. Soc.* 2010, *132*, 14721.

[17] J. Robertson, *Rep. Prog. Phys.* 2006, *69*, 327.

[18] R. Wallace, G. Wilk, *MRS Bull.* 2002, *March 2002*, 192.

[19] H. Yanagisawa, T. Tamaki, M. Nakamura, K. Kudo, *Thin Solid Film.* 2004, *464*, 398.

[20] C. G. Choi, B.-S. Bae, *Electrochem. Solid-State. Lett.* 2007, *10*, H347.

[21] S. Jeong, D. Kim, S. Lee, B.-K. Park, J. Moon, *Appl. Phys. Lett.* 2006, *89*, 092101.

[22] C. Kim, A. Facchetti, T. J. Marks, *Adv. Mater.* 2007, *19*, 2561.

[23] H. S. Tan, S. R. Kulkarni, T. Cahyadi, P. S. Lee, S. G. Mhaisalkar, J. kasim, Z. X. Shen, F. R. Zhu, *Appl. Phys. Lett.* 2008, *93*, 183503.

[24] W. Xu, S.-W. Rhee, *J. Mater. Chem.* 2009, *19*, 5250.

[25] L. F. Drummy, D. C. Martin, *Adv. Mater.* 2005, *17*, 903.

[26] W.-Y. Chou, C.-W. Kuo, H.-L. Cheng, Y.-R. Chen, F.-C. Tang, F.-Y. Yang, D.-Y. Shu, C.-C. Liao, *Appl. Phys. Lett.* 2006, *89*, 112126.

[27] J. Kim, M. Kim, M. J. Lee, J. S. Lee, K. Shin, Y. S. Kim, *Adv. Mater.* 2009, *21*, 4050.

[28] R. Nakahara, M. Uno, T. Uemura, K. Takimiya, J. Takeya, *Adv. Mater.* 2012, *24*, 5212.

Chapter 6. Conclusions

In this paper, the two gate insulators were developed for improving the performance of organic semiconductor based-OTFTs. They assist the performance enhancement of organic semiconductor based-OTFTs, which have intrinsic limitation of organic semiconductor, such as electron mobility in conducting channel. To achieve improved performance of organic semiconductor based-OTFTs, the superior gate insulators need certainly as well as organic semiconductor of high electron mobility.

First, a TiO_2-PVP composite (TPC) gate insulator was introduced for OTFTs operation at low gate bias voltage. The dielectric properties of TPC, which is composed of PVP, a cross-linker, and a TiO_2 precursor, were enhanced due to the dense chemical structure of the polymer (PVP) and high k materials (TiO_2 precursor). This TPC gate insulator can simply be used in solution processes, such as spin casting and showed good stability in ambient conditions, air environments and moisture conditions. The TPC as a gate insulator could sufficiently hinder leakage currents and successfully operates at low gate bias voltage ($\leq V_G = -3$ V). Furthermore, the TPC gate insulator exhibited enhanced performance characteristics of OTFTs, such as on/off ratio, mobility, and subthreshold swing, compared with

the pristine PVP gate insulator. Although this device shows low field-effect mobility because of intrinsic organic semiconductor limitation, it operated well at a low gate bias voltage with the considerable and remarkable performance.

Second, to overcome the intrinsic limitation of organic semiconductor, which is low electron mobility, the gate insulator organized with metal oxide materials was fabricated by sol-gel process. We propose the flexible double-coated gate insulator, which is composed of the charge-accumulation inducing layer and the electron-trap blocking layer. It was fabricated by simple solution process and could be applied at bendable pentacene based-OTFTs. To harmonize the properties of organic and inorganic materials, the charge-accumulation inducing layer of the double-coated gate insulator was synthesized with inorganic based materials and crack protecting material GLYMO by sol-gel process. It was formed with flexible metal-oxygen-carbon structure, the metalorganic compound, which was able to be curved on ITO substrate. However, the charge-accumulation inducing layer is the origin of hysteresis due to unreacted –OH groups inside the layer. To improve the drawback, the potassium cation-SiO_x layer was deposited by using solution process on top of the gate electrode for obstructing the electrons penetration

from the gate electrode to the charge-accumulation inducing layer. In this reason, the potassium cation-SiO_X can be named by the electron-trap blocking layer.

In addition, the charge-accumulation inducing layer can simply be manipulated with the diverse high dielectric constant material. We tried to control the operating gate bias voltage of the pentacene based-OTFTs by adding TiO_X in the charge-accumulation inducing layer. After that, the dielectric constant of the double-coated gate insulator was increased and the operating gate bias voltage of the pentacene based-OTFTs could be lowed at V_G = -5 V.

The double-coated gate insulator composed of the charge-accumulation inducing layer and the electron-trap blocking layer showed the merits of flexible organic materials and high quality inorganic material because they were properly combined with their pros features in molecular level. The pentacene based-OTFTs applied with the double-coated gate insulator exhibited the improved electrical property as well as the good flexibility of device.

Finally, the gate insulators were invented for organic semiconductor based-OTFTs, which have to show good flexible and high performance. To accord to the conditions of the gate insulators, the TiO_2-PVP composite (TPC) and the double-coated gate insulator

were fabricated and applied at organic semiconductor based-OTFTs. They exhibited sufficient flexibility and enhanced performance that TPC enabled the device operation at low gate bias voltage and the double-coated gate insulator helped the increment of field-effect mobility of OTFTs.

List of Publications

[1] **Preparing**: Joohee Kim and Youn Sang Kim*, "Double-Coated Gate Insulator for Flexible and High Performance Organic Thin Film Transistors" (2013)

[2] Kyunghee Lee, Joohee Kim, Kyusoon Shin*, Youn Sang Kim*, "Micropatterned crystalline organic semiconductors via direct pattern transfer printing with PDMS stamp" **Journal of Materials Chemistry**, 22, 22763 (2012)

[3] Joohee Kim, Sung Hee Lim, and Youn Sang Kim, "Solution-Based TiO_2-Polymer Composite Dielectric for Low Operating Voltage OTFTs" **Journal of the American Chemical Society**, 132, 14721 (2010)

[4] Xiaoqiang Chen, Sunwoo Kang, Min Jung Kim, Joohee Kim, Youn Sang Kim, Heejin Kim, Bo Chi, Sung-Jin Kim, Jin Yong Lee and Juyoung Yoon, "Thin Film Formation of Imidazolium Based Conjugated Polydiacetylenes and Their Application for Sensing Anionic Surfactants" **Angewandte. Chemie In. Ed.**, 49, 1422 (2010)

[5] Min Jung Lee, Joohee Kim, Ji Soo Lee and Youn Sang Kim, "Pressure-assisted printing with crack-free metal electrodes using an anti-adhesive rigiflex stamp" Journal of Materials Chemistry, 20, 2746 (2010)

[6] Minwoo Park, Dong Choon Hyun, Joohee Kim, Youn Sang Kim, and Unyong Jeong, "Dewetting-Induced Formation of Periodic Dot Arrays of Polymer/Au Composites by Capillary Force Lithography" Chemical Materials, 22, 4166 (2010)

[7] Sung Hee Lim, Joohee Kim, Sang-gi Lee and Youn Sang Kim, "Water-soluble polymer dielectric with potential for high performance organic thin-film transistors" Chemical Communications, 46, 3961 (2010)

[8] Joohee Kim, Mihee Kim, Min Jung Lee, Ji Soo Lee, Kyusoon Shin, and Youn Sang Kim, "Low-Cost Transparent and Hard Replica Mold for Imprint Lithography" Advanced Materials, 21, 4050 (2009)

[9] Jeongju Park, Joohee Kim, Seryun Lee, Joona Bang, Bumjun J. Kim, Youn Sang Kim* and Jinhan Cho* "Free-Standing Film

Electronics Using Photo-crosslinking Layer-by-Layer Assembly" **Journal of Materials Chemistry,** 19, 4488 (2009)

[10] Sung Jin Jo, Chang Su Kim, Jong Bok Kim, Joohee Kim, Min Jung Lee, Hyeon Seok Hwang, Hong Koo Baik, and Youn Sang Kim, "Surface property controllable multilayered gate dielectric for low voltage organic thin film transistors" **Applied Physics letters**, 93, 083504 (2008)

요 약 (국문초록)

본 연구에서는 유연한 고성능의 유기 전자에 적용하기 위한 절연막 개발에 초점을 두었다. 절연막은 고가의 장비를 사용하지 않는 저렴한 비용의 간단한 방법인 용액공정을 기반으로 하였다. 유기 전자소자는 주로 매우 유연하고 투명하여 차세대 소자로 각광을 받고 있지만, 소자의 낮은 성능으로 인해 극복해야 하는 문제점들이 아직은 존재한다. 지금까지는 대부분 반도체의 성능 향상시키는데 초점을 두었지만, 절연막의 성능향상이 함께 이루어질 때 보다 우수한 소자의 구현이 가능해질 수 있다. 일반적으로 절연막은 유기물과 무기물 그리고 유무기 하이브리드로 제작이 가능하며 그에 따른 각기 다른 장단점들이 있다.

유기물로 제작된 절연막은 매우 유연하고 투명하여 플렉서블 소자의 적용이 용이하지만, 낮은 유전상수로 인해 소자 성능의 저하를 불러올 수 있다. 반면에 무기물로 이루어진 절연막의 경우는 매우 높은 유전 상수를 가지는 다양한 물질들이 있어 소자 성능향상에 도움이 되지만, 비교적 좁은 밴드 갭과 200 도 이하의 온도에서 쉽게 다결정을 이루어 수 많은 결정입계를 형성하고 이들은 누설 전류의 원인으로 작용할 수 있다. 따라서 이러한 두 가지 종류의 물질을 함께 섞어 하이브리드 또는 합성물을 만들어 서로의 장점을 가져오고 단점을 보완하는 연구들이 최근 많이 이루어지고 있다.

본 연구에서도 유기물 기반에 무기물을 첨가하는 TiO_2-PVP 합성물 (TPC) 로 이루어진 절연막을 개발하였다. TPC 절연막은 TiO_2 로 인하여 -3 V 의 낮은 전압에서도 구동이 가능하였고 누설 전류 또한 PVP 수준과 비슷한 정도를 유지할 수 있었다. 이것은 TiO_2 의 첨가된 형태는 입자로 단순히 섞인 상태가 아닌 –OH 그룹이 있는 분자로 PVP 의 –OH 그룹들과 가교를 쉽게 이루어 매우 치밀한 절연막을 형성할 수 있었기 때문에 누설 전류의 증가를 막을 수 있었다. TPC 절연막을 유기 전자 소자에 도입하여 성능을 측정한 결과 -3 V 의 구동 전압 하에서 PVP 로 제작된 소자보다 약 2.5 배 정도의 0.105 cm^2/Vs 이동도 향상을 보였다.

또한 무기물 기반의 물질에 유기물의 성질을 가져갈 수 있도록 졸겔법을 이용하여 절연막을 제작하였다. 일반적으로 무기물 전구체들을 가교시켜 무기막을 형성할 수 있지만 이는 매우 딱딱한 성질을 가지고 있어 외부의 작은 자극에 의해서도 쉽게 깨질 수 있다. 이를 막기 위해 탄소체인을 가지고 있는 GLYMO 를 첨가하여 박막의 안정성을 높였다. 그러나, 졸-겔 법은 반응 중에 수 많은 –OH 그룹을 박막내부에 남겨둘 수 있으며 이는 소자의 치명적인 단점인 이력현상을 일으킬 수 있다. 이 박막 내부의 전자 트랩을 일으키는 원인이 되므로 이를 방지하기 위해 게이트에서 절연막으로 주입되는 전자를 막는 층의 삽입이 필요하다. 이 두 층은 모두 용액공정을 기반으로 하고 다양한 무기물 전구체의 도입이 가능하므로 다양한 물질을 배합하여 목적에 맞는 절연막을 만들 수 있다. 이들은 모두 비정질로서 무기물임에도 유연한 성질을 나타내며 높은 유전상수의 물질을

첨가함으로써 낮은 전압에서도 구동이 가능하다. 실제로 이 절연막을 이용하여 이동도를 측정한 결과 −20 V 의 구동 전압 하에서 2.59 cm^2/Vs 의 이동도를 나타냈고, −5 V 의 구동 전압에서도 1.08 cm^2/Vs 로 유기 반도체로 제작된 소자의 경우로서는 매우 우수한 성능을 나타내는 것을 확인할 수 있었다.

주요어 : 유기 전자 소자, 절연막, 고 유전 상수 물질, 하이브리드 물질, 졸−겔 법, 이력현상

학 번 : 2009−31183

Appendix

Simple fabrication of patterned organic semiconductors via direct pattern transfer process with PDMS stamp

1. Introduction

Solution-processable organic semiconductors have become attractive materials for low-cost, large-area, and flexible devices based on organic thin film transistors (OTFTs) such as active matix display backplanes, smart cards, and radio-frequecy identification (RFID) tags.[1, 2] 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN), chemically modified pentacene derivatives, have been great interested because of its excellent semiconducting behavior by strong π-π stacking of functional groups as well as high solubility in common organic solvents.[3] Several groups have reported effective approaches to produce organic single crystal semiconductors using solution process such as spin coating [4, 5], drop casting [6-10], ink-jet printing [11, 12], and dip coating [13, 14]. The formation and growth of TIPS-PEN single crystals in solution processes is strongly affected by the evaporation rate of solvents.[15, 16] Mono solvents, however, are limited to control the evaporation rate due to their intrinsic physical properties. Especially, for solvents with lower boiling point, they are

not proper solvents to grow single crystals because they have insufficient molecular organization by a short crystallization time with fast evaporation speed.[15, 16] Thus, Gelinck *et al*. have suggested azeotropic binary solvent mixtures to prepare large single crystals of TIPS-PEN by controlling evaporation rates.[17] The morphology change from polycrystalline to large single crystals was found at the azeotropic point with a moderate initial mixing ratio, and it leaded to the enhanced transistor performance.[17] Cho *et al*. have employed binary solvent mixtures for inducing two flows in a droplet, convective flow and Marangoni flow, to obtain single crystals during drying solvents.[12] Highly ordered TIPS-PEN crystals in a small droplet were produced by the balance of evaporation- and diffusion-driven flows, and showed the improved device performance with an effective field-effect mobility of 0.12 $cm^2V^{-1}s^{-1}$.[12] Although single crystal OTFTs are ideal device structures due to high mobility and outstanding electrical characteristics, it still remains a technical problem to integrate single crystals in practical device applications. Single crystal OTFTs are manufactured one device at a time by handpicking, but this handpicking process has critical limitations to place it onto the substrate for a very tiny crystal in submicrometer scale and to control precise locations of organic single crystals.[18-21]

Moreover, selective deposition of organic semiconductors is essential to reduce or eliminate parasitic current paths (crosstalk) between neighboring devices.[22]

Chemical or physical approaches to control the deposition of single crystals at the required position are suggested. Bao and coworkers have focused on solution processing techniques for selective deposition of organic single crystals in a certain location with the introduction of wettability-controlled patterns on the surfaces.[23, 24] Even though single crystals selectively deposited on preferential regions, it was impossible to obtain uniform films due to different number and shape of organic crystals in patterned region. Recently, patterning technique of single crystals based on the selective etching of TIPS-PEN by thermal evaporation has been developed.[25] It was a novel process to fabricate the micropatterned single crystals with different sizes and shapes. However, it depends on the location of the pre-formed initial single crystal grown the substrate before selective etching.

2. Results and discussions

In this research, we present a direct pattern transfer process using patterned poly(dimethylsiloxane) (PDMS) stamp including TIPS-PEN crystals to fabricate uniform organic semiconductor films on the desired position. Our method is based on the crystallization of TIPS-PEN along the patterned surface of PDMS stamp, which obtained after soaking in TIPS-PEN solution and drying solvents. Here, we employed mono solvents, in fact, which have been reported that it is limited to fabricate uniform thin films by conventional deposition techniques due to their intrinsic evaporation rate.[12, 15, 26] For example, as the film was prepared by spin-coating of TIPS-PEN solution, it has a low degree of crystalline microstructures by fast evaporation rate during solution casting and is discontinuous film with the disorder grain connectivity between small crystals, as shown in Figure 1(a). In drop casting case, a ring-like (coffee-staining) structure that marked at the perimeter of the droplet was observed. (Figure 1(b-2)) Additionally, when the chemical patterns were introduced on the surfaces, the aggregation of TIPS-PEN crystals were discovered at the edge of surface pattern, producing a discontinuous morphology in the pattern. (Figure 1(c)) However, Figure 1(d) represents homogeneous TIPS-PEN films prepared by our method, the direct

pattern transfer process. The TIPS-PEN crystals on the PDMS stamp could be transferred to any substrates by the difference of surface adhesion between PDMS stamp and the substrate. The transferred TIPS-PEN films are not large single crystals, but quite uniform. Furthermore, it has no further etching step for patterning the semiconductors to avoid the crosstalk. We could also adjust the position of TIPS-PEN semiconductors via stamping the TIPS-PEN/PDMS stamp to the substrates. The OTFTs with patterned TIPS-PEN crystalline films show the typical p-type device behavior with an On/Off ratio of ~10^4 and the field effect mobility of ~0.1 $cm^2 V^{-1} s^{-1}$, which is much higher than that of the OTFTs prepared by other coating processes with similar solution.[15, 16, 27] We also demonstrate that thin and uniform TIPS-PEN semiconductors with different sizes and shapes are readily formed on organic/inorganic gate insulators.

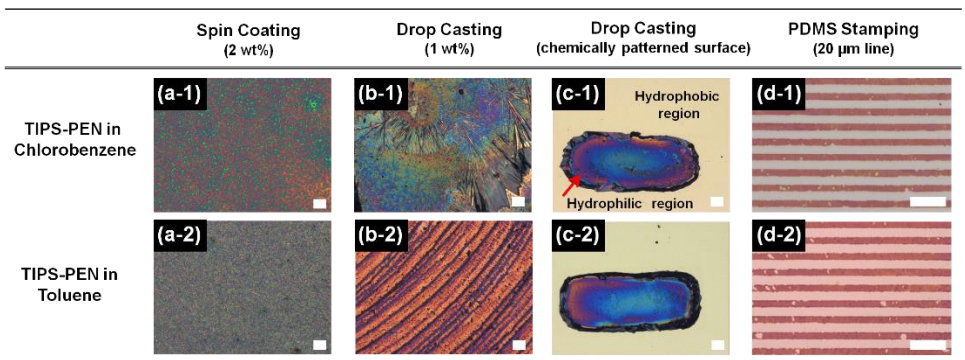


Figure 1. OM images of surface morphologies of TIPS-PEN films obtained by various deposition methods. Each film is prepared by spin coating with 2 wt% TIPS-PEN solution (a), drop casting with 1 wt% TIPS-PEN solution on SiO_2 surface (b) and on chemically patterned SiO_2 surface (c), and direct pattern transfer process with 1wt% TIPS-PEN solution (d). Scale bars are 100 μm.

Figure 2. shows schematic illustration of experimental procedures. The bottom surface of PDMS pad was attached to the glass in order to induce directional evaporation to the patterned top surface during drying solvents. When the patterned PDMS pad was immersed in 1 wt% TIPS-PEN/chlorobenzene solution for 1 hr, the PDMS pad was swelled by organic solvents, containing TIPS-PEN solution. During drying solvents under vacuum, the swelled PDMS pad returned to the initial size, and most TIPS-PEN crystals were formed along the patterns at the top surface. If the PDMS pad was not stuck to the glass, the TIPS-PEN crystals could prefer to form bulky crystals at the unpatterned bottom surface, so few TIPS-PEN crystals could exist on the patterned top surface.(Figure 3(a,b)) Evaporation time was an important factor to obtain homogeneously thin films according to the size of PDMS stamp. The longer the evaporation time was, the thicker the thickness of TIPS-PEN films gets from the edge to center region of pattern.(Figure 3(c,d)) For the PDMS surface with ~50 mm^2, the effective evaporation time was approximately 4 hrs in this study. To transfer the TIPS-PEN crystals, the TIPS-PEN/PDMS stamp was subsequently in conformal contact with the substrates.

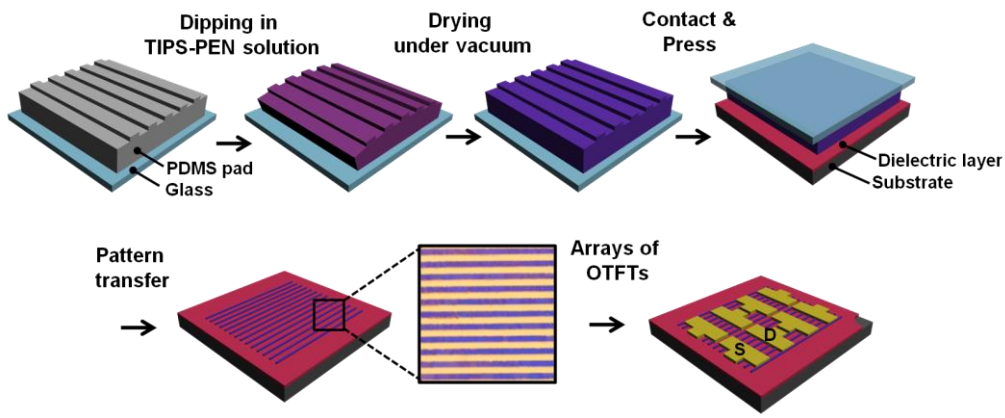


Figure 2. Schematic route for preparing the micropatterned TIPS-PEN semiconductors via the direct pattern transfer process.

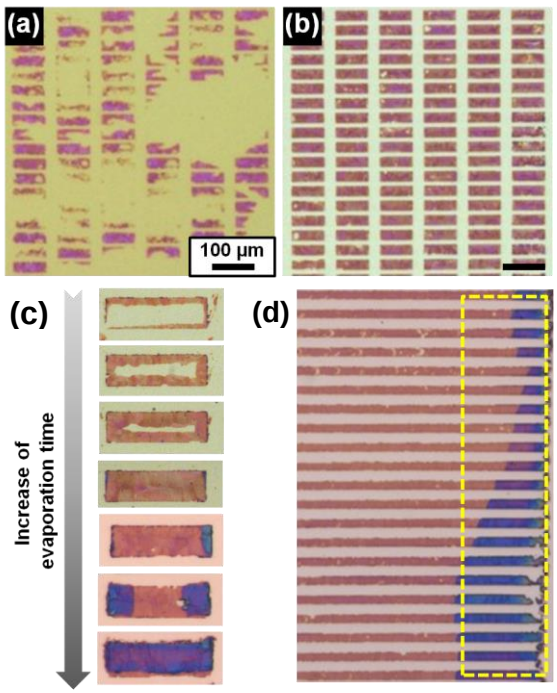


Figure 3. OM images of the transferred TIPS-PEN films by the direct pattern transfer process with free standing PDMS pad (a) and the PDMS pad attached to the glass (b).

The degree of TIPS-PEN crystallization with the increase of evaporation time in rectangular patterns (c) and in line patterns (d).

The TIPS-PEN crystals onto PDMS surface were transferred onto the substrates because of a low surface energy of PDMS (~21 mN/m). The films, however, was discontinuous and it was difficulty in controlling the film thickness. Thus, the TIPS-PEN/PDMS stamp was placed on the substrates after spin-coating of pure solvents (for Si/SiO_2 substrate) or polymer solutions (for Si or ITO-glass substrate) in order to improve interfacial contact between TIPS-PEN crystals on the protruding regions of the PDMS stamp and the substrates. Then, the TIPS-PEN/PDMS stamp was slightly pressed for a few seconds, and detached. The residual solvent on the substrates after spin coating made TIPS-PEN crystals better contact with the substrate, so uniformly thin films were obtained.(Figure 4) The transferred TIPS-PEN crystals were shown in Figure 5. The thickness of the films was approximately 60 nm measured by atomic force microscopy (AFM). (Figure 5(a)) Line patterned TIPS-PEN films with a variety of sizes ranging from 10 to 40 μm were fabricated with regular thickness via the direct pattern transfer process using the TIPS-PEN/PDMS stamp. (Figure 5(b-g))

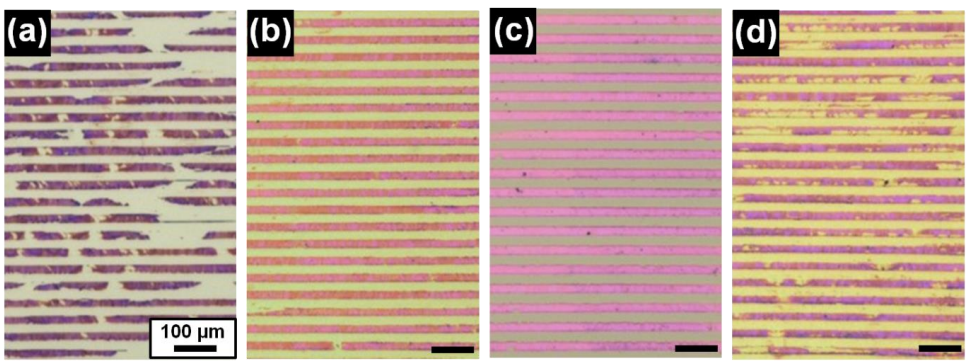


Figure 4. OM images of the transferred TIPS-PEN patterns. When the TIPS-PEN/PDMS stamp is in conformal contact with the SiO_2 surface, the transferred TIPS-PEN film is discontinuous (a). After spin coating of pure solvent (for the SiO_2 surface) (b) or PMMA solution (for the Si surface) (c), the TIPS-PEN film becomes uniformly continuous. As the TIPS-PEN film is transferred onto the PMMA surface after the removal of residual solvent, the line patterns are irregular (d).

Additionally, the rectangular patterns with length x width dimensions of 20 x 70 μm^2 were transferred onto the Si/PMMA, Si/SiO_2, and ITO glass/PMMA substrates, as shown in Figure 5(h-j) without any further etching process. Regardless of the type of the bottom electrode or gate insulator materials, organic semiconductors were well transferred on the surface at the desired position. The crystalline nature of TIPS-PEN was confirmed with x-ray diffraction (XRD). The diffraction pattern from TIPS-PEN/PDMS stamp contains a (00*l*) reflection corresponding to a *c*-axis 16.6 Å in the TIPS-PEN unit cell, similar to previous reported results.[15, 16] Even though the crystallization of TIPS-PEN on the protruding surfaces was restricted by the pattern size of PDMS pad, the TIPS-PEN onto TIPS-PEN/PDMS stamp exhibits comparable crystallinity. The peak intensity of the transferred surfaces was relatively weak because the film was thin and already patterned, but the transferred TIPS-PEN on SiO_2 and PMMA dielectric layer represented at least crystalline. (Figure 6)

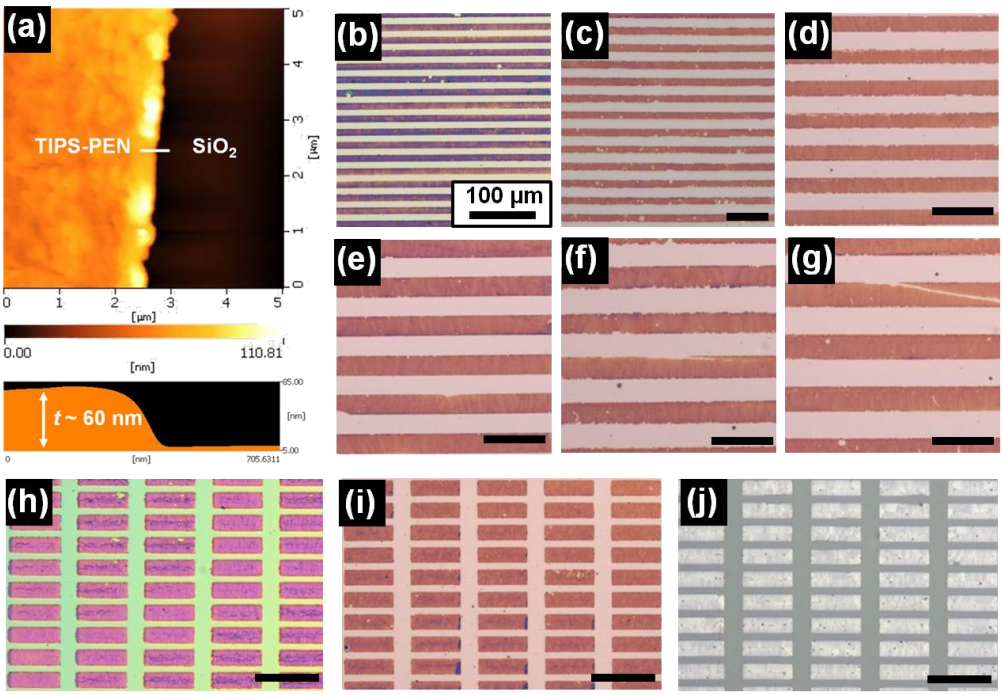


Figure 5. AFM images (a) and OM images of the transferred TIPS-PEN micropatterns with various sizes and shapes on the dielectric surfaces. The sizes of line pattern are 10 (b), 20 (c), 25 (d), 30 (e), 35 (f), and 40 μm (g). The rectangular patterns are transferred onto Si/PMMA (h), Si/SiO_2 (i), and ITO glass/PMMA (j) surfaces.

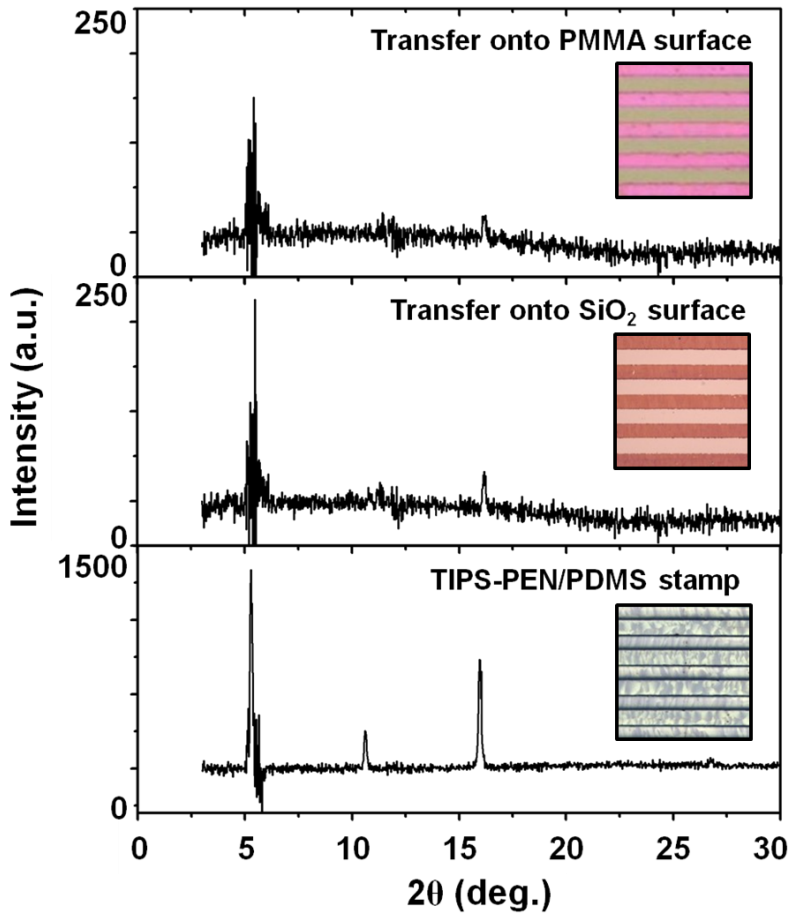


Figure 6. X-ray diffraction patterns ($\theta/2\theta$ mode) for the TIPS-PEN crystals on the TIPS-PEN/PDMS stamp and transferred surfaces. The peaks are attributed to the (00*l*) lattice plane in the crystals.

Figure 7. represents the electrical properties of bottom gate and top contact OTFTs with micropatterned TIPS-PEN semiconductors muanufactured by the direct pattern transfer process. About 25 lines of TIPS-PEN micropatterns were bridged between each Au source and drain electrode.(the inset of Figure 7(a), left) The representative transfer curve from the OTFTs with patterned semiconductor films on inorganic (SiO_2) and organic (PMMA) gate insulator in Figure 7(a) and b, respectively, show typical p-type current modulation. The output characteristics of the OTFTs also show saturation behavior beyond a V_D of -40V. (Figure 8(a,b)) In transfer curve of Figure 7(a), an On/Off ratio was ~10^4 and the field-effect mobility (μ) was calculated to be approximately 0.1 $cm^2V^{-1}s^{-1}$, according to the MOSFET standard model in the saturated regime, $I_D = (W/2L)C_i\mu(V_G - V_T)^2$, where W presents the width of the channel, L is the length of the channel between the source and the drain contacts, C_i is the areal capacitance of dielectric layer, and V_T is the threshold voltage. The values of this OTFTs present more enhanced device performance than that of the devices prepared by typical deposition methods using mono solvents, previously reported.[15, 16, 27] The AFM iamge of Figure 7(a) shows that the morphological uniformiety of the transferred TIPS-PEN plays a critical role in improving charge

transport. (Figure 7(a), right) In contrast, the field-effect mobility on PMMA dielectric layer was calcuated to be ~0.03 $cm^2V^{-1}s^{-1}$. The reduced mobility can be explained by the presence of drain current offset in a low gate bias of the output curve. (Figure 8(a,b)) The drain current offset induced by poor film morpholgy leads to the leakage current, which contributes to poor drain current modulation.[28] The AFM iamges of Figure 7(b) supported that the device performance is dramatically influenced by the morphological structures of organic semiconductor, which correlated to the charge carrier transport. Moreover, the polymer bulge was also observed at the edge part of TIPS-PEN patterns. (Figure 8(c-e)) It was considered that the PMMA surface was slightly patterend by PDMS stamp during the contact and press process because polymer chains could be mobile by residual solvent after spin coating of polymer solution. As a result, these surface heterogeneities on PMMA dielectric layer could lead to decline the electrical properties of OTFTs. However, the threshold voltage (V_T) of the transistor with polymer gate insulator was ~0.69 V. It was interpreted that the interface states of semiconductors/dielectrics are still favorable in spite of the morphological heterogeneities.

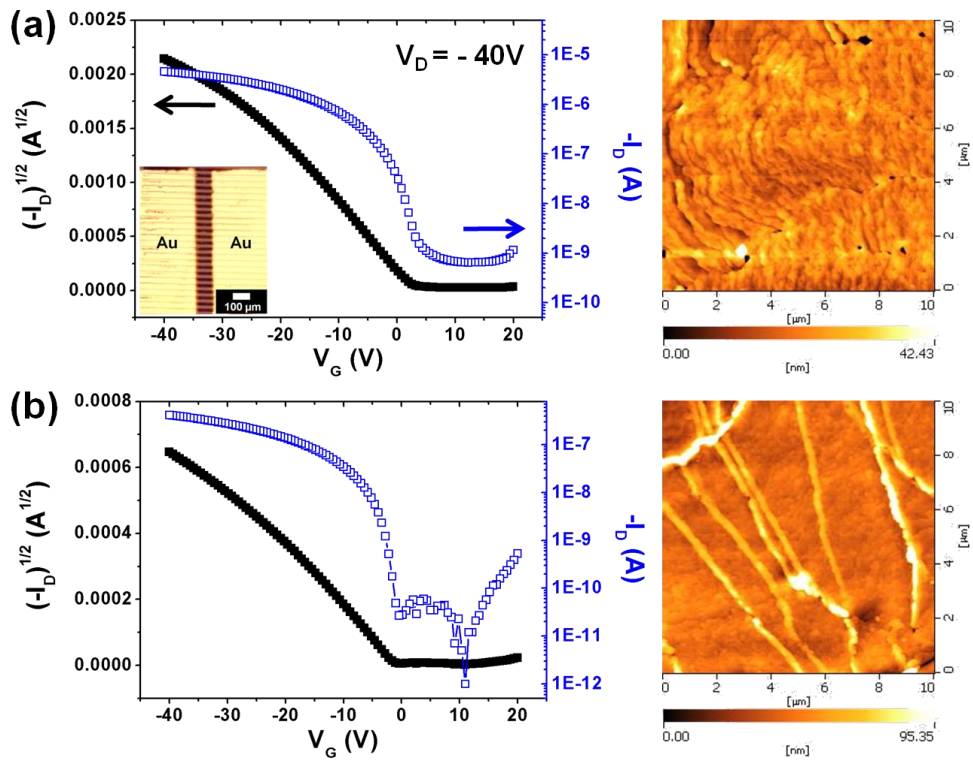


Figure 7. The transfer curve (left) and AFM image (right) of the OTFTs with patterned TIPS-PEN semiconductors on SiO_2 surfaces (a) and PMMA surfaces (b). The inset displays bottom gate, top contact OTFTs with ~25 lines of TIPS-PEN channels bridged between Au source and drain.

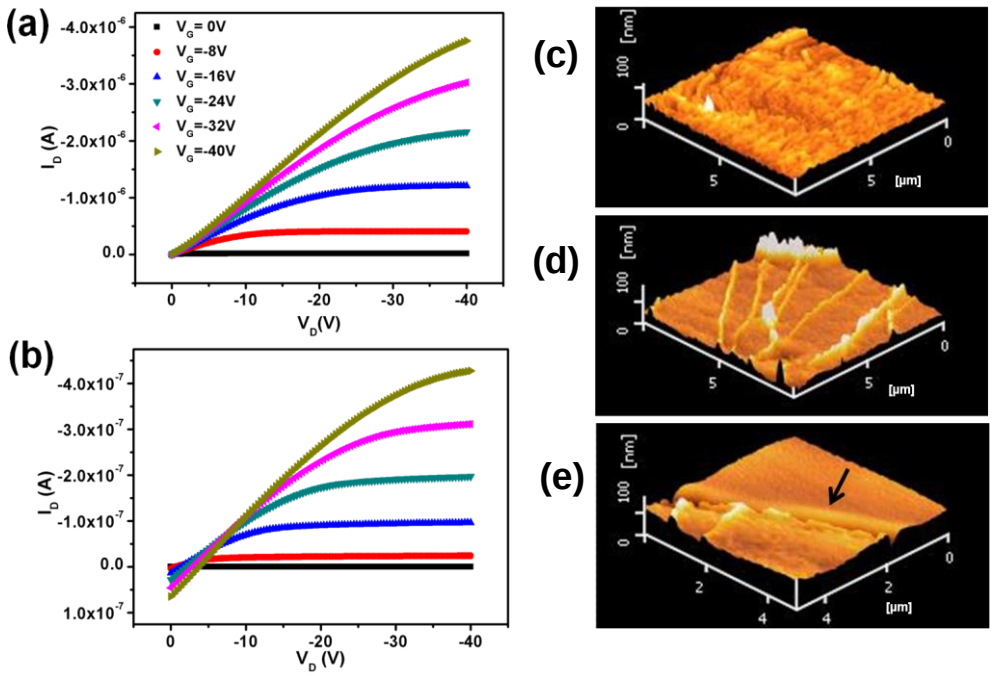


Figure 8. Output curves of the OTFTs with micropatterned TIPS-PEN semiconductors on Si/SiO_2 (a) and Si/PMMA surfaces (b). Three-dimensional AFM images of the transferred TIPS-PEN morphology on Si/SiO_2 (c) and Si/PMMA surfaces (the center region: (d)/ the edge region: (e)). The arrow in (e) indicates the patterned PMMA surface during stamping process.

We also investigated the dependence of soaking solution of PDMS stamp on the electrical properties of OTFTs, as summarized in Table 1. The difference of the device performance on the basis of the soaking solution could be related to the crystalline microstructures and morphologies of the formed TIPS-PEN crystals on the patterned PDMS surfaces because of the different evaporation rate of solvents. Therfore, we conjectured if solvents with a moderate evaporation speed is discovered, it can allow to improve the morphological and crystalline structures of the semiconductor onto the patterned PDMS pad, and lead to the enhanced electrical characteristics of the OTFTs, comparable to that in the single crystal OTFTs.

Table 1. The electrical properties of the OTFTs. For SiO_2 dielectric layer, the solvent in the bracket indicates the residual solvent on surfaces after spin coating of pure solvent.

Electrode	Dielectric layer	Soaking solution	μ ($cm^2V^{-1}s^{-1}$)	$I_{On/Off}$	V_T (V)
Si	SiO_2 (chlorobenezene)	1 wt% TIPS-PEN in chlorobenzene	0.095	~10^4	2.94
Si	SiO_2 (toluene)	1 wt% TIPS-PEN in chlorobenzene	0.108	~10^6	1.89
ITO glass	PMMA	1 wt% TIPS-PEN in chlorobenzene	0.027	~10^4	0.61
Si	PMMA	1 wt% TIPS-PEN in chlorobenzene	0.026	~10^4	0.69
Si	SiO_2 (toluene)	1 wt% TIPS-PEN in toluene	0.025	~10^5	3.96

In summary, we investigated a simple and novel technique to fabricate micropatterned TIPS-PEN semiconductors via the direct pattern transfer process using the TIPS-PEN/PDMS stamp. The patterned TIPS-PEN semiconductor films were directly transferred onto the organic/inorganic gate insulator surfaces at the desired region by stamping (contact and press) process. These transferred TIPS-PEN films were highly uniform and at least crystalline. A variety of pattern sizes ranging from 10 to 40 μm were transferred, and the rectangular-shaped patterns were also prepared without any etching process. The OTFTs with micropatterned semiconductors presented reliable device performance with an On/Off ratio and the field effect mobility of ~10^4 and ~0.1 $cm^2V^{-1}s^{-1}$ on the inorganic gate insulator and ~0.03 $cm^2V^{-1}s^{-1}$ on the organic gate insulator, respectively. We thought that the difference of electrical characteristics is originated from morphological structures of TIPS-PEN on the dielectric surfaces. We also described that the device could be manufactured the TIPS-PEN/PDMS stamp acquired in another solvent with faster evaporation rate. Its broad applicability indicates that our direct pattern transfer technique is very promising to fabricate solution-processed organic semiconductors for the integrated devices.

3. Experimental

Preparation of the TIPS-PEN/PDMS stamp: PDMS molds were fabricated by mixing PDMS prepolymer with crosslinker (Sylgard 184, Dow Corning Corp) at a ratio of 10:1 (w/w). The mixture was poured on pre-patterned Si masters and then cured at 80 °C for 4 hrs. After fully curing the PDMS mold, it can be simply peeled-off from the Si master mold. The PDMS molds with periodic lines had several sizes ranging from 10 to 40 μm. The rectangular pattern with length × width dimensions of 20 × 70 μm^2 was employed. The bottom surface of PDMS pad was attached to the glass after UVO treatment for 20min, and the PDMS/glass stamp was treated at 90 °C for 1 hr for stronger binding. 6,3-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN) (99.9 % purity) was purchased from Sigma-Aldrich, Korea. The micropatterned PDMS pad was immersed in 1 wt% TIPS-PEN/chlorobenzene (toluene) solution for 30-60 min. Then, the soaked solvent in PDMS pad was evaporated under vacuum for 3-5 hrs.

Direct pattern transfer Process: To transfer the TIPS-PEN crystals on the protruding regions of the PDMS stamp onto the substrates, we used Si wafer and ITO-glass (thickness: 120 nm, sheet resistance: 15 Ω/ cm^2) as a gate electrode and SiO_2 (200 nm-

thick thermal oxide) and 10 wt% PMMA in toluene as a gate insulator. All substrates were subjected to 10 min washes in acetone, and isopropyl alcohol, and then rinsed with distilled water before being dried with nitrogen. In order to facilitate the continuous TIPS-PEN crystal film on the substrates, the pure solvent (chlorobenzene or toluene) was coated on SiO_2 surface by spin-coating at 1500 rpm for 10 s, and 10 wt% PMMA solution (thickness ~ 500 nm) was coated on Si or ITO-glass by spin-coating at 3000 rpm for 30 s before conformal contact with the substrates. The TIPS-PEN/PDMS stamp was in conformal contact with Si/SiO_2, Si/PMMA, and ITO-glass/PMMA surfaces, and then pressed for a few second at 90 °C and detached

Characterization: Optical microscopy (Olympus BX41, Japan) and atomic force microscopy (SPA300HV, Japan) in tapping mode were used to observe the morphology of the transferred TIPS-PEN films on SiO_2 and PMMA gate dielectric layer after the removal of residual solvent in dielectric layer. To investigate the crystalline structure of TIPS-PEN, X-ray diffraction (Bruker D8 Discover, Germany) measurements were performed.

OTFT fabrication and characteristics: Au electrodes for source and drain (thickness = 100 nm, width = 1000 μm, length = 100 μm) was

thermally evaporated in ~3 × 10^{-6} Torr (5 Å/s) through a shadow mask on a patterned thin TIPS-PEN film. The electrical properties of the devices were measured using semiconductor systems. The current-voltage measurements were executed under ambient conditions using an Agilent 4155B semiconductor parameter analyzer. All electrical measurements were taken in dark ambient conditions.

4. Reference

[1] J. E. Anthony, *Chem. Rev.* 2006, *106*, 5028.

[2] G. Horowitz, *Adv. Mater.* 1998, *10*, 365.

[3] J. E. Anthony, J. S. Brooks, D. L. Eaton, S. R. Parkin, *J. Am. Chem. Soc.* 2001, *123*, 9482.

[4] J. Kim, J. Jeong, H. D. Cho, C. Lee, S. O. Kim, S.-K. Kwon, Y. Hong, *J. Phys. D: Appl. Phys.* 2009, *42*, 115107.

[5] S. K. Park, T. N. Jackson, J. E. Anthony, D. A. Mourey, *Appl. Phys. Lett.* 2007, *91*, 063514.

[6] D. H. Kim, D. Y. Lee, H. S. Lee, W. H. Lee, Y. H. Kim, J. I. Han, K. Cho, *Adv. Mater.* 2007, *19*, 678.

[7] J.-H. Kwon, S.-I. Shin, K.-H. Kim, M. J. Cho, K. N. Kim, D. H. Choi, B.-K. Ju, *Appl. Phys. Lett.* 2009, *94*, 013506.

[8] W. H. Lee, D. H. Kim, Y. Jang, J. H. Cho, M. Hwang, Y. D. Park, Y. H. Kim, J. I. Han, K. Cho, *Appl. Phys. Lett.* 2007, *90*, 132106.

[9] C. S. Kim, S. Lee, E. D. Gomez, J. E. Anthony, Y.--L. Loo, *Appl. Phys. Lett.* 2008, *93*, 103302.

[10] J.-P. Hong, A.-Y. Park, S. Lee, J. Kang, N. Shin, D. Y. Yoon, *Appl. Phys. Lett.* 2008, *92*, 143311.

[11] B. K. C. Kjellander, W. T. T. Smaal, J. E. Anthony, G. H. Gelinck, *Adv. Mater.* 2010, *22*, 4612.

[12] J. A. Lim, W. H. Lee, H. S. Lee, J. H. Lee, Y. D. Park, K. Cho, *Adv. Funct. Mater.* 2008, *18*, 229.

[13] C. W. Sele, B. K. C. Kjellander, B. Niesen, M. J. Thornton, J. B. P. H. van der Putten, K. Myny, H. J. Wondergem, A. Moser, R. Resel, A. J. J. M. van Breemen, N. van Aerle, P. Heremans, J. E. Anthony, G. H. Gelinck, *Adv. Mater.* 2009, *21*, 4926.

[14] R. Z. Rogowski, A. Dzwilewski, M. Kemerink, A. A. Darhuber, *J. Phys. Chem. C* 2011, *115*, 11758.

[15] Y.-H. Kim, Y. U. Lee, J.-I. Han, S.-M. Han, M.-K. Han, *J. Electrochem. Soc.* 2007, *154*, H995.

[16] K. N. Choi, K. S. Kim, K. S. Chung, H. Lee, *IEEE Trans. Device Mater. Reliab.* 2009, *9*, 489.

[17] X. Li, B. K. C. Kjellander, J. E. Anthony, C. W. M. Bastiaansen, D. J. Broer, G. H. Gelinck, *Adv. Funct. Mater.* 2009, *19*, 3610.

[18] S. C. B. Mannsfeld, A. Sharei, S. Liu, M. E. Roberts, I. McCulloch, M. Heeney, Z. Bao, *Adv. Mater.* 2008, *20*, 4044.

[19] R. W. I. de Boer, M. E. Gershenson, A. F. Morpurgo, V. Podzorov, *Phys. Stat. Sol.(a)* 2004, *201*, 1302.

[20] S. C. B. Mannsfeld, A. L. Briseno, S. Liu, C. Reese, M. E. Roberts, Z. Bao, *Adv. Funct. Mater.* 2007, *17*, 3545.

[21] V. C. Sundar, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willett, T. Someya, M. E. Gershenson, J. A. Rogers, *Science* 2004, *303*, 1644.

[22] K. C. Dickey, S. Subramanian, J. E. Anthony, L.-H. Han, S. Chen, Y.-L. Loo, *Appl. Phys. Lett.* 2007, *90*, 244103.

[23] S. Liu, W. M. Wang, A. L. Briseno, S. C. B. Mannsfeld, Z. Bao, *Adv. Mater.* 2009, *21*, 1217.

[24] S. Liu, W. M. Wang, S. C. B. Mannsfeld, J. Locklin, P. Erk, M. Gomez, F. Richter, Z. Bao, *Langmuir* 2007, *23*, 7428.

[25] I. Bae, S. J. Kang, Y. J. Shin, Y. J. Park, R. H. Kim, F. Mathevet, C. Park, *Adv. Mater.* 2011, *23*, 3398.

[26] S. H. Lee, M. H. Choi, S. H. Han, D. J. Choo, J. Jang, S. K. Kwon, *Org. Electron.* 2008, *9*, 721.

[27] H. S. Lee, D. Kwak, W. H. Lee, J. H. Cho, K. Cho, *J. Phys. Chem. C* 2010, *114*, 2329.

[28] H. Jia, G. K. Pant, E. K. Gross, R. M. Wallace, B. E. Gnade, *Org. Electron.* 2006, *7*, 16.

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