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M.S. THESIS

Extraction of Average Interface Trap Density using Capacitance-Voltage Characteristic at SiGe p-FinFET and Verification using Terman's Method

SiGe p-FinFET의 C-V 특성을 이용한 평균 계면 결함 밀도 추출과 Terman의 방법을 이용한 검증

BY

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February 2016

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE COLLEGE OF ENGINEERING

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2016 년 2 월

서울대학교 대학원
전기정보공학부
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김현수의 공학석사 학위논문을 인준함
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ABSTRACT

In this paper, it was proposed and verified by simulation that a new method can extract average interface trap density simply and accurately using difference between ideal capacitance-voltage curve and stretch-out capacitance curve with high interface trap density in SiGe p-FinFET.

Two capacitance-voltage curves, one is ideal and the other is stretch-out due to high interface trap density at interface of oxide layer and channel, in high frequency were found by SiGe p-FinFET simulation. Average interface trap density was extracted by using two capacitance-voltage curves and two methods at the same energy band region. One is Terman's method and the other is the method proposed in this paper using voltage difference between two capacitance-voltage curves.

Comparing the average interface trap density found by method using voltage difference with Terman's method, it was verified that

the method using voltage difference is reasonable to extract average interface trap density in SiGe p-FinFET with high interface trap density.

Keywords : Voltage difference, Interface trap density, SiGe, Terman's method, p-FinFET

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1. Introduction

Many researches are in progress to increase drive speed to have high carrier mobility by applying stress to the channel region or introducing new materials to enhance operation performance of CMOS [1~4]. As one of these researches, high hole mobility is required in channels to make p-type devices that have good drive current characteristics. Among several materials that have high hole mobility, SiGe shows outstanding drive current characteristics compared to Si in which it is being spotlighted as a material to substitute Si. However, the interface between the oxide layer and channel which is not optimized is still left as an obstacle to overcome to enhance performance [5]. For this reason, many researches are in progress to improve the characteristics of interface between the oxide layer and SiGe channel [6, 7].

Interface trap density is a significant factor used to understand

the interface condition and enhance device performance. Several methods are used to extract this interface trap density in which the method of using the difference between the low frequency and high frequency capacitances and conductance method are the representative methods that use capacitance-voltage curve characteristics. The Terman's method, which uses the high frequency capacitance-voltage curve among capacitance-voltage curve using methods, is a method used to extract the interface trap density that exists to the regions close to the conduction band and valence band in the forbidden band [8].

This paper focused on the point that devices that use SiGe as channel material can have very high interface trap density. Compared with the ideal capacitance-voltage curve, the depletion and strong inversion region of the capacitance-voltage curve in high frequency with high interface trap density show noticeable stretch-out characteristic in the voltage axis. The degree of relative stretch-out can be found by the difference of voltages in comparison between the stretch-out capacitance-voltage curve

and ideal capacitance-voltage curve, and the average interface trap density could be extracted between the energy band gap using the found voltage difference. To verify the validity of average interface trap density extracted by the voltage difference between the ideal and stretch-out capacitance-voltage curves, the Terman's method that uses the stretch-out capacitance-voltage curve characteristic was used to extract interface trap density, and the average value of the extracted interface trap density was found. By comparing the average interface trap density by the two methods, validity of the average interface trap density extracted by the voltage difference between the two curves was proved.

2. Device structure and simulation

The SiGe p-FinFET structure was simulated using Sentaurus 3D TCAD [9]. The density-gradient model used when considering the quantum effect of the channel, and the band gap narrowing effect and fermi statistics model were used when considering intrinsic carrier density. The hydrodynamic model and shockley-read-hall model were included to consider current density and generation-recombination. The philips unified mobility model and high-field saturation model were used to consider mobility.

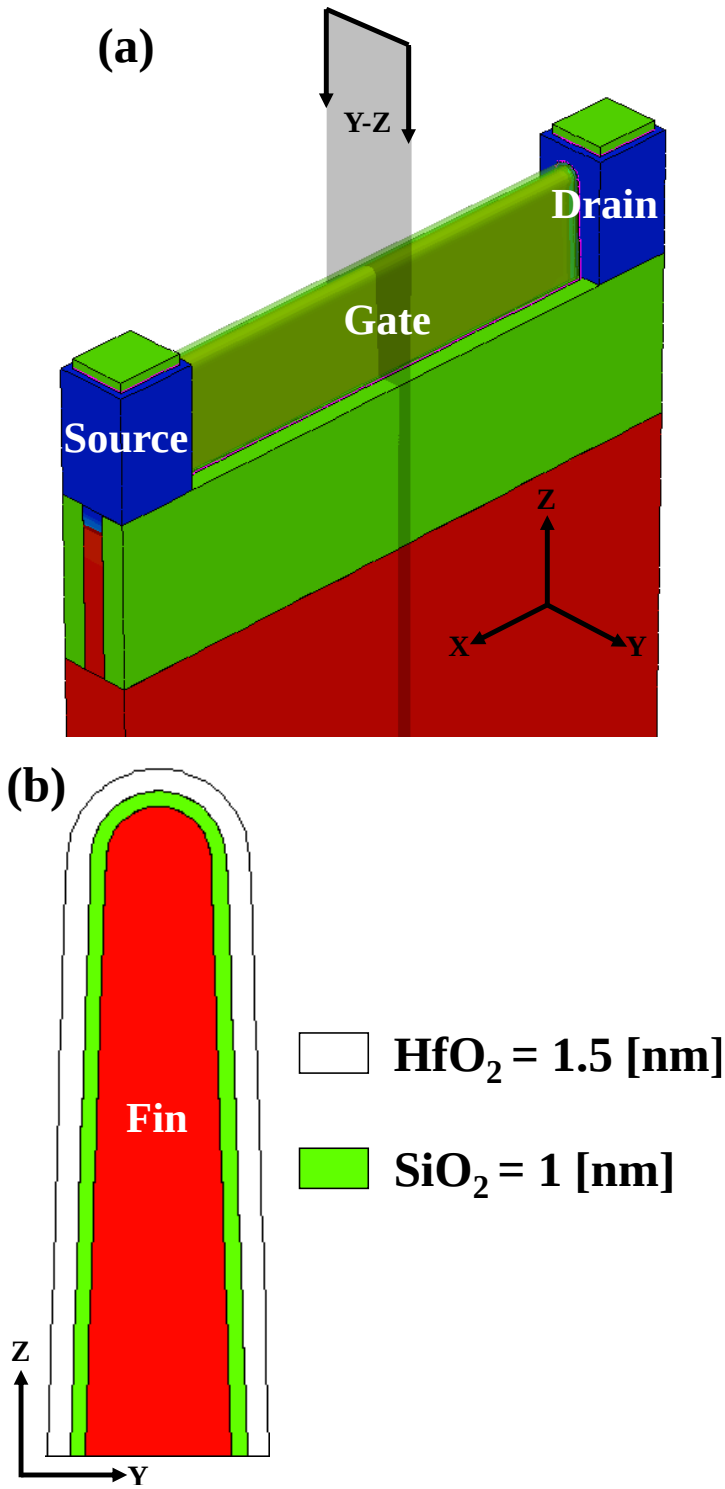

Figure 1. (a) Three-dimensional structure of SiGe p-FinFET.

(b) Sectional view of Fin.

Table 1. Data of SiGe p-FinFET structure.

L_g [nm]	200
Channel Doping [cm^{-3}]	$1x10^{17}$
S/D Doping [cm^{-3}]	$1x10^{20}$
EOT [nm]	1.25
Work Function [eV]	4.6
Channel Si/Ge Rate [%]	75/25

Table 2. Simulation parameter of SiGe.

E_g [eV]	0.94
Electron Affinity [eV]	4.054
n_i [cm^{-3}]	$3x10^{11}$

Figure 1 shows the simulation structure used in the paper, Table 1 shows the data on the structure, and Table 2 shows the parameters of the SiGe material. Figure 2 is the simulated split C-V curve of the structure in Figure 1 [10]. The capacitance by electrons and holes can be respectively separated in the split C-V. Capacitance drastically increases according to gate voltage in the accumulation region and strong inversion region where electron and hole density rapidly changes, but responsiveness according to gate voltage is small in other regions. The solid lines in Figure 2 are the ideal C-V curves which is in pure condition without interface trap between the oxide layer and channel. The dotted lines show the C-V curves with simulated high interface trap density, which are shown in the red line in Figure 3, were distributed in the interface between the oxide layer and channel.

The maximum capacitance value of the ideal C-V curve in Figure 2 can be seen by the oxide capacitance. The device was considered as a 3D structure, but the theoretical oxide capacitance value, which is the relation between permittivity and oxide thickness, is

$4.6x10^{-16}$ F in which it was similar to the maximum capacitance value of the ideal C−V curve in Figure 2 which was $4.5x10^{-16}$ F. The interface trap density distribution can spatially change because it has 3D structure, but this paper focuses on finding the average interface trap density rather than the spatial interface trap density. Therefore it was assumed that the interface trap density was spatially, uniformly distributed as shown in the red solid lines in Figure 3 in the FinFET structure in Figure 1.

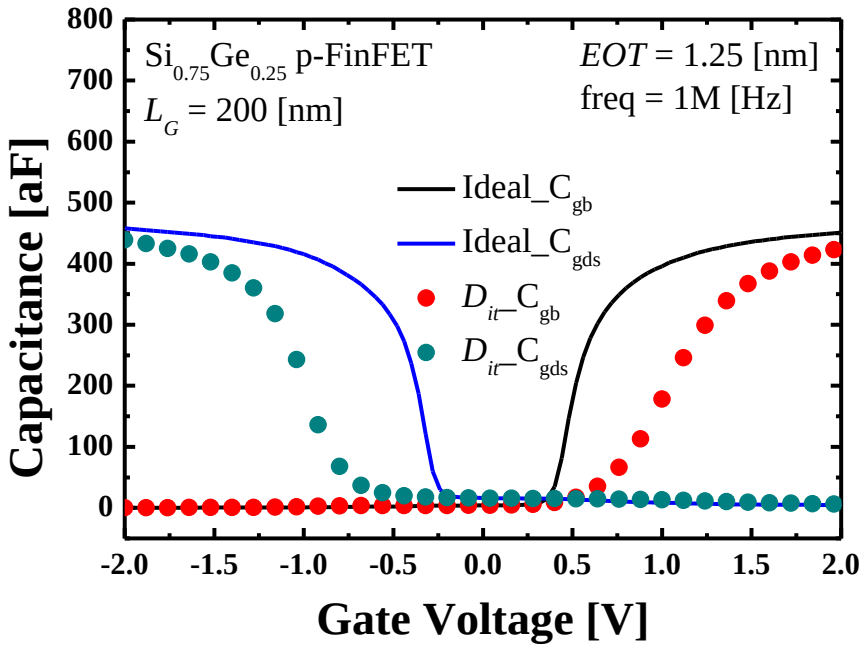

Figure 2. Simulation C-V curve of SiGe p-FinFET.

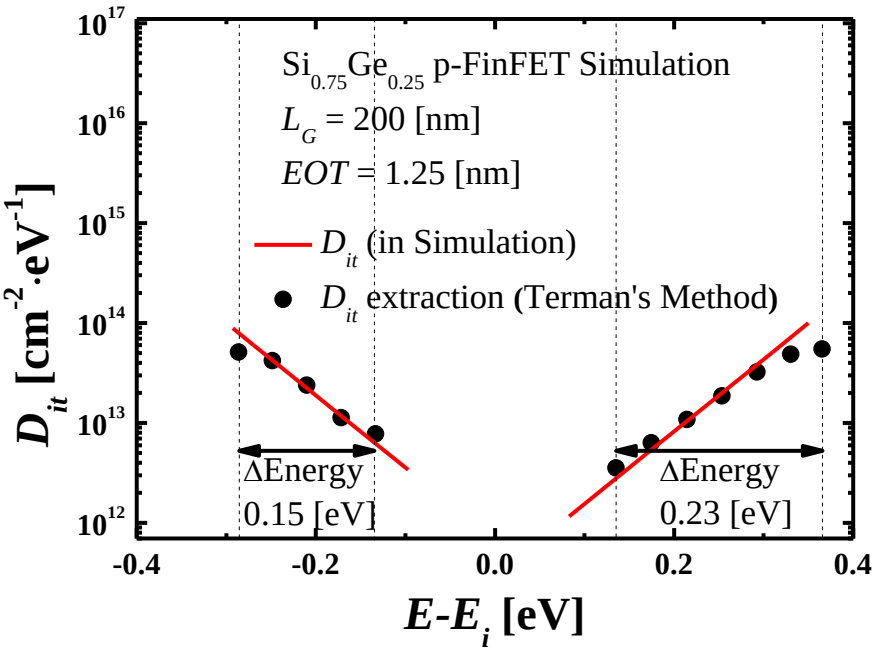

Figure 3. Interface trap density inputted in simulation (red line) and extracted by Terman's method (black dotted line).

3. Extraction of interface trap density

When the frequency of AC signals applied to the gate is low, interface trap adds capacitance components due to the characteristics of trapping or de-trapping of electrons in the interface trap. Due to the reason above, a hump is generated in the C-V curve. However, interface trap do not react to AC signals and react to DC gate voltage when high frequency AC signals are applied to the gate. DC gate voltage changes the surface potential and this change of potential changes the location of Fermi level. Electrons are trapped by interface trap in locations lower than the fermi level in which the amount of electrons trapped by the interface traps changes according to the location of fermi level in high frequency DC signals. Thus, the electrons trapped in the

interface trap influence the surface potential to show a stretch-out C-V curve compared to the ideal C-V curve as shown in Figure 2. Looking into the C-V curve in high frequency AC signals, the C-V curve is not dependent to the responsiveness of interface trap unlike low frequency AC signals in which slow interface trap can sufficiently contribute in trapping electrons. Therefore, interface trap density higher than other methods can be extracted by using the stretch-out characteristics of C-V curve in high frequency.

3.1. Extraction of interface trap density using the Terman's method

The Terman's method [11,12] is also called as the high frequency C-V method and uses the stretch-out characteristics of C-V curve of high frequency due to interface trap as explained above. In Figure 2 where the ideal C-V curve and C-V curve showing stretch-out characteristics due to interface trap are compared, surface potential is equivalent if the capacitance is the same despite of different voltage. Using this fact, the voltage difference of same capacitance between the ideal C-V curve and stretch-out C-V curve can be found as Equation (2). The surface potential that changes according to gate voltage can be found by using Equation (1) and the ideal C-V curve. In Equation (1), D is

the integration constant and can be made 0 by considering flat band voltage. Using this surface potential, distribution of interface trap density existing in the energy band gap can be shown according to the energy band. Then, the difference of gate voltages found in Equation (2) can be expressed as a function of surface potential like Equation (3) and the interface trap density can be found by using Equation (3). Figure 3 is based on the intrinsic Fermi level(E_i) in the energy band gap(E_g) in which the negative direction is close to the valence band(E_v) and the positive direction is close to the conduction band(E_c). The black dotted line in Figure (3) is the interface trap density extracted by Equation (3). It was seen that this well corresponded to the red lines in Figure (3).

$$\phi_s = \int_{V_{G1}}^{V_{G2}} (1 - C/C_{ox}) dV_G + D \quad (1)$$

$$\Delta V_G = V_{G,D_{it}} - V_{G,ideal} \quad (2)$$

$$D_{it,Terman} = \frac{C_{ox}}{q}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_S}{q} = \frac{C_{ox}}{q}\frac{d\Delta V_G}{d\phi_s} \quad (3)$$

$$D_{it,\Delta V} = \frac{C_{ox}}{q}\frac{\left(\Delta V_{D_{it}} - \Delta V_{ideal}\right)}{\Delta Energy} \quad (4)$$

3.2. Extraction of average interface trap density using voltage difference

Like the Terman's method that was referred above, the method extracting interface trap density using voltage difference also uses the stretch-out characteristics of the inversion and depletion regions in the interface trap existing C-V curve. Figure 4. (a) shows the C-V curve between the gate and drain/source of the inversion region of a SiGe p-FinFET and Figure 4. (b) shows the C-V curve between the gate and substrate of the depletion region. For comparison with the Terman's method, average interface trap density was extracted from the same energy band. Like the Terman's method, the fact was used that the surface potential is equivalent if the capacitance is the same.

$\triangle V_{ideal}$ in Figure 4. (a) and (b) are the voltage regions where interface trap density were found by the Terman's method in the energy band in Figure 3. Using Equation (1), it could be found that C_{gds} in the ideal C-V curve at the −0.24 V ~ −0.08 V corresponds to the energy band of −0.28 eV ~ −0.13 eV and C_{gb} in the 0.2 V ~ 0.44 V voltage interval corresponds to the energy band of 0.135 eV ~ 0.365 eV. $\triangle V_{Dit}$ of the stretch-out C-V curve can be found by using the C_{gds} values at −0.24 V and −0.08 V, and capacitance values corresponding to the C_{gb} values at 0.2 V and 0.44 V from the ideal C-V curve. Through this method, the values of $\triangle V_{ideal}$ of C_{gds}, $\triangle VD_{it}$ of C_{gds}, $\triangle V_{ideal}$ of C_{gb}, and $\triangle V_{Dit}$ of C_{gb} were shown to be 0.16 V, 0.415 V, 0.24 V and 0.59 V, respectively as shown in Figure 4. (a) and (b).

Wider voltage interval of same capacitance values than the voltage interval in the ideal C-V curve means that the C-V curve

shows stretch-out characteristics due to interface trap density in the energy band and the average interface trap density existing in the energy band can be found by Equation (4). △Energy in Equation (4) is the energy band of desired average interface trap density and the oxide capacitance can be found by permittivity and oxide layer thickness. The value of stretch-out characteristics of C-V curve due to interface trap density can be found by the difference between $\triangle V_{Dit}$ and $\triangle V_{ideal}$.

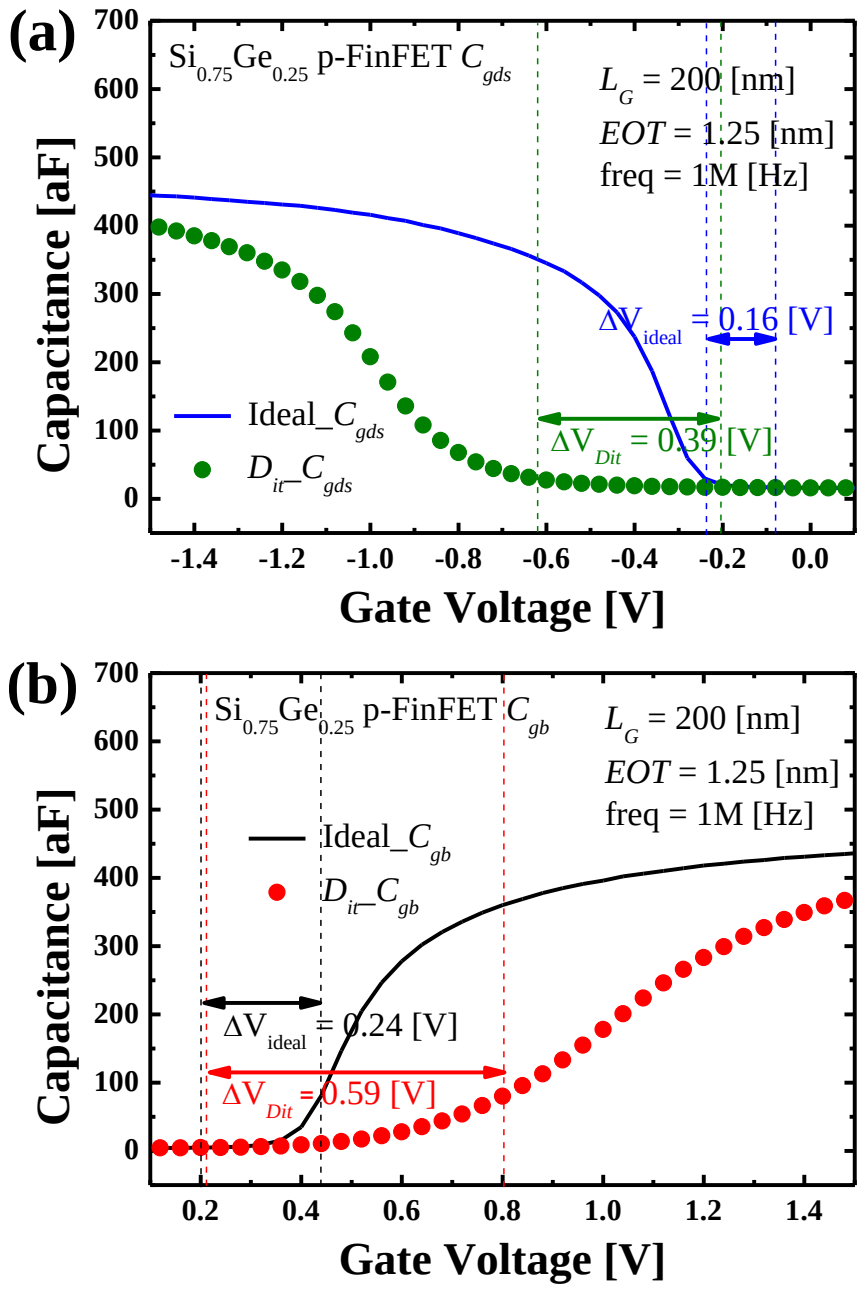

Figure 4. Comparison of voltage difference between ideal and stretch-out C-V curve (a) C_{gds} and (b) C_{gb}.

4. Conclusion

Average interface trap density existing in the energy band gap was found using Equation (4) and was also found by the Terman's method to compare average interface trap density. Average value was found by integrating interface trap density at the energy band gap and the average interface trap density found by the two methods are shown in Table 3. As seen in the results of Table 3, average interface trap density was found to have values very similar to the Terman's method in the same energy band even with simple voltage difference.

Interface trap density could be found using the high frequency ideal C-V curve and stretch-out C-V curve. Devices using SiGe have very poor interface condition and this poor interface condition causes the high frequency C-V curve to stretch out. In finding high interface trap density, the Terman's method allows more accurate

interface trap density distribution according to energy band, but there is inconvenience that voltages and surface potentials must be repetitively extracted from each capacitance with different values. On the other hand, when using the method, voltage difference mentioned in this paper, average interface trap density distributed in the energy band gap can be extracted simply and accurately. As a result, it was verified that method using voltage difference is reasonable to extract average interface trap density in SiGe p-FinFET with high density interface trap.

The Terman's method and voltage difference using method both require ideal C-V curves. However, it is difficult to gain these ideal curves in actual devices. In these situations, a structure that is very close to the actual device can be made through simulation to extract the ideal C-V curve in which it can become an outstanding alternative in the difficulty above when used in analysis of device characteristics.

In this study, the measurements were substituted to simulation. However, actually measured data should be included in analysis

along with the ideal C-V curves extracted by simulation to prove valid conclusions in future work.

Table 3. Average interface trap density extracted by Terman's method and voltage difference.

	C_{gds}	C_{gb}
ΔEnergy $(E-E_i)$ [eV]	0.15 (−0.28 ~ −0.13)	0.23 (0.135 ~ 0.365)
$D_{it,\Delta V}$ $[cm^{-2}\cdot eV^{-1}]$	$2.9x10^{13}$	$2.6x10^{13}$
$D_{it,Terman}$ $[cm^{-2}\cdot eV^{-1}]$	$3x10^{13}$	$2.9x10^{13}$

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초 록

SiGe p-FinFET의 C-V 특성을 이용한 평균 계면 결함 밀도 추출과 Terman의 방법을 이용한 검증

성 명 : 김 현 수

학과 및 전공 : 전기정보공학부

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이 논문에서는, SiGe p-FinFET의 이상적인 커패시턴스-전압 곡선과 높은 계면 결함 밀도에 의하여 늘어진 커패시턴스 전압 곡선의 차이를 이용하여 간편하고 정확하게 평균 계면 결함 밀도를 추출할 수 있는 새로운 방법을 제안하고 시뮬레이션을 이용하여 증명하였다.

우선, SiGe p-FinFET 시뮬레이션에서 높은 주파수의 이상적인 커패시턴스-전압 곡선과 산화막과 채널의 계면에 높은 계면 결함 밀도가 존재하여 늘어진 커패시턴스-전압 곡선을 구하였다. 시뮬레이션으로 구한 두 가지 곡선을 이용하여 Terman의 방법과 이 논문에서 고안된 두 곡

선의 전압 차이를 이용한 방법으로 동일한 에너지 밴드 영역에서 평균 계면 결함 밀도를 추출하였다.

이 논문에서 제안된 두 곡선의 전압 차이를 이용하여 추출한 평균 계면 결함 밀도를 Terman의 방법으로 추출한 평균 계면 밀도와 비교하여, 전압 차이를 이용하여 추출한 평균 계면 결함 밀도가 높은 계면 결함 농도를 갖는 SiGe p-FinFET에서 평균 계면 결함 농도를 추출하기에 적합하다는 것을 증명하였다.

주요어 : 전압차이, 계면 결함 밀도, SiGe, Terman의 방법, p-FinFET

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김현수의 공학석사 학위논문을 인준함
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위 원 장 김 수 환 (인)

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ABSTRACT

In this paper, it was proposed and verified by simulation that a new method can extract average interface trap density simply and accurately using difference between ideal capacitance-voltage curve and stretch-out capacitance curve with high interface trap density in SiGe p-FinFET.

Two capacitance-voltage curves, one is ideal and the other is stretch-out due to high interface trap density at interface of oxide layer and channel, in high frequency were found by SiGe p-FinFET simulation. Average interface trap density was extracted by using two capacitance-voltage curves and two methods at the same energy band region. One is Terman's method and the other is the method proposed in this paper using voltage difference between two capacitance-voltage curves.

Comparing the average interface trap density found by method using voltage difference with Terman's method, it was verified that

the method using voltage difference is reasonable to extract average interface trap density in SiGe p-FinFET with high interface trap density.

Keywords : Voltage difference, Interface trap density, SiGe, Terman's method, p-FinFET

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1. Introduction

Many researches are in progress to increase drive speed to have high carrier mobility by applying stress to the channel region or introducing new materials to enhance operation performance of CMOS [1~4]. As one of these researches, high hole mobility is required in channels to make p-type devices that have good drive current characteristics. Among several materials that have high hole mobility, SiGe shows outstanding drive current characteristics compared to Si in which it is being spotlighted as a material to substitute Si. However, the interface between the oxide layer and channel which is not optimized is still left as an obstacle to overcome to enhance performance [5]. For this reason, many researches are in progress to improve the characteristics of interface between the oxide layer and SiGe channel [6, 7].

Interface trap density is a significant factor used to understand

the interface condition and enhance device performance. Several methods are used to extract this interface trap density in which the method of using the difference between the low frequency and high frequency capacitances and conductance method are the representative methods that use capacitance-voltage curve characteristics. The Terman's method, which uses the high frequency capacitance-voltage curve among capacitance-voltage curve using methods, is a method used to extract the interface trap density that exists to the regions close to the conduction band and valence band in the forbidden band [8].

This paper focused on the point that devices that use SiGe as channel material can have very high interface trap density. Compared with the ideal capacitance-voltage curve, the depletion and strong inversion region of the capacitance-voltage curve in high frequency with high interface trap density show noticeable stretch-out characteristic in the voltage axis. The degree of relative stretch-out can be found by the difference of voltages in comparison between the stretch-out capacitance-voltage curve

and ideal capacitance-voltage curve, and the average interface trap density could be extracted between the energy band gap using the found voltage difference. To verify the validity of average interface trap density extracted by the voltage difference between the ideal and stretch-out capacitance-voltage curves, the Terman's method that uses the stretch-out capacitance-voltage curve characteristic was used to extract interface trap density, and the average value of the extracted interface trap density was found. By comparing the average interface trap density by the two methods, validity of the average interface trap density extracted by the voltage difference between the two curves was proved.

2. Device structure and simulation

The SiGe p-FinFET structure was simulated using Sentaurus 3D TCAD [9]. The density-gradient model used when considering the quantum effect of the channel, and the band gap narrowing effect and fermi statistics model were used when considering intrinsic carrier density. The hydrodynamic model and shockley-read-hall model were included to consider current density and generation-recombination. The philips unified mobility model and high-field saturation model were used to consider mobility.

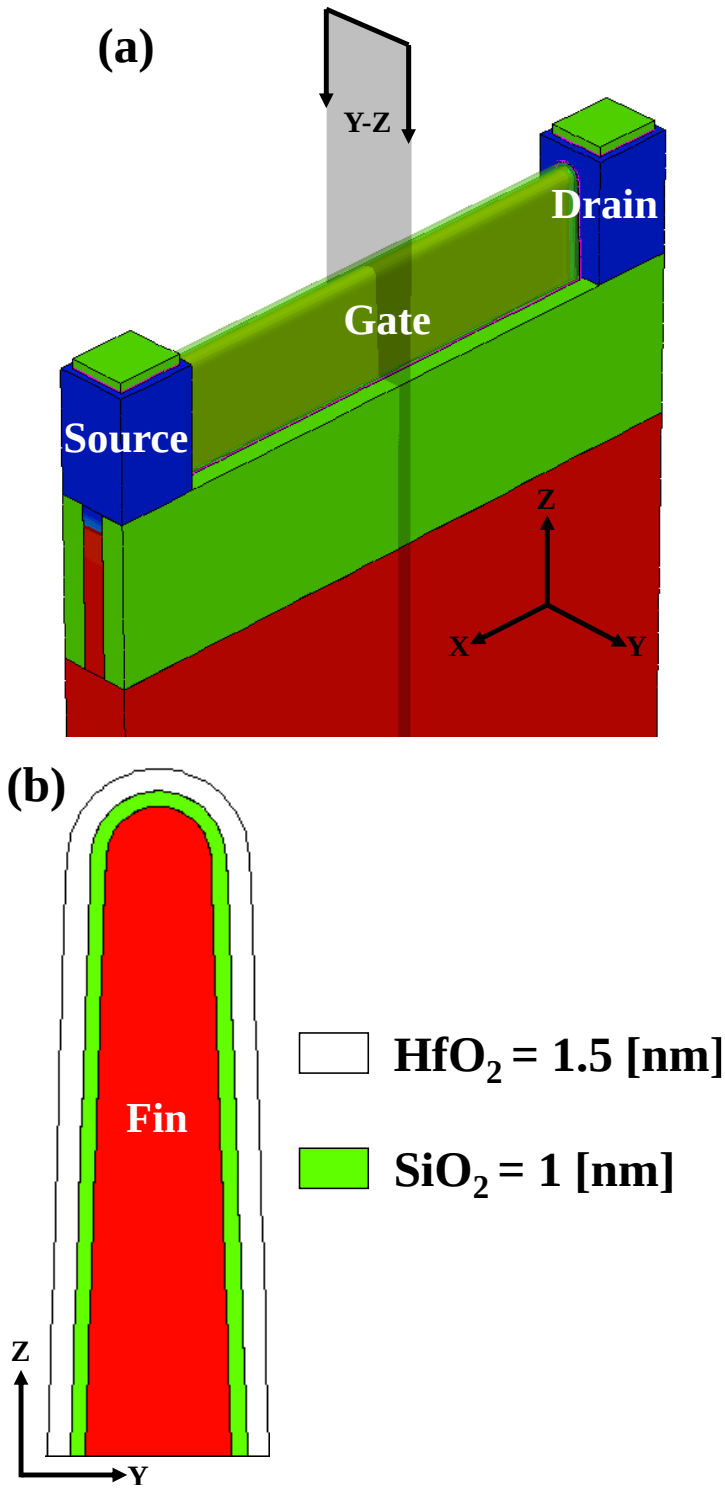

Figure 1. (a) Three-dimensional structure of SiGe p-FinFET.

(b) Sectional view of Fin.

Table 1. Data of SiGe p-FinFET structure.

L_g [nm]	200
Channel Doping [cm^{-3}]	$1x10^{17}$
S/D Doping [cm^{-3}]	$1x10^{20}$
EOT [nm]	1.25
Work Function [eV]	4.6
Channel Si/Ge Rate [%]	75/25

Table 2. Simulation parameter of SiGe.

E_g [eV]	0.94
Electron Affinity [eV]	4.054
n_i [cm^{-3}]	$3x10^{11}$

Figure 1 shows the simulation structure used in the paper, Table 1 shows the data on the structure, and Table 2 shows the parameters of the SiGe material. Figure 2 is the simulated split C-V curve of the structure in Figure 1 [10]. The capacitance by electrons and holes can be respectively separated in the split C-V. Capacitance drastically increases according to gate voltage in the accumulation region and strong inversion region where electron and hole density rapidly changes, but responsiveness according to gate voltage is small in other regions. The solid lines in Figure 2 are the ideal C-V curves which is in pure condition without interface trap between the oxide layer and channel. The dotted lines show the C-V curves with simulated high interface trap density, which are shown in the red line in Figure 3, were distributed in the interface between the oxide layer and channel.

The maximum capacitance value of the ideal C-V curve in Figure 2 can be seen by the oxide capacitance. The device was considered as a 3D structure, but the theoretical oxide capacitance value, which is the relation between permittivity and oxide thickness, is

$4.6x10^{-16}$ F in which it was similar to the maximum capacitance value of the ideal C−V curve in Figure 2 which was $4.5x10^{-16}$ F. The interface trap density distribution can spatially change because it has 3D structure, but this paper focuses on finding the average interface trap density rather than the spatial interface trap density. Therefore it was assumed that the interface trap density was spatially, uniformly distributed as shown in the red solid lines in Figure 3 in the FinFET structure in Figure 1.

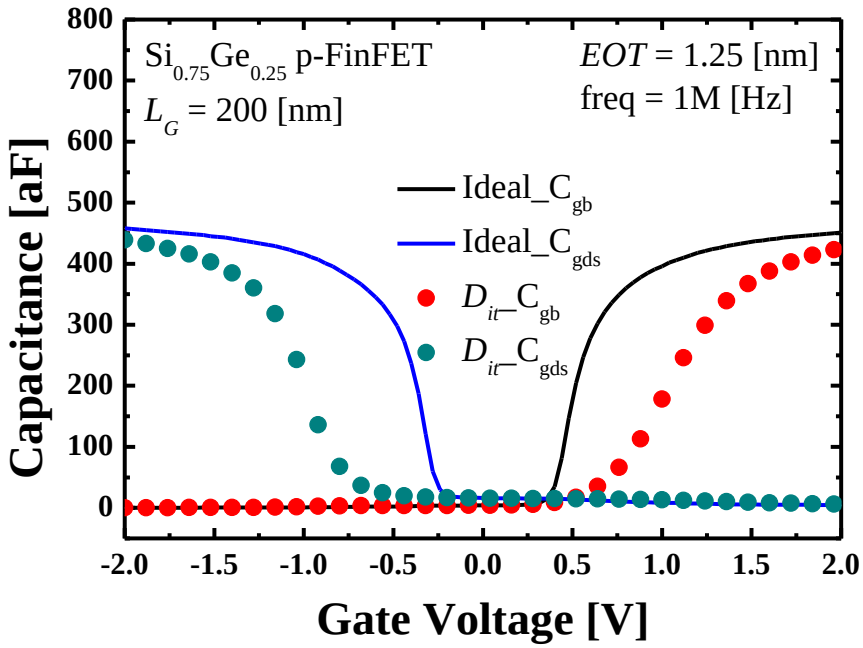

Figure 2. Simulation C-V curve of SiGe p-FinFET.

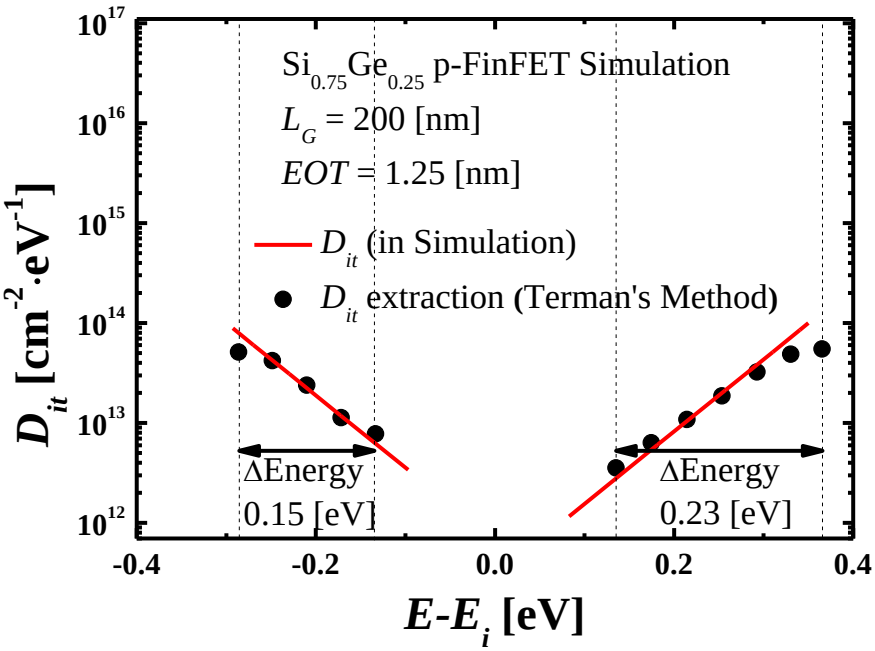

Figure 3. Interface trap density inputted in simulation (red line) and extracted by Terman's method (black dotted line).

3. Extraction of interface trap density

When the frequency of AC signals applied to the gate is low, interface trap adds capacitance components due to the characteristics of trapping or de-trapping of electrons in the interface trap. Due to the reason above, a hump is generated in the C-V curve. However, interface trap do not react to AC signals and react to DC gate voltage when high frequency AC signals are applied to the gate. DC gate voltage changes the surface potential and this change of potential changes the location of Fermi level. Electrons are trapped by interface trap in locations lower than the fermi level in which the amount of electrons trapped by the interface traps changes according to the location of fermi level in high frequency DC signals. Thus, the electrons trapped in the

interface trap influence the surface potential to show a stretch-out C-V curve compared to the ideal C-V curve as shown in Figure 2. Looking into the C-V curve in high frequency AC signals, the C-V curve is not dependent to the responsiveness of interface trap unlike low frequency AC signals in which slow interface trap can sufficiently contribute in trapping electrons. Therefore, interface trap density higher than other methods can be extracted by using the stretch-out characteristics of C-V curve in high frequency.

3.1. Extraction of interface trap density using the Terman's method

The Terman's method [11,12] is also called as the high frequency C-V method and uses the stretch-out characteristics of C-V curve of high frequency due to interface trap as explained above. In Figure 2 where the ideal C-V curve and C-V curve showing stretch-out characteristics due to interface trap are compared, surface potential is equivalent if the capacitance is the same despite of different voltage. Using this fact, the voltage difference of same capacitance between the ideal C-V curve and stretch-out C-V curve can be found as Equation (2). The surface potential that changes according to gate voltage can be found by using Equation (1) and the ideal C-V curve. In Equation (1), D is

the integration constant and can be made 0 by considering flat band voltage. Using this surface potential, distribution of interface trap density existing in the energy band gap can be shown according to the energy band. Then, the difference of gate voltages found in Equation (2) can be expressed as a function of surface potential like Equation (3) and the interface trap density can be found by using Equation (3). Figure 3 is based on the intrinsic Fermi level(E_i) in the energy band gap(E_g) in which the negative direction is close to the valence band(E_v) and the positive direction is close to the conduction band(E_c). The black dotted line in Figure (3) is the interface trap density extracted by Equation (3). It was seen that this well corresponded to the red lines in Figure (3).

$$\phi_s = \int_{V_{G1}}^{V_{G2}} (1 - C/C_{ox}) dV_G + D \quad (1)$$

$$\Delta V_G = V_{G,D_{it}} - V_{G,ideal} \quad (2)$$

$$D_{it,Terman} = \frac{C_{ox}}{q}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_S}{q} = \frac{C_{ox}}{q}\frac{d\Delta V_G}{d\phi_s} \quad (3)$$

$$D_{it,\Delta V} = \frac{C_{ox}}{q}\frac{\left(\Delta V_{D_{it}} - \Delta V_{ideal}\right)}{\Delta Energy} \quad (4)$$

3.2. Extraction of average interface trap density using voltage difference

Like the Terman's method that was referred above, the method extracting interface trap density using voltage difference also uses the stretch-out characteristics of the inversion and depletion regions in the interface trap existing C-V curve. Figure 4. (a) shows the C-V curve between the gate and drain/source of the inversion region of a SiGe p-FinFET and Figure 4. (b) shows the C-V curve between the gate and substrate of the depletion region. For comparison with the Terman's method, average interface trap density was extracted from the same energy band. Like the Terman's method, the fact was used that the surface potential is equivalent if the capacitance is the same.

$\triangle V_{ideal}$ in Figure 4. (a) and (b) are the voltage regions where interface trap density were found by the Terman's method in the energy band in Figure 3. Using Equation (1), it could be found that C_{gds} in the ideal C-V curve at the −0.24 V ~ −0.08 V corresponds to the energy band of −0.28 eV ~ −0.13 eV and C_{gb} in the 0.2 V ~ 0.44 V voltage interval corresponds to the energy band of 0.135 eV ~ 0.365 eV. $\triangle V_{Dit}$ of the stretch-out C-V curve can be found by using the C_{gds} values at −0.24 V and −0.08 V, and capacitance values corresponding to the C_{gb} values at 0.2 V and 0.44 V from the ideal C-V curve. Through this method, the values of $\triangle V_{ideal}$ of C_{gds}, $\triangle VD_{it}$ of C_{gds}, $\triangle V_{ideal}$ of C_{gb}, and $\triangle V_{Dit}$ of C_{gb} were shown to be 0.16 V, 0.415 V, 0.24 V and 0.59 V, respectively as shown in Figure 4. (a) and (b).

Wider voltage interval of same capacitance values than the voltage interval in the ideal C-V curve means that the C-V curve

shows stretch-out characteristics due to interface trap density in the energy band and the average interface trap density existing in the energy band can be found by Equation (4). △Energy in Equation (4) is the energy band of desired average interface trap density and the oxide capacitance can be found by permittivity and oxide layer thickness. The value of stretch-out characteristics of C-V curve due to interface trap density can be found by the difference between $\triangle V_{Dit}$ and $\triangle V_{ideal}$.

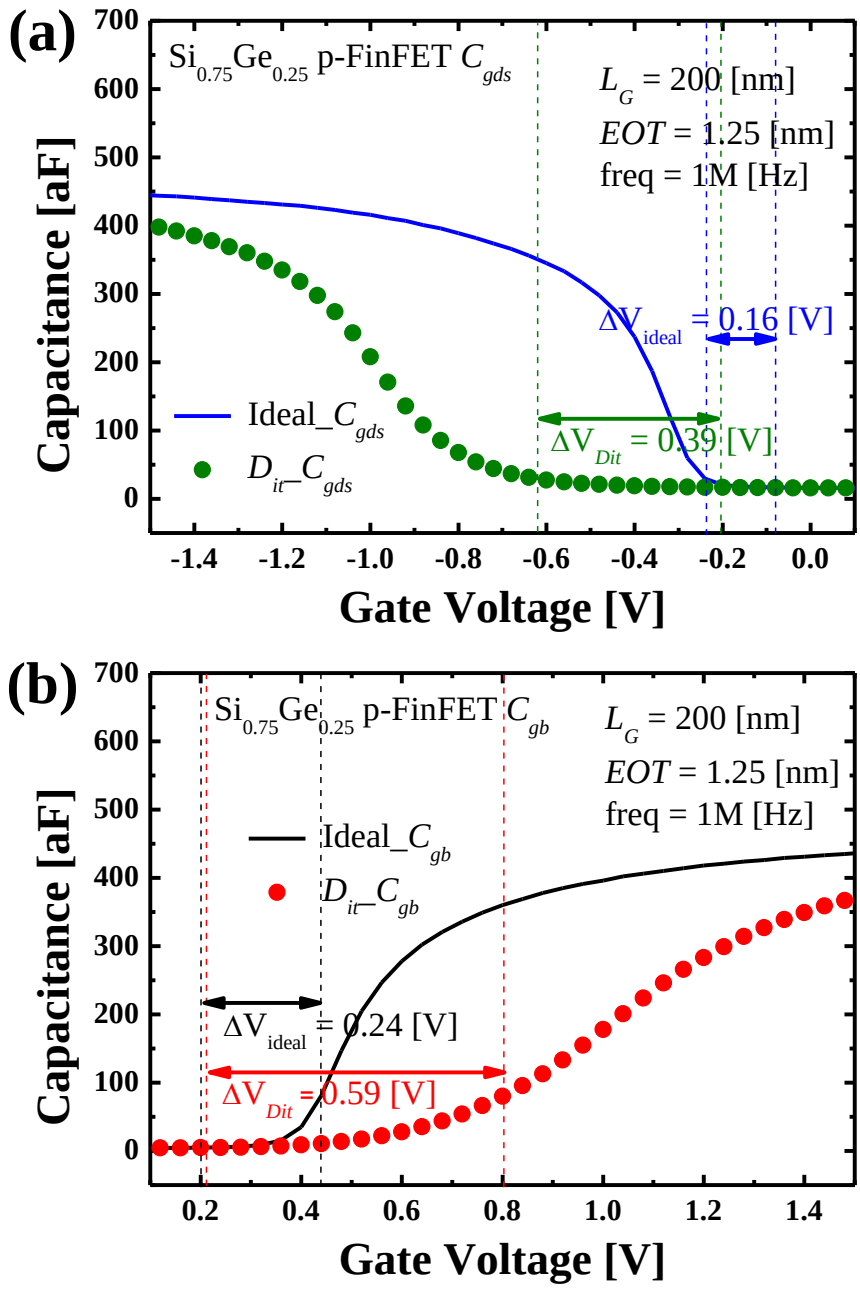

Figure 4. Comparison of voltage difference between ideal and stretch-out C-V curve (a) C_{gds} and (b) C_{gb}.

4. Conclusion

Average interface trap density existing in the energy band gap was found using Equation (4) and was also found by the Terman's method to compare average interface trap density. Average value was found by integrating interface trap density at the energy band gap and the average interface trap density found by the two methods are shown in Table 3. As seen in the results of Table 3, average interface trap density was found to have values very similar to the Terman's method in the same energy band even with simple voltage difference.

Interface trap density could be found using the high frequency ideal C-V curve and stretch-out C-V curve. Devices using SiGe have very poor interface condition and this poor interface condition causes the high frequency C-V curve to stretch out. In finding high interface trap density, the Terman's method allows more accurate

interface trap density distribution according to energy band, but there is inconvenience that voltages and surface potentials must be repetitively extracted from each capacitance with different values. On the other hand, when using the method, voltage difference mentioned in this paper, average interface trap density distributed in the energy band gap can be extracted simply and accurately. As a result, it was verified that method using voltage difference is reasonable to extract average interface trap density in SiGe p-FinFET with high density interface trap.

The Terman's method and voltage difference using method both require ideal C-V curves. However, it is difficult to gain these ideal curves in actual devices. In these situations, a structure that is very close to the actual device can be made through simulation to extract the ideal C-V curve in which it can become an outstanding alternative in the difficulty above when used in analysis of device characteristics.

In this study, the measurements were substituted to simulation. However, actually measured data should be included in analysis

along with the ideal C-V curves extracted by simulation to prove valid conclusions in future work.

Table 3. Average interface trap density extracted by Terman's method and voltage difference.

	C_{gds}	C_{gb}
ΔEnergy $(E-E_i)$ [eV]	0.15 (−0.28 ~ −0.13)	0.23 (0.135 ~ 0.365)
$D_{it,\Delta V}$ $[cm^{-2}\cdot eV^{-1}]$	$2.9x10^{13}$	$2.6x10^{13}$
$D_{it,Terman}$ $[cm^{-2}\cdot eV^{-1}]$	$3x10^{13}$	$2.9x10^{13}$

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초 록

SiGe p-FinFET의 C-V 특성을 이용한 평균 계면 결함 밀도 추출과 Terman의 방법을 이용한 검증

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이 논문에서는, SiGe p-FinFET의 이상적인 커패시턴스-전압 곡선과 높은 계면 결함 밀도에 의하여 늘어진 커패시턴스 전압 곡선의 차이를 이용하여 간편하고 정확하게 평균 계면 결함 밀도를 추출할 수 있는 새로운 방법을 제안하고 시뮬레이션을 이용하여 증명하였다.

우선, SiGe p-FinFET 시뮬레이션에서 높은 주파수의 이상적인 커패시턴스-전압 곡선과 산화막과 채널의 계면에 높은 계면 결함 밀도가 존재하여 늘어진 커패시턴스-전압 곡선을 구하였다. 시뮬레이션으로 구한 두 가지 곡선을 이용하여 Terman의 방법과 이 논문에서 고안된 두 곡

선의 전압 차이를 이용한 방법으로 동일한 에너지 밴드 영역에서 평균 계면 결함 밀도를 추출하였다.

이 논문에서 제안된 두 곡선의 전압 차이를 이용하여 추출한 평균 계면 결함 밀도를 Terman의 방법으로 추출한 평균 계면 밀도와 비교하여, 전압 차이를 이용하여 추출한 평균 계면 결함 밀도가 높은 계면 결함 농도를 갖는 SiGe p-FinFET에서 평균 계면 결함 농도를 추출하기에 적합하다는 것을 증명하였다.

주요어 : 전압차이, 계면 결함 밀도, SiGe, Terman의 방법, p-FinFET

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