M.S. THESIS

Analysis of dependence on oxide trap's location of RTN in GIDL current of DRAM cell transistors

DRAM 셀 트렌지스터의 GIDL RTN 에 의한 산화막 트랩의 위치 의존성 분석

BY

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DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

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지도교수 신 형 철

이 논문을 공학석사 학위논문으로 제출함

2014 년 2 월

서울대학교 대학원

전기컴퓨터공학부

콴뉴엔기아

콴뉴엔기아의 공학석사 학위논문을 인준함

2014 년 2 월

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Abstract

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As device dimensions are minimized, random telegraph noise (RTN) is dominant in determining the performance and reliability of metal-oxide-semiconductor field effect transistor (MOSFET). The origin of RTN is attributed to trapping/de-trapping of carriers in trap located in a gate oxide or at a Si/SiO_2 interface. Until now, most research on the characterization of an oxide trap investigates for the channel or gate leakage current and a few for gate-induced drain leakage current, a significant leakage component of current in modern MOSFETs which is mainly associated with both band-to-band or trap-assisted-tunneling in a gate to drain overlapped region. As a result, RTN in GIDL current is believed to be a cause of variable retention time in DRAM devices. Due to those reasons, there has been much interest regarding RTN in GIDL current. Previous authors have reported that oxide traps cause RTN in GIDL current from experimental work. For better understanding of characterization of oxide traps that lead to fluctuations of GIDL current, it is

necessary to obtain accurate information about the characterization of these traps.

In this thesis, we have developed an accurate model to represent the variation of GIDL current which depends on location of an oxide trap by all vertical, lateral and width direction, and expected the trap's position at the gate oxide. We also analyzed the amplitude of RTN in GIDL current as a function of the drain to gate voltage. Also, we investigated the characterization of the oxide trap with 20-nm Saddle MOSFET, a promising candidate for DRAM high-density applications.

Keywords

Gate-induced drain leakage (GIDL), random telegraph noise (RTN), Saddle MOSFET, location of an oxide trap, amplitude of $\Delta I_{GIDL}/I_{GIDL}$

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Contents

1. Introduction

As device dimensions are minimized, random telegraph noise (RTN) is dominant in determining the performance and reliability of metal-oxide-semiconductor field effect transistor (MOSFET). The origin of RTN is attributed to trapping/de-trapping of carriers in trap located in a gate oxide or at a Si/SiO_2 interface. Until now, most research on the characterization of an oxide trap investigates for the channel or gate leakage current and a few for gate-induced drain leakage current, a significant leakage component of current in modern MOSFETs which is mainly associated with both band-to-band or trap-assisted-tunneling in a gate to drain overlapped region. As a result, RTN in GIDL current is believed to be a cause of variable retention time in DRAM devices. Due to those reasons, there has been much interest regarding RTN in GIDL current. Previous authors have reported that oxide traps cause RTN in GIDL current from experimental work. For better understanding of characterization of oxide traps that lead to fluctuations of GIDL current, it is necessary to obtain accurate information about the characterization of these traps.

Chapter 2 is about gate-induced drain leakage current which significant effect the performance and reliability of memory cell transistors. Several

models of GIDL current were developed to planar MOSFET. We described a model for GIDL current included Trap-assisted tunneling and band-to-band tunneling and compared with the measurement data with the modeling data.

In chapter 3, the dependence both on the trap position of RTN in GIDL current and on drain to gate voltage of conventional n-MOSFET is provided. We extracted the possible trap position at the gate oxide from both simulation and measurement data.

In chapter 4, the investigation of RTN in GIDL current of 20-nm Saddle MOSFET, a promising candidate of high-density DRAM cell, is given. Especially, we analyze the effect of multi-traps with RTN in GIDL current.

2. Gate-Induced Drain Leakage (GIDL) Current

Gate-Induced Drain Leakage Current is one of the significant leakage current components, especially, determining data retention time of DRAMs. GIDL current is attributed to tunneling taking place in the deep depleted drain region underneath the gate oxide. GIDL current is mainly affected by the electric field at the gate to drain overlapped region.

For an n-MOSFET transistor with grounded gate and drain bias at Vd, significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electron are collected by the drain, resulting in GIDL current.

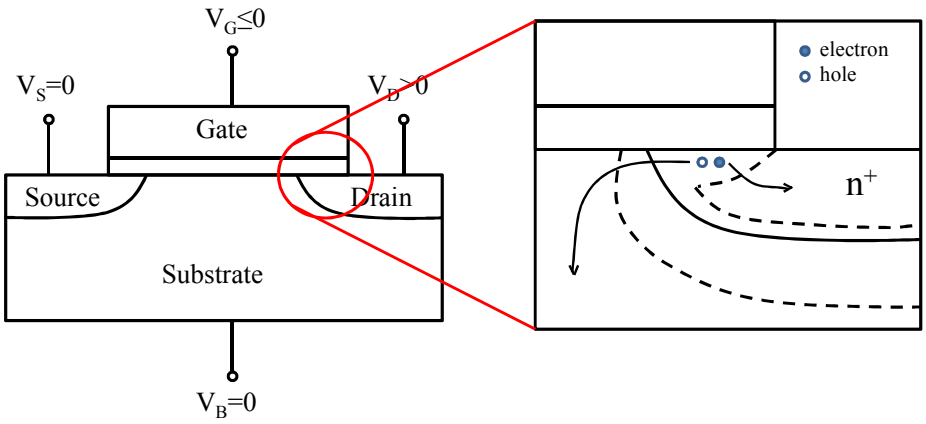


Figure 2.1: Cross-sectional view of planar n-MOSFET

The total GIDL current is obtained through the integration of the generation function over the structure:

$$I_{GIDL} = Wq\iint (R_{BBT} + R_{TAT})dxdy \qquad (2.1)$$

where W is the gate width.

Trap-assisted tunneling (TAT) and band-to-band tunneling (BBT) are the main mechanisms contributing to GIDL with proportions depending on electric field.

2.1 Band-to-band tunneling

Band to band tunneling is only possible in the presence of a high electric field and when the band bending is larger than the energy band gap E_g

[1]. The electric field in silicon at the interface also depends on the doping concentration in the diffusion region and the drain to gate voltage.

$$R_{net}^{bbt} = A \cdot D \cdot F^{P} \cdot \exp\left(-\frac{B.Eg(T)^{3/2}}{Eg(300)^{3/2} F} \right) \qquad (2.2)$$

2.2 Trap-assisted tunneling

Trap-assisted tunneling dominates under the condition of small electric field and its carriers enhances the Shockley-Read-Hall (SRH) generation of electron-hole pairs in space charge region. Trap-assisted tunneling is modeled by including Trap-assisted tunneling is modeled by including appropriate enhancement Γ_n^{Dirac} and Γ_p^{Dirac} in the trap lifetimes.

$$R_{TAT} = \frac{pn - n_i^2}{\frac{\tau_n}{1+\Gamma_{tat}}\left[p + n_i \exp\left(\frac{E_i - E_T}{kT} \right) \right] + \frac{\tau_p}{1+\Gamma_{tat}}\left[n + n_i \exp\left(\frac{E_T - E_i}{kT} \right) \right]} \qquad (2.3)$$

(3)

Field-effect factor:

$$\Gamma_{TAT} = \int_0^{\tilde{E}_n} \exp\left[u - \frac{2}{3} \frac{\sqrt{u^3}}{\tilde{E}} \right] du \quad (2.4)$$

An approximate for field-effect factor:

(4)

$$\Gamma_{TAT} = \begin{cases} \sqrt{\pi}\,\tilde{E}\cdot\exp\left[\frac{1}{3}\tilde{E}^{2}\right]\left\{2-erfc\left[\frac{1}{2}\left(\frac{\tilde{E}_n}{\tilde{E}}-\tilde{E}\right)\right]\right\} & E \le \sqrt{\tilde{E}_n} \\ \sqrt{\pi\,\tilde{E}}\cdot\tilde{E}_n^{\,1/4}\cdot\exp\left[-\tilde{E}_n+\tilde{E}\sqrt{\tilde{E}_n}+\frac{1}{3}\frac{\sqrt{\tilde{E}_n^{\,3}}}{\tilde{E}}\right] erfc\left[\tilde{E}_n^{\,1/4}\sqrt{\tilde{E}}-\tilde{E}_n^{\,3/4}/\sqrt{\tilde{E}}\right] & E > \sqrt{\tilde{E}_n} \end{cases}$$

(2.5)

2.3 Result and discussion

We performed the structure of 3D – n-MOSFET using TCAD Sentaurus tool to investigate GIDL current change with an electron trapped:

The width/length of transistor is 0.2/0.1 μm, the oxide thickness is 3.7 nm, the doping concentration of body is $1.4\text{x}10^{18}$ cm^{-3}, gate is n - type poly-si licon which has the doping concentration $5.8\text{x}10^{20}$ cm^{-3}, and the doping conce ntration of n^{+} region is $1\text{x}10^{20}$ cm^{-3}.

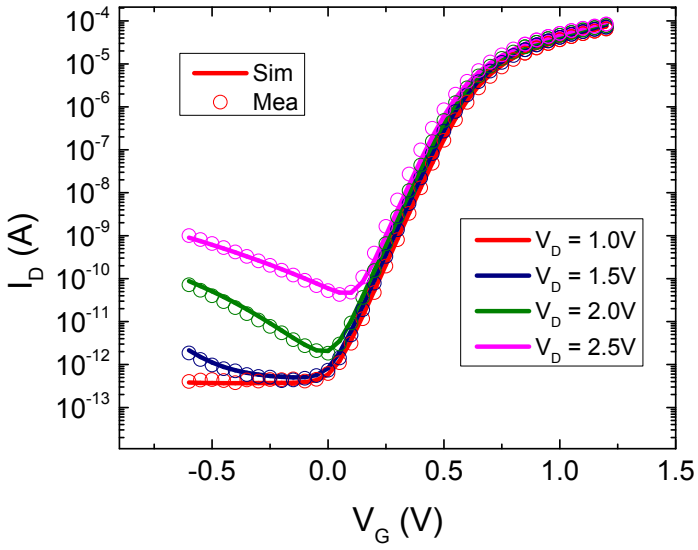


Figure 2.2: Fitting I_D-V_G curves between measurement data and simulation data

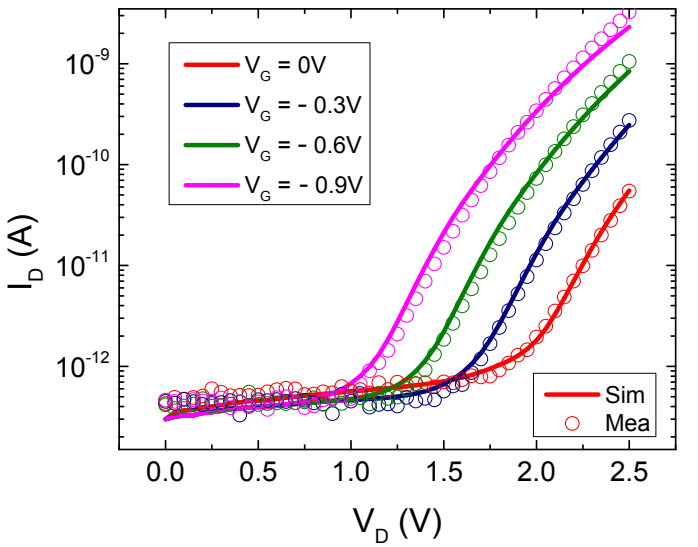


Figure 2.3: Fitting I_D – V_{DG} between measurement data and simulation data. The drain currents are GIDL current in case of negative gate bias.

GIDL current has two main components, band-to-band tunneling current and trap-assisted tunneling current. At high V_{DG}, GIDL current increases rapidly with increasing bias while at low V_{DG}, it changes a little. Data obtained by simulation fits well with measurement data.

3. Dependence on an oxide trap's position of Random Telegraph Noise (RTN) in GIDL current of n-MOSFET

Abstract

We investigated the variation of random telegraph noise (RTN) in gate-induced drain leakage (GIDL) current by changing location of a trap inside the gate oxide of n type metal-oxide semiconductor field effect transistor (n-MOSFET). The dependence on drain to gate bias was then considered. This approach has been assessed with Technology Computer Aided Designed (TCAD) simulations.

Keywords

Gate-induced drain leakage (GIDL), random telegraph noise (RTN), location of an oxide trap, amplitude of $\Delta I_{GIDL}/I_{GIDL}$

3.1 Introduction

As device dimensions are minimized, random telegraph noise (RTN) is dominant in determining the performance and reliability of metal-oxide-semiconductor field effect transistor (MOSFET). The origin of RTN is attributed to trapping/de-trapping of carriers in trap located in a gate oxide or at a Si/SiO_2 interface [2]- [3]. Until now, most research on the characterization of an oxide trap investigates for the channel or gate leakage current [4, 5, 6, 7, 8] and a few for gate-induced drain leakage current, a significant leakage component of current in modern MOSFETs which is mainly associated with both band-to-band or trap-assisted-tunneling in a gate to drain overlapped region [9]. As a result, RTN in GIDL current is believed to be a cause of variable retention time in DRAM devices [10]. Due to those reasons, there has been much interest regarding RTN in GIDL current. Previous authors have reported that oxide traps cause RTN in GIDL current from experimental work [11, 12, 13]. For better understanding of characterization of oxide traps that lead to fluctuations of GIDL current, it is necessary to obtain accurate information about the dependence on the location of these traps.

In this paper, we have developed an accurate model to represent the variation of GIDL current which depends on location of an oxide trap by all vertical, lateral and width direction, and analyzed the amplitude of RTN in GIDL current as a function of the drain to gate voltage.

3.2 Simulation Set-up and background

In the gate-to-drain overlapped region, if an electron is captured in an oxide trap, the electric field at the Si/SiO_2 interface is enhanced, as shown in Fig. 3.1. As the tunneling process can take place more easily due to the increased electric field, GIDL current is in high state when the trap is filled with an electron and GIDL current is low when the trap is empty [11]. The captured electron creates its own electric field that has the same direction with the vertical electric field from drain to gate, the main component leading to tunneling process. The amplitude of an electron's electric field is inversely proportional with square of distance.

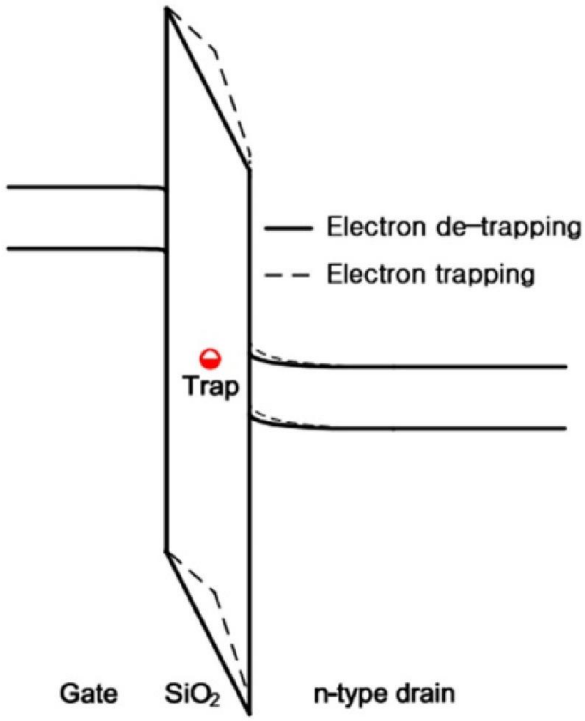


Figure 3.1: illustration of energy band diagram variation as electron captured (dash line) and emission (solid line)

For experimental work, we measured RTN in GIDL from the n type of metal-oxide semiconductor field effect transistor having a channel width of 0.2 μm, a gate length of 0.1 μm and an oxide thickness of 3.7nm. We obtain the two-level RTN in GIDL current as a function of time at a certain drain to gate voltage shown in Fig. 3.2. The gate, the source, and the substrate were biased to 0V in order to neglect other leakage components, except GIDL current [14].

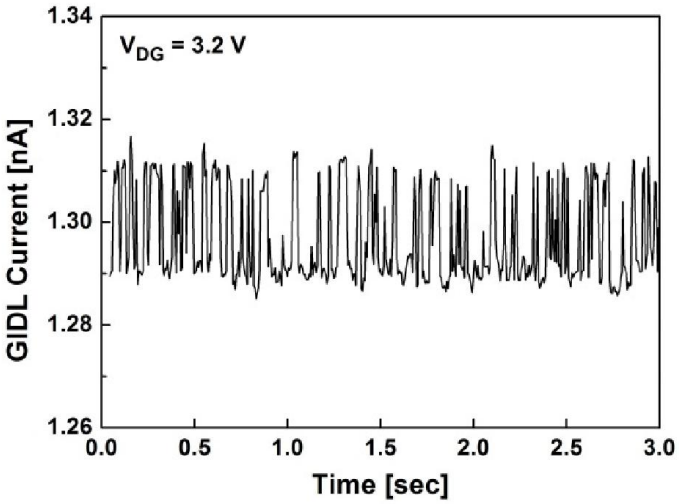


Figure 1.2: The measured RTN in GIDL current. $\Delta I_{GIDL}/I_{GIDL}$=1.55% and calculated x_T=1.4Å are used to extract the oxide trap's position

Three-dimensional simulation was performed by using TCAD [15]. The oxide thickness is 3.7 nm, the gate to drain overlapped length is 11 nm with the doping concentration for source/drain is 10^{20} cm^{-3} and for substrate is 1.4 x 10^{18} cm^{-3}. A trap is located respectively at one position among six predetermined positions inside the gate oxide on the gate to drain overlapped region shown in the Fig. 3.3. At every trap's position, we investigated the difference of GIDL currents when the trap is neutral and charged with an electron having charge of -1.602 x 10^{-19} C.

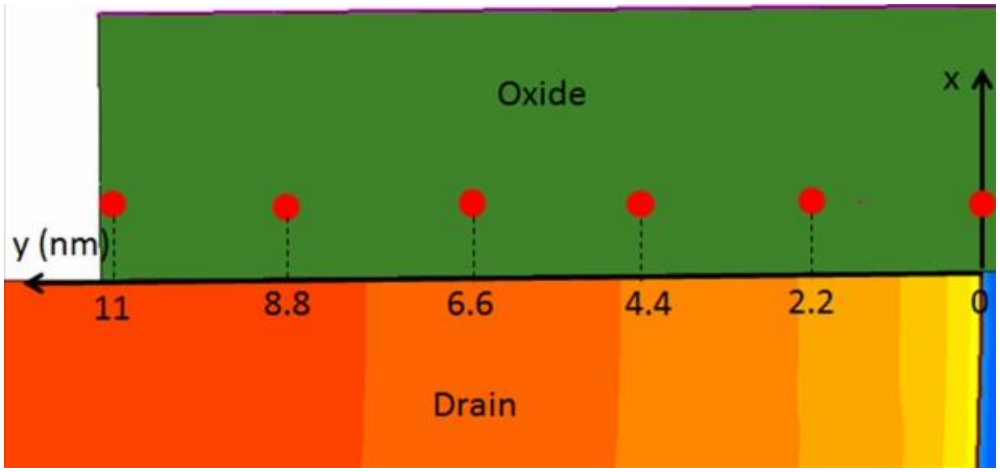


Figure 3.3: An oxide trap is located respectively at one position among six pre-determined positions

3.3 Result and Discussion

3.3.1 Location Dependence of $\Delta I_{GIDL}/I_{GIDL}$

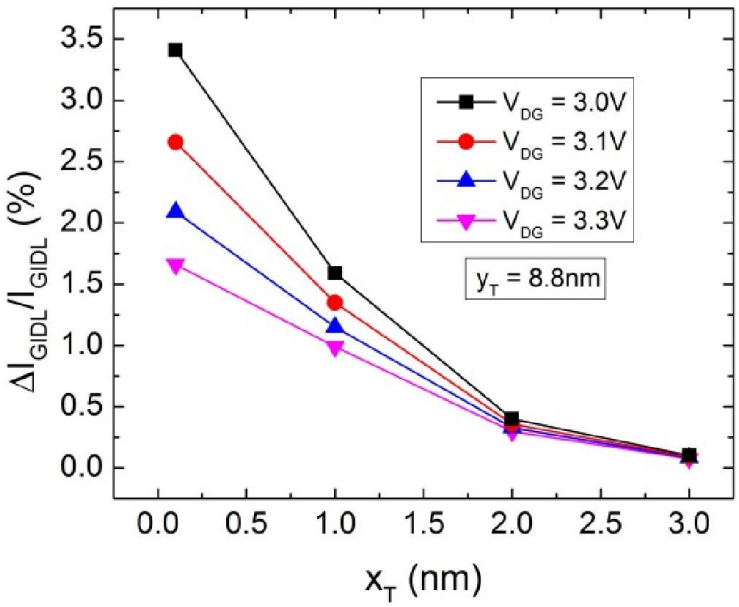


Figure 3.4: The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ increase due to decreasing distance from an oxide trap to Si/SiO_2 interface

Fig. 3.4 shows the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ versus vertical trap positions (x_T). As the trap was closer to the Si/SiO_2 interface, the relative amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ increased significantly. At the positions near gate poly-silicon, the relative amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ are almost zero and cannot

make the appreciable RTN. An oxide trap which can make appreciable RTN is almost close to the Si/SiO_2 interface.

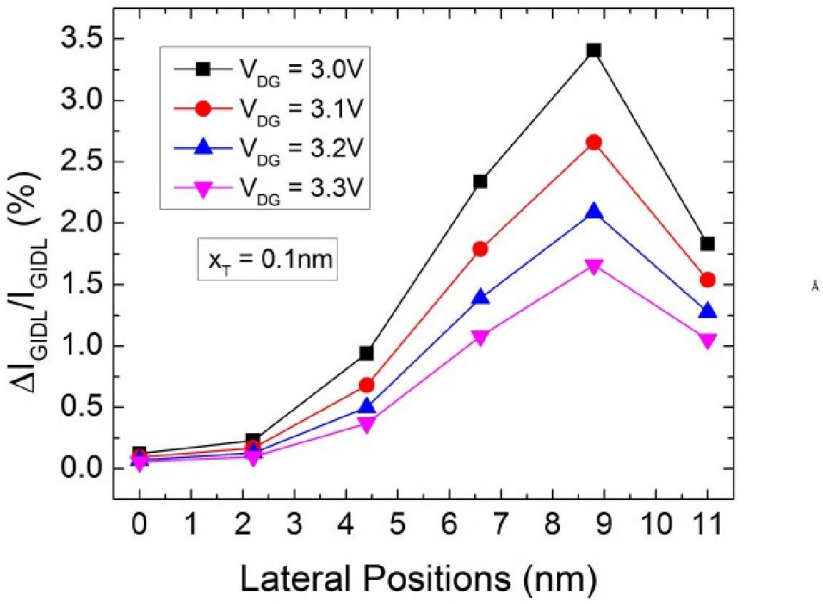


Figure 3.5: From the channel toward the edge of gate oxide, the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ increase significantly until y_T = 8.8nm and after that decrease

Fig. 3.5 shows the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ versus lateral trap positions (y_T). The largest amplitude of $\Delta I_{GIDL}/I_{GIDL}$ is at the lateral position of 8.8 nm, we believe that it is the closest to the band-to-band tunneling generation shown in Fig. 7. The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ at trap's position of 6.6 & 11 nm are almost same but the one at the lateral position of 11 nm is smaller a little

because of edge effect. The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ decrease significantly at positions for which y_T is smaller than 8.8 nm.

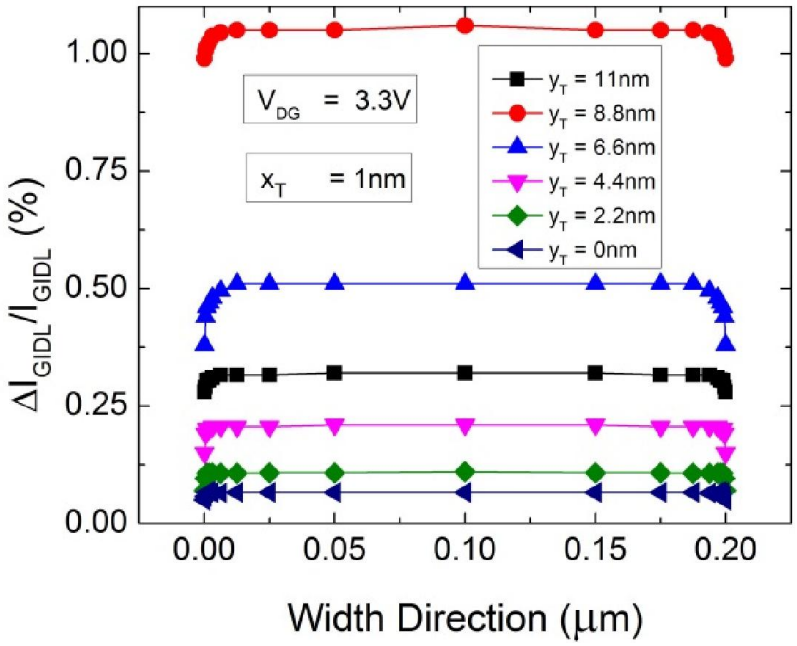


Figure 3.6: The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ are symmetric and almost same by the width direction

Fig. 3.6 shows the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ along the width direction. They are reduced at the edge of device and do not change at other positions because of the uniformity of GIDL current inside the device.

3.3.2 Extract the trap's location

After investigating the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ by all dimensions of the trap's position, we had the variation of GIDL current with the trap located at any position inside the gate oxide at gate to drain overlapped region. The relative amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ is almost same by the width direction so we just drew the 2D - contour along vertical and lateral direction as shown in Fig. 3.7.

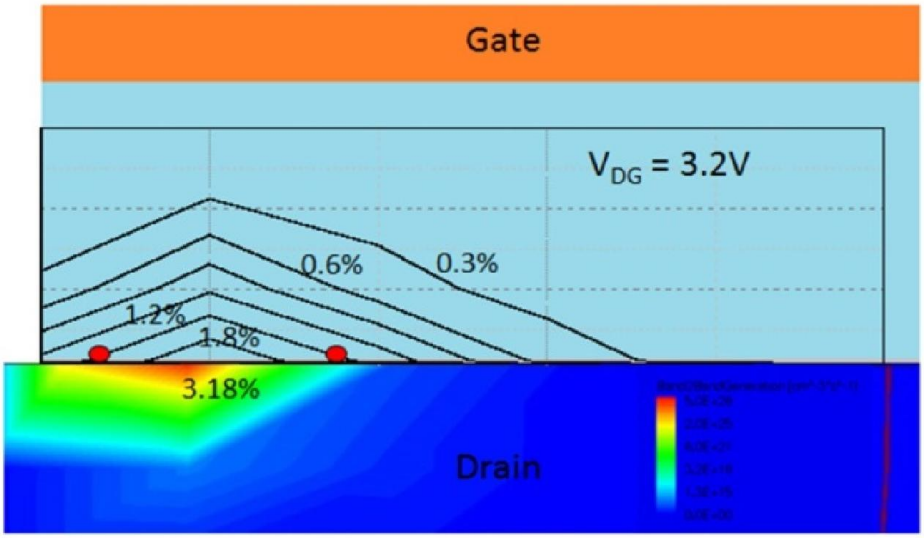


Figure 3.7: Illustration the contour of amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ with band to band generation. We can extract the trap's position from measurement and calculation data (experimented amplitude of $\Delta I_{GIDL}/I_{GIDL}$ and x_T)

From the experimental work of measuring RTN in GIDL current at V_{DG} = 3.2V, as shown in the Fig. 3.2. The relative amplitude of $\Delta I_{GIDL}/I_{GIDL}$ is 1.55% and calculated depth of trap (x_T) at the gate oxide is 1.4Å. The x_T was extracted by using the method in the previous study [12]. Using these data, we extracted two available trap's positions from the 2D-contour as shown in the Fig. 3.7 as the red points.

3.3.3 Bias Dependence of $\Delta I_{GIDL}/I_{GIDL}$

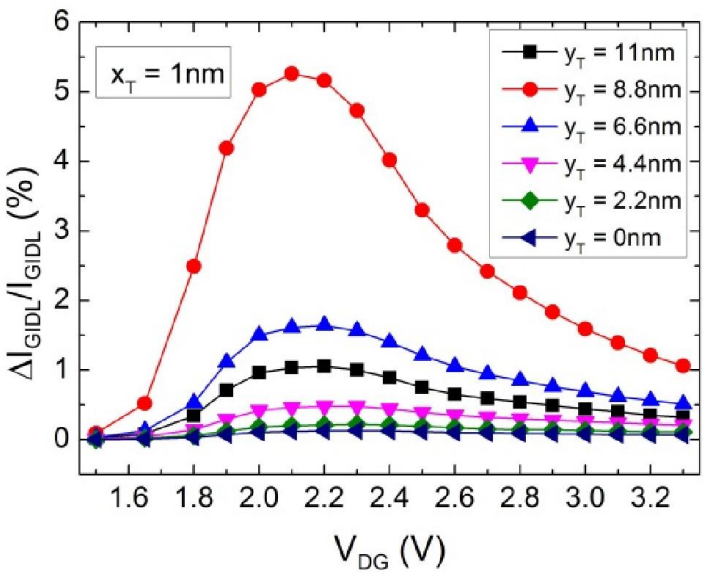


Figure 3.8: The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ increase at low drain to gate and decrease at high drain to gate voltage

Fig. 3.8 shows the dependence of the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ at each trap's position on drain to gate voltage V_{DG}. When V_{DG} increases, the electric field at the Si/SiO_2 interface (F) increases a lot. The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ at low V_{DG} region were represented by the equation (1) [16]. The exponential term increases leading to increasing the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$.

$$\frac{\Delta I}{I} = \left(1 + \frac{\Delta F}{F}\right) \exp\left(\frac{2F\Delta F}{F_{\Gamma,n}^2}\right) - 1 \qquad (3.1)$$

$$F_{\Gamma,n} = \frac{\sqrt{24 m_n^* (k_B T)^3}}{q\eta} \qquad (3.2)$$

where F is the electric field, ΔF is the increment of electric field due to a captured electron in the oxide trap at the overlap region, m_n^* is the effective mass of the carriers, k_B is the Boltzmann constants, T is absolute temperature, q is electronic charge, and $\hbar$ is reduced Planck constant.

At high V_{DG} region, the exponential term of the equation (3) decreases significantly leading to decreasing the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ [12].

$$\frac{\Delta I_{GIDL}}{I_{GIDL}} = \exp\left(B \cdot \frac{\Delta F}{F^2}\right) - 1 \qquad (3.3)$$

where parameter B is defined in [10].

The highest points of $\Delta I_{GIDL}/I_{GIDL}$ are at the transitional region between trap-assisted tunneling region and band-to-band tunneling region.

3.4 Conclusion

We have proposed the dependence on trap's location of RTN in GIDL current when an electron was captured. The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ vary significantly by vertical and lateral direction, while they are almost same by the width direction. An oxide trap is at the edge of gate oxide could make the appreciate RTN compared with the measurement data. From the 2D-contour of the amplitudes of $\Delta I_{GIDL}/I_{GIDL}$, we extracted the trap's location at the gate oxide of n-MOSFET. The amplitudes of $\Delta I_{GIDL}/I_{GIDL}$ were analyzed as functions of drain to gate voltage.

4. Simulation Study of Random Telegraph Noise (RTN) in GIDL current of Saddle MOSFET

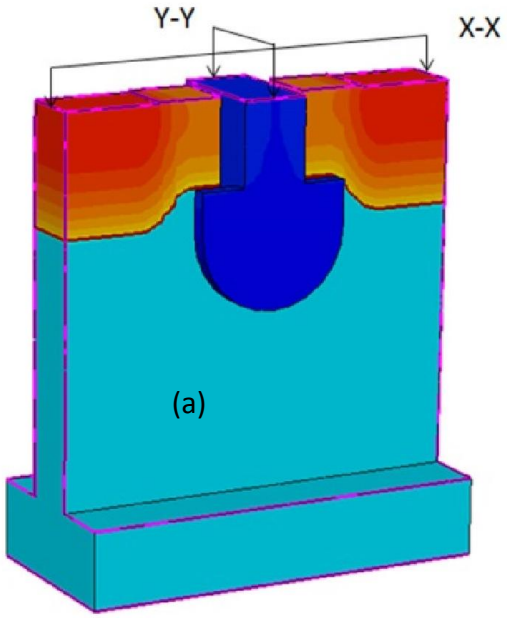
Abstract

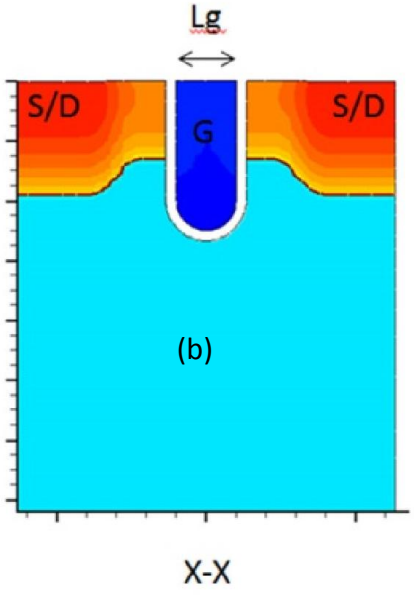
Random telegraph noise (RTN) magnitude in gate induced drain leakage (GIDL) current of Saddle MOSFET, a promising candidate for high-density DRAM applications, is analyzed using three-dimensional simulation TCAD. The RTN magnitude in GIDL current with electrons captured depend on oxide trap location, drain to gate voltage and numbers of oxide traps.

4.1 Introduction

Random telegraph noise (RTN) in GIDL current has been a serious concern in scaled down DRAM technology. The origin of RTN is attributed to trapping/de-trapping of carriers in trap located in a gate oxide or at a Si/SiO_2 interface [2, 3]. There are a few researches which investigate the characterization of an oxide trap for gate leakage current and GIDL current, a significant leakage component of current in modern MOSFETs which is mainly associated with both band-to-band or trap-assisted-tunneling in a gate to drain overlapped region [4, 5]. As a result, RTN in GIDL current is believed to cause variable retention time in DRAM devices [10]. As device dimensions are minimized, RTN in GIDL current becomes dominant, therefore there has been much interest regarding RTN in GIDL current. In this paper, we propose an approach for RTN in GIDL current with Saddle MOSFET structure, a promising candidate for high-density DRAM applications [17, 18], to determine its performance and reliability.

4.2 Method





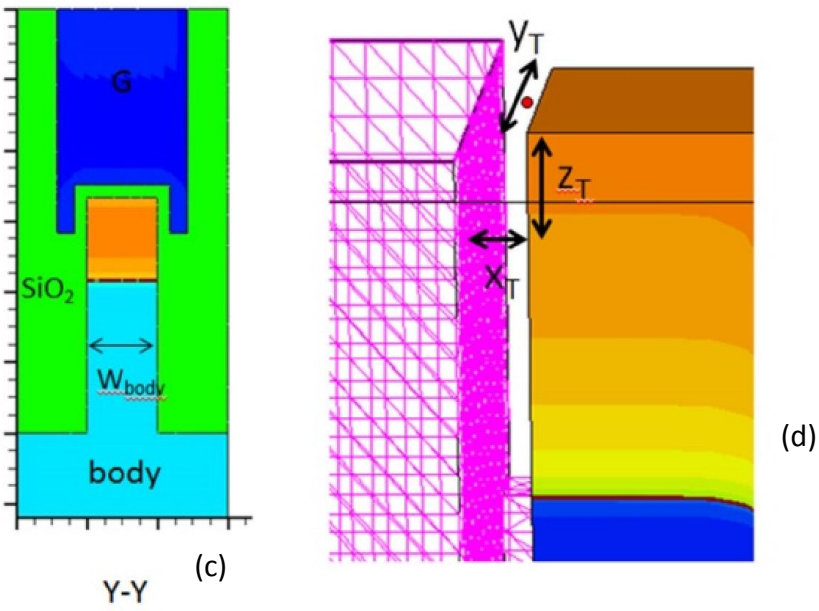


Fig 4.1: (a) 3-dimensional structure of Saddle MOSFET (b) (c) Cross section view across the gate and fin body (d) Location of a simulated oxide trap at gate-to-drain overlap region

Figure 4.1(a) shows a 3-D schematic view of Saddle MOSFET. The overlapped side gate is defined near the source/drain (S/D) junction depth to reduce the GIDL current. Fig. 4.1(b) and (c) shows the cross section views across the gate and the fin body, respectively. The LDD S/D junction depth is 21nm and the heavily doped S/D junction depth is about 33nm. The oxide thickness is 3.5nm. The fin body is directly connected to the substrate and the fin body thickness (W_{body}) is 20nm. The length of gate is fixed at 20nm. The uniform body doping is $1x10^{17}$ cm^{-3} and the LDD doping is $5x10^{18}$ cm^{-3}. Saddle

MOSFET, a promising candidate for highly scalable device application, has some advantages such as excellent short-channel effect (SCE) immunity, high I_{on}, low drain-induced barrier lowering (DIBL), excellent sub-threshold swing (SS) as shown in Fig. 4.2 [17, 18].

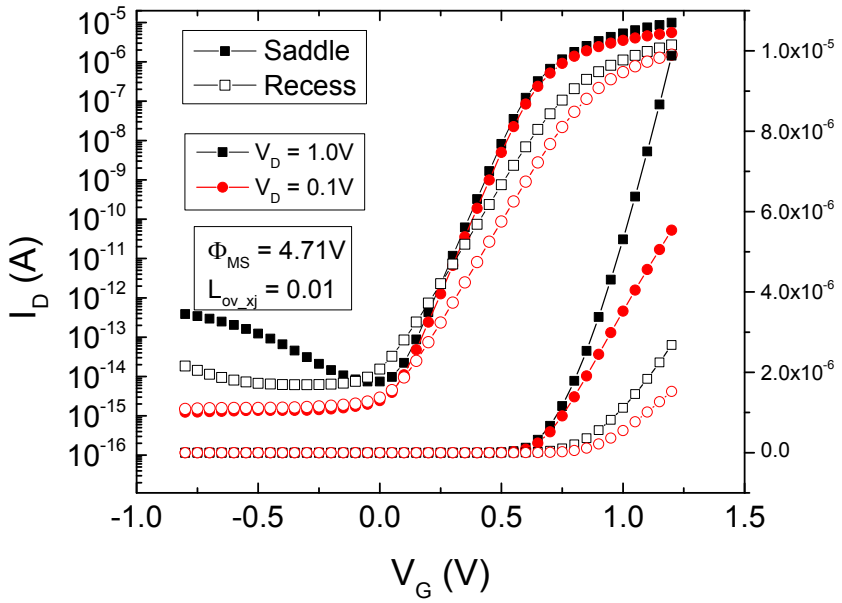


Figure 4.2: I_D-V_G curves of Saddle MOSFET and Recess Channel MOSFET

3-Dimensional simulation is performed by using TCAD [15]. A simulated oxide trap is located inside the gate oxide on the gate to drain overlapped region as shown in Fig. 4.1(d). At every trap's position, we

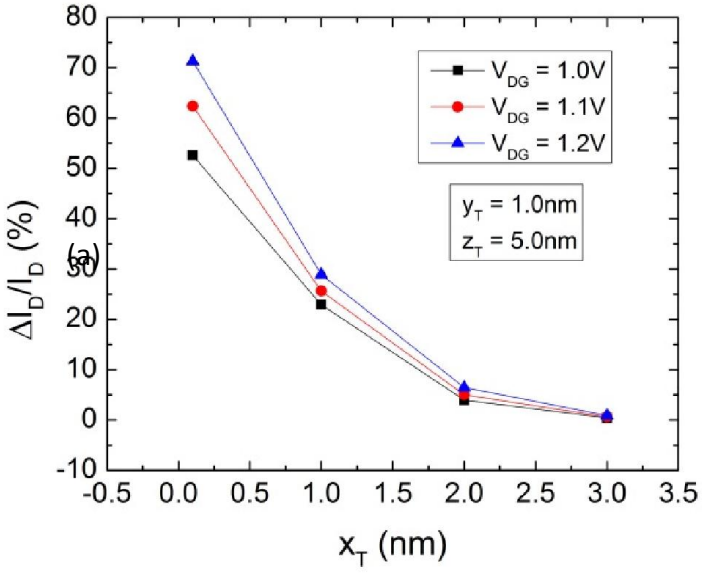
investigate the difference between GIDL current when the trap is neutral and charged with an electron having charge of -1.602×10^{-19}C.

4.3 Result and Discussion

4.3.1 Dependence on trap's location

If an electron is captured in an oxide trap in the gate-to-drain overlap region, the electric field at the Si/SiO2 interface increases as shown in Fig. 4.3(b). The increased electric field leads to the tunneling process can take place more easily, GIDL current increases [11, 14].

In Fig. 4.3(a), when the trap is located at x_T=0.1nm, the amplitude of $\Delta I/I$ is about 71% at V_{DG}=1.2V while the trap is at x_T=3nm, the amplitude of $\Delta I/I$ is about 1%. The amplitude of $\Delta I/I$ with x_T=3nm trap is very small due to the energy level of conduction band with trap does not change compared with the conduction band without trap as shown in Fig. 4.3(b).


80
70
60
50
40
30
20
10
0
-10
-0.5
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
$\Delta I_D/I_D$ (%)
x_T (nm)
V_{DG} = 1.0V
V_{DG} = 1.1V
V_{DG} = 1.2V
y_T = 1.0nm
z_T = 5.0nm
(a)

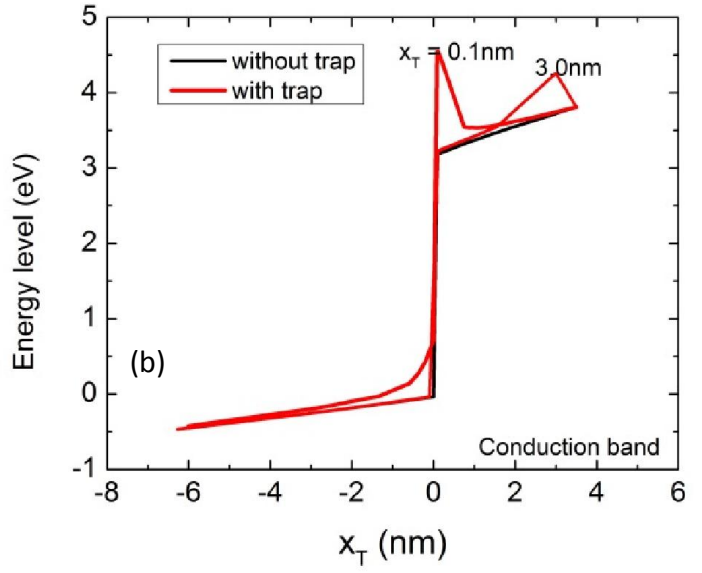
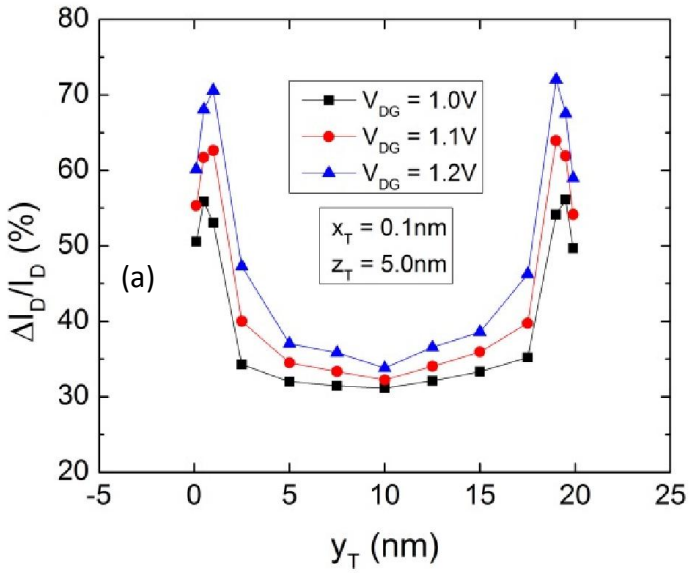

5
4
3
2
1
0
-1
-8
-6
-4
-2
0
2
4
6
Energy level (eV)
x_T (nm)
without trap
with trap
x_T = 0.1nm
3.0nm
(b)
Conduction band

Fig.4.3: (a) Dependence on trap location by lateral direction - x_T of ΔI/I (b) The energy level of conduction band increases significant at the interface when the oxide trap is at 0.1nm and it does not change when the trap is at 3nm.

To estimate the highest amplitude of ΔI/I, we locate the trap at x_T=0.1nm and we continue to investigate the trap's position by width direction from y_T=0~20nm.



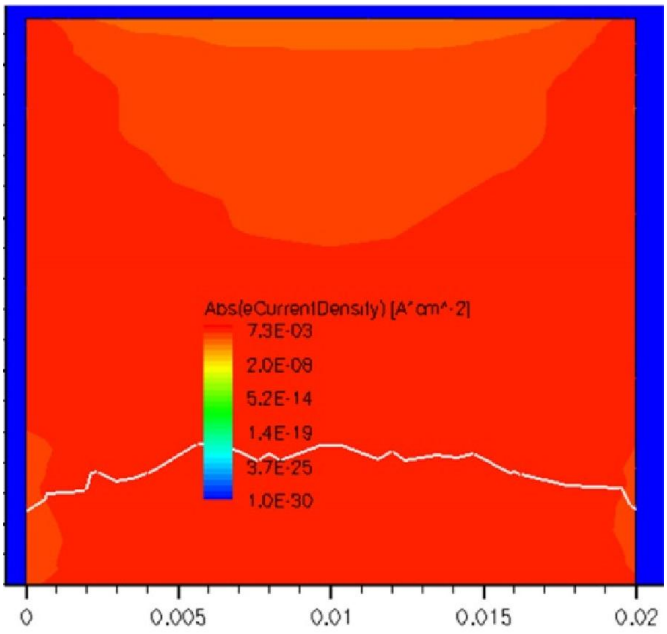
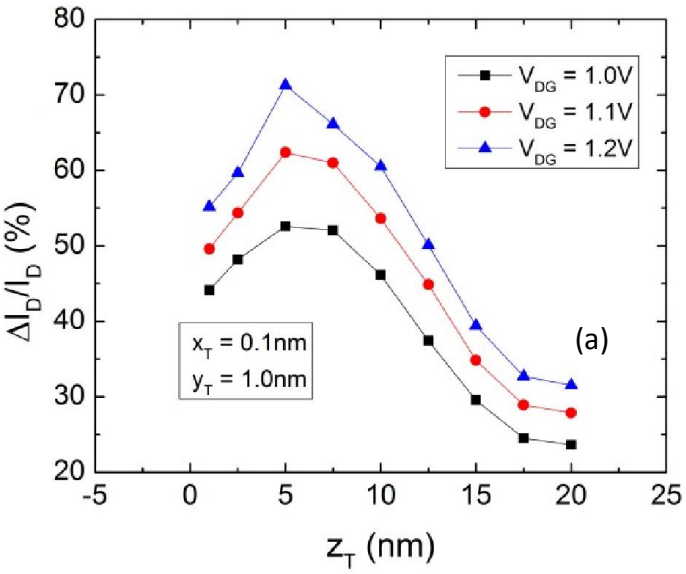


Fig.4.4: (a) Dependence on trap location by width direction– y_T of ΔI/I (b) The contour of electron current density by width direction.

The amplitudes of ΔI/I at the edge of fin body are higher than other position inside body. At V_{DG}=1.2V, the highest amplitude of ΔI/I is about 71% at x_T=0.1nm, y_T = 1nm. The distribution of ΔI/I values is quite symmetric by width direction as shown in Fig.4.4(a). The highest points of ΔI/I is located same with the highest points of electron current density, near the corner of fin body as shown in Fig.4.4(b).

We continue investigating the ΔI/I from z_T=0~20nm by vertical position with a trap fixed at x_T=0.1nm and y_T=1nm.


80
70
60
50
40
30
20
-5
0
5
10
15
20
25
$\Delta I_D/I_D$ (%)
z_T (nm)
V_{DG} = 1.0V
V_{DG} = 1.1V
V_{DG} = 1.2V
x_T = 0.1nm
y_T = 1.0nm
(a)

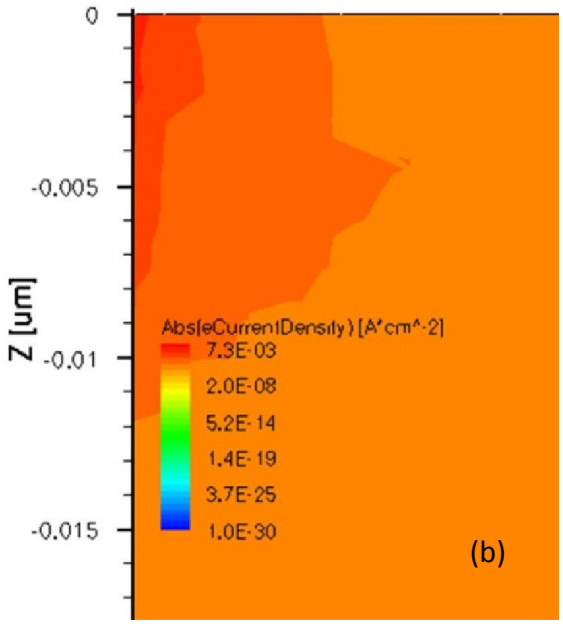
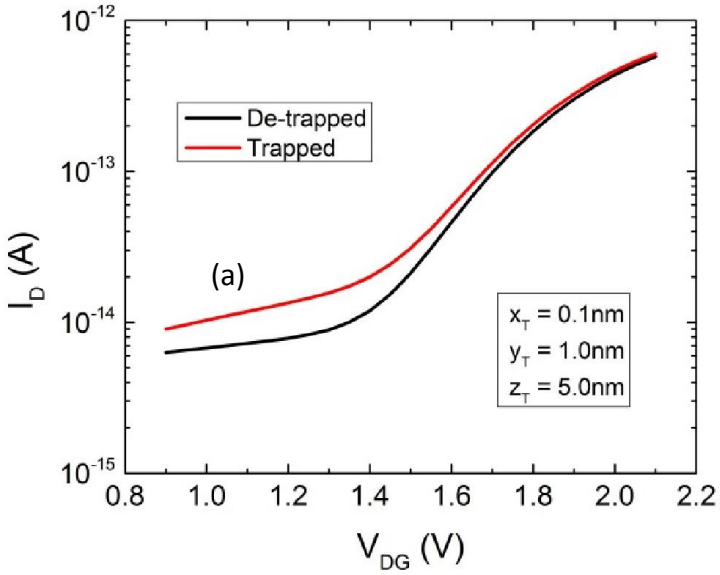

0
-0.005
-0.01
-0.015
Z [um]
AbsJeCurrentDensity) [A*cm^-2]
7.3E-03
2.0E-08
5.2E-14
1.4E-19
3.7E-25
1.0E-30
(b)

Fig.4.5: (a) Dependence on trap location by vertical direction – z_T of ΔI/I (b) The contour of electron current density by vertical direction.

As shown in Fig.4.5(a), the highest amplitudes is 71% at z_T=5nm and the distribution of ΔI/I is same with the contour of electron current density by vertical direction in Fig.4.5(b).

4.3.2 Dependence on drain-to-gate voltage



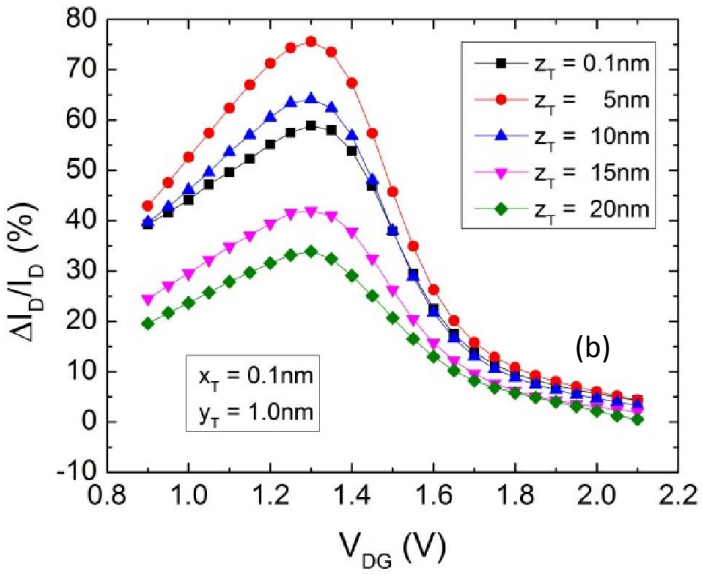
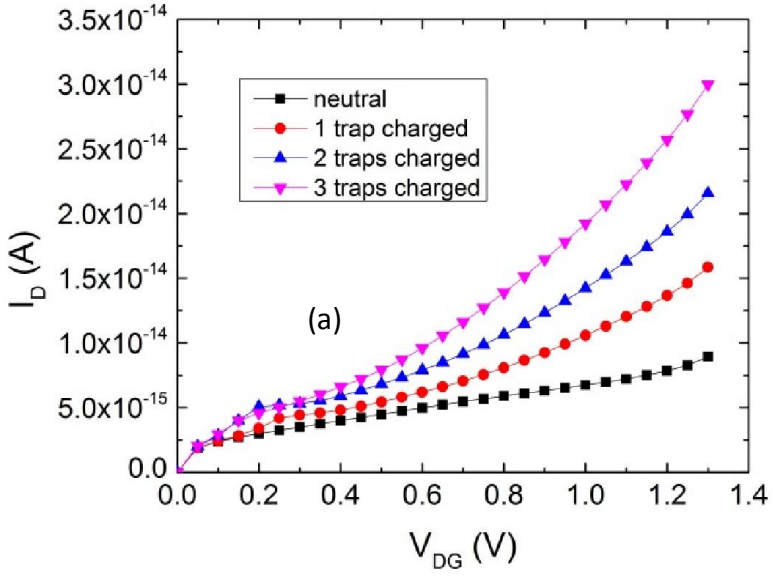


Fig.4.6: (a) I_D-V_{DG} curve of Saddle MOSFET with and without the captured electron (b) Dependence on Drain to Gate Voltage of ΔI/I

Figure 4.6(a) shows the I_D-V_{DG} curves with and without a captured electron. In Fig.4.6(b), the amplitudes of ΔI/I increase at low drain to gate voltage region and change inversely in high drain-to-gate voltage region [12, 16]. The highest amplitude of ΔI/I is about 76% at VDG=1.3V with trap located at x_T=0.1nm, y_T = 1nm and z_T=5nm.

4.3.3 Dependence on numbers of oxide traps

We investigate the changing of ΔI/I with multi-traps which are located at x_T=0.1nm, y_T = 1nm and get the result shown in Fig.4.7(a) and (b).


3.5x10^-14
3.0x10^-14
2.5x10^-14
2.0x10^-14
1.5x10^-14
1.0x10^-14
5.0x10^-15
0.0
I_D (A)
neutral
1 trap charged
2 traps charged
3 traps charged
(a)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
V_DG (V)

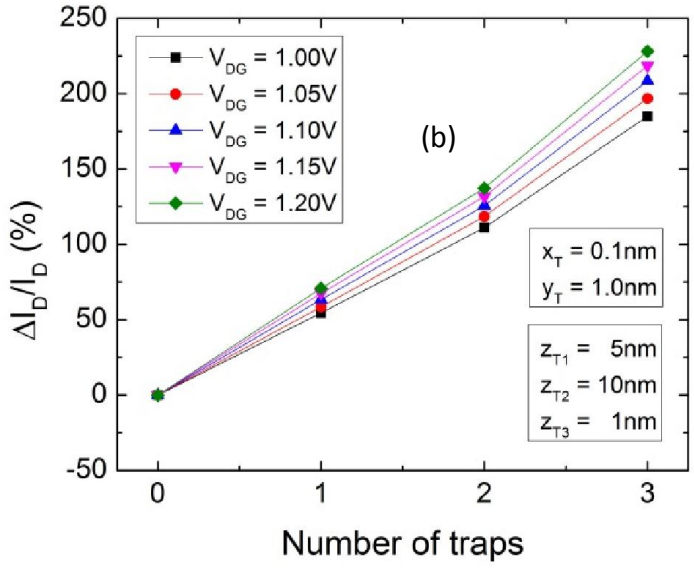

250
200
150
100
50
0
-50
ΔI_D/I_D (%)
V_DG = 1.00V
V_DG = 1.05V
V_DG = 1.10V
V_DG = 1.15V
V_DG = 1.20V
(b)
x_T = 0.1nm
y_T = 1.0nm
z_T1 = 5nm
z_T2 = 10nm
z_T3 = 1nm
0
1
2
3
Number of traps

Fig.4.7: (a) I_D-V_{DG} curves with traps or without trap (b) Dependence on number of traps of ΔI/I

The amplitudes of ΔI/I with 2 electrons captured increase twice compared with ΔI/I with a single electron captured and more than 3 times with 3 electrons captured. RTN in GIDL current increases significant not only with a single trap but also with several traps in the gate oxide.

4.4 Conclusion

We investigated the RTN in GIDL current of Saddle MOSFET, a promising candidate for highly-density DRAM application. We found that the highest value of ΔI/I is about 76% with a single electron captured at V_{DG}=1.3V and it increases significantly with two or three electrons captured. The amplitudes of RTN in GIDL current depend on trap's location, drain-to-gate voltage, and numbers of traps.

5. Conclusion

In this thesis work, we have carried out a study of random-telegraph-noise (RTN) in gate-induced drain leakage (GIDL) current and presented the characterization of an oxide trap.

With a planar n-MOSFET, RTN in GIDL current depends on the trap position by all three directions, vertical, lateral and width direction. We already presented a contour to extract two available trap at the gate oxide.

RTN in GIDL current also depends on drain-to-gate voltage. At high drain-to-gate voltage, RTN in GIDL current decreases with increasing bias while at low drain-to-gate voltage, it increases with increasing bias and reach the highest value at the transition region.

Saddle MOSFET is a promising candidate for high-density DRAM application. We investigated RTN in GIDL current with saddle MOSFET by all three direction and especially, the highest value of RTN in GIDL current is much higher than the one of planar MOSFET.

We also investigated the multi-level RTN in GIDL current. RTN in GIDL current also increases significantly with multi-traps.

This work can be useful to determine the performance and reliability of high-density DRAM cell transistor.

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Breathe and Smile

Nguyen Gia Quan

초 록

소자의 면적이 작아짐에 따라, Random telegraph noise (RTN) 이 metal-oxide-semiconductor field effect transistor (MOSFET)의 내구성과 성능을 결정하는 주 요인이 되었다. RTN 은 게이트 옥사이드 혹은 실리콘/실리콘 옥사이드 계면에 위치한 트랩에 전하들이 트랩되고 빠짐에 의해 생긴다. 지금까지 대부분의 연구들이 옥사이드트랩의 채널 또는 게이트 누설전류에 미치는 영향을 연구하는 방향으로 행해졌고 매우 적은 수만이 게이트와 드레인이 겹친 영역에서의 band-to-band 또는 trap-assisted-tunneling 에 의해 형성되는 모스펫의 가장 중요한 누설 전류 요소인 Gate-induced drain leakage 전류에 행해졌다. 그 결과로 GIDL 에서의 RTN 전류는 DRAM 소자들의 변하는 retention time 의 원인이라 믿어졌다. 이런 이유들 때문에 GIDL 에서의 RTN 전류가 더욱더 주목을 받게 되었다. 이전의 저자들은 측정을 통해서 GIDL 에서의 RTN 전류를 야기하는 옥사이드 트랩들을 보고했다. GIDL 전류를 변동시키는 옥사이드 트랩들의 특성에 대한 더 나은 이해를 위해 이런 트랩들의 특성에대한 정확한 정보를 얻는 것이 필수이다.

이 이론에서 우리는 트랩의 수직, 평행, width 방향에 의존하는 GIDL 전류의 변동을 나타내는 정확한 모델을 만들었다. 그리고 게이트 옥사이드에서의 트랩 위치를 예상했다. 우리는 또한 GIDL 에서의 RTN 전류의 크기를 드레인 게이트 전압의 함수로 분석했다. 또한 우리는 DRAM 소자에서 각광받는 고집적 응용소자인 20 나노 Saddle MOSFET 의 옥사이드에서의 트랩 특성을 연구했다.

주요어: Gate-induced drain leakage (GIDL), random telegraph noise (RTN), Saddle MOSFET, location of an oxide trap, amplitude of $\Delta I_{GIDL}/I_{GIDL}$

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