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Master Thesis

**Design of Digital PLL/CDR with
Advanced Digital Controller**

진보된 디지털 컨트롤러를 이용한 디지털 위상
동기화 루프와 클럭 및 데이터 복원 회로의 설계

By

Sigang Ryu

February, 2014

School of Electrical Engineering and Computer
Science College of Engineering
Seoul National University

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지도교수 김 재 하

이 논문을 공학석사 학위논문으로 제출함

2014년 2월

서울대학교 대학원

전기 컴퓨터 공학부

류 시 강

류 시강의 공학석사 학위论문을 인준함

2014년 2월

위 원 장 : _____

부위원장 : _____

위 원 : _____

Abstract

This thesis presents a design methodology of digital PLL/CDR with various digital controllers. In comparison with analog approaches, digital techniques can circumvent inherent design constraints of analog-based timing circuits, thereby achieve such as non-linear transfer, gear shifting (adaptive damping technique), fast-locking algorithm and so on.

First, this thesis describes a digital phase-locked loop (PLL) that realizes a peaking-free jitter transfer. That is, the PLL's second-order transfer function does not have a closed-loop zero. Such a PLL does not exhibit overshoots in the phase step response and achieves fast settling. Unlike the previously-reported peaking-free PLLs, the proposed PLL implements the peaking-free loop filter directly in digital domain without requiring additional components. A time-to-digital converter (TDC) is implemented as, a set of three binary phase-frequency detectors that oversample the timing error with time-varying offsets, achieving a linear TDC gain and PLL bandwidth insensitive to the jitter condition. The prototype 9.2-GHz-output digital PLL fabricated in a 65nm CMOS demonstrates a fast settling time of 1.58- μ s with 690-kHz bandwidth. The PLL has a 3.477-ps_{rms} divided clock jitter and -120dBc/Hz phase noise at 10-MHz offset while dissipating 63.9-mW at a 1.2-V supply.

Second, the proposed high-order clock and data recovery(CDR) employs tracking aid to track frequency modulated data using spread-

spectrum clocking(SSC) to mitigate steady-state jitter characteristic. This thesis describes the implementation of the tracking aid to achieve accurate estimation of the time instants. Instead of the noise sensitive differentiator used in previous works, the proposed architecture uses an integrator that is more resilient to noise or disturbance and more accurate. The design of the architecture fully implemented in digital achieves SSC timing errors less than < 10 cycles, locking time < 15 ms overall CDR jitter of $0.12U_{Ipp}$.

Key words : PLL, CDR, Digital loop filter, Digital controller, Digital PLL, Digital CDR, TDC, BBPFD, Transfer function

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Chapter 1

Introduction

1.1 Digital PLL/CDR

Phase-locked loop (PLL) is a kind of timing circuits which act as clock source in several system-on-chip (SOC) applications. And clock and data recovery (CDR) which extracts synchronous clock from input data and re-times it is a widely used circuit in data receiver. Traditionally, a PLL and CDR is regarded as analog building blocks. However, integrating PLL/CDR in a SOC environment becomes hard work in that incompatibility with a digital baseband which is constructed in a low-voltage deep submicron CMOS process.

As CMOS processes shrink into deep submicron regimes, the design of analog charge-pump PLL (CPPLL) and the conventional CDR based on it can be hindered by many challenges. First, the performance of the analog building blocks of PLL/CDR can be degraded due to limited voltage headroom. Second, capacitors and resistors, which are used in CPPLL/CDR, didn't scale with CMOS technology shrink to the same ratio. Third, the charge-pump based PLL/CDR suffers from reference spurs because of their correlative phase error detection. And finally, they have difficulty in achieving constant transfer characteristics which are immune to process,

voltage, and temperature (PVT) variations due to employing various active component.

PLL/CDR designed with digital CMOS component that is standard cells can overcome the problems mentioned above. Several digital PLLs and CDRs that based on digital PLL have been reported in [1]-[3]. By obviating the analog component such as capacitor-based loop filter and charge-pump which degrade performances in aspect of area and jitter, digital PLL/CDR (DPLL/CDR) provides area savings, immunity to PVT variations, and noise tolerance due to digital domain processing.

Most of all, the important attribution of digital PLL/CDR is programmability. Digital loop filter or digital controller in the digital PLL/CDR can circumvent inherent design constraints (such as loop bandwidth, damping factor, settling time and so on) different from its analog counterparts. For example, an important issue in frequency synthesis for today's wireless applications is the acquisition or settling time to a new channel frequency from the trigger event. Loop bandwidth in conventional CPPLL is fixed or is tuned narrowly to track frequency error. However, in digital domain, PLL can track frequency error with high-damping ratio triggered by acknowledge signal and optimize jitter after its output clock frequency settles in appropriate value by recovering adequate damping ratio (which called adaptive-damping or gear-shifting).

It should be noted that it is generally difficult to perform gear shifting (adaptive damping), fast settling algorithm, non-linear transfer function in

analog architecture. Therefore, in this thesis, the presented PLL and CDR employ advanced digital techniques to realize fast settling to reference clock, constant linear TDC gain, and more robust noise-insensitivity to spread-spectrum-clocking (SSC) type data stream and so on. As a consequence, these digital techniques can be overcome the architectural issues of conventional analog timing circuits and provide insight of solving problems derived from inherent constraints of analog timing circuits.

1.2 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces a digital phase-locked loop (DPLL) that realizes a peaking-free transfer function and analyzes its fast-settling ability in terms of transfer function and describes building blocks. Chapter 3 describes a digital clock and data recovery (DCDR) which employs tracking-aid to correct phase error stem from spread-spectrum clocking (SSC) type data stream. By using hierarchical description, the SSC tracking block is analyzed. After the explanation of two types of timing circuits, chapter 5 will conclude the thesis.

Chapter 2

Digital Phase-Locked Loop with Peaking-Free Transfer function

2.1 Introduction of Peaking-Free Digital PLL

A commonly well-known weakness of phase-locked loops (PLLs) against delay-locked loops (DLL) is jitter accumulation [4], which stands for the continued increase in the phase error even while the feedback loop has detected the error and tries to correct it. The jitter accumulation behavior is due to the presence of a zero in the closed-loop transfer function of a second-order PLL. For instance, the popular-used proportional-integral (PI) loop filter, such as a charge pump followed by a series-RC filter, places the closed-loop zero of which frequency cannot be changed without affecting the bandwidth or stability of the PLL. In frequency domain, this closed-loop zero causes peaking in the PLL's phase-domain transfer function, enhancing the phase noise at the vicinity of the PLL bandwidth frequency. In time domain, the closed-loop zero causes an overshoot in the phase step response, which slows down the settling ability of PLL. To overcome these problem, this thesis provides an extended description and analysis on the digital PLL presented in [5] that can achieve fast settling without overshoots and its transfer characteristic without peaking by removing the closed-loop zero.

Even if a number of PLLs with the same objective have been previously

reported in literature [6]-[8], the digital PLL in [5] has an advantage in that the closed-loop zero elimination is achieved only by a novel digital loop filter, without requiring additional noise-sensitive analog circuit components. As explained in [5], a key to eliminating the closed-loop zero is to have a way of correcting the phase error without altering the frequency of the oscillator. For instance, the peaking-free analog PLL in [6] used an additional voltage-controlled delay line (VCDL) to adjust the input clock phase. The PLLs described in [7] and [8] used a programmable divider to shift the phase of the feedback clock. However, these additional circuit components placed in the noise-sensitive input/feedback paths may degrade the jitter performance and increase hardware cost. In contrast, the digital PLL discussed in this thesis uses a digital loop filter to correct the phase error in digital domain. Since it is only the digital loop filter that requires a change, the presented peaking-free digital PLL design can be easily adopted by many existing digital PLLs with linear time-to-digital converters (TDCs).

This thesis further extends [5] by presenting an analysis on the peaking-free digital PLL loop dynamics and discussing the optimal selection on the loop filter parameters. For instance, although a basic loop filter with a nested-feedback phase compensation can realize a peaking-free closed-loop transfer function for the PLL, a actual digital loop filter would require an additional high-pass filter in order to eliminate the static phase offset.

The presented digital PLL employs a set of circuit to have the PLL's characteristics predictable and robust against external conditions, including

PVT variation and input jitter conditions. Most of all, a low-cost linear time-to-digital converter (TDC) is constructed as a set of bang-bang phase-frequency detectors (BB-PFDs) triggered by independently-dithered clocks, using a set of phase-domain digital-to-analog converters (phase DACs) and delta-sigma modulator (DSM). Adding intentional dither jitter to the BB-PFD triggering clocks helps achieve a constant linear TDC gain which is independent of the PVT and jitter conditions.

2.2. Peaking-Free Digital PLL Architecture

2.2.1. Jitter Peaking in Conventional Second-Order PLLs

As mentioned in the section 2.1, a second-order PLL employing a PI loop filter yields a closed-loop zero, which causes peaking in the jitter transfer and overshoots in the transient response. This subsection explain shortly the causes of such jitter accumulation behavior found in the conventional second-order PLLs.

Fig. 2.1(a) illustrates the s-domain model of a second-order PLL employing a PI loop filter. It can be shown that the PLL has a closed-loop transfer function expressed as below:

$$H(s) = \frac{K(K_I s + K_P)}{s^2 + K K_P s + K K_I} \quad (2.1)$$

Where K_P and K_I are the proportional and integral gains of PI loop filter, respectively. The gain parameter K is defined as $K = K_{TDC} K_{DCO} / N$, where

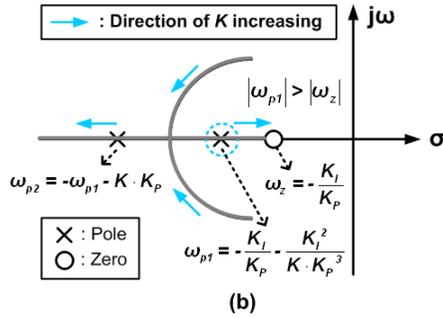
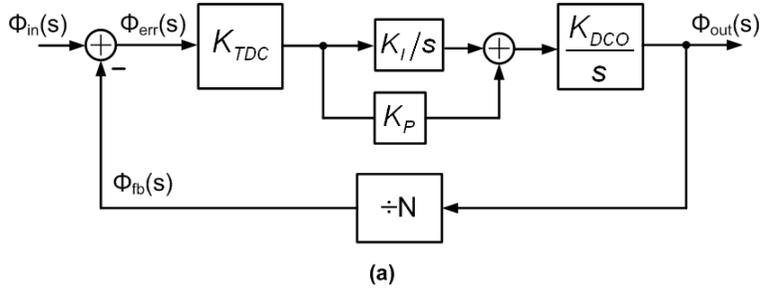


Fig. 2.1. (a) The s-domain system model of a conventional second-order PLL and (b) its root locus illustrating the pole/zero locations of the closed-loop system with the increasing K values.

K_{TDC} and K_{DCO} are the TDC gain and DCO gain, respectively.

Fig. 2.1(b) shows the root locus of $H(s)$ as the gain K increases. The closed-loop system initially has two complex poles with low K values, but the poles become real as K increases and the PLL response gets sufficiently over-damped. On the other hand, the zero is always located at the vicinity of the PLL bandwidth frequency. Since the lower pole frequency (ω_{p1}) is always higher than the zero frequency (ω_z), there always exists a peaking in the closed-loop transfer function, of which peak magnitude can be expressed as:

$$\max |H(s)| \approx 1 + \frac{K_I}{K \cdot K_P^2} = 1 + \frac{1}{4\zeta^2} > 1 \quad (2.2)$$

Note that the desired peak magnitude of $H(s)$ is 1 without exhibiting any jitter peaking. As can be seen from Fig. 2.1(b) and Eq.(2.2), although the amount of jitter peaking can be reduced by increasing K or increasing the ratio of K_P^2/K_I , it can never be completely removed since the zero is always placed at the lower frequency than the poles. Besides, an excessively over-damped system is not desirable as it has a slow settling response. Therefore, most second-order PLLs have some amount of jitter peaking and many PLL specifications prescribe the maximum jitter peaking permitted (0.1dB in the SONET jitter transfer standard [9]).

2.2.2. Previously Reported Peaking-Free PLLs

In order to remove the closed-loop zero and hence the jitter peaking observed in the conventional second-order PLLs, a few peaking-free techniques have been previously proposed in literature. For instance, Fig. 2.2(a) shows the block diagram of an analog-type peaking-free PLL described in [6]. The PLL uses an integration-only filter with the charge-pump, but instead employs an additional voltage-controlled delay line (VCDL) in the input clock path, which shares the control voltage V_{ctrl} with the voltage-controlled oscillator (VCO). The VCDL delay offsets the input clock phase arriving at the phase detector and the equation governing V_{ctrl} can be expressed as below:

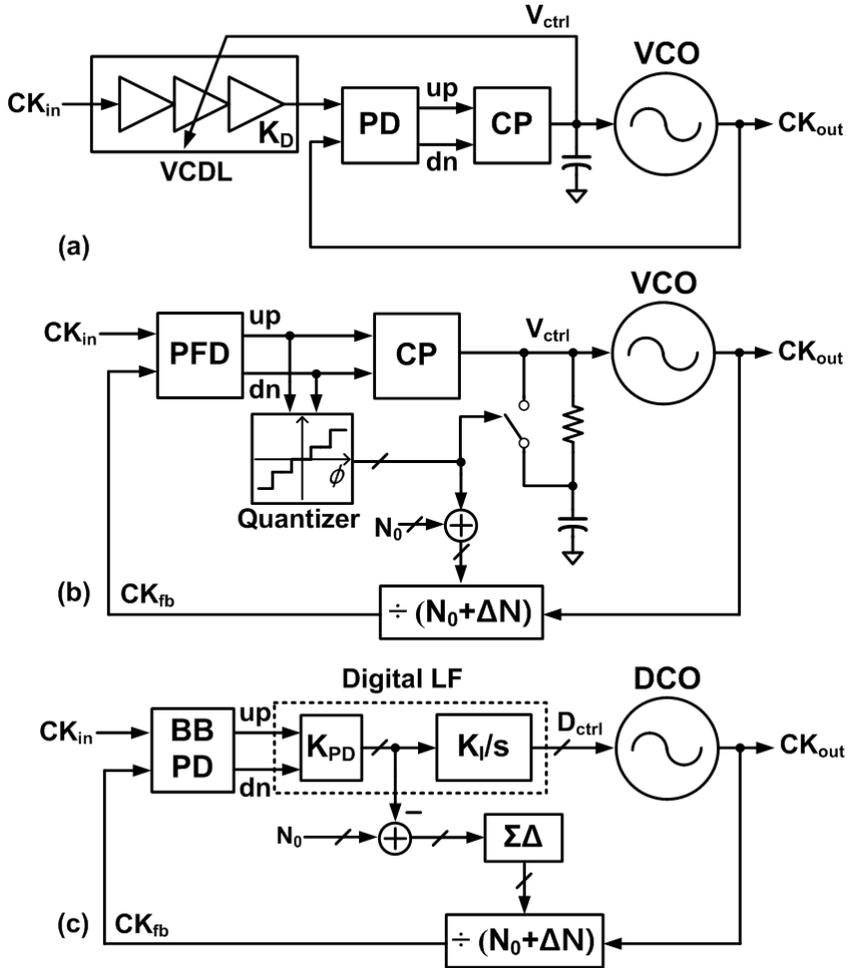


Fig. 2.2. The previously-published peaking-free PLLs: (a) the analog PLL with a cascaded VCDL [6], (b) the analog PLL with a programmable divider for phase error compensation [7], and (c) its equivalent digital PLL [8].

$$V_{ctrl}(s) = K_I/s \cdot (\phi_{in} - \phi_{out} - K_D V_{ctrl}(s)) \quad (2.3)$$

where K_D is the VCDL gain. Note that the $K_D V_{ctrl}(s)$ term compensates the phase error and thus serves the role of stabilizing the feedback loop. More

importantly, it can be shown that the resulting closed-loop transfer function of this PLL does not have a closed loop zero:

$$H(s) = \frac{K_I K_{VCO}}{s^2 + K_I K_D s + K_I K_{VCO}}. \quad (2.4)$$

Hence, the peaking-free transfer characteristic can be realized.

However, one difficulty associated with this design is that the VCDL must have a wide enough range to provide the necessary phase compensation for the entire range of V_{ctrl} and at all possible PVT conditions. Furthermore, such a wide-range VCDL is typically sensitive to the noise on the supply, substrate, or control voltage V_{ctrl} , which can adversely affect the overall jitter performance of the PLL.

On the other hand, PLLs using a programmable divider instead of the VCDL are recently reported with peaking-free characteristics [7],[8]. Fig. 2.2(b) and (c) show the block diagrams of the analog [7] and digital [8] versions of this PLL, respectively. Both of the PLLs share a commonality in that the necessary phase compensation in Eq. (2.3), i.e. the $K_D V_{ctrl}(s)$ term, is provided by momentarily changing the division ratio from its nominal value (N_0) relying on the phase detector (PD) output. Since the phase of the feedback clock (CK_{fb}) changes with the time-integral of the dividing factor's deviation from N_0 , controlling the programmable divider this way can realize the transfer function in Eq. (2.3) and hence the peaking-free characteristic. Specifically, the analog PLL shown in Fig. 2.2(b) quantizes the pulse widths of the phase-frequency detector (PFD) output signals (up and dn) to several

discrete levels and adjusts the division factor $N_0 + \Delta N$, accordingly. On the other hand, the digital PLL in Fig. 2.2(c) obtains a finer-resolution measure on the phase error by accumulating the bang-bang phase detector outputs for multiple cycles and applies the result to a delta-sigma based fractional divider.

However, one limitation of employing the programmable dividers is that the resolution of phase correction can be too coarse especially when the nominal division ratio N_0 is small, making the programmable divider inappropriate to correct a small phase error. For this reason, the PLL design [7] in Fig. 2.2(b) reverts back to a conventional second-order PLL by turning off the switch shorting the series resistance in the loop filter when the measured phase error is less than a certain minimum threshold. Although a fractional divider used in the PLL in Fig. 2.2(c) can alleviate this resolution problem somewhat, another limitation is that the quantization noise generated by the delta-sigma modulator (DSM) must be filtered before reaching the PLL output and therefore constrains the maximum bandwidth possible for the PLL.

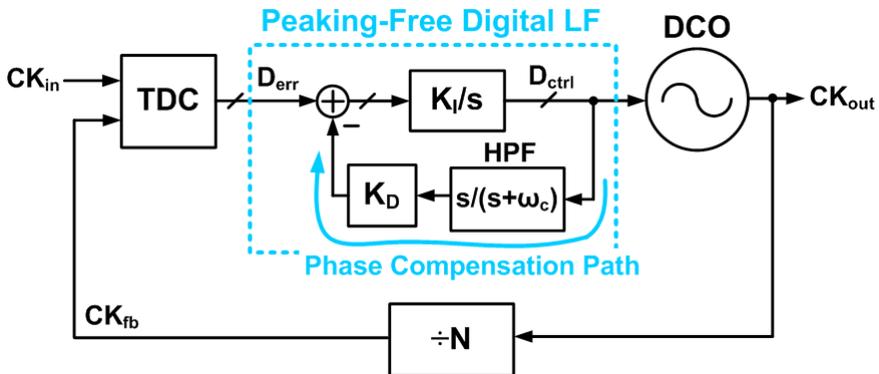


Fig. 2.3. The block diagram of the proposed peaking-free digital PLL.

2.2.3. The Proposed Peaking-Free Digital PLL

The peaking-free digital PLL first presented in [5] is different from the previously-published ones in that the solely change is made to the digital loop filter. In other words, the loop filter operation expressed in Eq. (2.3) is directly designed in digital domain, without demanding any additional circuit blocks on the input or feedback clock paths. Fig. 2.3 depicts the architecture of the proposed digital PLL, which is composed of a TDC, a peaking-free digital loop filter, a DCO, and a fixed-ratio frequency divider. The digital loop filter implements the necessary phase compensation by subtracting a K_D -scaled version of the control code of DCO (D_{ctrl}) from the digitized phase error (D_{err}).

The proposed peaking-free digital PLL has a number of advantages compared to the previously-reported designs. First, no additional circuit blocks are required on the clock paths which may adversely affect the clock jitter. For instance, no wide-range VCDL in the input clock path [6] or programmable divider in the feedback clock path is required. Second, fine-resolution phase compensation is possible unlike the ones in Fig. 2.2(b) and (c). In fact, the phase resolution is limited only by the bit resolutions of the digital accumulator (i.e., the K/s block in Fig. 2.3) and DCO control input. Third, this new type of digital loop filter can be easily incorporated into other existing digital PLLs and CDRs by re-programming the RTL descriptions for their digital loop filters. Table 2.1 compares some of the key features of the proposed peaking-free digital PLL with the previously-reported ones in

literature.

Note that in Fig. 2.3, a high-pass filter (HPF) with a cut-off frequency at ω_c is applied to the DCO control code (D_{ctrl}) before its K_D -scaled version is subtracted from the phase error (D_{err}). This HPF is necessary to suppress the PLL's static phase offset since otherwise the phase compensation path would always subtract a non-zero value from the phase error, causing a static phase offset that varies with the final D_{ctrl} value. The HPF blocks the DC component of D_{ctrl} and passes only its AC component. This HPF calls for some consideration as its improper design may change the loop dynamics and may even re-introduce jitter peaking. However, the analysis in the next section will show that with a sufficiently low cut-off frequency of the HPF, the PLL can maintain the initial peaking-free characteristic while also keeping the static phase offset at zero.

TABLE I
COMPARISON OF PRIOR PEAKING-FREE ARCHITECTURE

	[3]	[4]	[5]	This work
Filter Type	Analog	Analog	Digital	Digital
Phase Compensation Method	VCDL	Programmable Divider	Programmable Divider	Digital Loop Filter
Phase Compensation Resolution	Continuous	Coarse	Moderate	Fine
Challenges	Design of Noise-insensitive Wide-range VCDL	Coarse Phase Adjustment	Filtering Quantization-Noise of DSM	Design of Linear TDC

Table 2.1. Comparisons of Prior Peaking-Free Architectures.

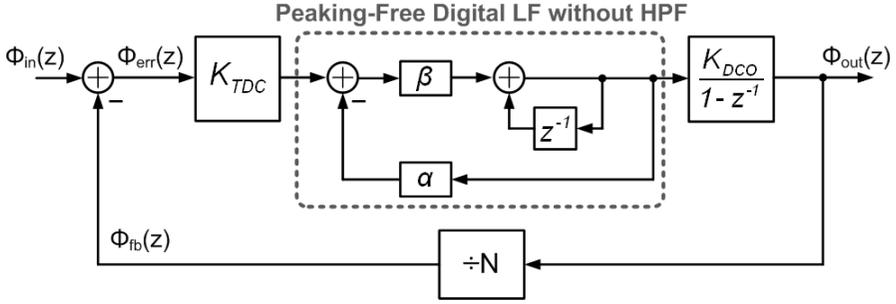


Fig. 2.4. The z-domain model of the proposed peaking-free digital PLL without a high-pass filter.

2.3. Analysis on Peaking-Free Digital PLL Dynamics

This section analyzes the loop dynamics of the proposed peaking-free digital PLL using a continuous-time linear system model. That is, a z-domain discrete-time system model of the PLL is derived first, which is then converted to a s-domain continuous-time system model by approximating z^{-1} as $\exp(-sT_s) \approx 1 - sT_s$. While such approximation is valid only for a frequency range well below the sampling frequency ($1/T_s$), it facilitates the easier analysis which is also sufficiently accurate for PLLs with low enough bandwidths [10].

In the next subsections, the analysis is carried out for two cases: the peaking-free PLLs without and with the HPF. First, the analysis excluding the HPF discusses how to determine the loop parameters such as K_I and K_D in Fig. in order to meet the required bandwidth and damping factor. Then, the analysis including the HPF derives the condition on the HPF's cut-off

frequency that can retain the original peaking-free characteristic while eliminating the static phase offset.

2.3.1. Case Without High-Pass Filter

Fig. 2.4 illustrates the z -domain system model of the proposed peaking-free digital PLL without the HPF. As mentioned earlier, the analysis without the HPF is carried out first in order to determine the basic loop parameters achieving the desired peaking-free characteristics. Based on the model depicted in Fig. 2.4, the transfer function of the peaking-free digital loop filter $H_{LF}(z)$ can be expressed as:

$$H_{LF}(z) = \frac{\beta}{\alpha\beta + (1 - z^{-1})} \quad (2.5)$$

where α and β are the gain coefficients which are related to K_D and K_I in Fig. 2.3, respectively. Then the open-loop transfer function of the PLL $G(z)$ can be expressed as:

$$G(z) = \frac{\phi_{out}(z)}{\phi_{err}(z)} = 2\pi \cdot K_{TDC} \cdot H_{LF}(z) \cdot \frac{K_{DCO}}{(1 - z^{-1})} \cdot T_s \cdot \frac{1}{N} \quad (2.6)$$

where K_{TDC} is the TDC gain and K_{DCO} is the DCO gain, in units of bits/radian and Hz/bit, respectively. In addition, N denotes the dividing ratio and T_s is the sampling frequency or update frequency of the digital filter. By using the aforementioned approximation of $1 - z^{-1} \approx sT_s$, the s -domain open-loop transfer function $G(s)$ can be derived:

$$G(s) = \frac{\phi_{out}(s)}{\phi_{err}(s)} = \frac{2\pi \cdot K_{TDC} \cdot K_{DCO}}{N \cdot T_s} \cdot \frac{\beta}{s\left(\frac{\alpha\beta}{T_s} + s\right)} \quad (2.7)$$

Finally, the overall closed-loop transfer function of PLL $H(s)$ is:

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{NG(s)}{G(s) + 1} = \frac{N \cdot K'\beta}{s^2 + \frac{\alpha\beta}{T_s} \cdot s + K'\beta} \quad (2.8)$$

where K_I is defined as $2\pi \cdot K_{TDC} \cdot K_{DCO}/N \cdot T_s$. As expected, the closed-loop transfer function $H(s)$ in Eq. (2.8) does not contain any zeros.

The expressions for the natural frequency (ω_n) and damping factor (ζ) of the PLL can be derived as the following:

$$\omega_n = \sqrt{K'\beta} = \sqrt{\frac{2\pi \cdot K_{TDC} \cdot K_{DCO} \cdot \beta}{N \cdot T_s}} \quad (2.9)$$

$$\zeta = \frac{\alpha\beta}{2T_s\omega_n} = \frac{\alpha}{2} \cdot \sqrt{\frac{N \cdot \beta}{2\pi \cdot K_{TDC} \cdot K_{DCO} \cdot T_s}} \quad (2.10)$$

Therefore, once the component characteristics such as the TDC gain (K_{TDC}), DCO gain (K_{DCO}), division ratio (N), and loop filter's sampling period (T_s) are known, the proper values for the gain parameters α and β for the desired bandwidth (ω_n) and stability (ζ) can be determined via Eq. (2.9)-(2.10). To avoid the use of full-fledged multipliers in the loop filter, α and β values rounded to power-of-two's or simple combinations of them are generally preferred.

Fig. 2.5 shows the root locus plot illustrating the trajectories of the closed-loop poles as the gain K' increases. As long as the gain K' is sufficiently

low to satisfy $\zeta \geq 1$ in Eq. (2.10), the PLL has only real-valued poles and therefore exhibits no jitter peaking:

$$K' \leq \frac{\alpha^2 \beta}{4T_s^2} \quad (2.11)$$

In comparison, the conventional second-order PLL discussed earlier has the $H(s)$ peak magnitude of $1 + 1/4\zeta^2$, always exhibiting jitter peaking even when $\zeta \geq 1$.

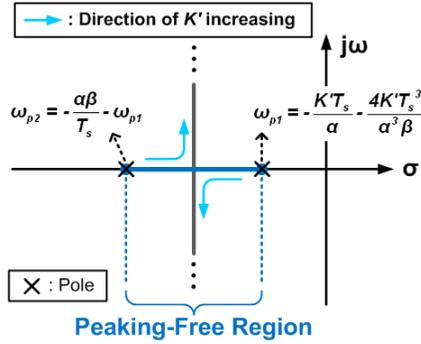


Fig. 2.5. The root locus plot of the proposed peaking-free digital PLL.

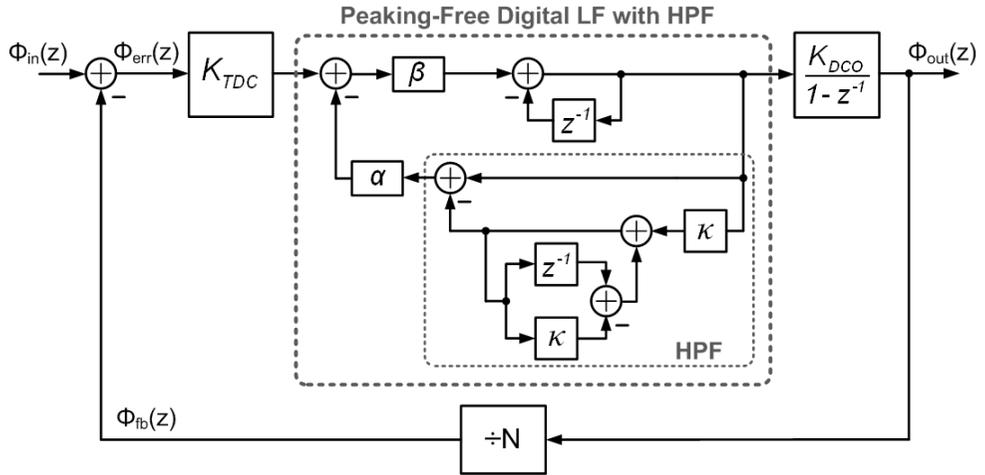


Fig. 2.6. The z -domain model of the the proposed peaking-free digital PLL with a high-pass filter.

2.3.2. Case With High-Pass Filter

Fig. 2.6 now shows the z -domain system model of the PLL including the HPF. As previously stated in Section 2.2, the HPF is necessary to suppress the static phase offset, but its presence may introduce an additional pole-zero pair and change the PLL loop dynamics. The objective of this subsection is to derive the required cut-off frequency of the HPF that can keep the PLL transfer function in Eq. (2.8) unaltered.

First, the z -domain transfer function of the loop filter including the HPF $H_{LF,HPF}(z)$ is:

$$H_{LF,HPF}(z) = \frac{\beta[(1 - z^{-1}) + \kappa]}{[(1 - z^{-1}) + \alpha\beta + \kappa](1 - z^{-1})} \quad (2.12)$$

where κ is the gain coefficient used within the HPF and it can be shown

that the cut-off frequency of the HPF is equal to κ/T_s . Similarly with α and β , the value rounded to a power of two is preferred in order to avoid the use of a full multiplier.

Using the modified loop filter transfer function in Eq. (2.12), the s-domain open-loop transfer function of the PLL, $G(s)$, is derived as:

$$G(s) = \frac{\phi_{out}(s)}{\phi_{err}(s)} = \frac{2\pi \cdot K_{TDC} \cdot K_{DCO}}{N \cdot T_s} \cdot \frac{\beta(s + \frac{\kappa}{T_s})}{s^2(\frac{\alpha\beta + \kappa}{T_s} + s)} \quad (2.13)$$

and the closed-loop transfer function $H(s)$ is given by :

$$\begin{aligned} H(s) &= \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{NG(s)}{G(s) + 1} \\ &= \frac{NK'\beta(s + \kappa/T_s)}{s^3 + \frac{\alpha\beta + \kappa}{T_s} \cdot s^2 + K'\beta s + \frac{K'\beta\kappa}{T_s}} \\ &= \frac{NK'\beta}{s^2 + \frac{\alpha\beta + \kappa}{T_s} \cdot \frac{s^2}{s + \kappa/T_s} + K'\beta} \\ &\approx \frac{NK'\beta}{s^2 + \frac{\alpha\beta}{T_s} \cdot s + K'\beta} \end{aligned} \quad (2.14)$$

Note that the closed-loop transfer function $H(s)$ in Eq. (2.14) converges to the previous one in Eq. (2.8) when κ is sufficiently small compared to $\alpha\beta$. This will serve as the criteria in determining the HPF's cut-off frequency.

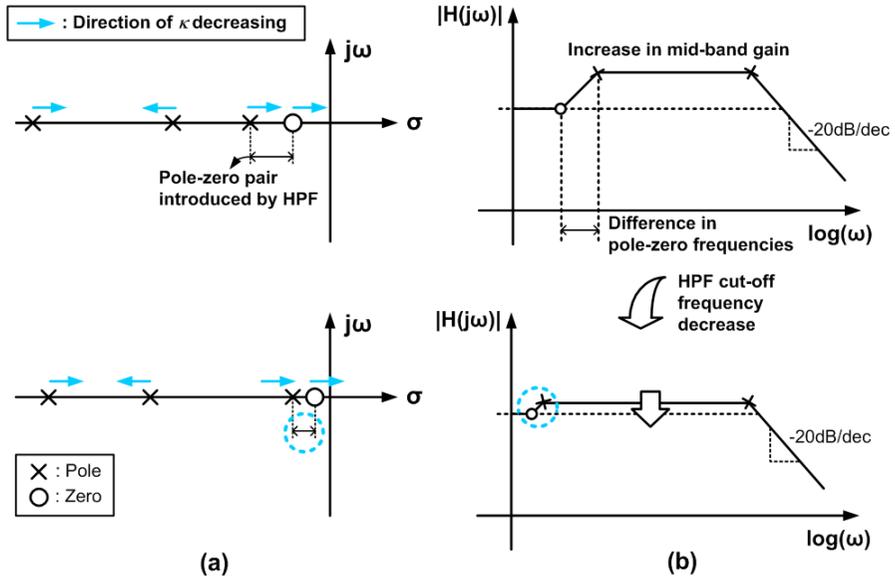


Fig. 2.7. (a) The root locus plot and (b) the Bode plot of the PLL with different values.

Fig. 2.7 presents the root-locus analysis to demonstrate that the original peaking-free characteristic can be retained with a low enough κ . As Fig. 2.7(a) shows, the HPF introduces a pole-zero pair near DC. If there is a difference between the pole and zero frequencies, it may cause an increase in the mid-band gain of the PLL transfer function, as the Bode plot in Fig. 2.7(b) suggests. However, this difference between the pole and zero frequencies diminishes as κ decreases and hence the HPF cut-off frequency decreases. Therefore, it is possible to keep the increase in the mid-band gain below the desired level (e.g. 0.01dB, far below the SONET specification of 0.1dB [6]) by making κ small enough.

Fig. 2.8 plots the simulated increase in the PLL's mid-band gain due to the HPF as a function of the HPF's cut-off frequency, when the target bandwidth and damping factor are 750-kHz and 1.45, respectively. The results suggest that with the HPF cut-off frequency below 11-kHz (corresponding to $\kappa = 2^{-14}$ in this design), almost negligible increase in the mid-band gain below 0.1-dB can be achieved. Note that thanks to the digital implementation of the HPF, there is no apparent difficulty in making κ low besides the increase in the number of bits required to express the internal signals. However, an excessively low cut-off frequency may make the settling of the static phase offset slow when the DCO frequency changes by a large amount. Nonetheless, it does not present an issue when the frequency is fixed and only the phase response is concerned.

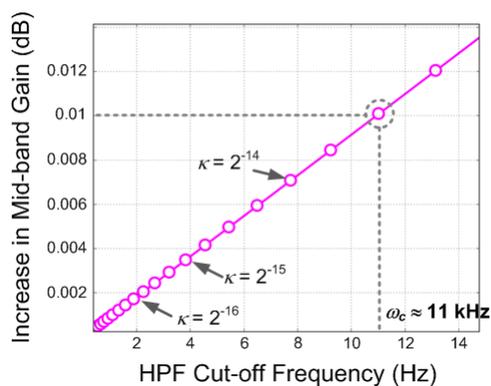


Fig. 2.8. The simulated mid-band gain as a function of the high-pass filter's cut-off frequency.

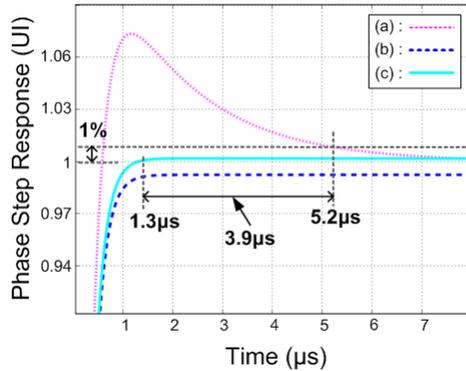


Fig. 2.9. The comparison between simulated phase step responses of (a) a second-order PLL, (b) a peaking-free PLL without HPF, and (c) a peaking-free PLL with HPF.

Fig. 2.9 compares the simulated phase step responses of the PLLs discussed in this section: the conventional second-order PLL, the peaking-free PLL without the HPF, and the peaking-free PLL with the HPF. All the PLLs are designed with almost identical bandwidth of $\sim 750\text{kHz}$ and damping factors exceeding 1 (2.2 for the conventional PLL and 1.45 for the peaking-free PLL). The cut-off frequency of the HPF is set at 8-kHz. As expected, the conventional second-order PLL exhibits an overshoot in its phase step response and therefore a slow settling time of 5.2- μs . On the other hand, the peaking-free PLLs achieve faster settling times of 1.3- μs without such overshoots. The peaking-free PLL without the HPF settles with a finite static phase offset, while the PLL with the HPF has no such static phase offset.

2.4. Circuit Implementation

The proposed peaking-free digital PLL analyzed in the previous section assumes that a linear TDC which can provide a digitized measure of the phase error is available. However, many linear TDCs reported in literature have the gain and resolution characteristics that vary with the operating conditions. For instance, a vernier-type TDC in [11] is made of a chain of delay buffers and phase detectors, and therefore its gain and resolution can change as the delays of the buffers change with the PVT conditions. For another instance, a binary TDC using a single bang-bang phase-frequency detector (BB-PFD) has low costs and may even offer a linearized response in presence of sufficient jitter. But again its effective linearized gain may change significantly with the jitter conditions.

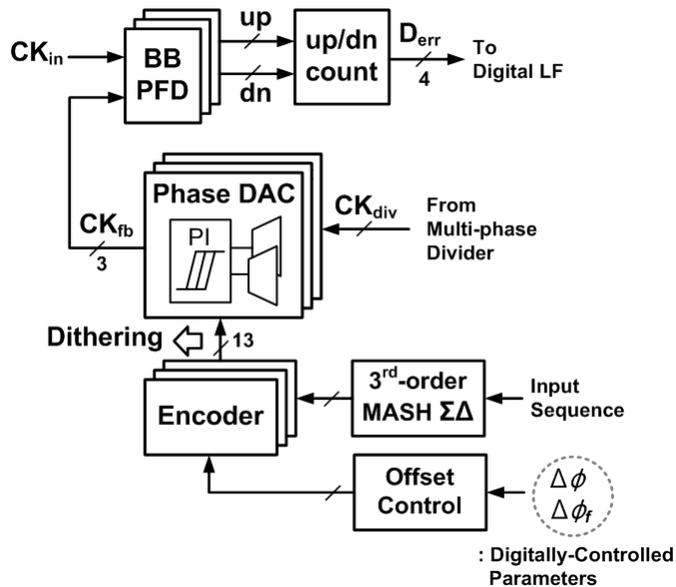


Fig. 2.10. The block diagram of the linear time-to-digital converter (TDC).

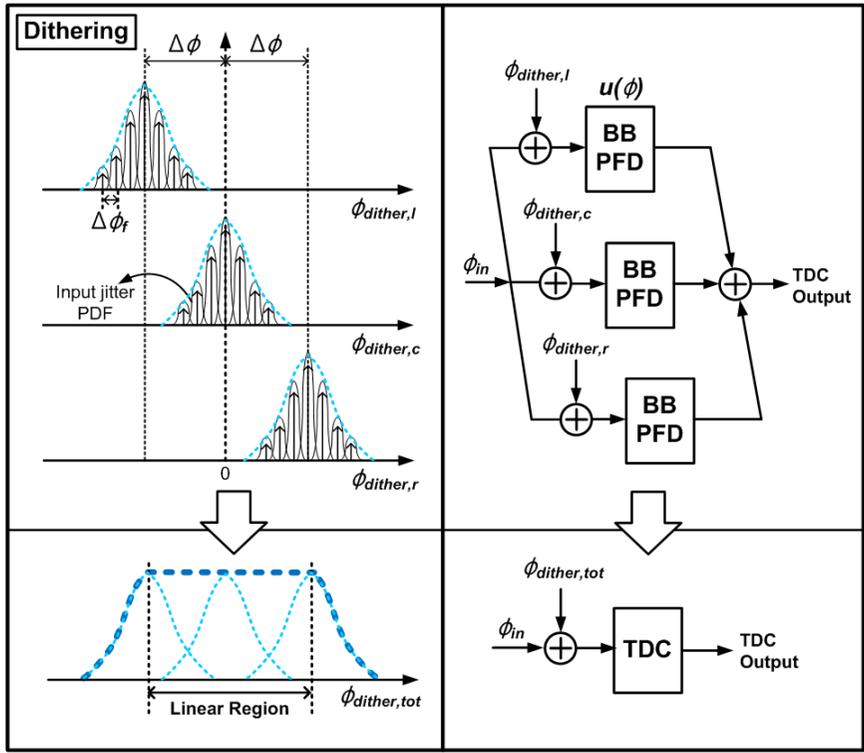
To reduce the sensitivity of the effective linearized gain of the BB-PFD to the jitter conditions, the previous works in [12] and [13] added intentional dither jitter to the input clock of the BB-PFD. For instance, Ref. [12] randomly modulated the delay of the buffer propagating the input clock by switching its capacitance load. Ref. [13] achieved the same by changing the drive strength of the buffer instead. While the added dither can reduce the dependence of the TDC's linearized gain on the external jitter, the resulting TDC characteristic is still subject to PVT variations, since the absolute amount of delay modulation both in [12] and [13] may vary with the PVT conditions.

The linear TDC design in this work adopts the similar design principles with [12] and [13], but improves its sensitivity to the PVT conditions by generating the dither jitter using a phase-domain digital-to-analog converter (phase DAC). In other words, the phase DAC modulates the delay in units of clock periods (i.e. UI) by interpolating between two adjacent clock phases, yielding a constant TDC characteristic that varies only with the operating frequency but not with the PVT conditions.

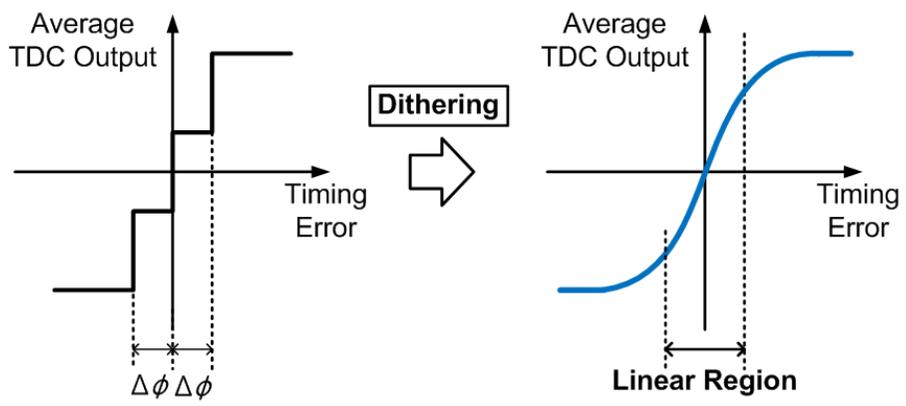
Fig. 2.10 shows the basic organization of the proposed linear TDC. It is composed of three BB-PFDs each of which is triggered by an individually phase-modulated clock using a dedicated phase DAC. The dithering sequence is generated by a third-order multi-stage noise-shaping (MASH) delta-sigma modulator (DSM) that shapes the resulting quantization noise into the high-frequency range. The logic that drives the phase DAC input with the

dithering sequence can also programmably adjust the phase offset between the BB-PFDs ($\Delta\phi$) and the unit step of the dither jitter ($\Delta\phi_f$). And the up/down counter tallies the BB-PFD outputs (up and dn) over input clock period and outputs the difference in the up/dn counts as the digitized phase error (D_{err}).

The operating principle of the proposed linear TDC is illustrated in Fig. 2.11. First, a set of 3 BB-PFDs oversampling the phase error at different offset positions of $-\Delta\phi$, 0 , and $+\Delta\phi$ recovers the coarse information on the phase error. Second, a pseudo-random dither sequence generated by the third-order 1-1-1 MASH-type DSM modulates the phase of each feedback clock triggering the BB-PFDs with a unit step size of $\Delta\phi_f$, therefore statistically recovering the fine information on the phase error. Fig. 2.11(a) shows the individual probability density functions (PDF) of the clock phases triggering the BB-PFDs and the aggregate PDF of all the clock phases combined. When finite input jitter is present, its PDF is convolved with the discrete PDFs of the dither jitter sequence. Note that the aggregate PDF takes approximately a uniform distribution for the range of $-\Delta\phi \sim +\Delta\phi$, resulting in the linearized characteristic of the TDC shown in Fig. 2.11(b). The effective TDC gain is determined largely by $\Delta\phi$, the phase spacing between the BB-PFDs, even when the dither jitter or input jitter further increases. In other words, the use of three BB-PFDs instead of a single one helps maintain a constant TDC gain when the external jitter condition changes.



(a)



(b)

Fig. 2.11. Linearization of the TDC characteristics with added random dither.

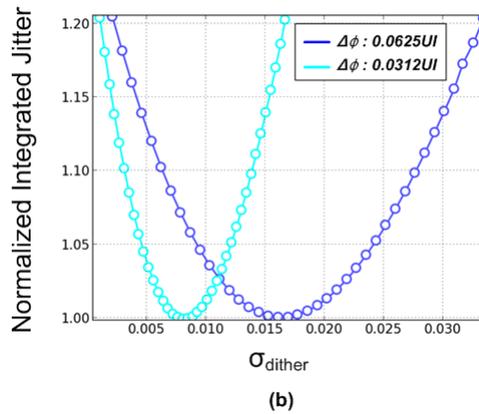
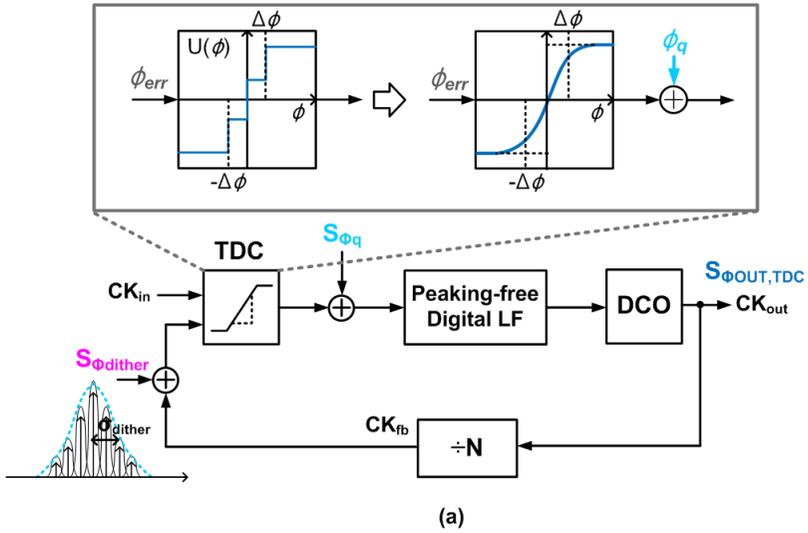


Fig. 2.12. (a) A PLL model for analyzing the noise contribution of the TDC quantization noise and dither jitter, and (b) the normalized total integrated jitter varying with dither jitter (σ_{dither}).

A special consideration is required for the DSM in order to generate the dither sequence with the best-shaped noise spectrum. Based on the theorem from [14], the third-order MASH-type DSM is designed to generate the

longest-length sequence by using the minimum fractional value possible as the input. In addition, the sampling frequency of the DSM is made high (> 140-MHz) so that most of its quantization noise can be filtered by the loop bandwidth less than 2-MHz.

Nonetheless, still a finite amount of quantization is emitted by the TDC which can degrade the overall phase noise performance of the PLL. Fig. 2.12(a) depicts the noise model to analyze the effects of the TDC quantization noise. Using the approach described in [15], the TDC is modeled as a linear gain element followed by an additive white noise source. The effective linearized TDC gain $K_{TDC,eff}$ and the variance of the equivalent TDC quantization noise σ_q^2 can be derived using the following equations:

$$K_{TDC,eff} = \frac{E[\phi_{err} \cdot U(\phi_{err})]}{E[\phi_{err}^2]} = \frac{\int_{-\infty}^{+\infty} U(\phi_{err}) \cdot \phi_{err} \cdot f(\phi_{err}) d\phi_{err}}{\int_{-\infty}^{+\infty} \phi_{err}^2 \cdot f(\phi_{err}) d\phi_{err}} \quad (2.15)$$

$$\begin{aligned} \sigma_q^2 &= E[U(\phi_{err})^2] - K_{TDC,eff}^2 \cdot E[\phi_{err}^2] \\ &= \int_{-\infty}^{+\infty} U(\phi_{err})^2 \cdot f(\phi_{err}) d\phi_{err} - K_{TDC,eff}^2 \int_{-\infty}^{+\infty} \phi_{err}^2 \cdot f(\phi_{err}) d\phi_{err} \end{aligned} \quad (2.16)$$

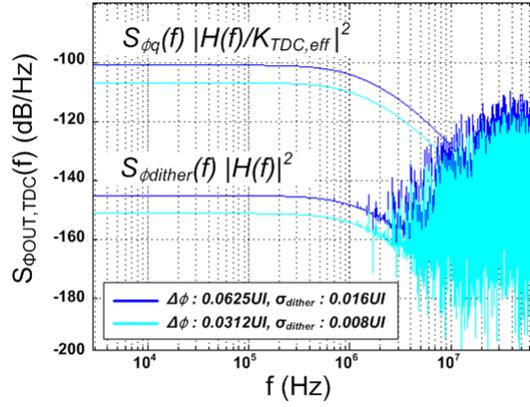
where $U(\cdot)$ is the raw transfer function of the TDC and $f(\phi_{err})$ denotes the PDF of the phase error input including the dither. Using Eq. (2.15) and (2.16), it can be shown that there exists an optimal amount of dither jitter (σ) that minimizes the TDC quantization noise (ϕ_q) for a given BB-PFD phase spacing $\Delta\phi$. Fig. 2.12(b) plots the normalized integrated jitter of $S_{\phi_{OUT},TDC}$ as a function of σ_{dither} for the $\Delta\phi$ values of 0.0625 and 0.0312-UI when the

PLL has a bandwidth of 750-kHz and damping factor of 1.5. The optimal σ_{dither} values are found to be 0.016 and 0.008-UI, respectively. When the high-frequency dither jitter is sufficiently filtered by the PLL bandwidth, the contribution of the quantization noise (ϕ_q) dominates over that of the dither jitter (ϕ_{dither}).

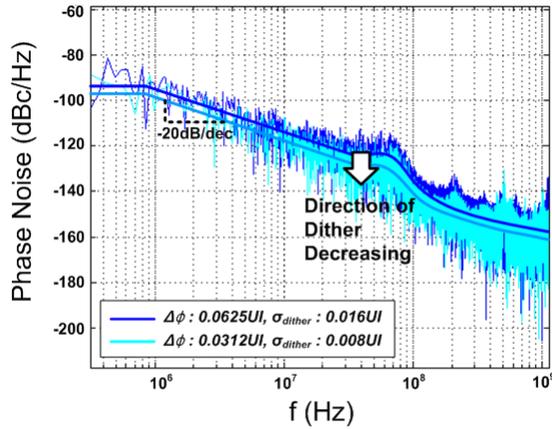
Once this linearized PLL model is derived, the power spectral density (PSD) of the output phase noise due to the TDC quantization noise (ϕ_q) and dither jitter (ϕ_{dither}) can be expressed as:

$$\begin{aligned}
 S_{\phi_{OUT,TDC}}(f) &= S_{\phi_{dither}}(f) \cdot |N \cdot H(f)|^2 + S_{\phi_q}(f) \cdot \left| \frac{N \cdot H(f)}{K_{TDC}} \right|^2 \\
 &= S_{\phi_{dither}}(f) \cdot \frac{(N \cdot K'\beta)^2}{(K'\beta - (2\pi f)^2)^2 + \left(\frac{2\pi\alpha\beta f}{T_s}\right)^2} \\
 &\quad + S_{\phi_q}(f) \cdot \frac{(N \cdot K'\beta/K_{TDC})^2}{(K'\beta - (2\pi f)^2)^2 + \left(\frac{2\pi\alpha\beta f}{T_s}\right)^2}
 \end{aligned} \tag{2.17}$$

Note that both the TDC quantization noise and dither jitter are low-pass filtered before reaching the output. Thus, one way to lower the phase noise contribution of these sources is to lower the bandwidth of the PLL, at the cost of increasing the lock acquisition time.



(a)



(b)

Fig. 2.13. (a) The simulated power spectral density (PSD) of the phase noise contributed by $S_{\phi_{dither}}$, S_{ϕ_q} and (b) total phase noise of the digital PLL including the DCO and input noise.

Fig. 2.13(a) plots the PSD contributions of the two TDC-related noises and Fig. 2.13(b) plots the overall phase noise PSD of the PLL including the DCO

$1/f^2$ phase noise of -120-dBc/Hz at 10-MHz and input jitter of $6.7\text{-ps}_{\text{rms}}$. The fabricated prototype PLL was designed with $\Delta\phi$ of 0.0625-UI and σ_{dither} of 0.022-UI and its output phase noise shows unfiltered TDC noises in the range of $20\sim 100\text{-MHz}$. A possible remedy to reduce this TDC-related noise contribution is to enhance the phase DAC resolution and lower $\Delta\phi$ to 0.0312-UI while keeping the same bandwidth of 750-kHz , as demonstrated in Fig. 2.13(a) and (b).

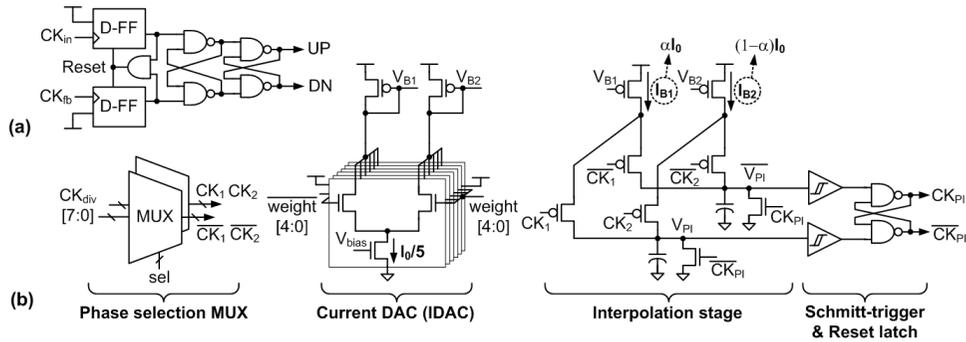


Fig. 2.14. The circuit implementations of (a) the bang-bang phase-frequency detector (BB-PFD) and (b) phase-domain digital-to-analog converter (phase DAC).

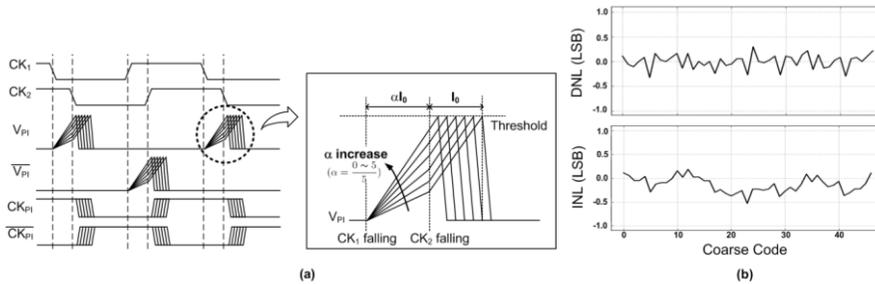


Fig. 2.15. (a) The waveforms illustrating the operation of the phase interpolator (PI) and (b) the measured DNL/INL of the proposed PI.

Fig. 2.14 describes the two key sub-circuit blocks composing the TDC: the BB-PFD and phase DAC. Fig. 2.14(a) shows the BB-PFD circuit which is basically a linear PFD followed by two cascaded SR-latches generating the binary information on the phase or frequency error [16]. On the other hand, Fig. 2.14(b) shows the phase DAC circuit which is a set of two multiplexers followed by a digitally-controlled phase interpolator. Fig. 2.15(a) illustrates the operation of the phase interpolator, which is similar to the one in [17] except that the presented circuit can interpolate both the rising and falling edges of the input clocks by employing a complementary structure. Basically, two switched current sources each biased at I_{B1} and I_{B2} charge a shared capacitor when the respective input clocks (CK_1 and CK_2) fall low. It then gives rise to a ramp signal on the node V_{PI} . When V_{PI} crosses the threshold of a Schmitt-trigger type comparator, its output toggles and so does the phase interpolator output clock (CK_{PI}). It can be shown that the interpolation weight (α) between the two input phases is determined by I_{B1} and I_{B2} , which are digitally controlled by a 5-bit thermometer-coded current-steering DAC as αI_0 and $(1-\alpha)I_0$, respectively.

The main advantage of this phase interpolator design over the other previously-reported ones that rely on contention between two driving stages is that the circuit does not dissipate crowbar currents even when the two input clocks have the different values. For instance, the implemented phase DAC dissipates only 216- μ W when interpolating two 143.75-MHz clocks. Fig. 2.15(b) shows the measured linearity characteristics of the phase interpolator,

with both the DNL and INL being less than 0.5-LSB.

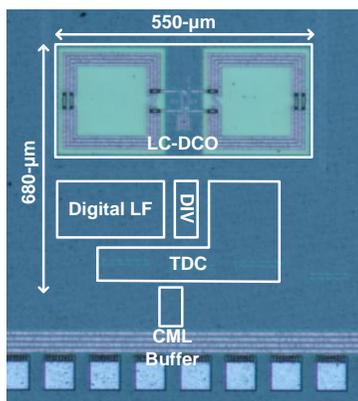


Fig. 2.16. Die photograph of the proposed peaking-free digital PLL.

TABLE II

SUMMARY OF THE PROTOTYPE CHIP PERFORMANCE

Technology	65-nm 1P8M CMOS LP
Supply Voltage	1.2 V
Input Frequency	139 ~ 148.44 MHz
Output Frequency	8.9 ~ 9.5 GHz
Bandwidth	0.3 ~ 1.5 MHz
Integrated Jitter	1.2-ps _{rms} (0.1 to 100MHz)
Phase Noise	-92.8 dBc/Hz at 1-MHz offset
	-114 dBc/Hz at 10-MHz offset
Clock Jitter (÷8 Clock)	3.477 ps _{rms} at 1.15 GHz
	24 ps _{pp}
Settling Time	1.58 μs at 0.7-MHz BW
Power Dissipation	63.9 mW
Active Area	0.374 mm ²

Table 2.2. Performance Summary of the Prototype Digital PLL.

2.5. Measurement Results

The prototype IC of the described digital PLL was fabricated in a 65-nm LP CMOS technology, of which die photograph is shown in Fig. 2.16. The PLL occupies the total active area of 0.374-mm^2 and its performance characteristics are summarized in Table 2.2. From a 143.75-MHz reference clock, the digital PLL generates a 9.2-GHz output clock while operating at a nominal supply of 1.2V. The DCO has a tuning range of 8.9~9.5-GHz and its phase noise is less than -120-dBc/Hz at a 10-MHz offset. The digital PLL consumes the power dissipation of 63.9mW in total, the majority of which, 51mW, is dissipated by the DCO.

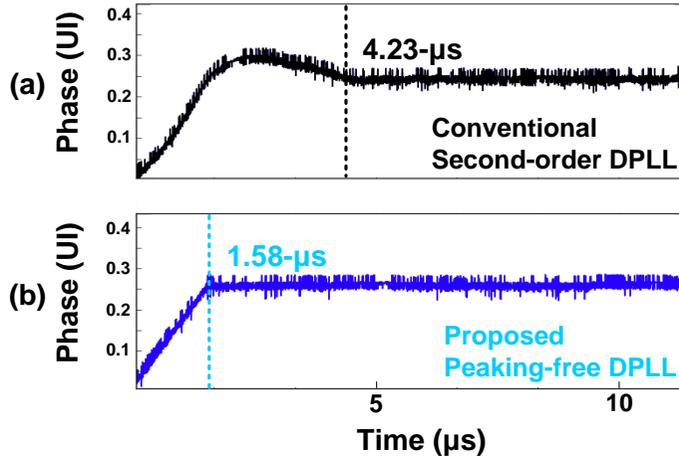


Fig. 2.17. The measured transient response of the PLL feedback clock phase to a 0.25-UI step change in the input clock phase: (a) the conventional second-order digital PLL and (b) the proposed peaking-free digital PLL.

Fig. 2.17 shows the measured phase responses of the feedback clock when the PLL receives a step change in the input clock phase, demonstrating the fast settling response of the proposed PLL without an overshoot. Note that the noise on the measured waveforms is due to the dither jitter on the feedback clock added to linearize the TDC. In fact, the step change in the input clock phase is emulated by introducing a step change in the feedback clock phase instead, which is done simply by using a built-in self-test (BIST) logic that periodically steps the digital code input to the phase DAC. For the purpose of comparison, the digital filter of the implemented PLL can be configured either as a conventional proportional-integral (PI) filter or as the proposed peaking-free filter.

Fig. 2.17(a) is the step response of a conventional second-order digital PLL having a bandwidth of 700-kHz and a phase margin of 82.5° , while Fig. 2.17(b) is the step response of the peaking-free PLL with almost the same bandwidth and phase margin of 80° . As expected, the former exhibits an overshoot due to jitter accumulation while the latter does not. Also, the measured settling times are 4.23- μ s and 1.58- μ s, respectively, showing 2.68 \times fast settling for the proposed peaking-free digital PLL even though the two PLLs have almost the same bandwidths.

Fig. 2.18 plots the measured TDC transfer curve, demonstrating its linear characteristic which is also insensitive to the input clock jitter condition. The TDC transfer curve is again measured using a BIST circuit, which adds a fixed number to the linear TDC output (D_{err}) while the PLL feedback loop is

closed. The resulting static phase offset between the input and feedback clocks of the PLL then corresponds to the input phase error for which the TDC yields the applied number, except that the polarity is inverted. With a BB-PFD phase spacing of 0.063-UI, the TDC has an effective linear gain of 35-steps/UI, which is invariant of the amount of input clock jitter varying from 5.4 to 24.6-ps_{rms}. On the other hand, when the BB-PFD phase spacing is changed to 0.017-UI, the TDC gain increases to 110-steps/UI. Since the BB-PFD phase spacing is controlled by the phase DAC and therefore constant in units of UIs, the TDC gain which is set mainly by the BB-PFD phase spacing is also constant in units of steps/UI regardless of the operating frequency and PVT conditions.

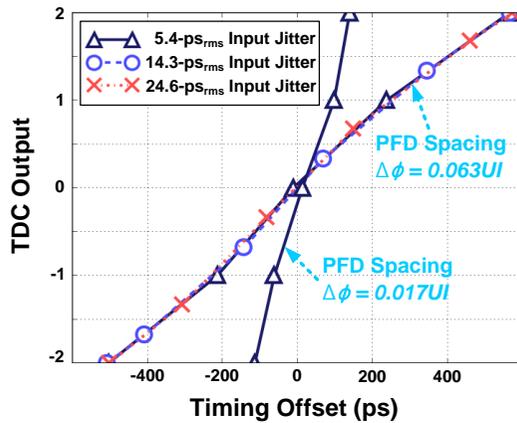


Fig. 18. The measured TDC transfer characteristic with various input jitter conditions and BB-PFD phase spacing $\Delta\phi$.

Fig. 2.19 shows the measured phase noise and integrated rms jitter of the 9.2-GHz output clock from the PLL. The DCO clock of the proposed peaking-free digital PLL has -92.8 dBc/Hz phase noise at 1-MHz offset and -114 dBc/Hz phase noise at 10-MHz offset. As indicated in Fig. 18, the contribution of the TDC quantization noise is observed in the 20~100-MHz frequency range, which agrees well with the simulated result in Fig. 2.13(b). The integrated rms jitter from 0.1 to 100MHz is 1.2-ps,rms, which may have been further reduced by lowering the added dither and hence reducing the TDC quantization noise.

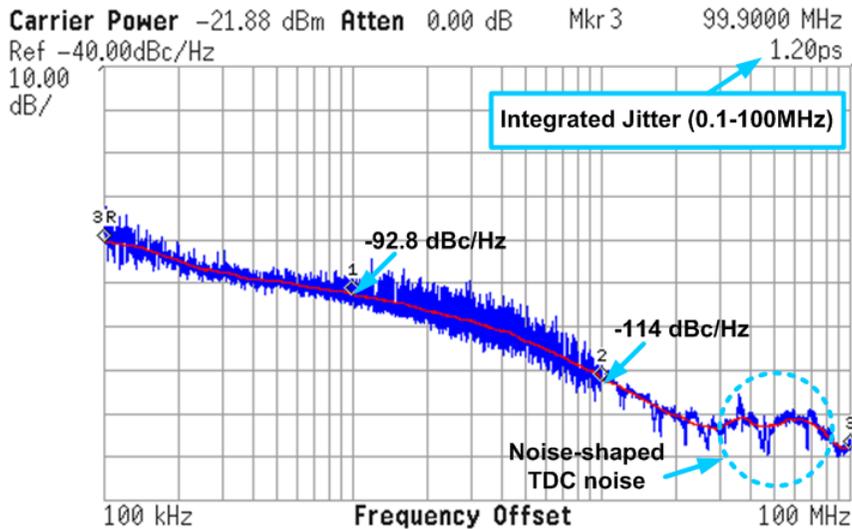


Fig. 19. The measured phase noise and integrated jitter of the 9.2-GHz output clock.

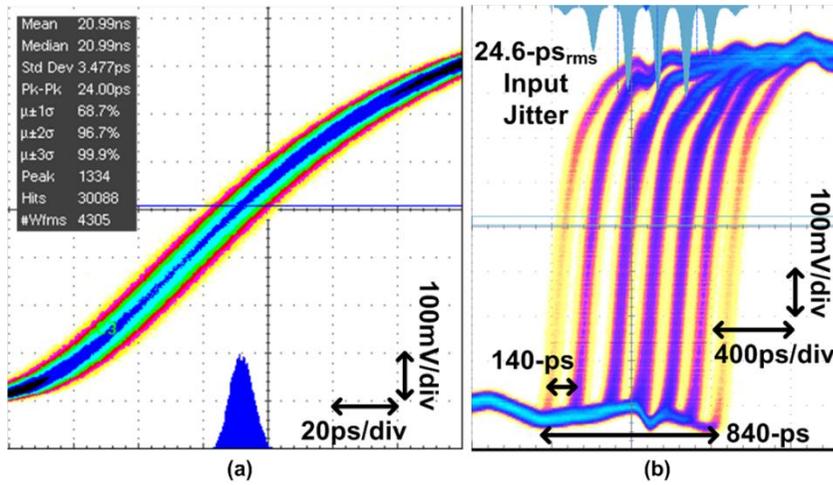


Fig. 20. The measured jitter histograms of (a) the 1.15-GHz divided by 8 output clock and (b) the 143.75-MHz feedback clock including the random dither.

Fig. 2.20(a) and (b) show the measured jitter histograms of the 1.15-GHz divided-by-8 output clock and the feedback clock including the added dither, respectively. The measured jitter on the divided-by-8 output clock is 3.477 ps,rms and 24 ps,pp. The jitter histogram in Fig. 2.20(b) shows the seven quantized phase positions visited by the random dithering pattern of the third-order MASH-type DSM. The pattern takes a discrete Gaussian distribution and the spacing between the quantized phases corresponds to the phase DAC resolution (~ 140 -ps). Even in the case with a large input jitter of $24.6\text{-ps}_{\text{rms}}$, the overall jitter distribution is still dominated by the dither jitter, keeping the TDC characteristic sufficiently linearized and keeping its gain largely determined by the phase step between the BB-PFDs and hence insensitive to

the external jitter conditions. However, as discussed in Section IV, the amount of dither jitter used in this prototype PLL was found a bit excessive, which led to the degradation in the PLL's overall jitter performance. Improving the jitter performance while retaining the linearized TDC characteristic is possible by reducing the dither jitter, for instance, by using a finer phase DAC resolution.

Chapter 3

A Noise-Resilient Tracking Aid for Digital Clock and Data Recovery of Spread-Spectrum Clocked (SSC) Signal

3.1. Introduction of SSC Tracking CDR

Spread Spectrum Clocking (SSC) known as clock dithering described in Fig. 3.1 is widely accepted and utilized method to prevent electromagnetic emission from being concentrated at a certain frequency (i.e. clock frequency). With a typical modulation range of 5000-ppm, the conventional CDRs with sufficient bandwidth are usually capable of tracking the resulting drift in the data timing and no dedicated design is necessary. However, as an extended frequency modulation range up to 50,000ppm described in Fig. 3.1 is demanded in some consumer applications, the CDRs, especially the bang-bang controlled CDRs, must employ some aiding circuits to track the timing drift without compromising the other characteristics. For instance, simply increasing the bandwidth of a bang-bang CDR can increase the steady-state jitter. Also, the sudden change in the frequency slope at the deflection points may cause certain CDRs to lose lock especially in situation that the slope of triangular waveform is getting larger. This thesis describes a SSC tracking aid for a bang-bang controlled CDR that can achieve robust phase tracking while maintaining low steady-state jitter.

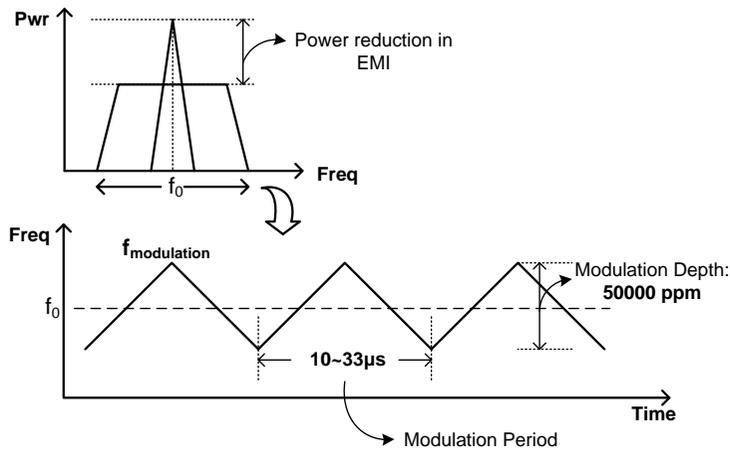


Fig. 3.1. A concept of spread-spectrum clocking (SSC) and time-trend of an example SSC.

One example of CDR without SSC tracking aid that is able to track wide-tracking frequency range is described in [18] which can achieve 5000-ppm of tracking range when the input data is modulated with a 20-kHz triangular waveform. Besides, with SSC tracking aid for a DLL has been describes in [19] which consists of a third-order loop filter and an estimation loop that predicts when the next event of the frequency slope change happens. Conventional phase-interpolating DLL [4] is required to track a finite frequency offset as well as a constant drift in the frequency with zero static phase offset. The author of [19] extends the semi-digital dual-loop first-order CDR of [4] using the third order loop filter and particular tracking aid. To predict the slope change events, the suggested tracking aid of [19] observes the derivative of frequency estimated by the loop filter (i.e. the integral

control path). Albeit being a viable concept in ideal settings, the real signal may bear noises and relying on previous approaches may magnify the dependence on noises.

This thesis proposes a new type of SSC tracking aid for a digital PLL-based CDR that can predict the time instants of the frequency slope can change based on integration rather than previous works. The proposed tracking aid is therefore more resilient to noises and disturbances that may exist in real system. Also, the CDR can control both locking time and accuracy of estimation time instants by adjusting loop parameters of SSC tracking loop.

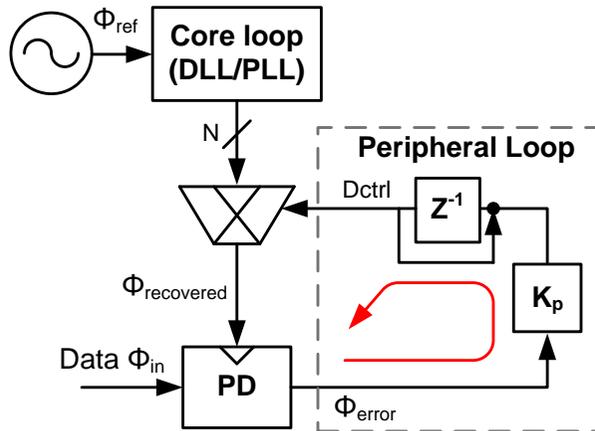


Fig. 3.2. Semi-digital dual loop architecture using digital estimator.

3.2. SSC Tracking Architecture

3.2.1 Conventional Architecture

A conventional overall structure of the third-order CDR with SSC tracking aid [19] is shown in Fig. 3.2. By using phase interpolation, the dual-loop can provide unlimited phase shift without the use of a voltage-controlled oscillator (VCO) [4]. The core loop multiplies reference clock frequency up by N -times. And the phase DAC controlled by the digital estimator generates multi-phase clocks. Using the estimation approach [19], a simple third-order loop filter that contains three accumulators can predict the phase of future bits of the triangular profile by estimating the phase, frequency, frequency ramp rate of the transmitter.

By applying final-value theorem in third order loop filter, according to Eq. (3.1), we can derive only higher order (>2) system can track frequency modulation with zero steady state phase estimation error.

$$Phase(\infty) = \lim_{x \rightarrow +\infty} s \cdot R(s) \cdot [1 - H(s)] \quad (3.1)$$

$R(s)$ can be substituted by s^{-3} for unit frequency ramp transfer and $H(s)$ means the transfer function of the CDR loop. However, third-order system has worse tracking ability than a second-order when the polarity of the frequency ramp rate changes abruptly. This is because CDR may exhibit an overshoot when the slope of the frequency suddenly changes its polarity since it takes some time for the filter components to readjust for the new slope (Fig. 3.3(a)). Hence, it is clear third order loop filter must have some tracking aid to

predict the accurate switching point of triangular profile.

The architecture of digital estimator which employs third-order digital loop filter is shown in Fig. 3.3(b) using previous tracking-aid. This estimator adopts the complex of two frequency ramp rate accumulators and two MUXes. When the slope of the frequency ramp changes, tracking-aid transmits the signal that estimates the ramp polarity to MUXes. When the output of tracking aid low, negative ramp rate accumulator turns on, and reversely, positive one turns on in opposite condition. The ramp accumulators saturate to maintain the correct polarity to help convergence. Therefore the CDR recognizes the triangular frequency as the monotone increasing, so track SSC profile without the phase offset.

There are two kinds of the previous SSC tracking aid in Fig. 3.3(c). The first method of estimating modulation uses differentiator that the output of frequency accumulator is differentiating by subtracting each sample from the previous one (Fig. 3.4(a)). And the other one using comparator that compares the triangular waveform (V_{freq}) to the reference level crossing V_{freq} to generate a square wave that is 90 degree offset from switching point (Fig. 3.4(b)). A digital PLL (DPLL) locked by these outputs is used to switch accumulators using MUXes. In practice, these previous SSC tracking aid cannot estimate completely the changing point due to various circuit non-idealities such as unwanted bubbles in the digital bits.

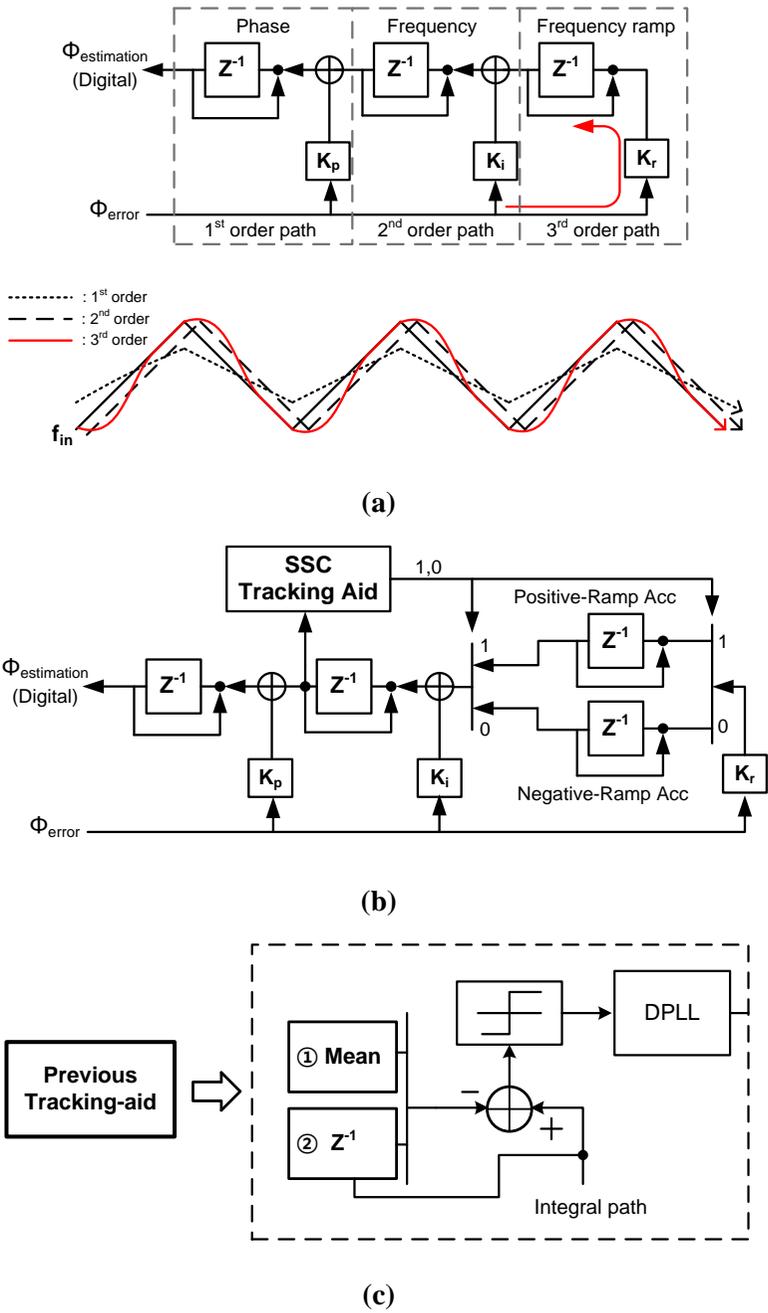
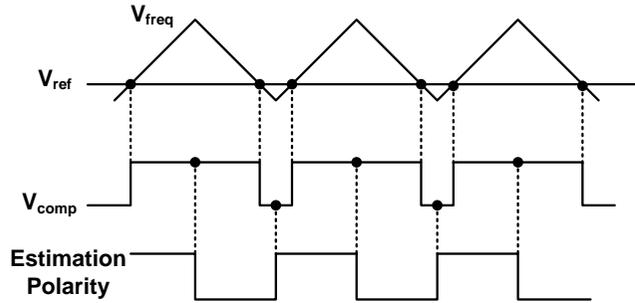


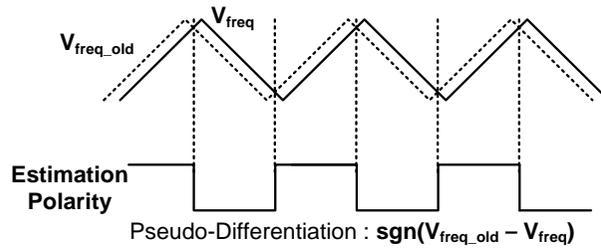
Fig. 3.3 (a) Overshoot due to 3rd-order system (b) 3rd-order digital estimator using previous tracking aid (c) previous tracking aids.

The previous approaches have several drawbacks oriented by noises or disturbances. First, the reverse estimation can occur. Both cases of using pseudo-differentiation and comparator, if there are bubbles in the integral path, in a moment, the opposite frequency ramp-rate accumulator can turn on and make an overshoot in the CDR loop. Especially, if there are noises in the integral path near the crossing point, the method using a comparator suffers from the above phenomena repeatedly every modulation period. Second, if the ramp rate is not large, glitches in random locations can occur easily. This problem can be solved by running pseudo-differentiation at a much slower sample rate of the tracking loop such that the change in frequency will be larger between samples. But, the slow sample rate can degrade accuracy between the output of DPLL and real frequency ramp polarity. And the estimation can't occur in accurate changing points, and CDR performance gets worse. Finally, the most vulnerable point is that the loop can be failed regardless of past operation. No matter how accurate the loop may be locked in an optimal point in a past moment, if there are glitches in the present situation, the overall loop will be unstable.

In view of these drawbacks, the proposed approach overcomes the limitation caused by noises and disturbance. Simultaneously, we can achieve our goal in that the discrepancy between the point estimated and real spot that ramp rate changes occur in our work is smaller than in previous.



(a)



(b)

Fig. 3.4. Prediction of previous tracking aids (a)using pseudo-differentiation, (b) comparator.

3.2.2 Concept of Integration-based SSC Tracking Loop

In Fig. 3.5, a triangular SSC frequency profile (V_{freq}) that means digital codes in integral path of the digital loop filter alternates between the rising slope and the falling slope. As illustrated in Fig.5, The basic idea is to *integrate* the difference between the estimated frequency and its mean value and observe its polarity. Concretely, if the reference level (V_{ref}) is settled at the middle point of the triangular SSC profile, the integral of the difference between V_{freq} and V_{ref} indicates the polarity of the frequency ramp. So, when

the reference level is locked, we can estimate the switching point by most-significant-bit (MSB) of integral of $(V_{freq}-V_{ref})$. As we concerned before, a common problem with previous tracking loop stems from the fact that the real system bear the noises and glitches exist in random location of SSC profile.

In comparison with the previous works, a new type of frequency modulation tracking loop, which we call SSC tracker, provides a noise-resilient way of predicting the polarity change. Tolerating glitches when they exist in mid-point of SSC profile is of great concern in previous mean-level scheme in Fig. 3.4(b). In Fig. 3.4(b), the tracking method try to find the middle point of comparator voltage (V_{comp}) but, if there are glitches near the crossing point between V_{freq} and V_{ref} , comparator voltage may suffer distortion. Also, as we can see, in the case of with another tracking method (Fig. 3.4(a)), glitches in every location make trouble.

In our new type SSC tracking loop as illustrated in Fig. 3.5, However, can estimate accurate changing-point of polarity regardless of glitches, especially in mid-point of SSC profile because there is a very low probability of the integral waveform, whose MSB coincides with the polarity of the frequency slope, crossing zero value more than once within each half SSC period. When the integral waveform crosses a zero, the frequency error is either at its maximum or minimum and is least likely to change its direction of the integral. On the other hand, other schemes, as mentioned, are susceptible to glitches in the estimated outputs due to multiple zero crossing events within a

half SSC period.

Fig. 3.6 shows the simulated timing-error between the real and estimated point verses signal-to-noise-and-distortion ratio (SNDR) derived in random Gaussian white noise and spurs. In comparison with previous algorithm (Fig. 3.6(a)), it can be seen that new type SSC tracking algorithm (Fig. 3.6(b)) is more suitable for withstanding noise. The simulated result of proposed algorithm shows better timing accuracy than that of previous one in the low SNDR. Furthermore, maximum timing error of proposed algorithm is also smaller than that of previous one. Because the worst case of proposed algorithm results in divergence of reference level to positive/negative value, maximum timing error does not exceed half period of SSC modulation. On the other hand, timing error of previous one can occur at any point in certain case. However, the pre-requisite to this SSC tracking aid is the accurate knowledge of the frequency's mean value (V_{ref}). If this mean value is not accurate, the integral value can keep accumulating the residual error and may go out of bound. So, when designing the SSC tracker, designers have to bear in mind the mean-tracking is the prerequisite of implementation.

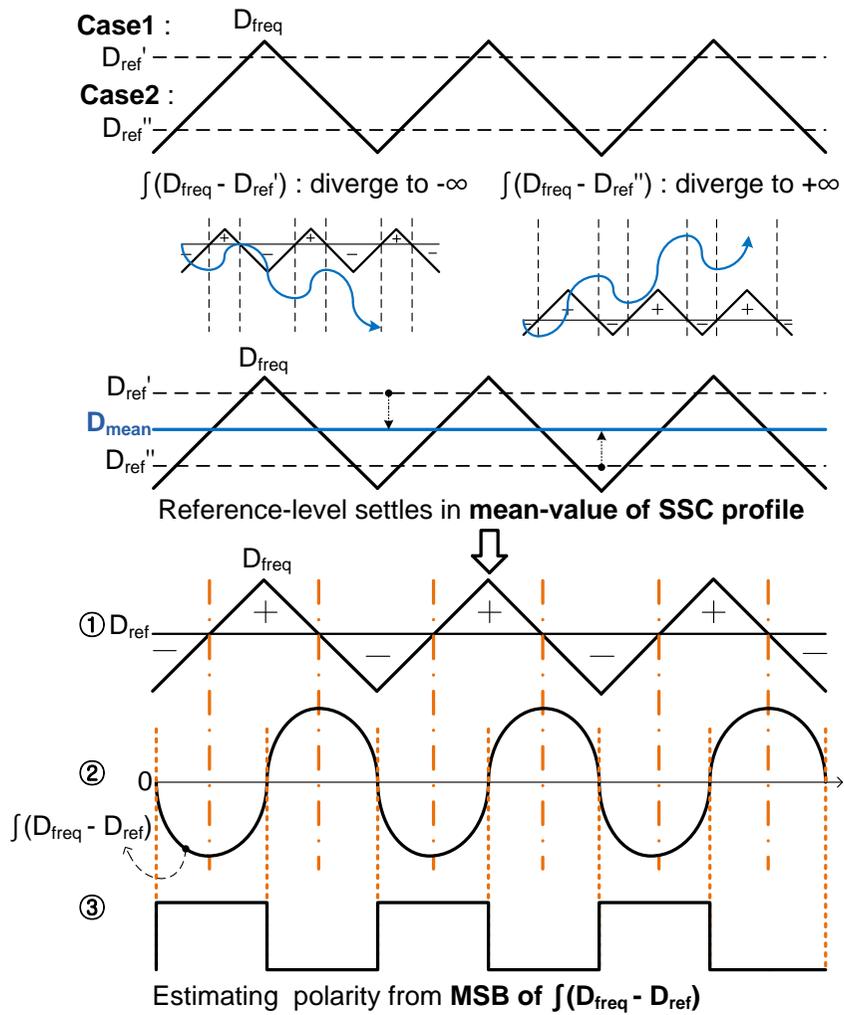


Fig. 3.5. SSC polarity change prediction based on integration.

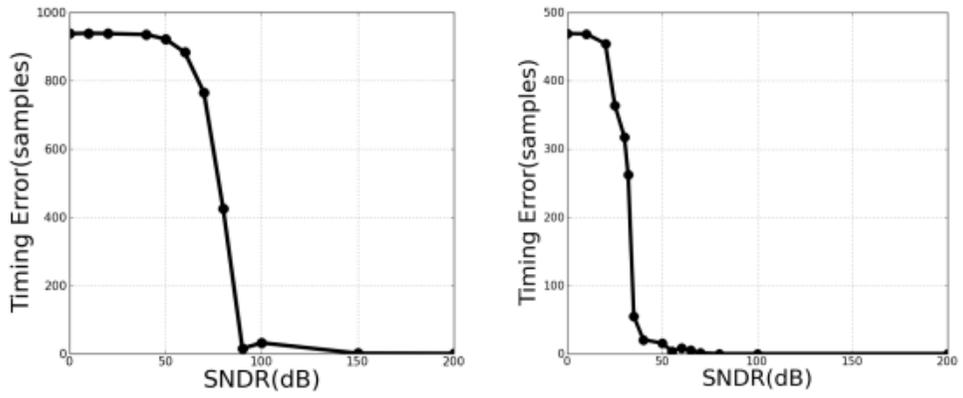


Fig. 3.6. SNDR - polarity timing error.

3.3 CDR Architecture with SSC Tracking Loop

3.3.1 SSC Tracking Loop

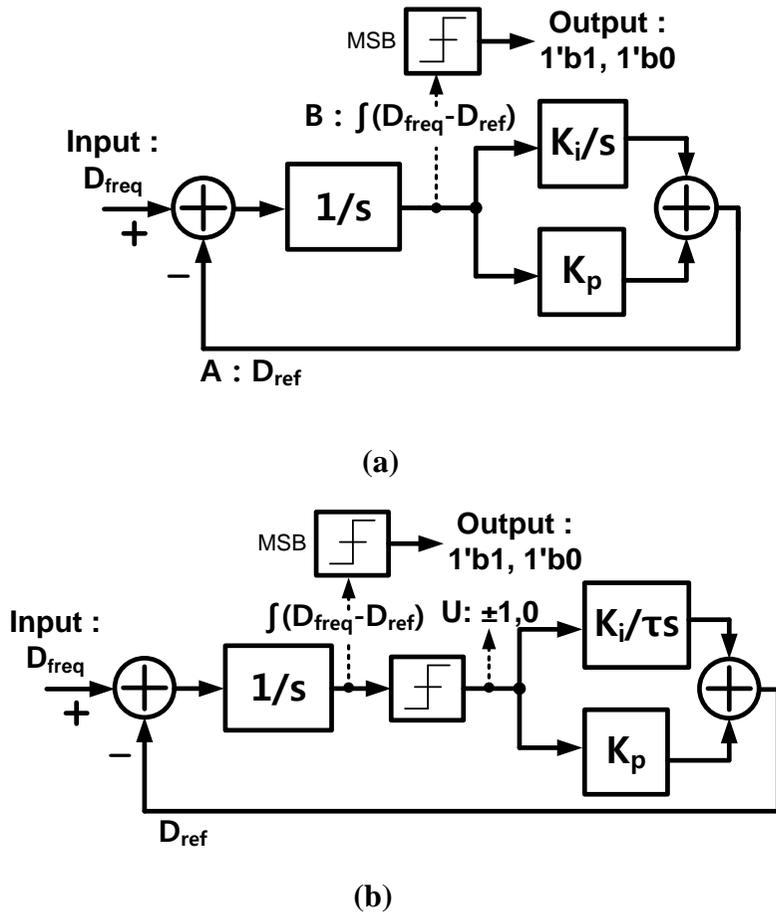


Fig.3.7 Block diagram of (a) the SSC tracking aid using linear controller (b) SSC tracking aid using bang-bang controller.

As mentioned earlier section, the prerequisite which is needed to implement proposed algorithm in Fig. 3.5 is how reference-level track the mean value of triangular waveform. SSC tracking loop aims to control reference level to be adjusted by feedback loop. And finally, SSC tracker generates output signal estimating accurate changing point of frequency ramp rate and sets the reference-level to mean value of frequency profile, simultaneously.

Fig. 3.7 illustrates the block diagram of our SSC tracking loop. The input of SSC tracking aid is integral term of whole CDR loop that is recovered triangular profile expressed by digital codes. The output of the accumulator before linear/bang-bang controller that integrates the difference between integral term and reference level means the information of time instants of the frequency slope (Fig. 3.5-②). MSB of this output implemented with signed bits estimates the polarity of the slope of frequency ramp (Fig. 3.5-③). Linear/Bang-bang controller detects the integral of $(V_{\text{freq}}-V_{\text{ref}})$ and generates the scaled error by linear/bang-bang algorithm. Next, this scaled error adjusts the reference-level. At first, the loop employs an integral control feedback system that tries to settle ref-level in the mean-value of integral term. However, the integral control can make the feedback unstable because it generates two poles in the low-frequency region. To stabilize this reference-level control loop using feedback, proportional control that provides a compensating zero is needed. Note that the mean value is determined as a

sum of the scaled version of the accumulated frequency error and the integral version of the accumulated error. The control gain for each term is denoted as K_p (proportional gain) and K_i (integral gain), respectively. Hence, the sum of proportional and integral path outputs constitutes the reference level that performs mean-tracking role.

Controller can be implemented by different way Linear/Bang-bang controller. As we choose what kind of controller (linear/BB), many property of our SSC tracking loop changes. The following subsections discuss advantages/disadvantages stem from using different controllers. Basically, we implemented our tracking loop with linear controller.

A. Linear controller

Fig. 3.7(a) shows block diagram of the proposed SSC tracking loop using linear controller. It is interesting to note that the dynamics of the described mean-tracking loop (path : Input to A) is identical to a second-order linear PLL, with open-loop transfer function and closed-loop transfer function are expressed as:

$$G(s) = \frac{sK_p + K_i}{s^2} = \frac{2\zeta\omega_n + \omega_n^2}{s^2} \quad (3.2)$$

$$H_1(s) = \frac{sK_p + K_i}{s^2 + sK_p + K_i^2} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.3)$$

Where ω_n and ζ are the natural frequency and damping factor of the second-order system, respectively.

And transfer function from input to integral waveform (B) is:

$$H_2(s) = \frac{s}{s^2 + sK_p + K_i^2} = \frac{s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.4)$$

To estimate the locking time and stability of SSC tracking loop, we have to analyze both $H_1(s)$ for reference level and $H_2(s)$ for integral of (D_{freq} - D_{ref}) waveform.

To all-digitally SSC implement our tracking loop, we need to convert continuous-time model (Fig. 3.7(a)) to discrete-time model. The discrete-time open loop transfer function (path Input to A) can be expressed as:

$$G(z) = \frac{1}{1 - z^{-1}} \cdot [K_{p,discrete} + K_{i,discrete} \cdot \frac{1}{1 - z^{-1}}] \quad (3.5)$$

Where $K_{p,discrete}$, $K_{i,discrete}$ are discrete-time system proportional, integral gain respectively. An approximate continuous-time transfer function can be obtained by substituting $e^{-sT_{sampling}} \approx 1 - sT_{ref}$ for z^{-1} .

And compared with Eq. (3.2), discrete-time gains ($K_{p,discrete}$, $K_{i,discrete}$) can be derived as :

$$K_{p,discrete} = 2\zeta\omega_n \cdot T_{sampling} \quad (3.6)$$

$$K_{i,discrete} = 2\zeta\omega_n \cdot T_{sampling} \quad (3.7)$$

Where $T_{sampling}$ is the update period of the loop.

The example SSC tracking loop is designed for ω_n of 80π and $\zeta = 0.7$ and discrete-time loop gains are $K_{p,discrete} = 2^{-19}$, $K_{i,discrete} = 2^{-38}$, respectively. Fig. 3.8 shows transient behavior of reference level of SSC tracking loop using linear controller with above loop parameters. It can be seen that reference level for the SSC input, which is expressed DCO input digital code,

settles in the mean-level of the triangular profile. The locking behavior is determined by the closed loop transfer function $H_I(s)$.

Fig. 3.9 shows transient waveform of integral of $(D_{freq}-D_{ref})$ which is corresponding to $H_2(s)$. we estimate the accurate changing point of frequency modulation in effect. In steady-state, the MSB of node B in Fig. 3.7(a) can be synchronized with the polarity of frequency ramp.

The above analysis and existing linear system theories are convenient to make tracking loop with linear controller so using linear controller seems rational, in practice, however, with linear controller, we have difficult time implementing the accumulator in integral path of tracking loop. Because digital codes in node B in Fig. 3.7(a) must be added to accumulator on integral path without making any adjustment. And then, after applying gain factor to this codes and the accumulator on integral path recover the reference level with proportional path. In other words, the register on integral path must accommodate the sum of bits of accumulator in front of controller and bits of reference level. Originally, reference-level related to DCO control codes is not very large. But accumulator in front of controller need to bulky register because of operating integration and the latter is primary trouble-maker component. In high-speed digital system, a large size of register can degrade circuit performances causing setup-time violation. So, several attempts to solve these problems must be exist like pipelining technique (but can increase latency problem).

B. Bang-bang controller

Many timing loops in high-speed environments, such as PLL/DLL/CDRs, use binary, bang-bang phase detection since their circuits are simple, fast, and accurate to digital implementation. Our SSC tracking loop is also variant these timing loops, so we can use bang-bang controller like bang-bang PD of other timing circuits.

However, strongly nonlinear transfer characteristic of bang-bang controller hinders the analysis of loop characteristics. But, by aid of established analysis of bang-bang architecture [21]-[23], we can derive the equivalent linear model and design SSC tracking loop using bang-bang controller.

The block diagram in Fig. 3.7(b) shows bang-bang controlled SSC tracking loop. It can be modeled by the bang-bang controller that provides the determined output, $\pm 1, 0$ each indicating that only polarity of integral difference of reference level and SSC profile digital codes. In discrete-time model of this bang-bang controlled loop, for each error detected, the proportional path makes a step of $\omega_{bb} \cdot T_{sampling}$ and the integral path makes a step of $\omega_{bb}/\tau \cdot T_{sampling}$ either up or down. In case of a zero loop delay ($t_{d,eff} = T_{sampling}$), the factor $\kappa = \tau/t_{d,eff}$ that determines the stability of the bang-bang timing loop become $\tau/T_{sampling}$ [21]. the larger the factor κ , the smaller the dithering contribution of integral-control loop and the lower the total dithering jitter [21]. Like the preceding, we can implement the

tracking loop using 2nd order bang-bang parameters(ω_{bb} , τ , K_p , K_i). In the bang-bang PLL analysis in [21], linear parameters K_p , K_i are ω_{bb} , ω_{bb}/τ respectively. In the end, we have to get the discrete-time proportional/integral gain $K_{p,discrete}$, $K_{i,discrete}$ we already denoted. Continuous time linear parameter can be written, $K_i = \omega_n^2$ and $K_p = \omega_n^2 \cdot \tau$, and then, discrete time gains are described as $K_{p,discrete} = \omega_n^2 \cdot \tau \cdot T_{sampling}$, $K_{i,discrete} = \omega_n^2 \cdot T_{sampling}^2$. Hence, by using above linearization analysis, we can implement tracking loop with target parameters.

Furthermore, using bang-bang controller provides smaller usage of register distinct from using linear one. Basically, the size of register on integral path has no relation to that of accumulator in front of controller. Because the output of bang-bang controller can be only admitted finite discrete value ($\pm 1, 0$). Therefore, digital implementation of bang-bang controller can be achieved easier than that of linear controller. And with existing analysis mentioned above, we can derive our circuit parameters for adequate specification.

In subsequent section, we will discuss the analysis of the parameters that determines loop characteristics. So throughout subsequent subsection, it is explained that how the dynamics of the described proposed tracking loop analyzed in Section 3.3.1 influence the circuit specification and analyze the relationship (trade-offs) among loop parameters.

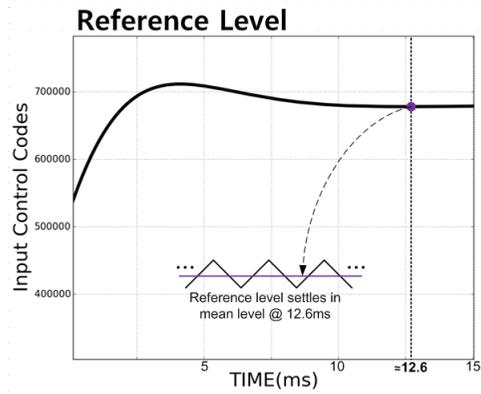


Fig. 3.8. Transient waveform of reference level on linear mean tracking loop.

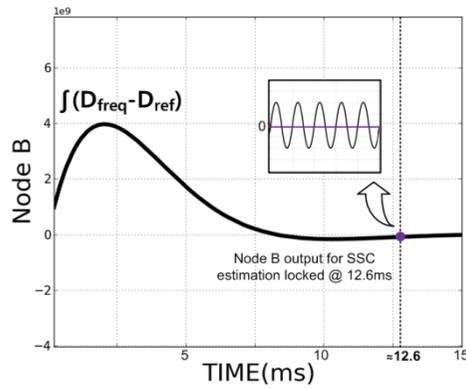


Fig. 3.9. Transient waveform of integral ($D_{freq} - D_{ref}$).

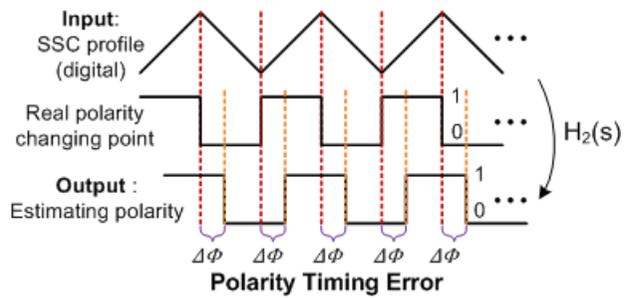


Fig. 3.10. Concept of polarity timing error.

3.3.2 Trade-offs among Parameters

Above all, in this section, we introduce some definitions of primary specifications of our SSC tracking loop in advance.

First, we call the discrepancy in predicting the slope change events “polarity timing error”. In other words, polarity timing error means the time-difference between real changing point of polarity of frequency ramp and MSB of integral of $(D_{freq}-D_{ref})$ in steady-state. In relationship with polarity timing error, “locking time” of SSC tracking loop is the moment that polarity timing error is the smallest value in given loop parameters. Strictly speaking, the locking time in our tracking loop is different from that of general PLL/DLLs. However, both cases can be equal each other in that locking time means the moment reaching steady-state. Now that we have decided on circuit parameters and set the design goals, we need a methodology to find the optimal set of design parameters that yield both of minimum locking time and minimum polarity timing error. There are several parameters that affect mentioned specifications as follows:

- 1) ω_n (bandwidth)
- 2) ζ (damping factor)
- 3) f_{SSC} (SSC modulation frequency)

In this section, the optimization of loop parameters related in polarity timing error and locking time will be discussed. Note that the goals of subsequent analysis is how can we derive adequate loop parameters that make the shortest value of locking time as long as polarity timing error maintains minimum.

Fig 3.10 presents the concept of polarity timing error in SSC tracking loop

that input is SSC profile and output is estimating polarity pulse from node B (Fig. 3.7(a)) in steady state. In previous section, the transfer function $H_2(s)$ was derived from the loop in Fig. 3.8(a) that has corresponding input/output in Fig. 3.10. If we consider SSC profile input signal is correspond to sinusoidal input $x(t) = A \cdot \cos \omega t$, SSC modulation amplitude/frequency come under A/ω , respectively.

When the input form is sinusoidal as above, the output $y(t)$ is expressed as:

$$y(t) = A \cdot |H_2(j\omega)| \cdot \cos[\omega t + \angle H_2(j\omega)] \quad (3.8)$$

Thus, from above frequency response, the phase difference $\angle H_2(j\omega)$ is exactly same as polarity timing error of our tracking loop in Fig. 3.11. Then, the frequency response of $H_2(s)$ can be calculated from substituting $s=j\omega$ in Eq. (3.4) as :

$$H_2(j\omega) = \frac{j\omega}{(K_i - \omega_n) + j\omega \cdot K_p} \quad (3.9)$$

It follows that the polarity timing error $\angle H_2(j\omega)$ can be expressed as:

$$\angle H_2(j\omega) = \tan^{-1} \frac{\omega \cdot K_p}{K_i - \omega^2} \quad (3.10)$$

Where $\omega = \omega_{SSC}$, $K_i = \omega_n^2$, $K_p = 2\zeta\omega_n$. And it follows that :

$$\angle H_2(j\omega) = \tan^{-1} \frac{\omega_{SSC} \cdot 2\zeta\omega_n}{\omega_n^2 - \omega_{SSC}^2} = \tan^{-1} \frac{2k\zeta}{k^2 - 1} \quad (3.11)$$

Where k is the ratio between ω_n and ω_{SSC} ($k = \omega_{SSC}/\omega_n$).

Fig. 3.11 and 3.12 illustrate the effects of above parameters on polarity

timing error. As seen in Fig. 3.11, under condition that the damping factor is constant value ($\zeta = 0.7$), when the natural frequency get larger and ratio k get smaller, polarity timing error increases. This plot shows increasing monotonically because the ratio k is located in linear region of arctangent curve $\angle H_2(j\omega)$.

Similarly, Fig. 3.12 plots the resulting polarity timing error with respect to ω_{SSC} (modulation frequency). While the damping factor ζ is fairly constant for stability related to smaller polarity timing error, polarity timing error is inversely proportional to modulation frequency ω_{SSC} . Strictly speaking, the ratio k aforementioned parameter makes polarity timing error vary. As seen in Fig 3.12, we can also find not only effects of modulation frequency but also that of parameters that have an effect bandwidth such as sampling frequency of digital filter because bandwidth is getting wider as sampling frequency getting faster.

Next, dissimilar to the case of polarity timing error, the locking time of our tracking loop can be estimates by loop dynamics of second-order PLL. As described in [24], generally, locking time of second order approximation to transient response can be estimated as follow:

$$T_{settling} \approx \frac{1}{\zeta\omega_n} \cdot \ln\left[\frac{1}{\sqrt{1-\zeta^2}}\right] \quad (3.12)$$

Eq. (8.12) means that the locking time is minimized when $\zeta\omega_n$ is maximized.

Therefore, unfortunately, there exists a trade-off between the locking time

and the accuracy in predicting the slope change events. In the condition damping factor is fixed, low bandwidth (high k) is desired to produce a steady mean value of reference level that does not change within an SSC modulation period while high bandwidth is desired to expedite the locking process.

3.3.3 Additional SSC Tracking Aid

To circumvent the limitation results from trade-off mentioned above section, we investigated the use of additional tracking aids. It is important to note that the key factor is how to reduce the locking time as long as keep minimum polarity timing error.

First, we can think about confinement stem from initial value. Locking time of SSC tracking loop may become dependent upon the initial value because of fixed output of bang-bang controller or confined size of register of linear controller, respectively. So, a proper initialization helps SSC tracking loop lock quickly. Fig. 3.13(a) shows the initialization method. During the initialization period such as certain calibration sequence, the SSC tracking aid observes the estimated frequency value for a given period and uses the averaging point between the minimum and maximum value as the initial value.

Next, Fig. 3.13(b) plots reference level using the gain-boosting method. Likewise, synchronized with one of the calibration signal such as frequency detection period, during calibration sequence, the SSC tracking loop operates

in condition that reference level tracks with larger proportional gain than that of normal mode. As using this additional module, while the locking time is fast, we can see timing accuracy is degraded during gain-boosting mode. During normal CDR mode, SSC tracking loop operates at moderate proportional gain and poor timing accuracy is recovered and consequently, the overall locking time is reduced without degrading other performance. So, final value of polarity timing error in steady-state is same as that of SSC tracking loop without gain-boosting aid.

Therefore, the proposed additional tracking aids mitigate the effects come from trade-off between locking time and the accuracy in predicting the slope change events. The current reference tracking loop implementation has been also added these additional tracking aids. The locking time with additional tracking aids, while tracking loop maintaining the same timing accuracy compared with normal-mode, is reduced from 13~16ms to 8~9ms.

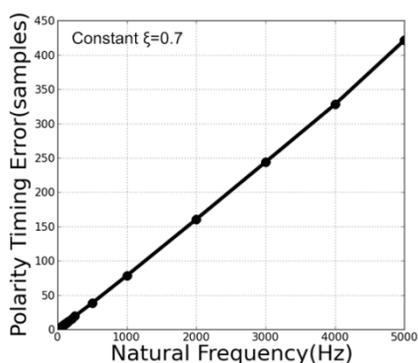


Fig. 3.11. ω_n -polarity timing error.

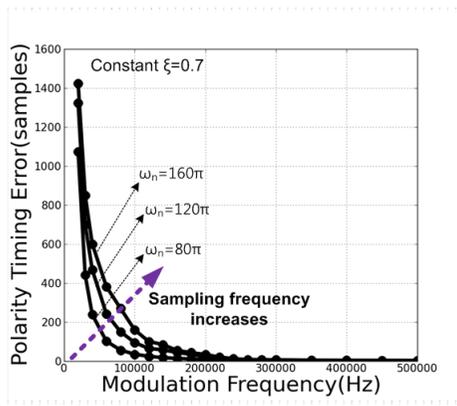


Fig. 3.12. Modulation frequency – polarity timing error.

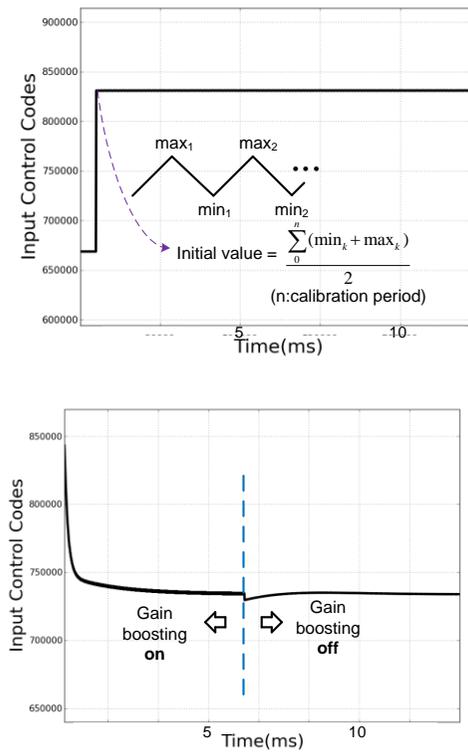


Fig. 3.13. (a) Initialization module and (b) gain-boasting.

Table I
Design constraints

At constant ζ and minimized loop latency,

Locking-time driven :	Sampling frequency \uparrow Modulation frequency \downarrow
Timing-error driven :	Sampling frequency \downarrow Modulation frequency \uparrow

Table. 3.1. Trade-off between Loop Parameters of SSC Tracking Aid.

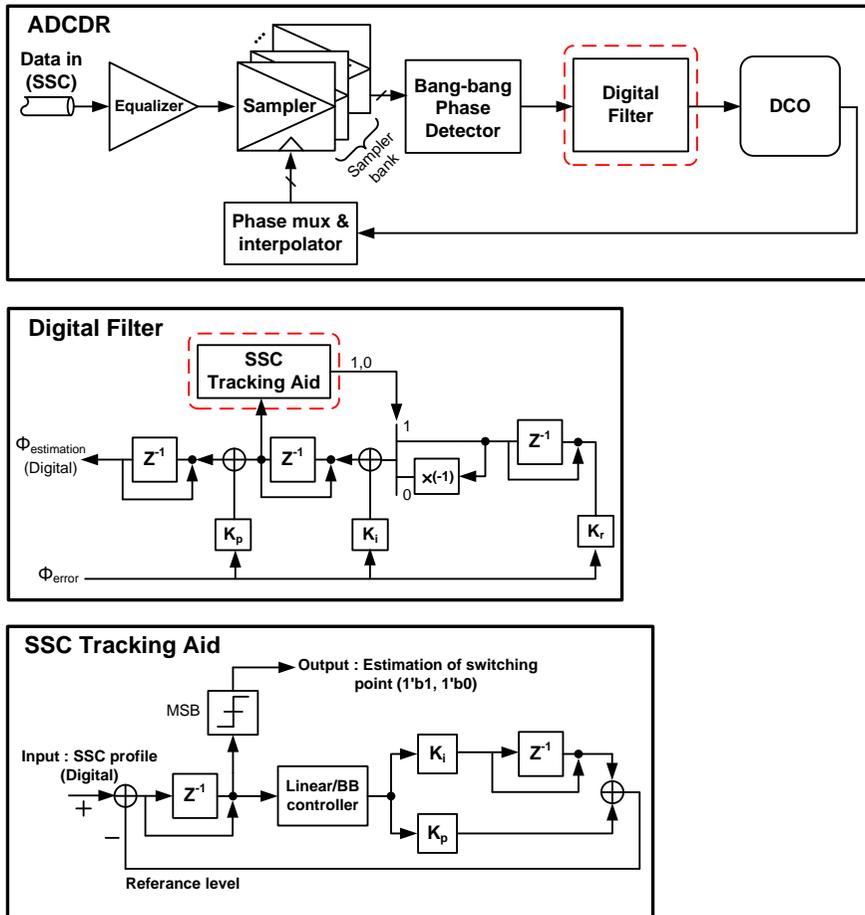


Fig. 3.14. Block diagram of the 3rd-order CDR with the proposed SSC tracking aid.

3.3.4 Overall CDR architecture

Fig. 3.14 illustrates the block diagram of our third-order bang-bang CDR. When the SSC modulated data-stream comes from transmitter, High-speed samplers quantize the output of the linear equalizer at clock edges to generate the digital signal. The phase detection logic runs at a frequency corresponding to one half rate of the symbol rate, considering the gate speed in our 65nm CMOS technology. And the output of the bang-bang phase detector controls the timing of the DCO through two paths: the proportional and the integral path. The digital filter operates in 187.6-MHz that is fully synthesized include both of SSC tracking loop and third order path. In Fig. 3.14, the SSCG tracking aid (marked in a dotted box) generates the polarity information of the frequency slope and estimates the mean value of the frequency via feedback. The rest of loop filter accumulates phase error with the corresponding gains (p-gain, i-gain, r-gain). The modulation estimation requires accumulator on integral path to first track the information of frequency of the transmitter. Moreover, after the modulation estimation is completed, the frequency ramp rate can be estimated by the ramp accumulator and ramp accumulators saturate certain value according to the slope of frequency modulation. Because absolute value of slope of SSCG profile is always same, the third-order term of digital filter needs only one accumulator locked at absolute value slope of SSCG profile. And the output of SSCG tracking loop plays a role mux-selection signal that changes the polarity of saturated value of third order accumulator.

For stability the loop, the proportional gain must be sufficiently larger than the integral gain. This is equivalent to having large enough damping ratios in linear PLLs. However, an integral gain that is too low may slow down the frequency tracking. So, to meet stability and frequency tracking, we have to increase both proportional gain and integration gain in 2nd order CDR. But there is the tradeoff between wanting a lower bandwidth to filter jitter more and the need for a larger bandwidth to minimize error in tracking the phase offset trajectory.

Fig. 3.15 shows the jitter transfer curve of (a) 2nd order (b) 3rd order in same proportional and integral gain. Bandwidth of each loop is same in spite of adding the 3rd order term with very lower gain compared to 2nd order term. The ability of jitter cancelation is 3rd order CDR is better in same proportional, integral gain and there are the comparison result in Section 3.4.

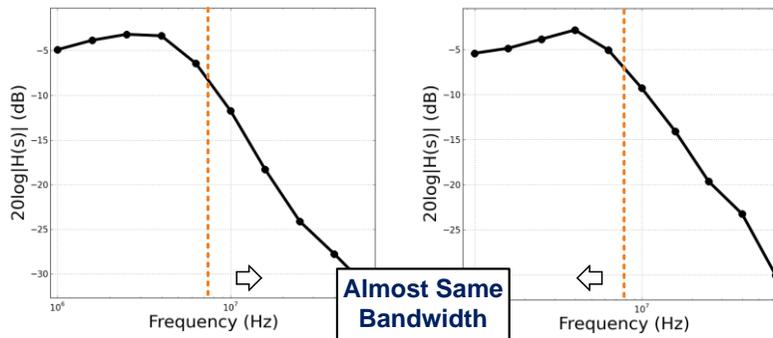


Fig. 3.15. The comparison of bandwidth (a) 2nd order (b) 3rd order.

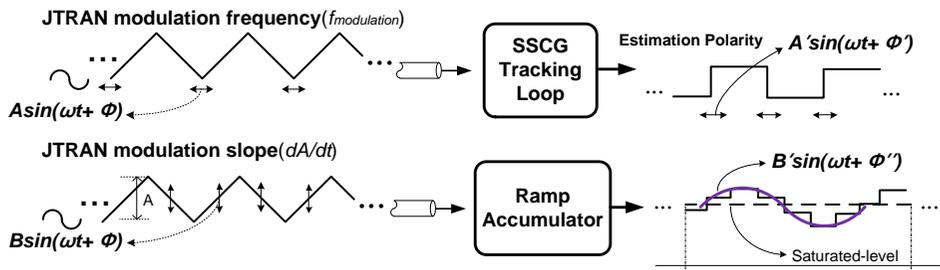


Fig. 3.16. Jitter transfer of SSCG tracking aid (a) modulation frequency (b) slope.

In Fig. 3.16, there are two methods to derive two kinds of jitter transfer curves (one is modulation tracking and the other is slope tracking) of SSCG tracking loop. From this property, we can find real performance of SSC tracking loop that track SSC modulation data. When analyzing jitter transfer, we add the sinusoidal small signal to SSC input data stream. One dithers the period of SSC modulation and the other dithers the slope of SSC modulation.

It is desired to minimize the bandwidth of the SSC tracking loop (frequency-modulation tracking loop) and ramp accumulator (frequency-slope tracking loop) in order to reduce the amount of jitter of SSCG profile caused by transmitter. As we mentioned, our part of estimation modulation period of SSC is reference tracking loop and the part that locked at certain saturated-level that means the derivative of SSC modulation in time-domain is third order ramp accumulator.

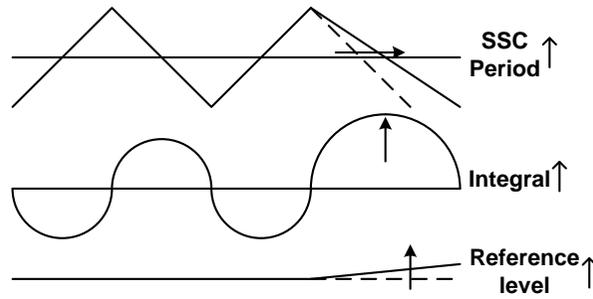


Fig. 3.17. Relationship of reference level and bandwidth.

As we see in Fig. 3.16(a), the transfer function in case of modulation frequency is second order low-pass response. It has 3-db bandwidth at around 2-kHz. In this case, this plot is related in original parameter of reference tracking loop. The ω_n is about 1-kHz and it satisfies the condition $\omega_{3db} \approx 2\xi\omega_n$.

The reason why bandwidth of reference tracking loop coincide with that of Fig. 3.16(a) is revealed in Fig. 3.17. Illustrated in Fig. 3.17, if the modulation period gets longer (that is regarded as jitter insertion), integral value increases, which results in reference level increases. In other words, the cancellation ability of jitter ingredient is related to reference tracking loop dynamic corresponding to ω_n . Fig. 3.16(b) shows jitter transfer of frequency-slope tracking loop that is first order system. It has 3-dB bandwidth at 9-kHz. It coincide with fitting plot $1/(1+s\gamma)$. Where $\gamma (=2^{-17})$ is the gain of third order path of digital filter in continuous time domain. Likewise, mentioned in section 3.1, the tracking ability of the slope of frequency is related to third order ramp accumulator.

Consequently, SSC tracking loop performance can be seen in two respects like above analysis. The principle of jitter cancellation of SSC tracking loop can be summarized the bandwidth of reference tracking and third-order gain are substantial parameters.

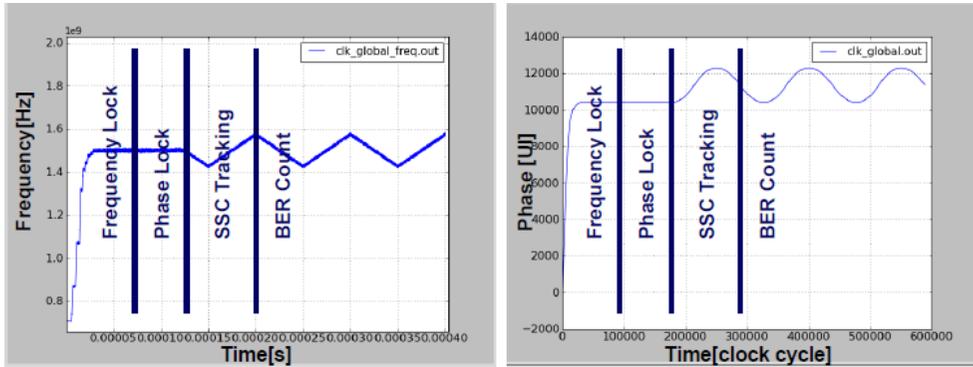


Fig. 3.18. Frequency acquisition and phase trajectories during the initial calibration.

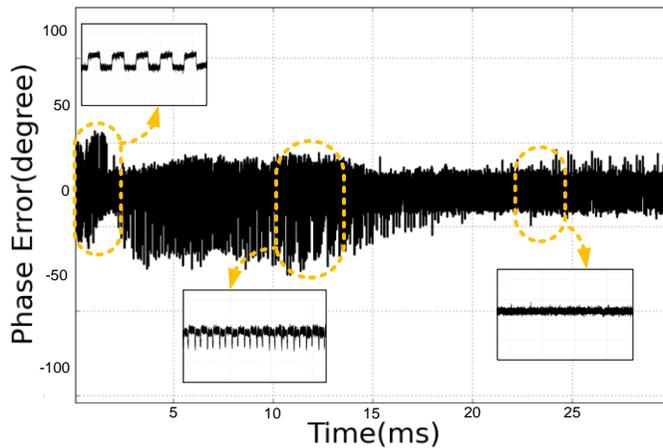


Fig. 3.19. CDR transient with VHDL simulation.

3.4 Simulation Results

Fig. 3.18 shows the frequency acquisition and phase trajectories during the initial calibration sequence. The recovered clock frequency is modulated with 1.5-GHz center frequency and Fig. 3.19 is the transient simulation with phase error between input data and recovered clock after calibration sequence in Fig. 3.18.

In Fig. 3.19 transient phase error simulation, at first, the SSCG tracking loop is off and CDR tracks SSC data stream with second-order loop filter. Because second order system cannot track ingredient of frequency ramp rate, the phase error can be seen as distribution of two steps each SSC period. After 3rd order loop with SSC tracking loop turns on, initially, the reverse estimation can occurs until SSC tracking loop enter steady-state. Due to the reverse estimation we called polarity-timing error earlier section, CDR may exhibit overshoots in each point of SSC polarity changing referred in Fig. 3.3(a). Finally, when the SSC tracking loop is locked and polarity timing error diminished in optimal comprise, the phase error is reduced by half of second order.

Fig. 3.20 illustrates the efficacy of the described SSC tracking loop with jitter histogram. Without the tracking aid, a second-order PLL-based CDR has a simulated jitter of $0.3 \cdot UI_{pp}$ when tracking a 6-Gbps random data stream with SSC modulation width of 40000-ppm. The jitter is dominated by the change in the static phase offset when the polarity of the frequency slope changes. In comparison, a third-order PLL-based CDR with the SSC tracking

aid achieves the jitter of $0.1 \cdot UI_{pp}$ for the same loop parameter, same bandwidth of 7.6-MHz. this corresponds to the 60% reduction in the peak-to-peak jitter level.

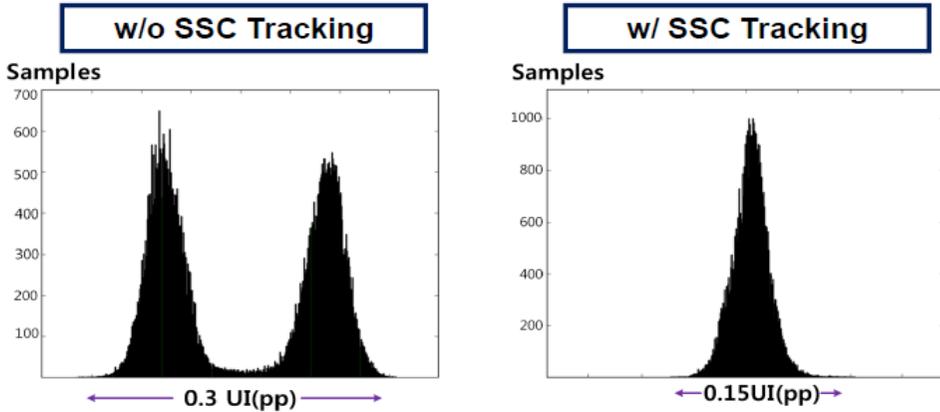


Fig. 3.20. Jitter suppression due to SSC tracking.

Table II
CDR Characteristic Summary

Process technology	0.65 μ m CMOS LVT process
Supply	1.1V nominal
The Area of digital loop filter for the 3rd order CDR	7370 μ m ²
Power dissipation of digital loop filter	1.25mW
Data rate	6Gb/s
Loop bandwidth	\approx 7.6MHz
SSC Modulation frequency range	30~100kHz
SSC Modulation rate	12000ppm (@100kHz) ~ 40000ppm (@30kHz)
Jitter _{peak-peak}	
w/ proposed SSC tracking loop	86.66ps,pp (@ 30kHz, 40000ppm)
w/o proposed SSC tracking loop	198ps,pp (@ 30kHz, 40000ppm)

Table. 3.2. Performance Summary of the SSC Tracking CDR.

Chapter 4

Conclusion

In this thesis, all of the introduced implementations including peaking-free transfer, TDC gain linearization technique and tracking aid for SSC-type data are realized by digital-domain circuits such as digital filter or digital controller. With these advanced digital controlled technique, we can finally achieve fast-settling, constant loop characteristic and deterministic jitter suppression.

First, digital PLL with a peaking-free transfer function is presented. The nested-feedback for phase-compensation is realized entirely within the digital loop filter, without adding any noise-sensitive components on the input or feedback clock paths. And the presented TDC achieves a linearized characteristic insensitive to the external jitter condition. The measurement results demonstrated the fast settling in the PLL's phase step without exhibiting an overshoot and the TDC gain invariant with the input jitter condition.

Second, a new-type SSC tracking aid based on integration to reduce noise sensitivity is proposed. The polarity of the SSC frequency ramp can be more robustly estimated based on our scheme. The estimate on the frequency slope polarity and the mean value is provided by proposed feedback loop and, through the analysis of parameters relationships, we can know that how to design with optimal parameters and mitigate the adverse trade-off such as

between bandwidth and locking time with additional tracking aids. Finally, our 3rd-order PLL-based CDR with the SSC tracking aid achieves $> 50\%$ reduction in jitter compared with the original 2nd-order CDR, which breaks the conventional trade-off between the tracking bandwidth and steady-state jitter.

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초록

본 논문은 진보된 디지털 컨트롤러를 이용한 디지털 위상동기화 루프 (PLL) 와 클럭 및 데이터 복원회로 (CDR) 의 설계를 제안한다. 기존의 아날로그 설계의 접근 방식과는 다르게, 디지털 방식의 설계는 아날로그 방식의 타이밍 회로들의 설계 제한 조건들을 완화시킬 수 있으므로, 비선형 전달함수나 빠른 안정화 속도와 같은 테크닉들의 구현을 가능하게 한다.

첫째로, 본 논문은 **peaking**이 없는 전달함수를 가진 디지털 PLL의 설계를 제안한다. 즉, 기존의 2차 PLL이 가지는 페루프의 전달함수의 영점을 제거함으로써 **peaking**이 없는 전달함수를 구현하였다. 따라서, 제안하는 PLL은 위상이 변함에 따라서 **overshoot**현상이 발생하지 않고, 빠른 안정화 속도를 가능하게 한다. 기존에 발표된 **peaking-free PLL**들과는 다르게 제안하는 디지털 PLL은 **peaking-free** 디지털 루프 필터를 이용하여, 다른 부가적인 회로 없이 **peaking**이 없는 전달함수를 구현할 수 있다. 본 논문의 PLL에 쓰여진 시간-디지털 컨버터 (TDC)는 3개의 이진 위상-주파수 디텍터 (BBPFD)를 사용해서 타이밍 오차를 과 샘플링 (**oversampling**)으로 보정하고 적절한 시간에 따라 변하는 (**time-varying**) 오프셋을 가하여 선형적인 전달함수를 구현하였다. 본 논문의 디지털 PLL은 65nm CMOS 공정으로 제작되었으며, 1.58- μ s 의 빠른 안정화 속도를 690-MHz 대역폭에

서 나타낸다. 8분주의 클럭 지터 (jitter)는 $3.477\text{-ps}_{\text{rms}}$ 를 나타내며, 10-MHz 오프셋에서의 위상 잡음은 -120 dBc/Hz 이다. 총 전력 소모는 63.9-mW 이다.

본 논문에서 소개하는 두 번째 회로는 고차의 클럭 및 데이터 복원 회로로 Spread-Spectrum Clocking (SSC) 방식으로 들어오는 데이터를 정상상태의 위상 오차 없이 복원하기 위해 설계되었다. 기존의 동일한 목적의 CDR 과는 달리, 잡음에 취약한 미분기를 사용하지 않고, 제안하는 구조는 적분기를 사용함으로써, 훨씬 더 잡음에 강하고, 정확하게 SSC정보를 복원해낸다. SSC정보의 오차는 10-사이클 이내로, 안정화 속도는 15ms이내로 데이터를 복원할 수 있고, 전체 CDR의 지터는 $0.12\text{-UI}_{\text{pp}}$ 이다.

주요어 : PLL, CDR, Digital loop filter, Digital controller, Digital PLL, Digital CDR, TDC, BBPFD, Transfer function

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