공학석사학위논문

Photo-triggered Destructible Ultra-thin Flexible Resistive Random Access Memory

빛으로 파괴 가능한 매우 얇고 휘어지는 저항메모리

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이학용

Photo-triggered Destructible Ultra-thin Flexible Resistive Random Access Memory

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Abstract

Photo-triggered Destructible Ultra-thin Flexible Resistive Random Access Memory

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Flexible memories for the Internet of things (IoT) have attracted great attention due to its wide applicability to various items such as healthcare electronic patches. However, they are prone to be hacked by unauthorized access when it is lost, although they store important personal identification data. Therefore, memory devices should be able to be physically destructed on

demand by certain triggers while having large data storage. Here, I propose a photo-triggered destructible flexible resistive memory of which fabrication process is suitable to the conventional one so that it can be fabricated on a high density transistor array. Poly ethylene oxide film containing photo acid generator molecules was coated on the resistive memory. The top electrode and the resistance switching layer of the memory are made of Mg and Mn doped ZnO (3 wt%), respectively, which dissolve under acidic conditions. This intrinsic nature of Mg and ZnO:Mn and ultrathin thickness of the ZnO:Mn layer helped complete erase of the stored data in the memory device when ultraviolet light is illuminated on it. This system enables a novel technology of IoT with information security and large data storage.

Keywords: Flexible memory, resistive memory, destructible memory, silicon nano-membrane transistor.

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1. Introduction

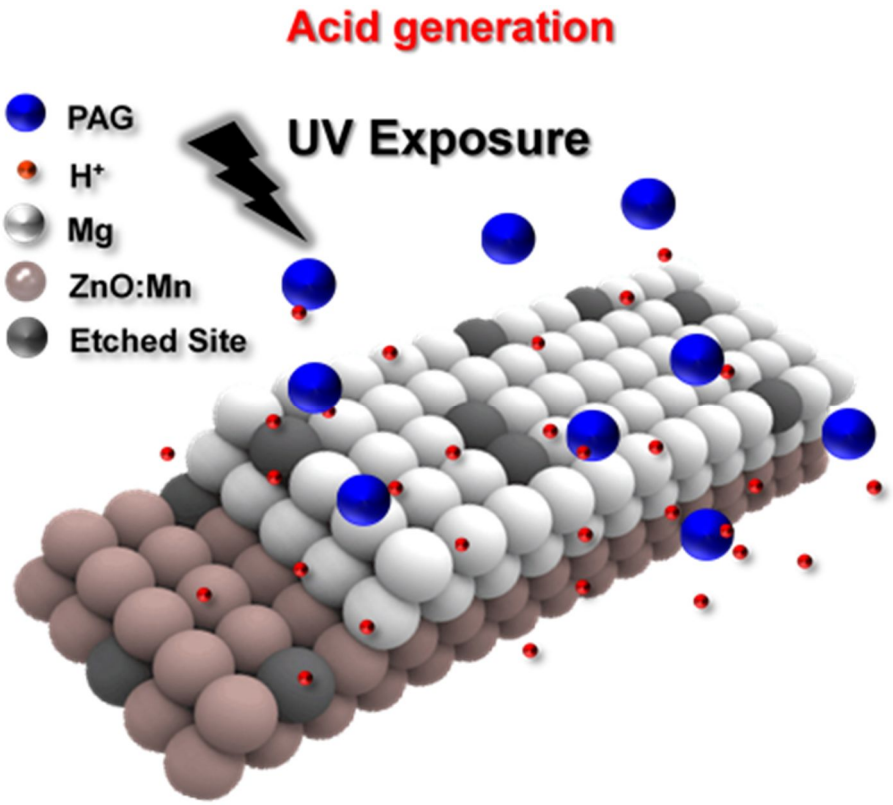
Recent development of the Internet of things (IoT) have attracted notable attention due to their potential for establishment of close network between our life and common electronic devices. The IoT devices, such as smart watches or healthcare machines, are usually composed of sensing/ processing/ memory/ network parts. However, these IoT platforms lack of the information security equipment and are too rigid to employ them for soft and flexible objects[1]. Especially, the memory units have their and their users' identification information to give the objects the Internet connectivity, but they are vulnerable to unauthorized access or hacking (simple erase of data is fully recoverable[2]). Recently, chemically destructible memory[3] and flexible memories[4-6] have reported. However, the destructible memory is water-soluble, which is not appropriate for the commercial semiconductor fabrication process and does not have a proper electronical trigger, and the flexible memories have no information security equipment. Therefore, to widen the applications of IoT technologies and make it more secure, the development of novel flexible and security-enhanced memory devices are highly demanding. This ideal memory can be physically destructed and delete

data unrecoverably when it is needed and change its shape freely.

To establish the high density self-destructible memory, material selection is extremely important because the materials should be dissolvable to certain chemical atmospheres and, therefore, can be physically destroyed by external triggers. Since high density memories can only be made with active array electronic components such as transistors or selectors[6], the materials also has to be suitable to conventional semiconductor process such as photo-lithography and etching processes. Recently, chemically destructible electronics whose destruction-triggers are heat[7] or photons[8] were reported. However, they are destroyed by collapse of their substrates which is susceptible to acids and organic solvents, and therefore, they cannot be fabricated through the conventional semiconductor process, which results in impossibility of silicon fabrication and high density memories.

In this paper, I propose a system design and fabrication of a flexible high density information secure memory. The system is composed of active silicon array on support polymer substrate, acid-dissolvable non-volatile ultra-thin resistive random access memory (ReRAM) and an acid generating layer. The memory is constructed with a Cr bottom electrode and acid-dissolvable parts; a Mn doped ZnO (ZnO:Mn) resistance switching layer (RSL) and a Mg top electrode. The memory cells were fabricated on the high-performance single crystal silicon transistor array and coated by poly (ethylene oxide)

(PEO) film containing photo acid generator (PAG) molecules which generates acids under ultraviolet (UV) exposure. When the UV is illuminated on the memory, top electrodes and RSLs are physically destroyed by the generated acids (Scheme 1), which leads an unrecoverable data erase. This memory system allows a novel IoT technology with information security as well as a large data storage.



Scheme 1. Acid-degradable Mg/ZnO:Mn layer in the ultra-thin resistive memory.

2. Ultra-thin non-volatile resistive memory

2.1. Structure and electrical characteristics of the resistive memory

The resistive memory has metal / insulator / metal (MIM) structure. The bottom and top metal electrodes are Cr and Mg respectively, and the RSL is ZnO:Mn. On the Cr bottom electrode, 5 cycles of Al_2O_3 were deposited by plasma enhanced atomic layer deposition (PEALD). The thickness of the RSL is sub 10 nm (~5 nm) (Fig. 1), and the size of the memory cell is 20 μm x 20 μm.

The representative current-voltage curve (IV curve) of the resistive memory is shown in Figure 2a. "1" is written when the top electrode is under positive voltage (positive set process) with 300 μA current compliance, and "0" is written when the top electrode is under negative voltage (negative reset process). The memory has a low operating voltage between -2 V and 1.5 V. The cumulative probability plot is presented in Figure 2b. The switching behavior of the memory is uniform over the entire array with a large memory operation window (about 2 orders different between "1" (LRS ~ 1 kΩ) and "0"

(HRS > 100 kΩ)). The retention and the endurance behavior of the resistive memory are shown in Figure 3a and 3b, respectively. The “1” (LRS) and “0” (HRS), written in a memory cell, maintained over 10^4 seconds, and the memory worked well during 100 cycles of writing “1” (LRS) and “0” (HRS).

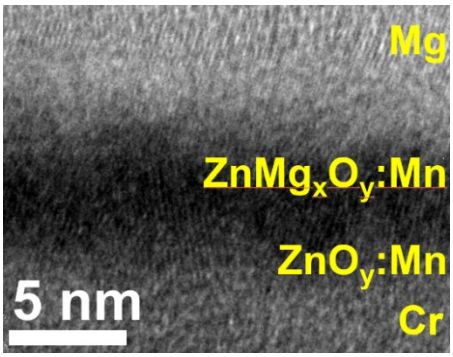


Figure 1. Tunneling electron microscope (TEM) image of the resistive memory.

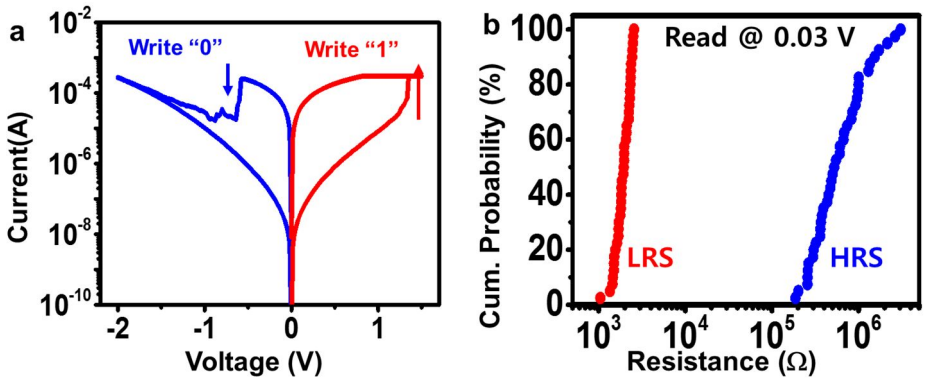


Figure 2. Switching Behavior of the resistive memory. Representative (a) current-voltage curve (IV curve) and (b) cumulative probability plot of its resistance (red for LRS and blue for HRS).

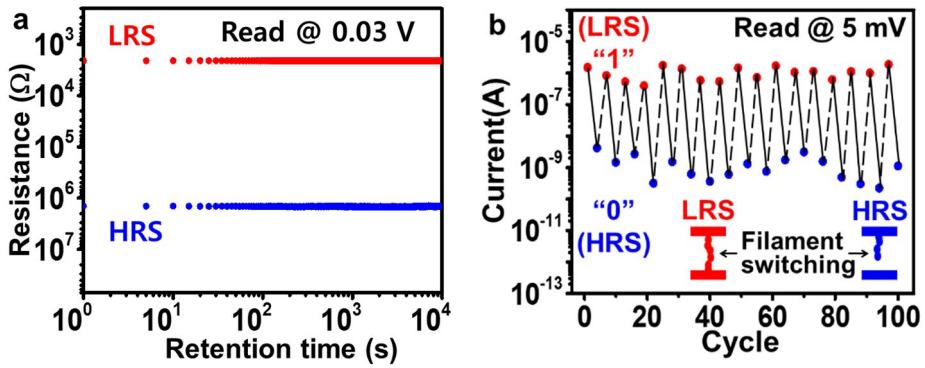


Figure 3. Reliability tests ((a) retention behavior and (b) endurance) of the resistive memory.

2.2. Resistance switching mechanism of the resistive memory

When the memory is in its LRS, the IV curve of the memory is linear (Fig. 4), and the resistance of HRS is dependent on the size of the memory (it decreases with the increasing size), while the resistance of LRS does not change with the increasing memory size (Fig. 5). These are typical signals of ohmic conducting paths across the insulating resistance switching layer.

Mn atoms in ZnO are known to increase oxygen vacancies[9], and there was no switching behavior with pure ZnO resistance switching layer (Fig. 6). Therefore, presumably, Mn dopant atoms generate lots of oxygen vacancies in the ZnO:Mn layer, and the top Mg atoms make oxygen vacancies at the interface by consuming oxygen atoms to oxidize themselves. The oxygen vacancies are positively charged and therefore can migrate from top region to bottom Cr electrode following electric field during set process (positive bias), which results in formation of conductive paths (Scheme 2). In reverse way, the negative bias repels oxygen vacancies from bottom electrode and breaks the conductive paths (reset process).

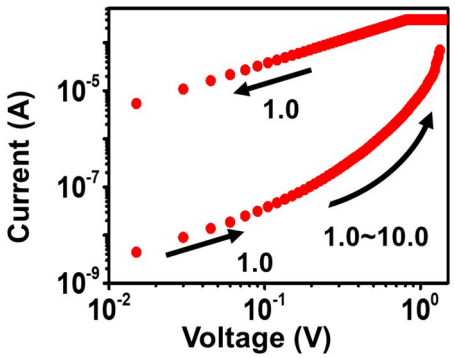


Figure 4. Log-log IV plot of set process. Current is linearly proportional to voltage when the memory is at LRS.

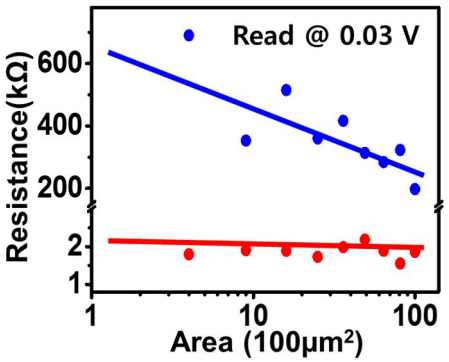
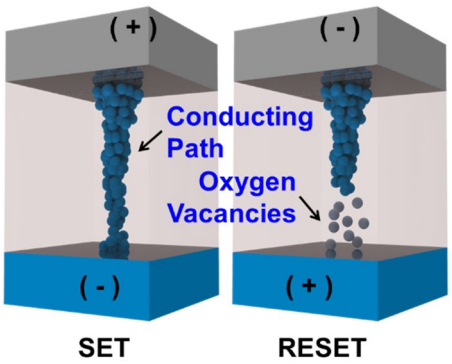


Figure 5. Size dependency of LRS (red dots) and HRS (blue dots).



Scheme 2. A conducting path forms during set process, and it breaks down during reset process by migration of oxygen vacancies.

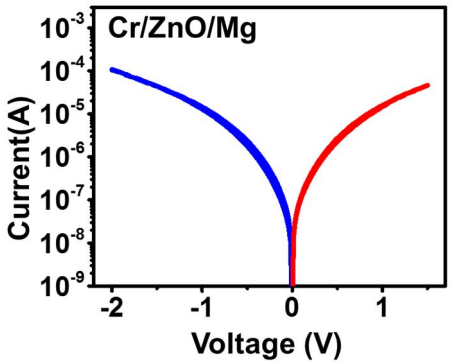


Figure 6. IV curve with pure ZnO insulating layer. There is no switching behavior.

2.3. The resistive memory in a flexible form

In order to make the memory flexible, the substrate has to be changed from SiO_2 wafer, which is rigid, to flexible polymer film. Moreover, there should be another polymer layer on the memory to locate it at a neutral mechanical plane to avoid fracture during bending it[10]. Therefore, the memory was fabricated on a poly imide (PI) film and covered by PEO layer which containing PAG molecules. Because it is too flexible and soft to handle, conventional tape was used for a flexible support. It results in a flexible device, and the memory worked suitably with various bending radius (Fig. 7).

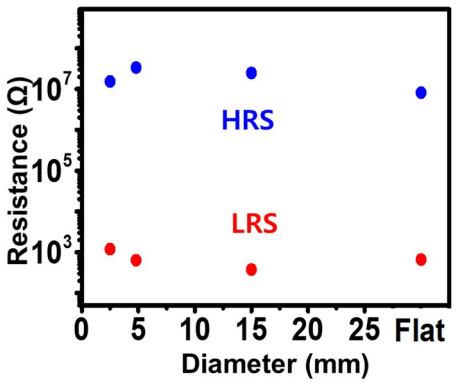


Figure 7. Resistance of LRS and HRS at various bending diameter.

3. Photo-induced destruction of the resistive memory

3.1. Acid generation in the acid generating layer

2-(4-methoxystyryl)-4,6-bis(trichloromethyl)-1,3,5-triazine (MBTT) was used for PAG in PEO (M.W. 600,000) film. The PAG molecule absorbs UV lights with maximum absorption wavelength at 379 nm (Fig. 8). The absorbance decreases as UV exposure time goes and some molecules are consumed to generate acids (Fig. 8). When the PAG molecule absorbs a UV photon, a chlorine atom is detached from the molecule and forms a chlorine radical[11] (Scheme 3). The generated chlorine radicals react with ambient hydrogens and become hydrogen chloride, which is a strong acid.

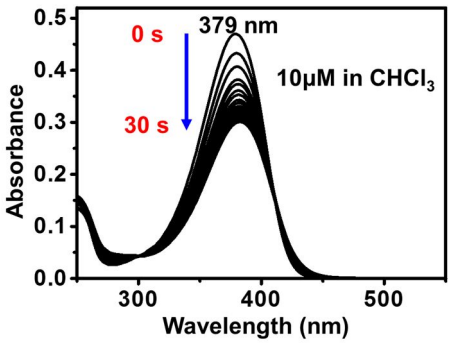
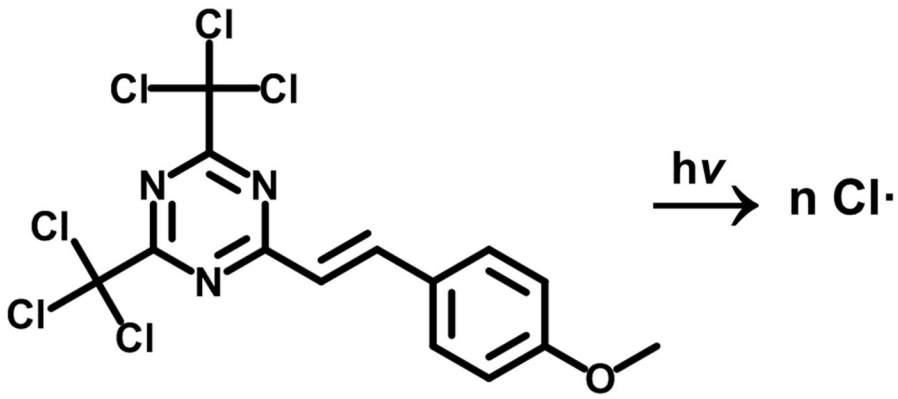


Figure 8. Absorption spectra of PAG molecules in chloroform solution with various UV exposure time.



Scheme 3. Chlorine radical generation by UV absorption of a PAG (2-(4-methoxystyryl)-4,6-bis(trichloromethyl)-1,3,5-triazine (MBTT)) molecule.

3.2. Dissolution of Mg thin film under UV illuminated acid generating layer

Due to the intrinsic nature of Mg, it dissolves under acidic conditions. When the acid generating layer on the Mg film is illuminated by UV light, the Mg atoms are dissolved by the generated acids, and roughly deposited Mg thin film is etched to be smooth (Fig. 9). Therefore, it is possible to etch a portion of the Mg film by expose UV through a certain patterned mask (Fig. 10). The mechanism of the dissolution is presumably an ionization of Mg atoms by the acids and their consequent diffusion into the acid generating layer. As shown in Figure 11, Mg atoms were detected in the acid generating layer.

To verify that Mg electrodes break down under the acid generating layer and their etching rate, I performed a resistance measurement under UV exposure (Scheme 4). The Mg electrode failed in 220 seconds with 33.3 wt% PAG concentration (Fig. 12), and more time was needed to break the Mg electrodes when PAG concentration is decreased. Figure 13, TEM images of Mg thin film under acid generating layer before and after UV illumination (8.3 mW/cm^2, 10 minutes), visually shows the etching rate of Mg thin film. The 7.5 nm of Mg layer was etched out, and remaining Mg and Cr adhesion layer were damaged by the diffused acids.

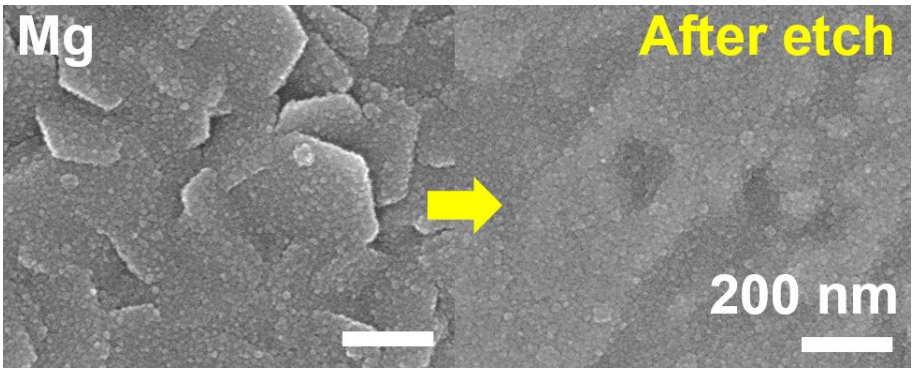


Figure 9. Scanning electron microscope (SEM) image of top view of Mg layer before and after the etching.

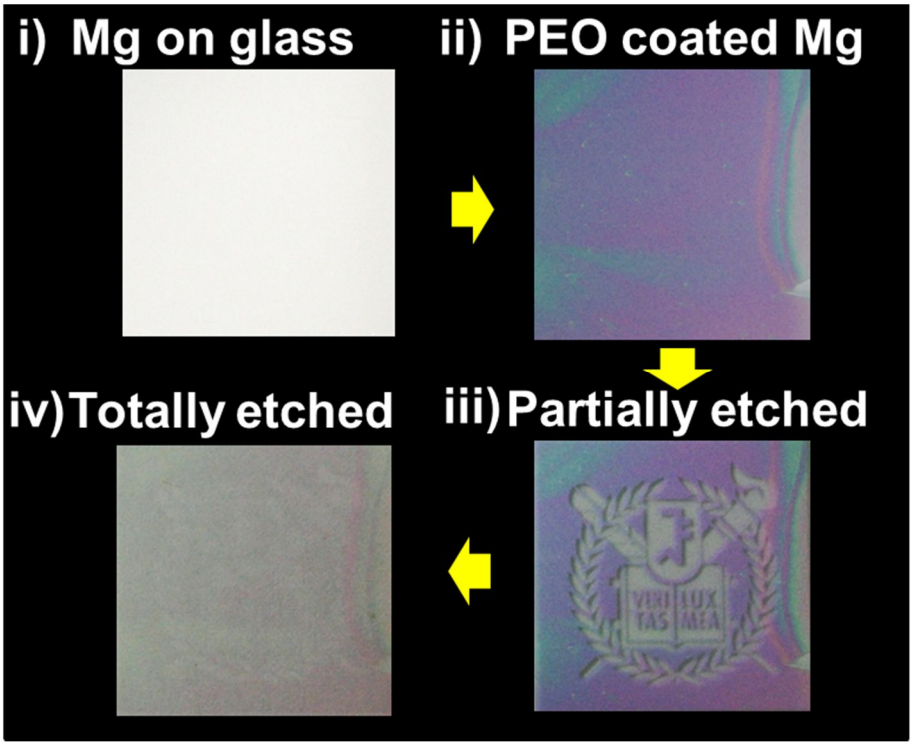


Figure 10. Etching of Mg film on a glass substrate. i) before PEO coating, ii) After coating PEO (containing PAG molecules), iii) partially etched Mg layer by UV exposure through a mask, iv) totally etched Mg layer after UV exposure all area.

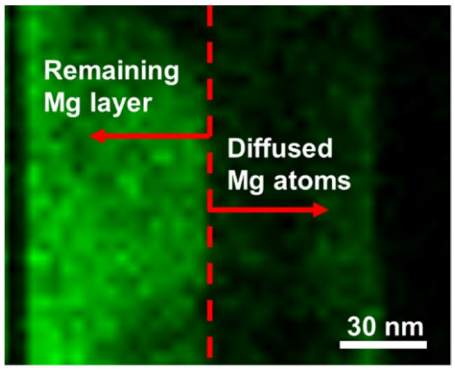
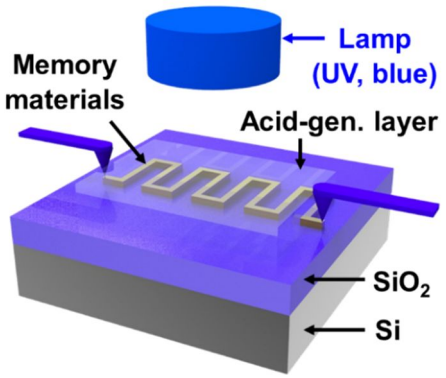


Figure 11. Energy dispersive X-ray spectroscopy (EDS) image of the etched Mg layer. Green dots express the Mg atoms.



Scheme 4. Schematic image of the time dependent resistance measurement under UV illumination.

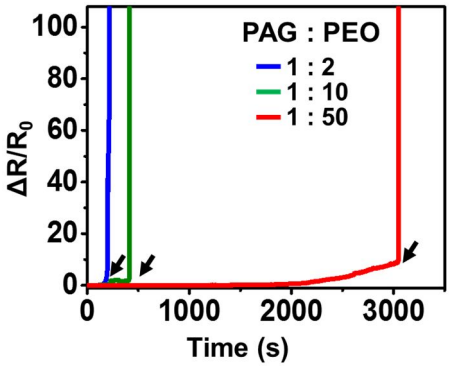


Figure 12. Results graph of the time dependent resistance measurement under UV illumination.

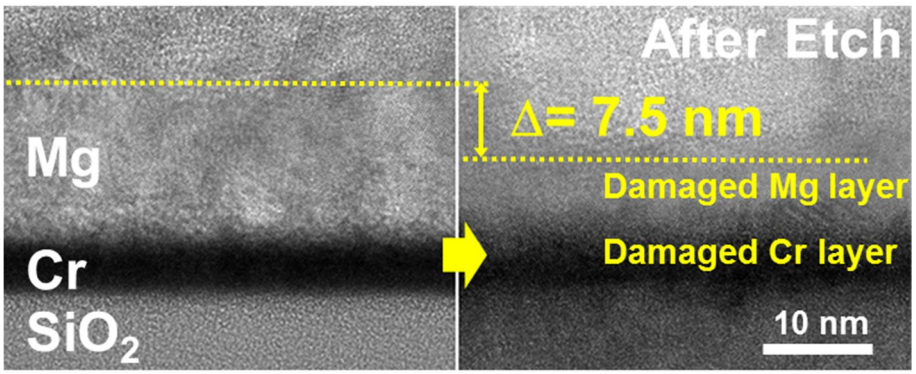


Figure 13. TEM images of Mg thin film on a Cr adhesion layer under acid generating layer before and after UV illumination (8.3 mW/cm^2, 10 minutes).

3.3. Dissolution of ZnO:Mn thin film under UV illuminated acid generating layer

ZnO:Mn layer also dissolves under acid generating layer (Fig. 14). Under 8.3 mW/cm^2 UV exposure during 10 minutes, ZnO:Mn layer etched out about 2 nm, and the remaining layer was not damaged (Fig. 15). This etching rate of ZnO thin film is much slower than that of Mg thin film, and ZnO is sturdier to the generated acids than Mg in that the remaining layer maintained intact. These difference presumably arose from the oxidation state and atomic weight of ZnO and Mg atoms. Because the ZnO is already oxidized as Zn^{2+}while Mg is neutral, Zn^{2+} ions have less tendency to react with acidic molecules than neutral Mg atoms. Moreover, because the atomic weight of Zn (~65.4) is much bigger than that of Mg (~24.4) Zn atoms are more immobile than Mg atoms so that Zn diffuses slower into the acid generating layer.

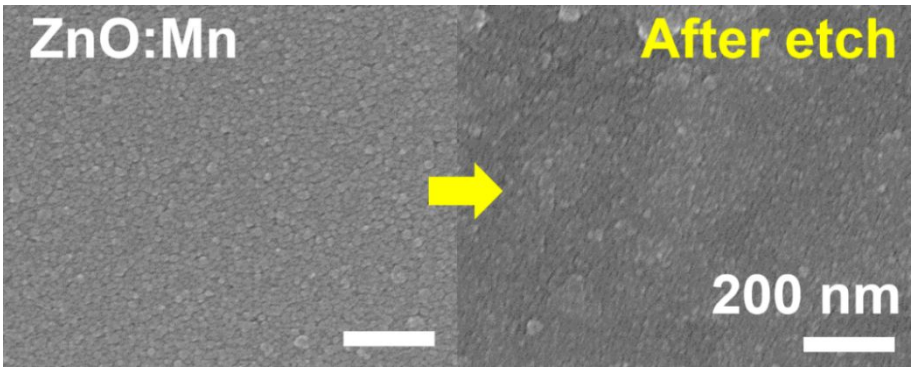


Figure 14. SEM image of top view of ZnO:Mn layer before and after the etching.

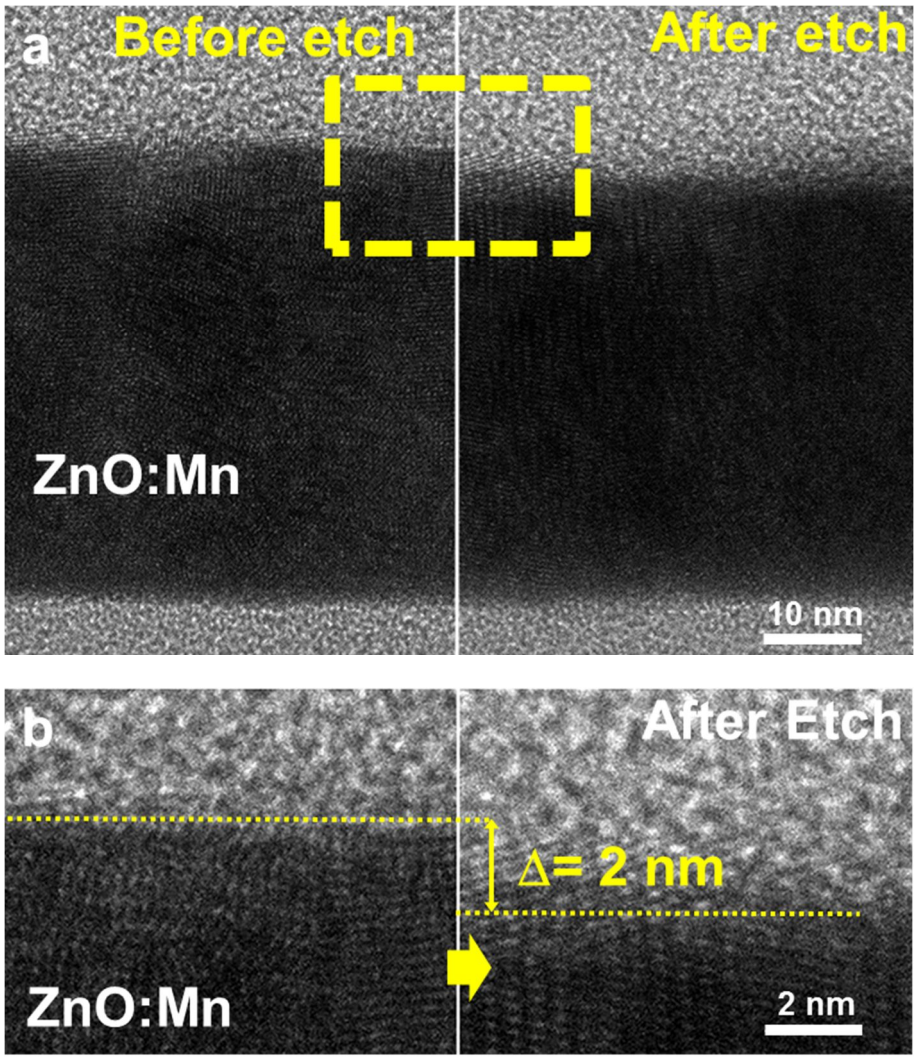


Figure 15. TEM images of ZnO:Mn thin film under acid generating layer before and after UV illumination (8.3 mW/cm^2, 10 minutes). b is magnified image of the yellow square in a.

3.4. Destruction of the resistive memory under UV illuminated acid generating layer

The PEO film, containing PAG molecules, was spin-coated on the resistive memory. Before the UV exposure, the memory on a rigid substrate worked normally while it showed no on/off switching behavior and was not able to be told “0” or “1” after the UV induced data erase (Fig. 16), which means that the memory broke down when UV is illuminated on it. Figure 17 shows how the memory is changed by the generated acids. Mg layer is etched, and the remaining Mg and ZnO:Mn layers are damaged to lose its properties. Although the ZnO:Mn layer etched slowly as mentioned before, it is too thin to be etched and damaged by little amount of acids. Therefore, the top electrode and the resistance switching layer are totally failed by the UV induced acids in acid generating layer.

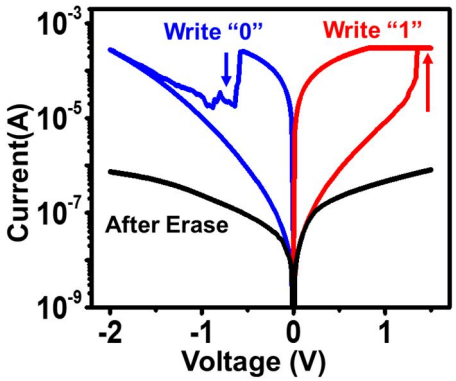


Figure 16. IV curve of the resistive memory before (blue and red lines) and after (black line) erase by the UV exposure.

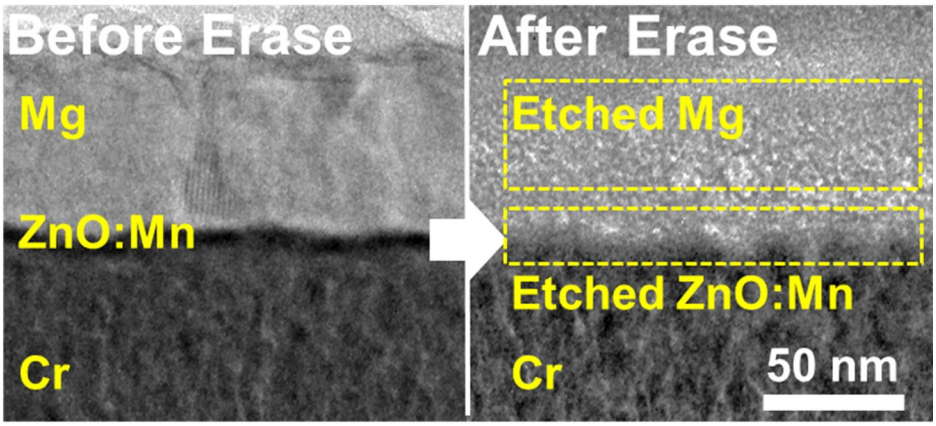


Figure 17. TEM image of cross section of the resistive memory before and after erase by UV exposure.

4. The resistive memory on single crystal silicon nano-membrane transistor array

4.1. The resistive memory on the single crystal silicon nano-membrane transistor

For the individual addressing of the memory cells, integration of each cell with active component such as transistor is essential. I employed single crystalline silicon nano-membrane transistor, which has the similar performance to commercial silicon transistors. The n-type (100) single crystal silicon transistor was fabricated on a poly imide (PI) film by transfer printing technique. Its on-current at gate voltage (V_g) 10 V and drain voltage (V_d) 0.5 V is about 4 mA which is much higher than the set and reset current of the memory (over 300 μA and less than 2 mA) (Fig. 18a). Also the transistor has low resistance of 124 Ω at V_g = 10 V around the set and reset current (Fig. 18b). These are enough electrical properties to use in an active memory array.

To read data stored in a memory on a transistor, I compared drain current versus gate voltage curve (V_gI_d curve) of LRS and. As shown in Figure 19, there seem to be no current is flowing with HRS compared to LRS,

which means they can be perfectly differentiated, and data stored in memory on a transistor array can be read without ambiguousness.

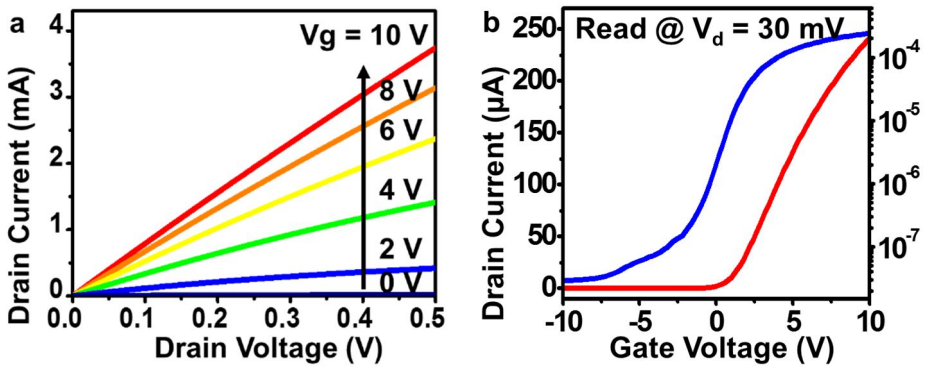


Figure 18. (a) drain voltage – drain current curve of the transistor. (b) gate voltage – drain current of the transistor (blue line represents log scale drain current).

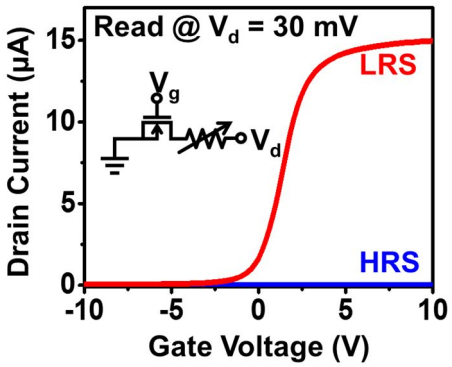


Figure 19. Gate voltage – drain current curve of the transistor which is connected with device in series. The red line is when the memory is at LRS, and the blue line is when the memory is at HRS.

4.2. Erase of data stored in the resistive memory on the transistor array

To demonstrate the full device of UV induced destructible memory, I made 141 memory cells (3 cells failed) on a 12 x 12 transistor array (Fig. 20). First, all cells were set and reset again to be at HRS, of which the resistance is higher than 100 kΩ (Fig. 21a). In sequence, the cells were set and become LRS to have resistance lower than 2 kΩ (Fig. 21b). As the third step, some cells were reset to write SNU, and the LRS and HRS can perfectly distinguished from each other as in Figure 21c. Lastly, all the memory cells were exposed to UV lights, and they lose their data (Fig. 21d). It is impossible to find SNU letters after the data erase, which means that the erased data in the memory device cannot be recovered.

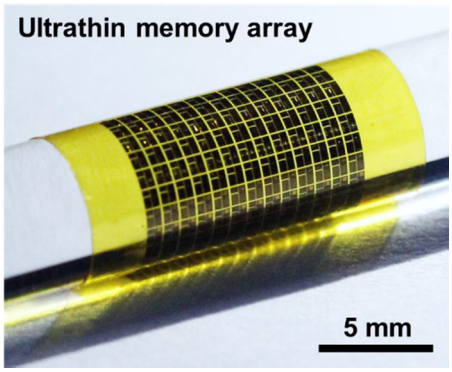


Figure 20. Memory array integrated with transistors on a PI substrate.

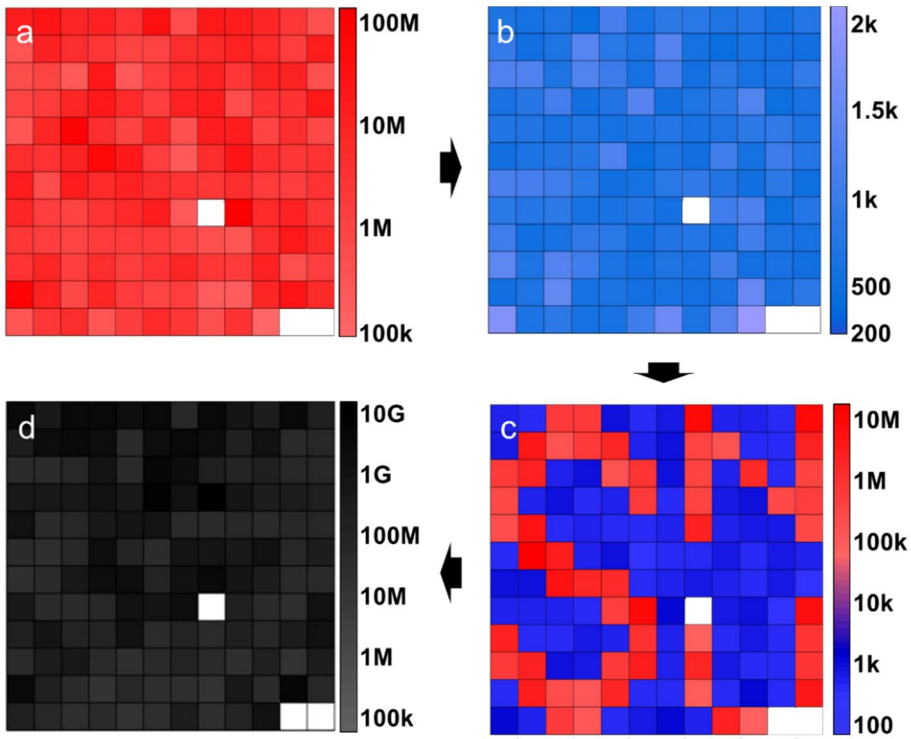


Figure 21. Resistances of the memory cells on a transistor array. (a) all cells were at HRS. (b) all cell were at LRS. (c) some cells were reset to write SNU letters. (d) UV was illuminated on the entire array to erase data. SNU letters were disappeared.

5. Experimental Section

5.1. Materials for device fabrication

340 nm (100) top silicon p-type silicon-on-insulator (SOI) from Soitec (France) was used for the transistor array, and spin-on-diffusant (SOD, P509) from Filmtronics (USA) was used for n-doping. SiO_2 wafer was purchased from 4Science (Korea) and made from LG Siltron (Korea). Thermal evaporating source of Cr (adhesion layer) and Mg were purchased from Taewon Scientific Co., Ltd (Korea). 99.99% ZnO:Mn (Mn contents: 3wt%) and Cr sputter target were from Thifine (Korea). Poly ethylene oxide (M.W. 600,000) for acid generating layer, poly imide (Poly(pyromellitic dianhydride-co-4,4′-oxydianiline), amic acid solution) and PAG (2-(4-methoxystyryl)-4,6-bis(trichloromethyl)-1,3,5-triazine (MBTT)) were purchased from Sigma Aldrich.

5.2. Fabrication of the destructible memory

Cr bottom electrode was deposited on a SiO_2 wafer substrate by DC sputtering at current of 200mA in Ar 15 mtorr for 20 minutes. The deposited

Cr was patterned using S1805 photoresist (PR) and Chromium etchant. After washing out S1805 PR with acetone, the remaining one was removed by oxygen plasma of 100 W for 20 seconds. Above the Cr layer, 5 cycles of Al_2O_3 were deposited by plasma enhanced atomic layer deposition (PEALD). For the next, Su-8 2000.5 was spin-coated and patterned with 20 μm × 20 μm square shaped hole and opening on the Cr bottom electrode for tipping the electrode. About 5 nm ZnO:Mn (Mn 3 wt%, Thifine, Korea) was deposited by AC sputtering at power of 50W in Ar 15 mTorr atmosphere. Mg top electrode was deposited about 30 nm by thermal evaporator immediately on the deposited ZnO:Mn layer and patterned using S1805 photoresist and Mg etchant.

5.3. Endurance and retention behavior test of the destructible memory

The endurance test was conducted by repetitive DC voltage sweeping from -2 V to 1.5 V and current compliance of 300 μA for programming LRS. Both resistances of HRS and LRS were measured at the read voltage of 30 mV and showed stable operation (fig. S5 e). For retention measurements, HRS and LRS was programmed by DC voltage sweeping (from 0 V to 1.5 V for LRS and from 0 V to -2 V for HRS) and read at 30 mV

for every 5 seconds.

5.4. Fabrication of flexible memory

PI film was spin-coated on the SiO_2 wafer substrate at 4000 rpm for 60 seconds. It was full cured over 1 hour on a 250 ^{0}C hotplate. Then, 70nm SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) to protect PI film from O_2 plasma for wash out residual photoresist. On the SiO_2 layer, I followed the same process as the previously explained memory fabrication.

5.5. Fabrication of the single crystal silicon nano-membrane transistor

SOI wafer was cut in a proper size and cleaned by a piranha solution (H_2O_2 1 : H_2SO_4 3) for 10 minutes. In sequence, 350 nm SiO_2 was deposited by PECVD on the cleaned SOI pieces as doping mask. Then the SiO_2 layer was patterned by reactive ion etching (RIE, O_2 6 sccm, CF_4 60 sccm, 0.055 torr, 150W) and consequent wet etching 6:1 diluted buffered oxide etchant (BOE) with AZ5214 PR (S1805 is too thin so that it wear out during reative ion etching of SiO_2). For the next, the SOI pieces with SiO_2 doping mask is cleaned by a piranha solution and then spin-coated with P509 SOD. For the

pre-diffusion, I put the SOI pieces on a 200 ^{0}C hotplate for 15 minutes, and for doping, put them in a 975 ^{0}C furnace for 1 minutes and 30 seconds. After the doping, the doping mask was removed by dipping the SOI piece into HF (2 minutes) – piranha solution (2 minutes) – HF (2minutes) in sequence. Then the SOI was hole-patterned, and buried oxide was undercut by HF solution. The undercut silicon nano-membrane was transferred to PI substrate, and the PI was full cured on a 250 ^{0}C hotplate over 1 hour. The transferred silicon nano-membrane was partially etched out to isolate transistors from each other. The gate dielectric 60 nm SiO_2 was deposited with PECVD and then opened on the source and drain. Finally, metal (Au or Cr) was deposited and patterned to be the source and drain electrode and the gate for the transistor.

5.6. Experimental equipments

The focused ion beam (FIB) SMI3050SE was used to make TEM sample. The TEM images and EDS data were obtained by Tecnai F20 which has a built-in EDS of EDAX company. Electrical properties of the resistive memory and the transistor were measured with B1500A (Agilent, USA).

6. Conclusion

In summary, with acid-dissolvable materials; ZnO:Mn and Mg, the destructible memory for information security was successfully developed. The resistive memory under the acid generating layer (PEO thin film containing PAG) has reasonable properties as a data storage device, even in a flexible form, while it perfectly loses its function after the UV exposure. It was revealed that when the acids were generated in the acid generating layer, Mg was etched out and diffused into the acid generating layer, and the ZnO:Mn was damaged by the acids. Also, the transistors were integrated to the resistive memory array. The transistor showed enough properties to set and reset the memory and read data without any ambiguousness. The memory cells on the transistor array had uniform set and reset property and lost its data unrecoverably. Therefore, this destructible resistive memory enables information security with large data storage for a novel IoT technology.

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요약 (국문 초록)

빛으로 파괴 가능한 매우 얇고 휘어지는 저항메모리

사물인터넷 (IoT, Internet of Things)을 위한 휘어지는 메모리는 의료용 전자패치와 같이 부드러운 사물에도 적용할 수 있어서 높은 적용 가능성으로 많은 주목을 받고 있다. 하지만, 이 메모리는 중요한 개인정보를 많이 가지고 있음에도 불구하고 허가 받지 않은 접속으로부터 보호받지 못한다는 문제점을 가지고 있다. 따라서 특정 자극을 받으면 물리적으로 완전히 부서져 기능을 상실하도록 하는 기술이 필요하다. 이 논문에서는 기존 반도체 공정으로 만들 수 있어 높은 밀도의 트렌지스터 행렬 위에 올라갈 수 있으면서도 빛에 의해 부서질 수 있는 저항메모리를 개발하였다. 산에 의해 부식되는 마그네슘과 산화아연을 이용하여 저항메모리를 만들고 그 위에 PAG (photo acid generator) 분자를 포함한 고분자 필름을 코팅하였다. 이러한 구조를 통해 메모리에 자외선을 쪼였을 때 PAG에 의해 산이 생성되고 이에 의해 메모리가 파괴되는 특징을 갖도록 하였다. 이 시스템은 완전한 정보보안 기능과 높은 용량을 가진 새로운 사물인터넷 기술을 가능하게 해 줄 것이라 기대된다.

주요어: 휘어지는 메모리, 저항 메모리, 부서지는 메모리, 실리콘 나노 박막 트랜지스터

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