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Fast and Reproducible pH Detection with Nanowire Field Effect Transistors

나노와이어 트랜지스터를 이용한 빠르고 재현성있는 pH 측정

BY

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February 2014

DEPARTMENT OF INTERDICIPLINARY
IN NANOSCIENCE AND TECHNOLOGY
COLLEGE OF NATURAL SCIENCE
SEOUL NATIONAL UNIVERSITY

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지도교수 박 병 국

이 논문을 공학박사 학위논문으로 제출함

2014 년 2 월

서울대학교 대학원

나노과학기술 협동과정

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ABSTRACT

As the fabrication technology of nano-size material has continued to develop, various biomedical devices, especially detection devices, have been widely researched since the size of biological entities, such as DNA, proteins, and virus, are similar to them. Chemical sensors with fluorescent labeling and parallel optical detection techniques are widely used. However, they have a number of drawbacks such as expensive and time-consuming processing for sample preparation and data analysis. To solve the problem, FET sensors have been developed as promising devices, which have benefits of free-labeling and real-time detection.

Owing to its scalability and its low power requirement, complementary metal-oxide-semiconductor (CMOS) processes are dominant in modern integrated circuit manufacturing. The use of the SiNW FET sensor should enable the co-integration of CMOS for high performance sensor system. SiNW FET sensors integrated with CMOS have been demonstrated in our and other researches.

However, it is still debatable whether the sensors operate stably in repeated measurements owing to its drift characteristics. Since the drain current increases slowly during DC measurement, it is almost impossible to read precise current value in fast measurement. It takes at least 15 minutes for the drain current to settle down at a constant value. If we would like to make a fast measurement requiring less than 100 s, the drift

effect should be removed or the drain current should be saturated under 50 s. To solve the problem, the drift effect is analyzed as building the schematic model using resistors and capacitors. That means that the drift effect is explained by exponential function with a long and short time constant from the model. As a result, the new operation scheme employing 2-step bias voltage is proposed to reduce necessary time for compensation. The method removes drift effect very fast under 50 s by compensating the exponential function with a long time constant.

Keywords: 2-step bias method, drift effect, silicon nanowire FET sensor, pH detection, electrical circuit model, repeated measurement.

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CONTENTS

Chapter 1

Introduction

1.1 Background

As the fabrication technology of nano-size material has continued to develop, various biomedical devices, especially detection devices, have been widely researched since the size of biological entities, such as DNA, proteins, and virus are similar to them[1,2]. The main reason is that the comparable size with biological entities, such as DNA, protein, nuclieic acid, etc., makes it possible to react with them easily. In addition, the scalable materials show improved performance as they possess unique physical and chemical properties arising from their small size (for example, high surface-to-volume ratio (S/V), which means that a large fraction of atoms are located near surface) [3.4]. Since only the atoms at surface interact with targets for sensing, the high S/V ratio increase the surface reaction rate, resulting in high sensitivity. The properties of the interface has effects on physical, chemical and electonic properties, and nanomaterials can be superior substrates for molecular sensing applications. Sensor architectures composed of nanomaterials have been diversified during last decades[3-18].The nanomaterials using sensor include cantilevers, quantum dots, nanotubes, nanobelts

nanogaps and nanowires (NW). Among them, chemical sensors unsing quantum dot are widely used owing to its high sensitivity and fast response[19]. However, the chemical sensors require fluorescent labeling and parallel optical detection techniques. Consequently, they cause a number of drawbacks such as expensive and time-consuming processing for sample preparation and data analysis.

These reasons demand that the sensors operating like FETs have attracted much attention. The FETs provide the electrical output signal from directly translating the analyte-surface interaction without integration with optical components. In other words, the interaction between FETs and target modelcules acting as another input source provide the output property of electrical change such as current, voltage, conductance, etc. Sensors based on FETs is expected to achieve label-free and fast measurement. Especially, it is believed that silicon nanowire field effect transistor (FET) sensors are promising devices owing to its electrically controllable propertires and compatible fabrication[20-23].

1.2 Silicon Nanowire FET Sensor

A silicon nanowire FET has the structure of a common three-electrode transistor. Silicon nanowire channel is located between source and drain electrodes and the gate electrode is stacked on the channel to modulate channel potentials. The dependence of the conductance on the gate voltage makes FETs promising cadidates for electrically based

sensor. Since the binding molecules or charged species on gate dielectric also modulate the conductance, it is analogous to applying a voltage on the gate electrode. For the reason, the surface treatment of FET sensors is one of the most important factors directly related to their sensing ability. Since its structure is the same as MOSFET, the surface of the silicon material has been intensively researched and offer a well-understood surface chemistry for sensor applications.

In addition, the silicon devices dominate the industry of the microelectronics chips and integraion with the system of the fabricated sensor is also inevitable to modify the electrical signal which interprets chemical reactions. Therefore, the reduction of the integration complexity is imfortant to fabricate FET sensor. In addition, the scale-down improves the properties of the sensors and MOSFETs. Silicon nanowire (SiNW) FET has been originally researched to overcome the short channel effect in complementary metal-oxide-semiconductor (CMOS) technology [24, 25]. When used as a sensor, SiNW FET also has advantages of high sensitivity due to its high surface-to-volume ratio. The mature production techneology gives the solutions for reproducibility such as good uniformity, and controllable alignment [26-31].

1.3 Surface Properties for a pH Sensor

Silicon nanowire FET sensor has been demonstrated in 2001 to detecthydrogen ion concentration or pH level. The key idea is surface tratment to modify the oxide surface

with 3-aminopropyltriethoxysilane. The created amino groups are located at gate dielectric surface with naturally occuring silanol (Si-OH) groups of the oxide. Both groups act as receptors for hydrogen ion or detecting pH level through protonation and deprotonation reactions as illustated in Fig. 1.1 [27,32]. This interaction results in the change of the channel potential. The SiNW FET sensor with 3-APTES exhibit stepwise increse in conductance as the various pH solution which is delivered by a micro-fluidic channel. The amino and siliano groups result in nearly linear increase in conductance with pH with complementary interaction in different pH solution. These studies suggest that the surface receptors react only with hydrogen ions in solutions including other ions.

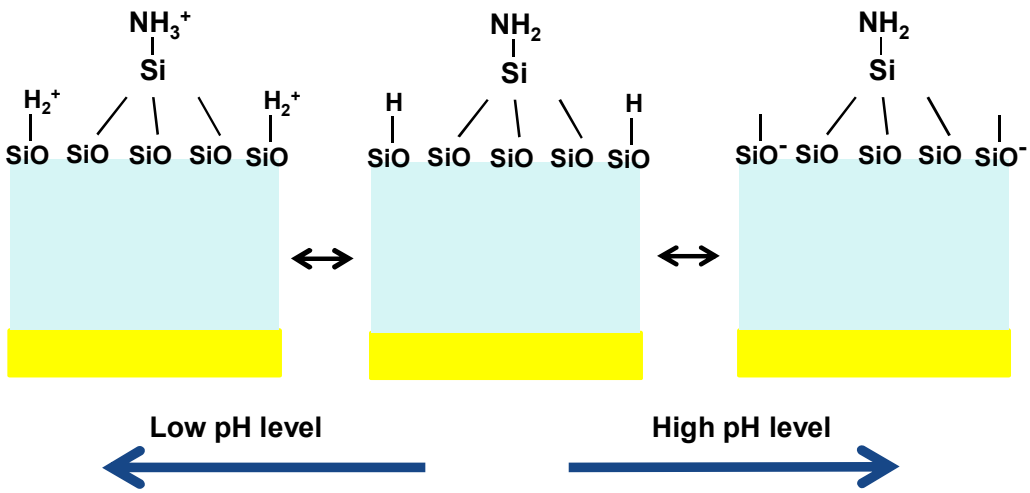


Fig. 1.1 Schematic diagrams of the surface reations of the oxide with 3-APTES. Low pH level, high hydrogen ion concentrations, lead to hydration of silano and amino group. At high pH level, the deprotonation occurs.

1.4 Requirements for Device Fabrication

As mentioned above, silicon nanowire FET sensors have been investigated intensively due to high sensitivity based on high surface-to-volume ratio and compaitible fabrication. Compared with bottom-up methods, top-down methods usually produce uniformly distributed well-aligned NWs in high yields, in a predetermined orientation and position on the substrate, making them easy to integrate into functional devices. In addition, many researchers have demonstrated the CMOS-compatible sensors by using top-down processed NWs. Considering integraion with MOSFET, the equipments and conditions for the sensor fabrication have to be the same as those of the conventional MOSFET. For this reason, we designed one of the simplest methods using conventional 0.25 μm process technology and e-beam lithography for nanowire formation. Fig. 1.2 illustrates the structure of the proposed SiNW FET sensor.

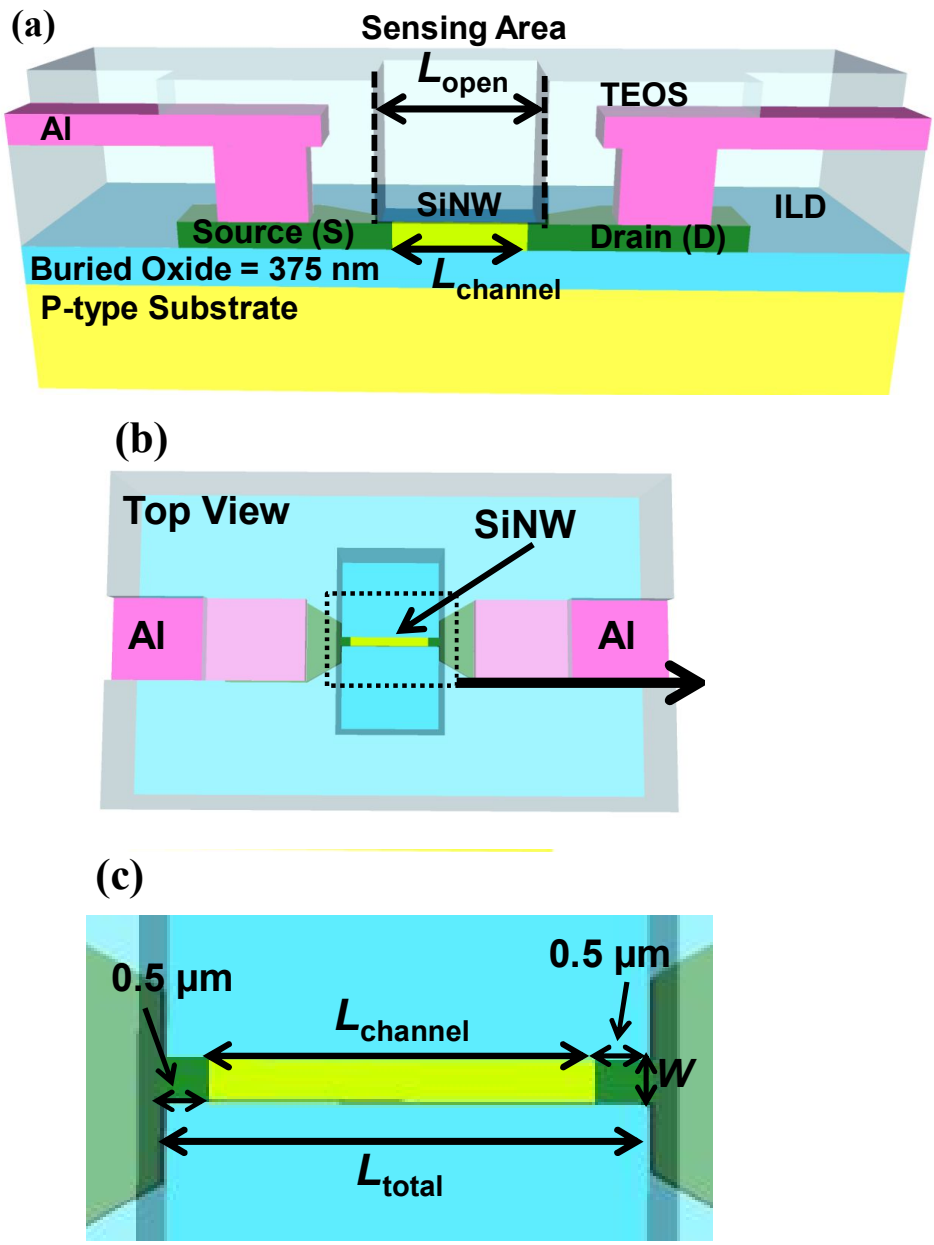


Fig. 1.2 (a) Schematic diagram of the cross-sectional view, (b) top view of the proposed SiNW FET sensor, and (c) close-up of the channel area (dotted box in (b))

Chapter 2

Sensor Fabrication and Measurement

2.1 Process Flow

Various fabrication methods of SiNW FET sensors have been demonstrated. However, simple and low cost fabrication process of that with CMOS integration has not been demonstrated until recently [26-29]. The process flow of the SiNW FET sensors which we fabricated is almost the same as that of MOSFETs. For this reason, except for the opening of sensing area, all the other process steps were conducted simultaneously.

The process flow is illustarated in Fig. 2.1. To build silicon nano-wire channels efficiently, devices are fabricated on $4x10^{15}$ cm^{-3} boron doped (100) SOI wafers prepared by the separation-by-implanted-oxygen (SIMOX) technique. The top 100-nm-thick Si layer is separated from the Si substrate by 350-nm-thick buried oxide (BOX). The first process step is channel implantation. To form a buffer oxide layer as a protection for implantation, the thickness of the top Si layer is thinned to 90 nm via thermal oxidation, and the 20-nm-thick SiO_2 is deposited, and implantation is conducted for channel doping, p-region (dopant: B^+, energy: 20 keV, dose: 5E13) and n-region (P^+ 40 keV 3E13). Although SiNW FET sensor and MOSFET operates in depletion mode and inversion

mode, respectively, p-channel SiNW FET sensor and n-channel MOSFET can be fabricated in the p-region simultaneously. Therefore, the channel implantation is perfectly compatible. After, stripping buffer oxide in HF solution, the annealing process is conducted at 950℃ for 30 minutes for uniform channel doping of 80-nm thick silicon channel.

The active region is defined by mix-and-match process of e-beam and conventional photolithography on the top silicon layer. The 90-nm-thick silicon layer is anisotropically etched in HBr/O_2 inductively coupled plasma (ICP) by using HSQ and PR resist as a mask. The range of nanowire widths written by e-beam lithography is from 25 nm to 300 nm. Fig. 2.2 shows the results of the mix-and-match process. Fig. 2.2(a) indicates the test pattern by e-beam process. The possible minimum size of active pattern is 25 nm. The active formation by mix-and-match process is shown in Fig. 2.2(b).

The nanowire size is reduced by growing 13 nm and 10-nm thick gate oxide layer on the device region at 850 °C using a dry oxidation in sequence. To protect boron penetraion, nitrited oxide is essential. Since ISRC does not provide the process, additional 10-nm-thick oxide is deposited at 780 °C and 100-nm-thick poly-silicon is also deposited at 630 °C via low pressure CVD system (LPCVD). In addtion, the gate oxide is used to protect silicon channel from silicon etch when building gate of MOSFETs. The gates are defined by the conventional photolithography and ICP etch method. By using PR mask which covers only SiNW channel, the gate for MOSFETs and source/drain regions for both kinds of the devices are doped by As^+ ion implantation for n-type source/drain and

BF_2^+ ion implantation for p-type source/drain, respectively. After PR strip, they are annealed at 1000 °C for 30 minutes for unifrom doping concentration for 80nm-thick source/drain region.

Although the back-end process of SiNW FET sensor is compatible with conventional CMOS process technology, some critical issues should be considered in sensing area formation. Same as conventional back-end process, 500-nm-oxide as an inter-layer dielectric is deposited via HDP CVD and is planarized through chemical mechanical planarization (CMP) process. There are two reasons for the CMP process. The first is to prevent poor surface which can cause disconnected metal line. The other is related to the opening of sensing area. To detect pH level, the surface of silicon channel should interact with chemical solution directly. Therefore, all oxide material surrounding SiNW channel including gate oxide and ILD should be removed. During the oxide etch, only dry etch is allowed, since wet etch process causes vacant space at the bottom of the silicon nanowire channel, resulting in broken nanowire. To prevent the formation of oxide sidewall spacer on SiNW, the planarization is necessary. After CMP process, the contact holes are formed by the photolithography and magnetically enhanced reactive ion etching (MERIE) in CHF_3 /CF_4 plasma, and the formation of aluminum electrodes is performed using Al sputtering, photolithography, and RIE in BCl_2/Cl_2 plasma. Then, tetra-ethyl-ortho-silicate (TEOS) is deposited as passivation oxide to protect metal lines from chemical solution, and the pad region for measurement is formed by the photolithography and RIE in CHF_3 /CF_4 plasma. The final key process is opening sensing

area which is only different from MOSFET process.

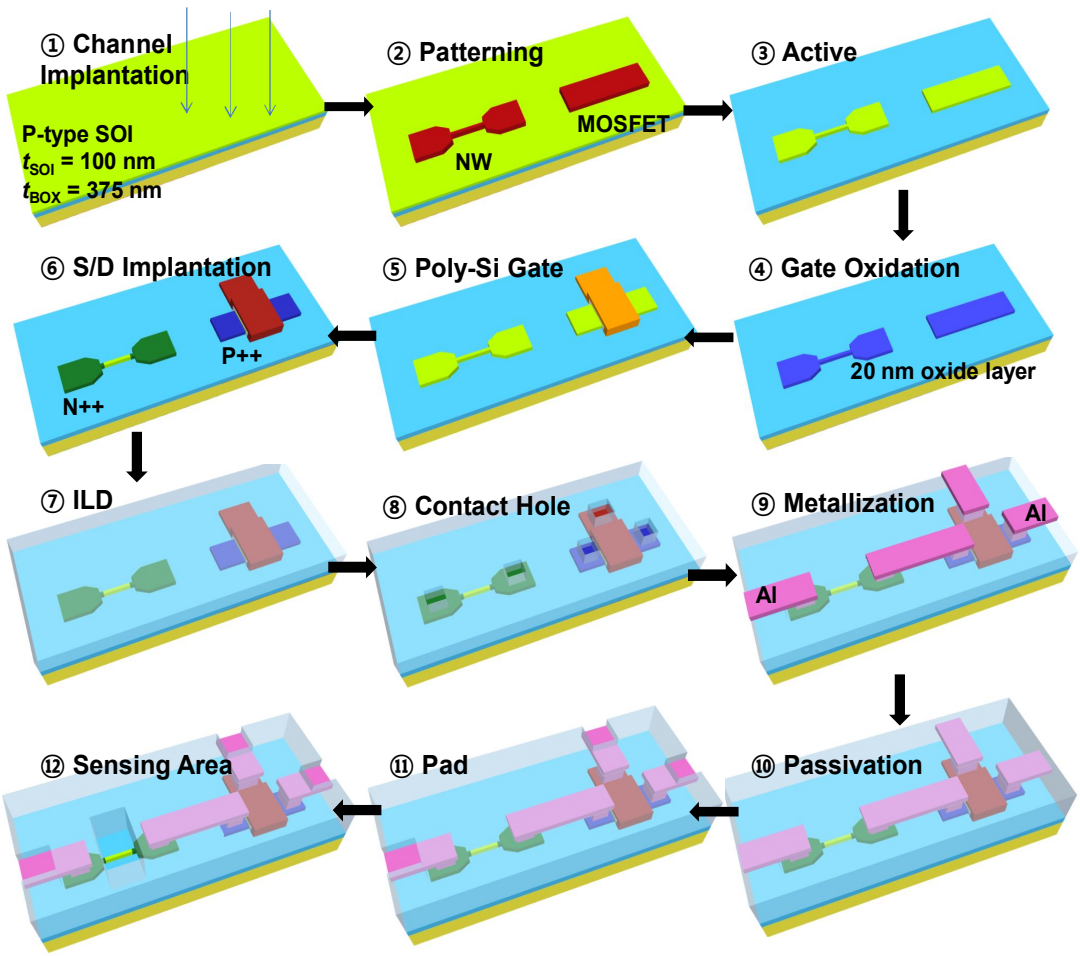


Fig. 2.1 Fabrication process of the SiNW FET sensor with MOSFET.

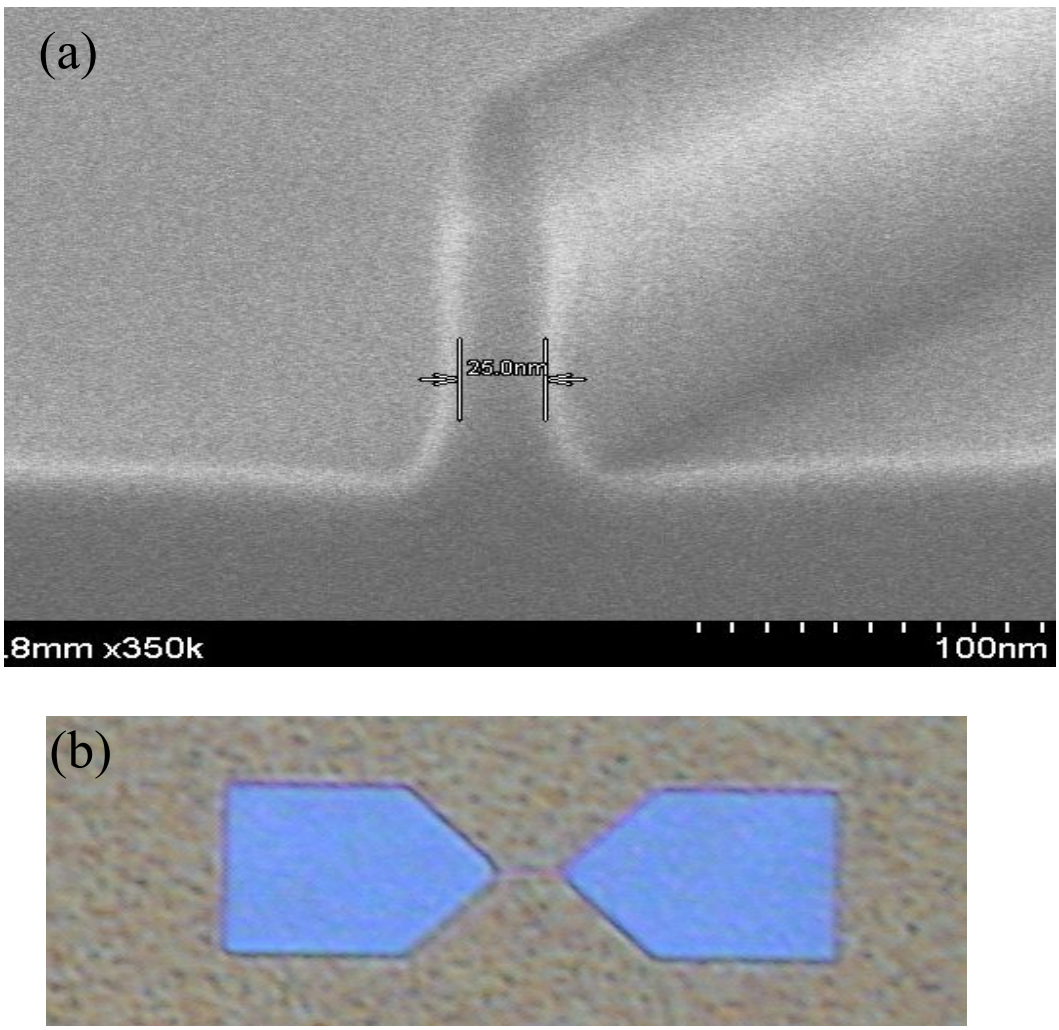


Fig. 2.2 (a) Scanning electron microscope(SEM) image of nanowire pattern by e-beam lithography and etch and (b) optical image after mix-and-match process.

After patterning by photolithography, the 300nm-thick oxide layer should be etched by RIE in CHF_3 /CF_4 plasma to prevent the damage to the silicon channel since the RIE has possibility to remove silicon nano-wire channel.

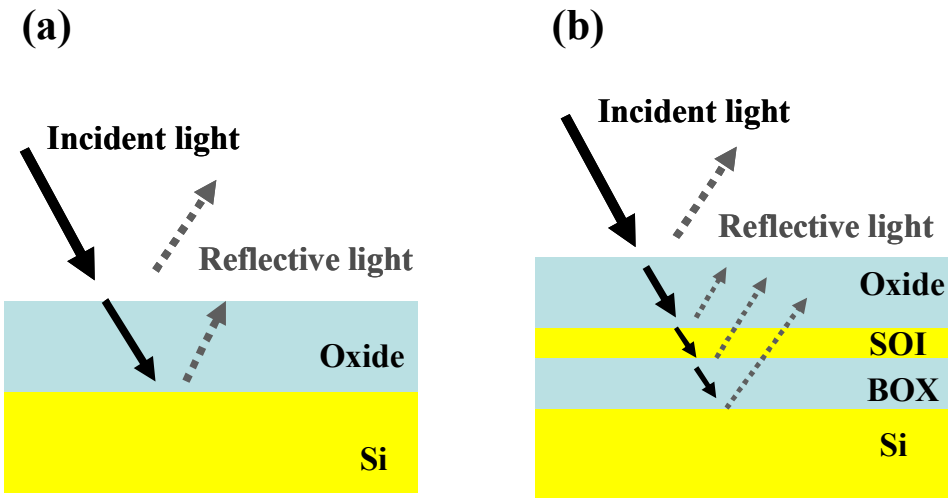


Fig. 2.3 Optical interference effects on (a) bulk silicon and (b) SOI wafer

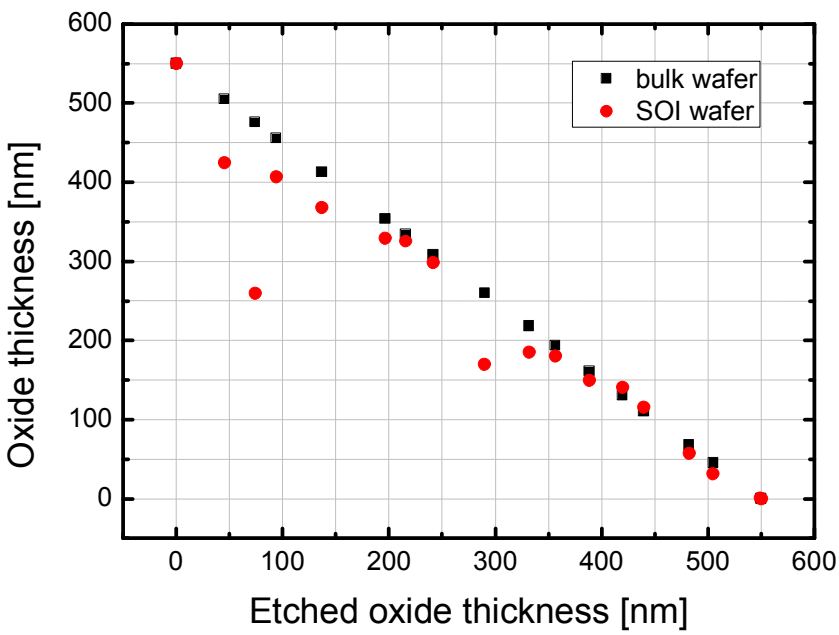


Fig. 2.4 Optical measuremets of the oxide thickness on the sample.

For the reason, timed etch process is used through semi-real time monitoring which means repeating oxide etch and thickness measurment. The oxide layer is measured by optical method and this causes a critical problem. Since it is imposssible to measure the oxide layer on silicon nano-wire channel, we measured it on the capacitor pattern. However, the optical equipement cannot detect the thickness correctly in a particular range on SOI wafer (differently from that on bulk silicon wafer) as shown in Fig. 2.3. Since the interference is dominant, the critical error occurs in the paticular range near 220 nm and 450 nm of oxide thickness. The result is presneted in Fig. 2.4

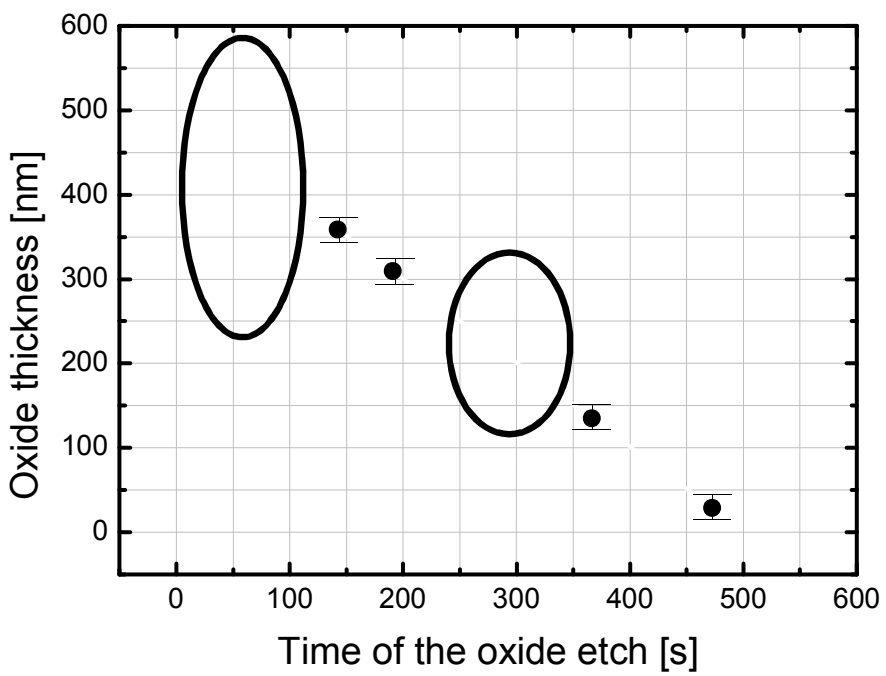


Fig. 2.5 Optical measuremets of the same oxide thickness on the sample.

To avoid the interfence range, the oxide etch and optical measurement are repeated to open sensing area. The progress of removing oxide layer for sensing area is illustrated in Fig. 2.5. After alloy process, the fabrication is completed.

2.2 Investigation of the Fabricated Devices

To check the fulfillment of some essential requirements mentioned in Chapter 1, investigation by scanning electron microscope(SEM) images is conducted before electrical measuremnt. The fabricated 6-inch SOI wafer and its single chip (9 mm × 9 mm) are shown in Fig. 2. 6 (a) and (b), respectively. 11 masks are used in the wafer-scale process. 83 SiNW FETs are integrated in each chip. To attach micro-fluidic channel and make aqueous solution reach the silicon channel, the SiNW sensors are located at the center of each chip and pads are located on the edge of each chip.

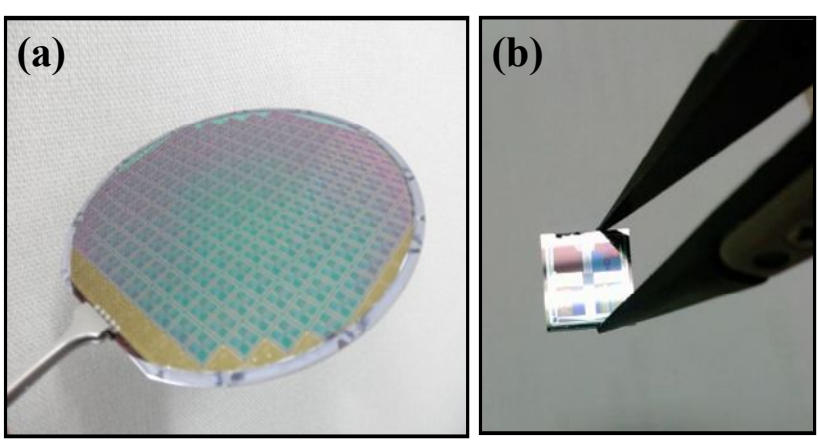


Fig. 2.6 Optical images of the (a) wafer and (b) a single chip incluing SiNW FET sensors and MOSFETs

As mentioned above, nanowire formation for a high surface-to-volume ratio are verified through SEM images shown in Fig. 2.7. From the observations, the controllability of the width and alignment of SiNWs are proved in our fabrication as shown in Fig. 2.8. The measured samples indicate that over 99 % of SiNWs among all integrated ones on the 6-inch SOI wafer have been built as the designed value. Fig 2.9 shows the cross-sectional SEM image of test pattern to verify the formation of the sensing area. The oxide on the sensing region is etched down to the level of the active region. The result proves that the progress in Fig. 2.5 is effective for oxide etch on SOI wafer. Therefore, the proposed process flow is confirmed to be suitable for high-quality mass production.

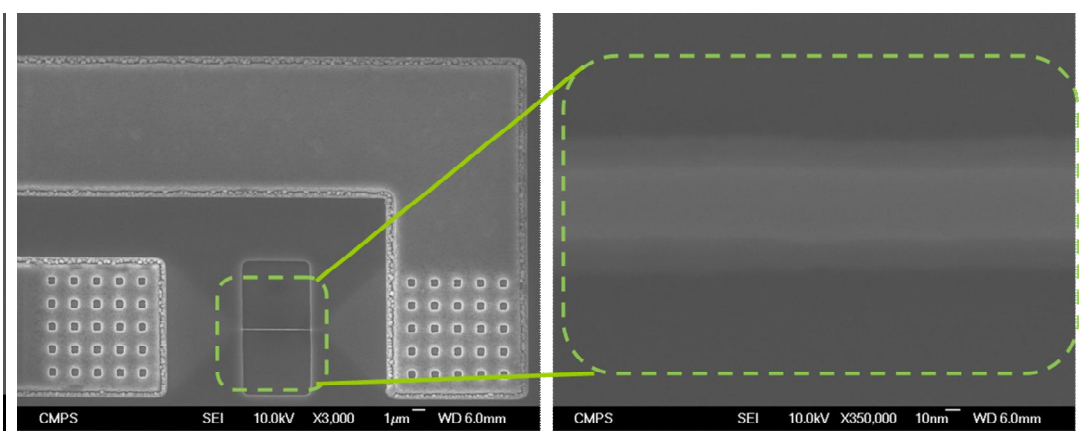


Fig. 2.7. SEM image of the fabricated silicon nanowire FET sensor.

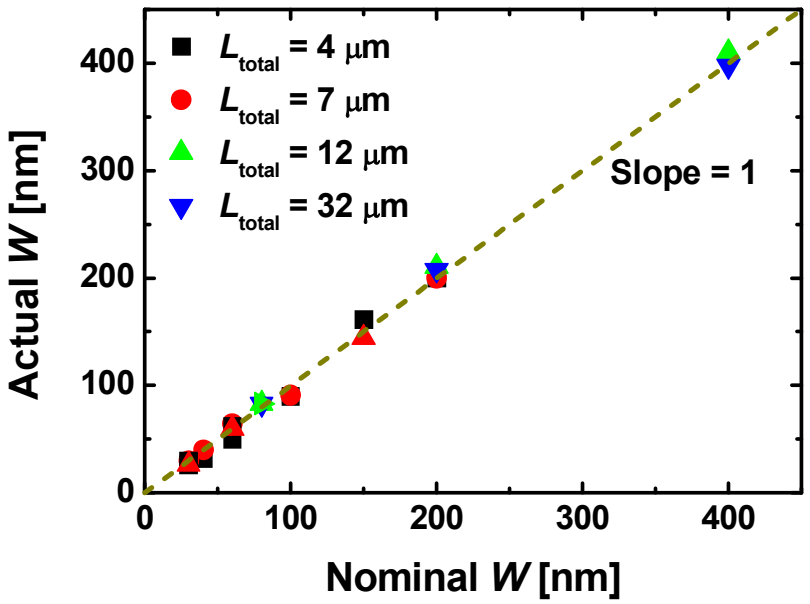


Fig. 2.8. Nominal *W* versus actual *W* of SiNWs integrated on the 6-inch SOI wafer.

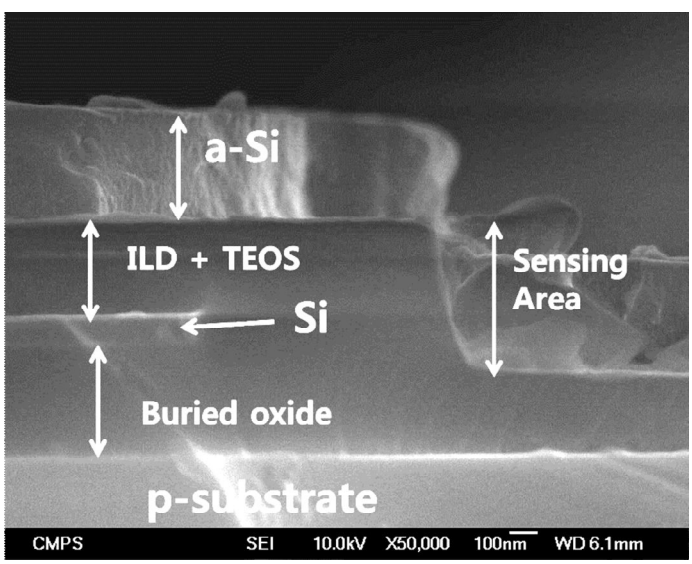


Fig. 2.9. Cross-sectional SEM image of the active region by sensing area.

2.3 Surface Treatement and Microfluidic Channel

To have a linear change in the total surface charge density as a function of pH, we applied the amine ($–NH_2$) functionalization on the SiO_2 surface introduced in Section 1.2. It allows us to observe the linear response [27,32]. Immobilization of $–NH_2$ on a thin oxide surface of SiNW parts was prepared via the following three-step procedure. First, the device was treated by UV O_3 for 330 sec to introduce more hydroxyl (-OH) group on Si oxide surface than usual. Second, the device was functionalized with 1 % 3-aminopropyltriethoxysilane (APTES) in 95 % ethanol solution for 30 min. Last, it was dried in N_2 and heated on hotplate for 10 min at 120 °C. After 3 times of repeated rinsing it with 95 % ethanol and dried in N_2, it is heated again at the same condition as above. Finally, the $–NH_2$ surface was obtained on thin oxide surface on SiNW parts.

In addition, the another role of the 3-APTES is protection layer for silicon channel. Without 3-APTES, the gate insulater has only hydroxyl (-OH) group. In this case, the sensor has unstable properties as shown in Fig. 2.10. At first, the drain current appears to be increased. However, after the increase, the current is decreased continuously and the devices are broken in very high possibilty since the oxide is unstable material in aqueous solution. 3-APTES prevent the decreasing effect. Therefore, the current is saturated stably.

A polydimethylsiloxane (PDMS) fluidic channel was prepared for a fluidic transport of the analyte solution. First of all, PDMS master was fabricated on a 1-mm-thick 4-inch Si wafer in Fig. 2.11 (a). The master was filled with a fully-stirred mixture of 40 g

Sylgard-184 silicone elastomer and 4 g Sylgard-184 silicon elastomer curing agent and then it was baked at 80 °C for 3 hours. Then, the cured PDMS was taken off and cut to fit with the final chip dimensions around the channel. The volume of the cell is as follows: the size of the fluidic channel on the chip (9 mm × 9 mm) is approximately 4.6 mm × 3 mm × 200 μm (length×width×height). In order to construct a PDMS fluidic channel on the chip (Fig. 2. 11 (b), (c) and (d)), they were exposed to UV O_3 for 330 sec and bonded together.

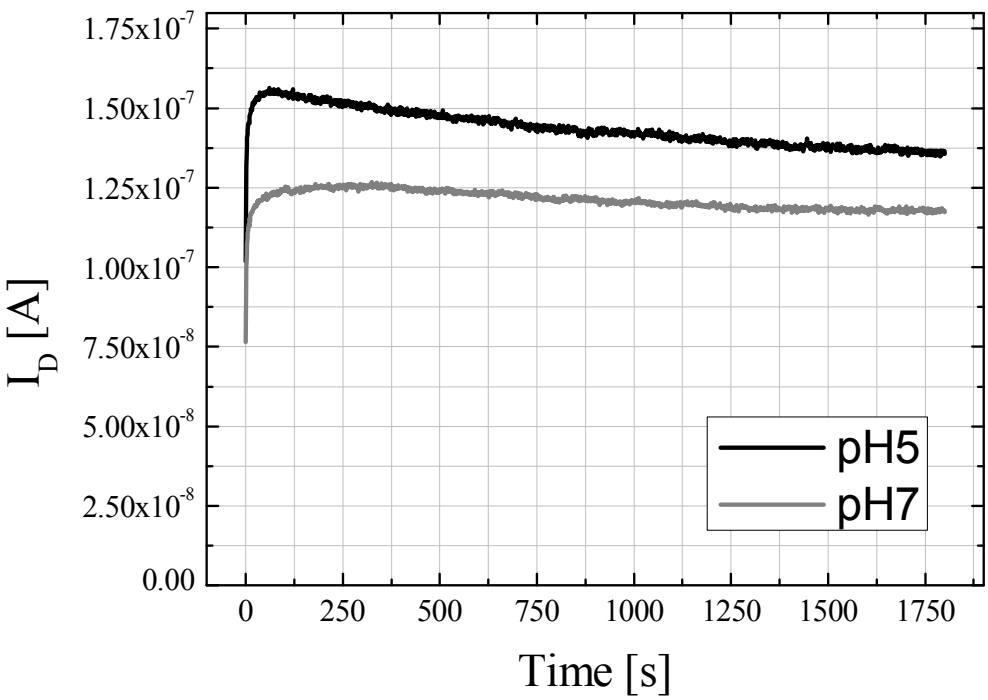


Fig. 2.10. Transfet characteristics of the fabricated sensor without 3-APTES. The silicon channel is surrounded by oxide. The current is decreased continously after increase.

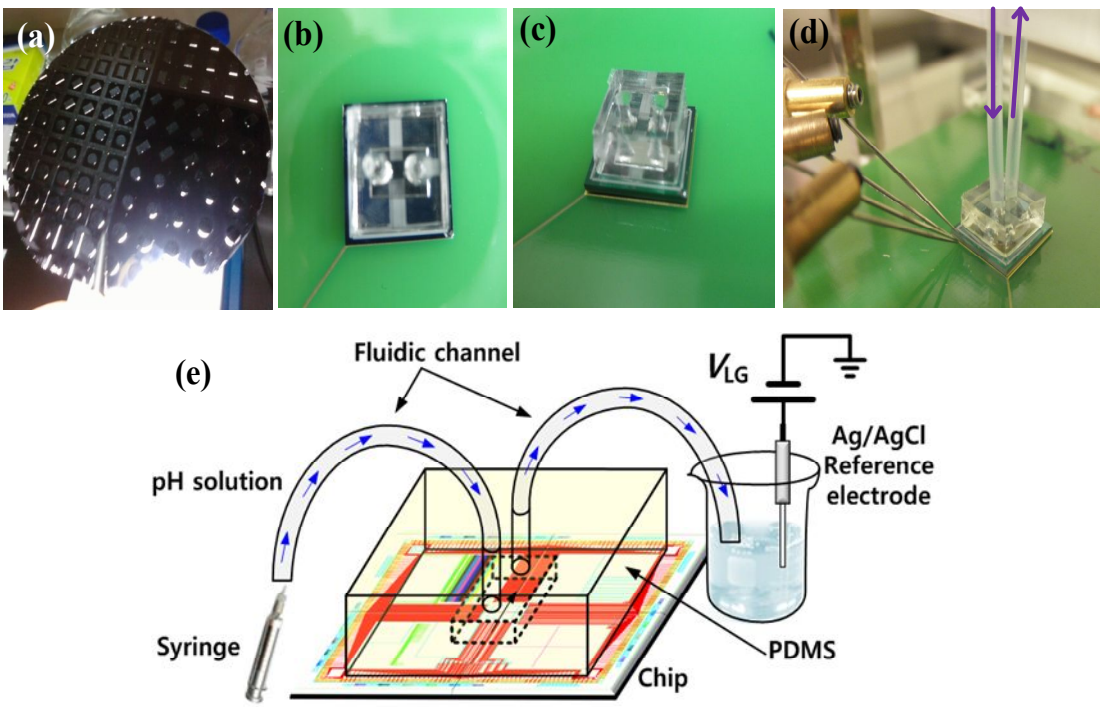


Fig. 2.11. (a) Fabricated PDMS channel master on 4-inch Si wafer. (b) Top view and (c) bird's eye view of PDMS channel attached to the fabricated chip. (d) Measurement setup with tube. (e) Schematic diagram of the measurement set-up.

Then, it was heated on a hot plate at 120 °C for 10 min. This procedure was performed prior to the amino-functionalization because it is difficult to bond PDMS on the $-NH_2$ surface. The final measurement setup with tubing lines (inner diameter = 400 μm, outer diameter = 1.6 mm) on a probe station was shown in Fig. 2.11(d). A schematic diagram for the measurement setup using the PDMS fluidic channel is shown in Fig. 2.11(e).

2.4 Buffer Solution and Reference Electrode

The fabricated SiNW FETs for measurement had only the gate of back side, i.e. Si substrate. The bias voltage of the back side causes the measurement unstable owing to fluctuation of the liquid potential[33]. For the reason, the Ag/AgCl reference electrode was employed as a liquid-gate (V_{LG}) to control the reference electrical potential of electrolyte solution. In addition, potassium dihydrogen phosphate (KH_2PO_4) and potassium monohydrogen phosphate (K_2HPO_4) were used to control buffer solutions with HCl and KOH. The salt concentration used in this study were 0.1 M (pH 5~9). We use a disposable syringe to change the pH value of electrolyte solution. The electrical measurement was conducted with the semiconductor parameter analyzer (Agilent 4156C) after the flow of electrolyte solution was sufficiently stabilized.

Chapter 3

Electrical Properties

3.1 Concept of the ISFET

As silicon technology is widely used for sensor development, the silicon devices are devised for the application to biosensors. One of the outstanding invention is ion sensitive field effect transistor (ISFET), proposed in 1970 by Bergveld [34, 35], which detect the hydrogen ions and produce electrical output. Due to their small size, rapid pH response and rugged solid-state construction, ISFETs exhibit a number of advantages over conventional pH-glass electrodes.

Since many biochemical reactions produce or release the hydrogen ions in the solution, it lead to changing concentration of the hydrogen ions. By detecting the concentration, other reactions can also be probed. The popular example of ISFET application is non-optical DNA sequencing introduced by Ion Torrent of Life Technoloy[53]. The ISFETs can detect the DNA senquencing since the realeased protons from the ion senquencing produce a shift in the pH of the surrounding solutions. Since ISFET is the basic sensor in many biochmical sensors, many researches of physical models provide well understood operation mechasism. These are the reasons why our

fabricated SiNW sensor operates as a pH detector.

Fig. 3. 1 (a) shows the basic structure of ISFET measurement contition [36]. Since our devices are fabricated on an SOI wafer, the condition is like Fig. 3.1(b). The BOX and Si substrate act as a back gate insulator and a back gate, respectively. However, the measuement condition results in instability owing to floating state of electrolyte which is more dominant to nanowire channel [33]. In terms of theoretical background, the site-binding model is the most popular and well proven. A potential distribution and charges shown in Fig. 3.2 is the basis of most physical models [36]. By using the site-binding model[36] and Poisson-Boltzman equation, the surface potential (ψ_s) with the pH level at the interface between the native oxide and the electrolyte can be defined as follow:

$$\psi_s \ \alpha \ -2.303a\frac{kT}{q}(pH - pH_{pzc}) \tag{3.1}$$

where pH_{pzc} is the point of zero charge of the insulator, a is a constant dimensionless parameter such that the response of sensors vary linearly with pH of solution [$0 \leq a \leq 1$ (ideal case)] [37]. That means the surface potential is proportional to the pH level. The common logarithmic change of the hydrogen concetration results in linear changes in the threshold voltage.

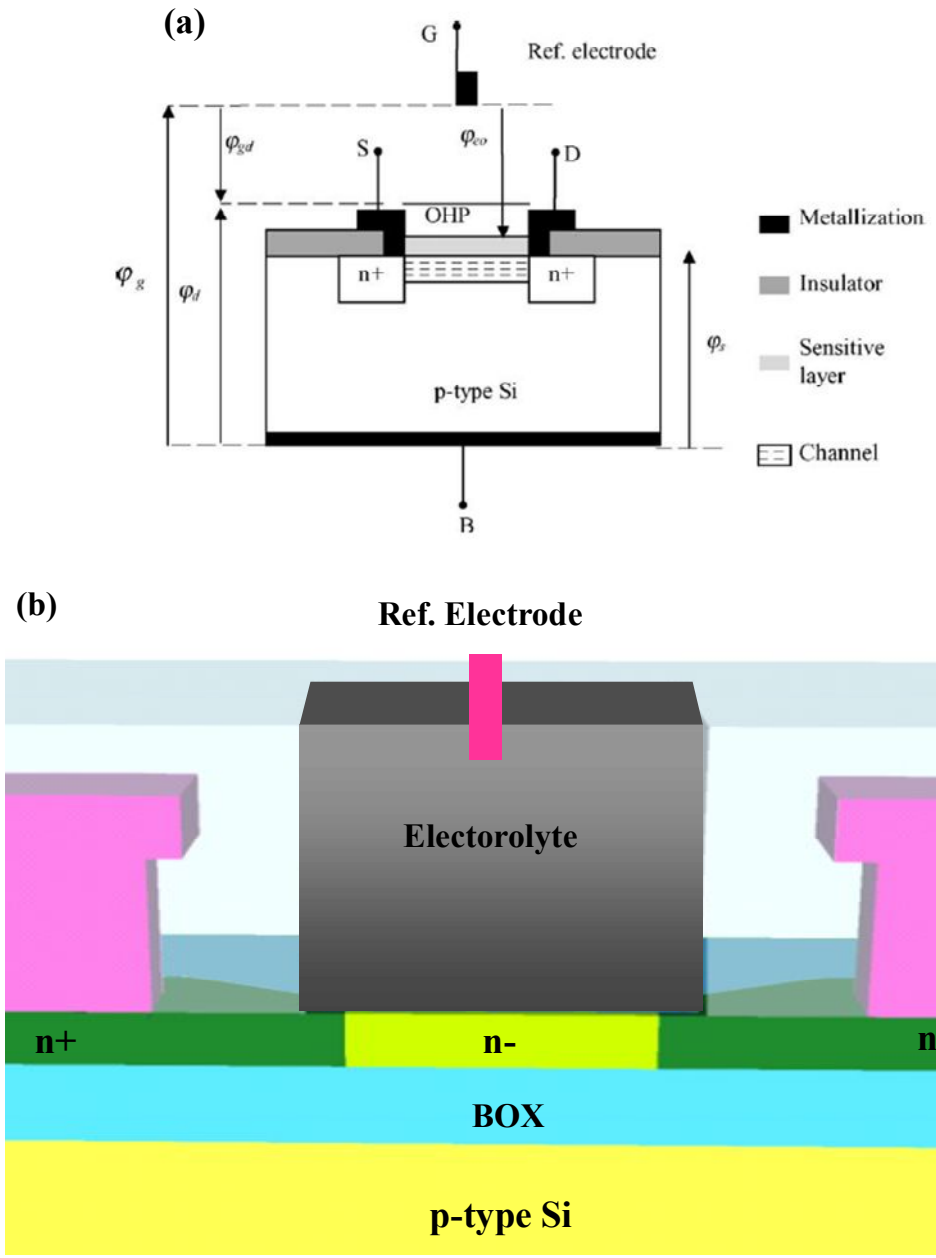


Fig. 3.1. (a) Typical measurement condition of bulk Si ISFET [36] and that of SOI wafer. The substrate is isolated by BOX. OHP indicates the outer Helmholtz plane.

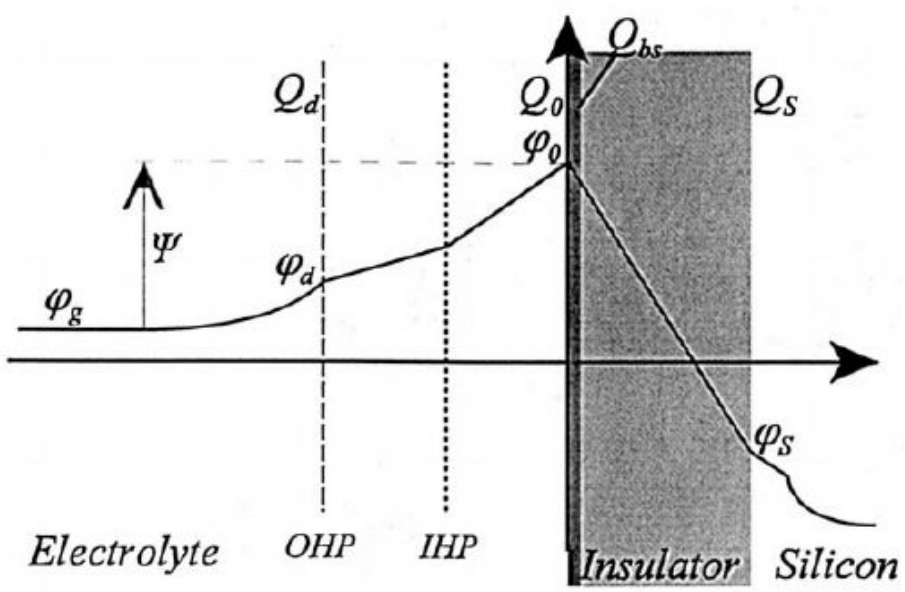


Fig. 3.2. Potential distribution and charges of an n-channel ISFET. OHP/ IHP indicates the outer/inner Helmholtz plane, respectively.

Considering the change of pH level, the surface potential changes more negatively when pH increases from Eq. (3.1). Therefore, n-type NW FET in depetion mode becomes more depleted with the increase of pH and the p-type NW FET is more accumulated. The theoretical limit for the rate of change of surface potential with pH is predicted as

$$\frac{d\psi_s}{dpH} = -2.303a\frac{kT}{q} \tag{3.2}$$

The rate of the maximun change of the surface potential with pH is 60 mV/pH at room

temperature according to Eq. (3.2), which is the well-known Nernst limit.

3.2 Transfer Charateristics

Most electrical characteristics of the fabricated SiNW FET sensor have been demonstated except time dependent measurement [36, 38, 39]. The potential of the fabricated SiNW devices for electrochemical detection was evaluated by monitoring the behavior of APTES-modified SiNW as a function of the pH solutions. Five different pH values were investigated, *i.e.*, pH 5, 6, 7, 8, and 9 confirmed by pH meter. At each pH, the drain current I_{DS} was measured at a constant V_{DS} = 1.2 V while V_{LG} was swept from 0.7 to -0.3 V for p-type and from 0 to 1 V for n-type with 10 mV step. Finally, the transfer characteristics of p-type and n-type SiNW FETs are measured for five different pH values, respectively, as shown in Fig. 3.4. As the pH level becomes higher, the conductance of p-type NW FET increases while the conductance of n-type NW FET decreases as the threshole voltage is changed. Since the measurement conditions are sub threshold swing region, the changes are linear and the amount is under 60 mV/pH. The results are consistent with Eq. 3.4 from site-binding model and Nernst limit.

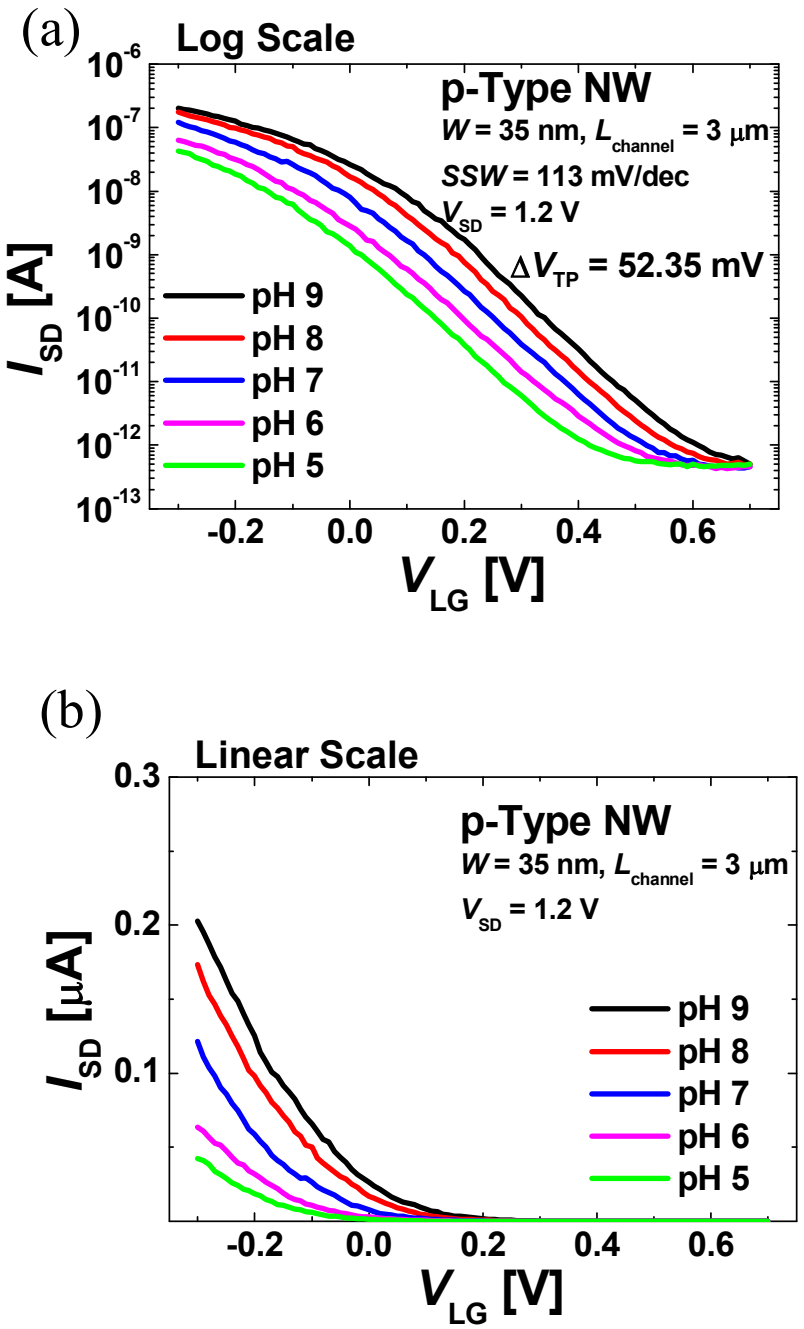


Fig. 3.4. Transfer characteristics of p-type SiNW according to pH level on (a) log scale and (b) linear scale of the drain current.

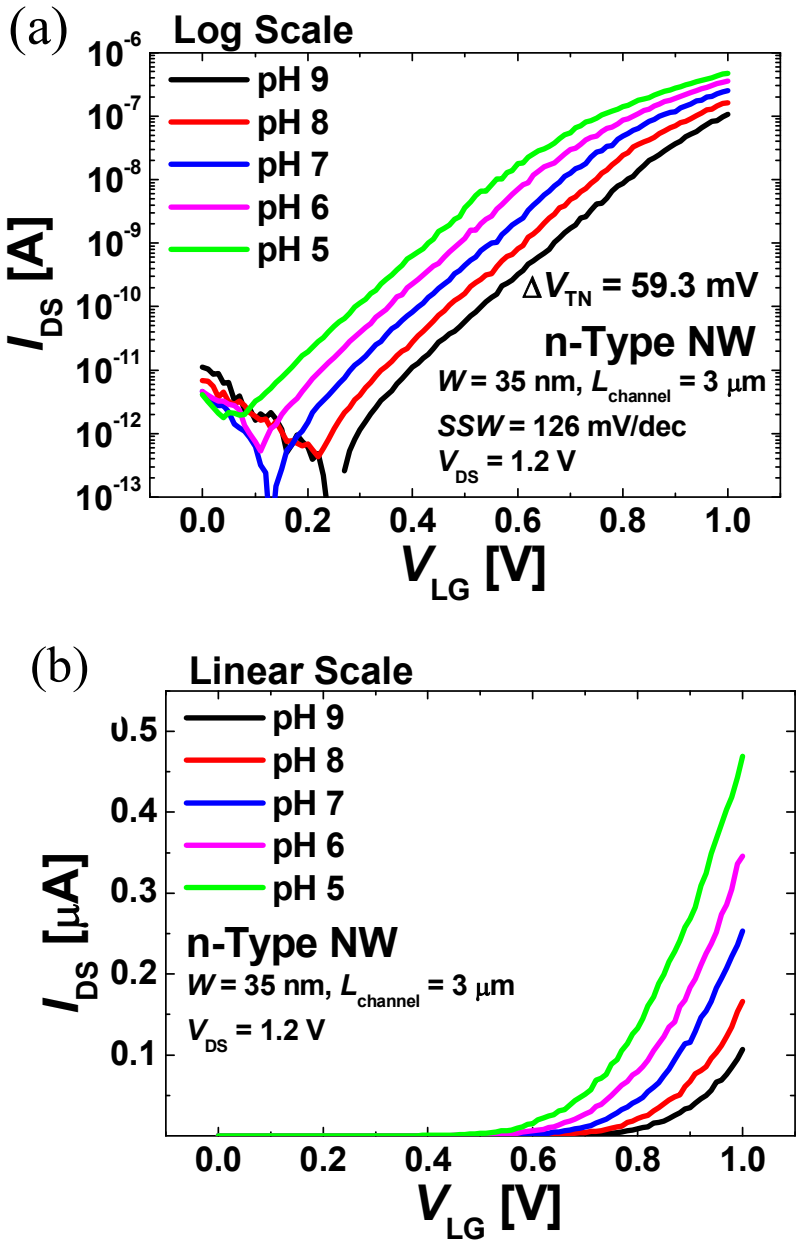


Fig. 3.5. Transfer characteristics of n-type SiNW according to pH level on (a) log scale and (b) linear scale of the drain current.

3.3 Integrated SiNW Nanowire FET sensor.

The SiNW FET sensor fabricated through the proposed method, complementary SiNW ISFET and SiNW-MOSFET hybrid ISFET, have been demonstrated in two papers[38, 39]. One of the most important issues of FET sensors is to increase sensitivity. It is the reason why high surface-to-volume ratio is emphasized in FET sensor study. However, the maximum change of threshold voltage is 60 mV by nernst limit. In other words, a single SINW ISFET has limitation to improve sensivity. Similar to micro-electronic system, the proposed SiNW FET can solve the problem by complementary SiNW ISFETs which has been demonstrated. Fig. 3.6 illustates the schematic diagram and a SEM image of that. The inverter type sensor can exceed the sensitivity of 60 mV/pH since both of the n-channel and p-channel FET react pH solutions simultaneouly, the threshold voltage changing in the same direction. For example, if the pH solution is changed from pH 7 to pH 5, the higher concentration of the hydrogen ions distributes surrounding the silicon channel. The threshold voltage of the n-channel FET, pull-down devices, is decreased and it induces increased conductance. In the case of the p-channel FET, the absolute value of the threshold voltage is decreased and the conductance of that is decreased. Both of the operations shift the logic threshold voltage (V_{TC}) as shown in Fig. 3.7(a). Figure 3.7(b) confirms that the inverter type ISFET can overcome the sensitivity limit of 60 mV/ pH defined by Nernst limit [38].

In addition, the operation of the SiNW-CMOS hybrid common source amplifier

is verified [39]. The schematic diagram and the equivalent circuit diagram of the integrated SiNW-CMOS hybrid common source amplifier is shown in Fig. 3.8. It is a typical prototype of SiNW-CMOS hybrid circuits. This circuit has an advantage to be relatively free from the problems arising from channel doping variation since the MOSFET can be controlled by its independent gate bias.

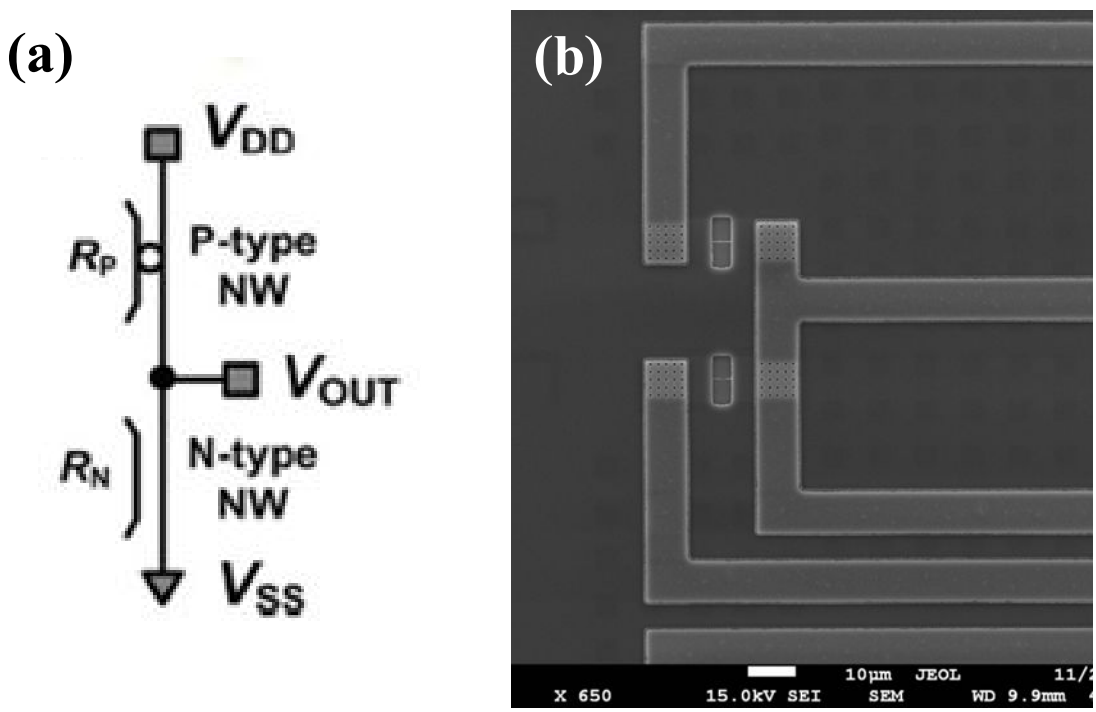


Fig. 3.6. (a) Schematic diagram of the complementary SiNW ISFET and (b) a SEM image of the fabricated devices.

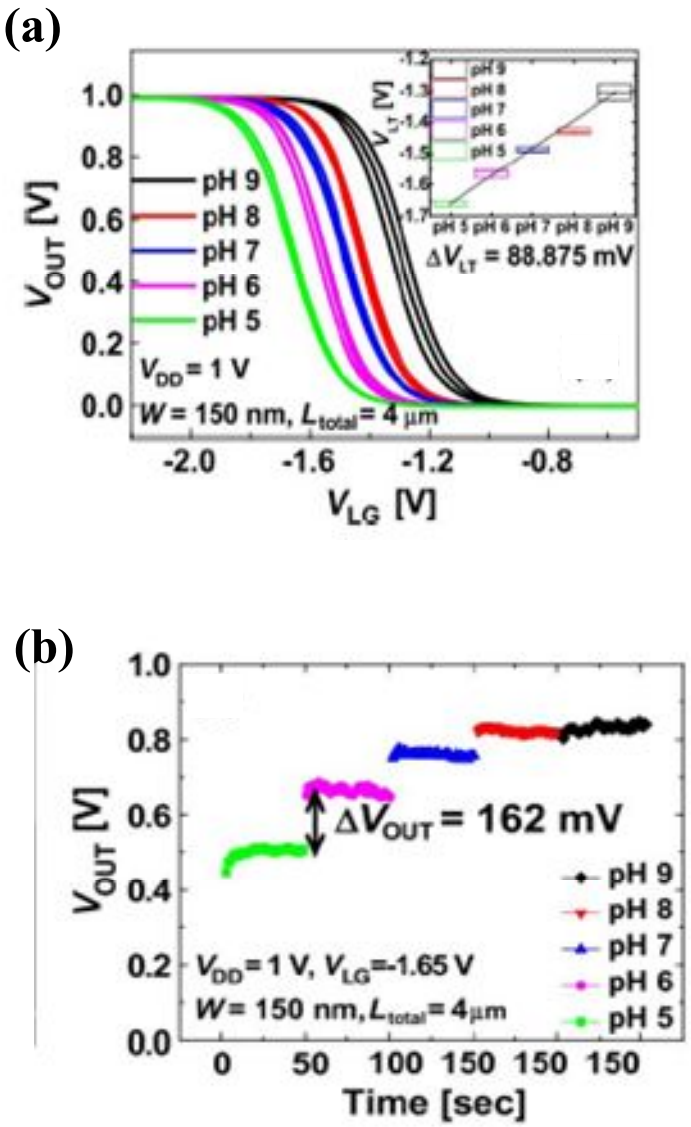


Fig. 3.7. (a) Voltage transfer characteristic of complementary SiNW sensor depending on pH levels. Inset shows the logic threshold (V_{LT}) at each pH level with error bars. (b) The measured time-dependent V_{OUT} with changing pH level at fixed V_{LG}.

The current, I_{DS}, is well modulated by V_{GS} and V_{DS}. Furthermore, the measured transfer characteristics of n-type SiNW FET composied of SiNW-CMOS hybrid common source amplifier is shown in Fig. 3.9(a). Therefore, it is found that CMOSFETs are successfully integrated with SiNWs on the same wafer. Fig. 3.9(b) shows the measured V_{TC} of SiNW-CMOS hybrid common source amplifier according to pH level, which is sensitively modulated by the change of pH level.

3.4 Reproducibility of the Fabricated Devices.

From the demonstration of previous section, the basic electical charateristics of the fabricated devices are verified except reproducibility which means that the value of output current should have the same value at the same pH level when the pH solutions are randomly changed. To test the repeatibility of SiNW FETs in pH detection, n-channel device with W = 50, 80 nm, L = 2 μm, is used of pH level ranging from 5 to 9. Experimental set-up is the same as that of Section 3.3. At each pH level, the drain current (I_D) is measured for 50 seconds with bias conditions of $V_{LG} = V_D = 1$ V. After detecting pH level for 50 s, the solution is changed to that with other pH level. It takes a few minutes to prepare each next measurement. Fig. 3.10 shows the measurement results at each pH level for 50 s. The variation of the output currents is quite large. Most output values are different in the repeated detection at the same pH level. The main reason of the poor reproducibility is the current drift effect.

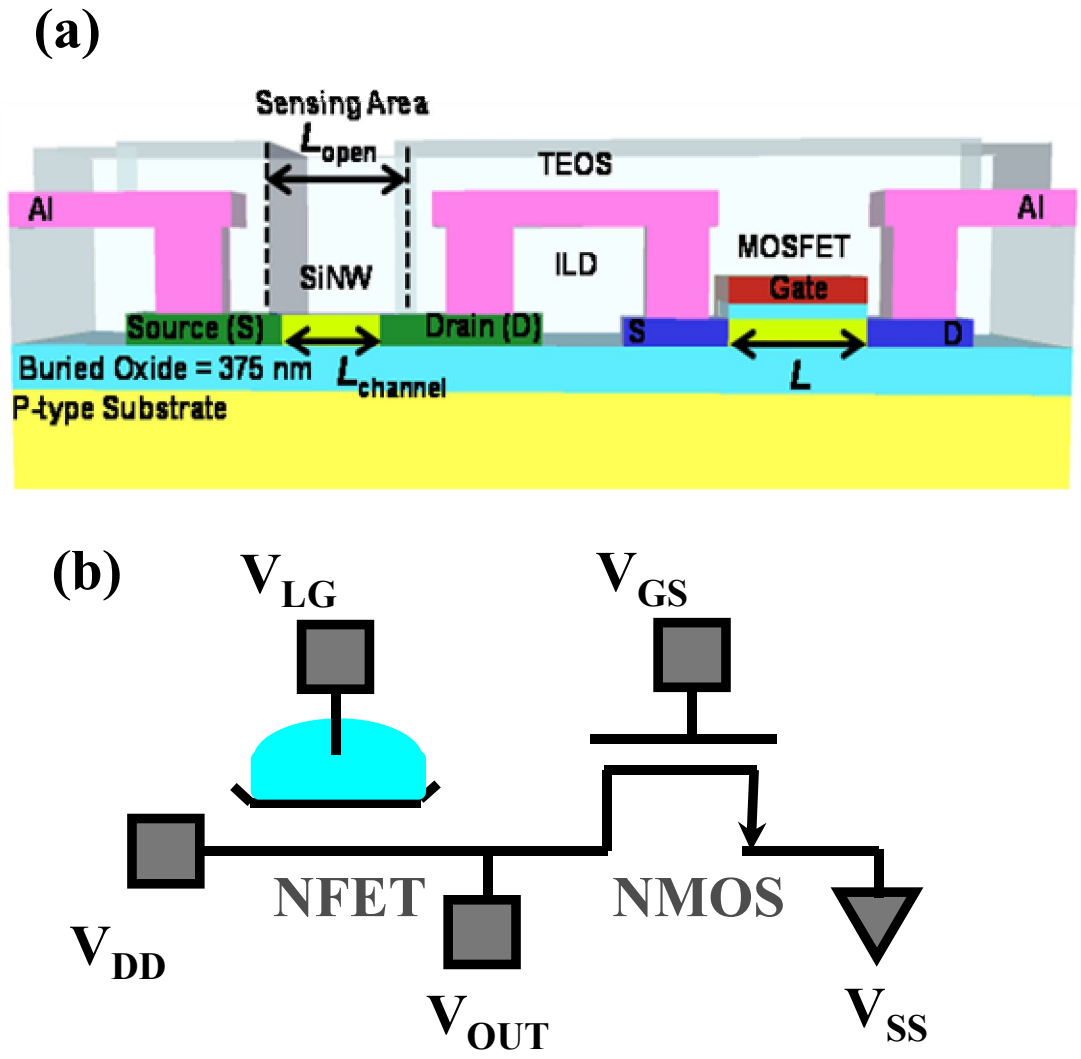


Fig. 3.8. (a) Schematic diagram of the complementary ISFET with MOSFET as common-source amplifier and (b) an equivalent circuit.

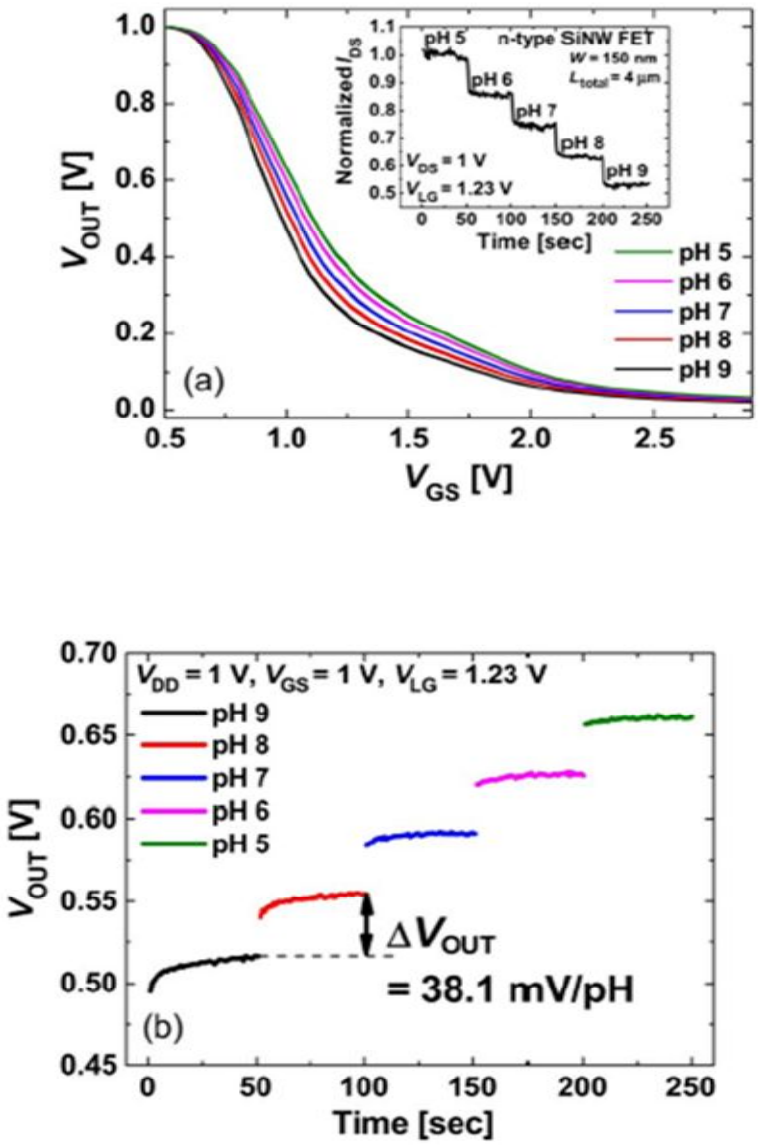


Fig. 3.9. (a) Measured V_{TC} of SiNW-CMOS hybrid common source amplifier according to pH level. (b) The measured time-varying V_{OUT} with changing pH level at fixed V_{LG}.

As seen in Fig. 3.10, quite a significant drift of current is observed during 50 s. In

addition, there are also significant drifts of current between measurements on the solutions with the same pH level. This means SiNW FET sensor has low reproducibility in this operation scheme. If the measurements were done only once for each pH level in an increasing (or decreasing) sequence of pH, such a drift might not be noticed. Without solving the drift problem, it is impossible for SiNW FET to work as a reliable pH detector.

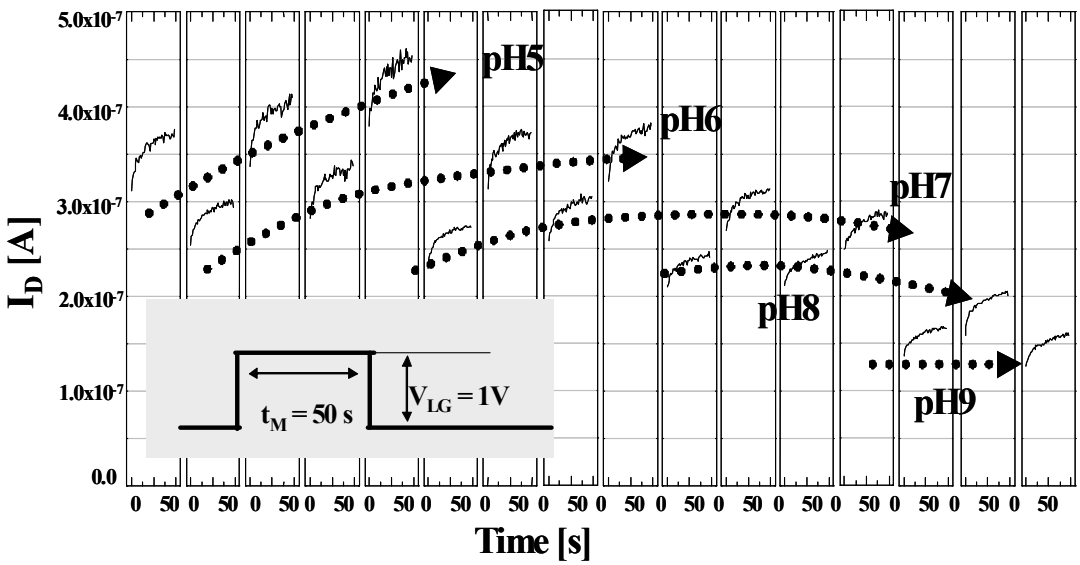


Fig. 3.10 Transient characteristic of fabricated SiNW FET sensor as a pH detector

(W = 50 nm, L = 2 m, V_S = 0 V, V_D = 1 V, V_{LG} = 1V)

For a example, the first and seventh measurements show almost the same current level, even though their pH levels are 5 and 6, respectively. The amount of current drift within and between measurements indicates that the time constant involved in the drift

mechanism is much longer than 50 s at the given bias conditions. Other researches also show the drift effect during pH detecion [28, 29, 40]. To anayze the drift effect, long time measurment is needed since it is very important how long time is required for the current to be saturated. As shown in Fig. 3. 11, long time measurement is conducted to find the time constant for the current drift.

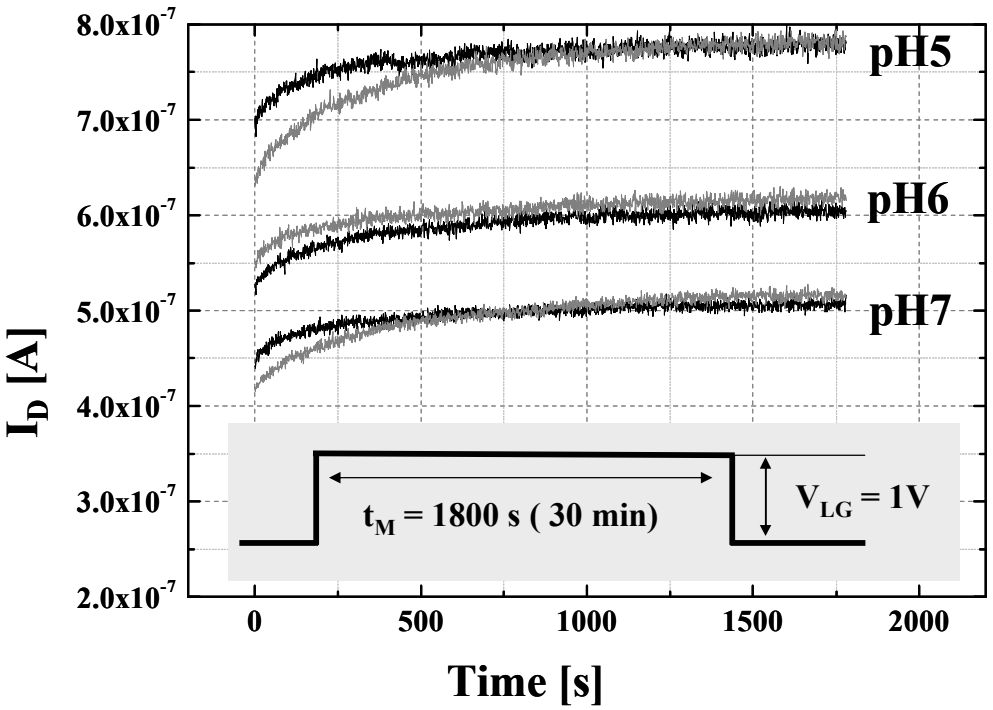


Fig. 3.11 Characteristic of SiNW FET as a pH detector with long measurement time, t_M = 1800 s. (W = 80 nm, L = 2 μm)

When the measuring time is increased to 30 minutes, the drain current (I_D)

reaches almost a constant value after 15 minutes. For the measuring time less than 15 minutes, the variation of I_D is significant. The long time delay before stabilization of current makes the measurement quite impractical since SiNW FET is expected to perform a fast measuremnent (less than a few minutes) as mentioned in Chapter 1.

Chapter 4

Electrical Circuit Model for Measurement

4.1 Previous Works

The drift effect means monotonic temporal change in the same direction and it has been researched owing its importance since it is impossible for SiNW FET to work as a reliable pH detector. Threfore, the phenomenon have been researched to understand the mechanism[41]. The reaction of output is categorized as slow and fast response. The fast response time is defined as the time which is needed for the output to change rapidly (less than a few second, usually). The slow response need extra time to reach the final value. There is a large time difference between them. In our case of the Fig 3.11, the drain current increase rapidly in a few seconds at first. After that, the current increase slowly until 1000 s. The fast and slow responses are ditinguished by time scale. The main reason of slow response is the presence of buried sites which is the basis of the modelings to explain drift phenomenon [41].

In addition, at various salt concentrations from 0.001x to 1x, the drift effect is also

observed, and at low pH level and high liquid gate bias (V_{LG}) which means higher hydrogen concentration, the change by drift is increased. It indicates that the main reason for slow pH response of inorganic ISFET is associated with hydrogen concentration and the presence of buried sites such as internal OH groups [41- 43]. Fig. 4.1 describes fast and slow response, quantitatively. Initial state is assumed in Fig. 4.1(a). As the positive bias is applied to the liquid gate, the high concentration of the hydrogen ions leads to the hydration on the surface quickly. The internal OH groups, however, need more time to change their states since the low diffusion constant of hydrogen ions in oxide leads to slow movement.

Especially, the diffusion constant of pure oxide is much lower than that of oxide with defects ($D_{ox}(H^+)$ with defects ~ 10^{-18} cm^2/s, $D_{ox}(H^+)$ of pure oxide ~ 10^{-23} cm^2/s). It is noted that the corresponding diffusion length in pure oxide is 0.2 nm in one year. That means that the ions cannot move through the pure oxide. On the other hand, H^+ can be diffused in the oxide with defects although the process is slow as shown in Fig. 4(d). For the reason, the slowly diffusing H^+ causes drift effect owing to the change of the potential in the silicon channel. In addition, there is another evidence. The reference electrode is free from the drift issue. Fig 2. 2 show the result. The input bias voltage in Fig 2. 2(a) is as same as obverved output bias voltage in Fig 2. 2(b) expcet for offset value from work-fuction difference between reference electrode and pH 7 solution. This suggests that the cause of drift exists between gate insulator and electrolyte.

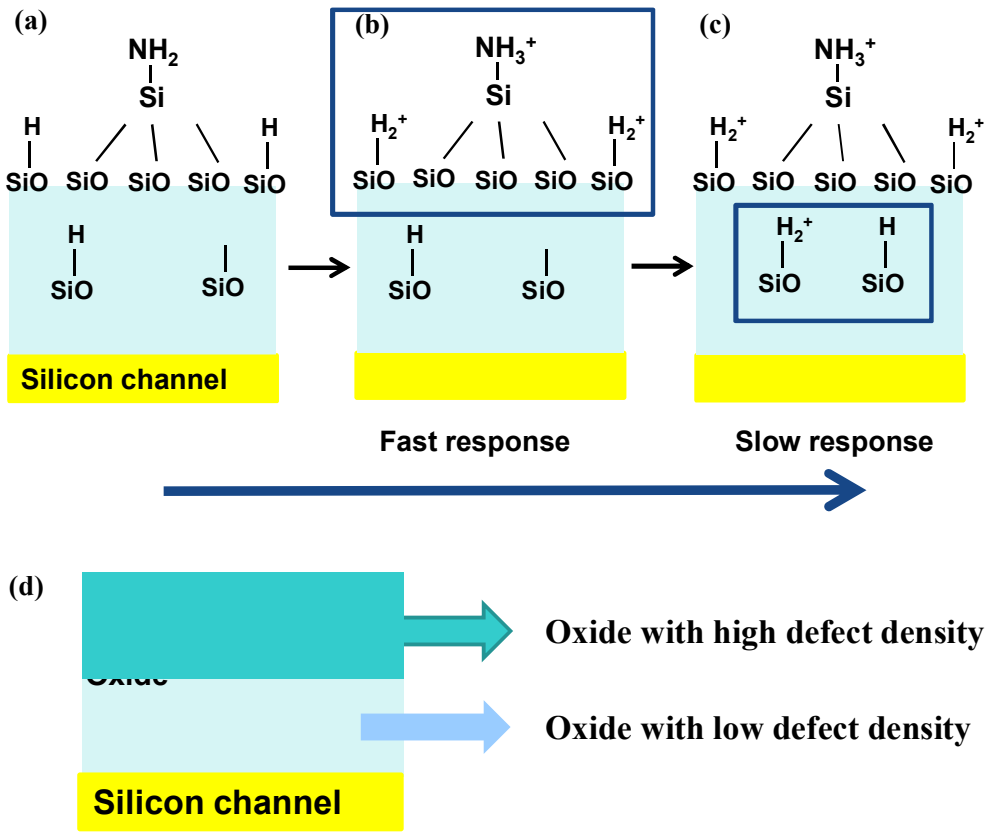


Fig. 4.1 A schematic diagrams to explain the role of the buried silano groups. A initial state is assumed before liquid gate is not applied. (b) As the bias applied, the reacions on surface occurs fast. (c) The buried sites, however, react slowly. (d) The gate oxide is composed of pure oxide and oxide with defects. It is assumed that hydrogen ions is moved only in defective oxide since the ions rarely are diffused in the pure oxide.

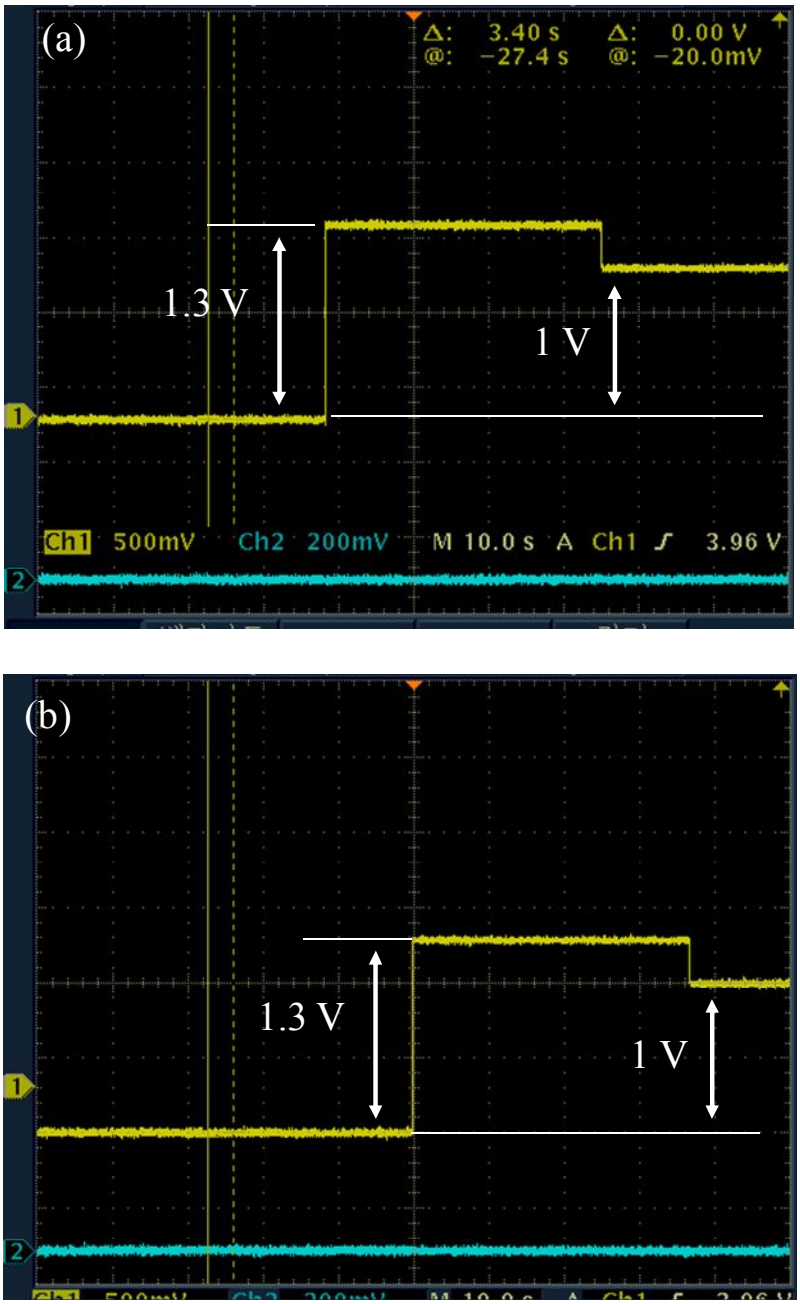


Fig. 4.2 Observations of (a) the bias voltage to reference electrode and (b) the bias voltage from the electrolyte, pH 7 solution. There is no drift effect.

The ISFET model has been researched in two main ways. The first is focused on development of physical chemical models [44-48] and the other is the model composed of electrical circuit by SPICE build-in model [45, 49-51]. The physical chemical models give the solutions related to the surface materials and fabrication conditions to reduce improvement. The physical chemical models give the solutions related to the surface materials and fabrication conditions for improvement [52]. These solutions, however, may be incompatible with the conventional CMOS technology.

4.2 Equivalent Circuit Model

In the view point of application of ISFET with ingrared circiut, the macro model is also needed. The basic electical model is introduced in Fig 4. 3 [45]. This model considers only electrostatic state. For the reason, there is no time dependency and that means that it cannot express drift. The improved model considering drift effect is illustrated in Fig 4. 4 [51]. However, the drift model is based on a physical method. For the reason, we propose the electrical model which explian the drift mechanidm to find a solution for drift effect and consist of electrical cicuit components. As mentioned about drift chatracteritic in chapter 4.1, at first we presume that the long time constant is related to the effect of hydrogen ion movement through oxide or Helmholtz layer (HL) [41, 51, 53]. In order to model this effect, we have set up a simple circuit as shown in Fig. 4. 5. This electrical circuit model can explian drift effects without other physical models.

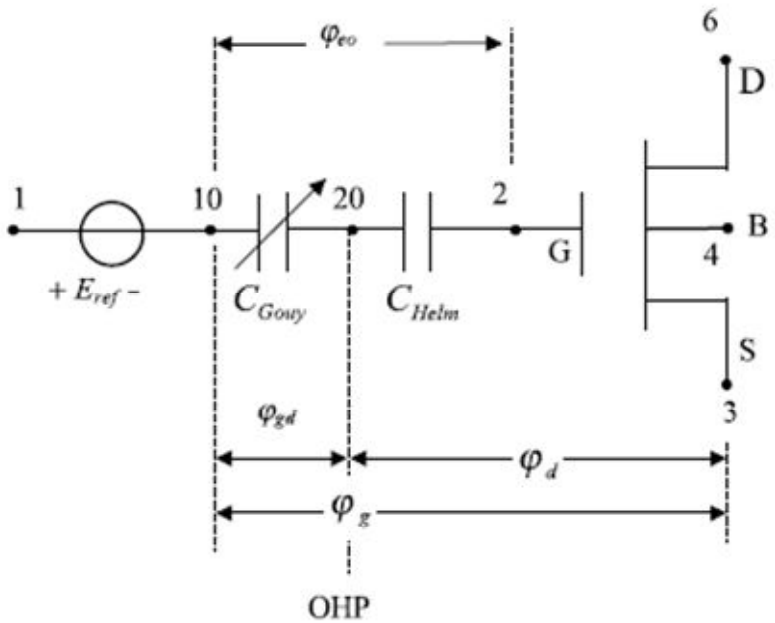


Fig. 4.3 Equivalent electric circuit (macromodel) of the ISFET corrsponding to Fig. 3. 2

(a) [45]. (R: reference electrode, D: drain, S: source, B: Bulk)

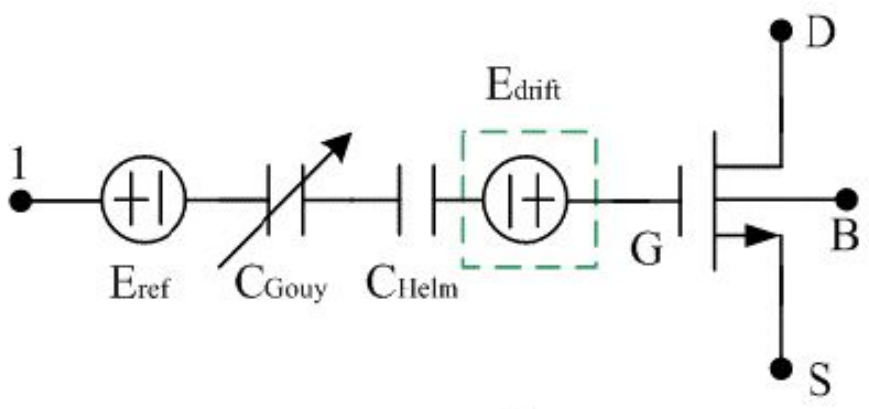


Fig. 4.4 Equivalent circuit of the ISFET including the drift effect [51].

In the electrical circuit model of Fig. 4. 5, R_1 represents the resistance of the electrolyte and the FET can be approximated as a capacitance, C_1 and C_2. C_2 is the capacitance by gate oxide with defects in which the hydrogen ions move relatively faster than that of pure oxides as shown in Fig. 4.4(d). C_1 is the capacitance of the pure oxide of gate in which the hydrogen ions move very slowly. R_2 represents the ion movement through the defective oxide. The low diffusion constant in oxide causes the bottleneck of the ion motions. The slow movement of hydrogen ions in the defective oxide is modeled as the parallel combination of a capacitance (C_2) and a large resistance (R_2).

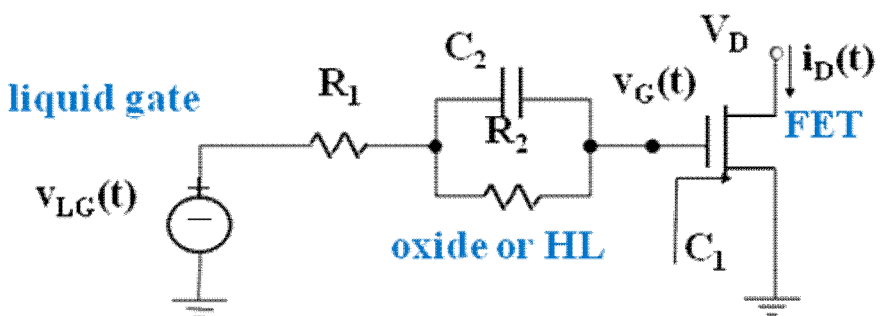


Fig. 4.5 A schematic model including drift effect. It is composed of electrical component. The pararell combination of R_2 and C_2 indicates the hydrogen ion movement near oxide to express the slow response.

It is noted that liquid gate bias ($v_{LG}(t)$) is applied as a unit step function. From the model, the liquid gate bias is the only voltage source and we need to consider the input

loop for the analysis of the response. According to Kirchhoff's law, we can get the two equations, Eq. (4.1) and (4.2) about liquid gate bias and current.

$$v_{LG}(t) = R_1 i + v_2 + \frac{1}{C_1}\int_0^t i dt' \tag{4.1}$$

$$i = C_2 \frac{dv_2}{dt} + \frac{v_2}{R_2} \tag{4.2}$$

As Eq. (4.2) is substituted into Eq. (4.1), the liquid gate bias is expressed by the circuit components, C_1, C_2, R_1, R_2 and the voltage across Helmoltz layer. The expreesion is given by

$$v_{LG}(t) = R_1 C_2 \frac{dv_2}{dt} + \frac{R_1}{R_2} v_2 + v_2 + \frac{C_2}{C_1} v_2 + \frac{1}{C_1 R_2}\int_0^t v_2 dt' \tag{4.3}$$

By using Laplace transform for $v_{LG}(t)=Vu(t)$, Eq. (4.3) is given by

$$\frac{V}{s} = R_1 C_2 s V_2 + \left[\frac{R_1}{R_2} + \frac{C_2}{C_1} + 1\right] V_2 + \frac{1}{C_1 R_2 s} V_2 \tag{4.4}$$

We can obtain the exact solution without much difficulty, but some approximation makes the solution much simpler. As the capacitance and resistance of drift term, (C_2, R_2) are much larger than that of rapid changing term, C_1 and R_2, the

effective gate bias volage of the gate node, v_G, can expressed by following equation.

$$V_G \cong \left[1 - \frac{C_2}{C_1 + C_2} e^{-(C_1+C_2)t/C_1C_2R_1} - \frac{C_1}{C_1 + C_2} e^{-t/(C_1+C_2)R_2}\right] Vu(t) \qquad (4.5)$$

The effective voltage to gate node is found. However, the voltage cannot be measured directly in the experiment. It is required to measure the drain current controlled by the gate voltage.

Fig. 4.5 shows the output characteristics to find the operation region of the device. The operation resion is in saturation mode ($V_{LG} = V_D = 1V$, $V_S = 0V$). Since we are measuring the drain current in the saturation mode ($v_G(t) - V_T < V_D$), the drain current is given by

$$i_D(t) = \begin{cases} \beta[v_G(t) - V_T]^2 / 2, & \text{for } v_G(t) - V_T > 0 \\ 0, & \text{for } v_G(t) - V_T \le 0 \end{cases}, \qquad (4.6)$$

where β and V_T represent the gain factor and threshold voltage of the FET, respectively. Thus, the drain current can be easily obtained by evaluating the FET gate voltage, $v_G(t)$.

The response of the voltage $v_G(t)$ to a step function input $v_{LG}(t) = V_{LG}\,u(t)$, where u(t) is the unit step function (u(t) = 1 for t > 0 and u(t) = 0 for t < 0), is given as

$$v_G(t) = \left[1 - A_S e^{-t/\tau_S} - A_L e^{-t/\tau_L}\right] V_{LG} u(t), \qquad (4.7)$$

where A_S and A_L are constants determined by the circuit parameters (R_1, R_2, C_1, and C_2). The exponentially decaying function with a long time constant (τ_L) is the cause of the current drift. As far as the slow drift of current is concerned, we can ignore the effect of the exponential function with a short time constant (τ_S) since it decays quickly. It will appear just like a part of the step function.

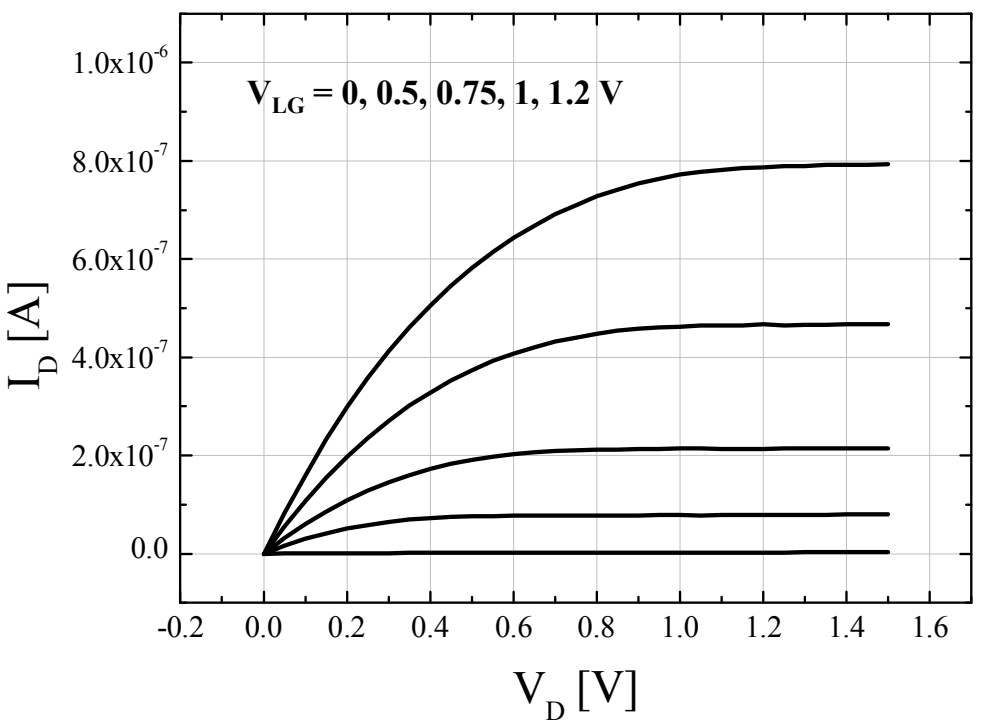


Fig. 4.6 Output characteristics to define operation mode for modeling.

(Measurement condition: V_S = 0 V, V_D = 1 V, V_{LG} = 1V)

Table. 4.1 Parameters for electrical circuit model. The key parameters are related to slow response since they cause drift phenomenon.

notation	compoenet	Reaction rate
C1	Gate node	**Fast response**
R1	Resistance of electrolyte	
C2	Hydrogen ion movement near oxide.	**Slow response**
R2		

Table. 4.2 Notations for simple expression and its physical measning of Eq. (4.7)

notation	components	physical meaning
τ_L	$(C_1 + C_2)R_2$	long time constant
τ_S	$C_1C_2R_1/(C_1 + C_2)$	short time constant
A_L	$\frac{C_2}{C_1+C_2}$	initial state for τ_L
A_S	$\frac{C_1}{C_1+C_2}$	initial state for τ_S

4.3 Drift Analysis by the Propsed Model.

Although the drift effect is caused by FET gate voltage, v_G, in Eq. (4.7), it cannot be measured directly. For the reason, the drain current is calculated by the proposed model and compared with measured data as shown in Fig. 4. 7. It is verified that

the model consisting of only electrical circuit compoenet reflects the drift effect related to hydrogen ion reaction. The relation between effective gate bias (v_G) and drain current (I_D) is explained in Appendix A.

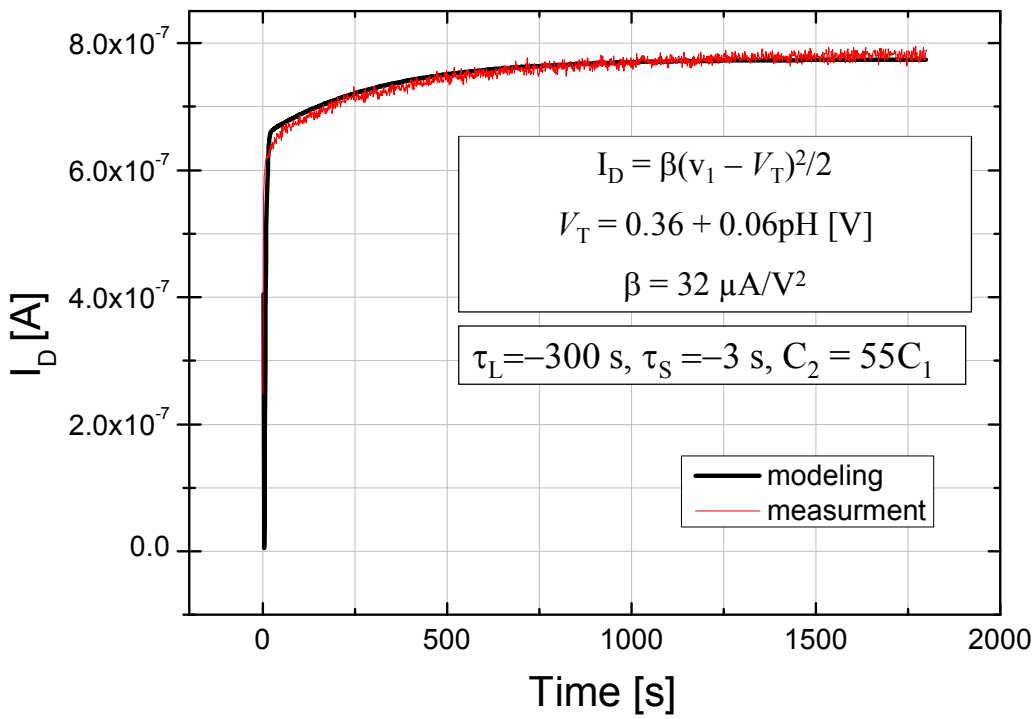


Fig. 4.7 Comparison of measured and calculated currents.

Chapter 5

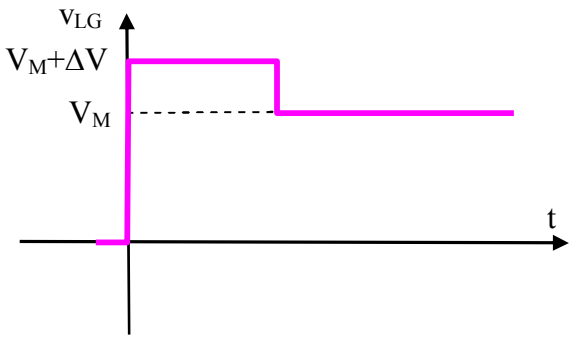
New Operation Scheme : 2-step Bias Method

5.1 Operation Principle

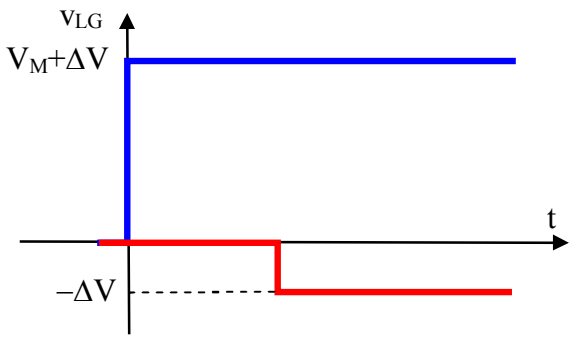
Based on the fact that an exponential function with the same time constant has self-similarity, we have devised a method to compensate the exponential function with the long time constant (τ_L) during the main measurement. It is a 2-step bias voltage method that employs an increased V_P (= V_M + ΔV) before the main measurement as shown in Fig. 5.1(a). As shown in Fig. 5.1(b), the 2-step bias voltage input can be decomposed into two components: the leading step function with the step size of (V_M + ΔV) and the following step function with the step size of $-\Delta V$.

The response function to a component step function was already obtained in the previous chapter. Since the linear system is assumed, the each unit step makes its own drift effect. We can easily find the component response functions as shown in Fig. 5.1(c). The next step is to compose the total response function, using the superposition principle. Fig. 5.1(d) shows that the response function to the following step input function can

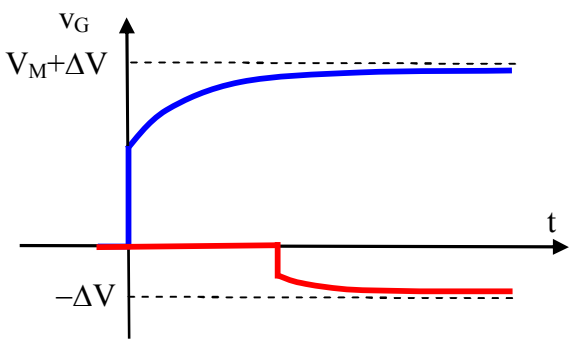
perfectly compensate the drift generated by the leading step input function.



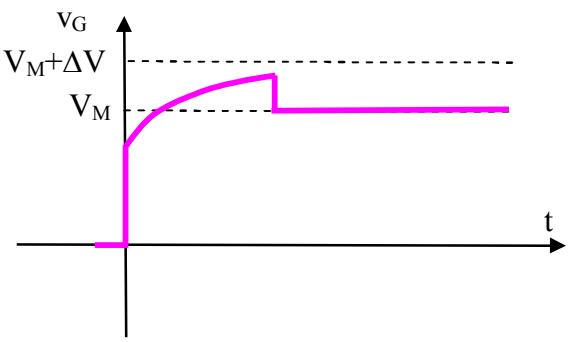
(a)



(b)



(c)



(d)

Fig. 5.1 Compensation principle: (a) 2-step bias function composed as the superposition of the two step functions, (b) decomposed input step functions (blue line: leading step function, red line: following step function), (c) decomposed response functions(blue line: response to the leading step function, red line: response to the following step function), and (d) response function to the 2-step bias input

The two drift effects which have opposite directions to each other are compensated. After comepensation, the gate bias voltage will be constant without change. Thus, the drain current will also be constant. This mechanism is applied to the fabricated devices, and the measurement is conducted.

5.2 Drift Compensation by a 2-step Bias Method.

At first, increased gate bias, $V_{LG} = V_P$, is applied as shown in the inset of Fig. 5. 2. At time T_P, we add a counter step function with the step of ΔV such that $A_L \Delta V - A_L (V_M + \Delta V) e^{-T_P/\tau_L} = 0$ (from Eq. (4.7)), eliminating the exponential function with τ_L during the main measurement ($t > T_P$). For the pre-measurement time, $t_P < T_P$, we will have under-compensation, while, for $t_P > T_P$, over-compensation.

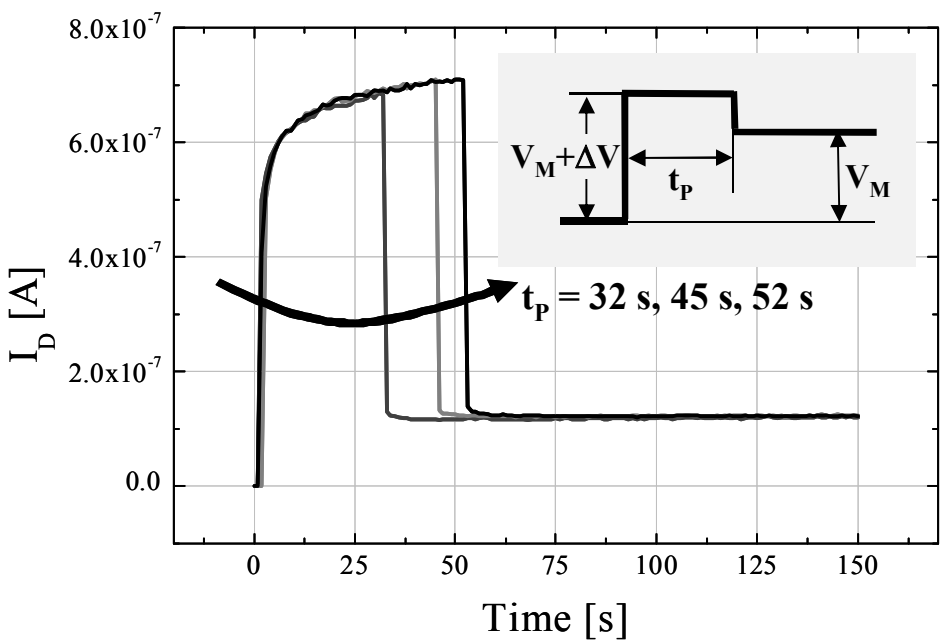


Fig. 5.2 Transient characteristic in pH 7 solution with 2-step bias measurement results for various pre-measurement time, t_P.

In Fig. 5.2 , we can confirm that the value of T_P is 45 s for the device under

measurement. In the case of under-compensation, t_P = 32s, the currnet is slightly increaed after conter step. Under over-compensation condition, t_P = 52s, the current is slightly decreased in same measurement bias. This results are consistent the the calcultated drain current through the proposed electrical circuit model.

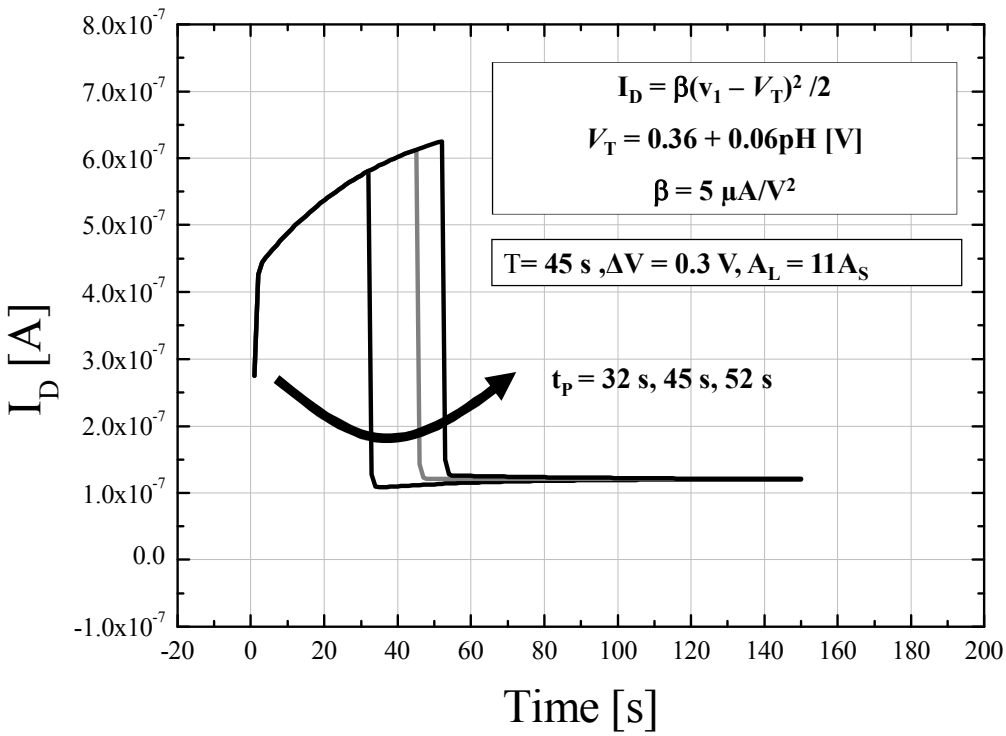


Fig. 5.3 Calculated drain current with 2-step bias measurement for various t_P.

In measurements of devices with various widths, we have found that T_p is independent of device geometry. The reason behind this surprising observation is that T_p is proportional to the product of C_2 and R_2 ($T_P \propto \tau_L \approx C_2 R_2$). C_2 is proportional to the

area while R_2 is inversely proportional to the area. Since C_2 and R_2 share the same area (i.e., the gate area of the device), their product, C_2R_2, is independent of the area. The area independence of T_P is really beneficial to our measurement scheme, since we don't have to measure T_P experimentally for each device. The experiement also proves the different width has same T_P as shown in Fig 5.2 and 5.3. For the reason, this method can be appllied to compensate the drift effect in all fabricated devices.

Since T_P is free from the device geometry, it is dependent on the interaction between the surface of the gate insulator and the surrounded electrolyte. By changing gate insulator or electrolyte, the changed drift effect is observed through finding T_P. The dependency on salt concentration is analyzed through the 2-step bias method. The buffer solution has other ions such as OH^-, K^+ and HPO^{3-}. Especially, the KOH is an etchant of silicon. The effects of the ions without hydrogen can be observed and the result is shown in Fig. 5.4. It shows no relation to the drift effect. It also supports the assumption that the drift is caused by hydrogen ions.

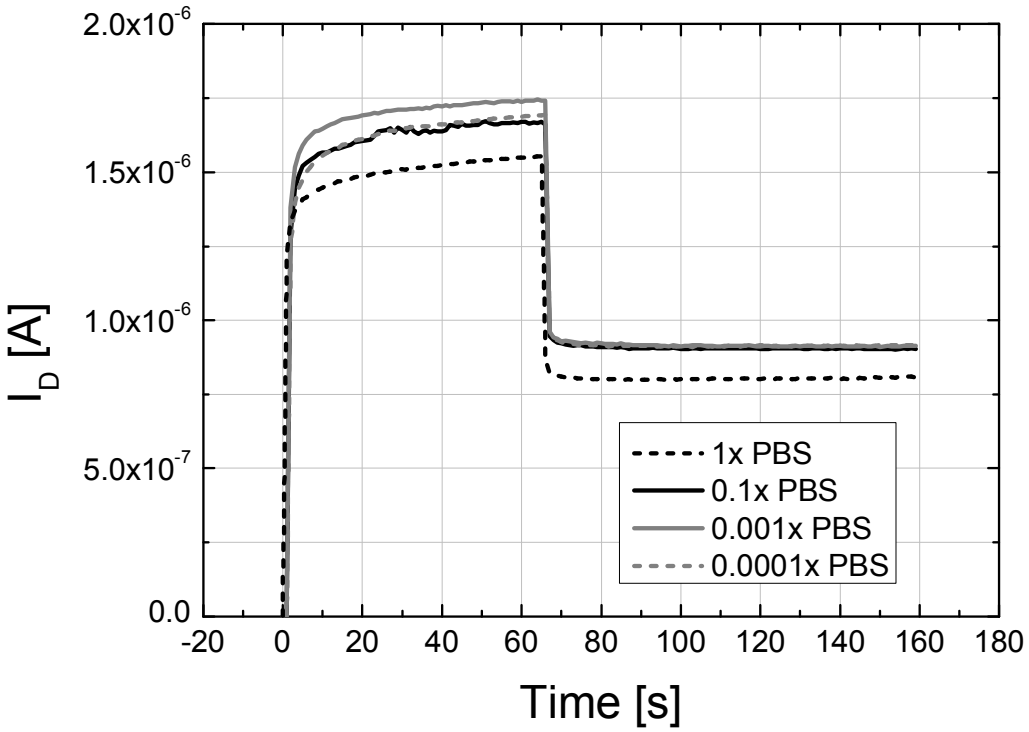


Fig. 5.4 Transient charateristics with various consentration of the buffer solutions.

As shown in Fig. 5.5, we can obtain almost perfect compensation for various pH levels. Since the drain current is given by Eq. (4.6), the perfectly compensated $v_G(t)$ results in an almost constant current during the main measurement. Figure 5.6 shows the measured current with 45s pre-measrement time for various pH levels in random sequence. We can confirm that measured current is almost constant during each measurement and quite reproducible throughout the entire measurement sequence.

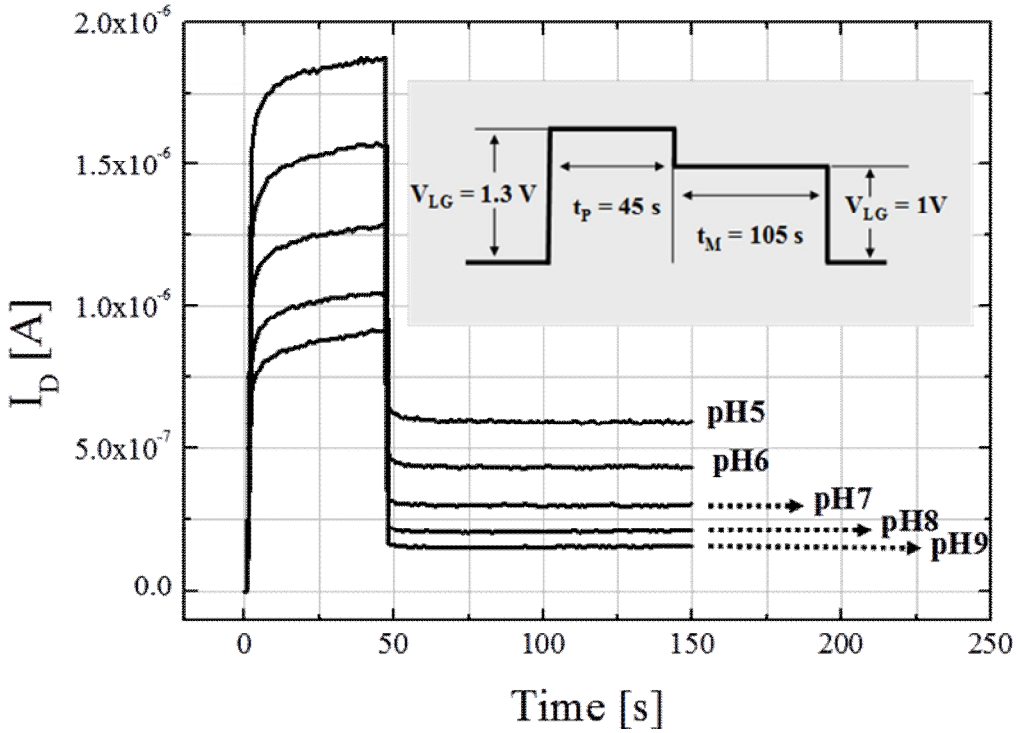


Fig. 5.5 Transient characteristics with 2-step bias voltage measurement for one measurement The pre-measurement time is 45 s (V_D = 1 V, V_{LG} = 1.3 V). The total sensing time for pH level is 105 s at each measurement (V_D = 1 V, V_{LG} = 1 V).

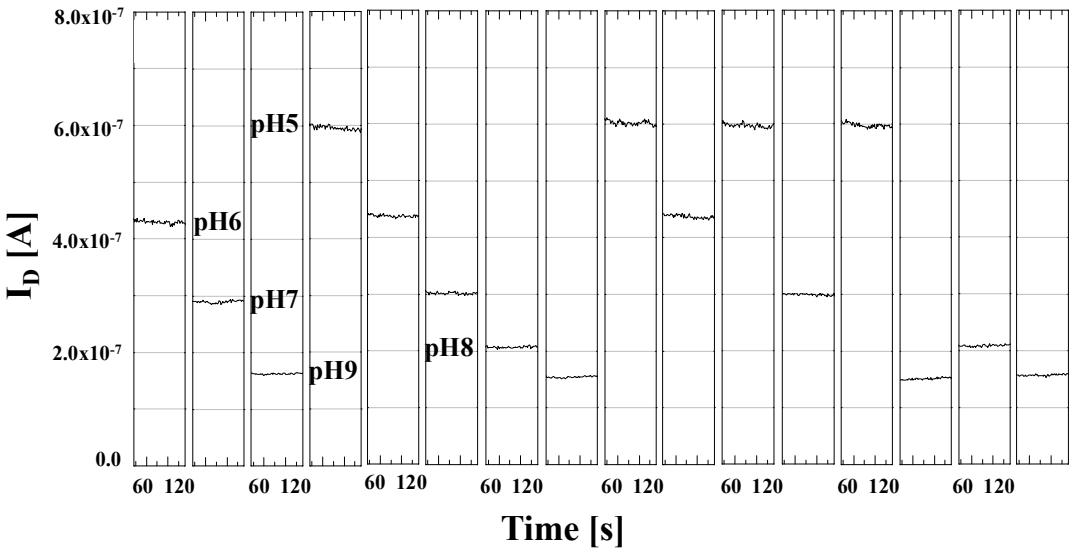


Fig. 5.6 Transient characteristics with 2-step bias voltage measurement for multiple measurements with random pH values. The pre-measurement time is 45 s (V_D = 1 V, V_{LG} = 1.3 V). The total sensing time for pH level is 105 s at each measurement (V_D = 1 V, V_{LG} = 1 V), and a part of it (60 s ~ 120 s).(W = 50 nm, L = 2 μm)

Chapter 6

Conclusion

Owing to its scalability and its low power requirement, complementary metal-oxide-semiconductor (CMOS) processes are dominant in modern integrated circuit manufacturing. For the reason, silicon nanowire field-effect transistor (SiNW FET) sensor is most applicable to scaling requirement because of its sensitivity and its compatibility with CMOS processes. Considering integraion with MOSFET, the equipments and conditions for the sensor fabrication have to be the same as those of the conventional MOSFET.

For the reason, we designed one of the simplest structures. The process flow of SiNW FET sensors which we fabricated is almost the same as that of MOSFETs. For this reason, except for the opening of sensing area, all the other process steps were conducted simultaneously. Most electrical characteristics of the fabricated SiNW FET sensor have been demonstated except time dependent measurement under the conditions with five different pH. In addition, the integration SiNW FET, such as complementary SiNW ISFET and SiNW-MOSFET hybrid ISFET, has been demonstrated. This indicates the proposed fabrication method is effective for integration with MOSFETs.

However, the reproducibility of the fabricated sensor is debatable. After detecting

pH level for 50 s, the solution is changed to that with other pH level. The variation of the output currents is quite large. Most output values are different for repeated detection at the same pH level. The main reason of the poor reproducibility is the drift effect. To solve the problem, we have proposed an electrical model which is based on the drift mechanidm and consists of electrical circuit components. The effect of hydrogen ion movement through oxide or Helmholtz layer is expressed by the long time constant

From the modeling, it is proven mathmatically that the drift effect can be removed by compensation. Based on the fact that an exponential function with the same time constant has self-similarity, we have devised a method to compensate the two different drift effects each other during the main measurement. Almost perfect compensation for various pH levels can be obtained. Finally, we can confirm that measured current is almost constant during each measurement and quite reproducible throughout the entire measurement sequence. Figure 6.1 shows the reduced time through the proposed measurment scheme. Differently from unit-step bias, 2-step bias method requires 100 s for reproducible measurement.

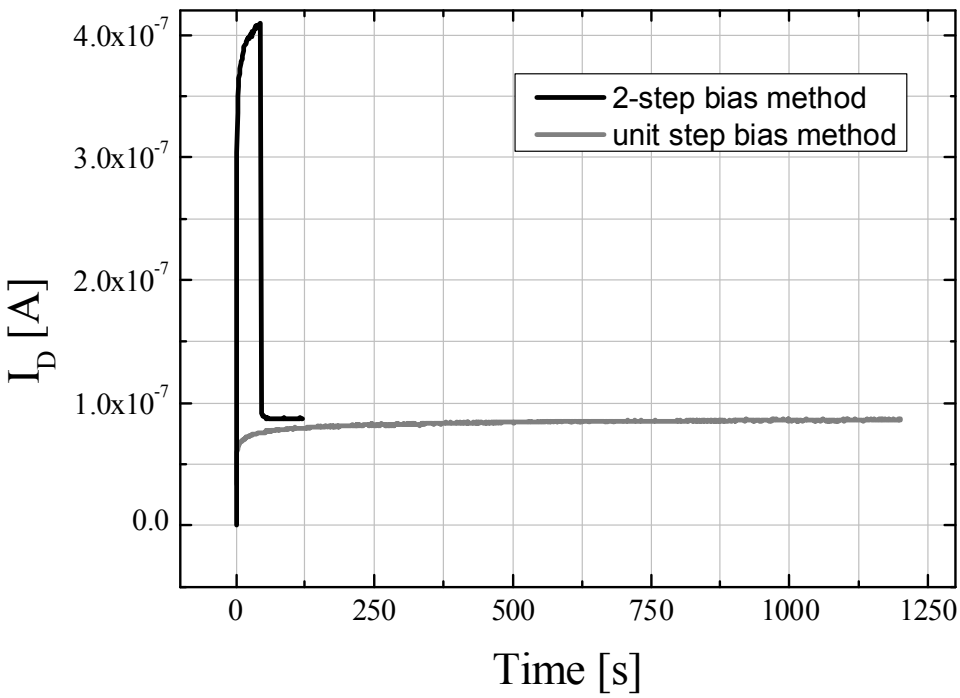


Fig. 6.1 Comparison of measurement time by unit step bias method and 2-step bias method. Different from unit-step bias, 2-step bias method requires 100 s for reproducible measurement.

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Myers, J. F. Davidson, A. Branting, J. R. Nobile, B. P. Puc, D. Light, T. A. Clark, M. Huber, J. T. Branciforte, I. B. Stoner, S. E. Cawley, M. Lyons, Y. Fu, N. Homer, M. Sedova, X. Miao, B. Reed, J. Sabina, E. Feierstein, M. Schorn, M. Alanjary, E. Dimalanta, D. Dressman, R. Kasinskas, T. Sokolsky, J. A. Fidanza, E. Namsaraev, K. J. McKernan, A.Williams, G. Thomas Roth, and J. Bustillo, "An integrated semiconductor device enabling non-optical genome sequencing", *Nature* 475, 348-352, 2011

Appendix A.

A1. Relationship between Effective Gate Bias Voltage and Drain Current in the pH detector.

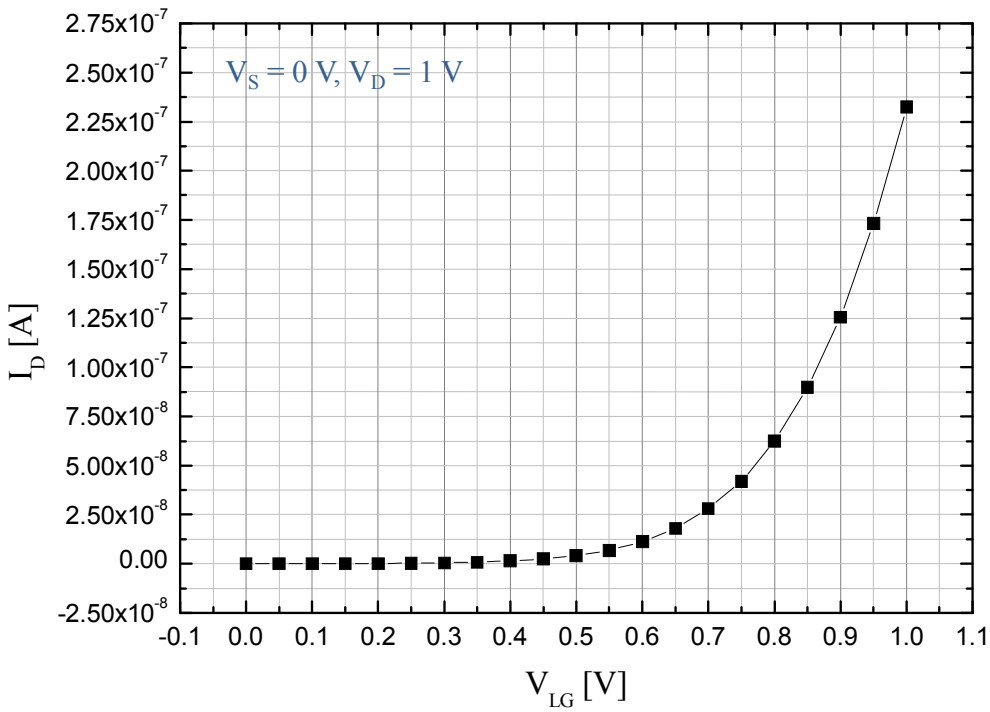

Fig. A.1 Transfer characteristic with long time integration time at each step (T_i ~ 15 s).

To find the relationship between the drain current and the gate bias voltage, the measurment is conducted. When the integration time is 0.16 ms, the transfer

chatacteristics cannot reflect the precise drain current and the value changes as the time goes on since it needs more time. However, long time integration provide precise aproximated current mapping with V_G. The transient chacteristic of the drain current as shown in Fig. A. 2 can be converted to the gate bias volatage through the transfer curve as shown in Fig. A. 1. Fig A. 3 shows the converted result and it helps to explain the drift effect more directly since it shows the gate bias change by the drift effect.

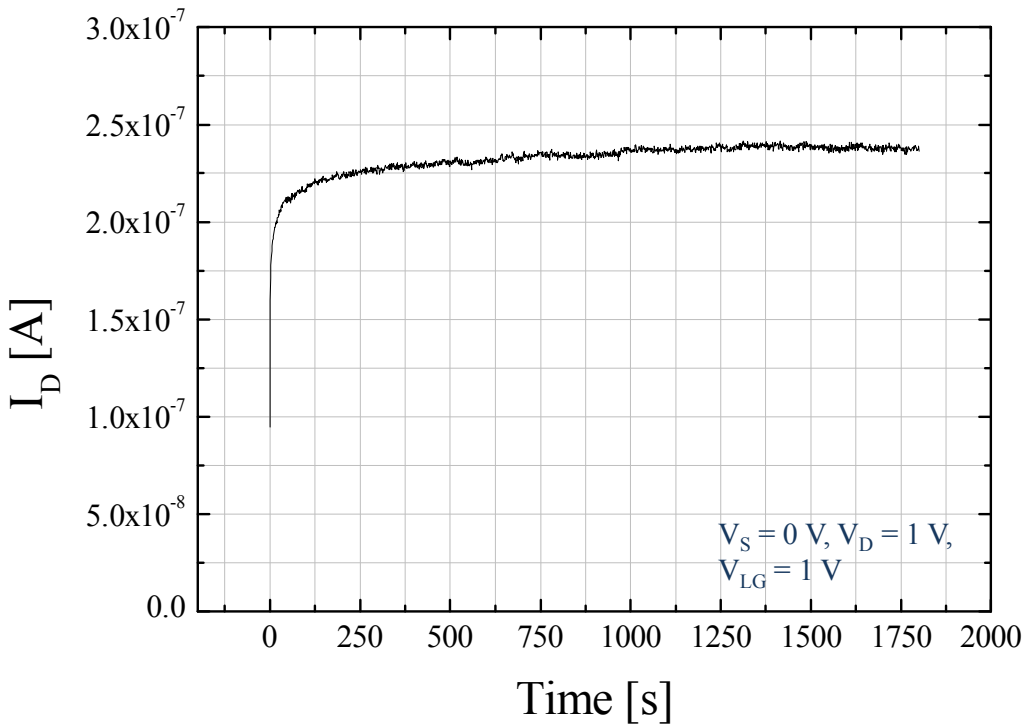

Fig. A.2 Transient characteristics of the drain current.

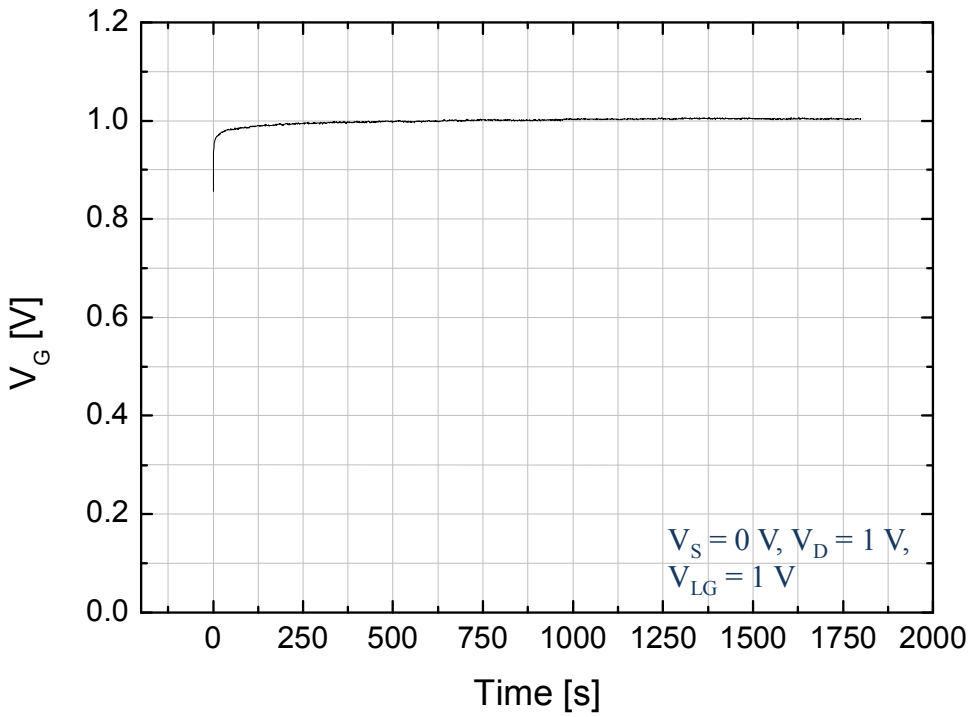

Fig. A.2 Transient characteristics with converted effective gate bias voltage instead of the drain current.

Appendix B.

B1. Transfer Charateristics of p-channel FET without 3-APTES

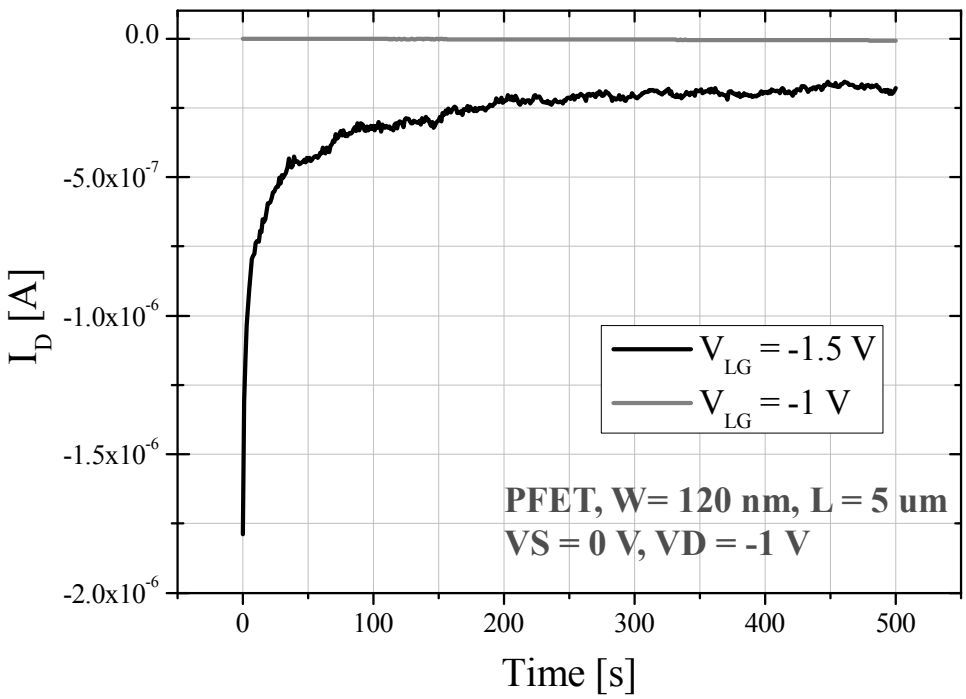

Fig. B.1 Transient characteristics of p-channel FET without 3-APTES in pH 7 solution.

B. 2. Transfer Charateristics of p-channel FET with 3-APTES

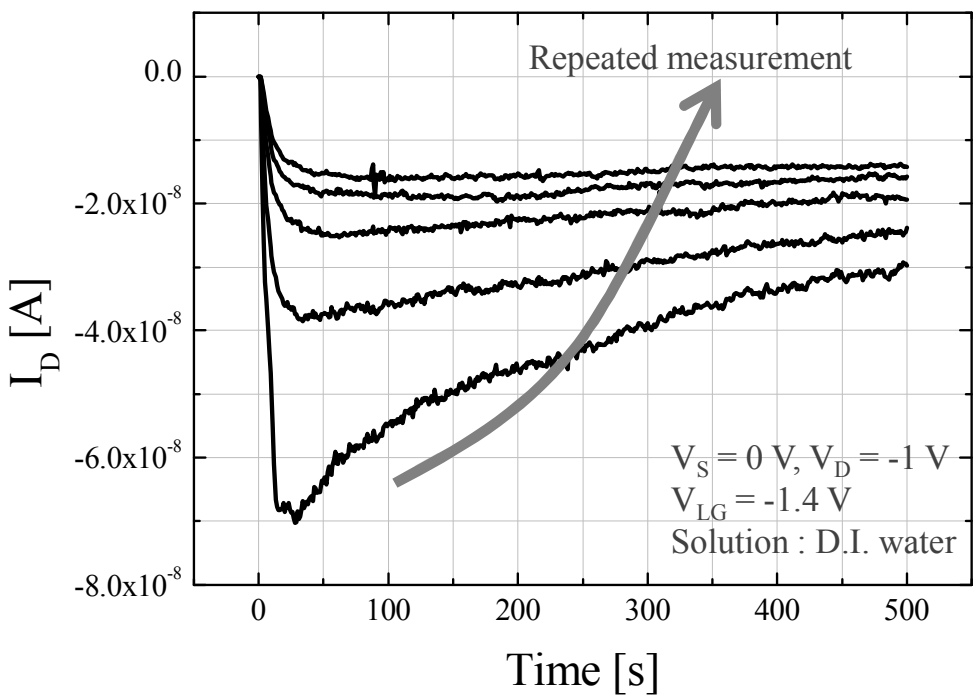

Fig. B.2 Transient characteristics of p-channel FET with 3-APTES in D.I. water.

Appendix C.

C. 1. Timer Switch Circuit for 2-step bias measuremnt.

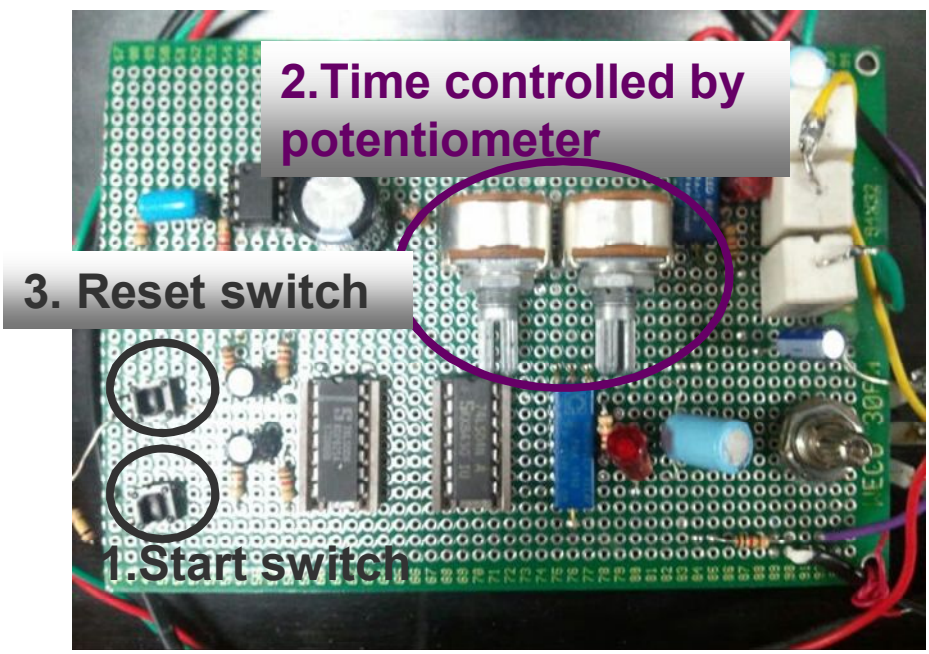

Fig. C.1 Timer switch circuit for 2-strp bias measurement. The potentiometer control the pre-measurement time by changing RC delay.

Appendix D.

D. 1. Transfer Chracteristics with Resistive Path.

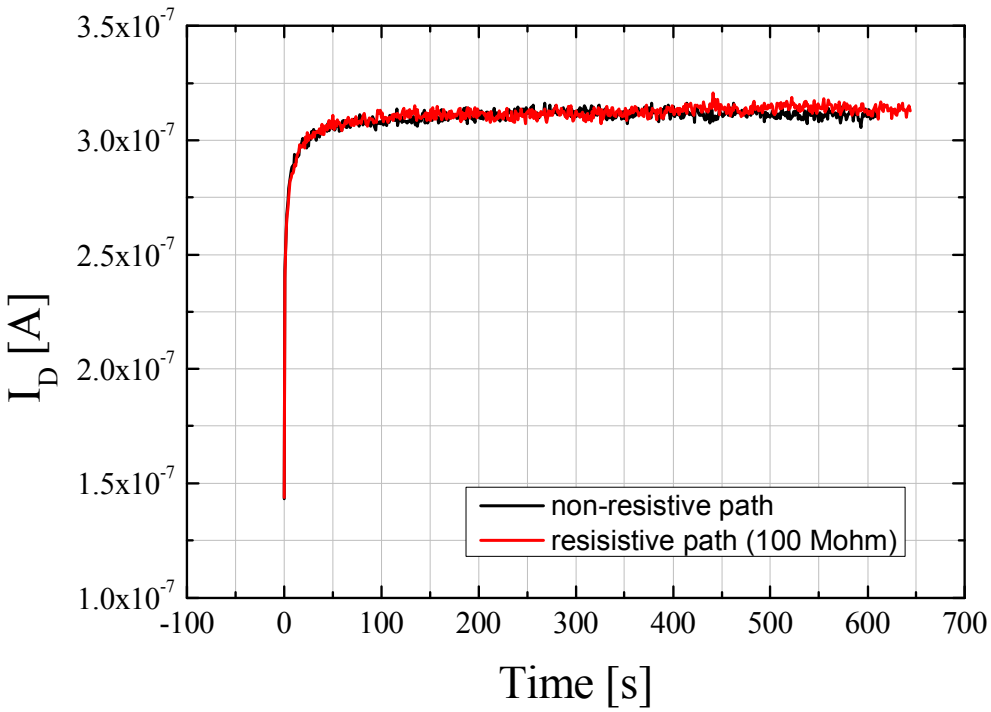

Fig. D.1 The rsistive path, 100 Mohm, is connected with second electrode grounded to remove floating charge in the electrolyte. However, they shows same results. This suggests there is no floating charge when using the reference electrode.

초 록

최근 나노 크기를 가지는 물질들의 공정 기술이 발전함에 따라, 이와 관련하여 의공학 소자들에, 특히 센서, 많은 연구가 이루어졌다. 이는 DNA, 단백질, 그리고 바이러스와 같은 생물학적인 개체들의 크기가 나노미터 단위의 크기와 비슷하기 때문이다. 형광 물질의 labeling과 빛을 이용한 탐지 기술을 이용한 화학적인 방법을 이용한 센서들이 널리 사용되고 있다. 하지만, 이 기술은 많은 문제점들을 가지고 있는데, 결과 분석과 샘플 준비에 시간이 오래 걸리고 가격이 비싼 것이 가장 큰 문제이다. 이런 이유로, labeling이 필요 없는 실시간 측정이 가능한 나노선 FET 센서가 유망한 소자로 떠올랐다.

기본적으로 SiNW FET는 CMOS 산업에서 short channel effect를 막기 위해 연구되었는데, 이 구조를 센서에 적용 시 높은 감도, free-labeling 그리고 실시간 측정이 가능하다. 게다가 SiNW FET 센서는 CMOS 기술과 호환성이 좋기 때문에 SjNW FET와 CMOS의 집적화로 고성능의 센서 시스템을 구현하는 것이 가능하다. 이런 이유로, top-down 공정 방법의 SiNWFET 센서를 제작되고 있지만, 실제 제작된 센서가 반복 측정 시 재현성을 보이지 못하는 것은 계속 문제가 되고 있다.

본 논문에서는, SiNW FET 센서와 MOSFET 소자를 동시에 제작할 수 있는 방법을 제안 하였고, 기존의 연구에서 보이지 않았던, 2가지 소자들을

실제로 집적하여 제작을 하였다. SiNW FET가 pH 용액에서 실시간 측정 시 보이는 drift 특성을 보이며 반복 측정 시 나타나는 불안정한 동작의 원인을 밝혔다. 이는 안정화 되기 위해 15분 정도의 시간이 필요하기 때문인데, 이는 실시간 측정이 불가능 함을 의미한다. 이 문제를 해결하기 위해, 모델링을 통하여 drift특성의 원인을 파악하고, 2가지 전압을 사용하는 새로운 측정 방법을 제안 하였다. 실제 측정 전의 pre-measurement 전압을 통해 전류의 saturation 속도를 증가시키는 방식이다. 이를 이용하여 총 필요 시간이 100초 이내로 실시간 측정이 가능할 수 있는 방법을 제시하였다.

주요어: SiNW FET 센서, pH 센서, 실시간 측정, 반복 특성, 2중 전압 측정, drift 특성, 등가 회로

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