M.S. THESIS

Analysis of nano-scale PMOSFET degradation under GIDL stress conditions

GIDL 스트레스 조건 하에서 나노 크기
PMOSFET 열화 분석

BY

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이 논문을 공학석사 학위논문으로 제출함

2017 년 8 월

서울대학교 대학원

전기정보공학부

조 수 앙

조수앙의 공학석사 학위논문을 인준함

2017 년 8 월

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ABSTRACT

The device degradation under gate-induced drain leakage (GIDL) mode stress is studied in nano-scale *p*-MOSFET for DRAM peripheral circuit. In order to discuss the degradation mechanism in *p*-MOSFET, the GIDL current and the other electrical parameters of target *p*-MOSFET are measured before and after high bias stress with different stress times. 2D TCAD simulation was performed using SENTAURUS^{TM} to know the internal physics of the *p*-MOSFET fabricated on the silicon substrate using the conventional CMOS process. With an intensive simulation, the gate or drain bias dependencies of the drain current before and after GIDL stresses of target device are fitted to the measurement results. Because band-to-band tunneling (BTBT) and trap-assisted-tunneling (TAT) are the main mechanisms for generating GIDL currents, the appropriate physical model was selected in the simulation set and modified for the tunneling mechanism.

According to the stress time, the changes of GIDL current and the on-state drain current before and after stress can be divided into two stages. The degradation mechanisms under GIDL stress are analyzed by considering TAT, BTBT, channel length modulation (CLM), and parasitic resistance degradation. It is found that the generation of interface states and the trapping of different types' charges cause the degradation of *p*-MOSFET under GIDL stress. The simulation

shows clearly the relationship between charge density and stress time, interface trap density and stress time.

Keywords: GIDL stress, TAT, BTBT, CLM, device degradation, activation energy, interface trap, oxide charge

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CONTENTS

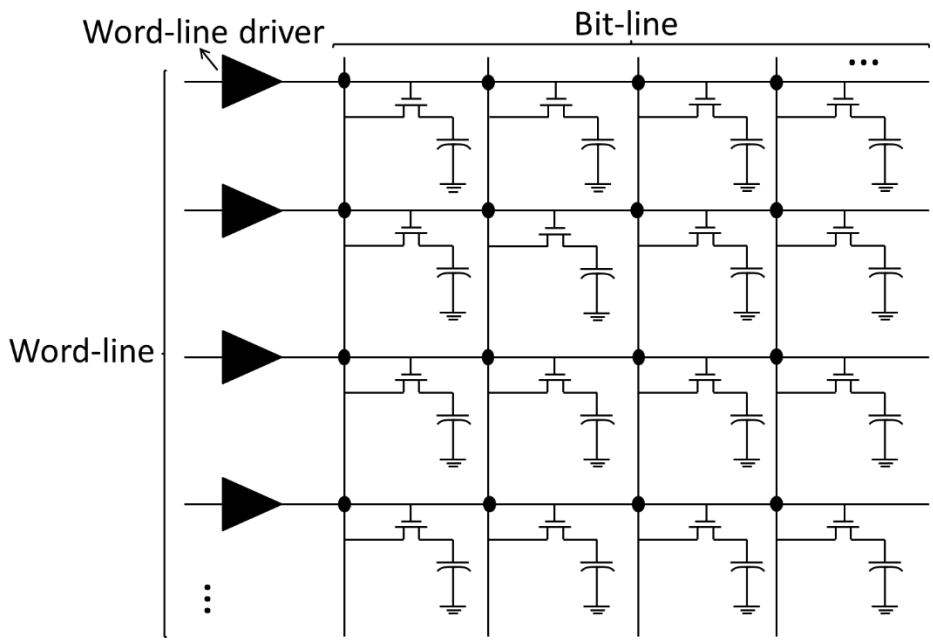
1. Introduction

1.1. Background and motivation

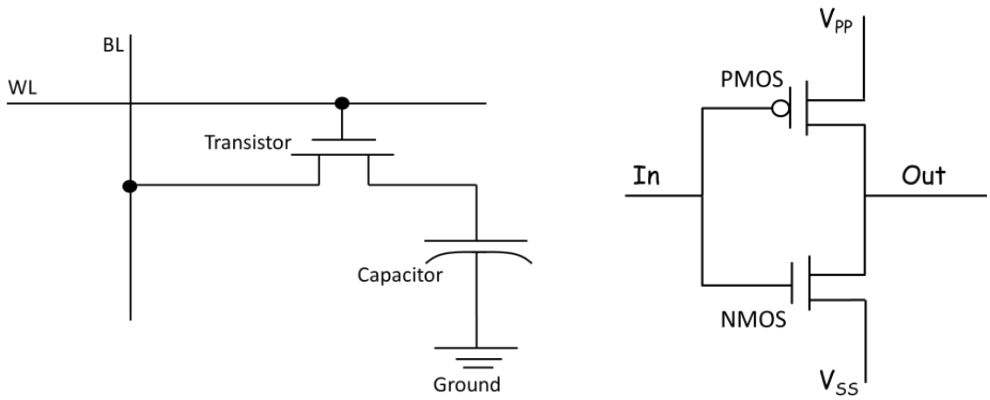
Recently CMOS technology has been scaled down to sub-50-nm to improve performances and densities of integrated circuits. But in the highly scaled MOSFETs, the leakage current increases due to the increased electric field, and the suppression of this current is an essential factor to reduce the power consumption of the circuits. Figure 1.1.1 shows a part of dynamic random access memory (DRAM) circuit with 1-transistor, 1-capacitor (1T1C) cell structure. Word lines with higher voltage (V_{pp}) than the normal operation voltage (V_{dd}) drive the gate nodes of transistors in every memory cell. The word-line driver in every row consists of a *p*-MOSFET and an *n*-MOSFET.

In fact, the CMOS word-line driver operates as an inverter. When a high voltage is inputted into CMOS word-line driver, the *p*-MOSFET in its off-state, *n*-MOSFET is on-state, and a low-level signal is inputted to

DRAM circuit finally. Namely, all the transistors in the corresponding row are off-state when a high voltage is inputted to corresponding CMOS word-line driver, and are on-state when a low voltage is inputted. At most time, nearly all the transistors are off-state, so it means that for most of the time, a high off-state bias is applied to the *p*-MOSFETs in the CMOS word-line driver.



(a)



(b) (c)

Fig. 1.1.1 (a) A part of dynamic random access memory (DRAM) circuit, (b) 1-transistor, 1-capacitor (1T1C) cell structure, (c) Word-line driver

Tiwari Vishal A. in [1] has explained that the MOSFET has four main leakage currents: gate leakage current, sub-threshold leakage current, gate induced drain leakage (GIDL) current, and junction leakage current showed in Fig. 1.1.2. The leakage current at high drain bias in off-state consists of GIDL current, negligible other leakage currents (GIDL mode). In the periphery circuit of the DRAM, many *p*-MOSFETs have a very small physical distance between the drain and the gate for the area efficiency. Since they are turned off in the GIDL mode, reducing the GIDL current in

these *p*-MOSFETs can play an important role in reducing power consumption of the entire circuit. In addition, the GIDL current in the *n*/*p*-MOSFETs can be greatly increased due to the hot carrier generation under GIDL mode stress. This increase in GIDL current can be observed simultaneously with degradation of other electrical parameters [2], [3].

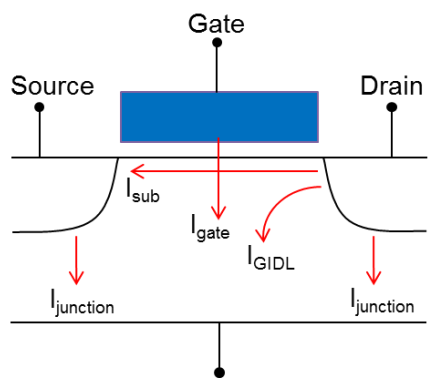


Fig. 1.1.2 Four main leakage currents in *p*-MOSFET

In this work, the characteristics of the GIDL current and the other electrical parameters of the *p*-MOSFET used in the peripheral circuits of the DRAM and its degradation under the GIDL mode stress were measured. And the mechanisms of degradation phenomena are analyzed, through in-depth analysis such as parasitic resistance extraction [3-6] and temperature-

dependent measurement [7], [8]. These results are verified through referring to previous studies on GIDL phenomena. Phonon-assisted band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT) are the main mechanisms of GIDL current generation [9], [10]. Note that the device in this thesis has no LDD structure, which is different from the devices in the literatures.

For ensuring the accuracy of the results and doing further analysis, the device is simulated using SENTAURUS^{TM}. In the simulation, the suitable tunneling models [11][12] were selected by fitting the simulated drain current with the gate or drain bias before and after GIDL stresses to the measurement results of the target device.

1.2. Gate induced drain leakage current

Figure 1.2.1 shows the terminal bias of a *p*-MOSFET under GIDL stress conditions in this work. In order to decrease the sub-threshold leakage current, the voltage difference between source and drain (V_{ds}) is -0.15 V.

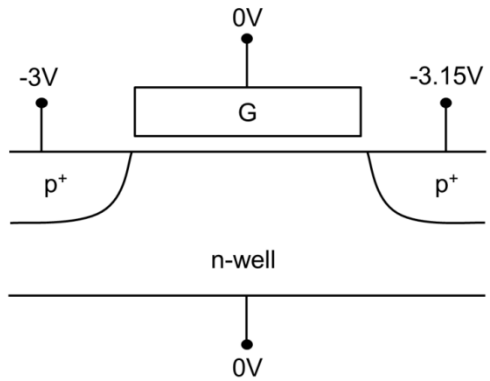


Fig. 1.2.1 Bias condition of a *p*-MOSFET under GIDL stress in this work

By applying a negative bias to the p^+ drain at a given gate bias of 0 V, the p^+ region near the interface between the drain and the insulator butted to the gate is depleted under the stress mode. Fig. 1.2.2 shows the electron-hole pairs generated by the tunneling process in which the electrons in the valence band tunnel to the conduction band. Electrons flown to the substrate and holes moved to the drain as GIDL current [8]. These tunneling phenomena include two important mechanisms. One is trap-assisted tunneling (TAT), the other is band-to-band tunneling (BTBT).

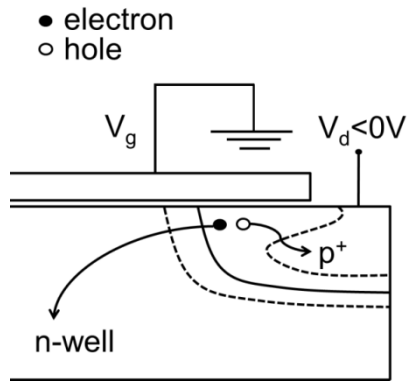


Fig. 1.2.2 Schematic cross section of PMOS drain region in GIDL mode

Trap-assisted tunneling (TAT) occurs in a low V_{dg} condition due to interface traps. Electrons from the valence band, through the thermionic emission, are trapped at interface states first and then tunnel to the conduction band. TAT is a kind of two-step tunneling [1]. Figure 1.2.3 shows the way of TAT with interface traps. The GIDL current in the low electric field is mainly attributed to TAT.

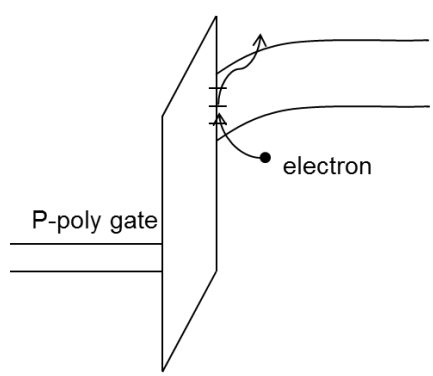


Fig. 1.2.3 Band diagram of PMOS drain region to explain TAT

Band-to-band tunneling (BTBT) occurs in a high V_{dg} condition. The high V_{dg} means there is a high electrical field to result in more serious band bending in the drain region, thus the electrons from valence band can tunnel to the conduction band directly. According to [9], GIDL current in leakage current can be explained in the following equation:

$$I = AVF^{1.5}\exp(-B/F) \tag{1}$$

where A is constant, B and F are shown separately:

$$B = 4\sqrt{2m_r}\sqrt[3]{E_g}/3q\hbar \tag{2}$$

$$F = (V_{DG} - 1.2)/3T_{OX} \tag{3}$$

where $\hbar$ is Plank's constant, m_r is effective mass of carrier and E_g is band gap energy. Figure 1.2.4 depicts the way of BTBT. The GIDL current in high electric field is mainly attributed to BTBT.

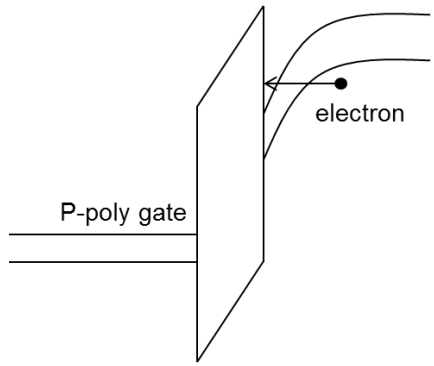


Fig. 1.2.4 Band diagram of PMOS drain region to explain BTBT

1.3. Thesis organization

In order to study the degradation mechanism of target *p*-MOSFET under GIDL stress, in section II, the GIDL currents and the other electrical parameters are compared before and after GIDL stress through measurement result. By analyzing the activation energy of GIDL current, body current based on CLM, and drain resistance degradation under GIDL stress, the degradation mechanisms during GIDL stress are elaborated. In section III, the simulation approach is presented and the results from different TAT and BTBT tunneling models are compared in TACD simulation. By fitting the simulated drain current to the measured drain current of the target device depending on the gate or drain bias under GIDL bias condition, the effect of

tunneling models on GIDL current is analyzed. It is shown that the activation energy has different behavior at different V_{dg}s, and the polarity and density of the trapped charges are changed as stress time increases.

2. Measurement of *p*-MOSFET after GIDL stress and the degradation mechanism discussion

2.1. High bias stress measurement

Normally, the lifetime of semiconductor device is about two to five years. For the verification of device reliability, acceleration test is often used, which is a kind of accelerated speed test for shortening the test period by adopting a high stress bias and/or high temperature. Agilent B1500A as a semiconductor analyzer was used in this measurement. The data obtained through the acceleration test are analyzed using Arrhenius equation [13] as given in the following equation:

$$t(T) = A\exp(-E_a/kT) \tag{4}$$

where A is the correlation coefficient and E_a is the activation energy, k is the Boltzmann constant, and T is the temperature. The activation energy will be discussed later.

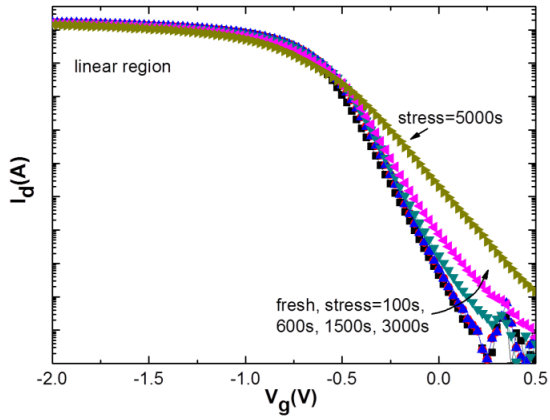
The variant of (4) is shown in (5):

$$t(V) = B\exp(-\gamma \mathrm{V}) \tag{5}$$

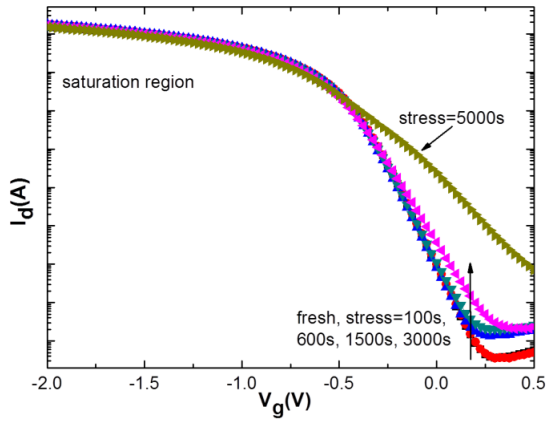
where B is constant, γ is voltage factor. From the results obtained by applying a high stress bias, it is possible to calculate the lifetime of the device under normal bias operation. The acceleration factor AF_{V} (6) can be obtained through (5).

$$AF_V = t(V_0)/t(V_1) = \exp\big(\gamma(\mathrm{V}_1 - \mathrm{V}_0)\big) \tag{6}$$

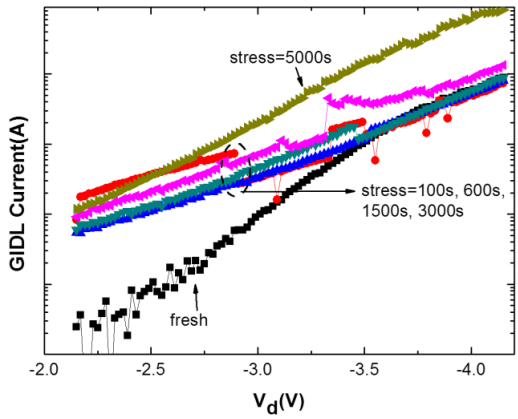
The biases for *p*-MOSFET at normal off-state are V_{d} = -3.15 V and V_{s} = -3 V, V_{g} = V_{b} =0 V. To accelerate the test, V_{d} = -5.15 V and V_{s} = -5 V are used as high GIDL stress biases. The V_{g} - I_{d} and V_{d} - I_{d} curves are measured at room temperature (300K) after the stress with different stress times, significant degradation of GIDL current and drain current is observed in Fig. 2.1.1.


linear region
stress=5000s
fresh, stress=100s,
600s, 1500s, 3000s
I_d(A)
V_g(V)
-2.0
-1.5
-1.0
-0.5
0.0
0.5

(a)


saturation region
stress=5000s
fresh, stress=100s,
600s, 1500s, 3000s
I_d(A)
V_g(V)
-2.0
-1.5
-1.0
-0.5
0.0
0.5

(b)



(c)

Fig. 2.1.1 *I-V* characteristics of PMOS device as a parameter of stress time after applying bias stress using V_d /V_s = -5.15 / -5 V. (a) V_g-V_d curves at V_d = -3.15 V (saturation region). (b) V_g-V_d curves at V_d = -0.1 V (linear region). (c) GIDL current versus V_{dg} at V_g = 0 V.

2.2.Device parameter after GIDL stress

In order to clarify how the GIDL current and the other electrical parameters change, the percentage of degradation is investigated with stress time. Firstly, the V_{th} (threshold voltage extracted by g_{m_max} method), I_{dlin} (on-current at linear region) and I_{dsat} (on-current at saturation region) are observed.

Figure 2.2.1 shows the percentages of these device parameters as the stress time increases. V_{th} increases with increasing stress time. I_{dlin} and I_{dsat}

are increased by 10% and 14% at first, respectively, and then start to decrease after around 1500 s.

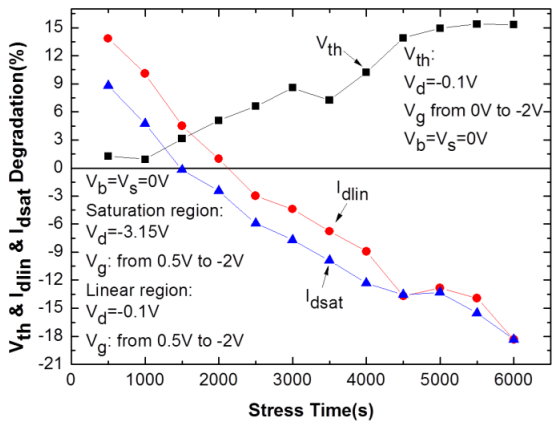
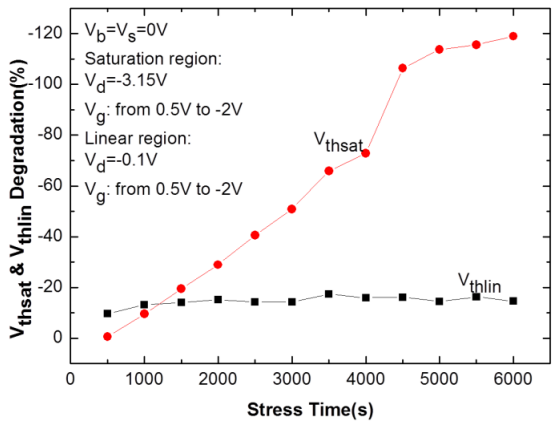


Fig. 2.2.1 Device parameter degradation after GIDL stress: V_{th}, I_{dlin}, I_{dsat}.

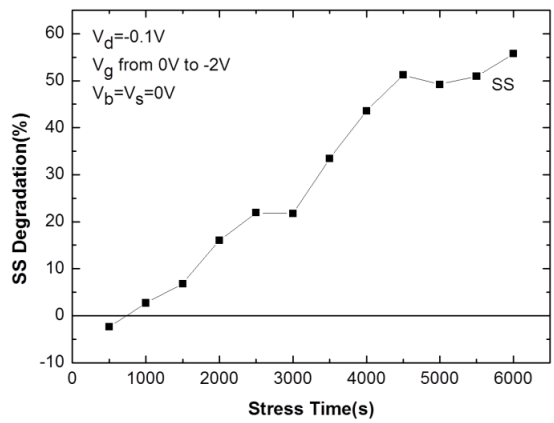
Secondly, the V_{thlin} (threshold voltage at linear region), the V_{thsat} (threshold voltage at saturation region) and *SS* (sub-threshold Swing) are observed.

Figure 2.2.2 (a) shows the percentage of V_{thlin} and V_{thsat} degradation as the stress times increases. Percentage of V_{thlin} degradation is almost independent of stress time, whereas that of V_{thsat} degradation increases with the stress time as a whole. In Fig. 2.2.2 (b), SS increases overall with increasing stress time because the interface trap capacitor (C_{it}) increases as

the interface trap increases [14].



(a)



(b)

Fig. 2.2.2 Percent degradation of device parameters with GIDL stress time. (a) V_{thlin}, V_{thsat}, (b) *SS*

Finally, the GIDL current dependence on stress time is measured, when the V_{dg} and V_s are swept from -2.15 V to -4.15 V and from -2 V to -4 V, respectively, at the same time.

Figure 2.2.3 shows the percentage of GIDL current increased as the stress time increases. Due to the large value of GIDL current before stress at high V_{dg}, the GIDL degradation percentage values at high V_{dg} are small. Note that the GIDL current degradation at V_d = -4.15 V before 1000s is negative value. It means that at high bias stress condition, the GIDL current decreases before about 1000s and increases after around 1000s. The polarity of the GIDL degradation changes with stress time because the polarity of trapped charge in the oxide changes from electrons to holes after ~1000s. It will be discussed later.

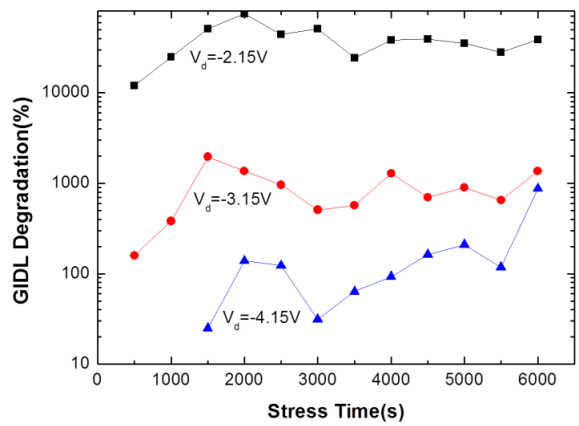


Fig. 2.2.3 Degradation percent of GIDL current after GIDL stress

2.3.Activation energy

With the purpose of finding the degradation mechanisms under GIDL

stress, three points should be noticed. They are activation energy, channel length modulation (CLM), and drain resistance degradation.

Equation (7) can be obtained from (6):

$$\ln\left(I_{leakage}\right) = \ln(A) - E_a(1/kT) \tag{7}$$

In (7) E_a can be calculated by using $\ln(I_{leakage})$ and $1/kT$.

The temperature-controlled measurement is used with the following conditions:

1) Temperature: 40 ℃, 60 ℃, 80 ℃, 100 ℃.

2) V_d: from -2.15 V to -4.15 V, (interval: 0.2 V).

3) V_d - V_s = -0.15 V.

4) V_g = V_b = 0 V.

Figure 2.3.1 shows the $\ln(I_{leakage\_GIDL})$~$1/kT$ curve. It should be noticed that the $I_{leakage\_GIDL}$ consists of GIDL current and junction leakage current.

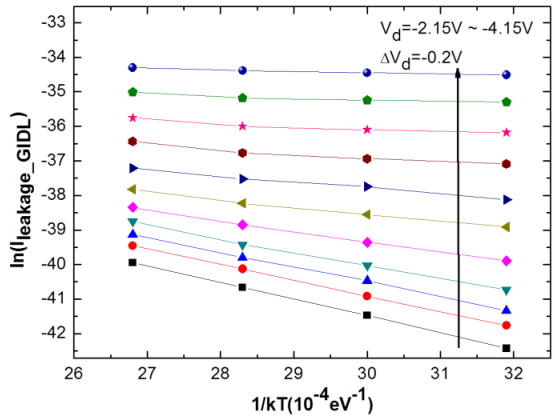


Fig. 2.3.1 $\ln(I_{\text{leakage\_GIDL}})$~$1/kT$ of p-MOSFET as a parameter of V_{d}

The activation energy of junction leakage current can be extracted by using the test structure with the gated diode, which is shown in Fig. 2.3.2.

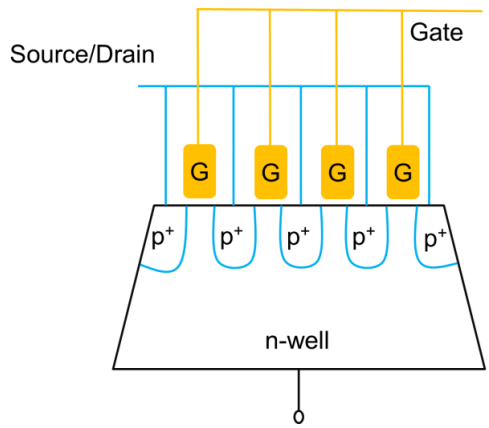


Fig. 2.3.2 Schematic cross-section of the gated diode test structure

The leakage current of the gated diode is measured by changing temperature, and the $\ln(I_{\text{leakage\_junction}})$~$1/kT$ curve is shown in Fig. 2.3.3. It

should be noticed that the $I_{leakage\_junction}$ in the test pattern is only the junction leakage current.

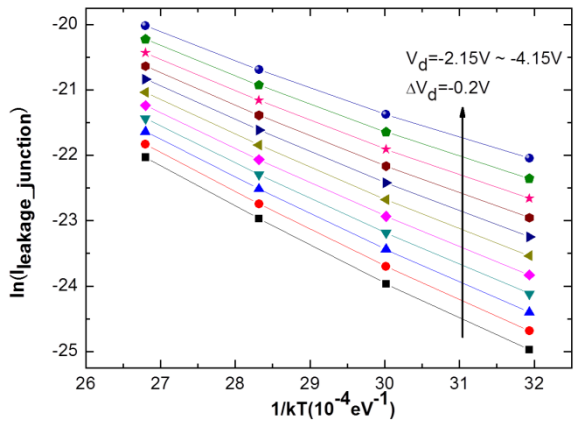


Fig. 2.3.3 $\ln(I_{leakage\_junction})$~$1/kT$ curve of the gated diode test pattern as a parameter of V_d

Figure 2.3.4 shows the activation energy versus V_d of the GIDL current and junction leakage current. As the field enhancement factor increases, the tunneling barrier decreases. So as V_{dg} increases, the activation energy decreases.

From the result shown in Fig. 2.3.4, there are three different slopes the GIDL current behavior.

1) E_a > 0.4 eV: E_a is relatively high near $E_g/2$. In this region, the slopes of the two lines are similar. SRH generation is responsible for the

leakage current.

2) 0.15 eV < E_a < 0.4 eV: E_a decreases significantly as V_{dg} increases. It means that field enhancement factor is high in this bias region. Equation (8) shows the relationship between the activation energy and applied bias [7]. The Poole-Frenkel (PF) effect is sensitive to the electric field and is the main mechanism to induce the TAT. The higher electric field, the higher concentration of emitted thermionic carriers, TAT needs the lower activation energy.

$$E_a \propto 1/\sqrt{V_{drain}} \tag{8}$$

3) E_a < 0.15 eV: E_a is quite small and reacts insensitively to V_{dg}. In this region, phonon-assisted tunneling (PAT) is the main mechanism instead of direct band-to-band tunneling (DBTB), because the activation energy is not close to 0 eV. Equation (9) shows the relationship between the activation energy and applied bias in this region [7].

$$E_a \propto 1/(V_{drain})^2 \tag{9}$$

From the result, 0.15 eV can be regarded as the turning point from

TAT to BTBT [15]. In this figure, 0.15 eV is corresponding to V_{dg} = -3.35 V. Note there is a certain difference between the activation energies of the different chip position.

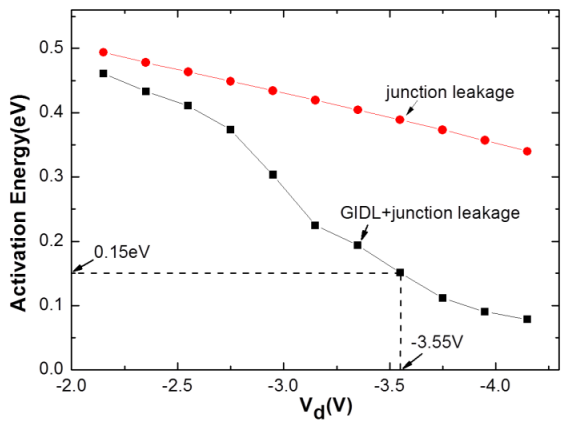


Fig. 2.3.4 Activation energy of GIDL and junction leakage current

2.4. Body current with CLM mechanism

In the second part of this chapter, the change of on-current degradation with the stress time has been described. At the beginning of the stress, the current increases, and the current decreases greatly as the stress continues.

The reason for the on-current change can be discussed in two respects: one is that the change of channel length affects the resistance of the channel.

The other is that the resistance of source/drain is affected by the density of traps generated by the stress.

Effective channel length can be modulated through CLM, which results in the change of on-current. When the drain bias is applied for more than saturation voltage, the pinch-off occurs. It means that at the beginning of the stress, the effective channel length decreases [16]. Equation (10) shows the relationship between effective channel length (L - ΔL) and physical channel length L.

$$I_{ds} = I_{d,sat}/[1 - (\triangle L/L)] \tag{10}$$

Meanwhile the CLM affects the performance of body current with gate voltage. In normal MOSFET, when pinch-off occurs in the channel region, the body current decreases as the gate voltage increase. And at the pinch-off point, the saturation voltage $V_{\mathrm{d,sat}}$ increases as the V_{gs} increases. So the max electrical field in the space charge region decided by the V_{gs} and $V_{\mathrm{d,sat}}$ decreases, the on-current decreases.

By analyzing the on-current measured with the stress time, the

effective channel length can be examined. In Fig. 2.4.1, the body current versus the gate voltage curves in a fresh state and after a stress (V_d / V_s = -5.15 V / -5 V, V_g / V_b = 0 V) of 5000s were compared. After GIDL stress, the body current did not decrease persistently as V_g increases more negatively than -1 V as in general cases, but increases. This illustrates after GIDL stress pinch-off does not occur in channel region and the effective channel length becomes longer, the max electrical field in the space charge region increases, and the body current increases. So the decrease of on-current after GIDL stress can be explained by increased effective channel length.

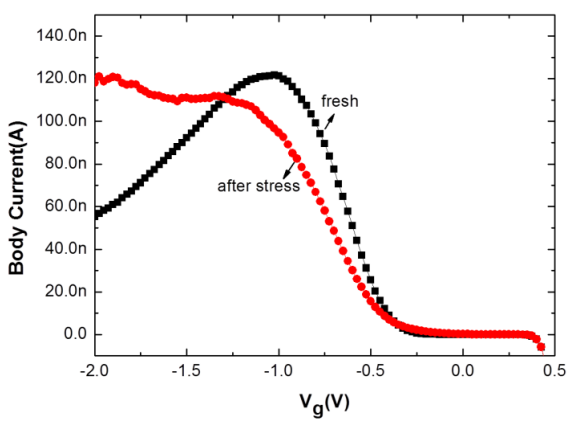


Fig. 2.4.1 Gate voltage dependence of body current: fresh and after 5000s GIDL stress (V_d / V_s = -5.15V / -5 V, V_g / V_b = 0 V)

2.5. Parasitic resistance degradation

The change of on-current also can be affected by channel resistance or source/drain parasitic resistance. The drain/source resistance after GIDL stress was analyzed and the change of on-current was explained.

As there is the only one kind of channel length for the device in this thesis, the parasitic resistance was measured at the fresh state and after GIDL stress by adopting the method in [4].

Equations (11) and (12) show the relation among source resistance R_s, drain resistance R_d, trans-conductance g_m, intrinsic trans-conductance g_{m0}, drain-conductance g_d, intrinsic drain-conductance g_{d0}, and intrinsic body-conductance g_{b0}.

$$g_m = g_{m0}/[1 + (g_{m0} + g_{b0})R_s + g_{d0}(R_s + R_d)] \quad (11)$$

$$g_d = g_{d0}/[1 + (g_{m0} + g_{b0})R_s + g_{d0}(R_s + R_d)] \quad (12)$$

Based on (11) and (12), if an external resistance R_x is added to source side, the new source resistance is $R_x + R_s$. The (13) is calculated by using (11) and (12). g_{ms} is the new trans-conductance after connecting an external

resistance to the source in series.

$$1/g_{ms} = 1/g_{m0} + R_s(1 + g_{b0}/g_{m0})$$

$$+(g_{d0}/g_{m0})(R_s + R_d) + R_x(1 + g_{b0}/g_{m0} + g_{d0}/g_{m0}) \qquad (13)$$

The same method can be adopted for the drain as (14). g_{md} is the new trans-conductance after connecting an external resistance to the drain in series:

$$1/g_{md} = 1/g_{m0} + R_s(1 + g_{b0}/g_{m0})$$

$$+(g_{d0}/g_{m0})(R_s + R_d) + R_x(g_{d0}/g_{m0}) \qquad (14)$$

In (13) and (14), when R_x is seen as the function, the slopes of the two equations are different because of the intrinsic conductance (g_{m0}, g_{d0}, g_{b0}). By analyzing the linear regression between external resistance and trans-conductance, the $1+g_{b0}/g_{m0}$ can be obtained. However, when the drain current is determined, intrinsic conductance is constant. It means that in this case the external resistance R_x cannot give any effect to the measurement result. Then R_d - R_s can be calculated by using (11) and (12) and is shown in

(15). The trans-conductance with the interchanged source and drain is g_{mr}. The trans-conductance without the interchanging is g_{mf}.

$$R_d - R_s = \left(1/g_{mr} - 1/g_{mf}\right)/(1 + g_{b0}/g_{m0}) \quad (15)$$

In this thesis, the external resistances are 991Ω, 2003Ω and 3868Ω, respectively. The curve of relation among $1/g_{ms}$, $1/g_{md}$ and the external resistance is shown in Fig. 2.5.1. The parameters extracted before and after the stress (3000s stress time, V_{dg} = -5.15 V and V_s = -5 V) are shown in Table 2.5.1.

Table 2.5.1 External resistance performance (measurements)

	$1+g_{b0}/g_{m0}$	$1/g_{mf}$	$1/g_{mr}$	R_d-R_s
Before stress	1.2349	16318.3	15773.9	-440.8
After stress	1.2611	15528.6	16330.6	635.9

In fresh condition, the resistance difference between drain and source is negative value because of asymmetrical S/D structure of *p*-MOSFET. However, after stress the difference between the drain and source resistance becomes the positive value. Compared to the value before stress, the difference is about 1076.7 Ω to 1270 Ω. It can be confirmed that the

resistance in drain side increases after stress, which results in the decreased on-current.

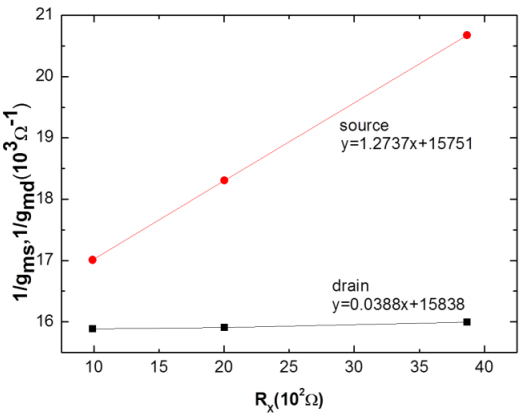


Fig. 2.5.1 Extracted $1/g_{ms}$ and $1/g_{md}$ versus the external resistance

2.6. GIDL current degradation under GIDL stress

In [3], it has been reported that the change of GIDL current under GIDL stress in LDD *n*-MOSFET can be divided into two stages through discussing from the high V_{dg} and the low V_{dg} conditions.

At the high V_{dg} condition, the polarity of the trap in the interface is neutral, thus only the oxide trapped charge influenced GIDL current. Due to the polarity change of trapped charge in the oxide, the GIDL current decreases firstly and then increases. At the first stage, the oxide trapped lucky holes depress the energy band bending of Si. The GIDL current

caused by BTBT will decrease. At the seconded stage, as the stress time increases, the electrons supplied by tunneling neutralize the holes trapped in the oxide. As the number of electrons is larger than that of the lucky holes, the band bending becomes serious. Ultimately, the GIDL current increases through BTBT.

At the low V_{dg} condition, the interface traps alter GIDL current through TAT. As the stress time increases, the interface traps density keeps on increasing, so the GIDL current persistently increases through TAT assists in BTBT. The main mechanism of the GIDL current is TAT, and it is BTBT at the high V_{dg}.

K.S. Kim *et al*. in [2] also discussed the influence of hot carrier caused by GIDL stress, but in the case of PMOS. At the beginning of stress, the hot carrier is lucky electron. As the stress further proceeds, holes are trapped due to tunneling. Due to the trapped electrons at the early stages, the channel length becomes shorter than before. And then holes are trapped at the late stage. As the number of trapped holes is higher than that of the

trapped electrons, the channel length becomes longer than before.

2.7. Degradation mechanism

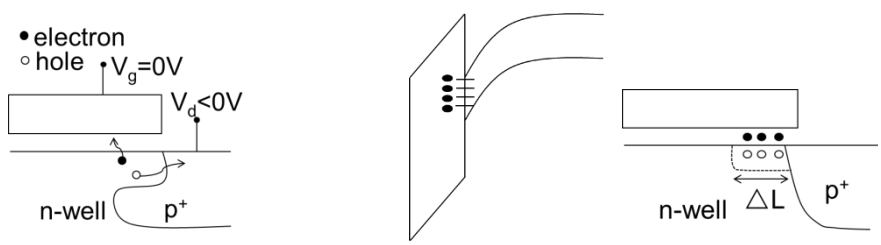
From the above measurement and discussion, the mechanisms responsible for the degradation of device parameters in *p*-MOSFET can be summarized in Table. 2.7.1.

Table 2.7.1 Degradation mechanisms in nano-scale *p*-MOSFET under GIDL stress at the early stage and late stage

	Effect	**Mechanism**	**Cause**
	Early stage		
I_d (linear)	increase	CLM	electron injection
GIDL (high V_{dg})	decrease	BTBT	
GIDL (low V_{dg})	increase	TAT	interface trap
SS	increase	C_{it}	
	Late stage		
I_d (linear)	decrease	resistance degradation	interface trap
		CLM	hole injection
GIDL (high V_{dg})	increase	BTBT	
GIDL (low V_{dg})	increase	TAT	interface trap
SS	increase	C_{it}	

In Table 2.7.1, the early stage indicates GIDL stress time before 1000s and the late stage means after 1000 s. In the early stage, as interface traps

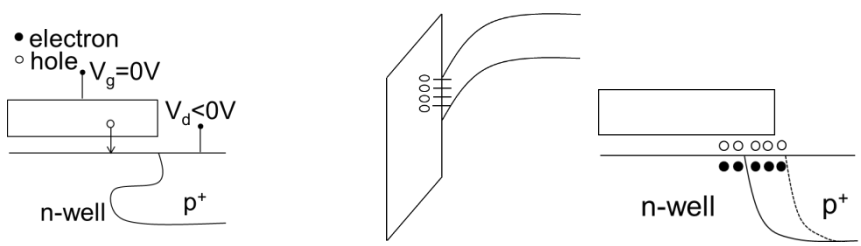
increase, the GIDL current increases through TAT at the low V_{dg} condition. At the high V_{dg} condition, electrons are trapped in the oxide due to the accelerated hot electrons. The trapped electrons in the oxide have two functions: the first is that the trapped electrons near drain side lead to the accumulation of holes in the channel region and then the effective channel length decreases and on-current increases; the second is the trapped electrons limit the energy band bending in the drain region overlapped by gate. In other words, BTBT is limited and the GIDL current in high V_{dg} condition decreases. The model graphs to explain the situation are shown in Fig. 2.7.1.



(a) (b) (c)

Fig. 2.7.1 Degradation mechanism model graph in early stage (a) hot electron trapping, (b) band diagram after stress, (c) channel length modulation

In the late stage, as the stress time increases, the more interface traps are generated. As a result, the occurrence of TAT increases, so the GIDL current at low V_{dg} condition increases. At high V_{dg} condition hole trapping occurs and the effective channel length becomes longer than the physical length. Therefore, *SS* is worse than before because of the increasing interface trap capacitors. Besides, the drain resistance increases, resulting in the decrease of the on-current. Hole trapping increases with increasing stress time. Trapped holes neutralize previously trapped electrons. The trapped holes result in the more serious energy band bending, and then BTBT occurs significantly. Consequently, the GIDL current at high V_{dg} condition increases. The model graphs to explain the situation are shown in Fig. 2.7.2.



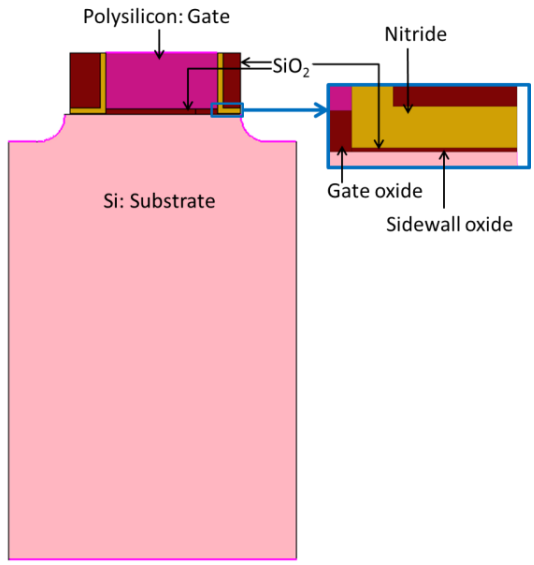
(a) (b) (c)

Fig. 2.7.2 Degradation mechanism model graph in late stage (a) hot electron, (b) band diagram after stress, (c) channel length modulation

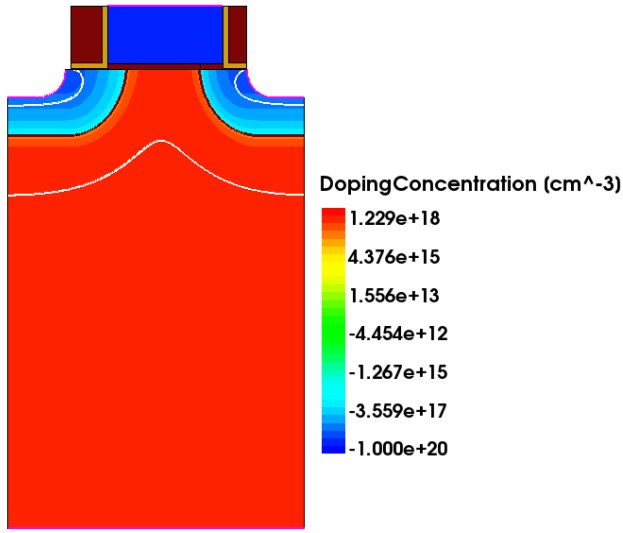
3. Simulation of *p*-MOSFET before and after GIDL stress

3.1. Simulation of *p*-MOSFET

The device structure was drawn by the TCAD simulation suite, Sentaurus [17], and then, the mesh and doping profile were set, the appropriate physical models are selected, and the parameters are calibrated through the degradation mechanisms. 2D TCAD simulation was performed using SENTAURUS^{TM} to know the internal physics of the *p*-MOSFET fabricated on the silicon substrate using the conventional CMOS process. A boron doping concentration of *n*-type substrate was 1×10^{15} cm^{-3} and that of the poly-silicon gate was 1×10^{20} cm^{-3}. Fig. 3.1.1 shows the simulation process from structure to doping profile.



(a)



(b)

Fig. 3.1.1 (a) Simulation device structure, (b) simulation doping profile

The experimental evidence shows the interface traps are distributed like a 'U'-shaped curves and two Gaussian distribution in the middle of 'U'-shaped curves [18][19]. In this work, the interface trap density distribution is showed in Fig. 3.1.2. With the capture cross section of 1×10^{-13} cm^2, donor-like traps density and acceptor-like traps density of 1×10^{13} $eV^{-1}cm^{-2}$ are distributed exponentially in the gate oxide/substrate interface. And in the sidewall oxide/substrate interface, in addition to the above-mentioned interface trap distributions, there are donor-like traps and acceptor-like traps distributed in Gaussian with the density of 8×10^{12} $eV^{-1}cm^{-2}$ and 7×10^{12} eV^{-1} cm^{-2}. And the central point of Gaussian distribution is 0.29 eV from the middle of the bandgap.

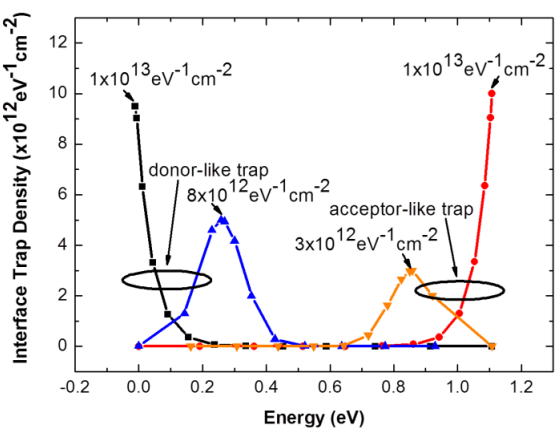


Fig. 3.1.2 Interface trap density distribution

For GIDL current fitting, the selection of tunneling model is an important issue. In Sentaurus, there are two standard simulation models for TAT: Schenk TAT model [20] and Hurkx BTBT model [21]. Besides, there are four standard simulation models for BTBT: Schenk BTBT model, Hurkx BTBT model, Kane BTBT model and the dynamic Nonlocal BTBT model [11][17]. For finding the suitable model of simulation, the two TAT models and the four BTBT models were compared respectively. And the V_d was from -2.15 V to -4.15 V, V_s was from -2 V to -4 V, $V_g = V_b = 0$ V, and all of the parameters in tunneling models were set as default at 300 K (room temperature) [17].

Figure 3.1.3 shows the simulation curves of Schenk TAT model and Hurkx TAT model and the measurement GIDL current curve. The different levels of current magnitude, but similar slope can be observed between the two TAT models. However, for the fitting purpose, Schenk TAT model is more flexible than Hurkx TAT model due to the five parameters can be modified: energy of trap level, Huang–Rhys factor, effective phonon energy,

smoothing at small electric fields and carrier tunneling mass. Besides, there are field enhancement factor and temperature dependence in Schenk TAT model, corresponding to the fitting of I-V curve and the activation energy. So the Schenk TAT model was selected. And then the value of effective phonon energy was adjusted from 0.068 eV to 0.09 eV and the carrier tunneling mass was adjusted from (0.258, 0.24) to (0.4, 0.4).

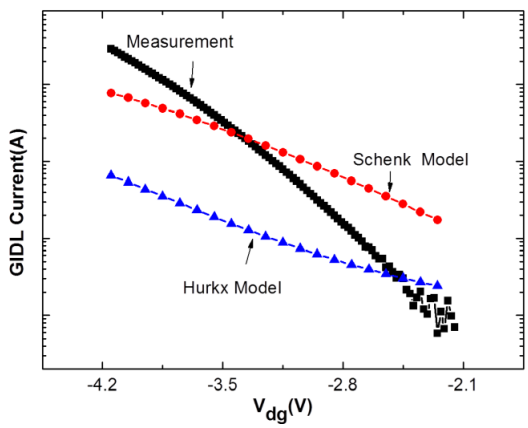


Fig. 3.1.3 Simulated GIDL current using standard trap assisted tunneling models with default parameters: Schenk TAT model, Hurkx TAT model versus measurement

Figure 3.1.4 shows the simulation curves of four BTBT models and the measurement GIDL current curve. The simulation curves corresponding to Kane BTBT model and the Dynamic Nonlocal BTBT model have the

similar slope, but the former one is too optimistic for the target device and the Schenk BTBT model too. And the Hurkx BTBT model has too small GIDL current to target device. While the Dynamic Nonlocal BTBT model has the similar slope and current level with measurement curve. Actually, the Dynamic Nonlocal BTBT model is an improvement of Kane model [11]. It supplies three tunneling paths, and every path can be set in indirect BTBT or direct BTBT respectively, the same as phonon assisted tunneling (PAT) and direct tunneling (DT), by setting whether the phonon energy is 0 eV [17]. Due to that it is flexible for fitting because the PAT and DT can be adjusted respectively, the Dynamic Nonlocal BTBT model is more appropriate for target device according to the degradation mechanisms.

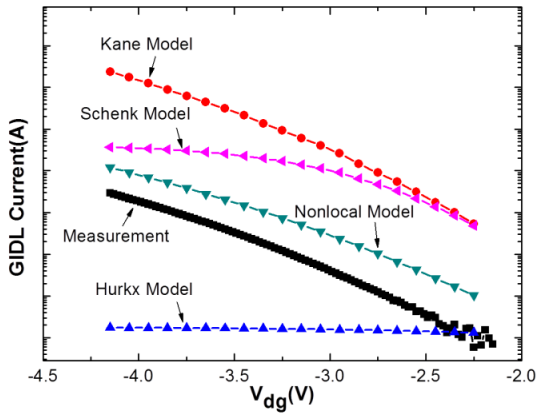


Fig. 3.1.4 Simulated GIDL current using standard trap band-to-band tunneling models with default parameters: Schenk BTBT model, Hurkx BTBT model, Kane BTBT model and the Dynamic Nonlocal BTBT model versus measurement

Finally, the results achieved by using the Schenk TAT model and the Dynamic Nonlocal BTBT model. For BTBT model, two paths were set. Due to the dominant tunneling is PAT in the silicon [11], the path1 was set as PAT and the path2 was set as DT. The parameters of the Dynamic Nonlocal BTBT model have been modified basing on the default value in [17] and the calibrated values in the literatures [11][12]. Table 3.1.1 shows the calibrated parameters in this thesis. To ensure the accuracy of the calibrated parameters, the drain current dependence on gate bias at on-state and the

GIDL current at high bias of target device were also simulated (V_d = -3 V, V_b = V_s = 0 V, V_g from -3 V to 3 V, at room temperature), and were shown in Fig. 3.2.2.

Table 3.1.1 Calibrated parameters for dynamic Nonlocal-tunneling: Path1 was used for phonon assisted tunneling (PAT); Path2 was used for direct tunneling (DT)

	A($(cm^{-3}s)^{-1}$)	B(V/cm)	D(eV)	P(eV)	R(-)
PAT	$5•10^{12}$	$1.33•10^{7}$	0	0.037	0
DT	$3•10^{21}$	$3.4•10^{7}$	0.15	0	0

3.2. Simulation results and analysis

The GIDL current simulation curves with no tunneling, only TAT, only PAT, only DT and the fitted result simulation curve versus measurement curve can be seen in Fig. 3.2.1. The GIDL current increases slightly through adding TAT model comparing to the curve of no tunneling. And compared with PAT, GIDL current is attributed to TAT when the V_d is less than about -2.75 V. When V_d is more than -2.75 V, GIDL current is mostly attributed to PAT. When V_d is more than about -3.55 V, the current due to DT increased significantly as the dominant part of GIDL current.

Finally the fresh GIDL current simulation curve is similar with the measurement curve can be observed.

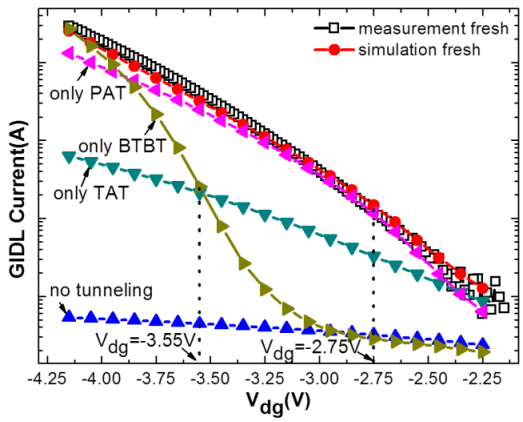


Fig. 3.2.1 Contributions of different paths to the GIDL current at V_s from -2 V to -4 V, V_b = V_g = 0 V: trap assisted tunneling (TAT), phonon assisted tunneling (PAT), direct tunneling (DT)

To observe the effect of PAT and DT clearly, for I_d -V_g simulation, the different simulation approach from the approach adopted in GIDL current simulation. The GIDL current at high electric field is mainly attributed to the BTBT, in Fig. 3.2.2, the drain current simulation curves with no tunneling, only TAT, both TAT and PAT, both TAT and DT and the fitted simulation curve versus measurement curve are showed in Fig. 3.2.2. All the

V_{th}s are nearly the same as the measurement curve and the slope of the fresh GIDL current simulation curve is similar to measurement curve. After adding TAT model, GIDL current increased, but did not reach the level of the measurement curve. This confirms that the GIDL current generation is mostly attributed to BTBT at high electric field. Based on the TAT curve, PAT is the dominant part of the GIDL current at the lower V_{dg}, DT dominated at the higher V_{dg}. Note that the different level of the fresh GIDL current simulation curve and measurement fresh curve is caused by the high gate voltage that affects the drain current through making the breakdown of the protection diode between the gate and the substrate, which is shown in Fig. 3.2.3.

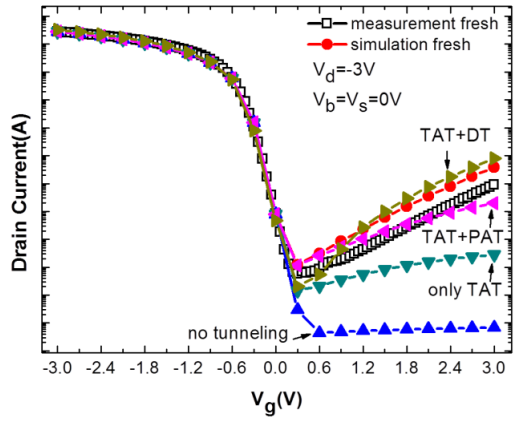


Fig. 3.2.2 Contributions of different paths to the Drain current at V_d = -3 V, V_s = V_b = 0 V: trap assisted tunneling (TAT), phonon assisted tunneling (PAT), direct tunneling (DT)

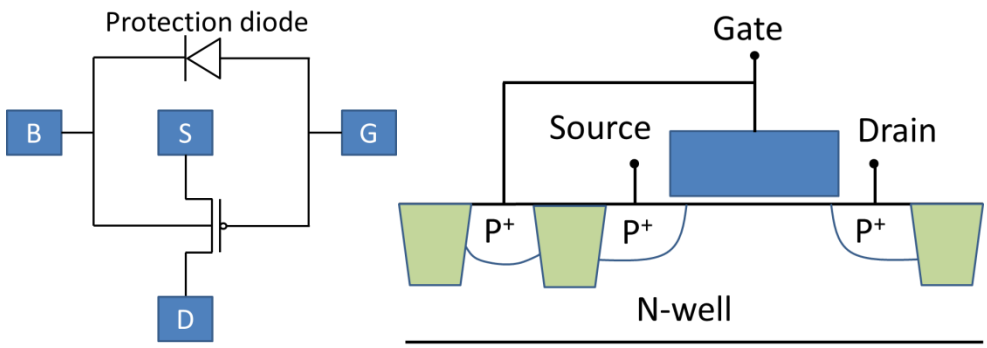


Fig. 3.2.3 Schematic cross-section of the target device with protection diode

In order to ensure the accuracy of previous simulations, the activation energy of GIDL current is compared between simulation and measurement. Note that the device showing the activation energy in Fig. 3.2.4 is the same device as that in Figs. 3.2.1 and 3.2.2 but different from the device in Fig.

2.3.4. So there is a difference between Fig. 3.2.4 and Fig. 2.3.4.

The simulated GIDL currents dependence on V_{dg} under GIDL mode at temperatures from 0 ℃ to 100 ℃ with an interval of 20 ℃ was shown in the inset of Fig. 3.2.4. And then the activation energy (E_a) was calculated using the method in [22] and was shown in Fig. 3.2.4. Due to BTBT is almost not dependent on temperature in activation energy below 0.15 eV [22]. The activation energy required for TAT is higher than that required for BTBT. In Fig. 3.2.4, when activation energy is 0.15 eV, both measured and simulated curves are corresponding to a V_{dg} of -3.8 V, which is similar with the result in Fig. 3.2.1. So V_{dg} = -3.8 V can be seen as the turning point from TAT to BTBT in target device.

The activation energy for DT in BTBT is nearly 0 eV [16]. In Fig. 3.2.4, from about 0.025 eV, the simulated and measured activation energies are nearly the same (~0 eV) around a V_{dg} of -3.55 V. This result corresponds to the description mentioned above and the GIDL is mainly attributed to DT.

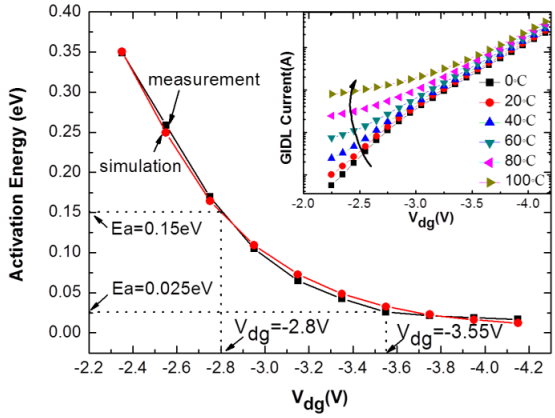
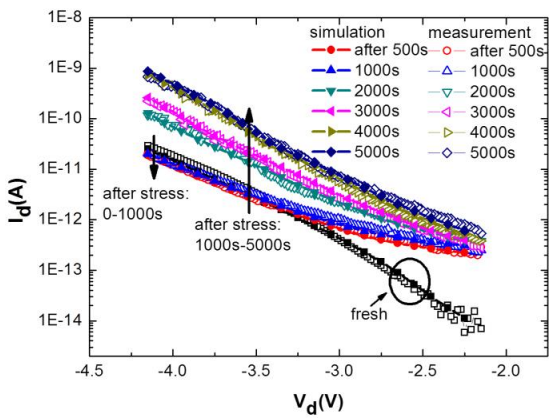


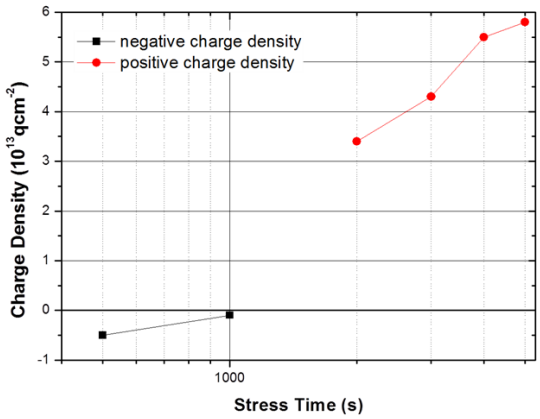
Fig. 3.2.4 Simulated GIDL current dependence on drain bias with different temperature; simulated activation energy versus measurement

As mentioned in chapter 2, the degradation of *p*-MOSFET at a high electric field is mainly attributed to the oxide charge. In order to ensure the generation of oxide charge in the simulation, a layer of oxide charge with a different polarity was added to the nitride very close to the sidewall/sidewall oxide interface. With the measurement condition: V_d from -2.15 V sweep to -5.15 V, V_{ds} = -0.15 V, V_g = V_b = 0 V, for early stage, the GIDL current curves after 500 s and 1000 s stress were simulated through adding negative charges and interface traps with different density. And for the late stage, the GIDL current curves after 2000 s, 3000 s, 4000 s and 5000 s stress were simulated through added positive charges and interface

traps with different density. The curve of GIDL current simulations fitted to the measurement results with different stress time and the curve of oxide charge dependencies on stress time are showed in Fig. 3.2.5 and the specify density values are shown in Table 3.2.1. The negative charge density decreases as stress time increases and the positive charge density increases as stress time increases. So the GIDL current decreases in the early stage at high electric field because of negative charge, increases in the late stage at high electric field because of positive charge.



(a)



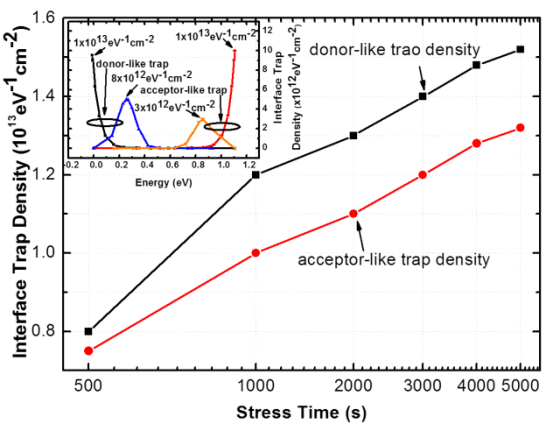
(b)

Fig. 3.2.5 (a) GIDL current simulations fitted to the measurement results after GIDL stress with different stress times, (b) negative charge density and the positive charge density dependencies on the stress time

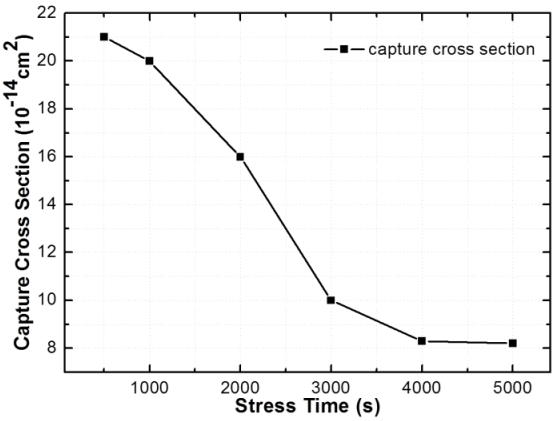
Table 3.2.1 Charge density dependence on stress time in simulation

Stress Time(s)	Charge Density(qcm^{-2})
Early stage	Negative charge
500	-5e12
1000	-1e12
Late stage	Positive charge
2000	3.4e13
3000	4.3e13
4000	5.5e13
5000	5.8e13

And the interface trap density and capture cross section dependence on stress time are shown in Fig. 3.2.6 and the specify density values are shown in Table 3.2.2. The interface trap density increases as increasing stress time and has the saturation. On the contrary, the capture cross section decreases as increasing stress time due to the oxide trapped charges from the Si/SiO_2 interface [23-25].



(a)



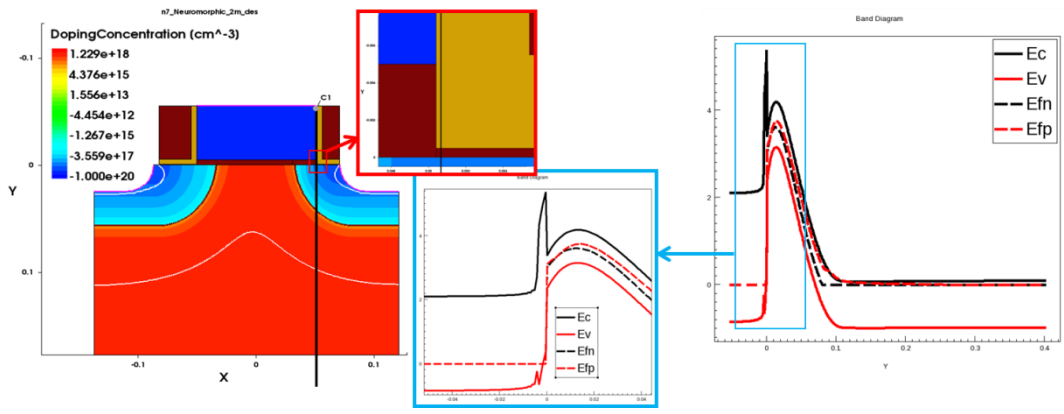
(b)

Fig. 3.2.6 (a) Interface trap density dependence on the stress time, (b) capture cross section dependence on the stress time

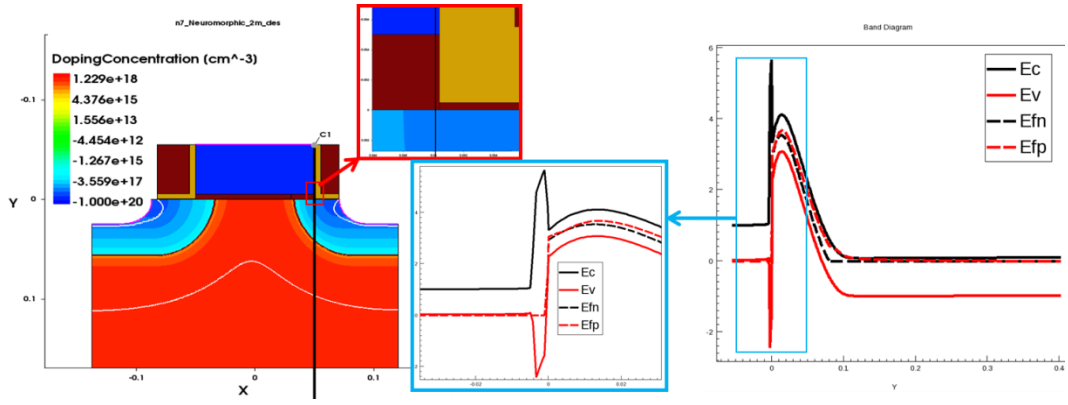
Table 3.2.2 Interface trap density and capture cross section dependence on stress time in simulation

Stress Time	**Interface Trap Density ($eV^{-1}cm^{-2}$)**		**Capture Cross Section (cm^2)**
Early stage	Donor-like	Acceptor-like	Early stage
After 500s	8e12	6e12	2.1e-13
After 1000s	1.2e13	1e13	2e-13
Late stage	Donor-like	Acceptor-like	Late stage
After 2000s	1.3e13	1.1e13	1.6e-13
After 3000s	1.4e13	1.2e13	1e-13
After 4000s	1.48e13	1.28e13	8.3e-14
After 5000s	1.55e13	1.35e13	8.2e-14

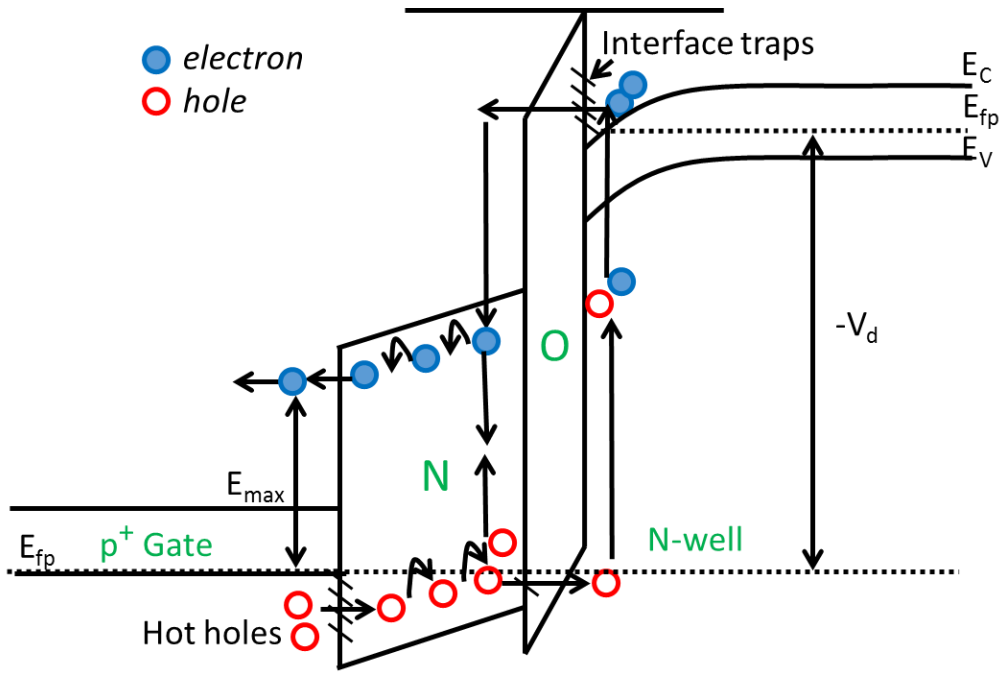
For the increasing interface trap density, the energy band diagrams at different positions in simulation is checked to observe the energy band bending under GIDL bias stress as shown in Fig. 3.2.7. Figure 3.2.7 (a) shows the band bending cut along Nitride, thin SiO_2 and p^+ Drain. And Fig. 3.2.7 (b) shows the band bending cut along p^+ Gate, SiO_2 and p^+ Drain. And then a schematic energy band diagram cut along p^+ Gate, Nitride, thin SiO_2, and p^+ Drain is shown in Fig. 3.2.8, and used to explain the trap generation at the interface between the SiO_2 and p^+ Drain. Because of a high negative bias at drain, holes in p^+ Gate move to the p^+ Drain. The hole passes through the nitride layer by Poole-Frenkel tunneling and goes through thin SiO_2 layer by direct tunneling. The holes moved from the gate to the drain have a high energy due to the high negative bias applied to the drain. These holes reaching the p^+ drain region lose energy and this energy is transferred to the electrons in the valence band. The electrons are excited on the conduction band to become hot electrons. These hot electrons impinge physically on the interface with SiO_2 to create an interfacial trap.


n7_Neuromorphic_2m_des
DopingConcentration (cm^-3)
1.229e+18
4.376e+15
1.556e+13
-4.454e+12
-1.267e+15
-3.559e+17
-1.000e+20
C1
X
Y
Band Diagram
Ec
Ev
Efn
Efp

(a)


n7_Neuromorphic_2m_des
DopingConcentration (cm^-3)
1.229e+18
4.376e+15
1.556e+13
-4.454e+12
-1.267e+15
-3.559e+17
-1.000e+20
C1
X
Y
Band Diagram
Ec
Ev
Efn
Efp

(b)



(c)

Fig. 3.2.7 (a) Band bending cut along Nitride, thin SiO_2 and p^+ Drain, (b) band bending cut along p^+ Gate, SiO_2 and p^+ Drain, (c) a schematic energy band diagram cut along p^+ Gate, Nitride, thin SiO_2, and p^+ Drain, and used to explain the trap generation at the interface between the SiO_2 and p^+ Drain

4. Conclusion

The GIDL current and the degradation phenomenon during device lifetime in PMOS are essential for better performance, higher densities and lower power consumption DRAM to reduce the standby power. In order to understand the mechanisms during this process, the electrical measurement result and the simulation result in a PMOS test pattern were discussed.

To verify the influence of GIDL stress in PMOS, acceleration tests with determined high bias stress were implemented. And then after adjusting the condition of acceleration incessantly, the appropriate DC high bias stress condition was confirmed and implemented. Then according to the result of measurement, the behavior of related device parameter was sorted. Besides, the behavior of important parameters such as GIDL current, on-current and SS was analyzed.

In order to clarify the reason of parameter degradation after bias stress, activation energy, body current with CLM phenomenon, and parasitic

resistance were discussed. Based on the measured results, the degradation mechanisms were analyzed. It was shown that the interface states and oxide charges are generated due to hot carriers. So the degradation mechanisms after high bias stress in PMOS were indicated.

Besides, the major mechanisms of GIDL current generation were studied in this paper through simulation using the appropriate tunneling models: Schenk TAT model and the Dynamic Nonlocal BTBT model. In order to match the simulation results to the measurement results, the value of the tunneling models' parameters were calibrated and then the results were discussed. The TAT is responsible for GIDL current generation at a low electric field, and needs higher activation energy. The BTBT dominates GIDL current generation at a high electric field, and needs lower activation energy.

Furthermore, for finding the density trend of the different polarity oxide charges and interface traps under different stress times, the GIDL currents were measured after different stress time and the simulation results

were fitted to the measurement results. As the stress time increases, at early stage, the negative charge density decreases and the interface trap increases; at late stage, the positive charge density increases and the interface trap increases.

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초 록

본 연구에서는 나노 크기 채널길이를 갖는 p-MOSFET에서 Gate Induced Drain Leakage (GIDL)이 발생하는 스트레스 조건하에서 소자의 열화 현상을 분석하여 발생 원인을 규명하고, 모델링하는 연구를 수행하였다. 열화 원인을 규명하기 위해 stress 시간을 변화시키면서 high bias stress측정을 실시한 이후에 소자의 GIDL 전류와 다른 전기적 특성들이 어떻게 변화하는지를 확인하고 분석하였다. 분석 결과를 바탕으로 열화의 원인을 검증하기 위해 시뮬레이션을 실시하였다. SENTAURUS^{TM}을 이용한 2D TCAD 시뮬레이션을 진행하면서 silicon 기판에서의 CMOS 공정에 대한 기본 매개변수를 사용하고, 필요에 따라 관련 매개변수는 기존 연구 결과를 바탕으로 조정되었다.

여러번의 시뮬레이션과 최적화 작업을 통해서 stress전후의 PMOS에서의 GIDL 전류에 대한 fitting을 진행하였다. 기존의 연구결과를 통해 잘 알려진 바와 같이 GIDL 전류 생성의 원인은 Band-to-band Tunneling (BTBT)하고 Trap-assisted Tunneling (TAT)이기 때문에, 상기 물리적 현상에 대한 적절한 모델을 선정하고, 매개변수에 대한 조정작업을 실시하였다.

High bias stress test에서 stress시간에 따라, stress 전후의 PMOS에서의 GIDL 전류와 on-current의 변화 경향은 두 단계로 구분할 수 있었다. GIDL stress에서의 PMOS 소자의 열화 원인은 TAT, BTBT, channel length modulation (CLM), 그리고 parasitic

resistance degradation으로 분석 되었다. 상기에 언급된 현상은 PMOS 소자의 열화의 과정에서 생성되는 interface state와 trap된 charge가 GIDL 전류와 on-current 변화의 경향을 잘 설명해 주고 있음을 분석하여 밝혀내었다. 추가적으로 GIDL stress 시간에 따라 증가하는 charge density와 interface trap density를 시뮬레이션을 통해 추출하여, GIDL stress 현상을 설명할 수 있는 열화 모델을 수립하였다.

주요어: GIDL stress, TAT, BTBT, CLM, 소자 열화, activation energy, interface trap, oxide charge

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