저작자표시-비영리-변경금지 2.0 대한민국

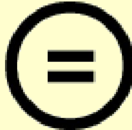
이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:

저작자표시. 귀하는 원저작자를 표시하여야 합니다.

비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 이용허락규약(Legal Code)을 이해하기 쉽게 요약한 것입니다.

Disclaimer

dCollection

M.S. THESIS

Capacitance–Voltage Characterization of Tunnel Field Effect Transistors with a Si/SiGe Heterojunction

Si/SiGe 헤테로 접합을 가지는 터널링 전계효과 트랜지스터의 전기 용량 특성

BY

TAEHYUNG PARK

July 2017

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

Capacitance–Voltage Characterization of Tunnel Field Effect Transistors with a Si/SiGe Heterojunction

Si/SiGe 헤테로 접합을 가지는 터널링 전계효과 트랜지스터의 전기 용량 특성

지도교수 박 병 국

이 논문을 공학석사 학위논문으로 제출함

2017 년 7 월

서울대학교 대학원

전기컴퓨터공학부

박 태 형

박태형의 공학석사 학위논문을 인준함

2017 년 7 월

위 원 장 : 박 영 준 (인)

부위원장 : 박 병 국 (인)

위 원 : 이 종 호 (인)

ABSTRACT

A Si capping layer on a SiGe channel is essential to improve the interface properties between the SiGe channel and the gate insulator. Thus, devices with a Si capping layer should be analyzed to understand their electrical characteristics. In this thesis, a strained Si/SiGe heterojunction TFET is investigated via capacitance–voltage measurements, which are rapid and non-destructive. The C–V analysis method in a strained Si/SiGe heterojunction TFET is improved through TCAD simulations. Through a C–V analysis, important parameters pertaining to devices, such as the layer thicknesses and threshold voltages, can be extracted.

Keywords: Tunnel Field Effect Transistor, Threshold Voltage, Apparent Carrier Concentration, Capacitance, Si Capping Layer, Centroid.

Student number: 2014-21725

CONTENTS

Abstract -- i

Contents -- iii

1. Introduction --- 1

2. Structure of SiGe Tunnel Field Effect Transistor with Si Capping Layer--- 5

2. 1. Device Configuration -- 5

3. Approximate the Thickness of Si Capping Layer ------------------ 8

3. 1. Introduction -- 8

3. 2. Apparent Carrier Concentration ---------------------------------------12

3. 3. Two Type of Threshold Voltage --13

3. 4. Approximate the Thickness of Si Capping Layer with C-V characteristics --15

4. Modify the Thickness of Si Capping Layer with Centroid Effect -- 19

4. 1. Introduction ---19

4. 2. Hole Centroid in the Si Capping Layer ---------------------------------21

4. 3. Modified Thickness of Si Capping Layer -------------------------------24

5. Conclusion --26

References --27

Abstract in Korean --29

1. Introduction

Many researchers have studied the tunnel field-effect transistor (TFET), which has a low sub threshold swing (SS) and small leakage current, unlike metal-oxide semiconductor field-effect transistors (MOSFETs). However, TFETs have the disadvantage of a low on-current value due to the high tunneling resistance (Fig. 1.1). To improve the current characteristics of TFETs, a SiGe channel is used because it has a narrow band gap compared to that with Si. Thus, the on-current can be increased and SS can be lowered. However, SiGe devices have the critical issue of poor interface properties between the SiGe channel and the gate insulator owing to the high interface trap density. In order to realize superior interface properties, specific

technologies have not yet been established. Therefore, a Si capping layer is inserted between the SiGe channel and gate insulator to reduce the trap density.

When a thick Si capping layer is grown, improved current properties arising from the narrow band gap cannot be obtained because tunneling occurs near the surface. Therefore, a thin Si capping layer should be grown on the SiGe channel. After forming a thin Si capping layer, layer information related to the Si capping layer must be analyzed to understand the device characteristics. The layer information can be obtained through transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS). However, these techniques are destructive and slow. Therefore, a non-destructive and rapid technique by which the layer information can be obtained is desirable. Among these techniques, capacitance–voltage (C–V)

characterization is widely used because it is rapid and nondestructive. Previous works have addressed the Si/SiGe heterojunction capacitance of metal-oxide-semiconductor (MOS) capacitors. We extend the C–V characterization technique to TFETs with the charge centroid effect.

In this thesis, the Si/SiGe heterojunction capacitances of TFETs with n-type substrates are investigated by means of C–V characterization techniques. In addition, the charge centroid effect is added to extract accurate parameters. The thickness of the Si capping layer and the threshold voltages are extracted by analyzing the C–V data. The extracted parameters are then compared with the device structural information.

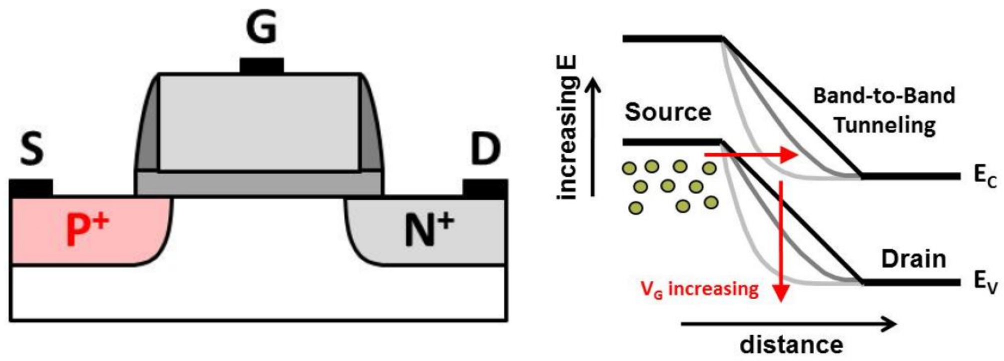


Fig. 1.1 Conceptual diagram of Tunnel Field Effect Transistor

2. Structure of SiGe Tunnel Field Effect Transistor with Si Capping Layer

2.1. Device Configuration

In previous studies, the C–V characterization of MOS capacitors was done to verify the thickness of the Si capping layer. To extract accurate parameters, the charge centroid effect, which considers the mismatch between the charge centroid and the physical interface, should be applied. In this thesis, a TFET with an n-type substrate is used in a simulation (Fig. 2.1).

In order to investigate the C–V characteristics of the TFET with the n-type substrate, a Sentaurus™ TCAD simulation system from Synopsys Inc. (ver. D-2010.12) is used. In this simulation, the gate length is fixed at 1000 nm

and the gate work function for the TFET with the n-type substrate is set to 4.05 eV. In addition, the thicknesses of the SiGe channel, Si substrate, and oxide are 10 nm, 100 nm, and 10 nm, respectively. Three thicknesses of the Si capping layer are used: 1 nm, 3 nm, and 5 nm. The doping concentrations of the source, channel, and drain are 1×1020, 1×1015, and 1×1020, respectively. The dopant of the source is boron, while the dopant of the channel and drain are phosphorous. The Ge mole fraction of the SiGe channel is 30%. The frequency of the AC gate voltage is 100 Hz to analyze the low-frequency C–V curve (Table 2.1).

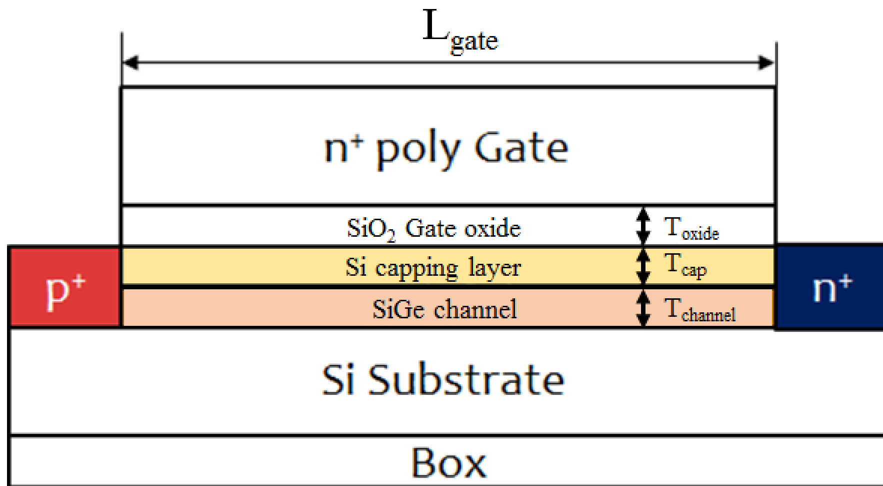


Fig. 2.1 Structure of the proposed SFST.

Table 2.1 Parameters used in the simulation.

Parameters	Value
Body thickness	10 nm
Channel length	1000 nm
Body doping concentration	10^{15} cm^{-3}
S/D doping concentration	10^{20} cm^{-3}
Gate oxide thickness	10 nm
Gate work function	4.05 eV

3. Approximate the Thickness of Si Capping Layer

3.1. Introduction

The low-frequency C–V curve from the TFET with the n-type substrate is extracted through a TCAD simulation. When the thicknesses of the Si capping layer are 3 nm and 5 nm, hump phenomena arise in the low frequency C–V curve in Fig. 3.1. Due to the valence band offset in the Si and SiGe energy band, there is a potential barrier at the interface between the Si capping layer and the SiGe channel in Fig 3.2. Therefore, the inversion is divided into two parts. First, the SiGe channel is inverted. Next, holes accumulate in the Si capping layer when the SiGe channel is fully inverted. For the device with a 1

nm Si capping layer, a hump arises due to the valence band offset. However, such a hump is not readily observed in the C–V curve. In order to understand the hump phenomenon in the device with the 1 nm Si capping layers and to analyze this quantitatively in all cases, parameter extraction from the C–V curve must be done.

In this chapter, how the thickness of Si capping layer is extracted from C-V characteristics is investigated. The apparent carrier concentration and the threshold voltage can be calculated from C-V characteristics. From these data, the thickness of Si capping layer can be approximated roughly.

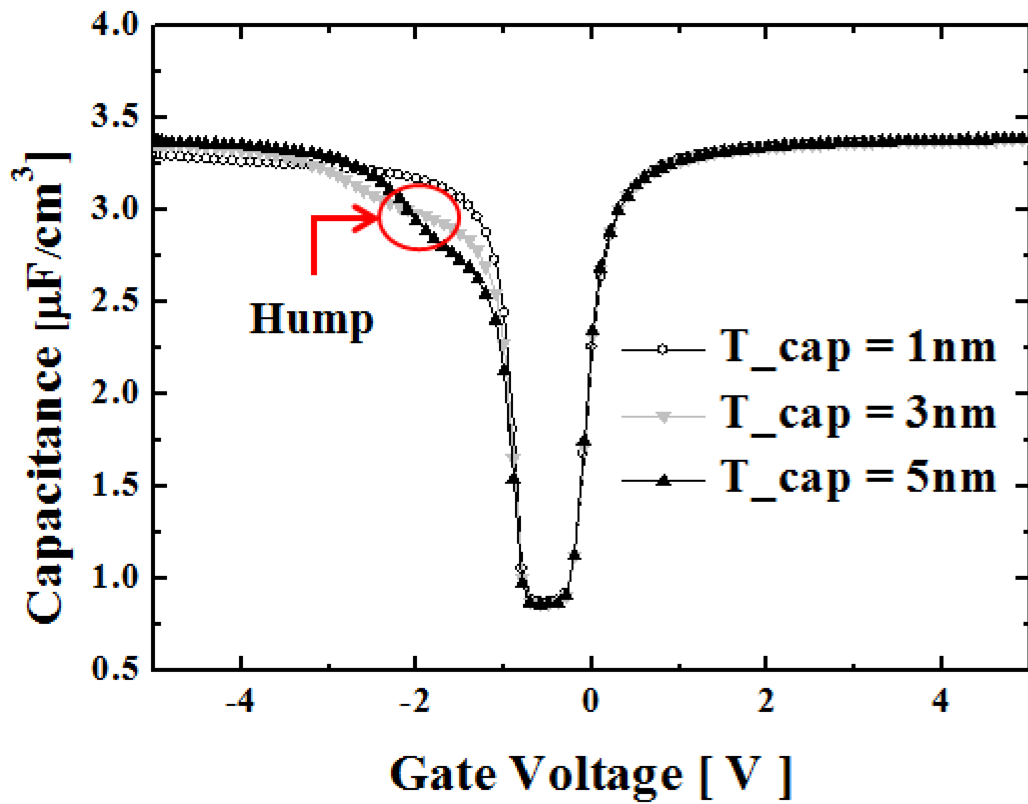


Fig. 3.1. C–V curve of TFET with n-type substrate with different thickness of

Si capping layer.

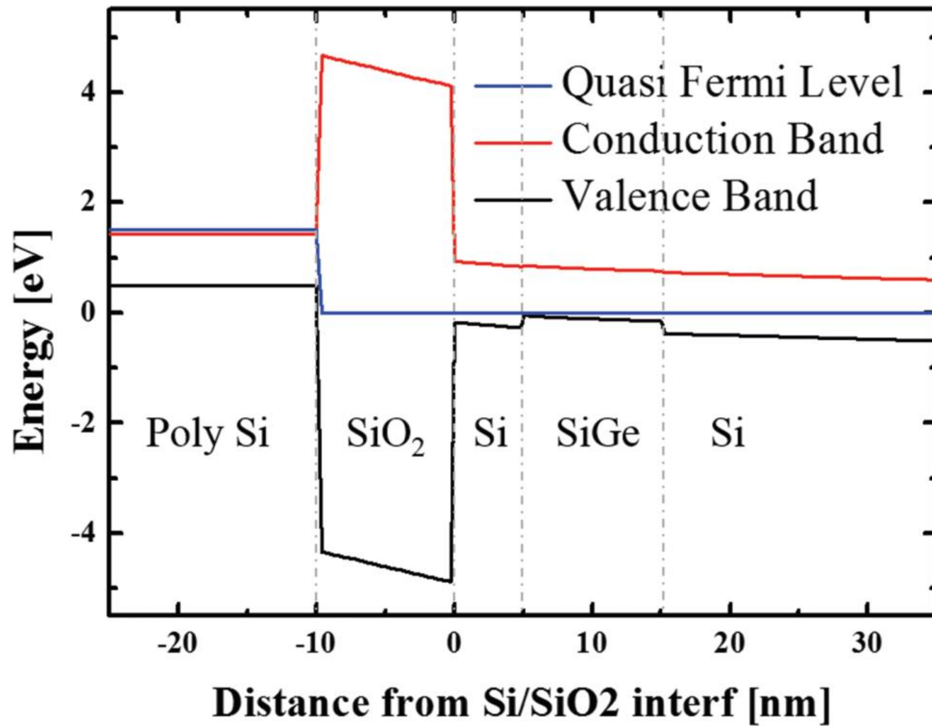


Fig. 3.2. Band diagram of TFET with n-type substrate when the thickness of Si capping layer is 5 nm.

3.2. Apparent Carrier Concentration

N_{app}, the apparent carrier concentration, takes into account the contributions from all types of electrically active carriers, including both fixed and mobile charges. The N_{app}–V_G curve can be calculated from the C–V value.

$$\frac{1}{N_{\text{app}}(V)} = \frac{q\varepsilon_{\text{Si}}}{2}\frac{\delta(1/C(V)^2)}{\delta V}$$

The absolute value of the apparent carrier concentration is plotted as a function of the gate voltage in Fig 3.3. The two type of threshold voltage can be extracted from N_{app}–V_G curve.

3.3. Two Type of Threshold Voltage

The threshold voltage can be extracted from the N_{app}–V_G curve. V_{SiGe} and V_{Si} denote the threshold voltages of the SiGe channel and the Si capping layer, respectively. At V_{SiGe}, the sign of the apparent carrier concentration is reversed because the inversion of the channel starts. Moreover, V_{Si}, which is the voltage of the Si capping layer inversion, can be extracted from the local maximum in the inversion region. V_{SiGe} and V_{Si} for a 5 nm Si capping layer are −0.50 V and −1.60 V, respectively. Correspondingly, V_{SiGe} and V_{Si} with 3 nm and 1 nm Si capping layers can be extracted in a similar manner.

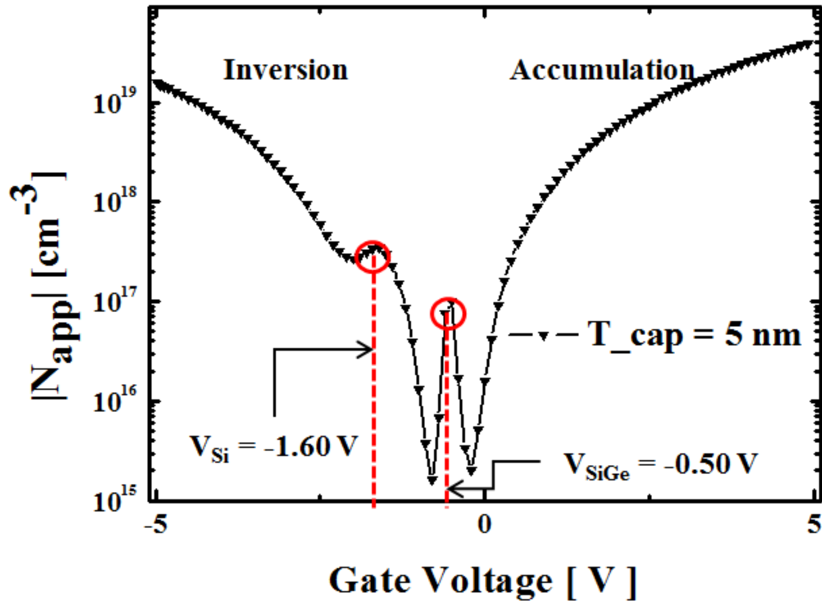


Fig. 3.3. N_{app}–V_G curve of TFET with 5 nm Si capping layer.

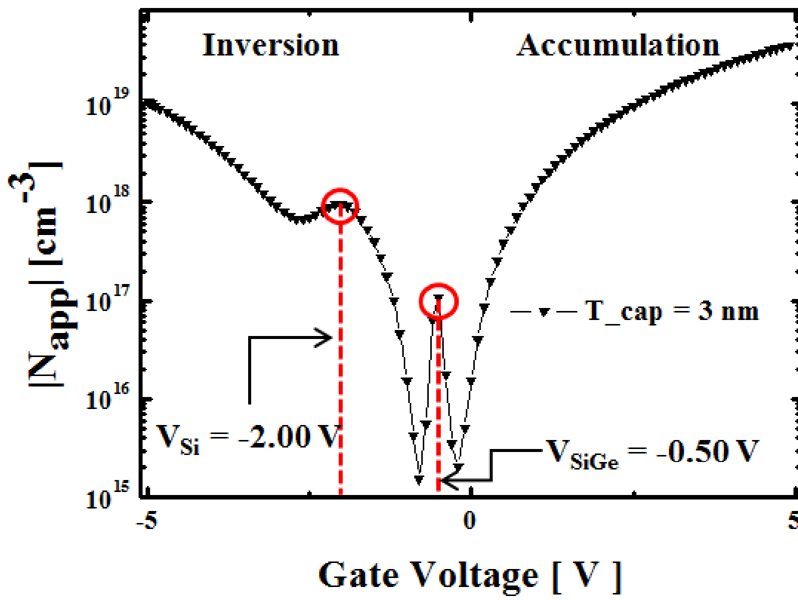


Fig. 3.4. N_{app}–V_G curve of TFET with 3 nm Si capping layer.

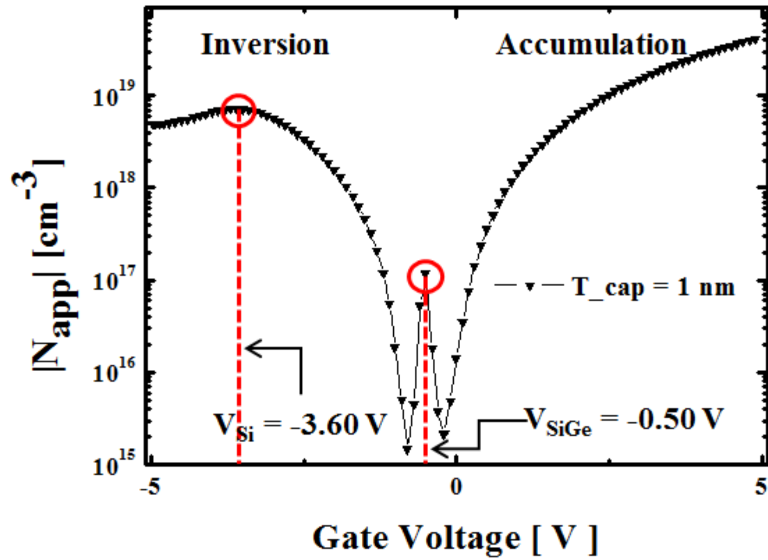


Fig. 3.5. N_{app}–V_G curve of TFET with 1 nm Si capping layer.

3.4. Approximate the Thickness of Si Capping Layer with C-V characteristics

To determine the approximate thickness of the Si capping layer, the N_{app}–x_{charge} curve should be plotted. The depletion width, x_{charge}, can be calculated by

$$x_{charge} = \varepsilon_{Si}\left(\frac{1}{C(V)} - \frac{1}{C_{ox}}\right).$$

The absolute value of the apparent carrier concentration is plotted as a

function of the depletion width in Fig 3.6. In the inversion region, there are three peaks (from the left to right) corresponding to:

(a) the accumulation of holes at the interface between the SiO2 and the Si capping layer, (b) the accumulation of holes at the interface between the Si capping layer and the SiGe channel, and (c) the maximum depletion depth.

The thickness of the Si capping layer can be extracted from the second peak because the second peak refers to the inversion at the interface between the Si capping layer and the SiGe channel. From the N_{app}–x_{charge} curve, the approximate thickness of the 5 nm Si capping layer is 7.25 nm. Similarly, the approximate thicknesses of the 3 nm and 1 nm Si capping layer are 4.21 nm and 1.56 nm, respectively (Fig. 3.7, Fig. 3.8). These results indicate that the approximate thickness is greater than the thickness of the Si capping layer.

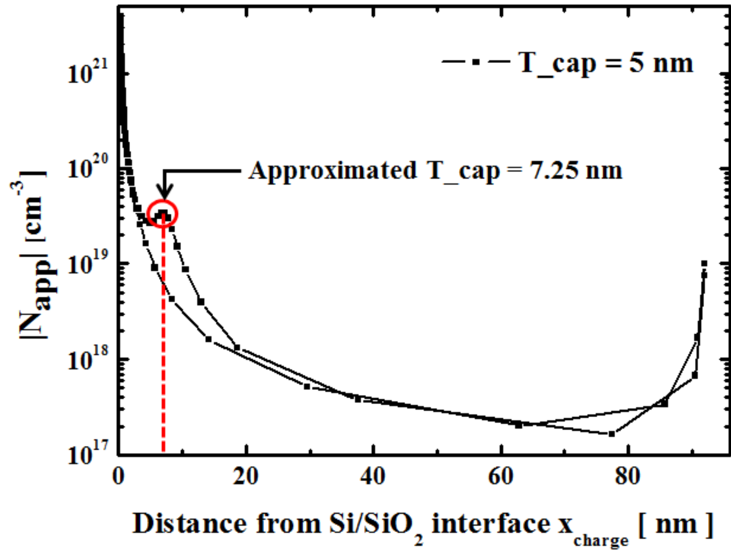


Fig. 3.6. N_{app}–V_G curve of TFET with 5 nm Si capping layer.

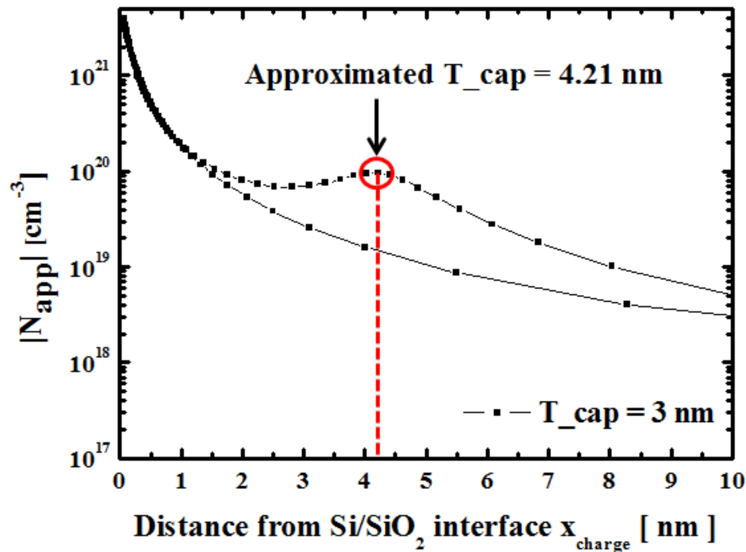


Fig. 3.7. N_{app}–V_G curve of TFET with 3 nm Si capping layer.

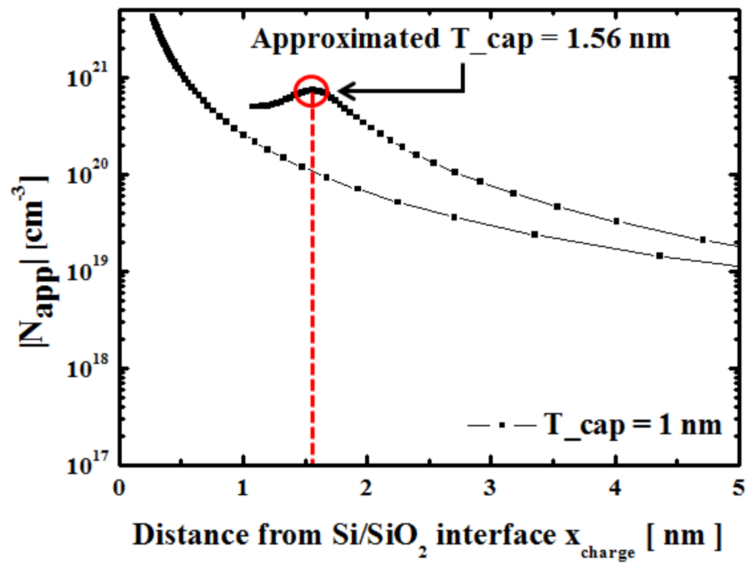


Fig. 3.8. N_{app}–V_G curve of TFET with 1 nm Si capping layer.

4. Modify the Thickness of Si Capping Layer with Centroid Effect

4.1. Introduction

There is a difference in the hole inversion distributions between a TFET and a MOS capacitor due to the source/drain region. While the hole distribution of a TFET with an n-type substrate is non-uniform in a direction lateral to the channel, the hole distribution of the MOS capacitance is uniform in an inversion state (Fig. 4.1). In a TFET with an n-type substrate, a p-type drain makes the hole supply more efficient. Therefore, a hole inversion state can more easily arise near the drain. Thus, at the interface between the SiGe channel and the Si capping layer, the simulation result shows a higher hole

density as the distance from the drain narrows. On the other hand, the hole density on the source side is lower owing to the n-type source. For this reason, a TFET with an n-type substrate and MOS capacitor have different C–V characteristics.

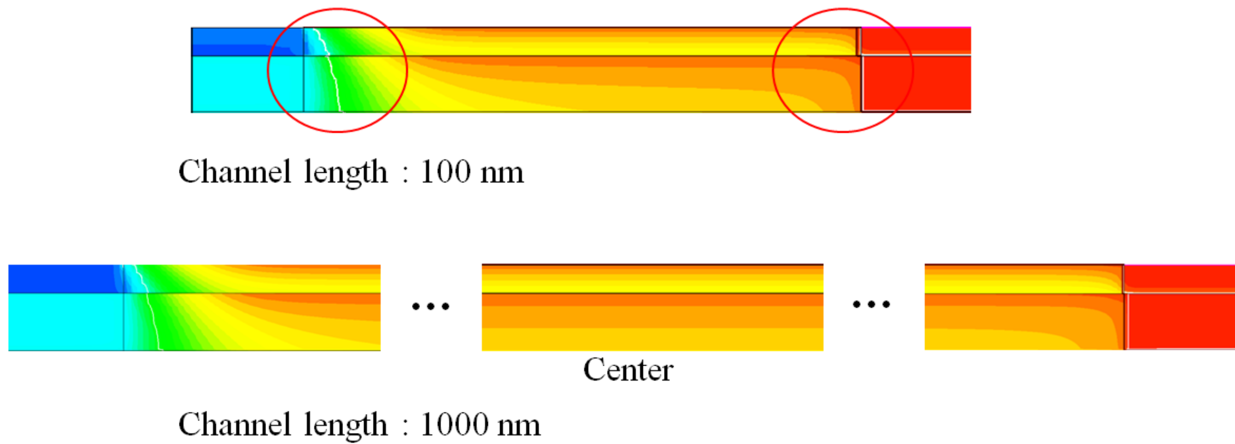


Fig. 4.1. Hole distribution of TFET with 100 nm channel in lateral direction (up). Hole distribution of TFET with 1000 nm channel in lateral direction (down).

4.2. Hole Centroid in the Si Capping Layer

Given that the centroid of the hole distribution during the inversion and accumulation states does not appear precisely at the physical interface, the centroid of the hole distribution should be considered when amending the

approximation. Because it is difficult to calculate the centroid through a simple method, the peak of the carrier density (centroid) is calculated using a simulation tool. The definition of the centroid is as follows:

$$x_{\mathrm{av}} = \frac{\int x p(x, V_{\mathrm{G}})\, dx}{\int p(x, V_{\mathrm{G}})\, dx}$$

Because the centroid of the hole distribution is a function of the gate voltage, it can be calculated at each gate voltage and the corresponding x_{av}–V_G curve can be plotted, as shown in Fig. 4.2. The centroid at V_{Si} is necessary because the approximate thickness of the Si capping layer is extracted when the gate voltage is V_{Si}. The centroid of the hole distribution can be identified at V_{Si} in each case from the x_{av}–V_G curve. Through this method, the centroids

of the 5 nm, 3 nm, and 1 nm Si capping layers at V_{SiGe} are 2.05 nm, 1.04 nm, and 0.49 nm.

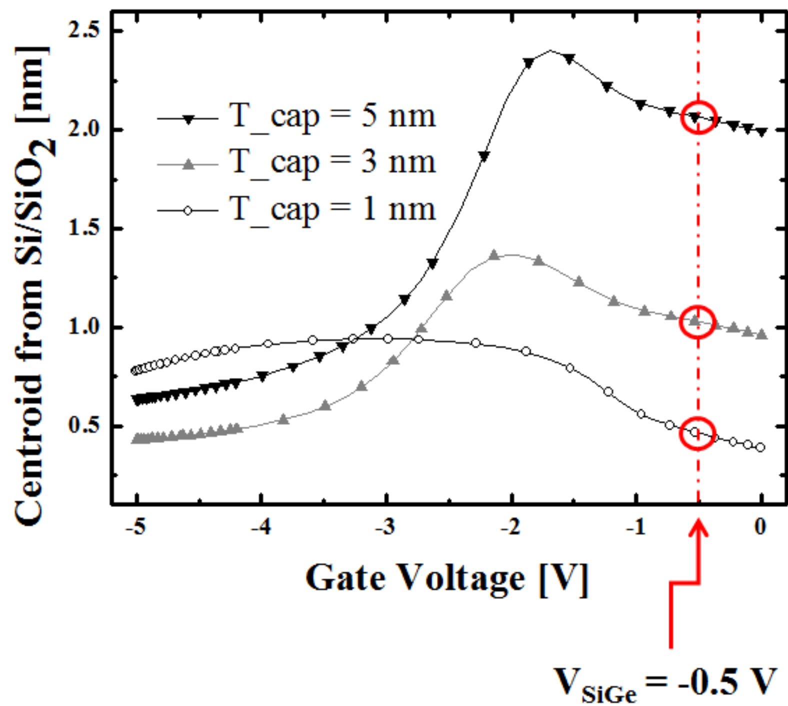


Fig. 4.2. Hole centroid position from Si/SiO2 with different thickness of Si capping layer.

4.3. Modified Thickness of Si Capping Layer

By subtracting the approximate thickness of the Si capping layer and the centroid at VTS, the modified thickness of the Si capping layer is calculated. In this case, the modified thicknesses of 5 nm, 3 nm, and 1 nm Si capping layer are 5.20 nm, 3.17 nm, and 1.07 nm in Table 4.1. Table II presents a summary of the data results in this work. Later, we will apply these results to the processed TFET with the n-type substrate.

Table 4.1 Parameters used in the simulation.

Parameters	5 nm	3 nm	1 nm
V_{SiGe} (V)	-0.50	-0.50	-0.50
V_{Si} (V)	-1.60	-2.00	-3.60
Approx. Thick. (nm)	7.25	4.21	1.56
Centroid (nm)	2.05	1.04	0.49
Mod. Thick. (nm)	5.20	3.17	1.07

5. Conclusion

In this thesis, we investigated the C–V characteristics of a Si/SiGe heterojunction of a TFET with an n-type substrate to determine the thickness of the Si capping layer. Based on TCAD simulation results, we could identify the hump in the C–V curve which originates from the offset of the Si/SiGe interface. Through a calculation, we could extract the threshold voltage and approximate thickness of the Si capping layer from the N_{app}–V_G and N_{app}–x_d curve which differs from the C–V curve. In addition, we could determine the modified thickness of the Si capping layer when considering the effect of the centroid.

References

[1] C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, and S. Mantl, Solid-State Electronics 53, 1126, 2009.

[2] K. Boucart and M. I. Ionescu, IEEE Transactions on Electron Devices 54, 4, 2007.

[3] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, Appl. Phys. Lett. 91, 053102, 2007.

[4] H. W. Kim, J. H. Kim, S. W. Kim, M. Sun, E. Park, and B. Park, Japanese Journal of Applied Physics: Regular Papers 53, 06JE12-1, 2014.

[5] A. Sareen, P. Lundgren, M. A. Yousif, and S. Bengtsson, J. Appl. Phys. 96, 3545, 2003.

[6] K. Iniewski, S. Voinigescu, J. Atcha, and C. A. Salama, Solid-State Electronics 36, 775, 1993.

[7] S. P. Voinigescuong, K. Iniewski, R. Lisak, C. A. T. Salama, J.-P. NoeL, and D. C. Houghton, Solid-State Electronics 37, 1491, 1993.

[8] F. Lu, S. K. Zhang, Z. M. Jiang, J. Qin, D. Z. Hu, and X. Wang, Journal of the Korean Physical Society 24, S73, 1999.

[9] J.-Y. Wei, S. Maikap, M. H. Lee, C. C. Lee, and C. W. Liu, Solid-State Electronics 50, 119, 2006.

[10] J. Sune, P Olivo, and B. Ricco, IEEE Transactions on Electron Devices 39, 1732, 1992.

[11] J. B. Roldan, F. Gamiz, J. A. Lopez-Villanueva, P. Cartujo, and A. Godoy, IEEE Transactions on Electron Devices 48, 2447, 2001.

초 록

SiGe 채널 위의 Si capping layer는 SiGe 채널과 게이트 절연막 사이의 경계 특성을 개선하기 위하여 중요하다. 그러므로 Si capping layer가 포함된 디바이스는 그것들의 전기적 특성을 이해하기 위하여 반드시 분석되어야 한다. 이 논문에선 strained Si/SiGe 헤테로 TFET을 빠르고 비파괴적인 방법으로 분석하기 위하여 전기용량-전압 측정 데이터를 사용하였다. Si/SiGe 헤테로 TFET의 C-V 분석 방법은 TCAD 시뮬레이션을 이용하여 개선된다. 이러한 C-V 분석을 통하여, 소자의 중요한 파라미터인 단층의 두께와 문턱전압과 같은 데이터를 추출할 수 있다

주요어 : 터널링 전계효과 트랜지스터 (TFET), 문턱 전압, 실질 수송자 농도, 전기 용량, Si 피복층, 중심

Tunnel Field Effect Transistor, Threshold Voltage, Apparent Carrier Concentration, Capacitance, Si Capping Layer, Centroid

학 번: 2014-21725