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Ph.D. Dissertation

Design and Fabrication of AlGaN/GaN-on-Si FETs for Ka-band MMICs

Ka-대역 MMICs를 위한 AlGaN/GaN-on-Si FETs의 설계 및 공정에 관한 연구

February 2018

Graduate School of Electrical and Computer Engineering

Seoul National University

Dong-Hwan Kim

Abstract

As the power amplifiers (PAs) become increasingly important for use in communication of wireless and satellite, and military applications, a high operation frequency bands are highly desired for microwave transistors and monolithic microwave integrated circuits (MMICs) due to the tremendous usage of bandwidth. Since the performance of current Si, GaAs, or InP technology does not satisfied next-generation, high-power amplifiers with their inherent material limitation, GaN based materials have been intensively explored for past few decades in the aspects of their excellent properties, such as wide bandgap and high electron saturation velocity. Especially, GaN-on-Si technology is of particular interest to radio frequency (RF) industry because of the potential for low cost and the large volume of wafer production.

This work firstly introduced the overall key process technologies of GaN millimeter-wave (mmw) device including ohmic contact, isolation, passivation, and gate process. For passivation process, we have decided the thickness of dielectric layer considering both mitigations of peak electrical field at the gate edge and degradation of small-signal characteristics due to an increase of parasitic capacitances. Also, gate structure was taken account of minimizing parasitic capacitances with short gate field-plate. The gate metal stack for millimeter-wave applications was suggested nickel and gold with molybdenum as diffusion barrier metal to achieve good thermal stability on RF performances.

The final goal of this work was improvement of output power of Ka-band GaN HEMT device and MMIC PA using the proper AlGaN/GaN heterostructure on Si substrate with several technologies that dealt with modifying GaN epitaxial structure, applying high-k dielectric on passivation process, and employing recessed metal-insulator-semiconductor (MIS) structure on gate instead of metal-semiconductor (Schottky) based on above overall processes of GaN mmw device. Using AlGaN/GaN heterostructure with undoped GaN buffer demonstrated better small-signal and large-signal characteristics at 18 GHz load-pull measurement which indicated the direction of epitaxial structure for mmw application. The MIS gate structure with high-k dielectric satisfied low gate leakage current and low current collapse at a time resulted in higher output power than the conventional Schottky gate structure.

To demonstrate 26.5~27 GHz GaN MMIC PA, we also optimized each fabrication process of passive elements including NiCr thin film resistor (TFR), metal-insulator-metal (MIM) capacitor, and coplanar waveguide (CPW) transmission line. Finally, the fabricated MMIC PA with employing thin SiN_x interface layer for dual MIS structure, ion implantation for device isolation, and field-plated Y-gate for low gate resistance and parasitic capacitance achieved higher output power without degradation of gain at higher operation voltage than conventional Schottky gate at higher center frequency. The front process technologies we developed in this work showed the potential of GaN-on-Si technology for mmw application with watt-level output power. The packaging with good thermal management and design

method of MMIC for the higher output power and PAE (power-added efficiency) might improve the performance of GaN-on-Si MMIC PA.

Keywords: AlGaN/GaN HEMTs, GaN epitaxial layer, gate structure, passivation, high-k dielectric, metal-insulator-semiconductor (MIS), Ka-band, out power, power amplifier (PA), monolithic microwave integrated circuit (MMIC)

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Chapter 1. Introduction

1.1 Backgrounds

Although the silicon (Si) technology has been the main stream of semiconductor industry for many decades [1], various compound materials have been investigated to surpass and overcome the limitation of Si material [2, 3] in specific area. For instance, SiGe, GaAs, and InP based transistors have been studied and developed for RF applications with the frequency range from few GHz to several hundred GHz owing to the higher electron mobility than Si [4-6]. Similarly, SiGe, InGaAs, or InAlAs have been regarded as the materials of logic devices by complementing the critical point of down scaling technology [7, 8].

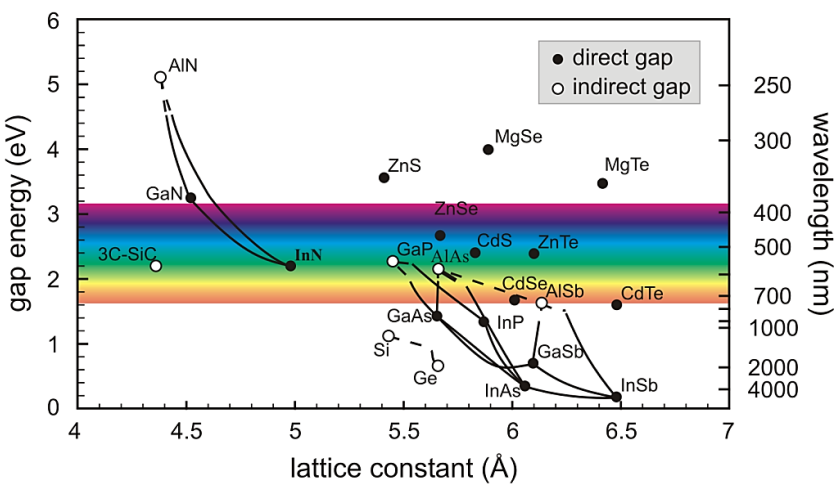

Fig. 1.1 Lattice constants and bandgap energies for compound semiconductor materials.

However, these materials have comparatively narrow band-gap so that they are not suitable for high power and high temperature applications. Among the Ⅲ-Ⅴ group, gallium nitride (GaN) has the larger band-gap which make it better to be employed at high power and high temperature applications. Actually, GaN has been developed with SiC to outperform Si heterojunction bipolar transistors (HBTs) or bipolar diodes as the breakthrough technology in high power devices [9-12]. The material properties of GaN are exhibited in Table. 1.1 with other semiconductors for high-voltage applications. Due to high critical breakdown field and high electron mobility of GaN and high thermal conductivity of SiC, these materials demonstrate high-speed switching, high breakdown voltage, low loss, and high operating temperature compared to Si. Low loss and high-speed characteristics make them to save energy and reduce the size of electronics. To be specific, GaN devices are positioned up to medium-voltage applications and SiC devices are applied to much higher voltage applications. Also, GaN are widely used for light emitting diodes (LEDs) and detectors with GaAs due to its direct band-gap property [13].

Table 1.1 Comparison of physical properties between silicon and wide bandgap materials.

	Si	**4H-SiC**	**GaN**	**AlN**
Crystal structure	Cubic (Diamond)	Hexagonal (Wurzite)	Hexagonal (Wurzite)	Hexagonal (Wurzite)
Lattice constant [Å]	5.4	3.1	3.2	3.1
Bandgap E_g [eV]	1.11	3.26	3.42	6.1
Critical breakdown field E_c [MV/cm]	0.3	2.2	3.3	11.7
Dielectric constant ε_r	11.8	10	9.0	8.4
Electron mobility μ_n [cm^2/Vs]	1350	700	1500~2000	1100
Saturation velocity v_{sat} [10^7 cm/s]	1	2	2.5	1.8
Intrinsic concentration n_i [cm^{-3}] @ T = 300 K	10^{10}	10^{-8}	1.9×10^{-10}	$\sim10^{-31}$
Thermal conductivity k_{th} [W/cmK]	1.5	4.5	1.3 ~ 1.5	2.5

Ⅲ-N materials including GaN, InGaN or AlGaN are grown by metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). When they are grown by MOCVD, the films have typically the [0001] orientation with the surface corresponding to the Ga-face [14] as shown in Fig. 1.2, and they shows much more smooth surface than the films grown with N-face. While the Ga-face is the industry and academic standard [15], it has been demonstrated that N-face GaN can be grown by both MBE and MOCVD using suitable nucleation steps [14], and the effect of substrate nitridation with different growth temperature on the surface roughness of N-face GaN was investigated [16]. Also it is possible to use Mg, Si-doping or In alloy to invert the polarity of Ga-face [14]. N-face GaN has some advantages on high frequency devices in terms of making the ohmic contact and maintaining the aspect ratio (L_G/$d_{channel}$) without the decrease of 2DEG charge [15] due to its opposite heterostructure. However, the applications of N-face devices are not sure yet because they have demonstrated less reliable characteristics than Ga-face, such as rough surface and chemical reactions [17].

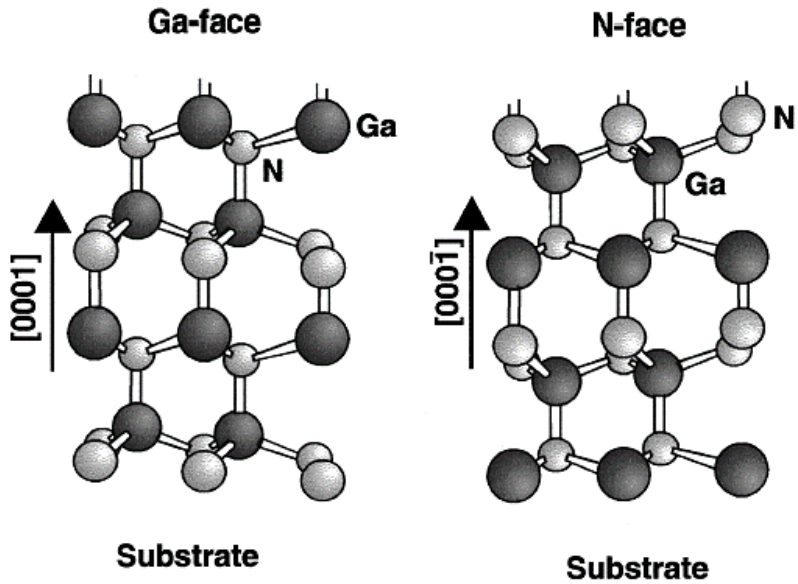

Fig. 1.2 Crystal structure of wurzite Ga-face and N-face GaN [17].

GaN devices are typically used by forming heterostructure with AlGaN so that two-dimensional electron gas (2DEG) can be generated as a channel. GaN exhibits the spontaneous polarization which can cause electric field up to 3 MV/cm as same with other Ⅲ-N crystals, and strain in pseudomorphically grown AlGaN/GaN or InGaN/GaN heterostructures can cause an additional piezoelectric field of about 2 MV/cm [17] which is related to the mismatch of the lattice constants resulted in elastic distortion of crystal lattice. These high polarizations produce high interface charge densities in GaN-based quantum well structure. The spontaneous polarization along the c-axis of the wurzite crystal and the amount of piezoelectric polarization in the direction of the c-axis can be defined by

$$\mathbf{P}_{\mathrm{SP}} = P_{SP}\mathbf{z} \ , \ \mathbf{P}_{\mathrm{PE}} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{\mathrm{C}_{13}}{\mathrm{C}_{33}}\right)$$

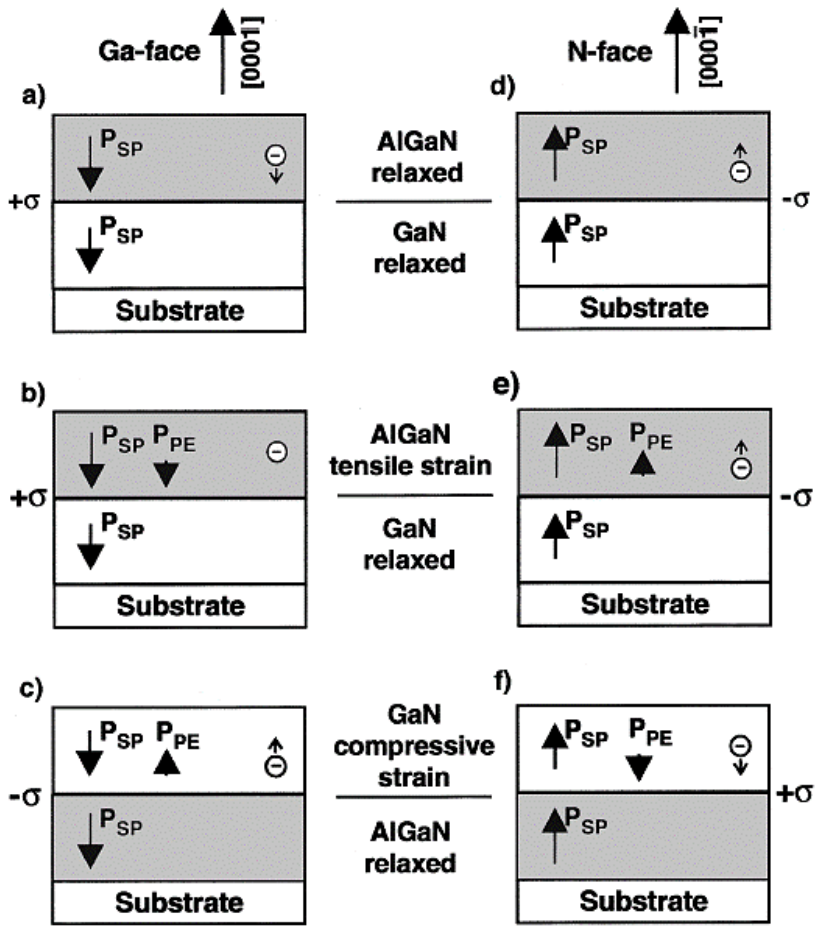

Fig. 1.3 Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures [17].

The spontaneous polarization for GaN was reported to be negative and the piezoelectric polarization of AlGaN/GaN or GaN/AlGaN heterostructure is negative for tensile and positive for compressive strained barriers, respectively. So the top layer will be tensile strained when the piezoelectric and spontaneous polarization are parallel and compressive strained when the piezoelectric and spontaneous polarization are antiparallel. By increasing the

Al-content of the AlGaN barrier, the spontaneous and piezoelectric polarization are increasing. Finally, free electrons tend to compensate the high positive polarization induced sheet charge which is called 2DEG at the AlGaN/GaN interface for Ga-face or at the GaN/AlGaN interface for N-face [17]. And the thicker AlGaN barrier makes the higher sheet carrier density [18].

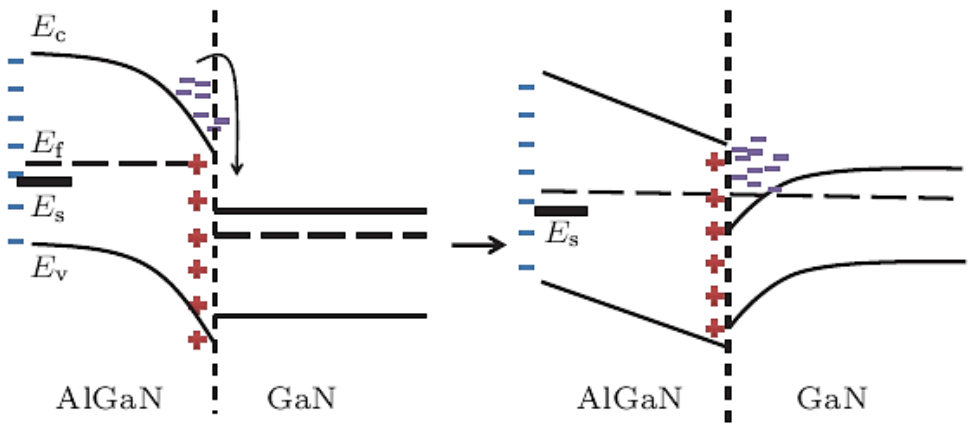

Fig. 1.4 Energy band of an undoped AlGaN/GaN heterostructure after the two layers contact. Electrons will flow into the GaN side and accumulate at the AlGaN/GaN interface resulted in forming 2DEG [19].

1.2 GaN for RF Applications

Saving the energy has been an important issue in recent technologies so that high power efficiency and low power loss are required at power devices [20]. There are various approaches for saving the energy from considering the better materials to developing the power conversion technology in the module. In this regard, power efficiency is also essential in RF applications to communicate a large amount of information with high speed and high accuracy. For example, 5th generation (5G) mobile communication

technology requires much bigger traffic volume with fast transmit/receive that must have low path loss and low energy consumption [21]. The main component with large energy consumption in RF module is a power amplifier that releases a lot of heat [22].

Table 1.2 Physical properties of semiconductor materials for high-frequency application.

	E_g [eV]	E_c [MV/cm]	μ_n [cm^2/Vs]	v_{sat} [10^7 cm/s]	k_{th} [W/cmK]
Si	1.1	0.3	1350	1	1.5
SiGe	0.7~1.1	0.2	3000	-	0.083~0.1
GaAs	1.4	0.4	8000	0.8	0.5
InP	1.3	0.5	10000	2.2	0.68
GaN	3.4	3.3	1500~2000	2.5	1.5

The semiconductor materials for RF applications are Si, SiGe, GaAs, InP, and GaN in these days. Table 1.2 and Table 1.3 show their material properties and suitable applications. As we mentioned above, GaN has the large band-gap and high saturation electron velocity which make to operate at high frequency with high operation voltage compared to other materials [23, 24]. Si-based RF device is still widely used at a low frequency band (< 3 GHz) and GaAs or InP based RF devices can be used at mmw band with low operation voltages. However, the low breakdown fields of these materials have been limiting their RF performance in terms of output power and power density owing to the low operation voltage. GaN-based device demonstrates comparable frequency-gain characteristic even at high operation voltage

resulted in high output power (power density). So the outstanding performance of GaN RF devices can make them to be employed at widespread frequency bands and to help for reducing the chip size. Actually, the GaN RF devices already have been employed in base stations and military applications with the considerable level of device technology [25, 26]. The superior power density of GaN, compared with Si LDMOS, will help this wide band-gap technology to dominate the RF power amplifier base station market [27]. Although each semiconductor material has much more suitable applications, GaN can be developed for various frequency bands. As the usage of bandwidth and the required RF power density increase, not only the general AlGaN/GaN heterostructure but also AlN/GaN or AlGaN with indium (In) compound heterostructure which can demonstrate much higher electron mobility due to the larger polarization have been also investigated to overcome the limitation of conventional materials at mmw applications [28, 29].

Table 1.3 Various semiconductor materials for RF applications and their advantages [source: MACOM].

	Radar	**Military**	**Wireless**	**Optical**	**Wired broadband**
Si	High peak power	High power, high linearity			
SiGe	Low noise, high frequency, high integration		Low noise, high frequency, high integration	High speed, low noise, high integration	High integration
GaAs	Low noise, high frequency	Low noise, high frequency	Low noise, high frequency,	High voltage, low power,	High linearity

			high linearity	high linearity	
InP				High speed, high voltage, low power	
GaN	High frequency, high power, high efficiency	High frequency, high power, high efficiency	High frequency, high power, high efficiency		High linearity, high efficiency

1.3 Substrates for GaN Growth

Because it is hard to grow thick-GaN bulk layer [30-32], employing substrate material is one of the key factors in GaN devices. As shown in Table. 1.4, there are several materials for the substrates of GaN devices. In many cases, semi-insulated (S.I) SiC has been used for GaN RF applications owing to the lower defect density and higher thermal conductivity [23, 33]. GaN and SiC exhibit relatively small lattice mismatch so that the GaN-on-Si wafer has low defect density which is directly associated with trapping phenomenon and leakage current path. Thus, the devices using GaN-on-SiC wafers demonstrate higher frequency-gain characteristic and higher output power density. However, the GaN RF devices cannot totally substitute conventional Si-based devices yet because the GaN-on-SiC wafers cost high [33, 34]. In this regard, Si substrate for GaN growth has a large potential for cost reduction to be much more commercialized. The Si substrate is used to be low-resistivity (LR) and high-resistivity (HR) with (111) direction and the HR-Si substrate must be employed in high-frequency devices to minimize the substrate loss, even though it is more expensive than LR-Si substrate and

lossier than S.I SiC substrate [35]. Also, few studies reported that the microwave characteristics of GaN-on-Si (LR) devices and bowing problem of HR Si substrate which limits the GaN-on-Si technology moving towards larger silicon substrate [36-38]. GaN-on-Si technology can be compatible with Si CMOS process. Using this technology, several groups demonstrated the integrated devices with Si CMOS, GaAs HEMT, or InP HEMT by wafer bonding or selective growth process [39-43], and these results made GaN-on-Si technology be more attractive. Some investigations predicted that the GaN RF device market may be divided with GaN-on-Si and GaN-on-SiC considering their applications, and the portion of GaN-on-Si devices in that area will gradually increase in the near future. The feasibility of widely employing GaN-on-Si for RF device has been estimated that based on the comparison of thermal conductivity. In spite of the difference of thermal conductivities between Si and SiC, their capabilities of thermal managing are not that far at the operation temperature of actual devices [44]. Recently, GaN wafers have been already developed with the size of 12 inches Si substrate and wafer processing is also available with 8 inches [45, 46]. The freestanding-GaN wafer is available for the size of 2 inch yet and its cost is extremely high [47].

Further, some groups reported about GaN-on-Diamond technology which has the matchless thermal conductivity compared to other substrate materials, even SiC, to improve the output power density remarkably [48-53]. Its thermal conductivity is varied in large range according to the quality of diamond and nucleation layer between GaN and diamond, and generally, there are two approaches of wafer bonding or chemical vapor deposition (CVD) growth of diamond at the backside of AlGaN/GaN heterostructure after removing original substrate.

Table 1.4 Physical properties of various materials for the substrate of GaN devices.

	Si	**SiC**	**Sapphire**	**GaN**	**Diamond**
Defect density [cm^{-2}]	10^9	~10^7	10^8	10^3~10^6	-
Lattice mismatch [%]	17	3.3	13.3	0	89
CTE mismatch [%]	54	25	34	0	81
Thermal conductivity [W/cmK]	1.5	4.9	0.35	1.5	15~30
Electrical resistivity [Ωcm]	2.3×10^5	10^4~10^6	10^{17}	10^6	10^{13}~10^{16}
Available wafer size	12	6	8	~2	6
Cost	Low	High	Medium	Very high	Extremely high

CTE : coefficient of thermal expansion

1.4 Research Aims

In this research, typical AlGaN/GaN HEMT-on-Si substrate is widely investigated for high-frequency application, especially for Ka-band. A lot of technical issues must have been studied including ohmic contact, Schottky contact, gate formation, passivation, epitaxial growth, and backside via because the all factors are critical in RF device to achieve both the high frequency-gain and output power. We optimized overall process details and developed the front process on the device with 0.15 μm gate. Unlike a long channel power transistor, there is the trade-off relationship between the reliability of the device and the frequency-gain characteristic so that we tried to consider each process of the device, such as the shape of gate, the thickness of passivation, even GaN epitaxial layer. In addition, we employed the MIS structure which has been regarded as the promising direction to complement the inferior characteristics of GaN-on-Si and realize the comparable RF performances with the GaN-on-SiC device. These device technologies will be developed to improve operating voltage, maximum drain current, and operating frequency that are the main factors of limiting the output power of GaN microwave devices (Fig. 1.5).

The final goal of this work is to demonstrate Ka-band MMIC PAs using AlGaN/GaN recessed MIS-HEMT-on-Si substrate with improved power characteristics by employing the investigated and optimized device processes, and suggest the suitable direction of GaN-on-Si RF technology. The 2-stage common source PA is designed from the modeling of the fabricated active and passive devices. Some differences on fabrication process are applied to each MMIC and their characteristics are compared in terms of output power, and finally the time dependent on-state reliability is compared to conventional GaN-on-Si MMIC with Schottky gate structure.

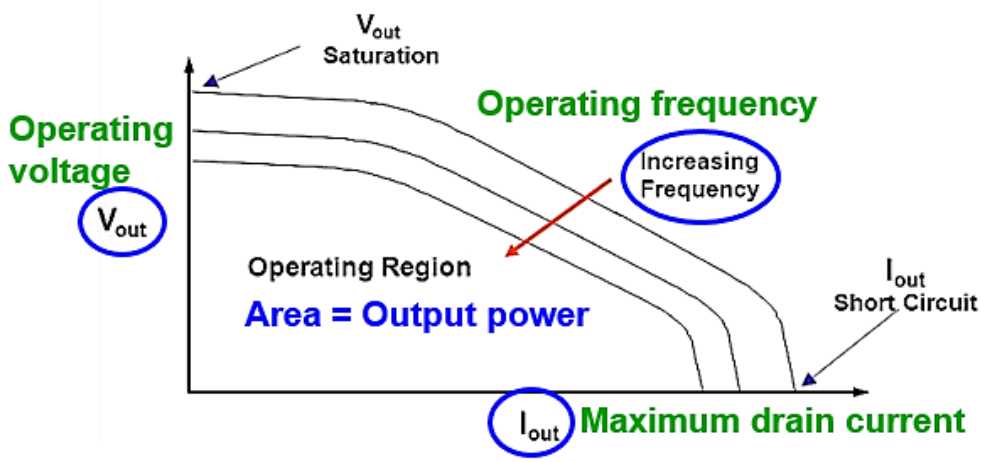

Fig. 1.5 Limiting factors of output power of GaN microwave devices that should be improved.

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Chapter 2. Overall Process Technologies of GaN-on-Si Millimeter-wave Devices

2.1 Introduction

This chapter introduces overall process flow of GaN HEMTs and important factors at each process step for high RF performance. Wafer cleaning and surface protection, ohmic contacts, isolation, surface treatment and passivation, gate contacts, and thick pad contacts with the air-bridge process were performed progressively. The researches of this chapter were focused on general optimization of detailed processes to achieve low ohmic contact resistance, low surface leakage current after mesa isolation process, and low parasitic capacitances related to both thickness of passivation and gate structure. Also, thermally stable gate metal stack with Mo insertion layer in terms of small-signal characteristics was employed on millimeter-wave devices.

2.2 Device Fabrication Processes

Entire fabrication was progressed in the Inter-university Semiconductor Research Center (ISRC) in Seoul National University. In this section, we will describe our process flow of GaN HEMTs devices in large scheme and some key factors that we should take care at each process step.

2.2.1 Process Flow

The general GaN HEMTs front-end process flow is shown in Fig. 2.1. After wafer cleaning with solvent and acid, a SiN_x film was pre-passivated using CVD in order to protect the GaN surface during high-temperature ohmic annealing [1, 2]. Next, recessed ohmic contacts were formed by SF_6 plasma for SiN_x opening using reactive ion etching (RIE) [3] and BCl_3/Cl_2 plasma for GaN/AlGaN shallow etching using inductively coupled plasma (ICP) - RIE [4, 5] followed by Si/Ti/Al/Mo/Au metallization and rapid thermal annealing (RTA) in N_2 ambient [6, 7]. Mesa isolation was carried out using BCl_3/Cl_2 plasma etching for general device isolation. In order to improve the interface condition between the passivation film and GaN surface, the pre-passivated SiN_x film was removed by low damage SF_6 plasma etching and a fresh SiN_x film was subsequently re-deposited at 400 °C chuck temperature with buffered oxide etchant (B.O.E) 30:1 wet treatment for 40 sec. SF_6 plasma etching and treatment were optimized to reduce the gate leakage current and suppress the current collapse phenomenon in our previous work [8, 9]. After the gate region was defined with a minimized gap from the source electrode by electron-beam (e-beam) lithography, Ni/Mo/Au based metal stack was evaporated for gate formation. Interconnection pad electrodes

were formed using photolithography and Ni/Au (=40/500 nm) evaporation. To make equipotential source electrodes, the thick air-bridge process was finally conducted with Ti/Au (=50/1450 nm) evaporation.

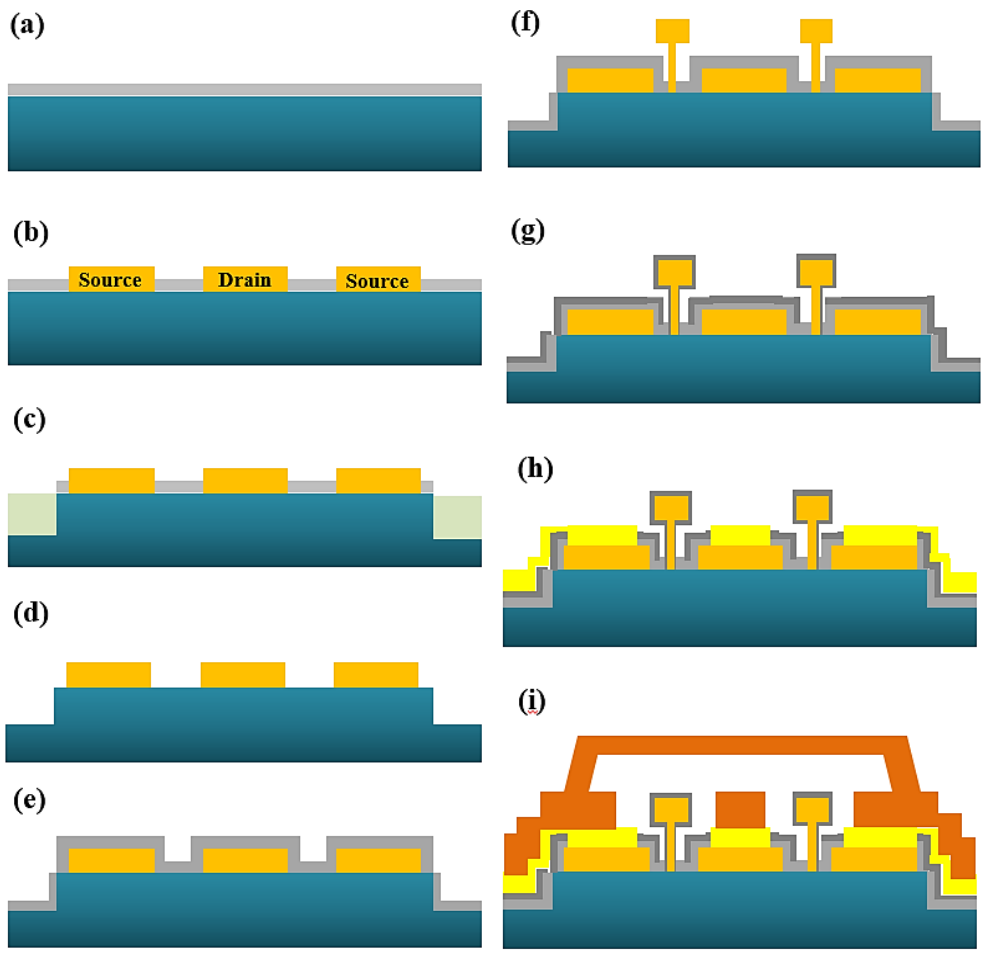

Fig. 2.1 Process flow of GaN HEMT: (a) surface cleaning and SiN_x pre-passivation (b) ohmic contact (c) device isolation (mesa etching or ion implantation) (d) damaged SiN_x removal (e) SiN_x re-passivation (f) Gate process (g) SiN_x 2nd passivation (h) ohmic open and M1 metal (i) M2 metal with air-bridge.

2.2.2 Ohmic Contact

The ohmic contact with low contact resistance (R_c) is the most basic process to get high RF performance [4]. However, it is hard to achieve the low R_c for GaN due to larger band-gap than other materials such as GaAs and InP [10, 11]. To make ohmic contact for GaN, titanium (Ti)/aluminum (Al)-based metal Schottky contact with high-temperature annealing is generally needed. Ti and Al can react with GaN and form TiN or thin AlN resulted in lowering barrier height or making direct contact with 2DEG by generation of N-vacancies under the ohmic contact [11, 12]. These N-vacancies has been introduced that occur electron tunneling through heavily bent conduction band. However, Ti and Al are sensitive to oxygen which increases their resistivities during high-temperature annealing. Thus, most of the cases adapt cap metals above the Al to suppress oxidation of the under metals, such as molybdenum (Mo) or nickel (Ni) [10, 13]. These metals also play a role as barrier metals that make gold (Au) cannot diffuse downward when high-temperature annealing is performed.

There are some results with employing shallow Si layer at the bottom of the metal stack based on above theories to make better surface morphology after high-temperature annealing and to induce doping effect into the GaN [6, 7]. As similar with this approach, we used shallow Ge layer instead of Si that also can be a dopant in GaN and estimated both of their ohmic contact characteristics. Fig. 2.2 shows the values of R_c employing Si/Ti/Al/Mo/Au metal stack with the different thickness of remained AlGaN barrier [14] and scanning electron microscope (SEM) image to confirm the edge acuity after high temperature annealing. Figure 2.3 shows the reduction of R_c and improvement of surface morphology with shallow Ge layer. But, opposite trend related with annealing temperature was observed.

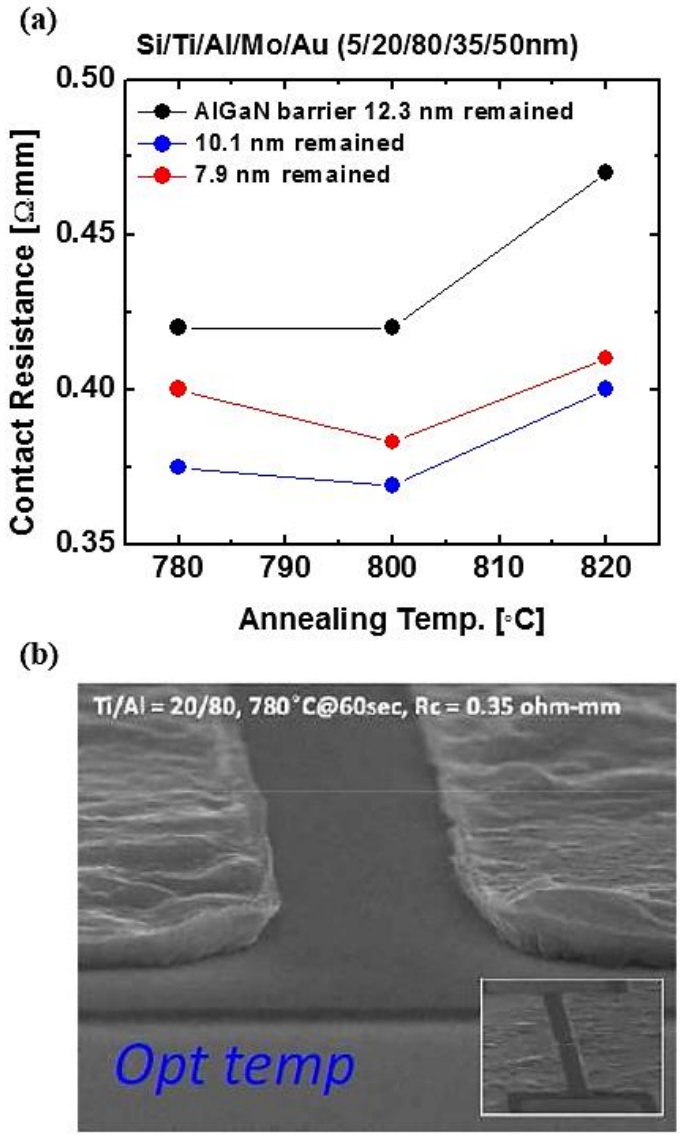

Fig. 2.2 (a) The value of contact resistances with different distance between metal contact and 2DEG channel at each annealing temperature for Si/Ti/Al/Mo/Au ohmic contact. (b) SEM image of ohmic contact with the source-drain distance of 2 μm.

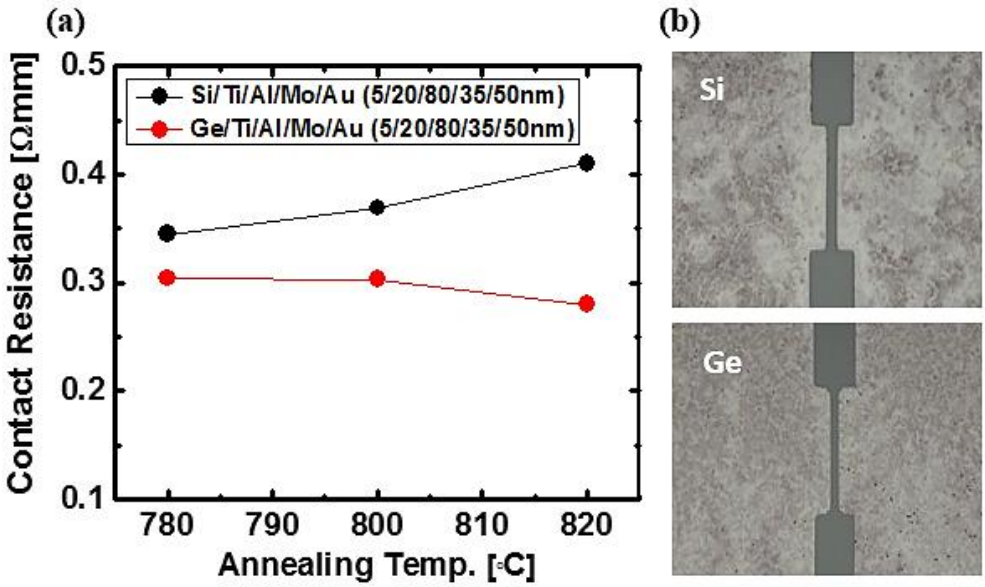

Fig. 2.3 (a) The result of Ti/Al/Mo/Au ohmic contact with thin Ge bottom layer instead of Si. (b) Microscope images of GaN ohmic contact with both Si and Ge as the bottom layers.

For several years, non-Au ohmic contact has been used for GaN HEMT devices especially at GaN-on-Si applications to integrate with Si CMOS technology [15-21]. There were some results of non-Au ohmic contact for GaN microwave devices with Au-free metal stack [22] and low-temperature annealing except for highly doped regrown layer [23, 24]. However, non-Au ohmic contact process is sensitive to achieve high current density and low R_c because the metal stack with only Ti/Al suffers from oxidation as we mentioned above.

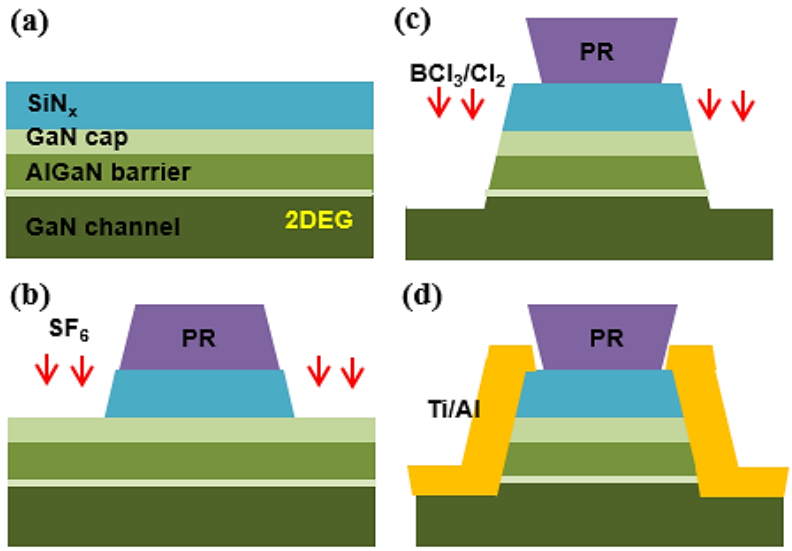

Fig. 2.4 Process flow of non-Au ohmic contact. The Ti/Al metal was directly contacted with the 2DEG channel by fully recessed etching.

We employed ohmic contact structure with fully recessed etching using BCl_3/Cl_2 low power plasma and overhang region [18] as shown in Fig. 2.4 (d). To mitigate oxidation effects, each metal source was cleaned and etched their surface, and surface treatments were mainly investigated. The fully recessed surface was GaN layer different with Au ohmic contact process with AlGaN surface so that it was better to remove surface GaO_x by using hydrofluoric acid (HF) instead of hydrochloric acid (HCl). Figure 2.5 (a) demonstrates the result of non-Au ohmic contact with different surface treatments before the metals deposition. The ohmic contact characteristics after surface treatments with HF or both HF and HCl showed high current density whereas surface treatment with only HCl showed Schottky property which was not ohmic. We achieved the value of R_c lower than 0.6 Ω·mm at Ti/Al (=60/200 nm) metal stack with 550 °C 1 min annealing at N_2 ambient. In addition, the defect density of AlGaN/GaN heterostructure impacts on low temperature ohmic process that the more defective structure can demonstrate

ohmic contact more successfully [25] which means the low temperature ohmic process depends on the quality of epitaxial layer. Although the current density and R_c characteristics were quite meaningful in comparison with the results of other groups, further investigation was needed to reduce the value of R_c as similar as the value of R_c in Au ohmic contact process for millimeter-wave application.

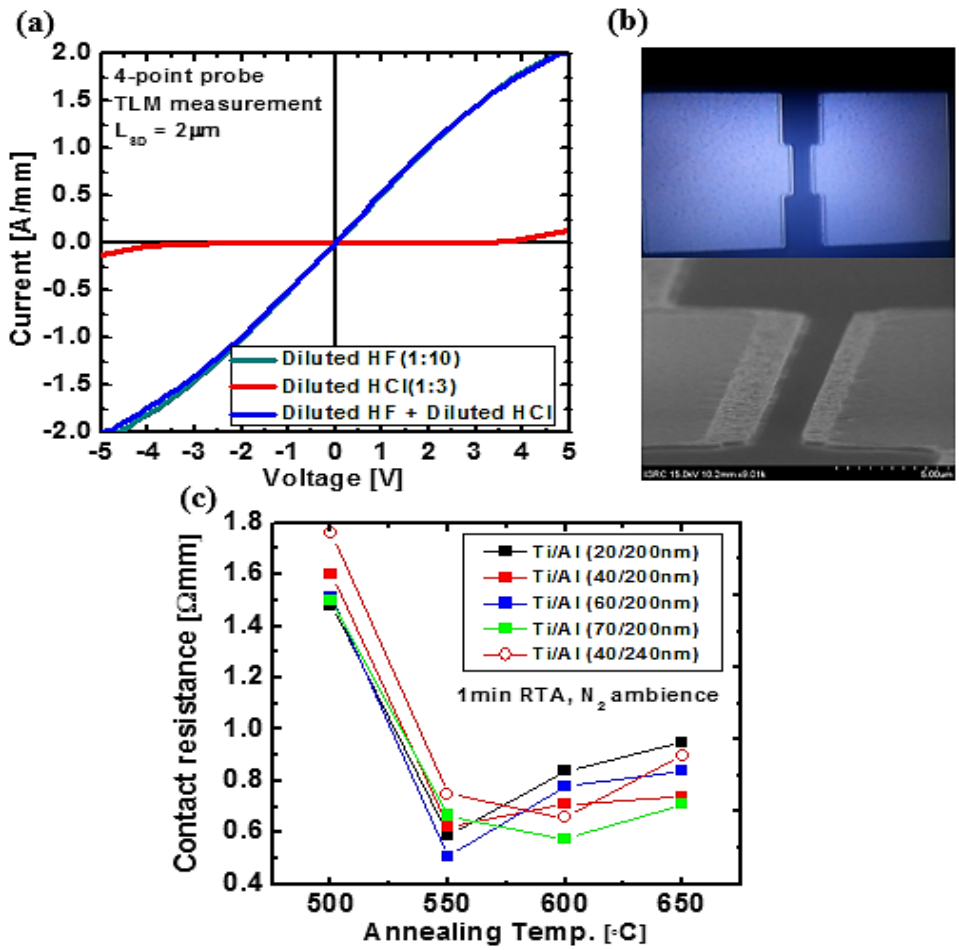

Fig. 2.5 (a) The source-drain current density with different acid surface treatment before the ohmic contact. (b) Microscope and SEM images of non-Au ohmic contact. (c) The contact resistance with various Ti/Al ratio and annealing temperature.

2.2.3 Device Isolation

Device isolation process is generally performed by mesa etching and ion implantation at GaN device technology. The main purpose of isolation process is the removal of 2DEG channel at an outside of the active region, but isolated device characteristic actually depends on a quality of epitaxial layer which means that isolation current is varied with different isolation depth. We investigated about isolation characteristics with each process by using AlGaN/GaN-on-Si wafer with un-doped GaN buffer. Deeper isolated layer is required to reduce isolation current through GaN buffer under 2DEG, thus the isolation depth of 400 nm at least might saturate the level of isolation current as shown in Fig. 2.6 (b).

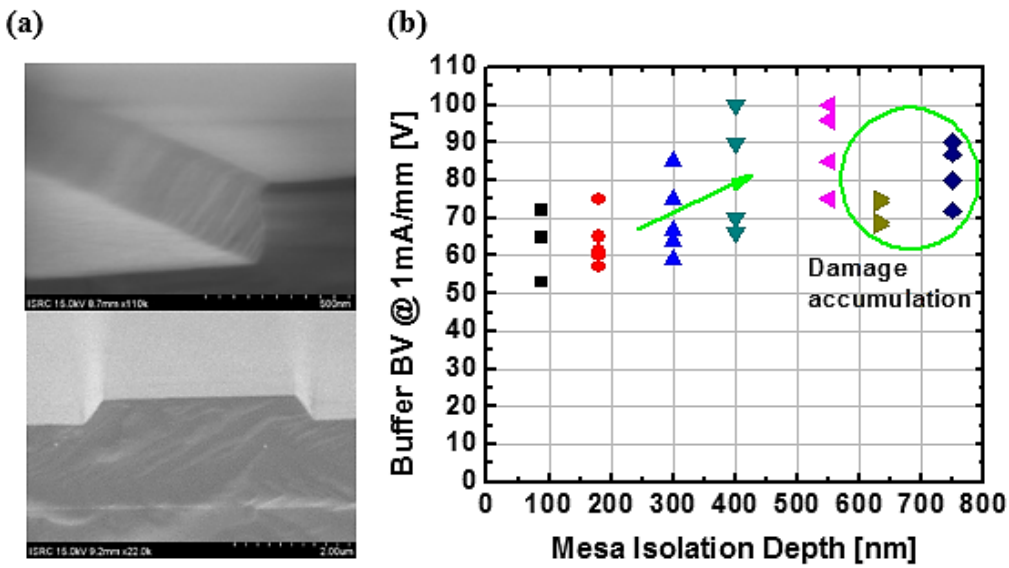

Fig. 2.6 (a) SEM images after mesa etching for device isolation. (b) Soft breakdown voltages with increasing mesa etching depth.

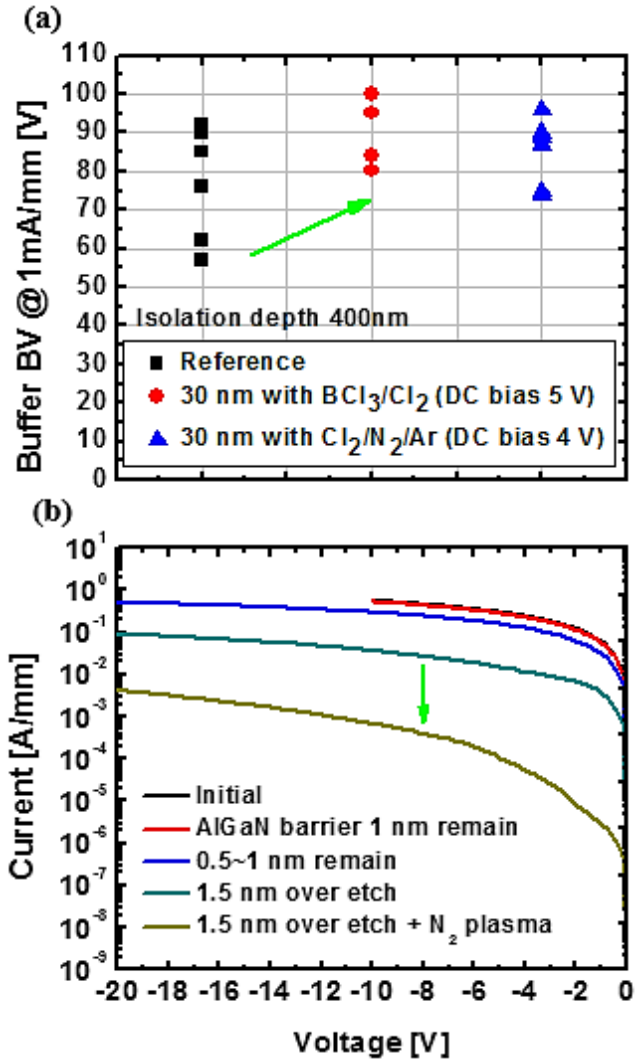

Fig. 2.7 (a) Soft breakdown voltages depend on etching condition. (b) Change of current density after the N_2 plasma treatment at the surface.

However, unlike ion implantation, mesa etching process can induce surface leakage current [26, 27] due to plasma damage. Figure 2.7 (a) and (b) demonstrate the effects of plasma damage and their recovery by N_2 plasma which indicated the plasma damage generated N-vacancies on the etched surface. We could found the surface effect absolutely that the current density

was reduced after N_2 plasma treatment on the surface by filling N-vacancies. From these results, we finally employed low power etching with BCl_3/Cl_2 at mesa etching process to improve breakdown voltage. Table. 2.1 shows the both GaN etching condition with high and low power.

Table 2.1 GaN etching condition of both low and high DC bias with ICP-RIE and high DC bias with RIE.

BCl_3 [sccm]	**Cl_2 [sccm]**	**Pressure [mTorr]**	**Source power [W]**	**RF power [W]**	**DC bias [V]**	**Etch rate [Å]**
2	18	5	350	4	4.5	1.2
2	18	5	350	15	23	5.5
6	18	75		100	89	5.5

In ion implantation case, it has advantages in terms of surface effect, mesa sidewall leakage [28], and substrate RF loss by keeping away pad metal from a substrate. Figure 2.8 shows the isolation current density of both mesa etching and ion implantation with Ar^+ 30 keV 1.5×10^{13} cm^{-2} followed by 160 keV 3.5×10^{13} cm^{-2} [29, 30]. We used SiN_x passivation layer on the isolated region before the ion implantation was performed. We could estimate the ion distribution profile by using TRIM ion implant simulation tool as shown in Fig. 2.8. The first step made Ar^+ distribute near the 2DEG channel and the second step made the wide Ar^+ profile from surface to 400 nm depth, so it was comparable enough to isolate inactive region with mesa etching. From the TRIM simulation, each implant step resulted in diffusion toward the active region with 17.4 nm and 60 nm, respectively.

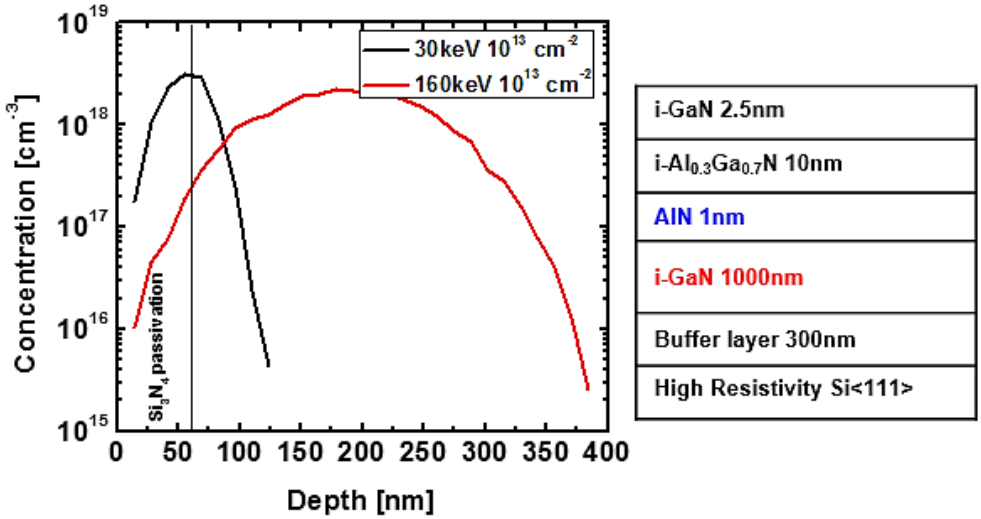

Fig. 2.8 Simulation result of depth profile of implanted Ar^+ ions with 30 keV and 160 keV energies.

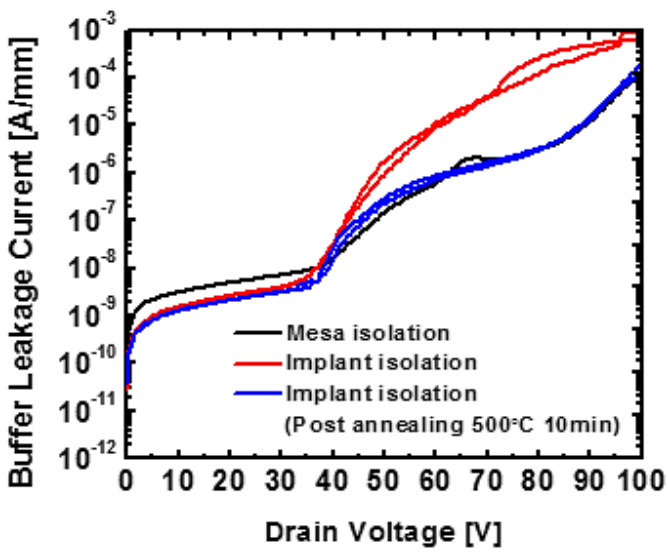

Fig. 2.9 Isolation current densities after mesa etching and ion implantation with and without post-implant annealing. Ar^+ ions were implanted with beam tilt of 7°.

Measured isolation current density of ion implanted device was lower than the device with mesa etching at low voltage region, and the isolation current density was decreased at high voltage region after the post annealing process was executed (Fig. 2.9).

The difference in device performances between mesa etching and ion implantation are simply described in Fig. 2.10. The device with mesa etching showed the higher gate leakage current density in forward region which was attributed to mesa sidewall effect, and the slightly higher drain off-state current density was exhibited at the mesa etched device. By making the device with plane structure, cut-off frequency characteristics were slightly increased as shown in Fig. 2.11 which was the mainly expected effect of ion implantation as the isolation process.

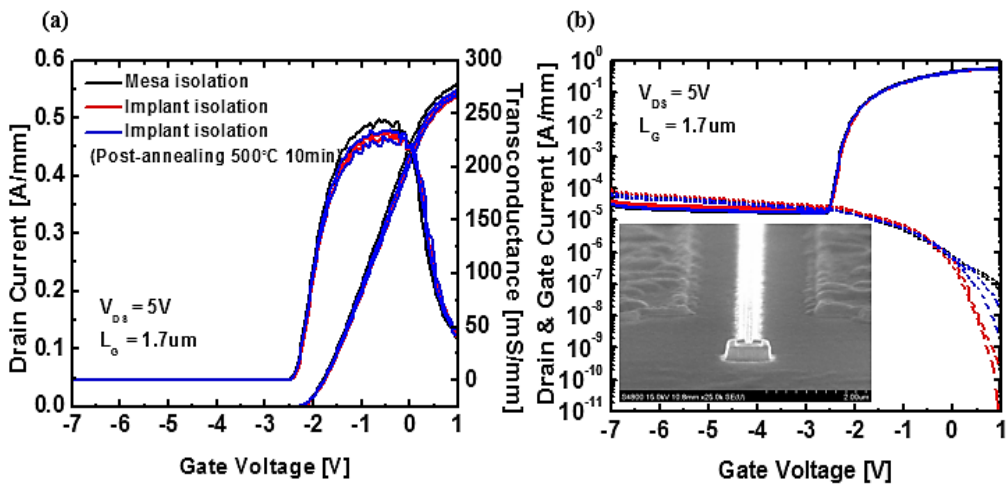

Fig. 2.10 Transfer characteristics of both devices with mesa etching and ion implantation. The source-drain distance is 16 μm, and source-gate distance is 2 μm.

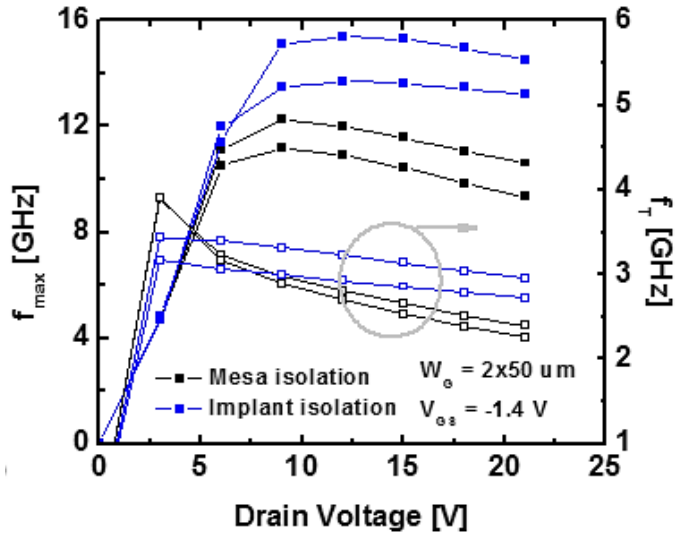

Fig. 2.11 Small-signal characteristics of fabricated devices with different isolation processes.

2.2.4 Passivation

A passivation layer is required for GaN HEMT devices to remove surface states which cause surface leakage current and 2DEG channel depletion called current collapse [31]. Also, passivation layer increases a density of electrons in 2DEG channel by inducing additional stress on AlGaN/GaN heterostructure [32]. There are several well-known dielectrics that have been used for passivation layer of GaN HEMT devices such as SiO_2, Si_3N_4, Al_2O_3, and AlN and so on [33-36]. In this research, we employed Si_3N_4 for passivation layer by using chemical vapor deposition (CVD) process and focused on the effects of their thickness to optimize the structure of GaN microwave devices.

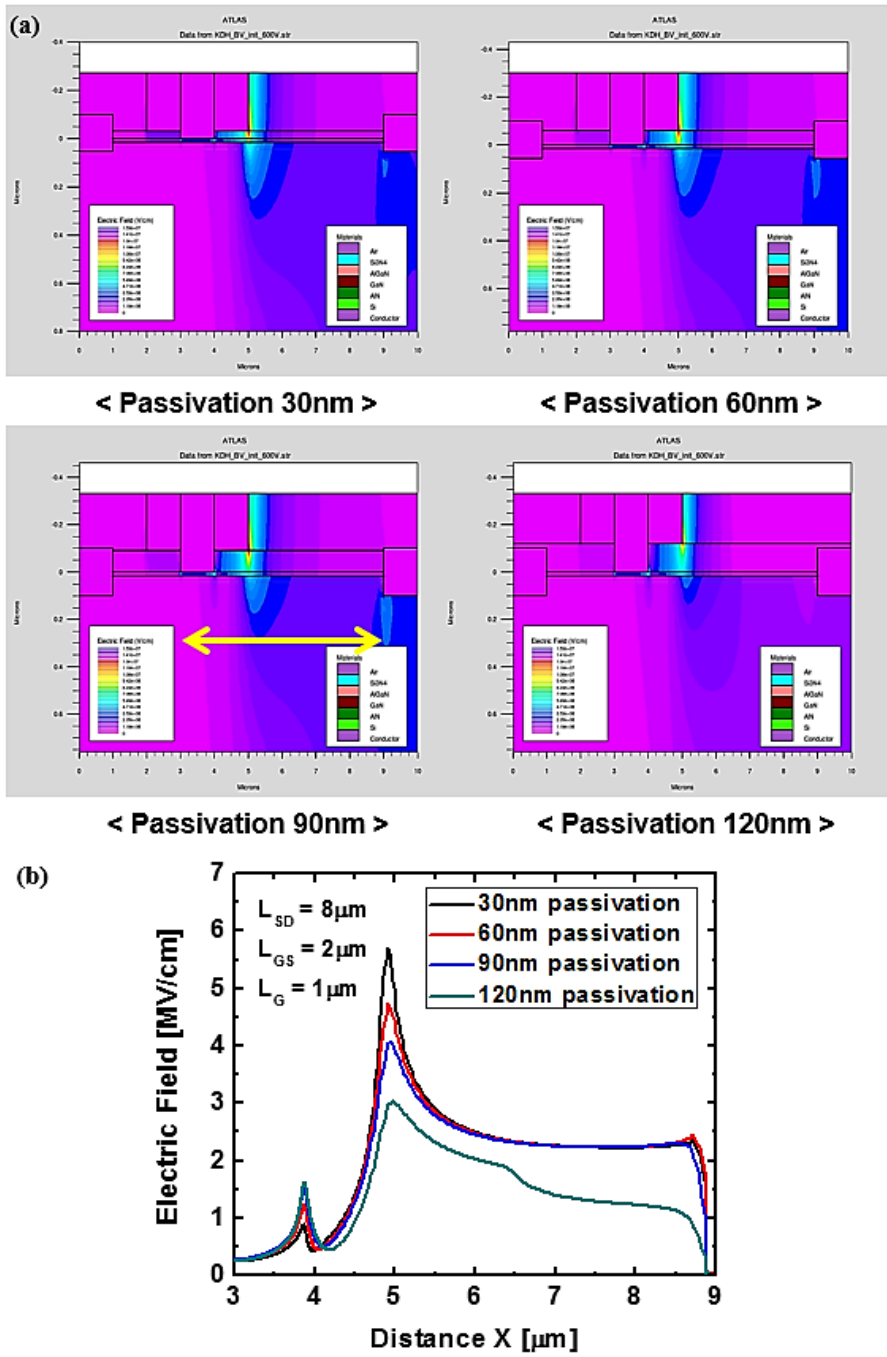

Fig. 2.12 (a)(b) Simulation results of electric field between the gate and drain with increasing the thickness of passivation layer.

The thicker dielectric can be more effective on improvement of breakdown voltage and reduction of current collapse phenomena commonly [37, 38]. We firstly proved the impacts of their thickness by using SILVACO simulation as shown in Fig. 2.12 (a) and (b). Only the dielectric thickness was different with varying from 30 nm to 120 nm-thick, and we could observe the reduction of peak electric field at the edge of gate and gate field-plate as the thickness increased.

The high electric field between gate and drain leads to early breakdown and large current collapse so that the GaN RF devices will exhibit low output power. In addition, AlGaN/GaN Schottky HEMTs with two different thickness of passivation layer were fabricated and evaluated their electrical characteristics. As same with the results of our simulation, the device with 60 nm-thick passivation layer showed lower breakdown voltage and larger current collapse than the device with 120 nm-thick passivation layer because of dispersion of electric field near the gate toward drain side (Fig. 2.13 (a) and (b)).

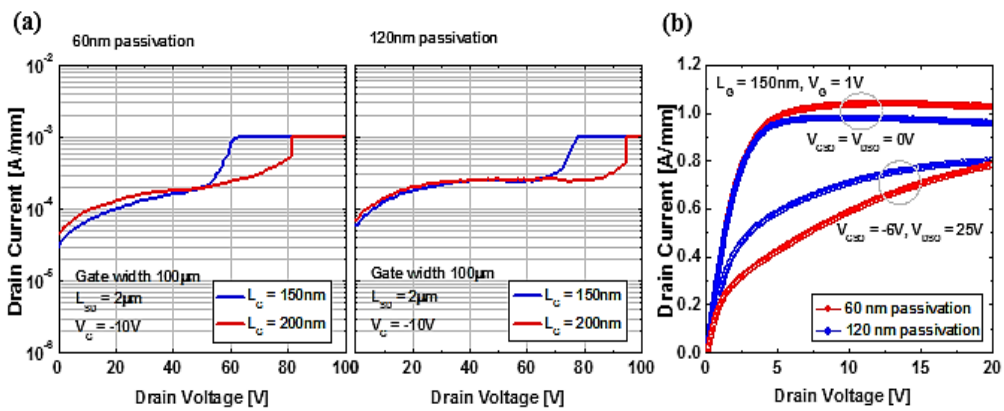

Fig. 2.13 (a) Drain off-state breakdown characteristics of the devices with 60 nm and 120 nm passivation layers. (b) Also pulsed I-V characteristics of both devices at V_{GSQ} = -6 V and V_{DSQ} = 25 V.

But, we must consider not only the characteristics related to large-signal performance of RF devices but also small-signal characteristics which can be degraded by increasing of parasitic capacitances. Indeed, small-signal characteristics decide the linear gain of large-signal performance. We compared current gain cut-off frequencies (f_T) and parasitic capacitances (C_{gs} and C_{gd}) of both devices through vector network measurement and small-signal equivalent circuit analysis as shown in Fig. 2.14 (a) and (b). Three different gate lengths were considered and the device with 120 nm-thick passivation layer presented lower f_T characteristic in all gate lengths. This result was mainly attributed to increase of C_{gs} which is the most important factor in f_T.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

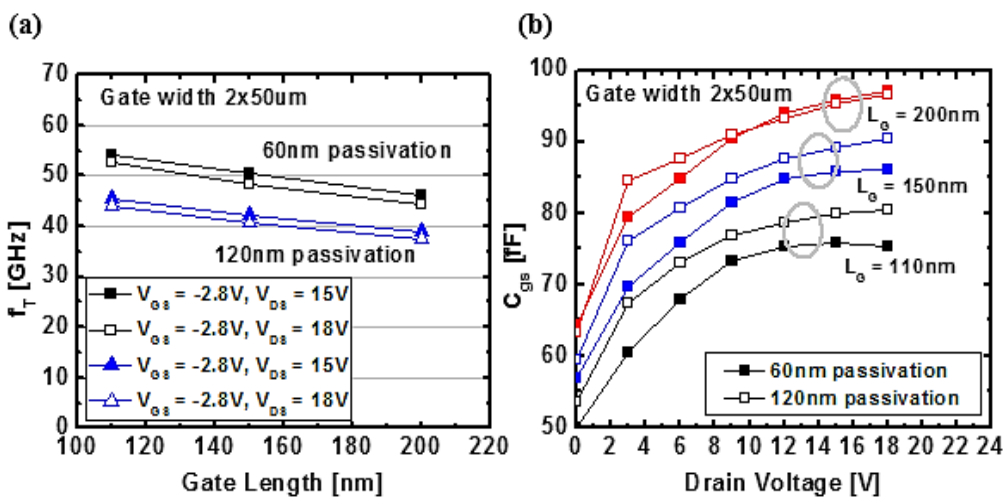

Fig. 2.14 (a) Current gain cut-off frequency (f_T) characteristics and (b) extracted C_{gs} values with different gate lengths.

The total gate parasitic capacitances are consists of intrinsic and extrinsic capacitances, but the intrinsic capacitance underneath the gate might be negligible when the gate length is getting shorter, thus the extrinsic capacitance becomes dominant [39]. At Fig. 2.14 (b), the difference of extracted C_{gs} in both devices became larger with shorter gate length which means that the RF performance of the device with thicker passivation layer will be degraded as the gate length decreases. And the extrinsic capacitance is composed with parallel plate capacitance which is inversely proportional to dielectric thickness and fringing capacitance all around the gate metal. If the passivation layer becomes thicker, the fringing capacitance will increase continuously, but parallel plate capacitance will slightly reduce and almost saturate (Fig. 2.15). As a result, we decided to employ Si_3N_4 passivation layer of 60 nm-thick on GaN HEMT device for Ka-band application.

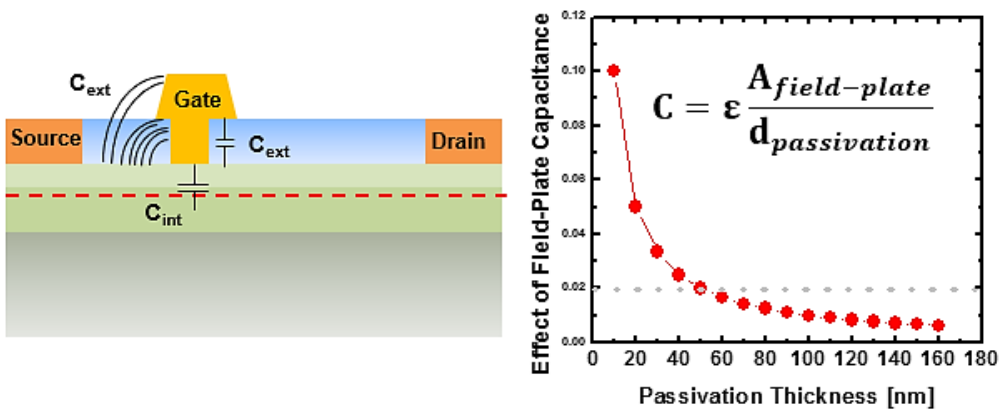

Fig. 2.15 Simple model used for estimating extrinsic parasitic capacitances (y = 1/d).

2.2.5 Gate Formation

The gate structure of RF device is directly associated with RF performance [40], both small and large-signal. There are two different gate structures for GaN RF devices in general, one is a T-gate [41] (or Y-gate) (Fig. 2.16(a)) and the other is a field-plated gate (Fig. 2.16(b)).

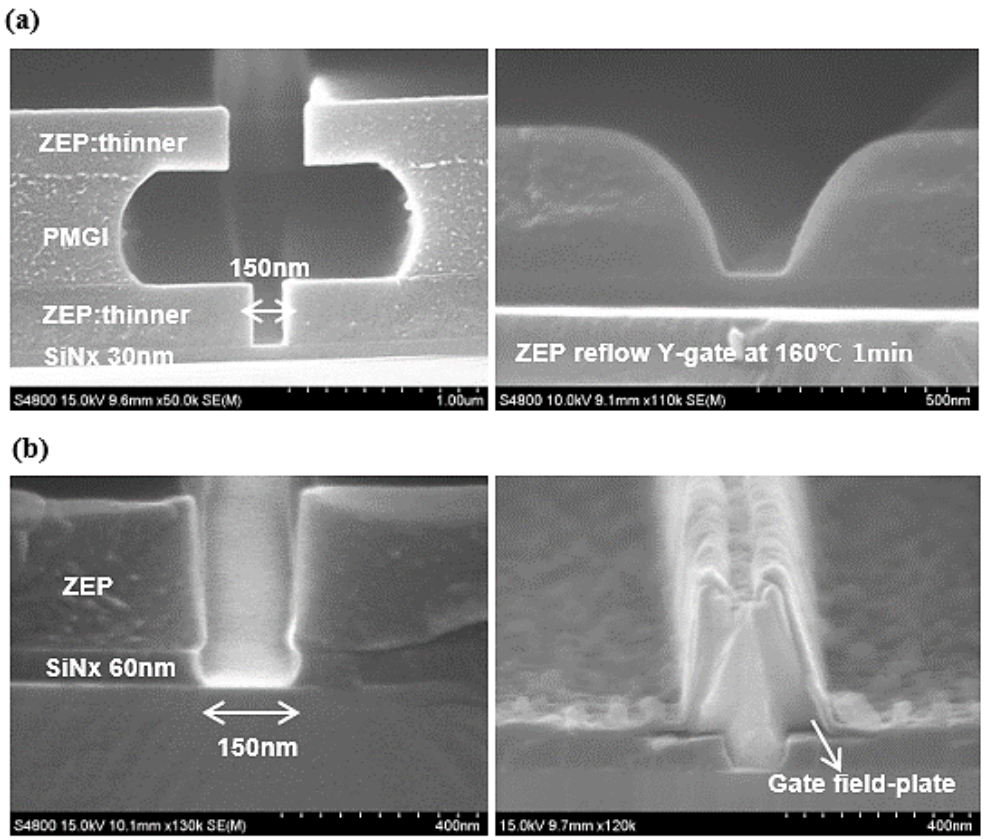

Fig. 2.16 SEM images of (a) T-gate(Y-gate) and (b) field-plated gate with gate length of 150 nm.

For the T-gate structure, ZEP/ polymethylglutarimide (PMGI) /ZEP triple layer was spin coated, and e-beam lithography of two times was performed. On the other hand, ZEP single layer was firstly used to form gate foot of field-plated gate structure followed by PMGI/ZEP double layer with second e-beam lithography for metal lift-off process. Each gate structure has advantages and disadvantages in terms of both small and large-signal performances.

As shown in Table. 2.2, the T-gate structure can achieve lower parasitic capacitance but lower breakdown voltage and poorer current collapse phenomena due to the higher electric field than the field-plated gate. The reason why we considered about the gate structure is the Ka-band which is the frequency band of our research target is placed at the beginning point of mmw so that requires both quite a high operation voltage and quite a high operation frequency.

Table 2.2 The effects of T-gate (left) and field-plated gate (right) structures on RF device.

Advantage	Disadvantage	Advantage	Disadvantage
Low gate resistance	Thin passivation	Higher breakdown	High parasitic capacitance
Low parasitic capacitance	Lower breakdown	Better current collapse	Lower cutoff frequency
Higher cutoff frequency	Poor current collapse	Stable structure	Field-plate length effect

Although identifying the device performances is actually complex that cannot be decided by only gate structure, we tried to find the optimized gate structure with field-plate which could demonstrate comparable small-signal

characteristic with T-gate and maintain the advantages of the field-plated gate structure [42]. Fig. 2.17 shows the effects of length of the gate field-plate on maximum oscillation frequency (f_{max}) and f_T of the device with the gate length of 110 nm. Due to the increase of the extrinsic gate capacitance, f_{max} and f_T were degraded drastically as the length of the gate field-plate increased slightly. So we suggested the gate structure with the field-plate length of lower than 100 nm resulted in both reasonable small-signal characteristic and improved breakdown voltage and current collapse phenomena for Ka-band application.

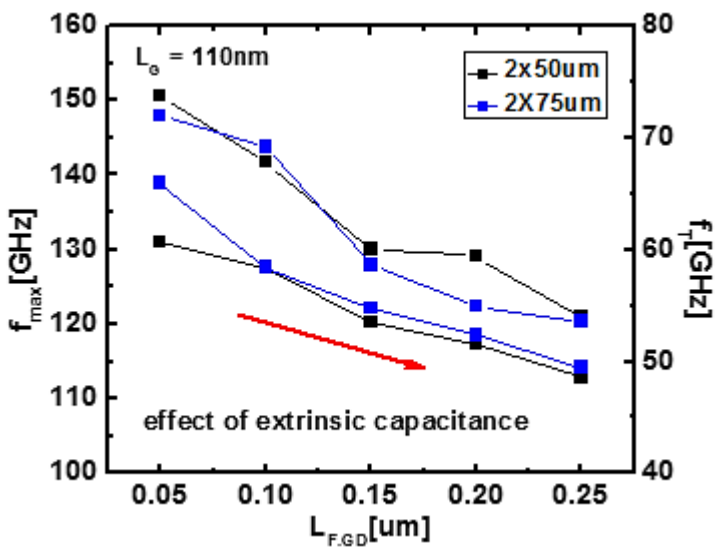

Fig. 2.17 Small-signal characteristics of 110 nm AlGaN/GaN HEMT with various length of gate field-plate to the drain side.

2.3 Schottky Gate Metal

In company with the gate structure, the Schottky gate metal stack can have an impact on the performance of GaN RF device. The thermal annealing process can reduce the leakage current density in conjunction with the improvement of Schottky metal/GaN interface quality and enhance the thermal stability of the devices. Many research groups have utilized various Schottky gate metals, such as Ni, Pt, Ir, Pd, Mo, Al, and Cu including Au top metallization [43]. Unfortunately, it can be easy to diffuse Au into GaN trhough the Schottky metal during the thermal annealing process, causing the degradation of device electrical characteristics. It was reported that the insertion gate metal layer between the Schottky bottom metal and an Au top metal reduced the gate leakage current and effectively suppress Au diffusion during high temperature annealing process [44]. It was also found that the electrical gate stress brought about the structural degradation because of diffused Au at the gate edge [45-47]. Recently, in order to avoid the electrical and structural degradations from Au, non-Au gate metal stacks have been studied. In the case of TiN and W gate metals, the annealing temperature is available up to 850 °C for post metallization annealing [48-50].

$$f_{max} = \frac{f_T}{2\sqrt{2\pi \times f_T \times C_{gd}(R_g + R_s) + \frac{R_g + R_s}{r_o}}}$$

However, Ni/thick Au metal stack has typically been employed for most of GaN RF devices due to a fairly high work function, good adhesion, and low gate resistance (R_g). The R_g is one of the most important factors for maximum oscillation frequency (f_{max}) power gain characteristic and should

be low enough especially at millimeter-wave. In addition, there were several demonstrations of different gate metal stacks, such as Ni, Pd, Ir, Mo, Cu, and Ti as the bottom contact only with studies on electrical characteristics for GaN microwave device [43]. In this section, we suggested the influence of the thermal annealing process on the R_g based on Ni/Au metal stack.

2.3.1 DC and Pulsed Characteristics

To identify our device characteristics and electrical properties gate metal stacks, firstly we used the epitaxial structure with a 2 nm GaN cap layer, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, 400 nm GaN channel layer, and 2 μm C-doped GaN buffer layer grown on a high-resistivity Si(111) substrate. And second epitaxial structure used to measure small-signal characteristics consisted of a 2.5 nm GaN cap layer, 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, 1 nm AlN spacer layer, and 1.3 μm un-doped GaN buffer layer also grown on Si substrate. The sheet resistances of each structure was 405 Ω/sq and 320 Ω/sq respectively. Employed gate metal stacks were Ni/Au (=40/360 nm) and Ni/Mo/Au (=40/15/360 nm) with the gate length of 0.25 μm, L_{DS} = 4 μm, L_{GS} = 1 μm, and L_{GFP} = 0.1 μm for first epitaxial structure. The Mo metal was representatively used as the insertion gate layer because of its high thermal stability. Figure 2.18 shows gate reverse leakage currents of both devices with increasing annealing temperature. The device with Ni/Mo/Au gate demonstrated stable reduction of leakage currents after 350 °C rapid thermal annealing for 2 min at N_2 ambient, and that indicated interface of the Schottky contact was successfully improved. On the other hand, the device with Ni/Au gate could not demonstrate effective reduction versus annealing temperature and the trends of current levels were scattered.

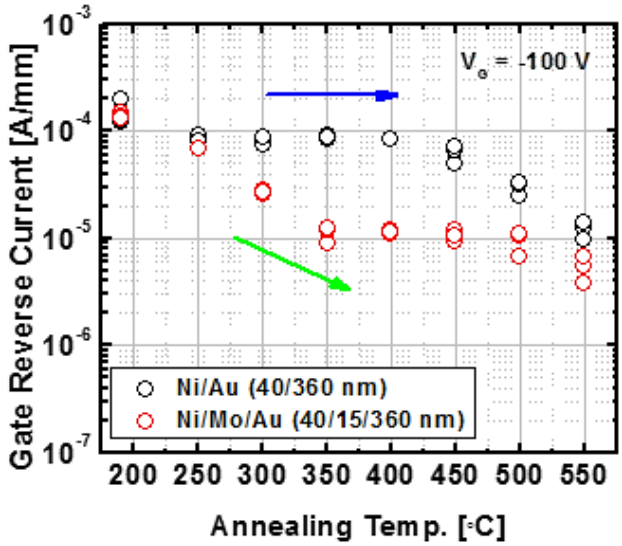

Fig. 2.18 Two-terminal (gate-drain) gate reverse leakage current characteristics of the fabricated AlGaN/GaN-on-Si Schottky HEMTs with gate length of 0.25 µm at V_{GS} = - 100 V (measurement from three devices at each annealing temperature) with gate metal stacks comprising Ni/Au and Ni/Mo/Au. Annealing time was 2 min at each temperature.

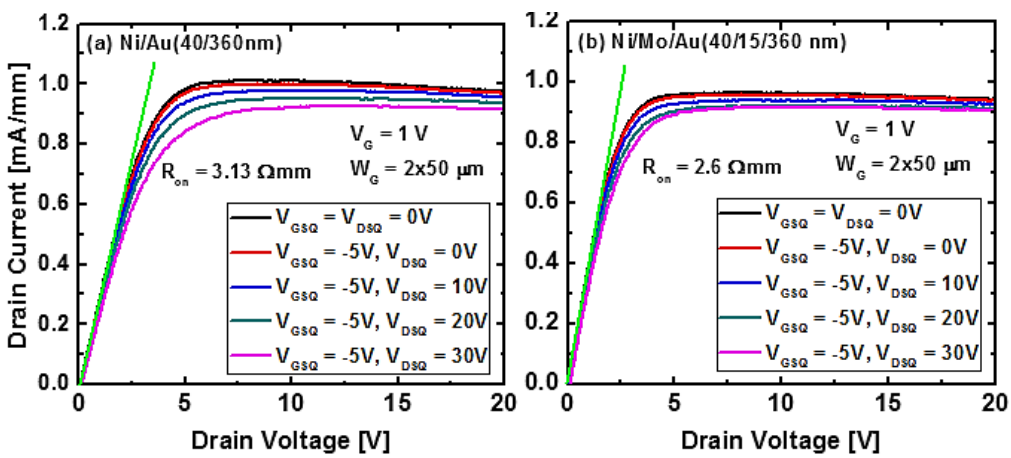

Fig. 2.19 Pulsed I-V characteristics of the devices with gate metal stacks comprising (a) Ni/Au and (b) Ni/Mo/Au. Pulse width = 200 ns and period = 1 ms. While the quiescent bias conditions for the gate lag measurements were - 5 V, and the drain lag measurements were up to 30 V.

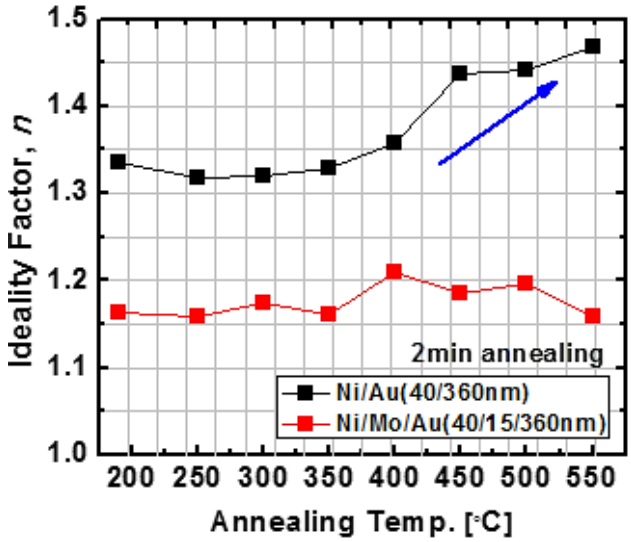

Fig. 2.20 Extracted ideality factors as a function of annealing temperature for the Ni/Au and Ni/Mo/Au Schottky contacts.

We estimated current collapse phenomena by pulsed I-V measurements only after SiN_x final passivation at 190 °C as shown in Fig. 2.19. The device with Mo insertion metal layer exhibited smaller drain current dispersion and smaller on-resistance (R_{on}) than without that layer, but the metal dependence of the current collapse results was not well understood, and it requires further investigation. From our point of view, the results of current collapse phenomena were not distinct from the initial Schottky ideality factors of both gate metal stacks in Fig. 2.20. After annealing at 400 °C, the Schottky contact without Mo insertion metal layer showed the increase on ideality factor [51]. We finally measured gate current with on-state high power stress condition of microwave power amplifying operation which can be affected by high channel temperature and hot electrons [45, 46].

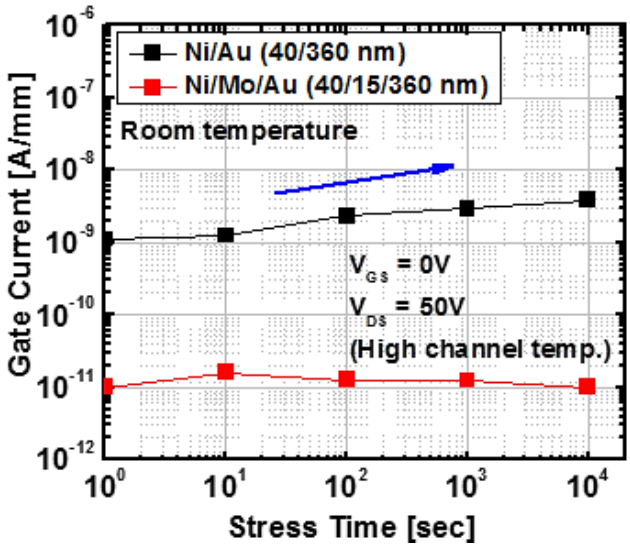

Fig. 2.21 Measured gate current as a function of on-state high power stress condition of the Ni/au and Ni/Mo/Au gate metal stacks at room temperature. V_{GS} = 0 V, V_{DS} = 50 V.

Figure 2.21 shows the time dependent gate currents with stress bias of V_{GS} = 0 V and V_{DS} = 50 V at room temperature. The device with Ni/Mo/Au gate metal stack demonstrated stable gate current up to 10^4 s, whereas the device with only Ni/Au gate metal stack showed the increase of gate current before 10^2 s that indicated thermally less stable. And the difference between these two Schottky contacts might be larger with the higher electric field of short channel device and longer stress time.

2.3.2 Gate Resistance

As we focused on the change of gate resistance with different gate metal stacks, we used 100 μm-wide rectangular line patterns with large pad region by using e-beam lithography for 2-point measurement which is presented in the inset of Fig. 2.22 (a). To avoid metal oxidation during annealing, all

patterns were passivated with SiN_x of 30 nm-thick. Figure 2.22 (a) shows the increase of measured metal resistances with the length of 0.2 μm depended on annealing temperature. The metal stack with Mo insertion metal layer exhibited effective suppression of metal resistance in comparison to only Ni/Au metal stack, and the results were more obvious for longer annealing time. The early increase of metal resistance near 350 °C with longer annealing time was due to Au diffusion into the Ni. If the line length became shorter, the portion of the reacted region between each metal might have the larger impact on metal resistance, as shown in the Fig. 2.22(b), and this indicated the importance of insertion metal layer at millimeter-wave application.

However, the measured values of metal resistances might be overestimated because the line patterns had not same structures with actual devices so that there was edge effect which was induced from Au flowing. Ni/Mo/Au (=25/15/360 nm) metal stack showed higher increase trends in Fig. 2.22 (b) that implied the edge effect indirectly with thinner bottom Ni layer. Removal of edge effect is not only related to the difference between the structure of tested line pattern and actual device but also related to the gate structure of the device, such as length of gate field-plate and thickness of dielectric under the gate field-plate [46]. In this study, we just examined at a center of the tested pattern using transmission electron microscope (TEM) energy dispersive X-ray spectroscopy (EDS) analysis, which is turned up in Fig. 2.23. After annealing at 500 °C for 5 min, the metal stack without the Mo insertion layer showed inter-diffusion of Au and out-diffusion of Ga, so that mixed Au-Ga and Ni-Au were detected, whereas the metal stack with Mo insertion layer minimized inter-diffusion. Au and Ga theoretically start reacting above 450 °C [52-54], and the Ni and Au thin film diffuse each other above 200 °C [55-57] that approved reaction between those metals which resulted in lower conductivities than pure metals [58-60].

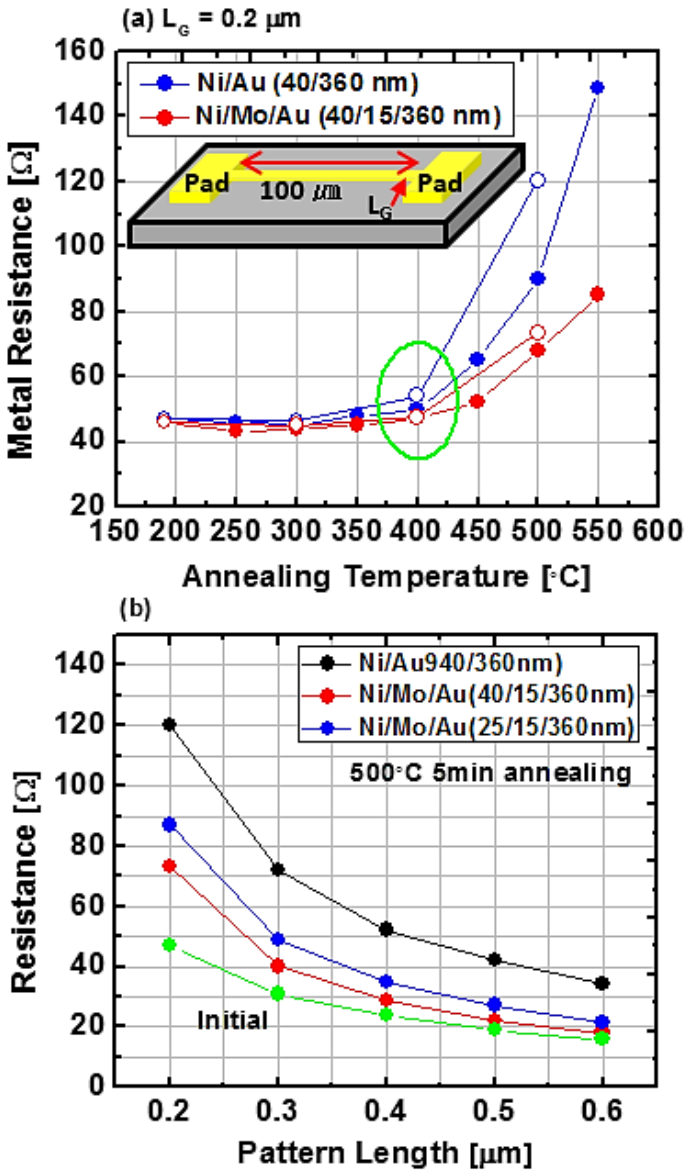

Fig. 2.22 Two-point measured metal resistance (a) versus annealing temperature for annealing times of 2 min (solid data points) and 5 min (empty data points) ; and (b) versus line pattern length after annealing at 500°C for 5 min, where the initial resistance values of the three metal stacks (green data points) were almost identical.

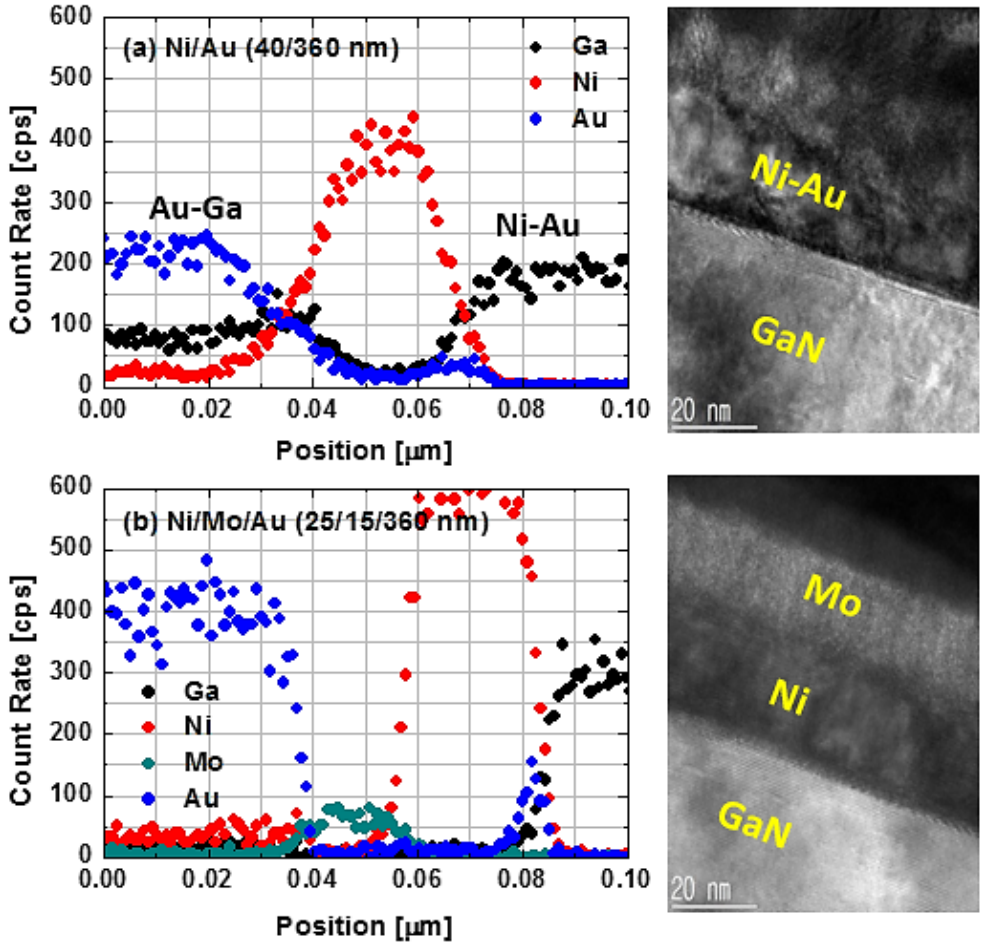

Fig. 2.23 TEM images and EDS analysis of the (a) Ni/Au and (b) Ni/Mo/Au gate metal stacks after annealing at 500°C for 5 min. EDS analysis of the each gate metal stack performed at the center of the metal line pattern.

2.3.3 Small-signal Characteristics

To evaluate the effect of the gate metal resistance on actual devices, we fabricated separate devices with shorter gate length (L_G = 0.12 μm, L_{SD} = 2 μm, and L_{GS} = 0.6 μm) and gate metal stacks with Ni/Au (=40/360 nm), Ni/Mo/Au (=40/10/360 nm), and Ni/Mo/Au (=40/20/360 nm) using same

fabrication process above. The results of small-signal measurements of 2-finger device without pad de-embedding are indicated in Fig. 2.24. Initially, two devices demonstrated similar power gain cut-off frequency (f_{max}), and only the differences were originated from device variations. The device without Mo insertion metal layer more significantly degraded on f_{max} characteristic after 500 °C for 5 min, and it was mainly due to the increase of gate resistance according to the parameter extraction. The equivalent circuit of the intrinsic FET model contained the low-frequency dispersion effect with the thermal and trap sub-circuits [61]. On the other hand, the devices with Mo insertion metal layer whether 10 nm or 20 nm showed less degradation after annealing. The thickness of insertion metal layer had no remarkable effect on small-signal characteristics.

Therefore, the insertion gate metal between Ni and Au is important for AlGaN/GaN Schottky HEMT to mitigate reduction of f_{max} due to the increase of gate resistance, especially for millimeter-wave with shorter gate length. The gate metal stack on RF application should be employed with not only electrically good Schottky contact properties but also thermally more stable characteristics, so that the change of f_{max} can be minimized. Also, optimization of the metal stack including other metals, such as Pt and Ir might be required with further investigation of the gate structure to more reduce the metal reaction.

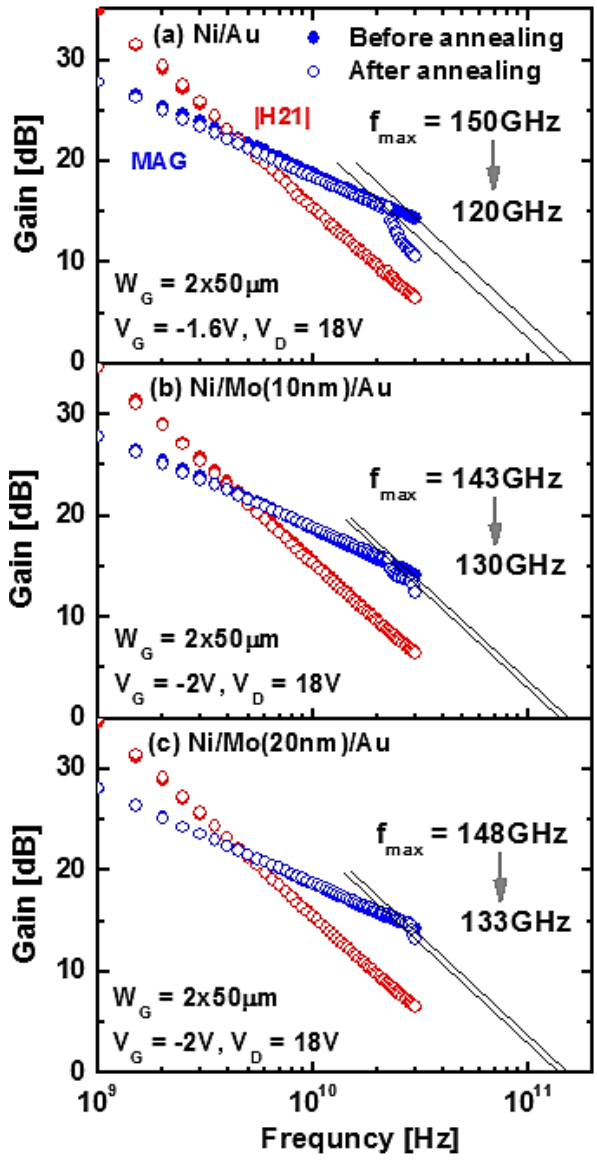

Fig. 2.24 Small-signal characteristics of fabricated 2 × 50 μm devices with gate metal stacks comprising (a) Ni/Au (=40/360 nm), (b) Ni/Mo/Au (=40/10/360 nm), and (c) Ni/Mo/Au (=40/20/360 nm) at each gate voltage of maximum transconductance before and after annealing. The annealing temperature was 500°C for 5 min.

2.4 References

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Chapter 3. Improving Output Power of Ka-band AlGaN/GaN HEMTs on Si Substrate

3.1 Introduction

This chapter introduces two key technologies that certainly required for the high performance of GaN RF devices. An AlGaN/GaN heterostructure on Si substrate demonstrate poorer epitaxial quality than that of SiC substrate due to lattice mismatch so that high dislocation density induces low breakdown voltage, current collapse phenomena, and inferior RF performance. Thus, we investigated the effects of the epitaxial structure with Si substrate by comparing doped buffer and un-doped buffer or different GaN channel thickness. Also, we tried to find the suitable epitaxial structure for our research about Ka-band application and expected the high performance that could be competitive with AlGaN/GaN heterostructure on SiC substrate.

In addition, the passivation process is one of the critical technologies to achieve high output power by suppression of surface effects even though we mentioned about this process briefly in the last chapter. We employed much more effective passivation process on GaN HEMT device with HfO_2 which has a high dielectric constant, and this approach allowed good current collapse characteristic without increase of the thickness of passivation layer.

3.2 Epitaxial Structure

In this section, we investigated the effects of doped buffer on the microwave performance of AlGaN/GaN-on-Si HEMT. AlGaN/GaN heterostructure generally employs doped buffer with carbon (C) or iron (Fe) to reduce isolation current by compensation of unintentionally induced donor during growth condition. However, this technology additionally causes trapping effects due to acceptor levels of the dopants so that the trade-off characteristic varies with the thickness of GaN channel above the buffer layer. We fabricated AlGaN/GaN-on-Si HEMTs and evaluated their electrical characteristics including DC and RF with each epitaxial structure. Finally, photoluminescence (PL) and secondary ion mass spectrometry (SIMS) measurements were carried out to investigate what disadvantages were in the highly-doped C buffer on microwave characteristics.

3.2.1 AlGaN Barrier Layer

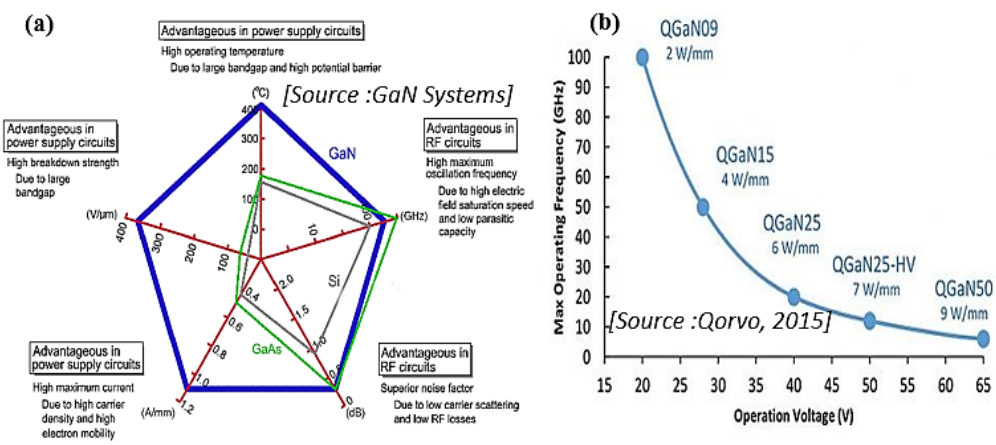


Fig. 3.1 (a) Advantages of GaN materials and devices. (b) And their operation voltages with respective target frequencies.

The GaN device has an advantage of output power density in comparison to Si or GaAs so that the higher operation voltage is usually applied to the device (Fig. 3.1 (a) and (b)). As we mentioned in the last chapter, GaN device for Ka-band application also requires the higher operation voltage than other mmw applications and the higher frequency response characteristics than microwave applications. So we must consider the thickness and Al mole-fraction of AlGaN barrier layer [1, 2] to satisfy both requirements firstly to avoid short channel effect by the biased drain voltage (Fig. 3.2) and achieve high transconductance. Thus, most of the GaN RF devices demand aspect ratio (L_G/$d_{channel}$) over 10 whereas the GaAs RF devices demand 2.5 ~ 6 [3, 4]. Table. 3.1 listed up several groups with their results of GaN HEMTs for K~Ka-band application. We also targeted 0.15 μm gate with the operation voltage up to 24 V in this research so that the thickness of AlGaN barrier layer was decided below 12 nm and Al mole-fraction was 30 % which was quite high to compensate low 2DEG density due to the thin AlGaN barrier layer.

Table 3.1 The aspect ratio and structure of AlGaN barrier layer of GaN HEMTs for K ~ Ka band.

Groups	Gate length [μm]	L_{SD} [μm]	AlGaN [nm]	Al [%]	L_G/d	F_{max} (DC bias) [GHz]	Operation frequency [GHz]	Operation voltage [V]
HKUST	0.2	4	18	26	9.5	180(24)	-	-
ETH-Zurich	0.2	2	17.5	26	10.2	118(10)	40	20
IEMN	0.125		12.5	26	8.6	125(4)	-	-
IEMN	0.1	2.5	6	100	16.6	192(15)	40	15
NEDI	0.15	2.5	20	28	10	63(24)	35	24
Triquint	0.25	-	-	31.5	-	-	35	20
Toshiba	0.18	-	-	30	-	-	31	24
UCSB	0.16	-	25 -> 12	32	13.3	155(5)	30	30
Toshiba	0.15	-	15	30	10	140(24)	28	24

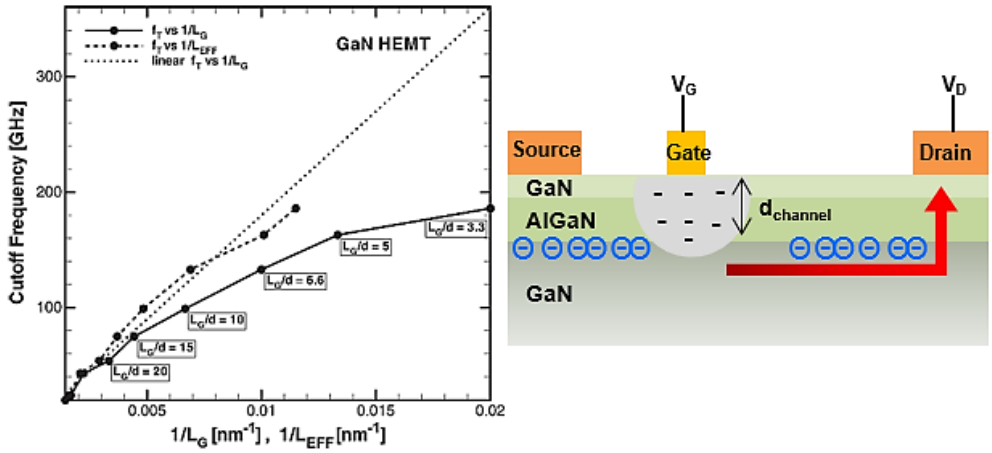


Fig. 3.2 The influence of short channel effect of GaN HEMT on cut-off frequency [3]. The high drain operation voltage can increase the short channel effect.

3.2.2 Buffer Doping

It is known that the un-doped GaN buffer exhibits n-type property due to impurities induced during GaN growth processes, such as N-vacancy, oxygen, and silicon [5]. Typical methods to achieve a high resistive buffer layer are Fe or C doping during buffer growth (Fig. 3.3). Employing a doped buffer layer can suppress the vertical leakage and can provide better confinement of 2DEG channel [6] which means the conduction band minimum (CBM) of GaN channel layer of AlGaN/GaN heterostructure is lifted up.

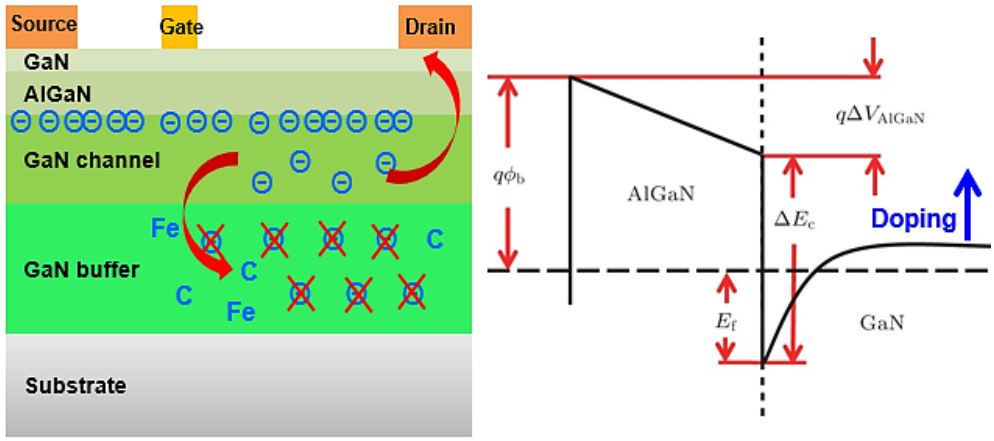


Fig. 3.3 Mechanism of i-GaN buffer doping by Fe or C to reduce buffer leakage current.

Although several studies have reported the disadvantages of buffer doping induced current collapse and limited dynamic characteristics [7-10], numerous groups are still employing the doped buffer layers for power and microwave devices in order to achieve high breakdown voltages [11-14]. While the effects of Fe-doping on microwave characteristics have been studied by several research groups, only a few reports are found on the influence of C-doping on microwave characteristics [15-18]. It should be noted that Fe is not compatible with a front-end Si processing because Fe diffuses into Si and deteriorates the device performance. Therefore, Fe-doped buffer wafers would limit the integration possibility with Si technology [19]. Also, Fig. 3.4 (b) shows the simple comparison of isolation current density between two different wafers with Fe and C-doped buffer respectively. At the wafer with Fe-doped buffer demonstrated the higher isolation current density than that with C-doped buffer even if the isolation depth was much higher. Generally known, Fe-doping has an advantage of less trapping effect [8] on devices than C-doping, but it suffers from memory effect in a chamber during

the growth process [20]. So usually the concentration of Fe-doping tends to be lower resulted in higher isolation current density than C-doping at buffer.

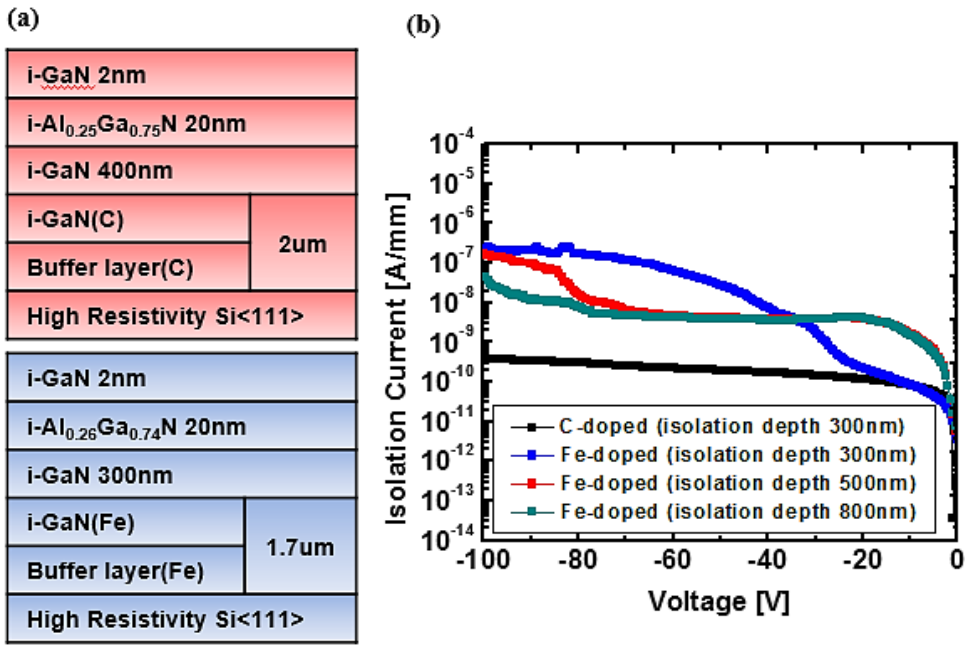


Fig. 3.4 (a) The structure of AlGaN/GaN epitaxial layers of both C and Fe doped on GaN buffer. (b) Comparison of isolation current densities of C and Fe doped structures with increasing isolation depth.

At this point of view, C would be a better choice for the source of donor compensation centers. In addition, the C-doping process is known to have less memory effects in the growth chamber [21, 22]. So we condensed with the C-doped buffer only which compared to AlGaN/GaN heterostructure with un-doped buffer for applying to our research by estimating their electrical characteristics. Most studies to date have been performed on counter doping effects and acceptor traps of C-doped buffer [10, 23, 24]. Recently, Gustafsson et al. reported the dispersive effects of microwave devices due to acceptor traps with C-doped buffer and proposed a stepped doping structure

to resolve the disadvantages of C-doping buffer [7].

3.2.3 Experiments

Three different AlGaN/GaN heterostructures (A, B, C) grown on high-resistivity (HR) Si(111) substrates were compared in this study. As shown in Fig. 3.5, structure A had a 300 nm thick un-doped buffer layer with a 1000 nm GaN channel layer whereas structure B and C had a 2 μm thick C-doped buffer layer with a 350 nm and 400 nm GaN channel layer respectively. The doping concentration of the C-doped buffer layer was ~1 × 10^{19} cm^{-3}.

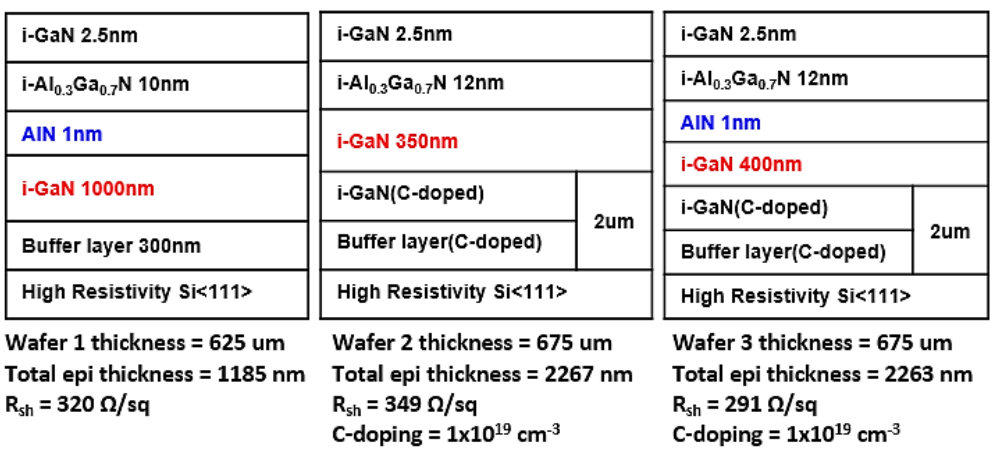


Fig. 3.5 The structures and characteristics of three wafers used for evaluating the effects of C-doping on GaN buffer. All wafers were supplied by NTTAT corp..

Figure 3.6 (a) exhibits X-ray diffraction (XRD) measurements for three wafers [25]. XRD measurements are generally used to estimate epitaxial quality of GaN wafer, and Ando et al. reported the relation between full-width at half-maximum (FWHM) values and threshold voltage (V_{th}) instability at

AlGaN/GaN-on-Si substrate. However, V_{th} instability is not only responsible for GaN channel but also AlGaN barrier, so that it is unclear which trap level is mainly attributed to device performance. We did not focus on well-known trap levels at GaN which were induced during various growth conditions, such as 0.42-0.47, 0.39-0.42, and 0.36-0.46 eV of activation energies [25-27]. Also, Lensik et al. reported the effect of C-concentration on dislocation density and crystal quality, and no influence was observed as increasing C-concentration even though it was GaN bulk layer on sapphire substrate [28]. At this point of view, we neglected the issues of epitaxial quality.

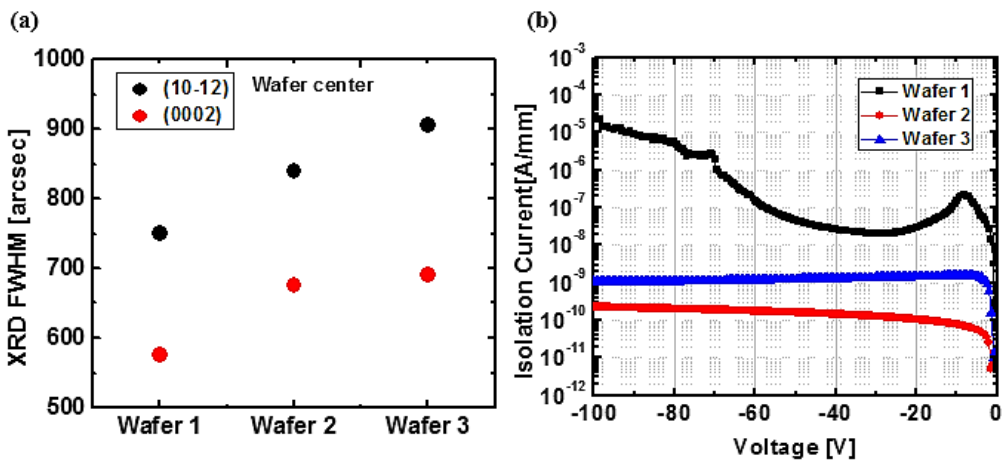


Fig. 3.6 (a) FWHMs of X-ray rocking curves (in arcsec) for three different wafers. (b) Buffer leakage current characteristics of each wafer. Isolation depths were 350 nm.

3.2.4 DC and RF Characteristics

The gate lengths of fabricated AlGaN/GaN HEMTs were 0.15 μm and L_{GS} were fixed with 0.6 μm for various source-drain distances (L_{SD} = 2, 3, 4 μm). Figure 3.6(b) shows the buffer leakage current characteristics for both

samples that were measured with the isolation gap of 30 μm, as illustrated in the inset. As expected, the C-doped samples exhibited much lower leakage current characteristics in comparison to the un-doped sample.

In order to evaluate the effects of the C-doped buffer, we focused on the channel modulation and current collapse phenomenon of the devices that are related to the short channel and deep level trapping effects. The sub-threshold slope characteristics are associated with pinch-off characteristics and cut-off frequency that are important characteristics for microwave devices. Figure 3.7 shows the sub-threshold slope characteristics of each sample with various source-drain distances at the same gate length of 0.15 μm and drain voltage of 5 V, and the results signify short channel effect indirectly. Previous studies reported the improved sub-threshold slope of AlGaN/GaN HEMTs by intentional Fe buffer doping and reduced GaN channel thickness [15, 17]. On the contrary, the sample with C-doped buffers in our study exhibited a relatively larger sub-threshold slope in comparison with the un-doped buffer sample, even though C-doped buffer with thinner GaN channel showed the relatively small sub-threshold slope. Although the off-state leakage current was lower for the samples with C-doped buffer, the transfer characteristics between on and off turned out to be poor, indicating that it had extra carriers might be induced from donor level states in the GaN channel layer associated with C-doping. Figure 3.8 demonstrates off-state drain currents at gate voltage of -10 V of each device. As known in the transfer curves, the devices with C-doped buffer showed lower drain currents at lower drain voltage region. However, similar breakdown voltages or drain currents were obtained at source-drain distance with 2 μm or at high drain voltage. This point also suggested that C-doping buffer made GaN channel layer to be conductive.

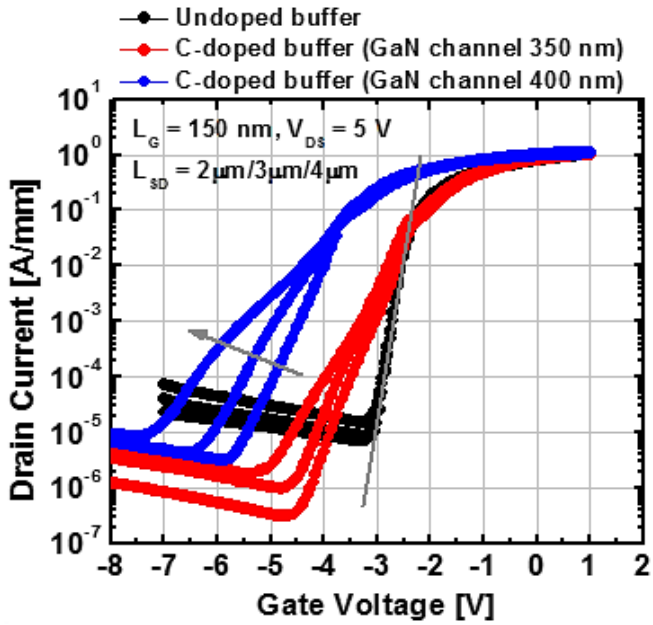


Fig. 3.7 Log scale transfer characteristics of the fabricated devices with un-doped and C-doped buffer layer.

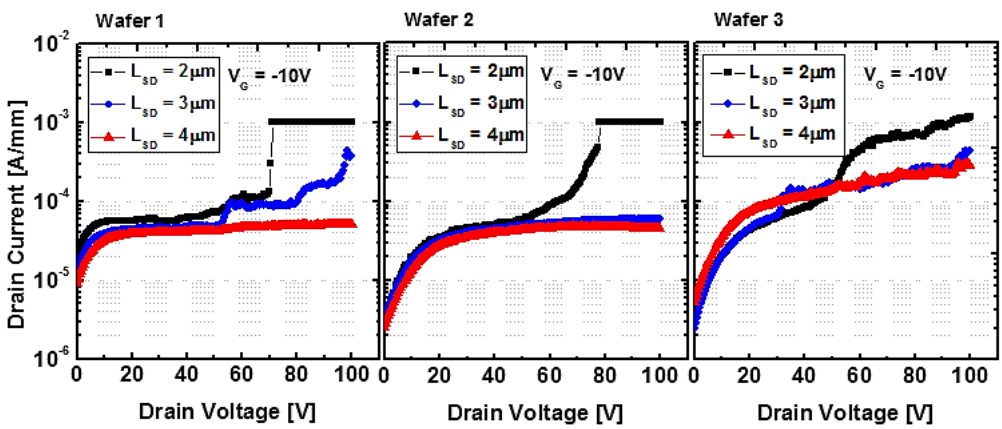


Fig. 3.8 Off-state drain leakage current characteristics of the fabricated devices on each wafer structures.

If the C-doping process generated acceptor level traps, the relevant current collapse phenomenon would lead to early saturation of output power

under RF operation [29, 30]. The gate and drain lag characteristics of these samples with the source-drain distance of 2 μm were measured to investigate the current collapse phenomenon under pulsed conditions with the pulse width of 500 ns at the gate and drain quiescent biases of -6 and 25 V, respectively. As shown in Fig. 3.9, significant degradation in drain current was observed for the C-doped sample with thinner GaN channel layer, meaning more trapping effects. It is obvious that such trapping effects were caused by C-doping induced traps. It was reported that the trapping effects became severe when the doped buffer is located closer to the 2-DEG channel [17, 24, 31]. These acceptor level traps have been investigated by several groups using luminescence measurements focused on C-doped GaN bulk layers [32, 33].

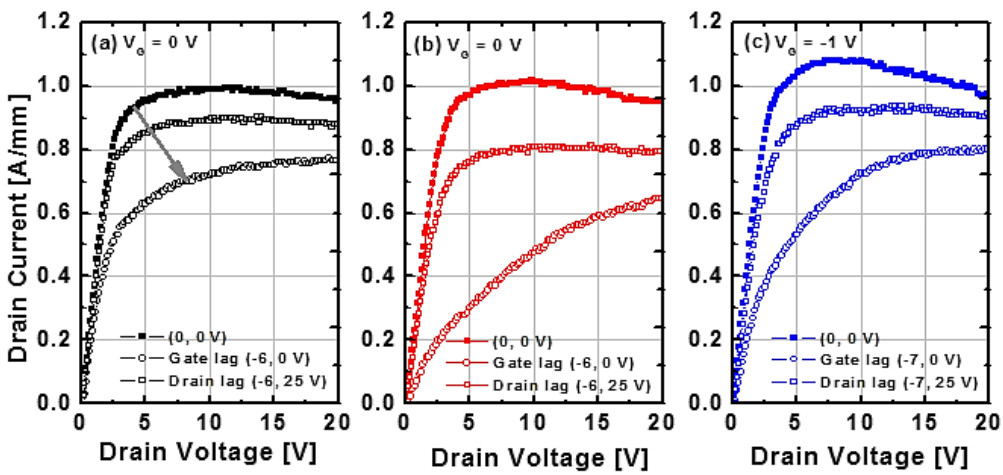


Fig. 3.9 Pulsed I-V characteristics of the devices with (a) un-doped buffer (b) C-doped buffer (350 nm GaN channel) (c) C-doped buffer (400 nm GaN channel). The pulse width and period were 200 ns and 1 ms, respectively. The quiescent bias conditions for the gate lag measurements were applied considering each threshold voltage, and drain lag measurements were 25 V, respectively.

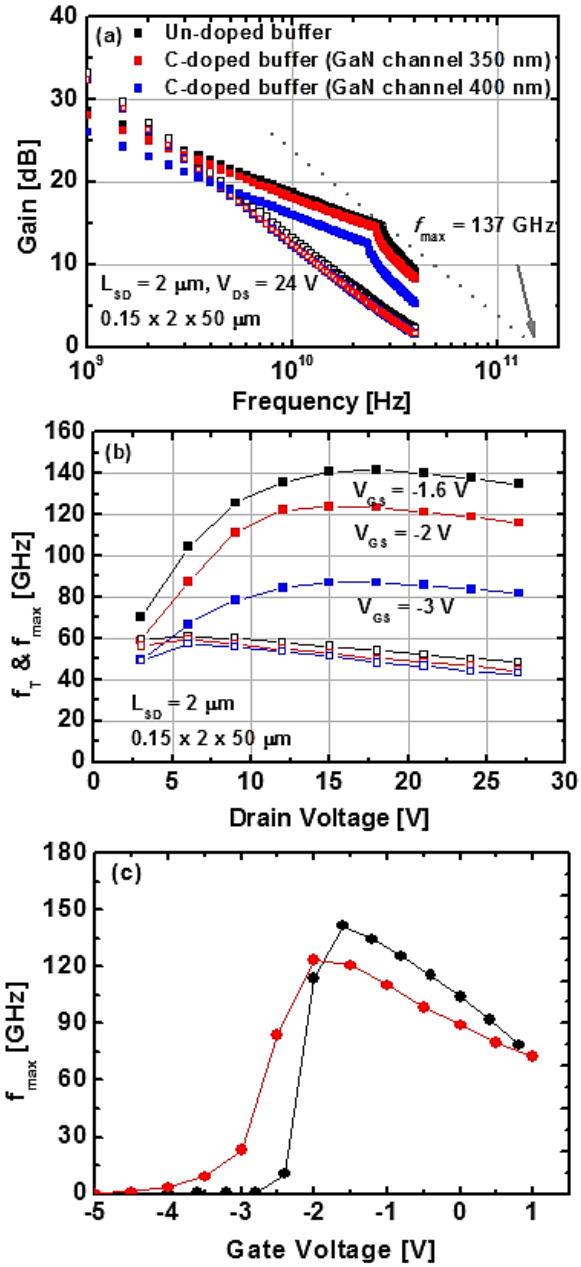


Fig. 3.10 (a) Small-signal characteristics of fabricated 2 × 50 μm devices with un-doped and C-doped buffer layers at gate voltage of -1.6 V, -2 V, and -3 V, respectively, considering each threshold voltage. (b) f_T and f_{max} characteristics as a function of drain bias voltages. (c) f_{max} characteristics as a function of the gate bias voltages.

Both small- and large-signal characteristics were measured for the fabricated 2 × 50 μm devices. The drain bias dependent f_T and f_{max} without de-embedding are plotted in Fig. 3.10. As expected from the channel modulation and pulsed characteristics, superior characteristics were obtained for the sample with the un-doped buffer layer. It should also be noted that the peak f_{max} was achieved at a relatively higher drain bias voltage for the un-doped buffer device: 15 V for the C-doped buffer devices, and 18 V for the un-doped buffer device. The large-signal characteristics measured at 18 GHz which was quite low in terms of gate length due to the limitation of load-pull [34] set up are compared in Fig. 3.11. Source and load matching were conducted at the input power of 15 dBm. The device with the un-doped buffer layer exhibited the maximum output power of 25.7dBm (≈3.7 W/mm). It is suggested that the smaller linear gain and faster gain compression observed for the devices with the C-doped buffer layers were attributed to the poor transfer characteristic and severe current collapse phenomenon.

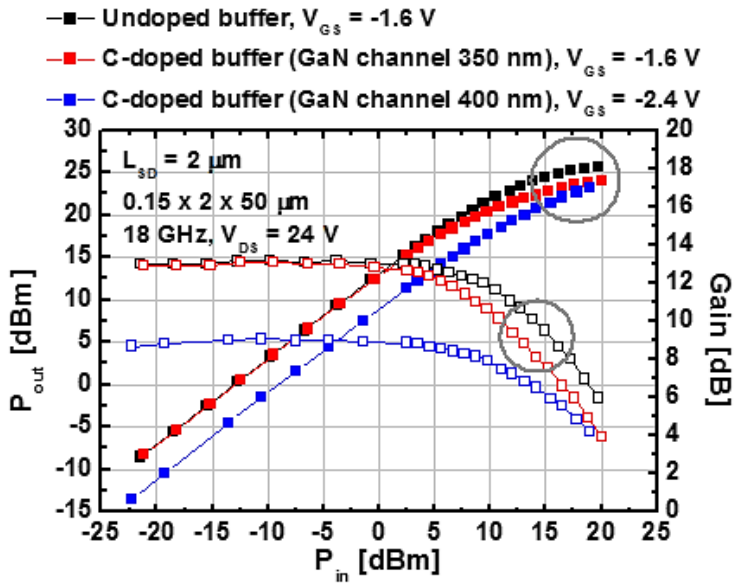


Fig. 3.11 Large-signal characteristics measured at 18 GHz with drain bias voltage of 24 V.

3.2.5 Analysis of Materials Properties

To understand the influence of C-doped buffer, PL measurements were carried out at different depths from the surface at 22 °C. It should be noted that PL related traps could be located not only at GaN channel but also at AlGaN barrier, so that the samples with different depths were prepared by low damage BCl_3/Cl_2 plasma etching: (i) on the GaN cap layer surface without being etched; (ii) at the GaN channel layer after removing the AlGaN barrier layer (etched depth = 25 nm), and (iii) at the GaN buffer layer after removing the GaN channel layer (etched depth = 500 nm for un-doped buffer wafer, 400 nm and 450 nm for C-doped buffer wafers, respectively). The measured spectra for un-doped and C-doped wafers are compared in Fig. 3.12. The band edge (BE) luminescence was obtained at ~3.4 eV, which was mainly

due to the transition between shallow donor and the Ga vacancy (V_{Ga}) deep acceptor level [35]. While no significant difference was observed between three wafers at the surface and GaN channel layers, the noticeable difference which was similar to previous reports about photoluminescence measurements of GaN bulk observed at the buffer layer. It should be noted that the etched depth for GaN channel layers is just under the 2DEG channel. In Fig. 3.12 (c), the C-doped buffer layers had lower BE luminescence intensities and higher yellow luminescence (YL) and blue luminescence (BL) intensities in comparison to the un-doped buffer layer, suggesting shallow donor compensation by C induced non-radiation recombination centers [5, 35]. The higher YL and BL intensities imply higher concentration of deep acceptor level defects that are responsible for the trapping effects observed in the pulsed characteristics. It was reported that the YL band was attributed to electron transitions from the conduction band minimum to the C_N, C_N-O_N complexes, or C_N-Si_{Ga} defect complexes [19, 36], whereas the BL band was attributed to electron transitions from C_{Ga} to C_N [5, 37]. Since the C-doped buffers have significant acceptor level defects, one can expect to see different PL profiles in GaN channel layers between these samples [28]. From the fact that no difference with BE-related luminescence at the surface and GaN channel layer was observed between these samples, it is indicated that the GaN channel layer on top of the C-doped buffers has considerable amount of donor level defects in comparison to the un-doped buffer sample.

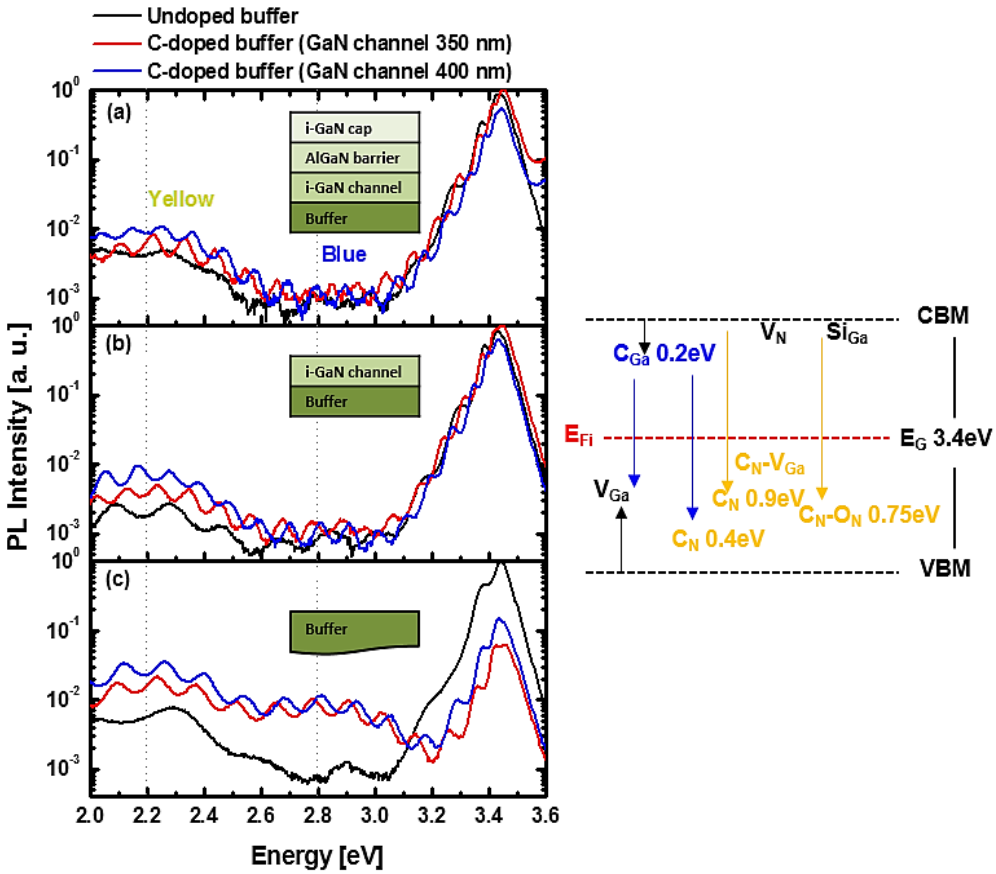


Fig 3.12 PL spectra of the samples (a) on the GaN cap layer surface (b) at the GaN channel layer, and (c) at the GaN buffer layer. The measurements were carried out with the wavelength of 266 nm.

Further investigation was performed for the sample with un-doped buffer and C-doped buffer (350 nm GaN channel layer representatively) by dynamic SIMS (magnetic sector SIMS) measurement with Cs+ of 15 keV gun and 20 nA to find out the relationship between near BE luminescence regime and extra carriers in the GaN channel layer which response to the horizontal field with drain voltage (Fig. 3.13).

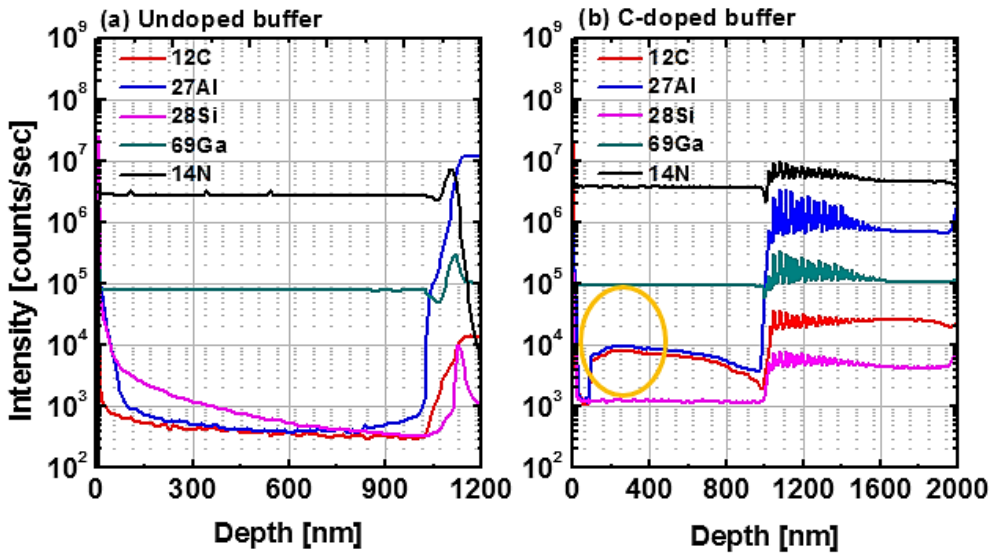


Fig. 3.13 Raw data of measured SIMS profiles for wafer structure 1 and 2, respectively. Oxygen and silicon impurities were also detected through all depth of wafers.

C was detected at the GaN channel layer due to the residual carbon from the underneath C-doped buffer, which would generate trap centers. It was found that Al profile in the data was not matched with the wafer structure but followed on C profile at the GaN channel layer. To confirm the wafer structure, Fig. 3.14 shows the raw intensity profiles of detected ions plotted with the estimated depth from TEM (Transmission Electron Microscope) measurement, and no Al was detected at the GaN channel and half of the buffer. This is because an atomic mass of Al is similar with C-N complex which means C_{Ga} or C-H-N complexes. C_{Ga} can act as not only a trap center but also a shallow donor state with transition level of 0.20 eV below the conduction band minimum that can provide extra carriers which, in turn, caused slow turn-on/off characteristics.

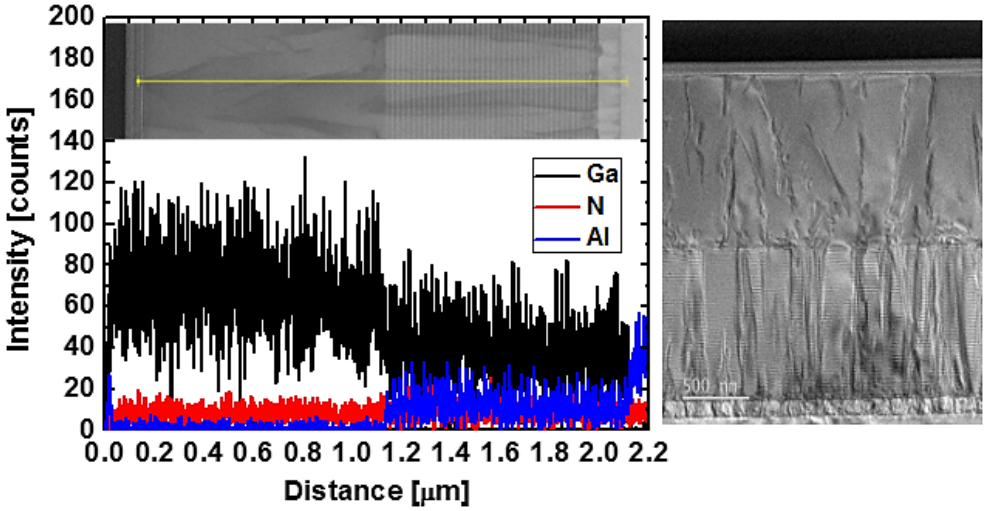


Fig. 3.14 The result of TEM energy dispersive spectroscopy (EDS) for the wafer with C-doped buffer.

Therefore, it is suggested that the C induced donor states in the GaN channel layer are responsible for the relatively poor transfer and off-state breakdown characteristics of the short channel device. While the C-doped buffer employed in AlGaN/GaN heterostructure is known to have advantages of leakage current reduction and breakdown voltage enhancement, careful attention must be paid to the drawback of RF performance degradation at microwave or higher frequencies. As a result, we have decided to employ AlGaN/GaN heterostructure without doping at buffer for Ka-band GaN HEMT device due to the higher RF performances and not that low breakdown voltage on short channel device which could demonstrate enough high operation voltage.

3.3 Passivation Process

In this section, we investigated the impact of passivation process on current collapse phenomenon and achieved the effective passivation process without increasing the thickness of dielectric layer due to parasitic capacitances. Not only protecting the surface of the fabricated device but also compensating the surface states and mitigating the peak electric field combined with field-plate structure are the main purpose of passivation process. Firstly, conventional SiN_x passivation process was employed with various conditions in terms of plasma damage on the surface during SiN_x deposition [38] and density of dielectric layer for blocking moisture which might induce oxygen at GaN surface [39]. After that, SiN_x and high-k dielectric were adapted with constructing dual passivation layer to achieve the higher breakdown voltage and better current collapse phenomena than single passivation layer.

3.3.1 Current Collapse for GaN HEMT

To be specific, the current collapse phenomenon is one of the most important issues in GaN device technology. The origins of current collapse phenomenon are hard to define simply. The most of origins are induced from GaN epitaxial layers such as buffer traps, GaN channel traps, AlGaN barrier traps, or surface traps (Fig. 3.15). Except the surface traps, GaN growth condition primarily influences on the trap densities so that the current collapse phenomenon caused by those traps are quite independent with front process technologies. As we referred in chapter 3.2, the acceptor-like traps in the GaN buffer or channel layers can make electron trapping at operation condition

with high drain voltage [10, 23, 24], but the surface traps are mainly due to donor-like traps such as N-vacancies [40, 41].

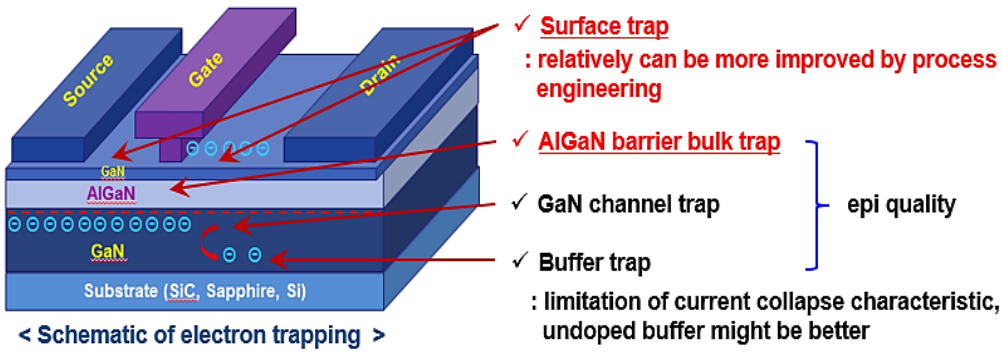


Fig. 3.15 The structure of AlGaN/GaN HEMT and location of various traps.

In principle, the donor level states in bulk layers can be the source of electrons for the 2DEG in AlGaN/GaN heterostructure and they are induced by growth condition. However, such traps at the GaN surface are the main source of the 2DEG inherently by transferring the electrons from occupied surface states to empty conduction band states of the AlGaN/GaN interface, leaving behind positive surface charge [42]. Thus, the surface donor-like traps are unoccupied and positively charged under no external field and occupied with electrons (neutralized) during large negative pulsed gate voltage ($V_{GS,Q}$) which form a virtual gate at an edge of the gate resulted in depleting the electrons in the 2DEG [40] as shown in Fig. 3.16. The depletion of electrons in the 2DEG incurs the decrease of drain current density what is called current collapse phenomenon.

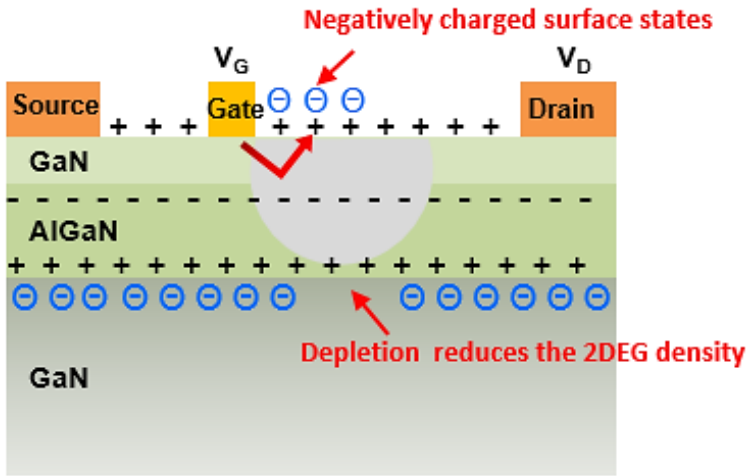


Fig. 3.16 Schematic representation of the charge distribution in a GaN-based HEMT and the effect of the virtual gate.

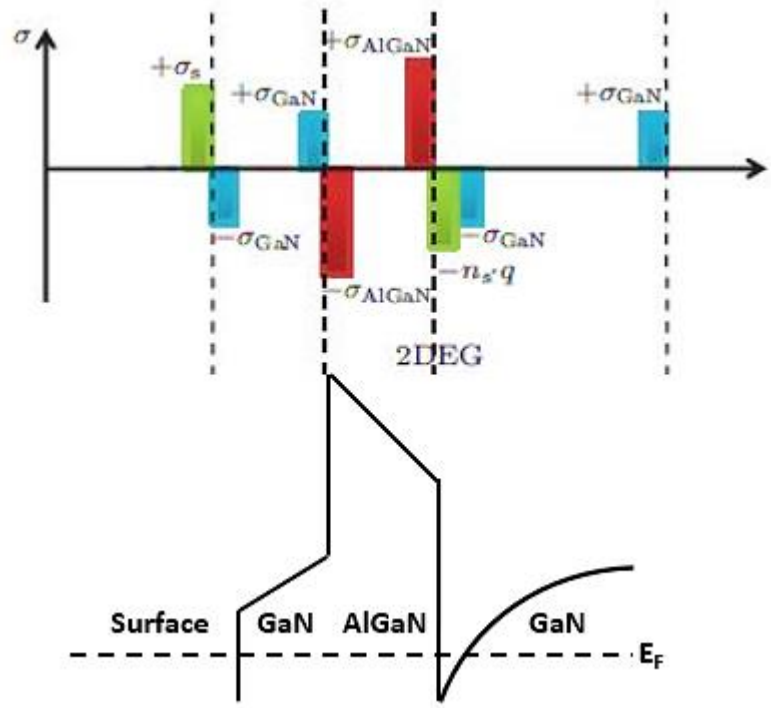


Fig. 3.17 Charge distribution and conduction band diagram of GaN cap/AlGaN/GaN heterostructure.

In GaN RF device, the decrease of maximum drain current density during operation makes a small output load-line and degradation of output power with early gain compression (i.e. distortion of output signal). These surface traps additionally can be generated during the process of the device, such as plasma damage and thermal damage [38, 43]. There are myriad of methods to suppress current collapse phenomenon such as surface treatment (wet or plasma), field-plate, passivation with effective dielectric, or modulation of epitaxial layer [44-51]. Our approach was focused on the surface traps and how to mitigate peak electric field effectively to reduce current collapse phenomenon.

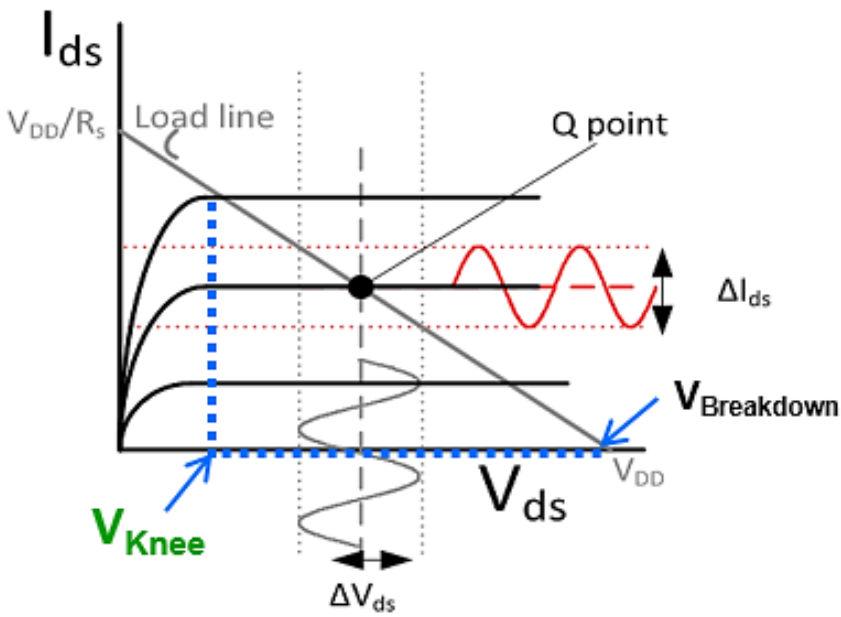


Fig. 3.18 I-V characteristics with load line showed to maximize the region of the RF power triangle.

3.3.2 SiN_x Passivation

Successful surface passivation prevents the surface states from being neutralized by trapped electrons which causes surface depletion and current collapse. The SiN_x is the most famous dielectric material for passivation layer at GaN device process due to the high quality of interface state. In general, the SiN_x layer is deposited with SiH_4 (with Ar) gas and N_2 or NH_3 plasma in CVD chamber. The disadvantage of the plasma enhanced CVD (PECVD) is the damage on the surface during deposition process by induced plasma [52]. The plasma damage varies with plasma power, but too low plasma power leads to poorer quality of SiN_x layer. So firstly, we used both remote PECVD to reduce plasma damage and Catalytic-CVD (Cat-CVD) [53] which do not use plasma for dielectric deposition in this research. Table. 3.2 indicates the conditions of both passivation processes.

Table 3.2 Process details of PECVD (top) and Cat-CVD (bottom) SiN_x deposition.

	$SiH_4/N_2/Ar$ [sccm]	**Pressure [mTorr]**	**Source power [W]**	**Chuck temp. [°C]**	**Dep. Rate [Å/sec]**
Remote PECVD (ICP-CVD)	2.8/9/90	35	200	400	0.55

	$SiH_4/NH_3/H_2$ [sccm]	**Pressure [mTorr]**	**Wire Temp. [°C]**	**Chuck temp. [°C]**	**Dep. Rate [Å/sec]**
Catalytic CVD	2/10/25	30	1700	400	0.9

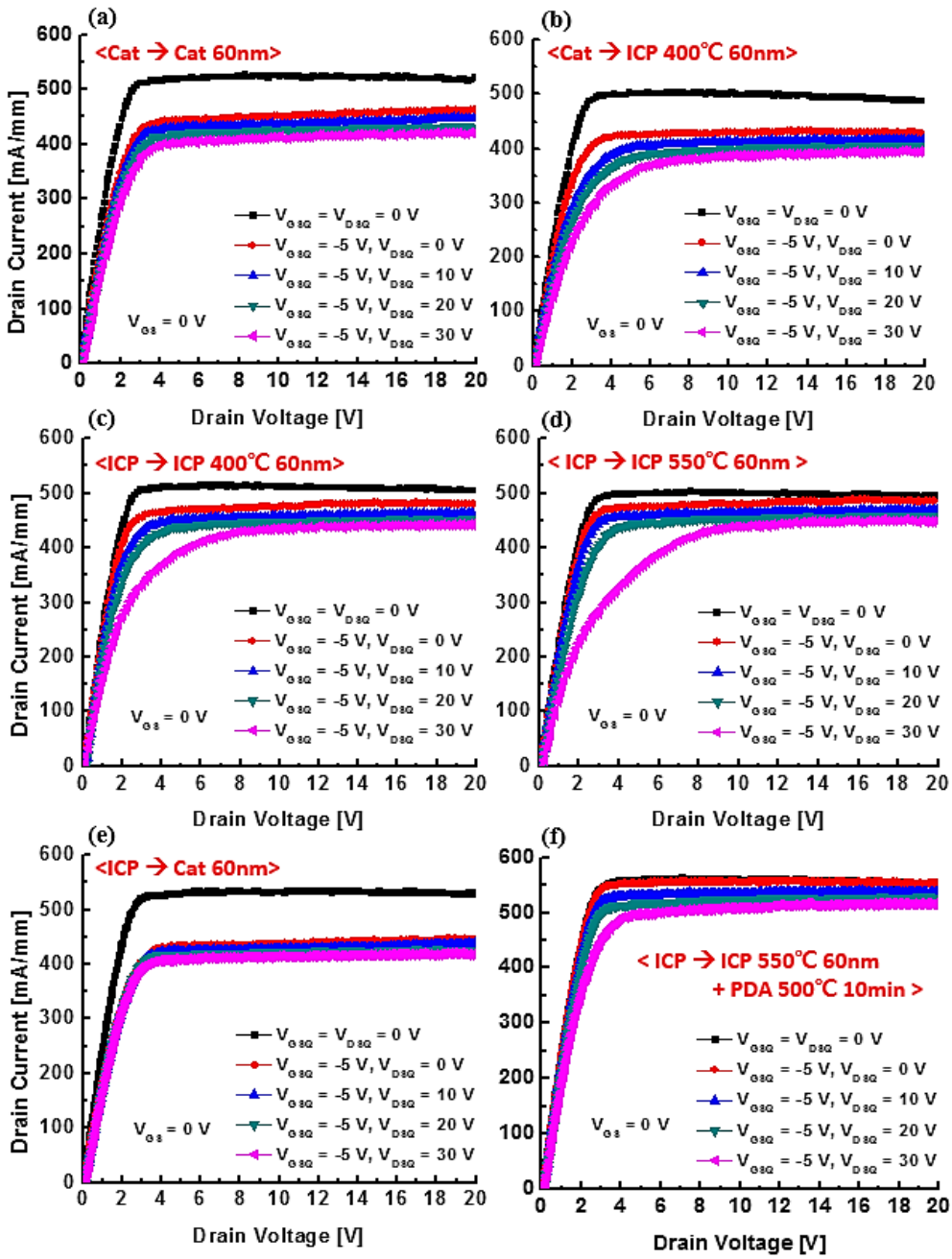


Fig. 3.19 The current collapse phenomena with different passivation process. The pulse width and period of pulsed I-V measurements were 200 ns and 1 ms, respectively.

Estimation of current collapse phenomenon was performed with AlGaN/GaN Schottky HEMT fabricated by our standard process. The gate length of the device was 2 μm, and the distance between the gate and drain (L_{GD}) was 7 μm, and the passivation layer of 60 nm-thick was employed equally at all samples. The sheet resistance of used epitaxial structure was 318 Ω/sq. Figure 3.19 shows each result of passivation process with various re-deposition (chapter 2) conditions. The device with passivation process using Cat-CVD demonstrated large initial current collapse when the $V_{GS.Q}$ was applied, but no more significant current collapse was observed. However, the devices with passivation process using remote PECVD presented good current collapse initially and large current collapse occurred after the $V_{DS.Q}$ was applied. There was only the difference at initial current collapse by the $V_{GS.Q}$ between two chuck temperatures. We could derive the main cause of the differences in both passivation processes by different measurement and post deposition annealing (PDA). The $V_{DS.Q}$ generally affected on current collapse phenomenon by inducing stress on the surface traps to the drain side and the bulk traps in the GaN epitaxial layers. So we measured only with the $V_{GS.Q}$ (gate lag) and $V_{DS.Q}$ (drain lag) respectively to separate each effect even though the measurement without $V_{GS.Q}$ also can be added the thermal effect a little bit, because the 2DEG channel might not be depleted at this condition. Figure 3.20 shows two different measurements for both passivation processes. The remote PECVD process occurred gate lag phenomenon continuously as the $V_{GS.Q}$ increased whereas the Cat-CVD process occurred gate lag phenomenon only at initial $V_{GS.Q}$. This indicated the peak electric field near the gate edge of the device with the remote PECVD process which was directly related to the $V_{GS.Q}$ was gradually increased with the increase of $V_{GS.Q}$, and the plasma damage was still induced on the surface during the SiN_x deposition. Also, the existence of plasma damage could be observed through

PDA process only for PECVD passivation by reduction of current collapse (Fig. 3.19 (f)) and the drain off-state leakage current density as shown in Fig. 3.21. From these results, we decided that the Cat-CVD process might be better for the surface condition even though the initial $V_{GS,Q}$ made gate lag phenomenon.

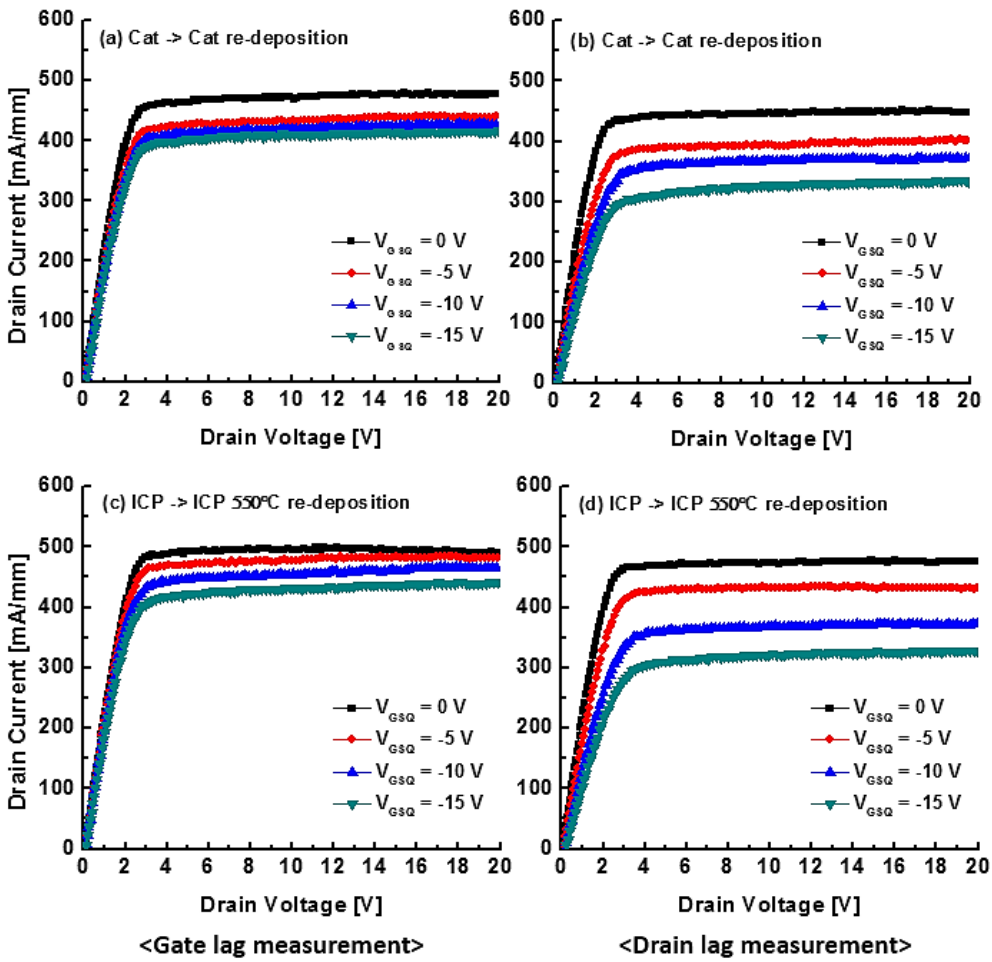


Fig. 3.20 Pulsed I-V measurements for both PECVD and Cat-CVD passivation with only negative V_{GSQ} stress and positive V_{DSQ} stress, respectively. The pulse width and period were 200 ns and 1 ms.

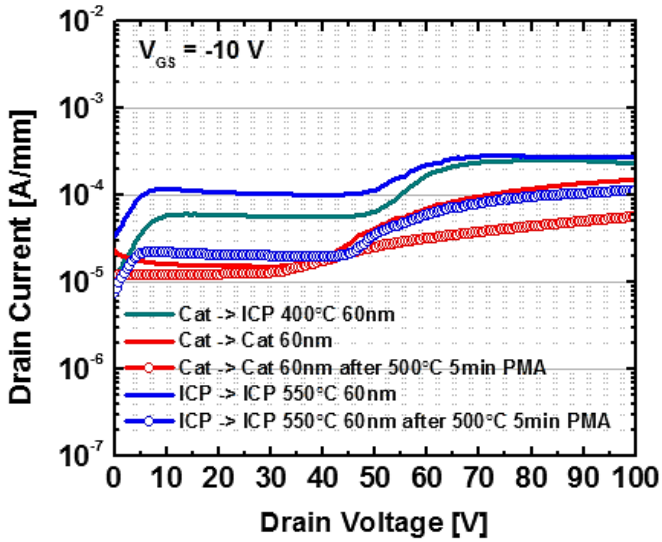


Fig. 3.21 Drain off-state leakage current characteristics of various conditions of passivation processes. The post annealing results were performed with post-gate metallization annealing (PMA) at 500 °C 10 min instead of PDA.

We tried to find out the way to solve the phenomenon with the initial $V_{GS.Q}$ for the Cat-CVD process. Both passivation processes have different deposition rate and etching rate, so the density of the SiN_x layer by using Cat-CVD might be low which means the surface was not enough blocked from the air (oxygen) [39]. The way we found was dual passivation structure with remote PECVD and Cat-CVD. The upper SiN_x layer by using remote PECVD effectively blocked the GaN surface from the air, but the drain off-state leakage current density was increased in comparison to the single SiN_x layer using Cat-CVD even though the current collapse phenomena were remarkably improved (Fig. 3.22 and Fig. 2.23). This result was because the bottom SiN_x layer was too thin to form stable dielectric structure. We could find the solution by increasing the thickness of the bottom SiN_x layer using Cat-CVD and reducing the thickness of the upper dielectric layer with high-k dielectric instead of SiN_x ($\varepsilon_r = 7$) in the next section.

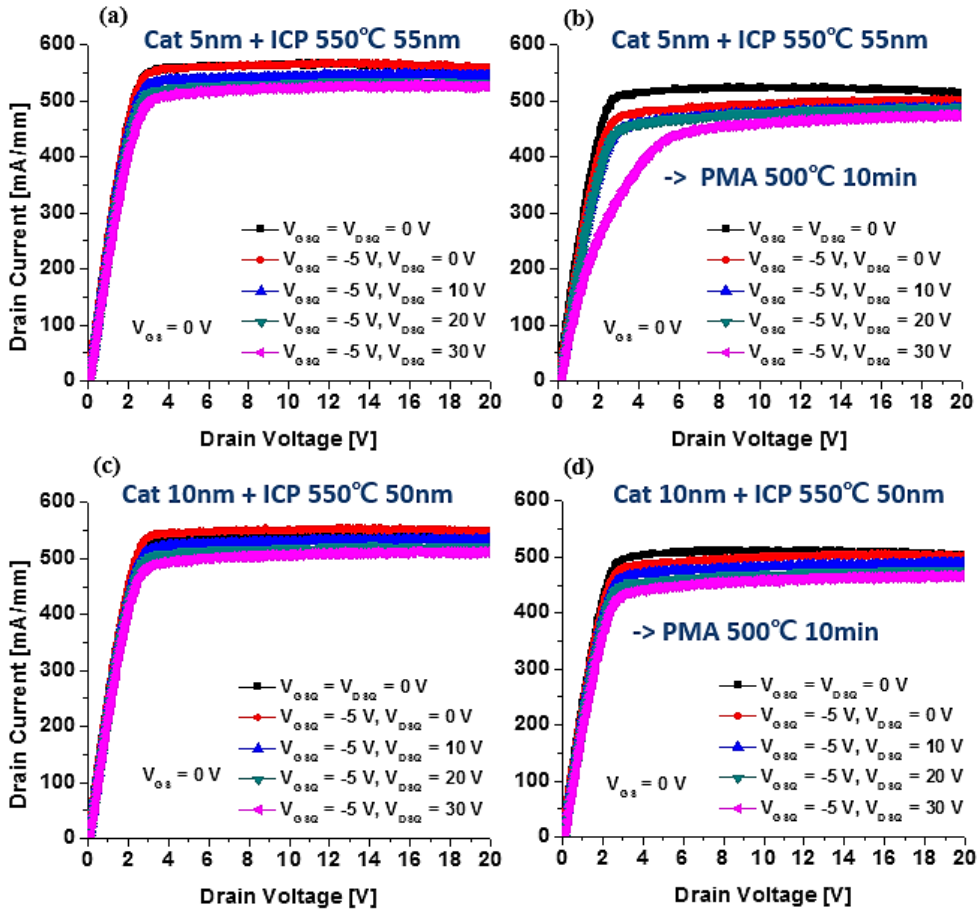


Fig. 3.22 Pulsed I-V characteristics of the devices with dual SiN_x passivation with different thickness of bottom interfacial layers before and after PMA.

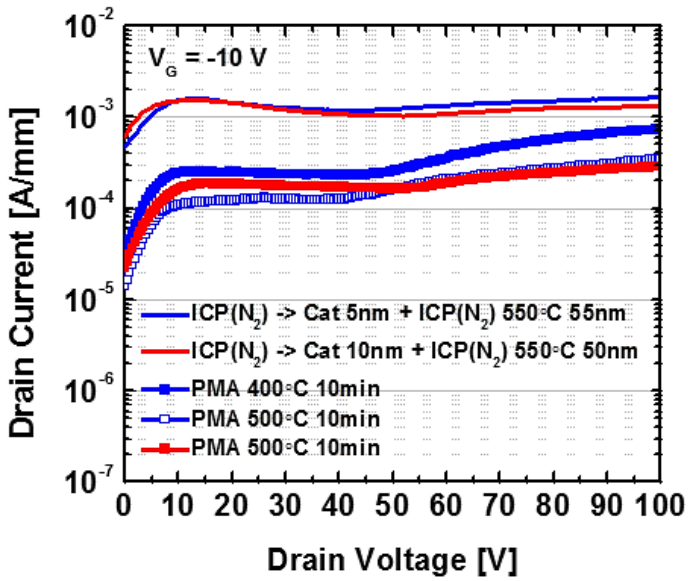


Fig. 3.23 Drain off-state leakage current characteristics of dual SiN_x passivation with different thickness of bottom interfacial layers before and after PMA.

3.3.3 Dual Passivation with High-k Dielectric

In this research, we focused on effective passivation process in terms of the current collapse phenomenon and the breakdown voltage of the devices without increasing the thickness of passivation layer. The high-k dielectrics have been investigated about their effects on electric field and breakdown voltage through the simulation work [54-56].

$$\nabla \cdot (\varepsilon \nabla \varphi) = -q(p - n + N_{Di} + N^{+}{}_{DD} - N^{-}{}_{DA})$$

$$\nabla \cdot J_n = -qG + q(R_{DD} + R_{DA})$$

$$\nabla \cdot J_p = qG - q(R_{DD} + R_{DA})$$

$$G = (a_n|J_n| + a_p|J_p|)/q$$

However, there were no actual results of the fabricated device with the high-k dielectric considering the electric field. We employed HfO_2 (ε_r = 17) as the high-k dielectric on AlGaN/GaN Schottky HEMT to achieve both blocking the oxygen from the air and decreasing the peak electric field near the gate edge using atomic layer deposition (ALD) process. Firstly, the long channel device with the same size with the above section was also fabricated for evaluation on the epitaxial structure with sheet resistance of 350 Ω/sq (Fig. 3.24 (a)). Figure 3.24 (b) shows the transfer characteristics of the fabricated devices with having slightly positive shift on dual passivated devices. As the ratio of the HfO_2 layer increased (Fig. 3.25), the current collapse phenomenon was significantly improved in comparison to the single SiN_x for passivation layer, and this result was attributed to reduction of electric field toward the drain side. Also, the breakdown characteristics were measured, but no remarkable differences were observed with long channel devices.

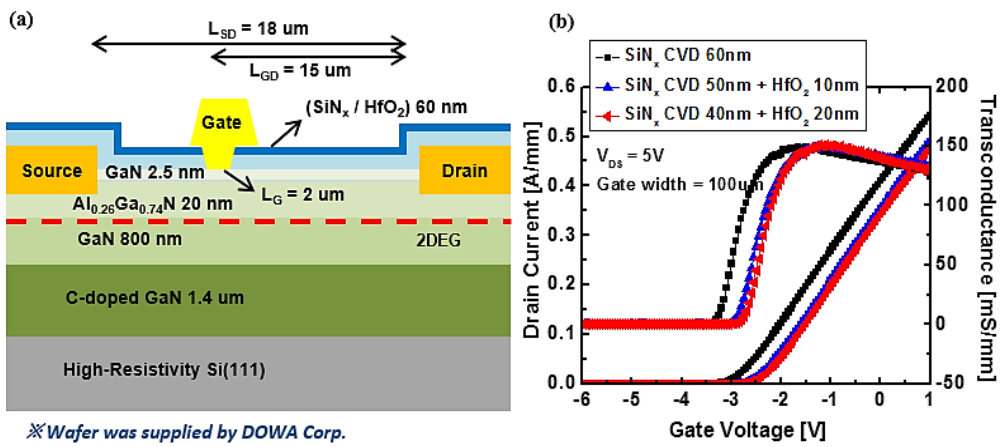


Fig. 3.24 (a) The structure of fabricated AlGaN/GaN Schottky HEMT device with SiN_x/HfO_2 dual passivation layer. (b) The comparison of transfer characteristics between single and dual passivated devices.

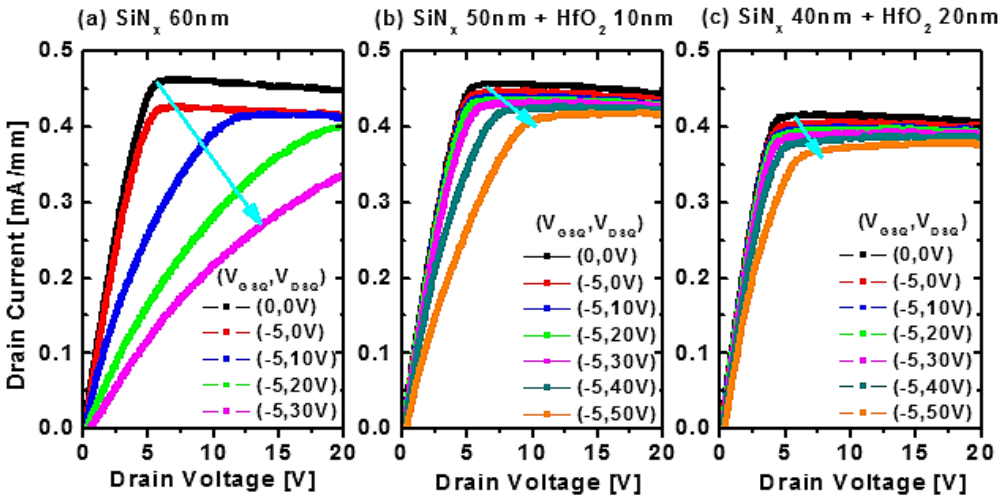
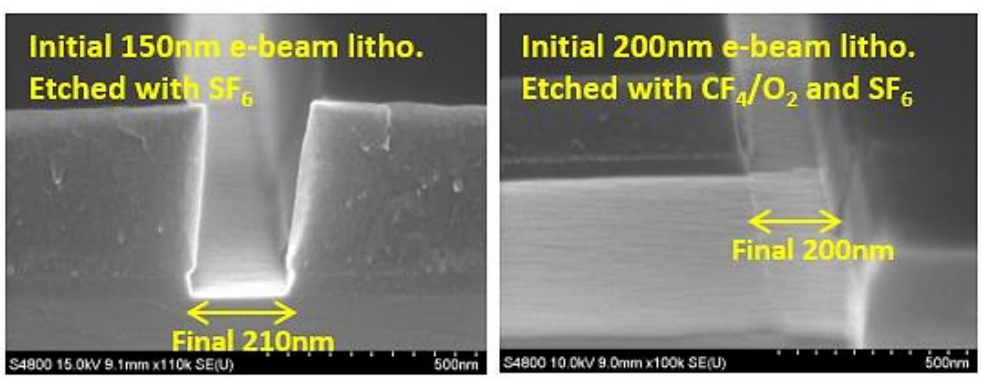


Fig. 3.25 Pulsed I-V characteristics of the devices with three different passivation layers. The total thickness of passivation layer was same as 60 nm and only the portion of HfO_2 layer was changed.

3.3.4 Results on Sub-micrometer Device



< SiN_x gate pattern > **< SiN_x + HfO_2 gate pattern >**

Fig. 3.26 SEM images after gate foot etching for both single SiN_x and dual SiN_x/HfO_2 passivation layers. The final gate lengths were similar as 200 nm.

Ultimately, the sub-micrometer device induced higher electric field with L_{SD} = 2 μm and L_{GD} = 1.4 μm was fabricated and evaluated their characteristics. To define the gate length of 200 nm for both passivation processes had different initial pattern length (Fig. 3.26) because the etching rate of HfO_2 was much lower than SiN_x. We used the thinner AlGaN barrier of 12 nm with Al content of 30 %, and GaN channel layer of 350 nm with 2 μm C-doped GaN buffer for the wafer structure in this experiment which was more suitable for high frequency application. Figure 3.27 shows notable improvement of the current collapse at the device with dual passivation layer with the HfO_2 of 15 nm-thick, and more improvement was achieved at longer length of field-plate whereas the SiN_x passivation layer with longer field-plate demonstrated less improvement of current collapse which indicated the different effectiveness of passivation layer with same distance from the gate edge to the edge of field-plate in terms of the electric field distribution. As same with the section 3.3.2, we measured the gate lag phenomenon to make the effects clear (Fig. 3.28). As the ratio of the HfO_2 layer increased, not only the initial gate lag phenomenon that we mentioned above but also the total gate lag phenomenon was remarkably suppressed that implied the effective mitigation of electric field even if the channel length of the device was short. Figure 3.29 shows the breakdown characteristics of the fabricated devices with different L_{SD}. It was obvious that the device with SiN_x/HfO_2 dual passivation layer demonstrated the higher and more uniform breakdown characteristics than SiN_x single passivation layer versus L_{SD}.

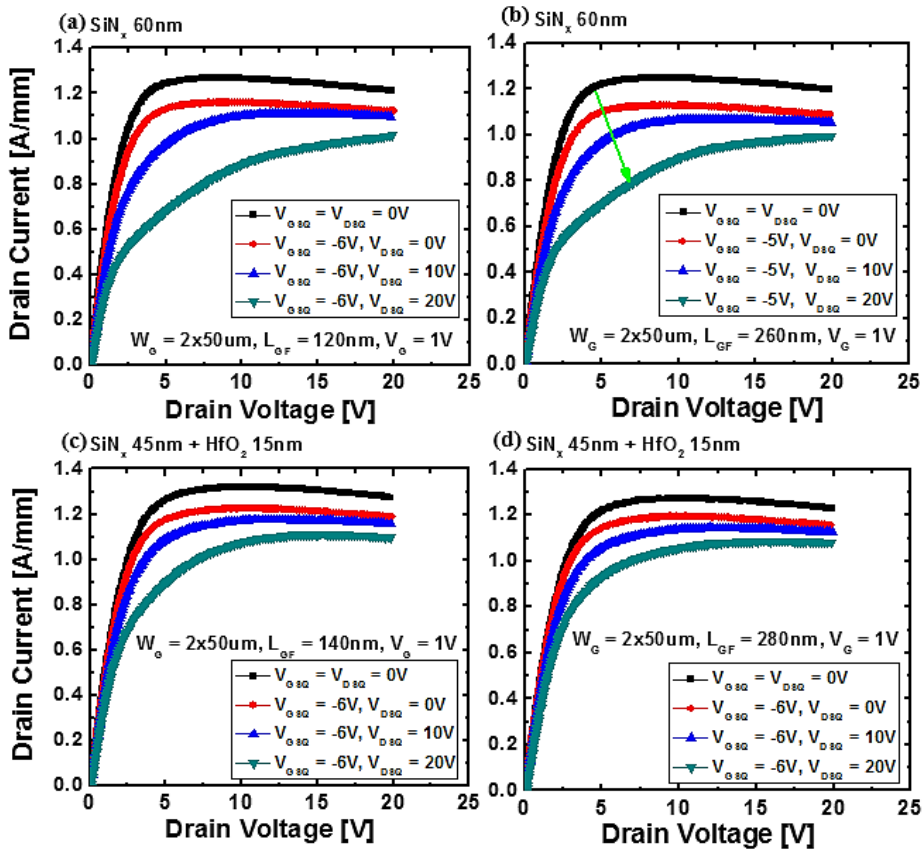


Fig. 3.27 Pulsed I-V characteristics of fabricated 0.2 μm AlGaN/GaN HEMTs-on-Si with different length of gate field-plate (L_{GF}).

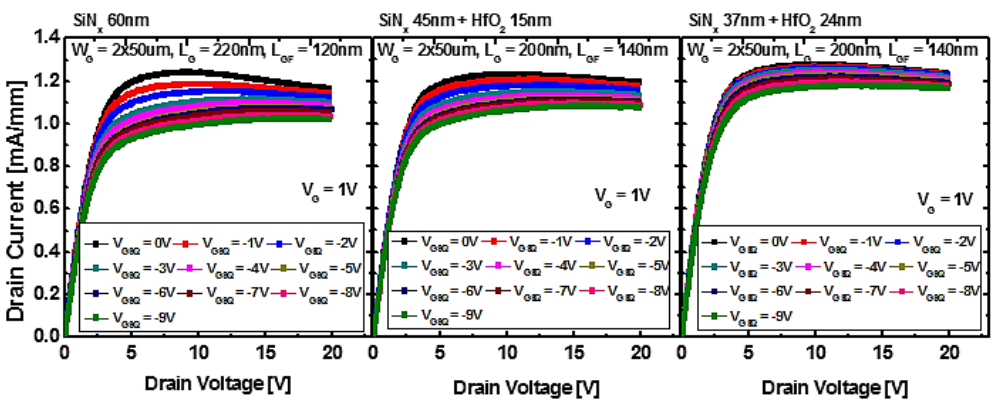


Fig. 3.28 Pulsed I-V characteristics only with increasing negative VGSQ for each device.

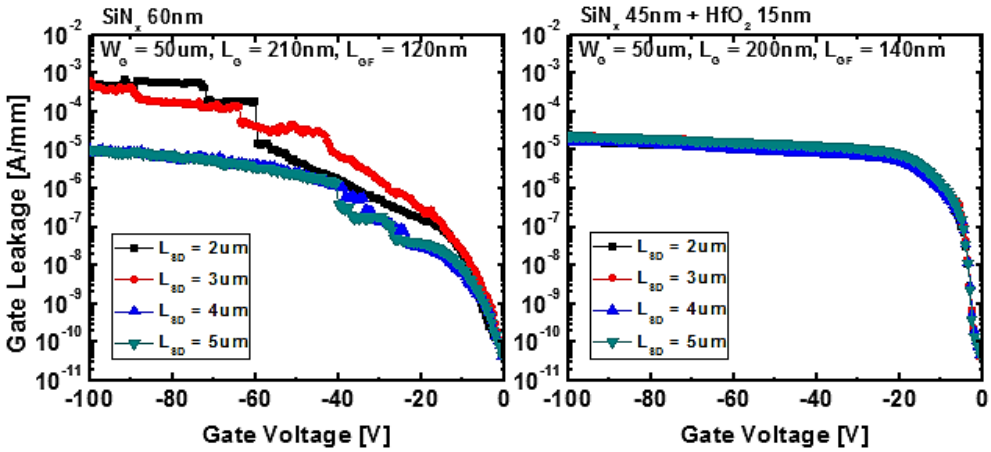


Fig. 3.29 Gate to drain 2-terminal breakdown measurements for devices with both single and dual passivation layers.

However, we had to consider about the small-signal characteristics when the high-k dielectric was employed at RF device even though the current collapse and breakdown voltage were improved. The equivalent circuit of the intrinsic FET model also contained the low-frequency dispersion effect with the thermal and trap sub-circuits. The extracted small-signal parameters are plotted in Fig. 3.30. The f_{max} of the devices with SiN_x/HfO_2 dual passivation layer exhibited the higher values than the device with SiN_x single passivation layer. From our extraction method, notable increases of parasitic capacitance (C_{gs}) were found due to high-k dielectric between the source and drain. Despite the increased parasitic capacitances, the extracted intrinsic G_m was much more increased resulted in the higher f_T and f_{max} as the ration of HfO_2 increased. The higher G_m might be attributed to different gate length, but the improved gate lag phenomenon also could influence on G_m. Further investigation will be needed to clarify the impact of high-k dielectric on small-signal characteristics [58].

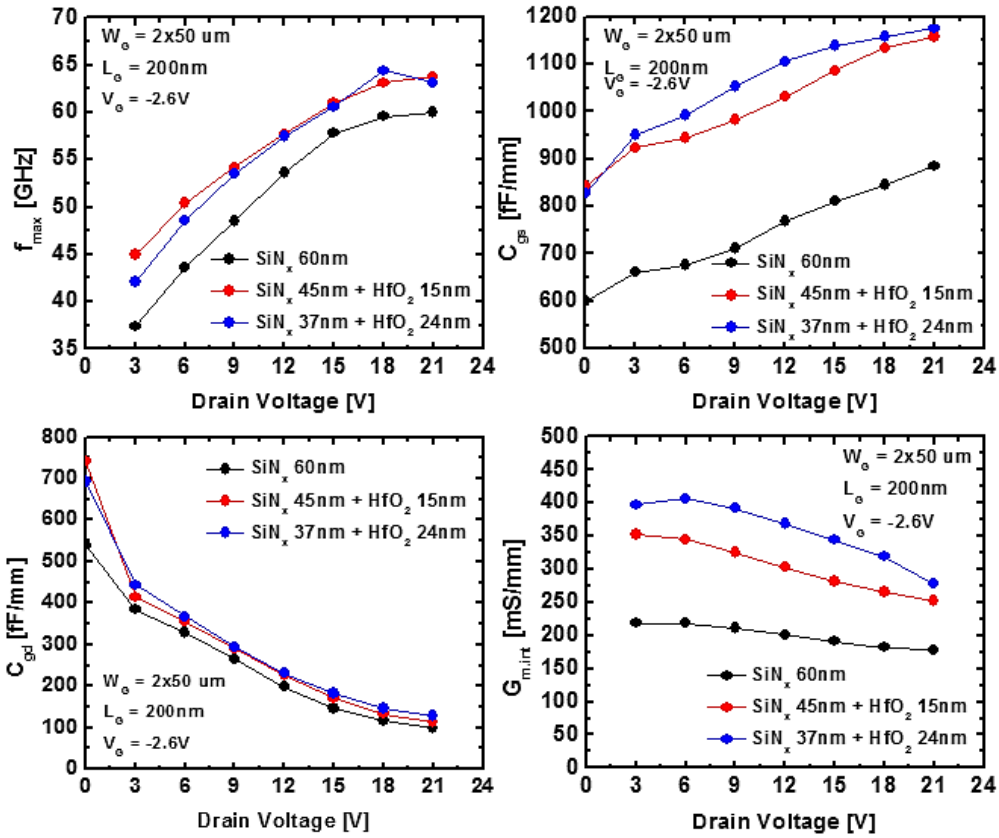


Fig. 3.30 Extracted small-signal parameters versus drain voltages for the devices with three different passivation layer.

3.3.5 Process Issues of Dual Passivation

Unlike the long channel device (L_G = 2 μm), the device with the gate length under few hundred nm is generally hard to define the exact gate length due to the etching process of the passivation layer for making Schottky contact. At dual passivation process, defining the gate length could be much more difficult because of the obvious difference of etching rate among two dielectric layers. Figure 3.31 (a) shows the process issue by cross-sectional

image. CF_4/O_2 gas [59] was used to remove HfO_2 layer with 50 mTorr 100 W and SF_6 gas was used to remove SiN_x layer with 100 mTorr 20 W at RIE both. Because the high plasma power was required to remove the HfO_2 layer, the bottom SiN_x layer could not be as an etching stop layer. Also, the etching rate of the SiN_x layer was varied after the plasma which was used in HfO_2 etching reacted with the SiN_x (Fig. 3.31 (b)). Thus, the finally defined gate profile was unstable as shown in Fig. 3.32 and it was easy to form undercut profile.

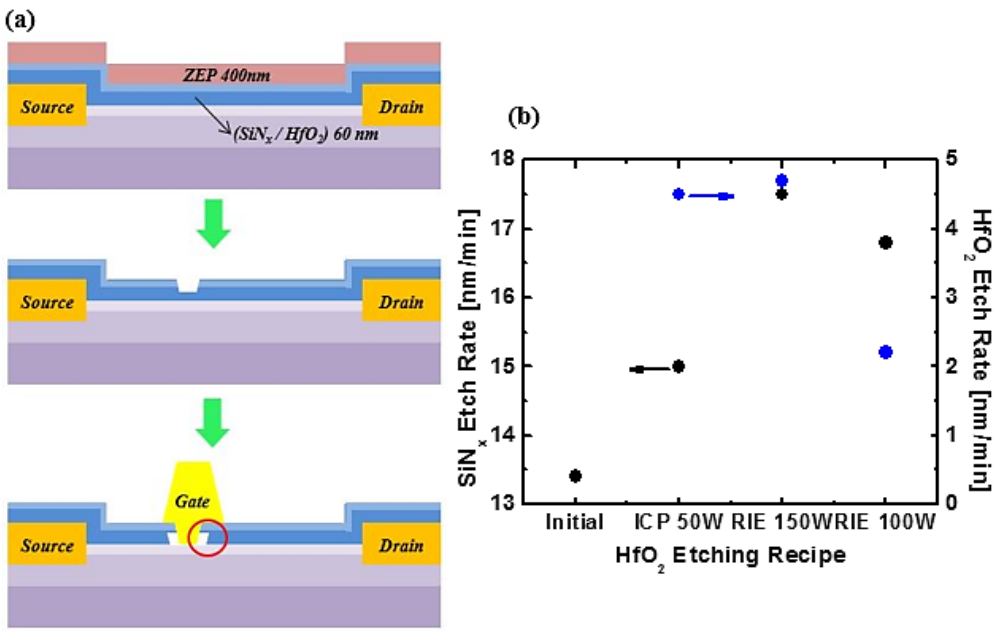


Fig. 3.31 (a) Problem with undercut profile after SiN_x/HfO_2 dual layer etching. (b) The etching selectivity and change of etching rate of SiN_x bottom layer before and after HfO_2 etching.

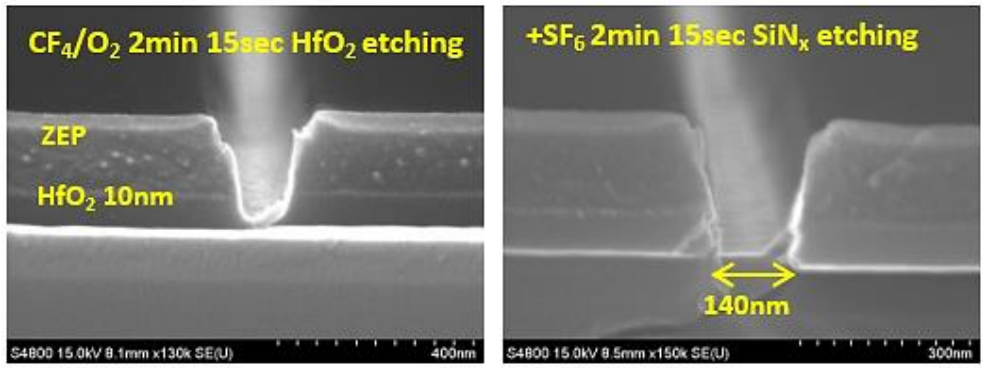


Fig. 3.32 SEM images of two-step etching for dual passivation layer. First-step was CF_4/O_2 high power etching for HfO_2, and second-step was SF_6 low power etching for SiN_x.

3.4 References

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Chapter 4. Recessed MIS AlGaN/GaN HEMTs for Ka-band Application

4.1 Introduction

This chapter will describe the device with other gate structure which called metal-insulator-semiconductor (MIS) instead of Schottky contact. The MIS structure is very common in semiconductor technologies to reduce the gate leakage current, and the GaN devices have employed MIS structure for various applications either [1, 2]. Also, there were some results of sub-micrometer GaN device with MIS structure by using several dielectrics [3, 4], but the researches have been limited to the device level.

We adapted MIS structure using high-k dielectric to achieve both the lower current collapse without the issue of passivation process that we mentioned in last chapter and higher breakdown voltage so that the higher output power of the device and MMIC could be made. In addition, the interface between the compound semiconductor and high-k gate dielectric generates a lot of trap states which can occur short channel effect, especially drain induced barrier lowering (DIBL) that reduces cut-off frequency of the device [5, 6]. So we employed thin SiN_x interface layer of 1.5 nm to improve the quality of interface using remote PECVD with ALD mode [7].

4.2. Gate Recess Etching Process

Gate recess etching process is one of the most general methods to control the threshold voltage (V_{th}) in GaN device technology [8]. For GaN power device, the gate recess etching process is employed to make positive V_{th} which is called "normally-off" by depleting naturally existent electrons in 2DEG channel [9]. However, the main purpose of gate recess etching process for GaN RF device is not moving V_{th} positively but an implementation of high aspect ratio by reducing the distance between the gate and 2DEG channel with maintaining "normally-on" state [10]. To be specific, the aspect ratio must be considered with gate dielectric on MIS structure (Fig. 4.1). It should be noticed that the etching depth impacts on device performance [11, 12]. Increase of etching depth reduces the thickness of AlGaN barrier layer, so that the polarization effect can be decreased resulted in lowering the density of 2DEG channel. Also, the electrons in 2DEG channel are sensitively affected by recess etching condition such as plasma power or pressure which can induce the damage on the etched surface [13, 14]. The damaged surface generates N-vacancies or other trap states that can cause the non-ideal device characteristics, for example, low drain current density, low transconductance due to low electron mobility, and large hysteresis due to trapping effect.

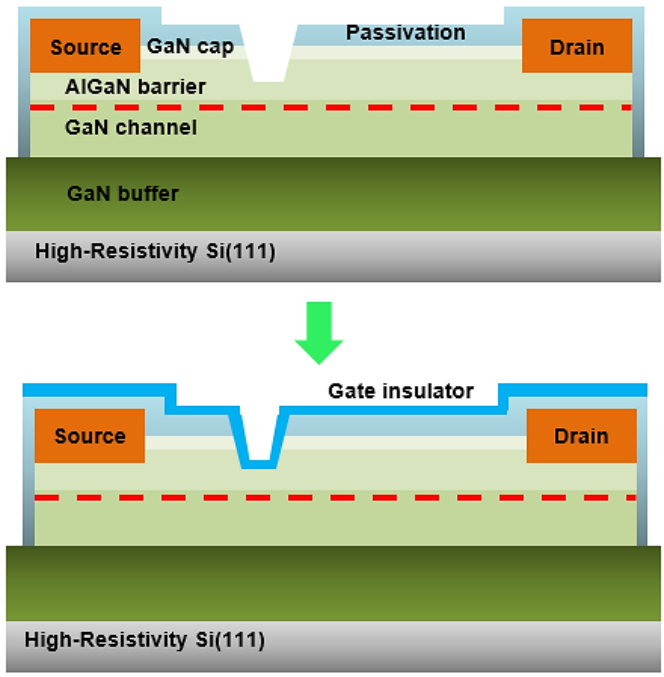

Fig. 4.1 Cross-sectional images of MIS structure with gate recess etching for maintaining high aspect ratio.

4.2.1 Damage and Recovery

We identified the effects of etching depth and the method of curing the damage to optimize the gate recess etching process for normally-on MIS device without any degradation of 2DEG properties even if the aspect ratio was maximized. Figure 4.2 plotted the results of electron mobility and sheet charge concentration by using Hall measurement versus the remained thickness of AlGaN barrier layer of AlGaN/GaN heterostructure. We could find the certain depth that made the abrupt decrease of electron mobility and sheet concentration. Before the depth that both electron mobility and sheet concentration decreased, the reduction of sheet concentration led to less

scattering than each initial condition resulted in the slight increase in electron mobility [15, 16]. Because it is hard to make the damage-free etched surface even though the plasma power is low enough, the damage curing process is required to avoid non-ideal 2DEG characteristics and achieve good MIS interface.

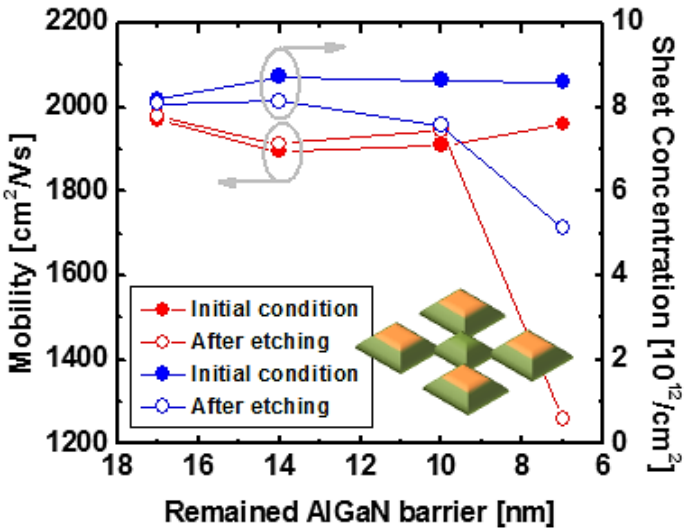

Fig. 4.2 Hall-measurement results with removing AlGaN barrier layer by BCl_3/Cl_2 power etching.

Figure 4.3 (a) shows the general methods of damage curing process and their impact of each method on 2DEG channel. After etching the surface of Van der Paw pattern until the degradation was generated considering the results of Fig. 4.2, N_2 plasma treatment and annealing process at N_2 ambient with RTA [17-19] were employed to identify the recovery of 2DEG properties. The annealing process with higher temperature demonstrated the most effective recovery rate in our work. Actually, there was another damage which should be regarded during deposition of the gate dielectric because of the plasma damage in CVD chamber either, so we investigated the 2DEG

properties after each process same as actual MIS device by using Hall measurement. As shown in Fig. 4.3 (b), the recess etching and plasma enhanced atomic layer deposition (PEALD) SiN_x [7] deposition for the gate dielectric using remote PECVD increased sheet resistance and decrease electron mobility gradually. This indicated dielectric deposition process additionally occurred the damage on 2DEG channel. The annealing process was finally employed to recover the induced damage totally, and the annealing temperature was 500 °C with 10 min which was the longer annealing time than previous results to compensate the lower annealing temperature. After the annealing process, the electron mobility was perfectly recovered and the value of sheet resistance was still higher than the initial value, but this was attributed to reduction of polarization effect due to the thin AlGaN barrier layer.

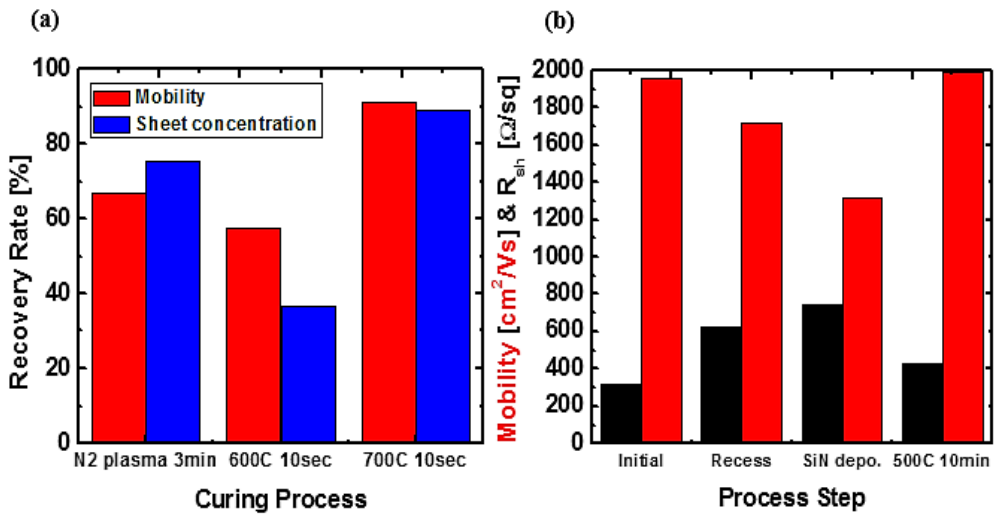

Fig. 4.3 (a) Hall-measurement results with various curing process of recess etching damage. (b) The effect on 2DEG channel of each process step when forming MIS structure.

4.2.2 Effects of Etching Depth on Device

In this section, we fabricated short channel recessed MIS-HEMT with 5 nm SiN_x as gate insulator by employing our standard process to investigate the effects of recess etching depth on devices characteristics. The epitaxial layers were grown on Si substrate consisted of a 2.5 nm GaN capping layer, 12 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, 350 nm undoped GaN buffer layer, and 2 µm C-doped GaN buffer layer. The used material showed carrier mobility of ~2000 cm^2/Vs. L_{SD} and L_{GD} of the fabricated devices were 2 µm and L_{GD} = 1.4 µm respectively. To evaluate the effects of recess etching depth on recessed MIS-HEMT, the gate regions of the devices were etched with masking by SiN_x passivation layer with each remained AlGaN layer of 4 nm, 7nm, and 10 nm, and we employed PEALD SiN_x of 5 nm-thick followed by post deposition annealing (PDA) at 500 °C with 10 min.

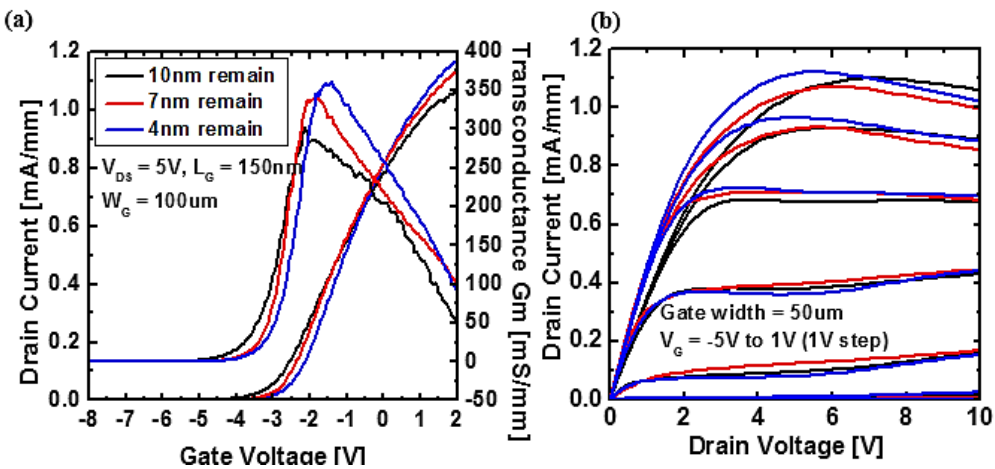

Fig. 4.4 (a) Transfer and (b) Output I-V characteristics of the fabricated 150 nm AlGaN/GaN recessed MIS HEMTs-on-Si with increasing gate recess etching depth.

We measured DC characteristics for fabricated devices of three different recess depths. As shown in Fig. 4.4 (a), the threshold voltages of the devices positively shifted as recess depth increased, and maximum transconductance (G_m) was improved with increasing of recess depth due to the high aspect ratio. Measured maximum G_m was 360 mS/mm at the device with remained AlGaN barrier layer of 4 nm at the drain voltage of 5 V. Reduction of the distance between 2DEG channel and gate metal enhanced aspect ratio and the ability of gate modulation. Also the effect of recess depth on static on-resistance (R_{on}) was evaluated from the drain current measurement through gate voltage from -5 V to 1 V (Fig. 4.4 (b)). We achieved maximum drain current of 1120 mA/mm at the gate voltage of 1 V, and R_{on} and knee voltages (V_{knee}) were reduced as the recess depth increased. Also, gate insulator was applied to sub-micrometer device to reduce gate leakage current originally. Figure 4.5 (a) and (b) show gate forward and reverse current densities for different recess depths respectively. There were no significant changes in forward current density until the gate voltage of 2 V. The low gate forward current density in MIS structure can help the device can operate with larger gate swing than Schottky gate device. However, gate reverse leakage currents by gate-drain 2-terminal measurement show remarkable tendency and difference among each recess depth. In general opinion, the vertical electric field is divided with the gate dielectric and AlGaN barrier layer, so breakdown voltage can be reduced when the remained thickness of AlGaN is decreased by recess etching. In our device, gate insulator was inserted between the gate metal and AlGaN that could generate early hard breakdown due to the thin dielectric. Figure 4.5 (b) shows gate reverse leakage current was reduced and breakdown voltage was improved as the recess depth increased which was different trend with general opinion with the gate recessed structure. This result indicated the breakdown occurred not only vertically but also laterally

which meant the direction through the sidewall of the gate insulator. Recess etching mitigated the electric field between the surface and gate edge, and breakdown voltage of gate insulator was increased. Finally, small-signal characteristics were measured from 10 MHz to 70 GHz with the devices of 2x50 μm gate width at the drain bias of 18 V (Table. 4.1). Contrast to DC performance, intrinsic G_m was high at the device with remained AlGaN barrier layer of 7 nm. This result caused higher f_{max} than other devices, and the reason why the tendency was different with DC transfer characteristics was unclear, but the device with smaller aspect ratio exactly showed larger short channel effect that could exhibit poor frequency response. This study presented optimization of the structure of normally-on recessed MIS in terms of DC and small-signal characteristics without any damage on MIS interface for RF applications.

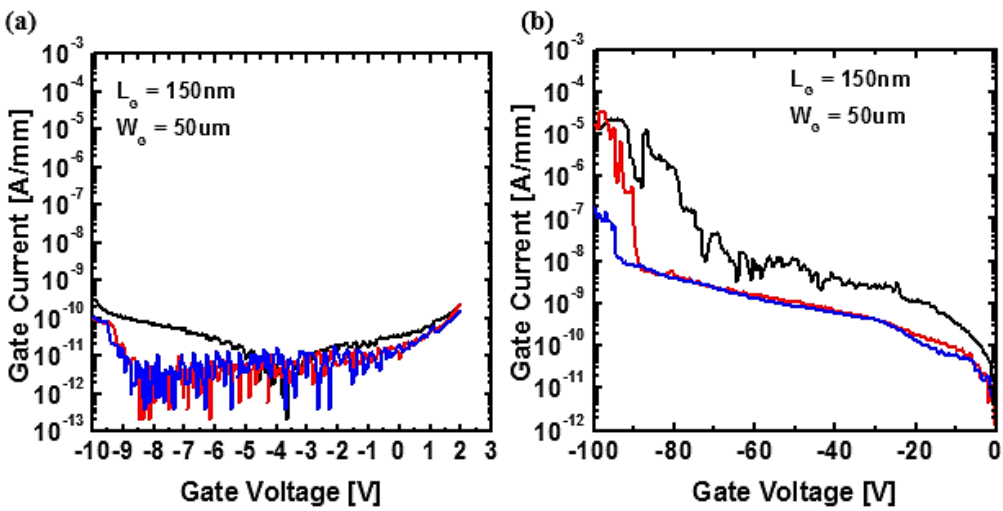

Fig. 4.5 (a) Gate forward and (b) 2-terminal reverse characteristics of the fabricated 150 nm AlGaN/GaN recessed MIS HEMTs-on-Si with increasing gate recess etching depth.

Table 4.1 Extracted small-signal parameters with different gate recess etching depth at V_{DS} = 18V without de-embedding.

	10 nm remain	**7 nm remain**	**4 nm remain**
Rg [Ω]	5.4	4.5	4.2
G_m [20]	14.4	23.0	20.9
R_i [Ω]	2.9	4.1	5.2
C_{gs} [fF]	50.3	67.6	63.5
C_{ds} [fF]	19.3	18.8	18.1
C_{gd} [fF]	7.2	8.4	8.6
G_{ds} [fF]	2.4	1.9	1.9
f_T [GHz]	35	42	41
f_{max} [GHz]	60	76	71

4.3 Advantages and Disadvantages of High-k MIS

The passivation process with high-k dielectric at Schottky HEMT demonstrated the large potential for low current collapsed GaN RF device by means of the front process. However, it was hard to employ high-k dielectric for the top layer of dual passivation structure due to the problem on etching process, so we decided to apply high-k dielectric on MIS structure which was expected lower gate leakage current additionally than Schottky contact. In this section, MIS structure was fabricated by using process details in the last section. The fabricated AlGaN/GaN recessed MIS-HEMT with HfON which was employed N_2 plasma into the HfO_2 layer by layer demonstrated both advantage and disadvantage in large-signal and small-signal characteristic respectively.

4.3.1 DC and RF Characteristics

We deposited HfON of 8 nm after the gate recess etching process was done with B.O.E 30:1 wet treatment [21, 22] for 40 sec followed by PDA 10 min at 500 °C. Figure 4.6 shows the transfer characteristic at the drain voltage of 5 V, and the maximum G_m [23] of 470 mS/mm which was the quite high value due to high gate capacitance (C_{eq}) in drain current equation of metal oxide field effect transistor (FET) was achieved.

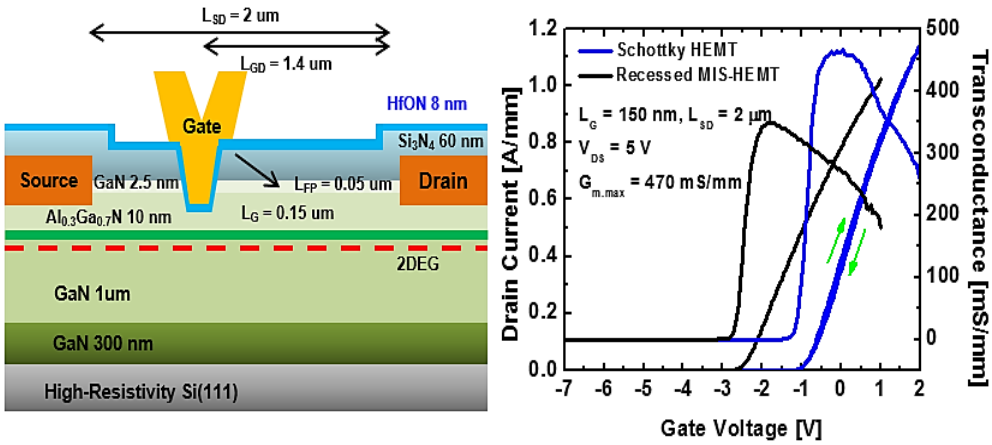

Fig. 4.6 The structure of fabricated 150 nm AlGaN/GaN recessed MIS HEMT-on-Si with HfON gate insulator of 8 nm and comparison of transfer characteristics with conventional non-recessed Schottky HEMT.

$$I_{d,linear} = \frac{\mu_{GaN} C_{eq}}{2} \left(\frac{W}{L_{SD}}\right) \left[2(V_{gs} - V_{th})V_{ds} - {V_{ds}}^2\right]$$

$$I_{d,sat} = \frac{\mu_{GaN} C_{eq}}{2} \left(\frac{W}{L_{SD}}\right) (V_{gs} - V_{th})^2$$

$$\text{Where } C_{eq} = \left[\frac{1}{C_{dielectric}} + \frac{1}{C_{it} + (\frac{1}{C_{AlGaN}} + \frac{1}{C_{2DEG}})^{-1}}\right]^{-1}$$

Unlike the compared Schottky HEMT, V_{th} was positively shifted due to high-k gate dielectric with high effective oxide thickness (EOT) [24-26] and it was required to move V_{th} negatively by controlling the recess depth to maintain high drain current density for RF device.

$$V_{th} = \gamma\left(\phi_M - \chi_{AlGaN}\right) + (1-\gamma)\phi_0 - \frac{\gamma q N_D d_{AlGaN}}{C_{dielectric}} - \Delta E_C$$

$$- \frac{\sigma_{pol} q d_{AlGaN}}{\varepsilon_{AlGaN}}$$

Where $\gamma = \frac{1}{1+D_{it}q^2/C_{dielectric}}$

ΔE_C

$= discontinuity\ in\ the\ conduction\ band\ at\ AlGaNGaN\ interface$

$\chi_{AlGaN} = electron\ affinity$

$\phi_M = gate\ metal\ workfunction$

ϕ_0

$= potential\ difference\ between\ neutral\ level\ and\ conduction\ band\ edge$

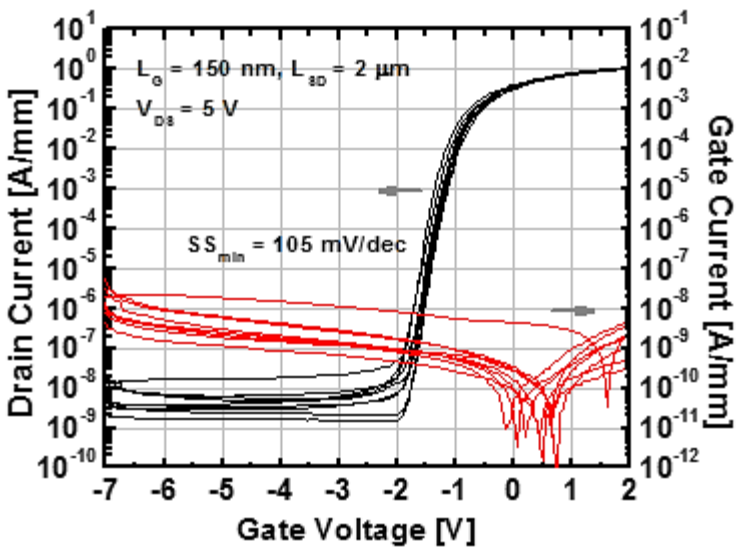

Fig. 4.7 Log scale of transfer characteristics of fabricated 150 nm AlGaN/GaN recessed MIS HEMT-on-Si. The minimum sub-threshold slope was 105 mV/dec which was quite small value for 150 nm gate length.

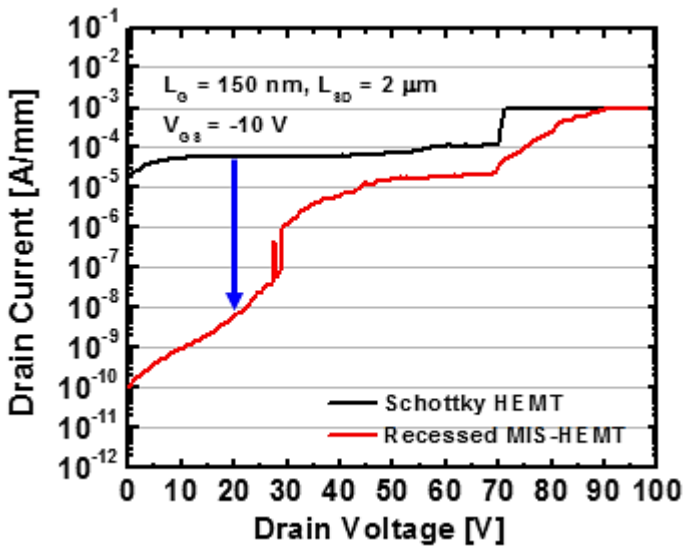

Fig. 4.8 Drain off-state leakage current of both Schottky and recessed MIS-HEMT with HfON as the gate insulator.

Also, the off-state drain current was significantly reduced because the gate leakage current was decreased with several orders in comparison to conventional Schottky contact (Fig. 4.7). The earlier hard breakdown which means the abrupt increase of off-state drain current as the drain voltage increased than Schottky HEMT in Fig. 4.8 was attributed to the breakdown of the thin gate dielectric, but it was the negligible range in terms of operating voltage for our devices. As we mainly focused on the improvement of current collapse phenomenon, Fig. 4.9 shows the comparison of pulsed I-V characteristics between Schottky HEMT with the single passivation layer of SiN_x and recessed MIS-HEMT with the gate dielectric of HfON so that the dual passivation structure with high-k dielectric was achieved. The biased gate voltage was in accordance with each V_{th}, and the current collapse phenomenon was suppressed about 50 % in recessed MIS-HEMT in

comparison to Schottky HEMT due to SiN_x/HFON dual passivation structure at ($V_{GS.Q}$, $V_{DS.Q}$) = (-6 V(-4V), 25 V). We could obtain much higher maximum drain current in operating condition which indicated the device demonstrated the larger output load-line. Figure 4.10 shows the large-signal characteristics of both Schottky and recessed MIS-HEMT with gate width of 2 × 50 μm by using load-pull measurement at 18 GHz. The source and load matching were also conducted, and the biased drain voltages were 24 V. The smaller gain compression was observed at recessed MIS-HEMT with output power of 7.24 W/mm which was attributed to the lower current collapse phenomenon and the lower off-state drain current.

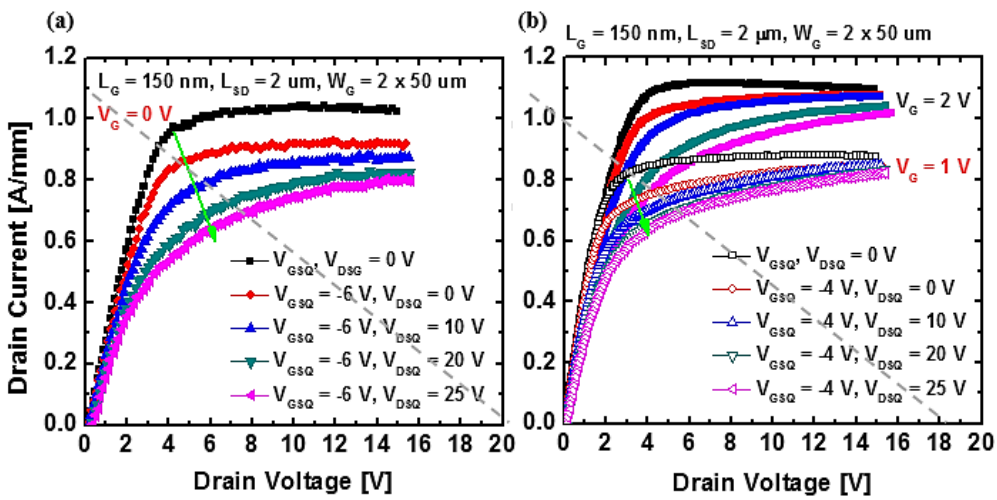

Fig. 4.9 Pulsed I-V characteristics of (a) Schottky HEMT with SiN_x single passivation (b) recessed MIS-HEMT with SiN_x/HfON dual passivation structure.

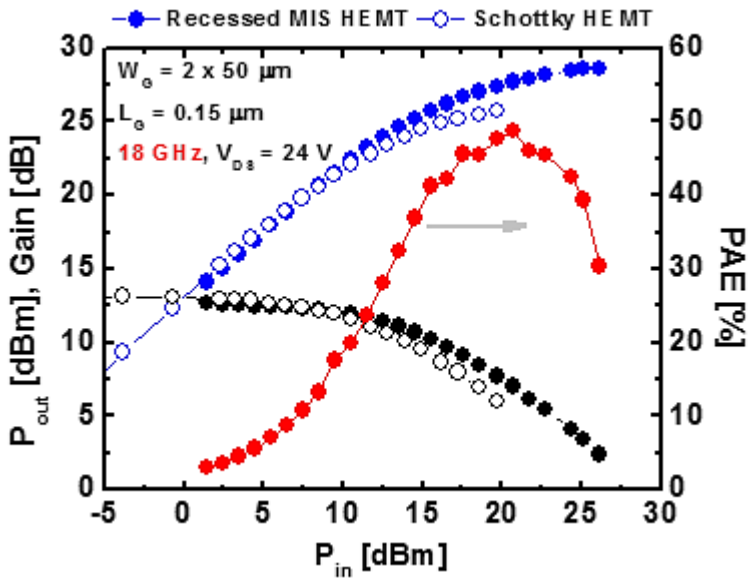

Fig. 4.10 Large-signal characteristics at 18 GHz for both Schottky and recessed MIS-HEMT with HfON as the gate insulator.

4.3.2 Issues on Small-Signal Characteristics

Despite superior large-signal characteristic of recessed MIS-HEMT with HfON for the gate dielectric, the interface issues are important for GaN MIS technology, especially at AlGaN/high-k dielectric. Also, high-k dielectric is generally known that it has much larger number of bulk traps than low-k dielectric such as SiO_2, SiN_x [27, 28]. The interface states at AlGaN/HfON occurred unstable output characteristic which was not observed at low drain voltage but degenerated at high drain voltage. Figure 4.11 shows output drain currents at each gate voltage with increasing drain voltage. The higher maximum G_m of fabricated recessed MIS-HEMT (Fig. 4.7) was promised to exhibit smaller R_{on} than the conventional Schottky HEMT, but the maximum drain current varied with different methods of measurement. The maximum drain current did not coincide with the drain current at transfer characteristic

(V_{DS} = 5 V) for the $V_G >> V_{th}$ state if we measured the output characteristic with until 20 V of drain voltage. However, if we measured until 10 V of drain voltage with each gate voltage, the maximum drain current was increased which was comparable to the drain current at transfer characteristic.

This phenomenon indicated hot electron trapping [29, 30] occurred into the empty donor-like traps at AlGaN/HfON interface due to the static high drain voltage, and the trapped electrons depleted the 2DEG channel. Also, the non-ideality versus the increase of drain voltage could be estimated at transfer characteristics in log-scale. Figure 4.12 shows the DIBL that might be caused by the such interface traps at AlGaN/HfON interface so that the device was hard to turn-off which means the trapped electrons hinder the depletion of 2DEG channel by the gate voltage when the drain voltage increased [31, 32], and these traps contributed to hot electron trapping. DIBL could be verified at output characteristic either (Fig. 4.11). The output conductance increased with increasing drain voltage at the sub-threshold region which was the same phenomenon that could be identified at transfer characteristic. DIBL is well known as the primary factor for the RF device, because the intrinsic G_m can be degraded more rapidly with increasing drain voltage than the device without DIBL. So the device may demonstrate low f_{max} with early saturation [6].

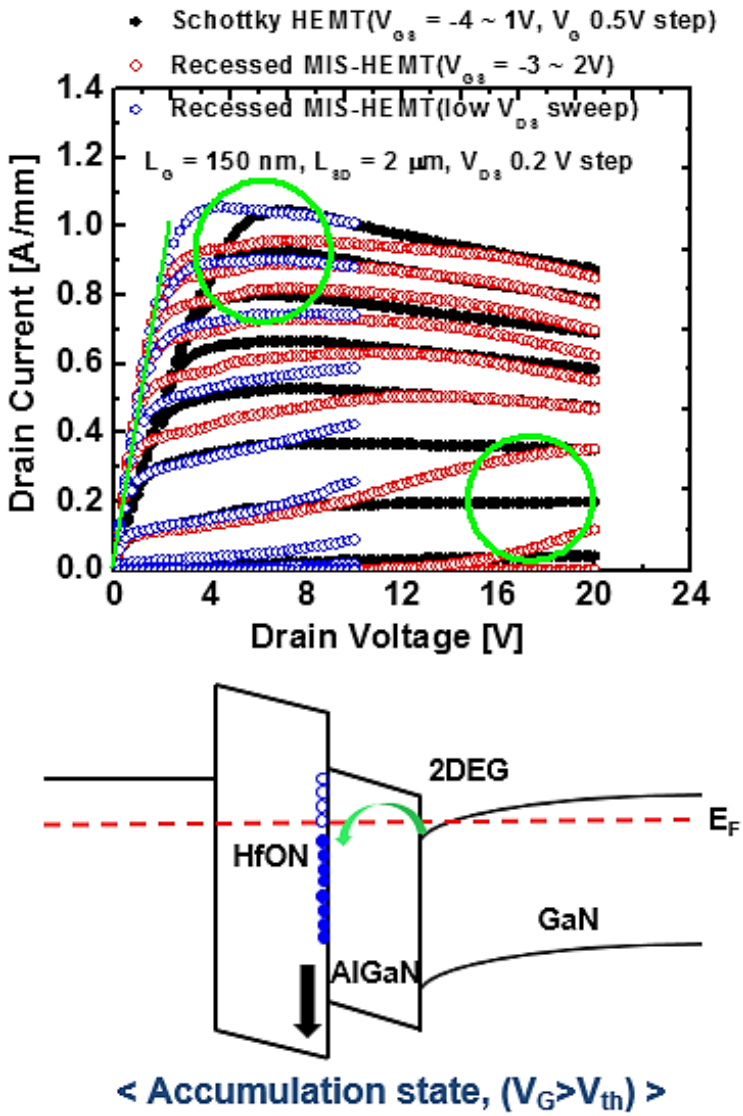

Fig. 4.11 Drain output characteristics with different sweep range to verify the effect of drain voltage on electrons in 2DEG channel.

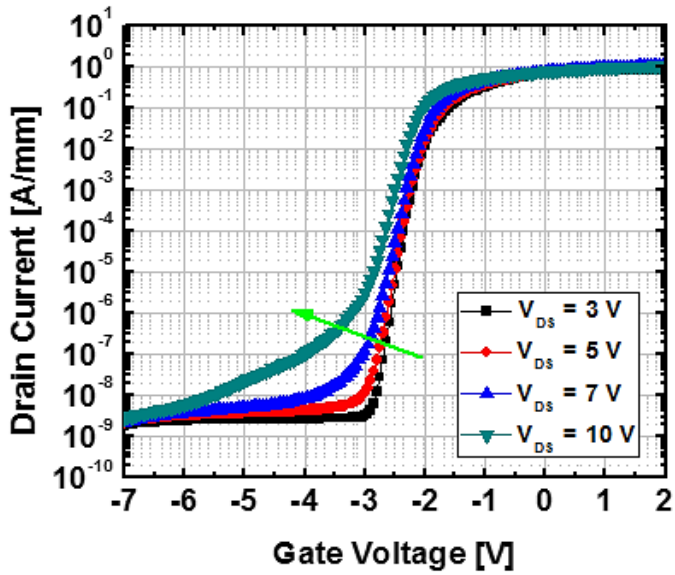

Fig. 4.12 Log scale of transfer characteristics of fabricated 150 nm AlGaN/GaN recessed MIS HEMT-on-Si with increasing applied drain voltage.

4.4 PEALD SiN_x for Interface Layer

There are additional phenomena that indicate the existence of donor-like traps at AlGaN/GaN/HfON interface. When the positive voltage induced at the gate electrode for the amount of time, the electrons from 2DEG were trapped into the AlGaN/HfON interface so that V_{th} moved positively due to depletion of 2DEG [33, 34]. This phenomenon rose consistently as the stressed time increased until the shift of V_{th} was saturated which implied the traps were almost occupied. Figure 4.13 shows the V_{th} instability characteristics of the fabricated 0.15 μm recessed MIS-HEMT with four different gate dielectrics. As we mentioned in the last section, the dielectric with higher dielectric constant may have the larger number of traps, and the device with HfON exhibited much more significant V_{th} instability than other devices. On the other hand, the devices with SiN_x or SiON which were deposited using remote PECVD [7] and ALD [35], respectively, demonstrated much lower trap densities. The effect of Si on AlGaN/gate dielectric interface [36-38] should be investigated further, but it was certain that the Si ions effectively compensated donor-like traps. The impact of generated oxygen by our ALD process should be also investigated more, because sometimes the oxygen has been known as the good surface bonding material in GaN technology [39].

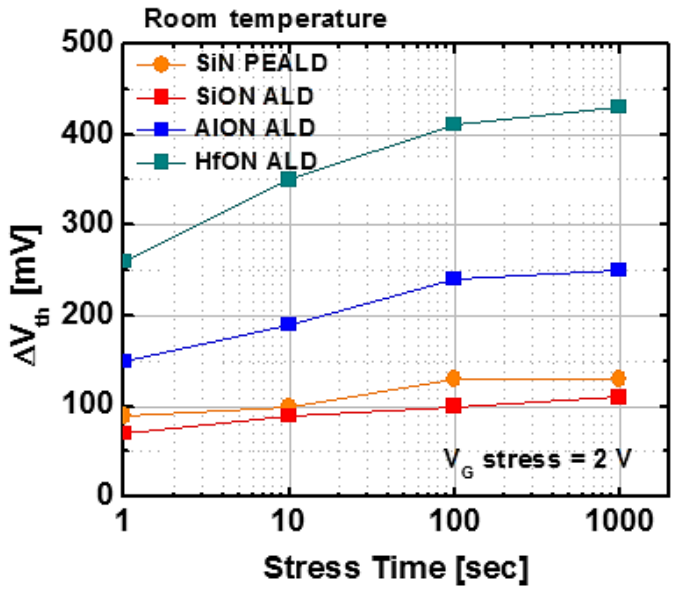

Fig. 4.13 The result of threshold voltage (V_{th}) instability of the fabricated each recessed MIS-HEMT at the drain voltage of 0.1 V with various gate insulators after the positive gate voltage was applied.

However, the impact on interface characteristic was different between PEALD SiN_x and ALD SiON. From the results of transfer characteristics of two different devices, only the device with PEALD SiN_x presented smaller DIBL (Fig. 4.14(a) and (b)). To suppress these traps, effective treatment was additionally required to change the bonding between two layers, such as high-density N_2 plasma. N-vacancies could be generated during the not only growth process of AlGaN layer but also gate recess process, and several studies reported that these shallow traps are hard to be distinguished from such analysis of trap density [40]. We tried to compensate these donor-like traps by in-situ N_2 plasma treatment before deposition of PEALD SiN_x [41-43] using inductively coupled plasma (ICP) method in remote PECVD chamber that could make high plasma density and be free from oxygen while ALD chamber was not easy to ingenerate pure N_2 plasma.

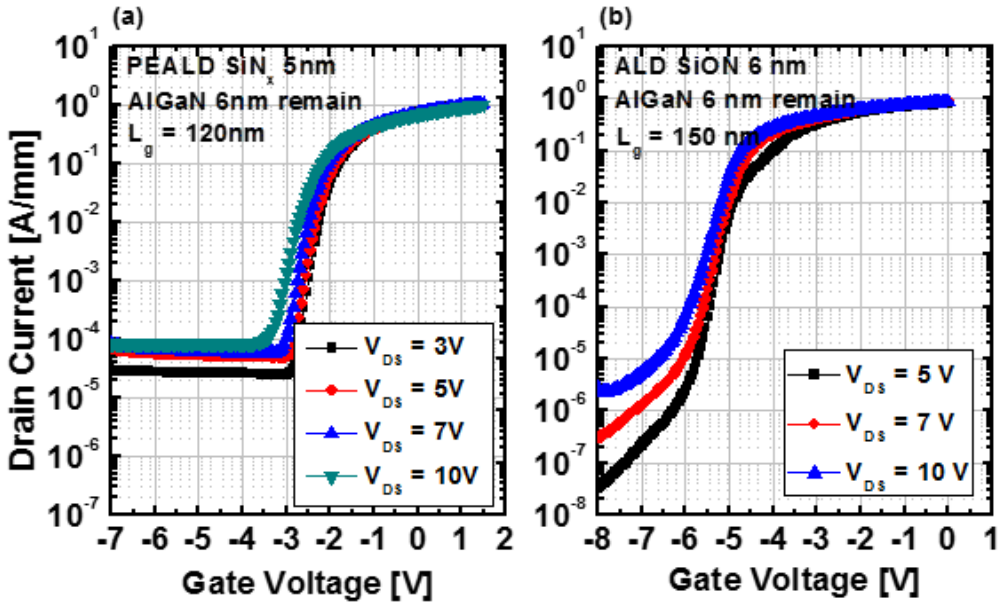

Fig. 4.14 Transfer characteristics of recessed MIS-HEMTs with (a) SiN_x in ICP-CVD chamber and (b) SiON in ALD chamber as the gate insulator with different drain voltages. Both recessed MIS-HEMTs were fabricated with same gate recess etching process and surface treatment (B.O.E 30:1).

4.5 Device Characteristics

First, we fabricated the recessed AlGaN/GaN MIS-HEMTs with only PEALD SiN_x and SiN_x/HfON dual layer as the gate insulator to compare with non-recessed AlGaN/GaN Schottky HEMT without any application of high-k dielectric. Table 4.2 shows the sequence of PEALD process which includes in-situ N_2 plasma treatment at first step. The N_2 plasma power can be reduced from 600 W to 300 W to suppress plasma damage during the deposition whereas the quality of SiN_x might be poorer, so we used the plasma power of 300 W for initial 0.5 nm and 600 W for last 1 nm. We employed the same gate recess etching process and surface treatment (B.O.E 30:1) before the gate insulator was deposited on both devices.

Table 4.2 Process sequence of PEALD SiN_x using ICP-CVD. The growth rate is 0.5 Å/cycle.

Process step	**1**	**2**	**3**	**4**	**5**
Ar [sccm]	10	10	0	100	5
N_2 [sccm]	50	50	50	75	50
SiH_4 [sccm]	0	0	0	25	0
Chamber pressure [mTorr]	60	60	0	70	0
Source RF power [W]	0	600	0	0	0
Time [sec]	10	60	5	10	5

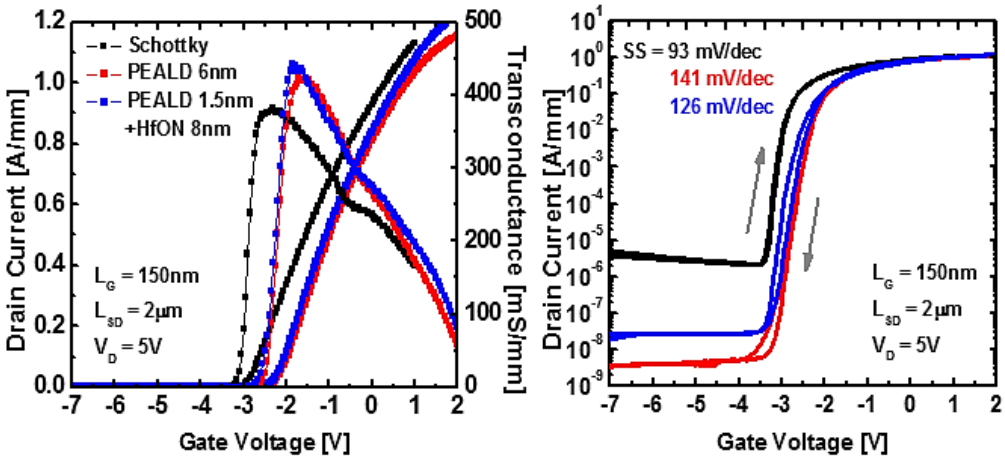

Fig. 4.15 Transfer characteristics of three different devices with linear (left) and log (right) scale. The SiN_x of 1.5 nm as the interfacial layer was employed for the recessed dual MIS-HEMT.

The transfer characteristics of three different devices were shown in Fig. 4.15 with linear and log scale at the drain voltage of 5 V. We could achieve the sub-threshold slope of 126 mV/dec at recessed dual MIS-HEMT which was the smaller value than the MIS-HEMT with only SiN_x due to the employed high-k dielectric (HfON). The maximum G_m of recessed dual MIS-HEMT with the gate length of 0.15 μm was 450 mS/mm which was the highest value among the three devices. The purpose of the thin SiN_x interfacial layer for recessed dual MIS-HEMT was the suppression of DIBL. We estimated this phenomenon by measuring the transfer characteristics of each device with different gate length indirectly (Fig. 4.16). The devices with gate length from 250 nm to 70 nm exhibited the increase of sub-threshold slope for both Schottky and recessed dual MIS-HEMT. The increment of sub-threshold slope for the recessed dual MIS-HEMT was smaller than Schottky HEMT by employing SiN_x interface layer, but V_{th} was more negatively shifted as the gate length was decreased. The recessed dual MIS-HEMT with

the gate length of 70 nm showed the maximum G_m over 600 mS/mm which was the effect of HfON bulk layer for gate insulator (Fig. 4.17).

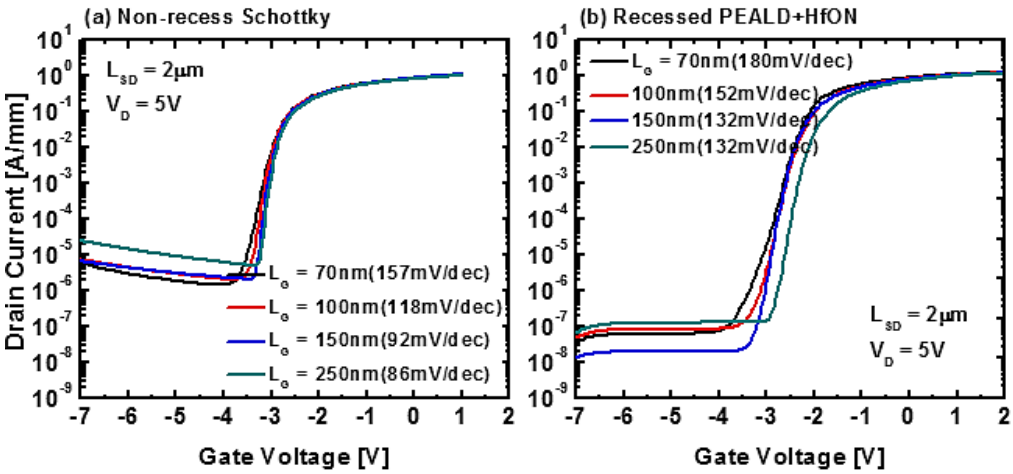

Fig. 4.16 Sub-threshold slope of (a) Schottky and (b) recessed dual MIS-HEMT with different gate length at the drain voltage of 5 V.

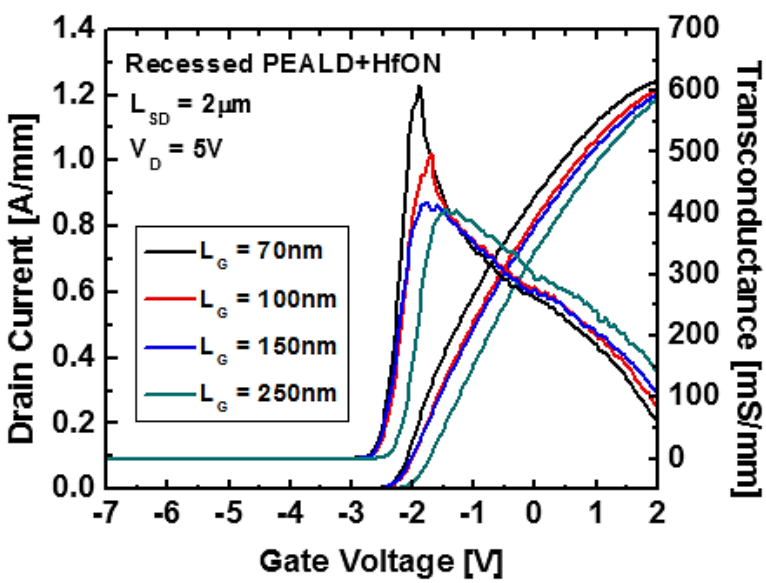

Fig. 4.17 Transfer characteristics of the recessed dual MIS-HEMT with various gate length at the drain voltage of 5 V.

The effect of HfON also can be seen at the pulsed I-V measurement. Figure 4.18 showed the gate lag phenomena of both Schottky and recessed dual MIS-HEMT with increase of negative gate quiescent bias (V_{GSQ}). The drain current of Schottky HEMT without any HfON layer gradually degraded as the V_{GSQ} negatively increased whereas the recessed dual MIS-HEMT with HfON layer exhibited the saturated degradation of drain current, and this was the same result with the recessed MIS-HEMT without SiN_x interface layer in the section 4.3.

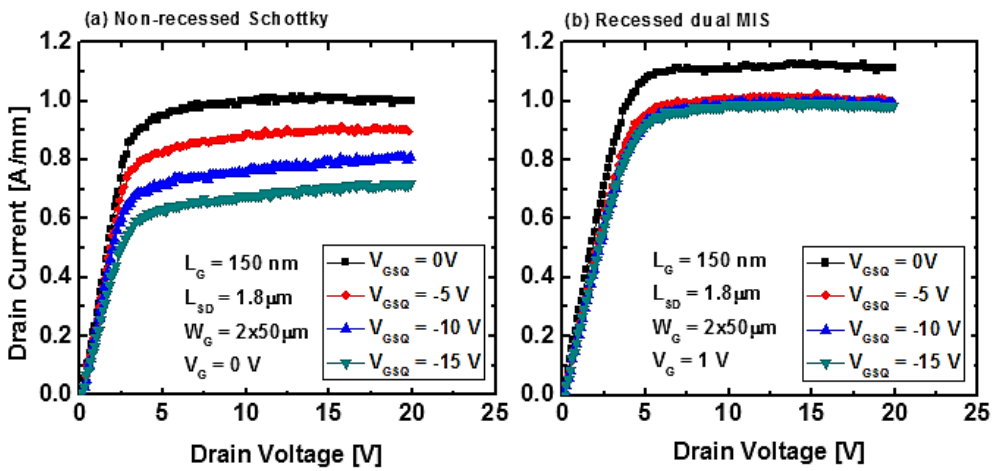

Fig. 4.18 The results of gate lag by pulsed I-V measurement for both (a) Schottky and (b) recessed dual MIS-HEMT with increase negative V_{GSQ}.

Our final device in this research was fabricated with Ar^+ ion implantation (section 2.2.3) for the device isolation process to reduce the substrate effect in terms of RF loss and the mesa sidewall effect by making planar device structure (Fig. 4.19). The transfer characteristics of fabricated 0.15 μm device are shown in Fig. 4.20. The maximum G_m at the drain voltage of 5 V was 500 mS/mm, and the off-state drain current was extremely low compared to the device had the mesa sidewall. Also, the current collapse phenomena were

measured and the improvement of drain current under the V_{GSQ} and V_{DSQ} biased condition was demonstrated in Fig. 4.21 from the Schottky HEMT with mesa etching for isolation to the recessed dual MIS-HEMT with ion implantation. After the device structure was changed as planar, the effect of HfON layer was improved due to the sidewall trapping, so that the lower current collapse was achieved. We could expect the low drain leakage current and the higher maximum drain current with the higher operation voltage at the finally fabricated recessed dual MIS-HEMT, and this might impact on the output power performance of MMIC PA in the next chapter.

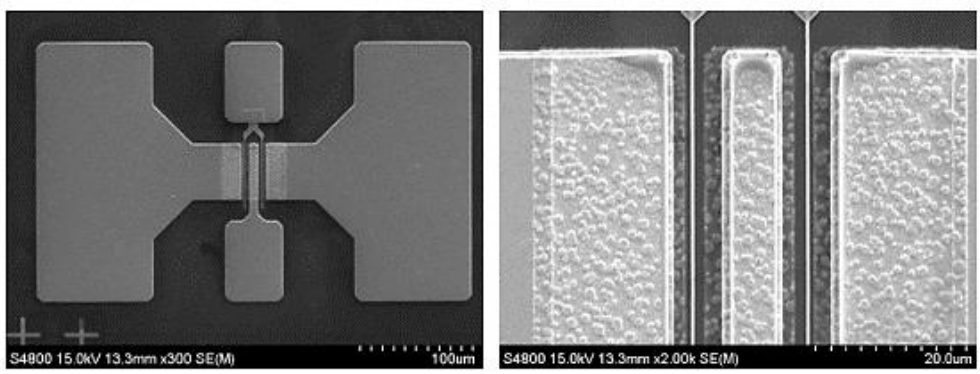

Fig. 4.19 SEM images of top view of the fabricated 2 × 50 μm recessed dual MIS-HEMT with gate length of 0.15 μm. The device was isolated by ion implantation.

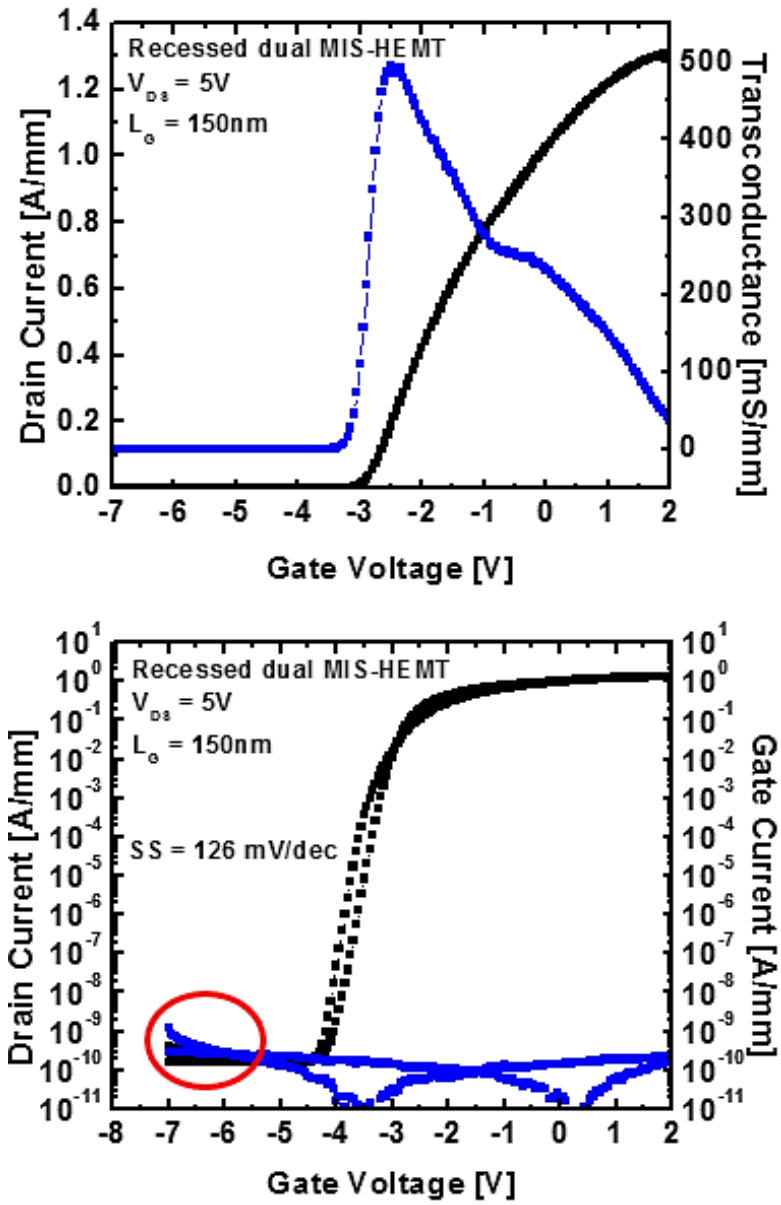

Fig. 4.20 Transfer characteristics of the fabricated 0.15 μm AlGaN/GaN recessed dual MIS-HEMT at the drain voltage of 5 V.

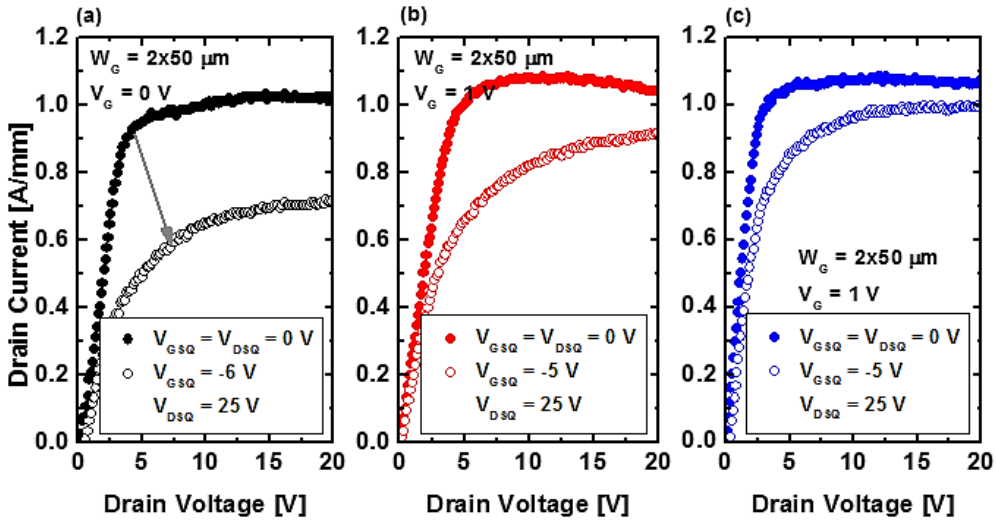

Fig. 4.21 Pulsed I-V characteristics of (a) non-recessed Schottky (b) recessed dual MIS-HEMT (mesa etching) and (c) recessed dual MIS-HEMT (ion implantation). The V_{GSQ} were applied considering V_{th} of each device.

The small-signal characteristics of recessed MIS-HEMT only with HfON demonstrated the lower intrinsic G_m resulted in the much lower f_T and f_{max} than the Schottky HEMT. Thus, we employed thin SiN_x interfacial layer with the in-situ N_2 plasma to mitigate the effect of HfON on the interface trap densities. Figure 4.22 shows the plot of f_T and f_{max} for the finally fabricated recessed dual MIS-HEMT with the Schottky HEMT which was also with the ion implantation for the device isolation. The extracted f_{max} of recessed dual MIS-HEMT was slightly low compared to the Schottky HEMT, but the drain biased voltage was higher when the peak f_{max} was achieved. The f_{max} was not saturated until the drain voltage of 21 V whereas the Schottky HEMT exhibited the peak f_{max} at the drain voltage of 18 V. This indicated that the recessed dual MIS-HEMT was promised for the higher operating drain voltage that could improve output power performance. However, further optimization of forming MIS structure such as surface treatment or the

thickness of SiN_x interfacial layer should be required to achieve the better peak value of f_{max} than the Schottky HEMT.

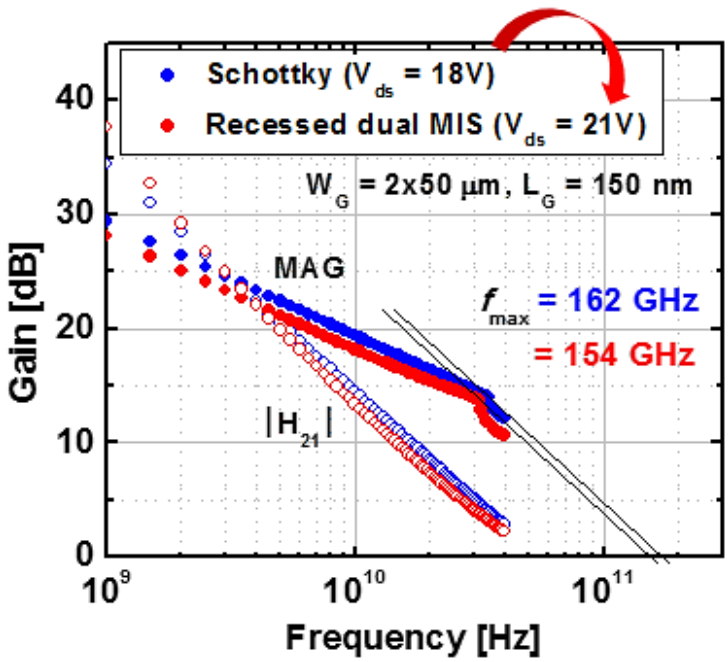

Fig. 4.22 Small-signal characteristics of both Schottky and recessed dual MIS-HEMT of 2 × 50 μm with ion implantation for device isolation. The biased drain voltage of recessed dual MIS-HEMT could be increased for the higher f_{max}.

4.6 References

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Chapter 5. Fabrication of Ka-band AlGaN/GaN MMICs Power Amplifier

5.1 Introduction

This chapter will demonstrate the integration process to make Ka-band 2-stage common source MMIC PA by using AlGaN/GaN-on-Si substrate with the optimized process of both the active and passive devices without backside via process. First, we will describe the method of modeling active device to design matched IC layout. MMICs consist of planar integrated active and passive elements that determine the circuit operation. Developments of the passive devices with high yields are very important work because they impact on MMICs yields decisively. The passive devices are composed of lumped elements such as resistors, capacitors, and inductors and distributed elements such as transmission lines. The process details of R, L, C are described with their several experiments data. Finally, we sorted out each passive with various sizes for MMIC design and successfully fabricated 26.5~27 GHz 2-stage MMIC PA with AlGaN/GaN-on-Si HEMTs. The effects of various process technologies were investigated through the small- and large-signal characteristics of the fabricated MMICs. Finally, we evaluated the power reliability of MMICs to suggest the next direction of GaN-on-Si RF MIS technology.

5.2 Active Device Layout

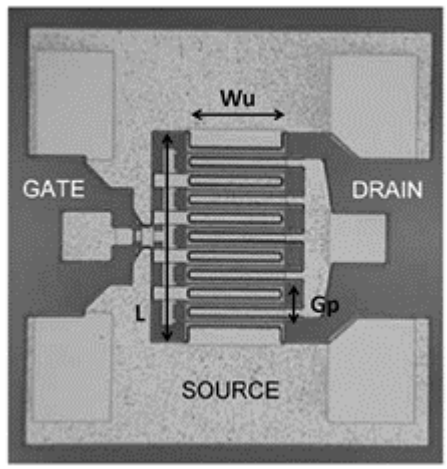
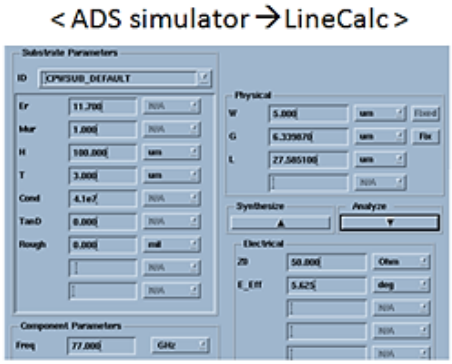


Fig. 5.1 General layout design parameters of RF devices.

To begin with, there are three device parameters that influence on RF device performance (Fig. 5.1). A large unit gate width (W_u) leads to an increase of drain output current which has advantage on high output power, but it degrades frequency response at high frequency operation owing to the large gate resistance. An increase of the number of gate finger (N) makes also large drain output current and high output power, but the large phase delay occurs resulted in the low frequency-gain characteristic. A longer gate pitch (G_p) has an impact on the phase delay, either, whereas the thermal effect may be reduced and the electromigration limit can be decreased due to the large electrodes of the source and drain. The G_p finally related to the area of GaN RF device so that the substrate with good thermal conductivity can make the smaller device with the high power density. From these device parameters, we could easily speculate the maximum size of the device layout using LineCalc. in ADS simulator (Fig. 5.2). The substrate and the thickness of metal were set up with Si and 2.5 μm respectively. If we assume that the

operation frequency is 30 GHz (Ka-band), the maximum possible distance from edge to edge will be defined by λ/16, and the G_p also can be decided according to the N. However, we considered the non-ideality of the fabricating device so that the standard devices had G_p of 14 μm, output (drain) pad of 12 μm, and source pad of 20 μm which did not reach at the calculated maximum size. Then we added the two different layouts that one increased the length of source pad at the center of device to estimate the thermal effect and another one increased each source pad (Fig. 5.3(a)).



	Electrical length	phase (rad)	phase (deg)	Ka-band (30 GHz)
	λ	2π	360°	4.53 mm
	λ/8	π/4	45°	566 μm
L	λ/16	π/8	22.5°	**283 μm**
W	λ/32	π/16	11.25°	**141.6 μm**
	λ/48	π/24	7.5°	**94.4 μm**

Fig. 5.2 LineCalc. tool in ADS simulator program [1].

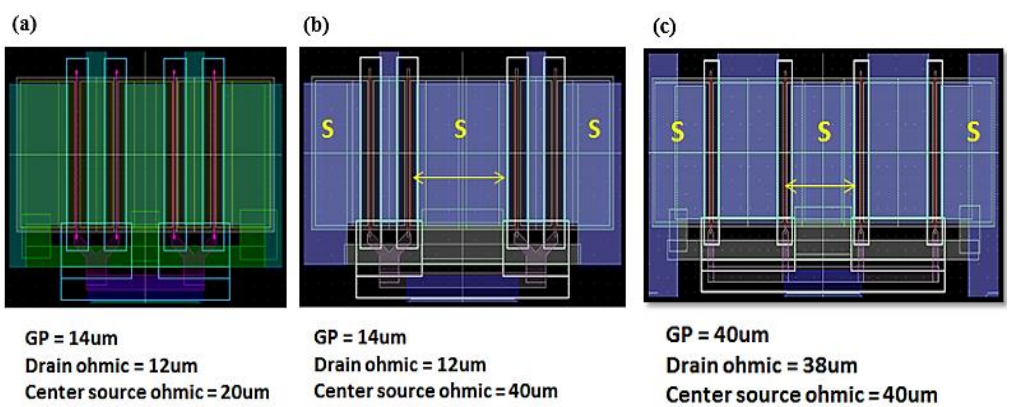


Fig. 5.3 Three different device layouts with varying gate pitch or the area of source and drain pad.

5.3 Active Device Modeling

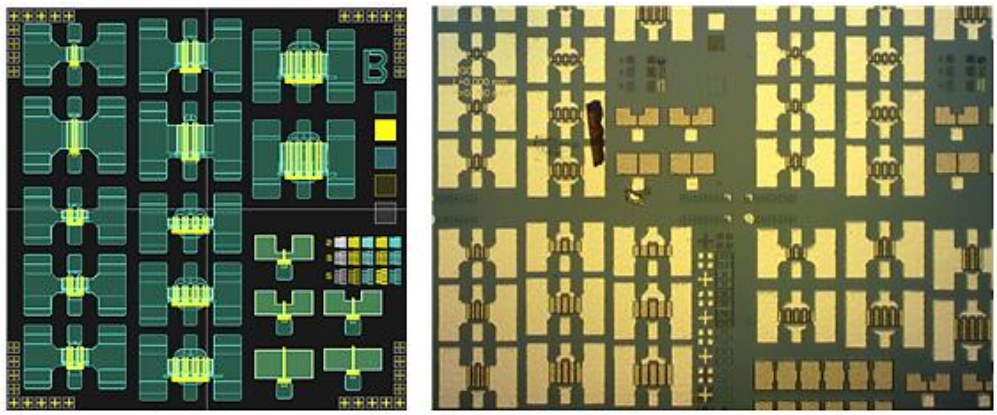


Fig. 5.4 Device layout with various size and chip images of the fabricated devices.

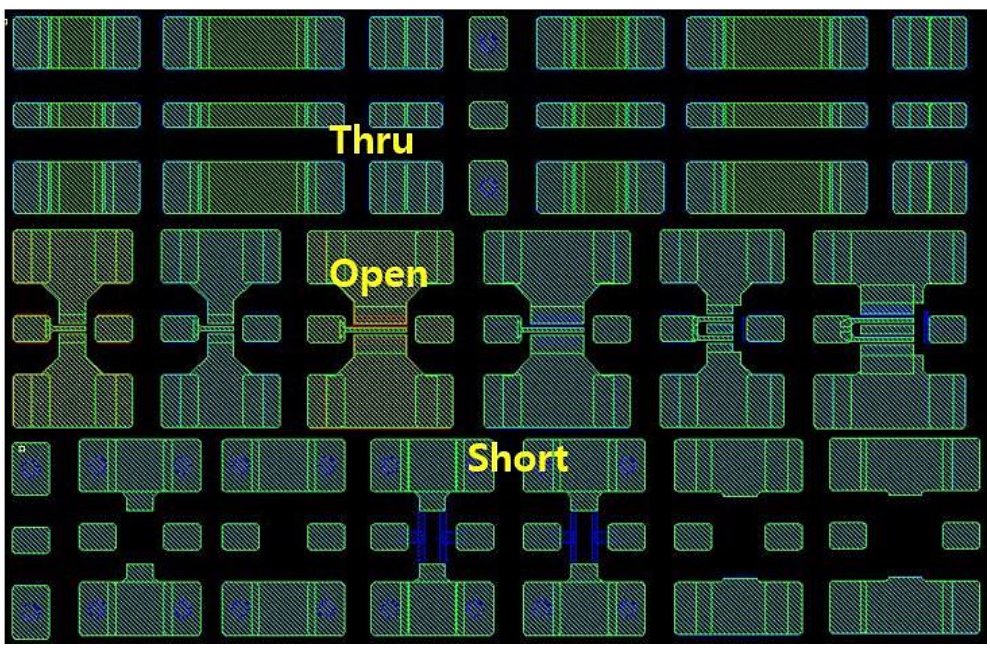
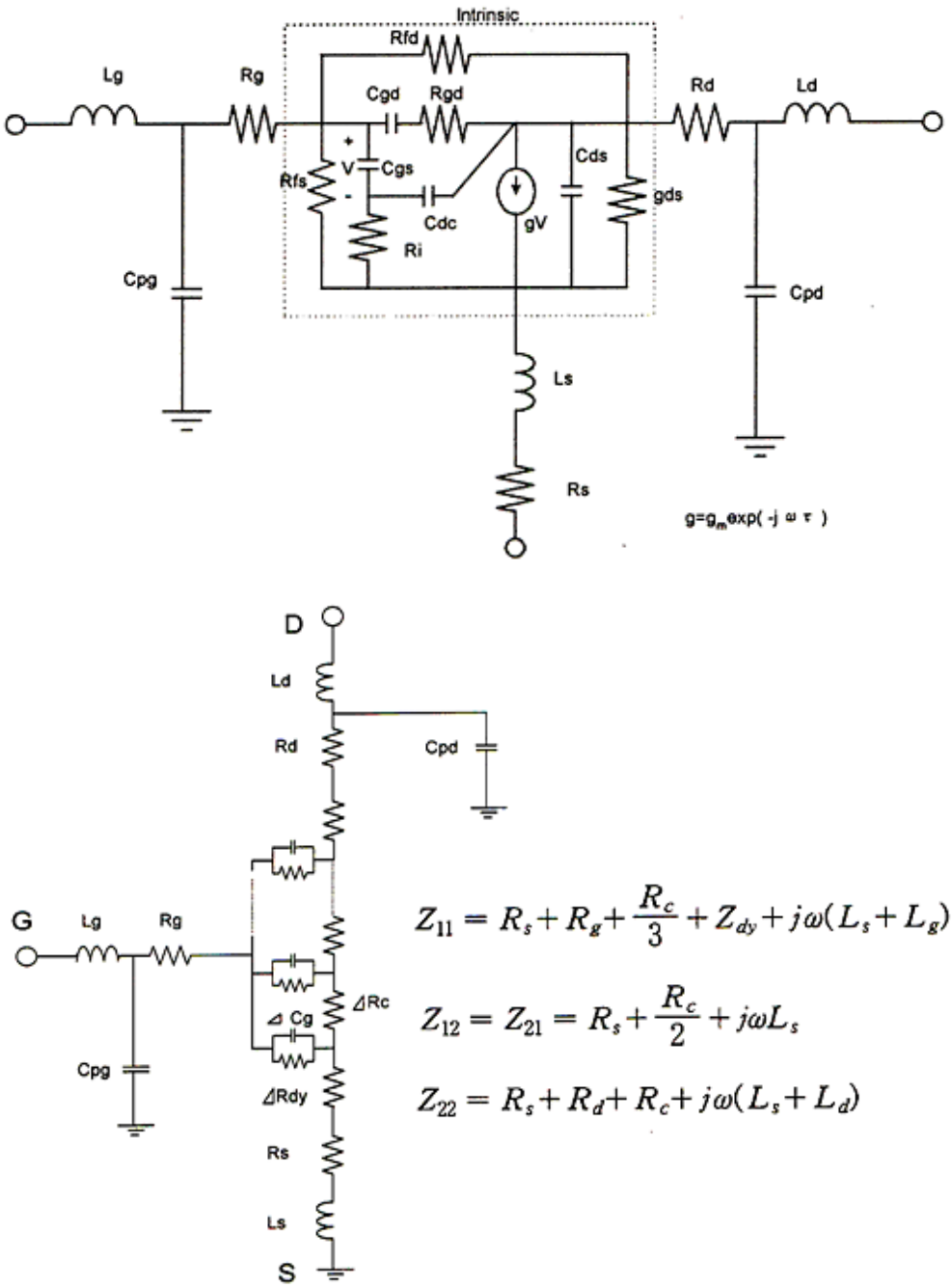


Fig. 5.5 Layout design for de-embedding including Thru., Open, and Short patterns with various gate width and number of gate.

In this section, we are going to describe the sequence of device modeling briefly. First, we measured the small-signal characteristics of the fabricated AlGaN/GaN recessed MIS-HEMT with various total gate widths (W_G) to extract their small-signal parameters. Usually, the intrinsic parameters are scalable, but the extrinsic parameters are not scalable versus the size of devices so that we extracted all extrinsic parameters of the devices in mask layout as shown in Fig. 5.4 using vector network analyzer (VNA) by on-wafer probing. Figure 5.5 shows the de-embedding pattern including open/short and thru patterns that were utilized at the extraction of extrinsic parameters [2]. We used "Cold-FET" method for parameter extraction [3], and the equivalent circuit at pinch-off condition could be described as shown in Fig. 5.6. Z-parameters could be defined from the equivalent circuit, and the intrinsic parameters with each biased voltage were extracted by de-embedding the extrinsic parameters from the measured s-parameters. The used equivalent circuit and equations are also presented. Figure 5.7 plotted the extracted extrinsic parameters with various W_G, and the parameters were not scalable as expected even though the large trends existed as the W_G increased. So we should have each extracted result of the fabricated devices which were employed in MMIC design. Finally, we could estimate the accuracy of our results of extraction up to 70 GHz by comparing between the measured s-parameters and reversely extracted s-parameters (Fig. 5.8).



$$Z_{11} = R_s + R_g + \frac{R_c}{3} + Z_{dy} + j\omega(L_s + L_g)$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d)$$

Fig. 5.6 Small-signal equivalent circuit (top) and equivalent circuit at pinch-off state for extraction of extrinsic parameters (bottom) and their equations.

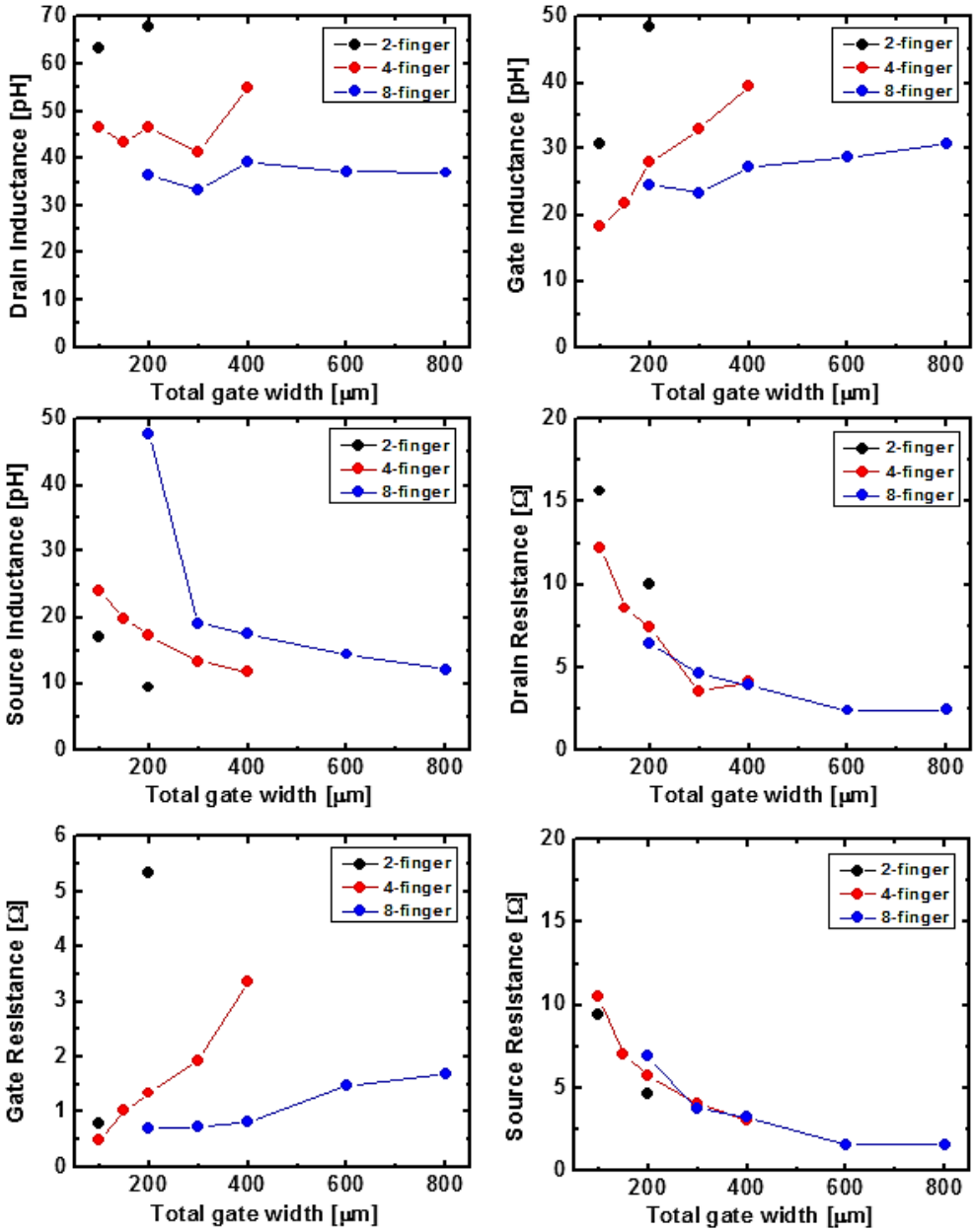


Fig. 5.7 Extracted non-scalable extrinsic parameters with various total gate width.

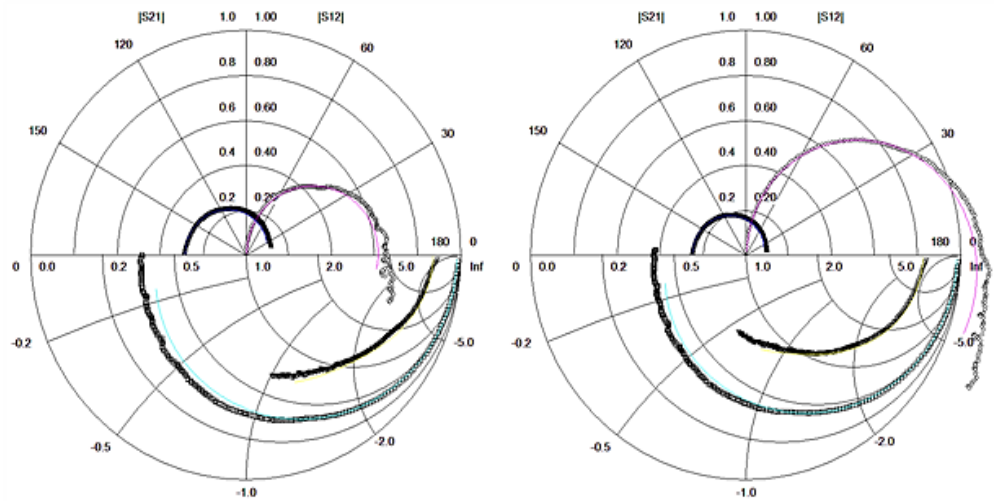


Fig. 5.8 The examples of estimating the accuracy of our small-signal parameters extraction by drawing smith chart reversely.

For large-signal model, we employed Angelov equation which is known as the model with high convergence [4]. First, the measured drain current from VNA was described by Eq. (5.1)-(5.2) to realize the curve of transconductance (G_m). Also, the non-linear capacitances were defined by Eq. (5.3)-(5.6).

$$I_{ds} = I_{pk0} \times (1 + \tanh(\Psi)) \times (1 + \lambda V_{ds}) \times \tanh(\alpha \times V_{ds}) \tag{5.1}$$

$$\Psi = P_1 \times (V_{gs} - V_{pk}) + P_2 \times (V_{gs} - V_{pk})^2 + P_3 \times (V_{gs} - V_{pk})^3 \tag{5.2}$$

$$C_{gs} = C_{gsp} + C_{gs0} \times (1 + \tanh(\psi_1)) \times (1 + \tanh(\psi_2)) \tag{5.3}$$

$$\psi_1 = P_{10} + P_{11} V_g + P_{12} V_d, \quad \psi_2 = P_{20} + P_{21} \times V_d \times \tanh(\alpha \times (V_g - b)) \tag{5.4}$$

$$C_{gd} = C_{gdp} + C_{gd0} \times (1 + \tanh(\psi_3)) \times (1 + \tanh(\psi_4)) \tag{5.5}$$

$$\psi_3 = P_{30} + P_{31} V_g + P_{32} V_d, \quad \psi_4 = P_{40} + P_{41} \times V_d \times \tanh(\alpha \times (V_g - b)) \tag{5.6}$$

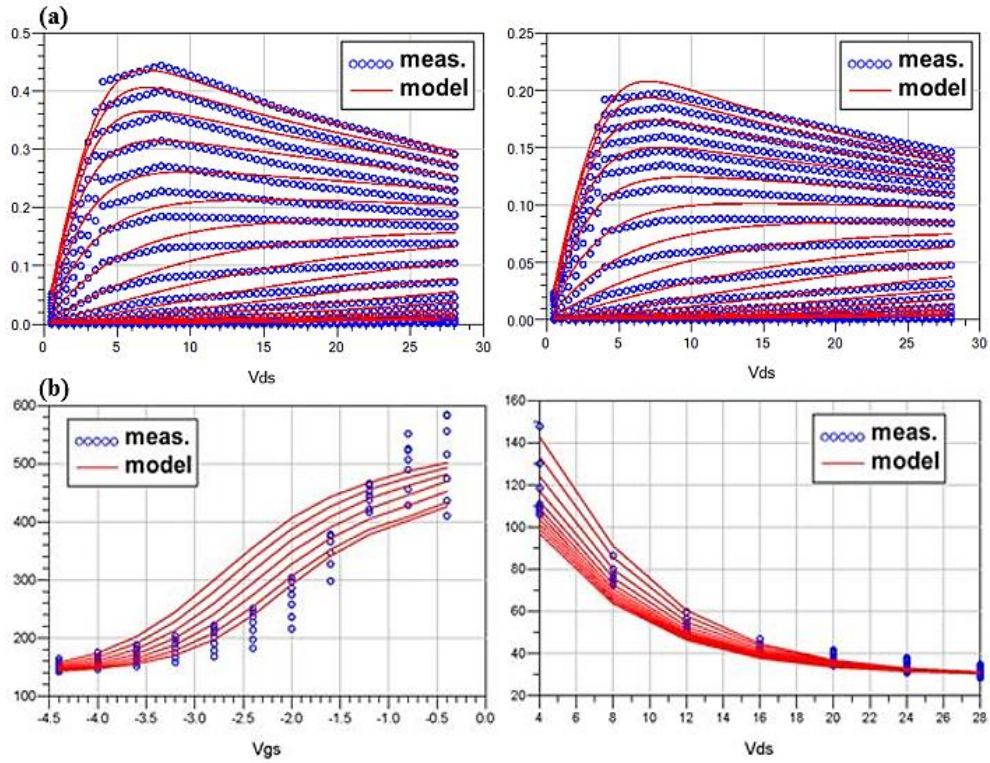


Fig. 5.9 Comparison between measured and modeled (a) scaled drain current (b) capacitance of 4×37 μm AlGaN/GaN recessed MIS-HEMT.

Figure 5.9(a) and (b) exhibit the models of drain current and non-linear capacitances. Both results were substantially matched up with the measurement data and demonstrated quite accurate scaling characteristics.

To increase the accuracy of the large-signal model, the thermal effect and trapping effect must be considered (Fig. 5.10). The self-heating due to the high output power of GaN HEMT degrades its output characteristics, such as the drain current or cut-off frequency (f_T). The electro-thermal model employed in Fig. 5.10 can make to predict the thermal response of operating device and to define the channel temperature. The thermal resistance (R_{th}) in this model must be small in RF device that can be generally reduced by the

substrate with high thermal conductivity or good packaging. The R_{th} is measured by pulsed I-V indirect method with hot chuck [5] or infrared (IR) camera during the device is operating. In this work, we adapted pulsed I-V method for extraction of R_{th}, and this method also has an advantage which can extract thermally related additional parameters from the pulsed I-V curve. As shown in Fig. 5.12 that we plotted the measured R_{th} of the fabricated devices with various gate widths, the R_{th} of GaN HEMT was also one of the parameters which are non-scalable. However, all R_{th} might be overestimated in these results, because the device was measured without any packaging or backside process which could disperse the self-heating effectively.

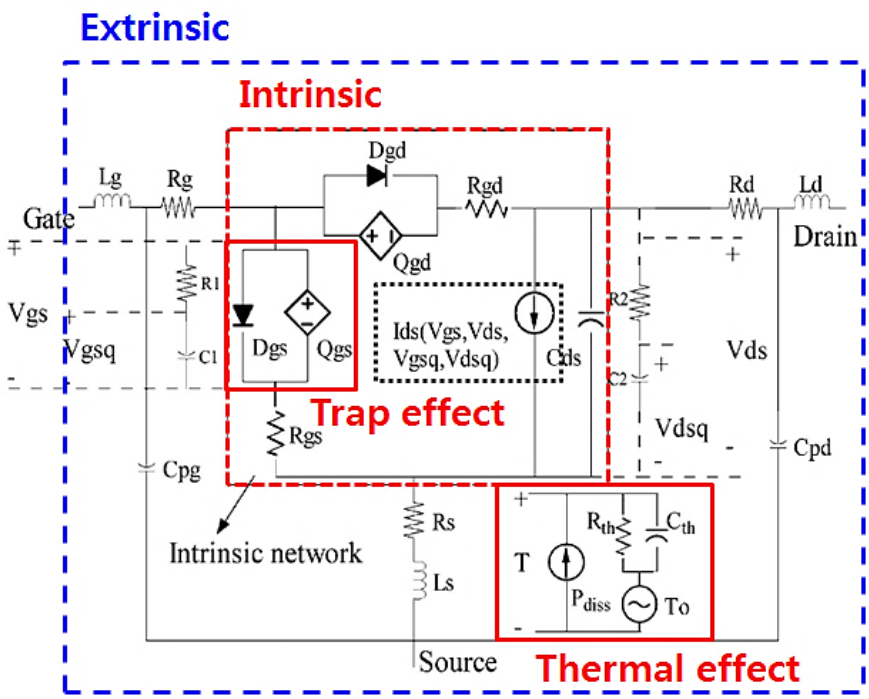


Fig. 5.10 Large-signal equivalent circuit including thermal and trap effect.

Fig. 5.11 Equipment (DIVA) for pulsed I-V measurement (left) and hot-chuck with temperature controller (right).

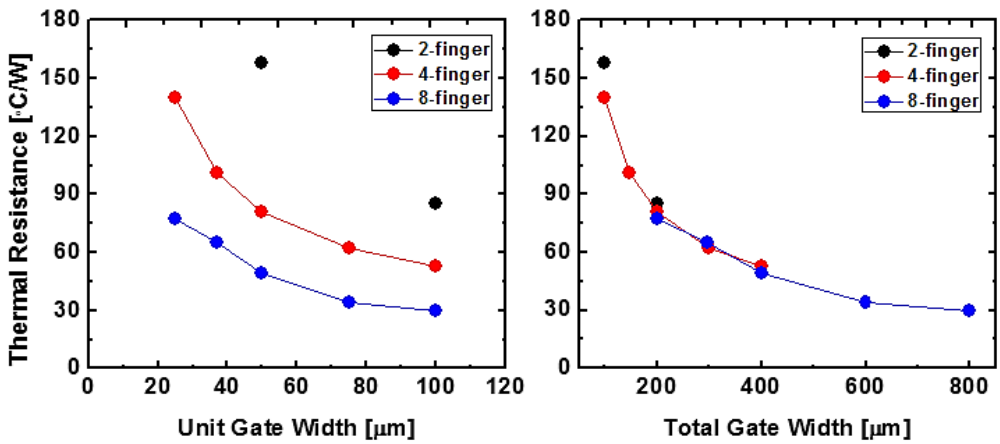


Fig. 5.12 Measured thermal resistances with various gate width by using pulsed I-V. All results were extracted without any thermal packaging.

Another non-ideality for device modeling is the trapping effect which means current collapse phenomenon during RF operation. The speculation of the reduced output drain current is important to estimate the expected output power. We used new parameters with additional variations to describe the trapping effect versus the quiescent bias (Eq. (5.7)-(5.10)). The parameter related to the gate quiescent bias ($V_{gs.q}$) could be found by comparing the output curve without and with gate lag followed by the extraction of both gate

and drain quiescent bias ($V_{ds.q}$) related parameter. The reason why the two parameters are separately extracted is that the trapping effect and thermal effect by the $V_{ds.q}$. To avoid the thermal effect, the 2DEG channel must be depleted so that the smaller $V_{gs.q}$ than pinch-off voltage was employed. Figure 5.13 exhibits the improvement of accuracy of the device modeling by utilizing these new parameters under the biased condition with trapping effect.

$$P_{1,rev} = \frac{P_1}{(1+P_{1V_{dsq}} \times \Delta V_{dsq}) \times (1+P_{1V_{gsq}} \times \Delta V_{gsq})} \tag{5.7}$$

$$I_{pk,rev} = I_{pk0} + I_{pkV_{dsq}} \times \Delta V_{dsq} + I_{pkV_{gsq}} \times \Delta V_{gsq} \tag{5.8}$$

$$V_{pk,rev} = V_{pk} + V_{pkV_{dsq}} \times \Delta V_{dsq} + V_{pkV_{gsq}} \times \Delta V_{gsq} + \omega \times V_{ds} \tag{5.9}$$

$$\alpha_{rev} = \frac{\alpha}{1+\alpha_{V_{dsq}} \times \Delta V_{dsq}} \tag{5.10}$$

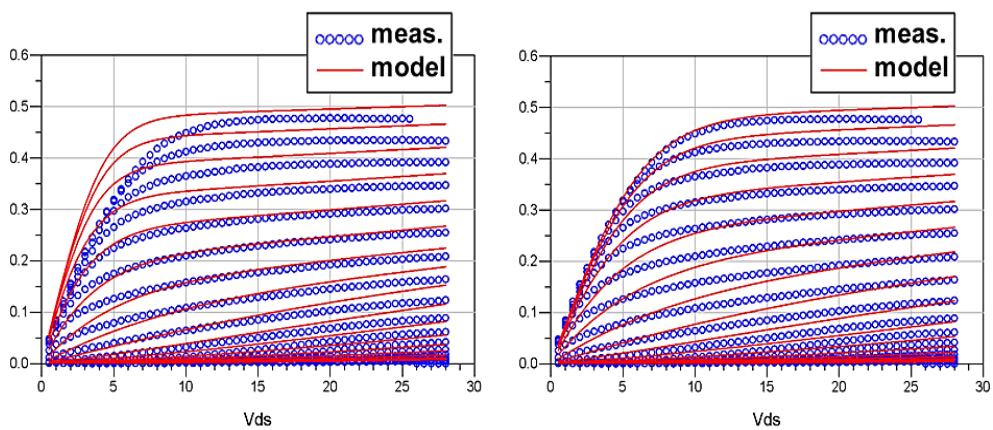


Fig. 5.13 Comparison between measured and revised drain current model (right) considering trap effect.

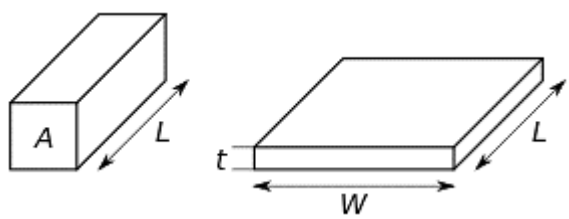
5.4 Thin Film Resistor (TFR)

In MMIC technology, the resistors are extensively used in feedback circuits, bias circuits, and as terminations. Two types of resistors are commonly used in MMIC fabrication, namely, thin films of lossy metals and lightly doped active layer (mesa resistors). Metal thin-film resistors are more temperature stable and are used as precision resistors of low to moderate values. TFRs in MMIC technology are conventionally fabricated with nickel chrome (NiCr) or tantalum nitride (TaN) by using sputtering or e-beam evaporation process. although other metals may be used[6, 7]. Table. 5.1 shows the properties of both metals. NiCr resistors have low thermal coefficient of resistance (TCR), small parasitic values, and their sheet resistance is easy to control by the deposition thickness [8, 9]. A limited range of sheet resistance (R_{sh}) is possible, from perhaps 10 Ω/sq to 250 Ω/sq. The R_{sh} of films is known to increase with time as the surface layer oxidizes. In order to minimize this effect, resistors are often stabilized by baking them at temperatures as high as 400 °C for up to one hour, thus pre-oxidizing the film to ensure far greater stability in use. The resistance value can increase as much as 40% during the stabilization, so the original geometry must take this into account and the resistors must start out substantially below their target value. This is very effective in preventing further change in resistance over time [10, 11]. It should be noted that NiCr thin-film chip resistors, if not well-sealed, may be subject to electromigration damage under conditions that include high humidity, low voltage, and ionic influence. This corrosion has resulted in occasional catastrophic failure in the industry.

Table 5.1 Material properties of TaN and NiCr thin film resistors.

	TCR [ppm/°C]	**Sheet Resistivity on Al_2O_3 [Ω/sq]**	**Sheet Resistivity on AlN, BeO [Ω/sq]**	**Stability**	**Tolerance**
TaN	±25	10 ~ 150	25 ~ 100	< 0.5%	1~10%
NiCr	±10	20 ~ 250	50 ~ 150	< 0.5%	1~10%

In this work, we used NiCr (80/20 %) [12] for TFR using e-beam evaporation and firstly checked the resistivity (ρ) versus metal thickness. Table 5.2 reports the results of measured R_{sh} with various conditions. NiCr metal alloy was deposited on both S.I GaAs substrate and Si with SiN_x to avoid the effect of substrate, and 4-point probe measurement was utilized.



$$R = \rho\frac{L}{A} = \rho\frac{L}{Wt} = \frac{\rho}{t}\frac{L}{W} = R_{sh}$$

As we mentioned above, NiCr metal source also oxidizes in an atmosphere, so that the resistivity could be increased. The additional factor which increased the resistivity of TFR was base pressure in evaporator chamber. So we fixed the base pressure at least 8×10^{-7} Torr for all experiments before using e-beam evaporation. The one way to reduce the resistivity is removing chrome oxide by wet etching, and we used Cr-7 chrome etchant to remove the oxidized surface layer of NiCr source. The R_{sh}

were compared in Table. 5.2 with different wet treatments and treatments time. The theoretical resistivity of NiCr is 1 ~ 1.5 × 10^{-6} Ω·mm. If NiCr source was evaporated after only with solvent cleaning, the achieved resistivity was higher about more than twice. On the other hand, much lower resistivity was obtained if we used Cr-7 chrome etchant for de-oxidizing. We increased the treatment time to reduce the resistivity more, but it was saturated already. Because the accurate R_{sh} of 20 Ω/sq (±2 Ω/sq) was required for designing MMIC, and the original R_{sh} must be lower than the target value to prevent further change as we explained above, we finally decided the thickness of NiCr as thick as 850 Å.

Table 5.2 The change of sheet resistance and resistivity of NiCr TFR on two different substrates with solvent cleaning and Cr etching by Cr-7 etchant.

	Thickness [nm]	**Substrate**	**Sheet Resistance [Ω/sq]**	**Resistivity [Ω·mm]**
Solvent cleaning	65	S.I. GaAs	55	3.57×10^{-6}
+Cr-7 Cr etching 10min	65	S.I. GaAs	30	1.9×10^{-6}
+Cr-7 Cr etching 10min	70	S.I. GaAs	27	1.89×10^{-6}
		SiN_x on Si	24	1.68×10^{-6}
+Cr-7 Cr etching 30min	75	S.I. GaAs	24	1.8×10^{-6}
		SiN_x on Si	23	1.725×10^{-6}

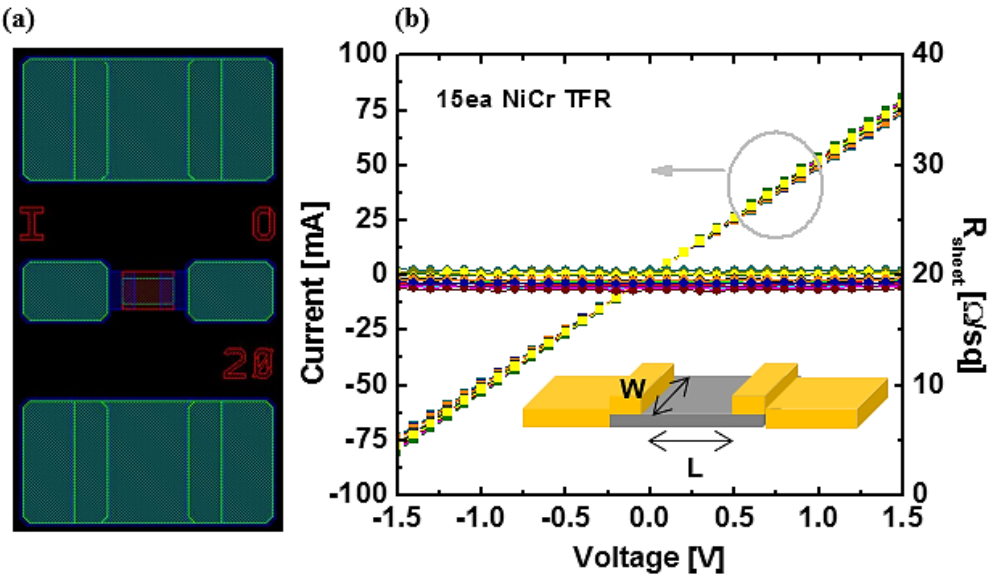


Fig. 5.14 (a) Layout design of TFR with 20 Ω/sq, representatively. (b) 2-point measurement of the fabricated NiCr TFRs which were targeted on 20 Ω/sq.

Figure 5.14(a) demonstrates the actual layout design of NiCr TFR test pattern on GaN-on-Si wafer, and the results of 2-point measurement with 15 TFRs are shown in Fig. 5.14(b). The TFRs were fabricated on inactive region of AlGaN/GaN heterostructure by removing 2DEG channel with SiN_x layer at bottom and top either to make the same structure with TFRs in MMIC, and we could achieve significantly uniform R_{sh}. Also, we checked the change of NiCr resistances after annealing at 400 °C chuck for 4 hours which was quite harsh condition as shown in Fig. 5.15. Due to the SiN_x protecting layer on NiCr, there were just slight increases of resistance with each size of TFRs.

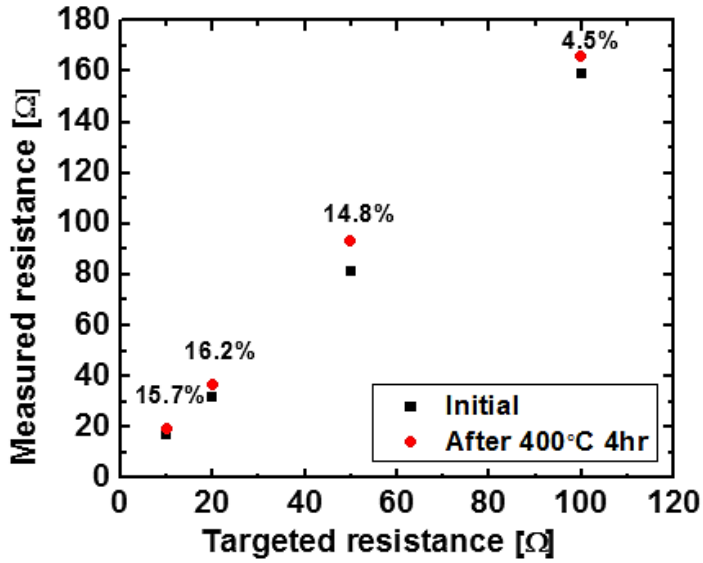


Fig. 5.15 The result of NiCr reliability test with high thermal stress which could be went through during MMIC process.

5.5 Metal-Insulator-Metal (MIM) Capacitor

MIM capacitors in MMIC technology have been investigated for long times. Most of the studies reported about their lifetime and yield which were directly related to breakdown characteristic [13, 14]. The improvement of the breakdown characteristic is associated not only with the dielectric property but also with a metal process so that the process is very sensitive. We also focused on the breakdown voltage of the fabricated MIM capacitor by improvement of the surface of the bottom metal. However, self-resonance frequency (SRF) of MIM capacitor [15] which could be known from small-signal measurement was another problem in GaN-on-Si technology because of an epitaxial layer below which is not semi-insulated. We first investigated various capacitor structures versus below conditions and thickness of used dielectric to increase the SRF as best we could.

5.5.1 Frequency Response of MIM Capacitor

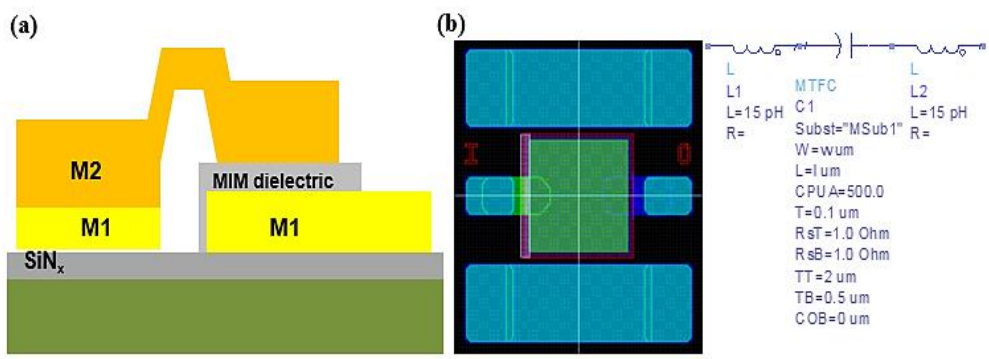


Fig. 5.16 (a) Cross-sectional image of MIM capacitor. (b) Layout design of MIM capacitor and an example of its model.

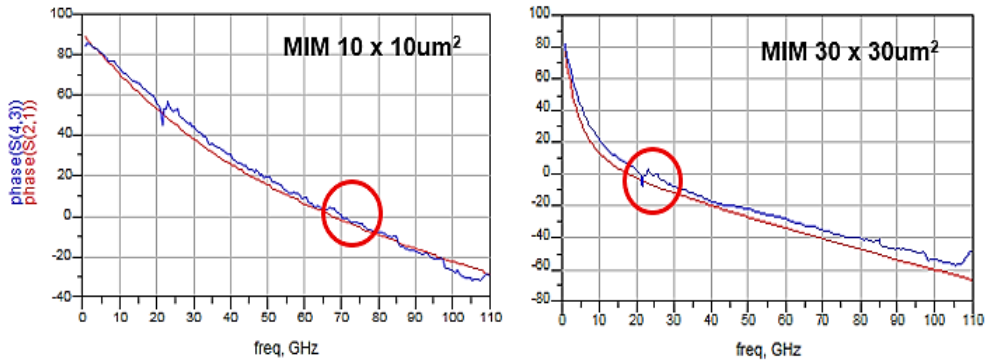


Fig. 5.17 The measured frequency response (phase) of MIM capacitor with two different size to evaluate their SRF characteristics. The measured (blue) and modeled (red) data were plotted together.

First, Fig. 5.16(a) and (b) presents the cross-sectional image of MIM capacitor used in MMIC and its layout with design model [16]. The SRF of capacitor is the frequency that the phase changes from + value to – value and its characteristic is directly associated with the size of the capacitor because an inductance can be increased by the large metal structure. However, Fig. 5.17 shows the result of frequency response that we found the problem about the SRF even if the size of the capacitor was not large enough. Because the small-signal measurement of the passive element is performed without voltage bias, it is easy to suppose that the main reduction factor of SRF is the thickness of dielectric (t_d). If the bottom and top metal separate far away using thicker dielectric, the inductance and the signal loss via dielectric may be decreased. As shown in Fig. 5.18, the SRF of MIM capacitor with the size of 30 × 30 μm^2 was increased from 20 GHz to 45 GHz which made it possible to be employed for RF matching in MMIC design at target frequency.

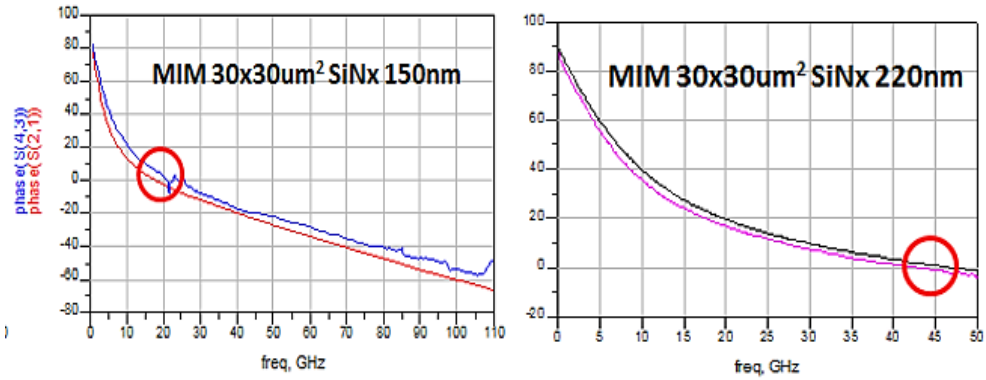


Fig. 5.18 The SRF characteristics of MIM capacitor of 30 × 30 μm^2 before (left) and after (right) increasing the dielectric thickness. The measured (blue) and modeled (red) data were plotted together.

Further, we estimated the additional factors that could have an effect on SRF characteristic. All experiments were performed with GaN-on-Si wafer and the capacitors in Fig. 5.19(a) were fabricated just on low-resistivity GaN buffer layer. Other two capacitors were fabricated on high-resistivity GaN buffer layer without and with SiN_x owing to the same reason with the experiment of NiCr TFR (Fig. 5.19(b) and (c)), because the substrate loss should be considered when the active and passive devices were designed even though the target frequency of this work was 27 GHz which was not that high. The phases of the S_{21} parameter are also plotted in Fig. 5.19, and the results from measurement and modeling almost corresponded. The main difference of among the three samples was observed at small size capacitors, such as 10 × 10 μm^2 and 30 × 30 μm^2. As the resistivity through the downside increased, the phase was close to the ideal value of modeling. However, there was no significant effect on SRF with different structures under the bottom metal. Fig. 5.20.

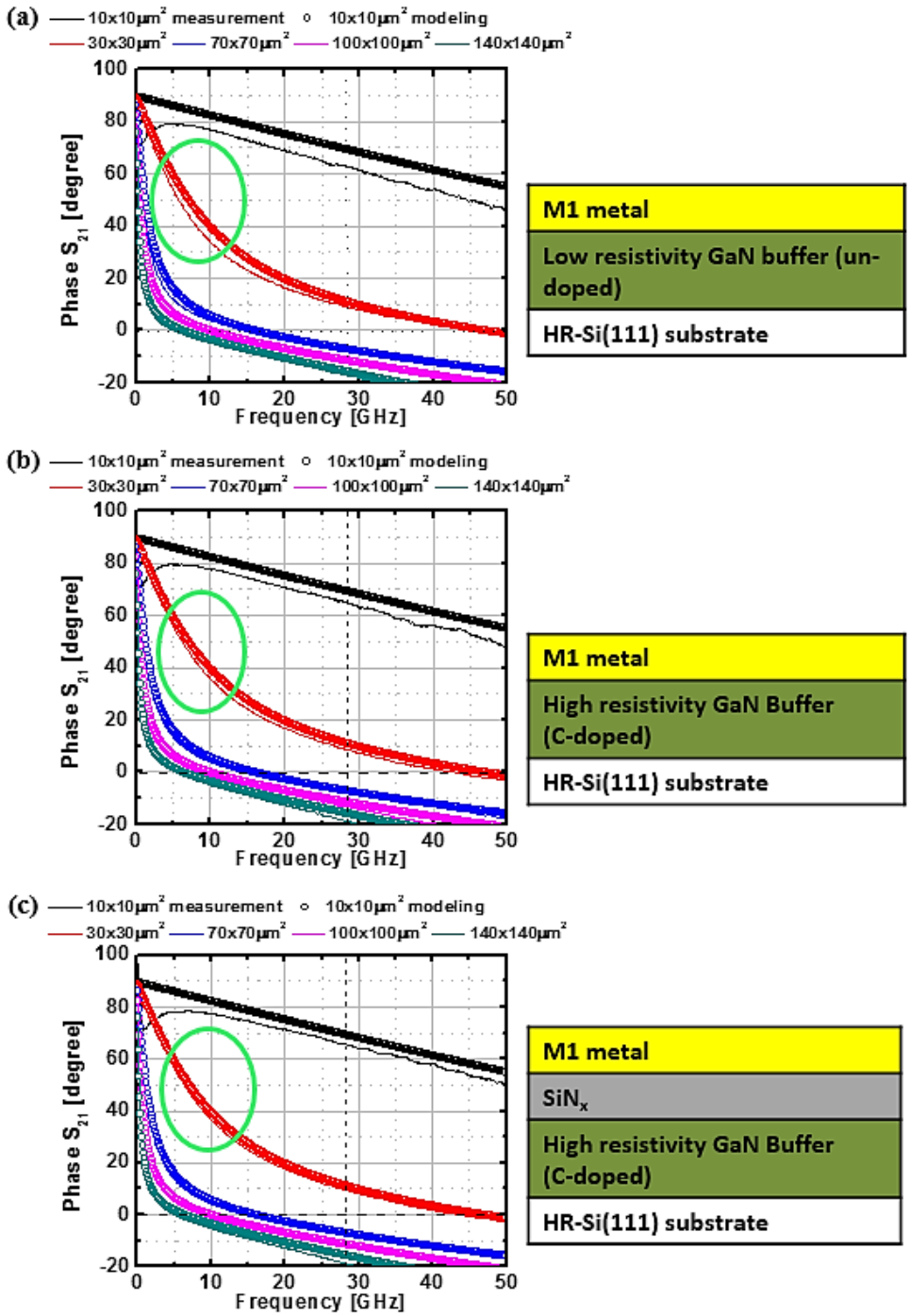


Fig. 5.19 SRF characteristics of the fabricated MIM capacitor with three different wafers and different size. MIM capacitor on (a) low resistivity buffer (b) high resistivity buffer (c) high resistivity buffer with SiN_x insulating.

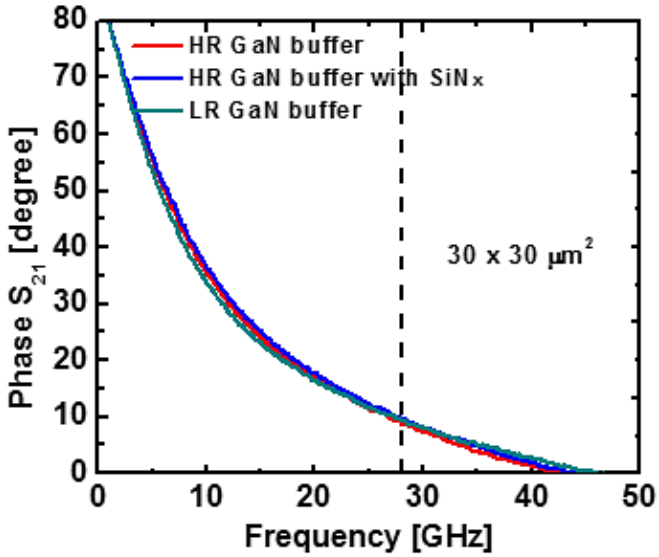


Fig. 5.20 Frequency-phase characteristics of MIM capacitors of 30 × 30 μm^2 with various bottom conditions.

Figure 5.21 shows the gain of S_{21} which could also provide the design rule of MMIC PA. The MIM capacitors with size up to 30 × 30 μm^2 were used for RF matching and the capacitors over 30 × 30 μm^2 were used for DC blocking and suppressing of low-frequency oscillation. The larger capacitor is better to be used for DC blocking, but the capacitor of 30 × 30 μm^2 which demonstrated the gain within - 1 dB also had no problem to be used for DC blocking at our target frequency.

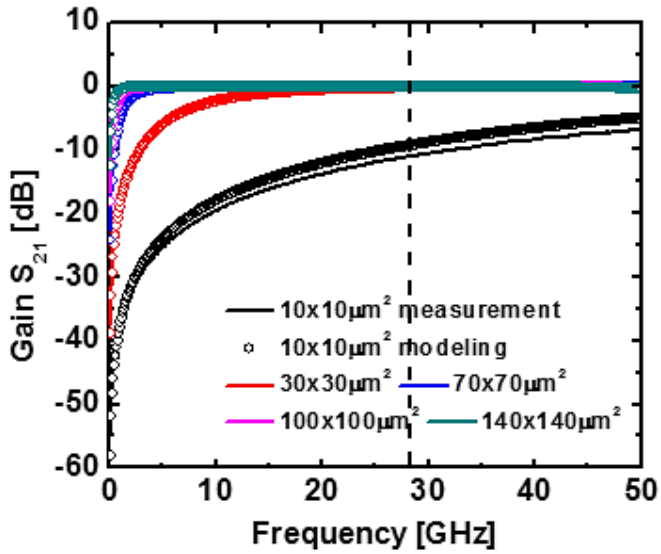


Fig. 5.21 Frequency-gain characteristics of MIM capacitors of various size.

5.5.2 Breakdown Voltage of MIM Capacitor

Table. 5.3 presents the properties of SiN_x using remote PECVD for the dielectric of MIM capacitor. Its breakdown field and dielectric constant (ε_r) were evaluated by making metal-oxide-semiconductor (MOS) capacitor with n-type Si wafer. From the evaluated breakdown field, we could predict the required minimum t_d considering the target breakdown voltage. If we targeted the breakdown voltage larger than 150 V, the t_d should be thicker than 166.6 nm (Table. 5.4). However, the actual MIM capacitor has a discrepancy in the breakdown characteristic from the theoretical estimation so that we utilized the dielectric thickness of > 200 nm to retain process budget, also this could help to improve the SRF characteristics.

Table 5.3 The conditions and properties of used SiN_x dielectric for MIM capacitor.

Chuck temp. [°C]	Source power [W]	Pressure [mTorr]	SiH_4/NH_3	Breakdown field [MV/cm]	Dielectric constant
200	300	20	8/40	9~10	7

Table 5.4 The required and resulted properties of MIM dielectric.

Breakdown voltage [V]	Dielectric thickness [nm]	Capacitance density [fF/μm^2]	Target frequency [GHz]
>150	>166.6	0.37	>26

Unlike MIS capacitor, the roughness of bottom metal [17, 18] which may cause early breakdown of dielectric is essentially considered to achieve more stable breakdown voltage, assuming the surface of metal region is cleaned. It is easy to be formed a particle (Au spitting) [19, 20] on the metal surface during the metal deposition, and it can be a start point of leakage current owing to the high concentration of electric field. Most of the studies reported about the metal sources cleaning to make the smooth surface [21-23]. We also employed solvent cleaning with methanol and isopropyl alcohol before the metal (Ni and Au) deposition using e-beam evaporation. Figure 5.22 shows the atomic force microscope (AFM) image of deposited Ni/Au surfaces without and with metal source cleaning. The measured average roughness was considerably reduced and we could obtain much smoother metal surface.

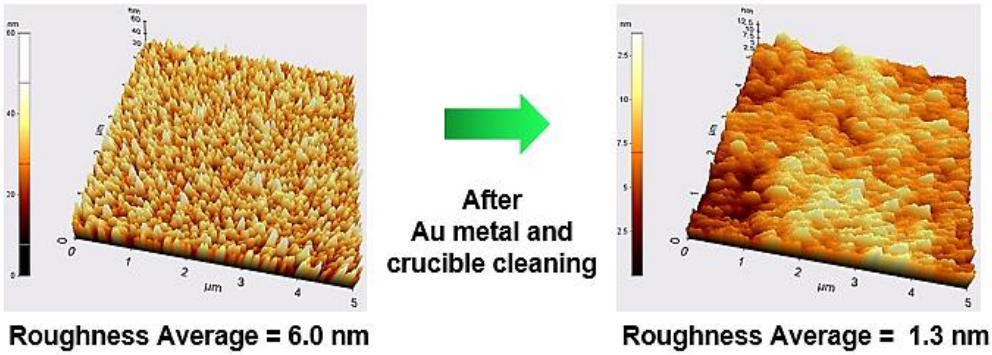


Fig. 5.22 AFM measurement of the surface of bottom plate for MIM capacitor without (left) and with (right) Au metal source solvent cleaning.

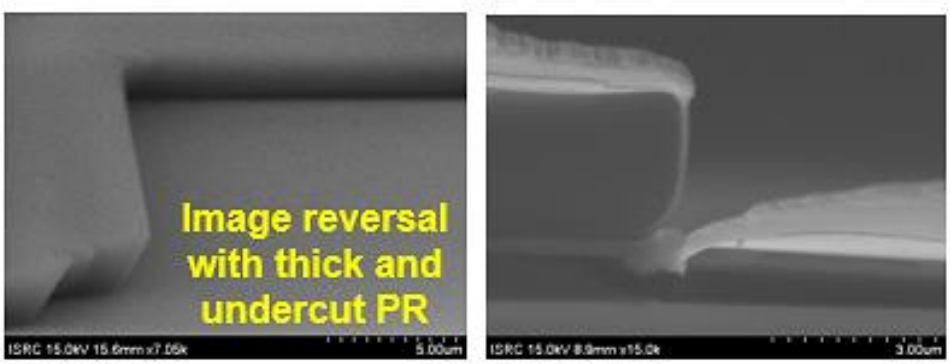


Fig. 5.23 SEM images of image reversal patter with thick AZ5214 for sputtered metal lift-off process.

But, in terms of repeatability, it had a disjunction between the research reports and the actual process. Because of the method of the metal deposition process, carbon can easily contaminate the metal source in e-beam evaporation chamber that makes particle on the metal surface whether the source was cleaned or not. So we adapted different method of metal deposition process to improve the yield of capacitor and process stability. A metal sputtering is generally independent of carbon contamination, whereas

used without photoresist (PR) patterning owing to the high step coverage which makes hard to employ metal lift-off process. In MMIC process, we should develop the thick and large under-cut profile with AZ5214 (image reversal) PR to apply metal lift-off process to form the bottom metal of MIM capacitor using sputtering. Figure 5.23 is the SEM images of optimized PR pattern to make lift-off possible even with sputtering of high step coverage. After employing this method, we could achieve the better bottom metal surface with high repeatability. As a result, the fabricated MIM capacitors demonstrated much more uniform breakdown voltage above 180 V, whereas the capacitors using e-beam evaporation showed the large variation (Fig. 5.24(a) and (b)).

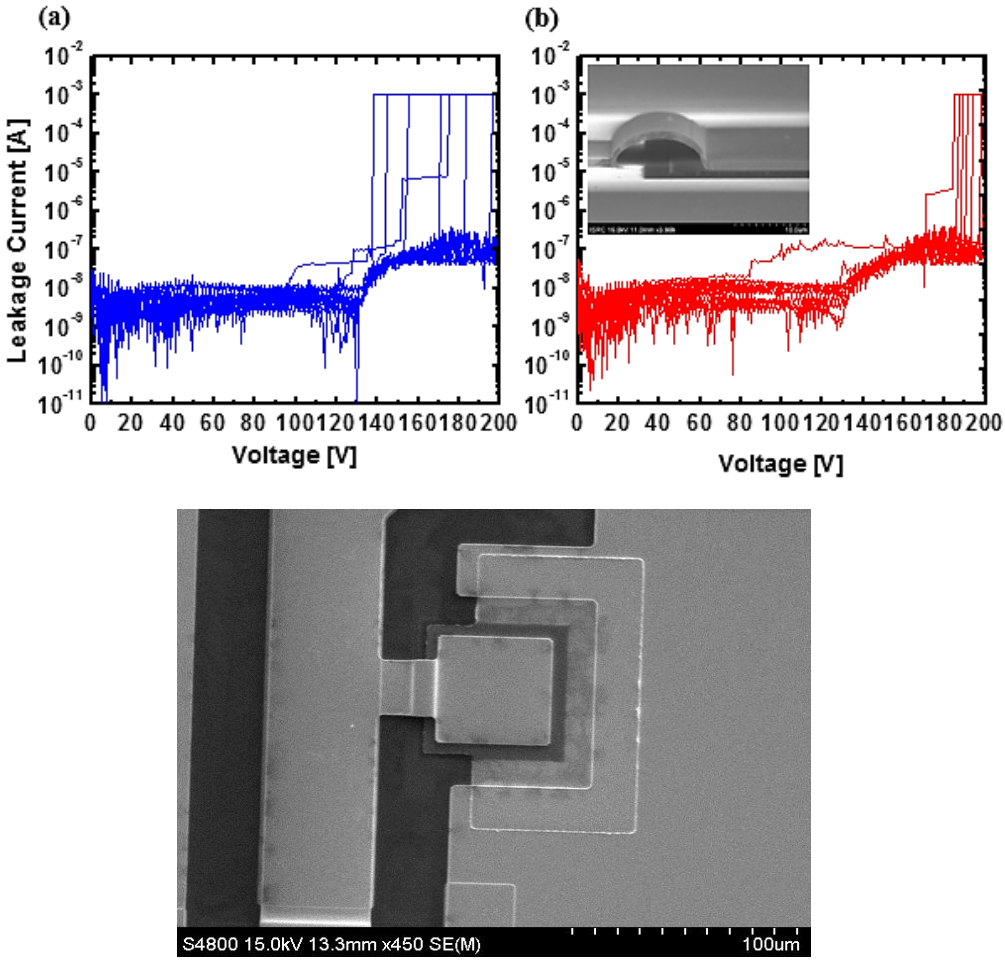


Fig. 5.24 Breakdown characteristics of 30 × 30 μm^2 MIM capacitor with metal (a) evaporation and (b) sputtering as the bottom plate. Inset of (b) shows SEM image of the fabricated MIM capacitor with air-bridge. SEM images of top view of the MIM capacitor employed in MMIC (bottom).

5.6 Coplanar Waveguide (CPW) Transmission Line

The separate spiral inductor model was substituted with transmission line because the Ka-band does not need such a long inductor line. CPW line was modeled by using conventional model in ADS library, and line loss of 1 dB/mm was measured at 30 GHz.

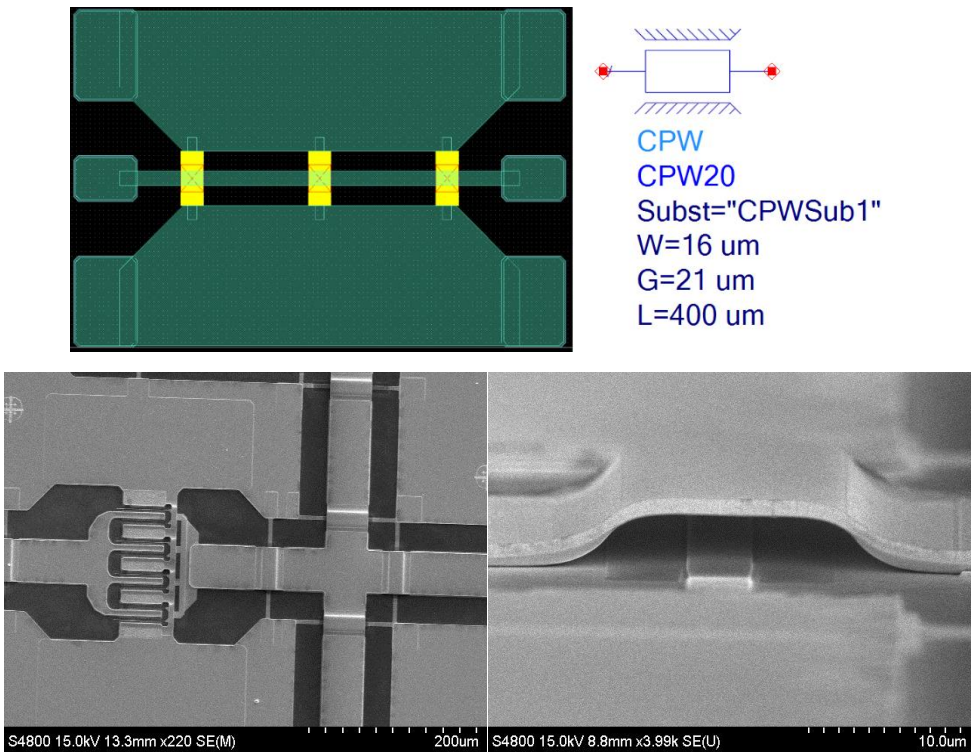


Fig. 5.25 Layout design of CPW transmission line and ADS model (top). SEM images of CPW transmission line and air-bridge to avoid short between ground and signal (bottom).

5.7 Unit Power Cell Design & MMIC Process

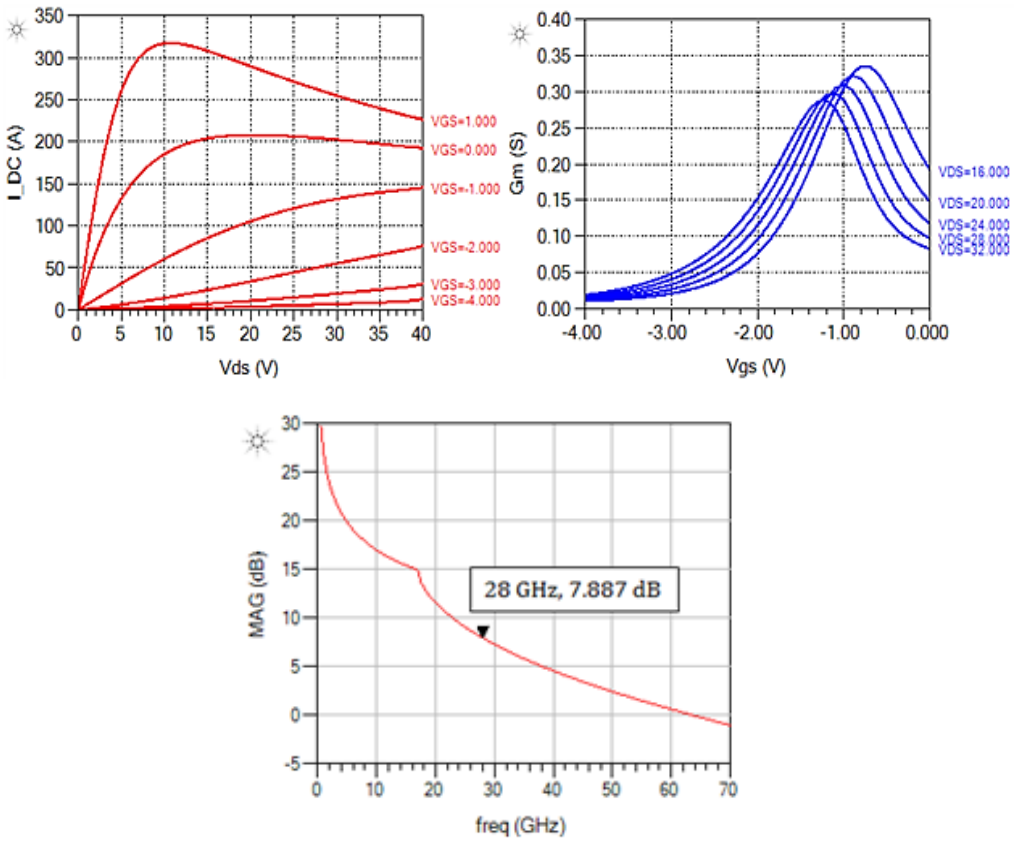


Fig. 5.26 ADS simulation results of DC drain current, RF transconductance, and MAG with the device of 8 × 50 μm.

A Ka-band unit power cell (PC) must demonstrate both the high output power and high gain characteristics at high operation frequency. To choose the device with large W_G and high gain for employing at circuit design, we considered G_m and maximum available gain (MAG) from the model of the fabricated devices. As a result, 8 × 50 μm device was utilized in this work (Fig. 5.26), but 1-stage power cell did not exhibit enough gain so that we

designed 2-stage cascade to achieve the high gain and high output power simultaneously as shown in Fig. 5.27. The device of 8 × 50 μm was employed for the main transistor (2nd TR) which generates output power and the device with 4 × 50 μm was employed as the drive transistor (1st TR). The power cell was designed with the center frequency of 28 ~ 30 GHz, and we also regarded the variation of the fabrication process so the input and output ports used double resonance matching to be matched at the large bandwidth. Especially, the output port was designed that the PA can obtain the maximum output power using power matching. The CPW which has superior characteristic at high-frequency and does not need backside process was applied to the transmission line (Fig. 5.28).

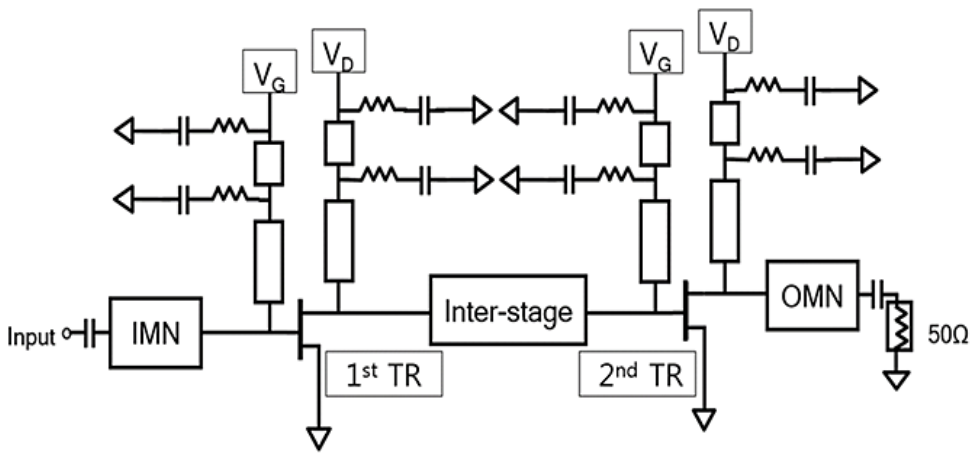


Fig. 5.27 Block diagram of designed 2-stage cascade power cell.

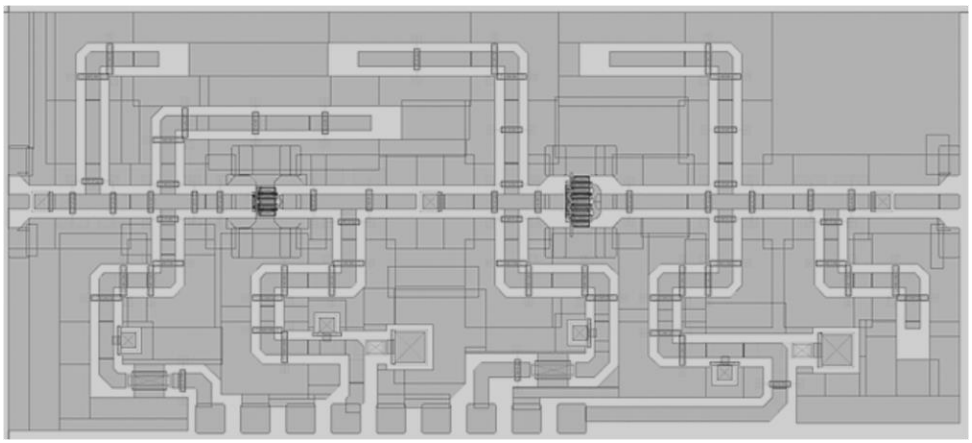


Fig. 5.28 Layout design of designed 2-stage common source MMIC power amplifier for Ka-band.

Our process flow of AlGaN/GaN-on-Si substrate MMIC is shown in Fig 5.29. The process details until fabricating the source, drain, and gate of AlGaN/GaN HEMT was same with the flow in chapter 2 and chapter 4. Due to MIS device process, such as wet treatment or dielectric deposition at high temperature, the fabrication of passive elements was done in conclusion. After the gate formation, a thin SiN_x film of 30 nm-thick was deposited at 250 °C to protect the devices using remote PECVD. The passive elements were fabricated on inactive region over deposited dielectric layers to avoid the exposure of epitaxial layer.

Surface cleaning

SiN_x Pre-passivation

Ohmic contact& alloy

MESA isolation

SiN_x Removal

SiN_x Re-passivation

Gate process (MIS)

SiN_x 2nd passivation

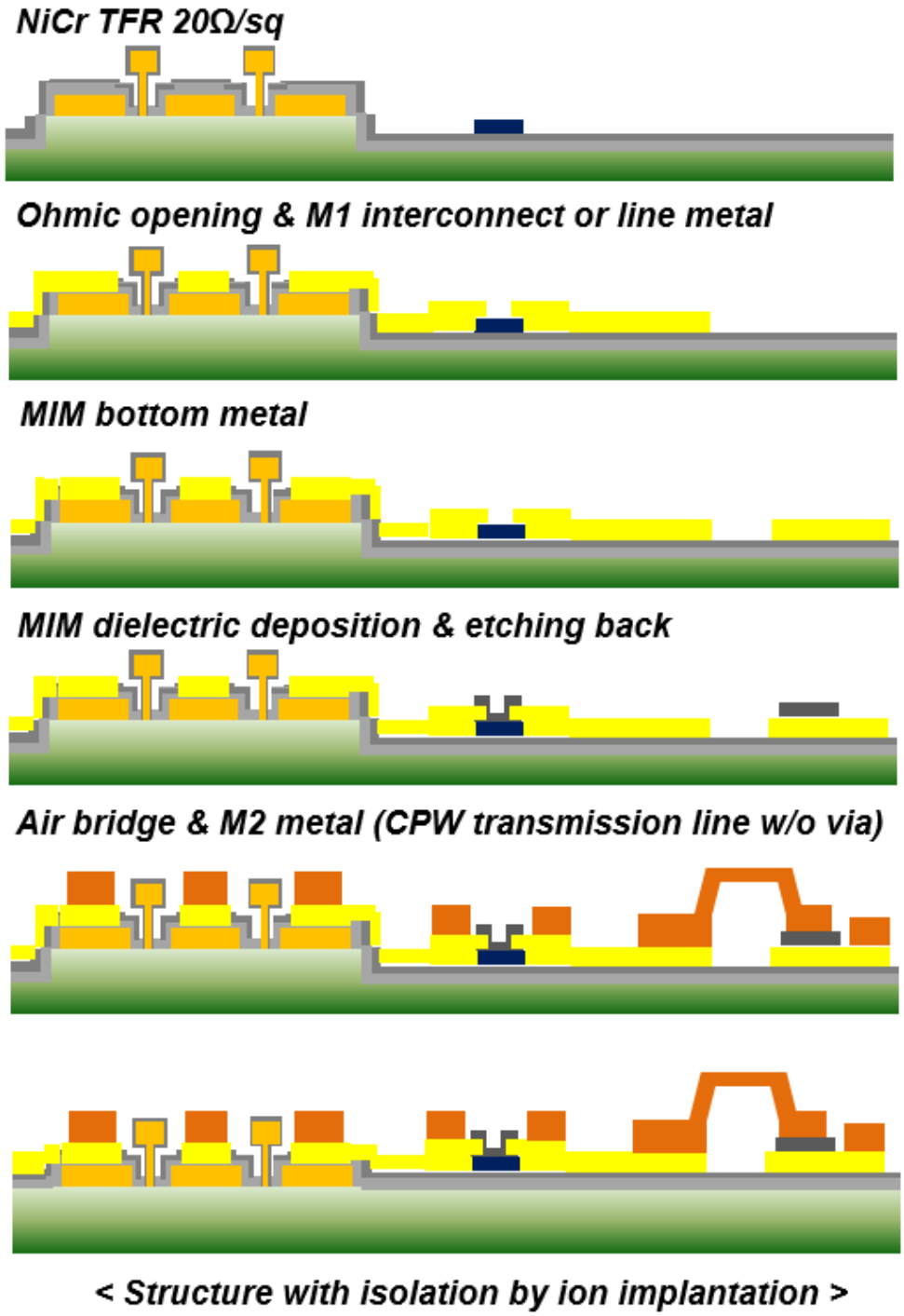


Fig. 5.29 Entire process flow of GaN MMIC of chip level without backside process.

- NiCr TFRs were evaporated with targeted R_{sh} value of 20 Ω/sq (±2 Ω/sq).
- Interconnection pad electrodes and signal lines were formed with Ni/Au (=40/450 nm) evaporation after ohmic and gate contact areas were opened by RIE etching. We designed and employed CPW line and all signal lines and passive elements were formed at inactive region without exposure of GaN surface.
- To make MIM bottom electrodes, Cr/Au (=40/300 nm) layer was deposited using sputtering. Unlike conventional sputtering process, we made the electrodes layer through metal lift-off method.
- After solvent (acetone/IPA) cleaning, a thick SiN_x film of ~250nm-thick was deposited at 250 °C for MIM dielectric and protecting top surface of NiCr from oxidation or ionic influence also using remote PECVD. Table. 5.5 contains both dry and wet etching rate of both SiN_x film for protection of active device and this step. The large difference in wet etching rate was required to remove SiN_x which was used for passive elements selectively.
- The thick SiN_x dielectric film except MIM and NiRr regions was removed (etch-back) because additional dielectric could increase parasitic capacitance at mmw application.
- To make equipotential source electrodes and MIM top electrodes, the thick interconnection metal and air-bridge processes were simultaneously conducted with Ti/Au (=50/1450 nm) evaporation.

Table 5.5 The properties of the dielectrics for both device protection (top) and MIM capacitor (bottom). Dry etch rate was measured by using SF_2 20W RIE and wet etch rate was measured with B.O.E 7:1.

	SiH_4 /N_2/Ar [sccm]	**Pressure [mTorr]**	**Source power [W]**	**Dep. rate [Å/sec]**	**Dry/wet Etch rate [Å/min]**
Device protection layer	2.8/9/90	35	200	0.55	150/110

	SiH_4/ NH_3 [sccm]	**Pressure [mTorr]**	**Source power [W]**	**Dep. rate [Å/sec]**	**Dry/wet Etch rate [Å/min]**
MIM dielectric	8/40	20	300	1.38	1400/1500

5.8 Performances of Fabricated MMIC PA

In this section, we will demonstrate the fabricated Ka-band GaN-on-Si MMIC PA with the flow of process improvement in the previous chapters. The small-signal characteristics of the MMICs with three different active device structures (Schottky, only PEALD SiN_x MIS, SiN_x and HfON dual MIS) were compared. And we fabricated the final version of MMIC to measure large-signal characteristics with isolating by ion implantation to reduce the off-state leakage current and improve current collapse phenomena and Y-gate process to reduce gate resistance with low parasitic capacitance. We also measured the power on-state time stress of each MMIC PA to estimate the reliability of MIS structure which has the high potential of the GaN-on-Si technology with improved output power in comparison to the conventional Schottky device. Because the interface states of MIS structure cannot be same as Schottky contact whatever good process technology is employed, the MIS MMIC exhibited the poorer reliability performance, but we could find the right direction of GaN-on-Si RF devices from the reliability measurement.

5.8.1 Small-Signal Characteristics

Figure 5.30 shows the fabricated MMIC with probing representatively, and all measurements were performed without any packaging or cooling system. And the Table 5.6 lists up the several MMICs with different process and wafer used in this work. We first measured the small-signal characteristic of each IC which was applied Schottky, PEALD SiN_x MIS, and HfON MIS (dual MIS) with thin SiN_x interface layer at various DC bias by using VNA.

As shown in Fig. 5.31, the maximum gain of MMICs with MIS structures were similar with Schottky, but the peak center frequency was negatively shifted at dual MIS MMIC. This was because the frequency-gain characteristic of dual MIS active device exhibited lower gain than other two devices definitely. Also the MMICs with wafer 2 demonstrated the higher maximum gain at the center frequency than with wafer 1, and the formation of CPW transmission line on dielectric layer slightly improved the maximum gain additionally (17.98 dB to 18.28 dB for Schottky and 18.5 dB to 18.71 dB for dual MIS). However, negative shift of center frequency at dual MIS MMIC was still observed in comparison to Schottky, and that center frequency could break the bounds of Ka-band which was our target frequency (Fig. 5.32).

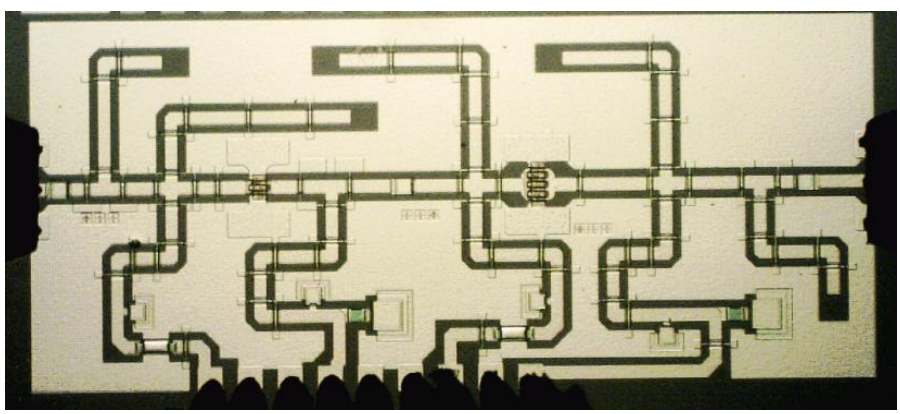


Fig. 5.30 Microscope image of the fabricated 2-stage common source GaN-on-Si MMIC PA with input (left) and output (right).

Table 5.6 Different process conditions of the fabricated MMICs. Wafer 1 and 2 are the same epitaxial structures.

	Wafer	**Isolation**	**Gate structure**	**CPW formation**	**Gate contact**
Sample 1	Wafer 1	Mesa	Field-plated (Normal)	On GaN	Schottky
Sample 2	Wafer 1	Mesa	Field-plated	On GaN	SiN_x
Sample 3	Wafer 1	Mesa	Field-plated	On GaN	Dual
Sample 4	Wafer 2	Mesa	Field-plated	On GaN	Schottky
Sample 5	Wafer 2	Mesa	Field-plated	On GaN	Dual
Sample 6	Wafer 2	Mesa	Field-plated	On SiN_x	Schottky
Sample 7	Wafer 2	Mesa	Field-plated	On SiN_x	Dual
Sample 8	Wafer 2	Implant	Field-plated	On SiN_x	Dual
Sample 9	Wafer 2	Implant	Y-gate (Field-plated)	On SiN_x	Dual

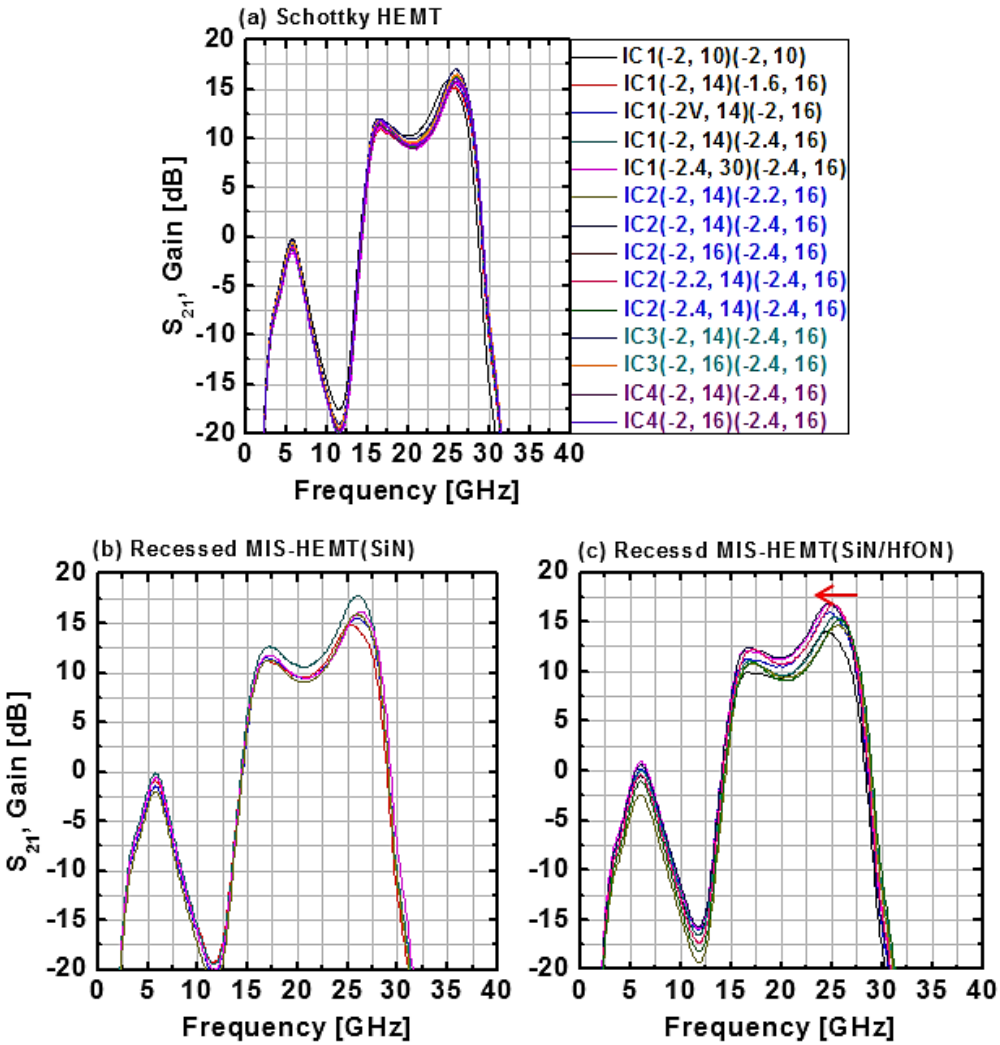


Fig. 5.31 Small-signal gain characteristics (S_{21}) of MMICs in (a) sample 1 ((V_{gs1}, V_{ds1})(V_{gs2}, V_{ds2})) (b) sample 2 (c) sample 3 with various DC bias.

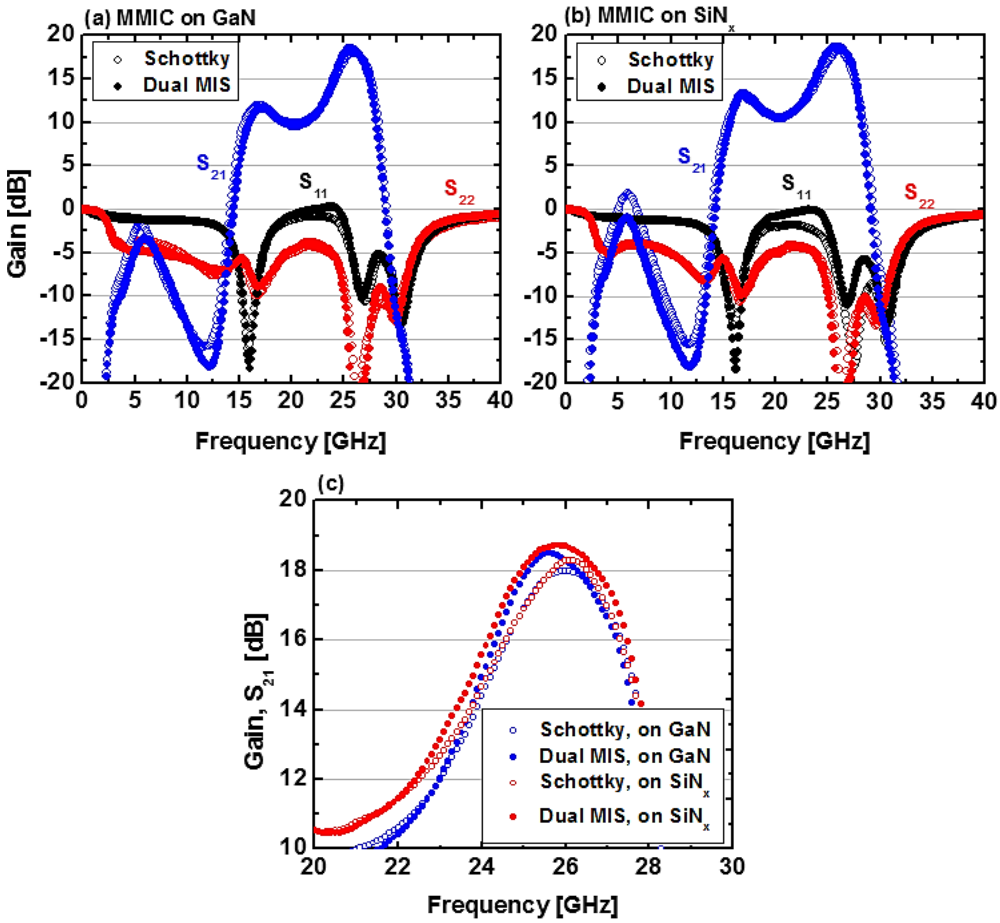


Fig. 5.32 Small-signal gain characteristics of (a) sample 4 (V_{gs1} = -2 V/V_{ds1} = 10 V, V_{gs2} = -2 V/V_{ds2} = 16 V) and sample 5 (-2.4 V/12 V, -2.4 V/20 V) (b) sample 6 (-2 V/16 V, -2 V/16 V) and sample 7 (-2.4 V/12 V, -2.4 V/20 V). (c) Increase of maximum gain by insulating GaN surface under the CPW transmission line.

We found the solution for increasing center frequency by forming inactive region with ion implantation process instead of mesa etching. Not only the improving the performance of the active device but also keeping the circuit away from the H.R Si substrate was achievable by forming the CPW transmission line with a planar structure. Figure 5.33 (b) shows the increase

of center frequency of dual MIS MMIC with more increase of maximum gain (> 19 dB) by employing ion implantation process that can be operating at real Ka-band.

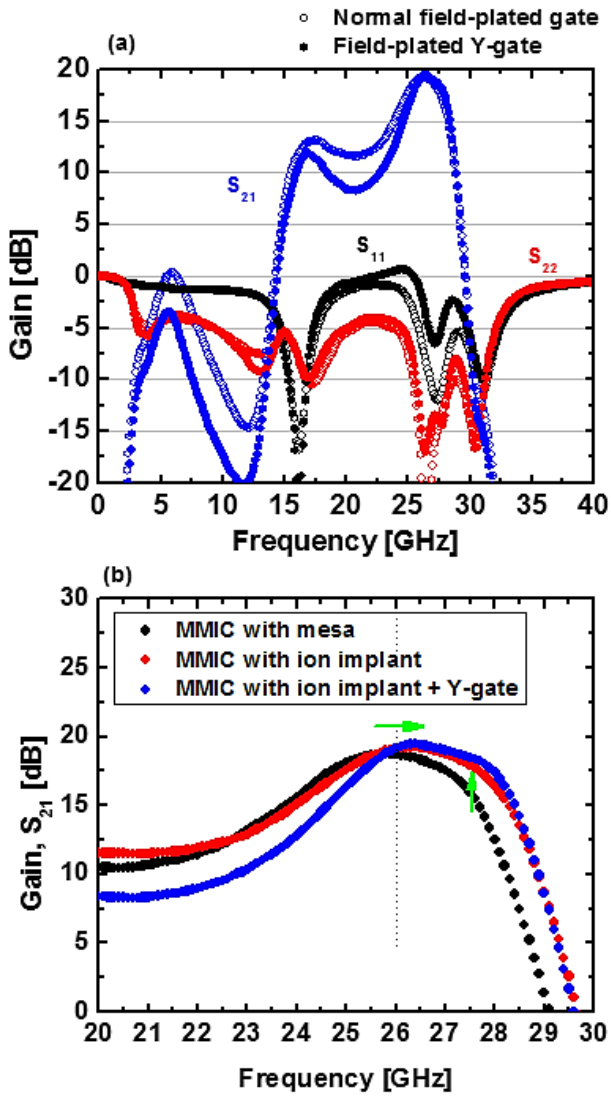


Fig. 5.33 Small-signal gain characteristics of (a) sample 8 (-1.6V/14 V, -1.6 V/20 V) and sample 9 (-2.4 V/14 V, -2.8 V/20 V) (b) Increase of maximum gain and center frequency by employing ion implantation and Y-gate structure with low gate resistance and low parasitic capacitance.

5.8.2 Large-Signal Characteristics

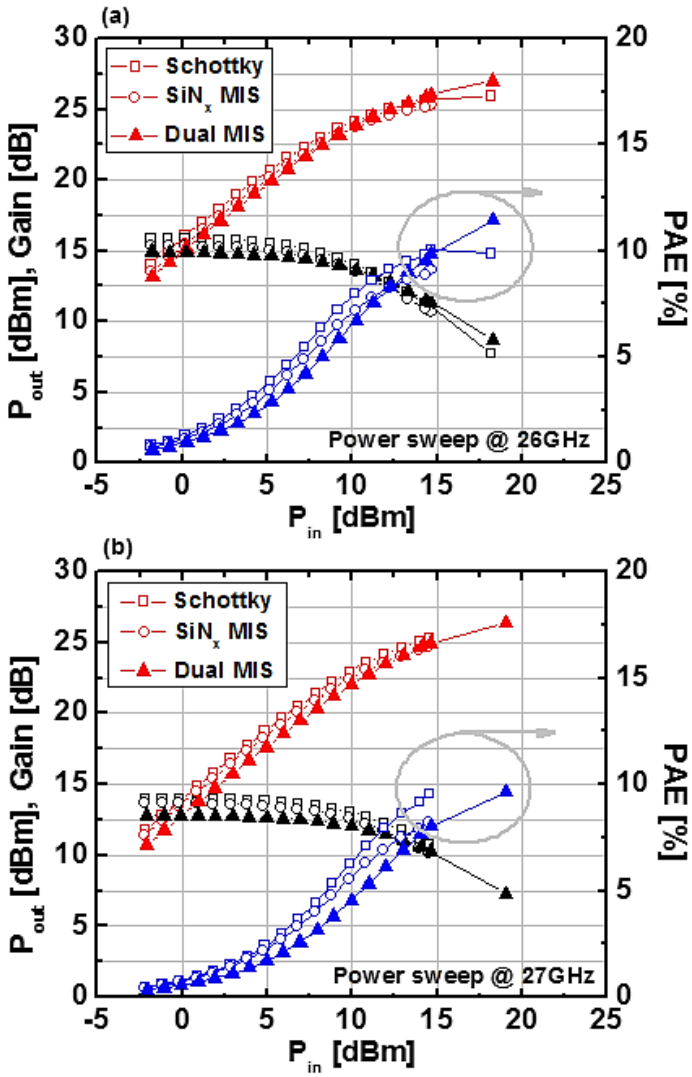


Fig. 5.34 Large-signal characteristics of sample 1, 2, and 3 at (a) 26 and (b) 27 GHz. The applied DC bias at each device was (-1.6 V/12 V, -1.8 V/18 V) for Schottky, (-1.6 V/12 V, -1.8 V/18 V) for SiN_x MIS, and (-2.2 V/18 V, -2 V/14 V) for dual MIS.

After we found the proper operating voltages of first stages and second stages for each MMIC, respectively, the large-signal characteristics were measured on the chuck. The MMICs with wafer 1 demonstrated the low output power and PAE as shown in Fig. 5.34, while the MMIC with dual MIS structure showed unsaturated output performance which could have the higher output power and PAE characteristics. As similar with the small-signal characteristics, the output power and PAE were gradually increased with the higher operation voltage as the different processes were applied (Fig. 5.35). The dual MIS MMIC always showed the higher output power and peak PAE performance than Schottky MMIC at each process condition. For the MMICs with mesa etching isolation, the maximum output power was achieved at 26 GHz, but the maximum output power of MMIC with ion implantation isolation was obtained at 26.5 GHz. The final versions of MMICs (sample 8 and 9) were fabricated with wafer 2 was employed ion implantation, dual MIS structure, and the CPW line was formed on the dielectric layer. The results of power sweep are plotted in Fig. 5.36. The MMIC applied normal field plate gate exhibited the maximum output power of 28.98 dBm at 26.5 GHz with PAE of 14.2 %, whereas the MMIC with field-plated Y-shaped gate demonstrated the output power of 29.5 dBm with PAE of almost 16 %. The output power was increased more than twice from sample 1 (0.339 W) to sample 9 (0.891 W) even if the optimum operation frequency was also increased.

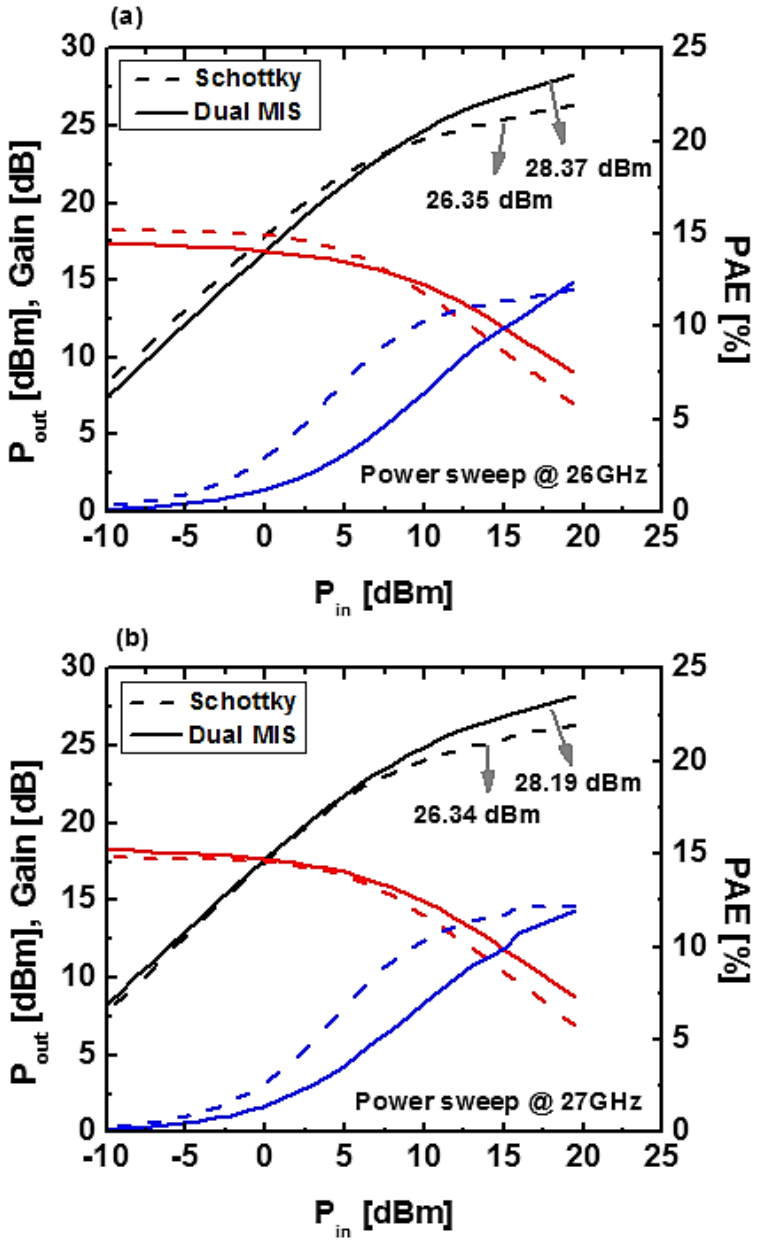


Fig. 5.35 Large-signal characteristics of sample 6 and 7 at (a) 26 and (b) 27 GHz. The applied DC bias at each device was (-2 V/12 V, -2 V/18 V) for Schottky, (-2.2 V/16 V, -2.2 V/20 V) for dual MIS.

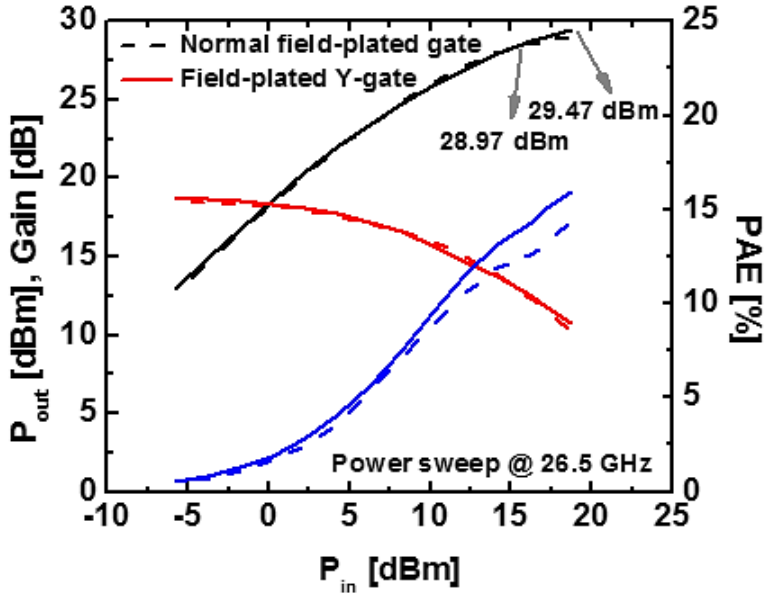


Fig. 5.36 Large-signal characteristics of sample 8 and 9 at 26.5 GHz. The applied DC bias at each device was (-1.8 V/18 V, -2 V/20 V) for normal field-plated gate, (-2 V/18 V, -1.8 V/20 V) for field-plated Y-gate.

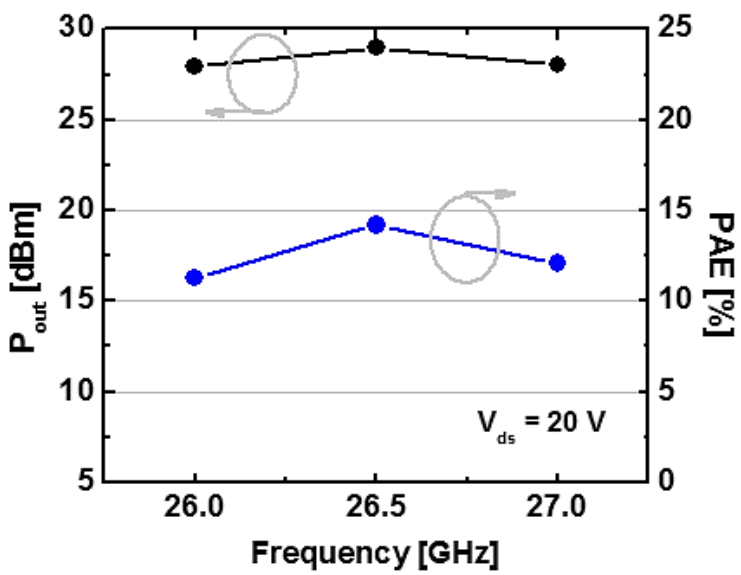


Fig. 5.37 Measured bandwidth of output power and efficiency of sample 8.

This result was achieved only with front-end process with typical AlGaN/GaN heterostructure on Si substrate, and that indicated the GaN-on-Si mmw MMIC can also demonstrate watt-level output power with 20 % PAE. Figure 5.38 and Fig. 5.39 present the results of GaN power amplifier of other research groups [24-45]. There are some results of GaN-on-Si devices for Ka-band [46, 47], but no results with amplifier level. Fig. 5.38 shows the results of output power and PAE beyond K-band, and their gate length and operation voltage were spread out from 0.1 to 0.25 μm and from 10 to 35 V, respectively. Although GaN-on-SiC is the main material for GaN RF technology due to their superior properties, GaN-on-Si can substitute with low cost and watt-level output power by employing MIS structure. Further improvements were simply expected by using large gate width devices in MMIC design or making a 3-stage amplifier as shown in Fig. 5.39. Also our measurement was not considered thermal degradation which could impact on both operating drain voltage and maximum drain current during operation and limited by input drive amplifier so that the output power was not saturated yet.

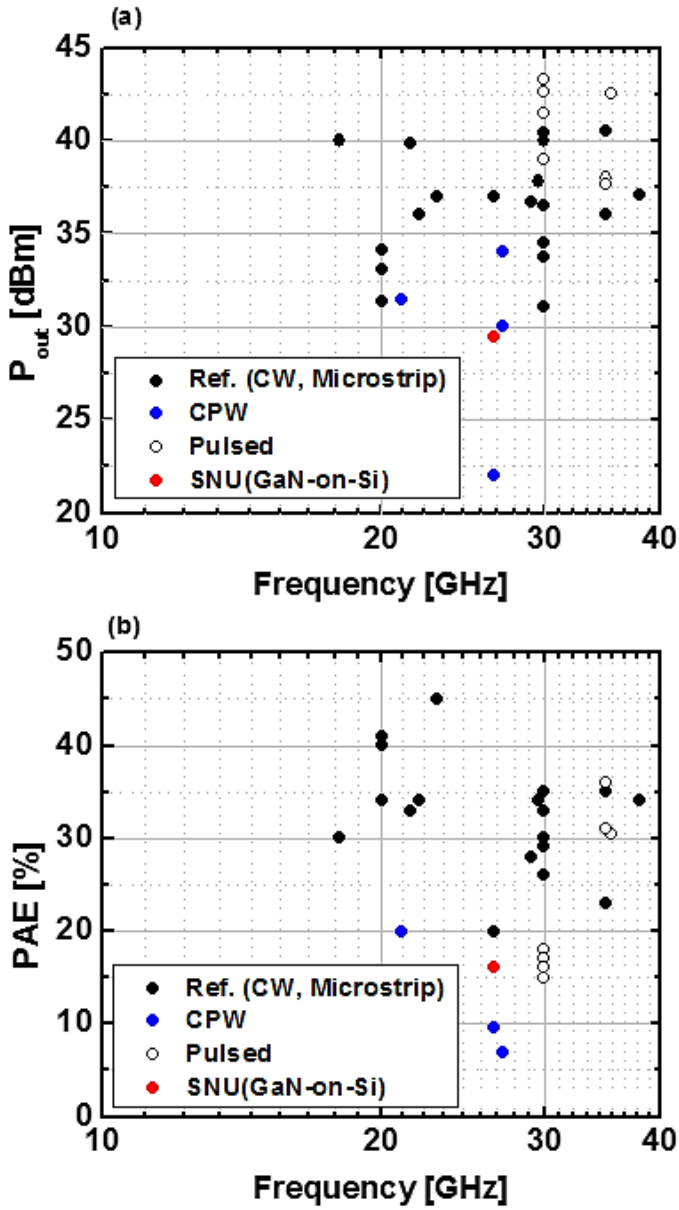


Fig. 5.38 The results of (a) output power and (b) PAE for GaN MMIC PAs beyond K-band versus operation frequency with different method of measurements. All results were demonstrated by GaN-on-SiC.

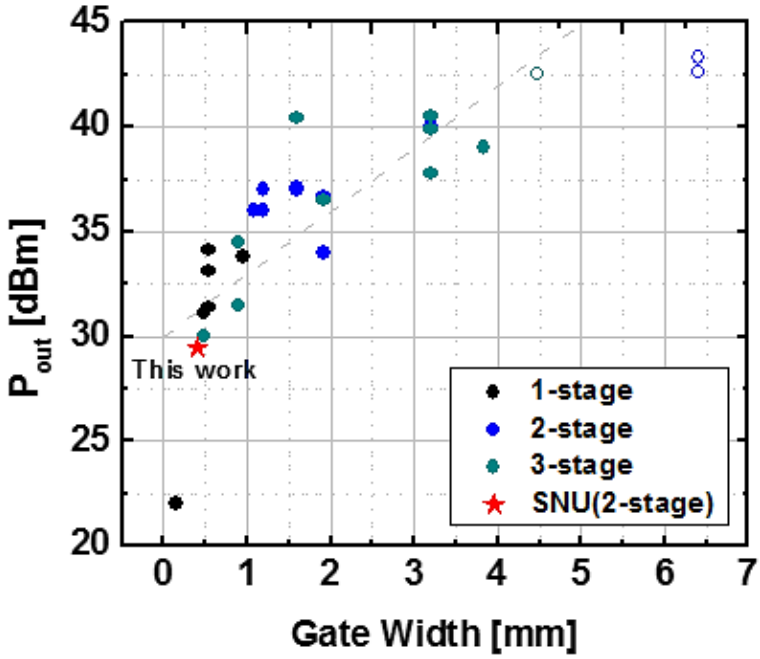


Fig. 5.39 The results of output power beyond K-band for GaN MMIC PAs versus total gate width of output stage with different number of stages. All results were demonstrated by GaN-on-SiC. Both continuous wave (solid) and pulsed (open) measurement are plotted.

5.8.3 Reliability of GaN-on-Si MMIC PA

We found the several methods to improve the output power characteristic of 26.5 GHz GaN-on-Si MMIC PA. However, the conventional GaN RF technology with Schottky gate contact has reached substantially stable performance in terms of not only maximum output power but also reliability. The MIS structure we applied to MMIC in this work presented better power performance than Schottky contact, but it was easy to anticipate its poorer reliability characteristic because of the MIS interface state which has larger non-ideality than Schottky contact. The reliability of MMIC usually evaluated

through the long-term injection of input power such as during 1000 hours, and observe the degradation of output power or failure [48, 49]. The input condition of estimating the reliability is P_{-3dB} point generally.

We similarly estimated the reliability of fabricated MMICs with each differently employed process. Before the measurement of time-stress, we considered the channel temperature when the device was operating to verify the effect of self-heating from the trapping effect which is also the factor of current degradation followed by gain compression. Our measurement condition had only external fan for cooling and no packaging structure such as backside process. The generated heat during the device operating was simply calculated from consumed DC power and output power. For example, the net consumed power for second power stage device of 8 × 50 μm in sample 9 can be expected by subtracting the average output power of 0.8 W from consumed DC power of 2.88 W (= 18 V × 0.16 A). The thermal resistance of the device of 8 × 50 μm was measured by the pulsed I-V method in the previous section without any cooling system either. Thus, the calculated channel temperature was 101.92 °C (= 2.08 W × 49 °C /W), and the actual temperature might be below then due to external fan cooling during power measurement. Because the size of device employed in MMIC design was not large enough, the expected channel temperature was not that high in comparison to that of theoretical microwave applications [36, 50] which require better cooling system than our result. Also, we confirmed the channel temperature by ANSYS thermal simulation with same structure with our fabricated devices as shown in Fig. 5.40. The results of simulation with 8 × 50 μm device in second stage of MMIC and applied power demonstrated similar peak channel temperature of 96.39 °C near the gate edge.

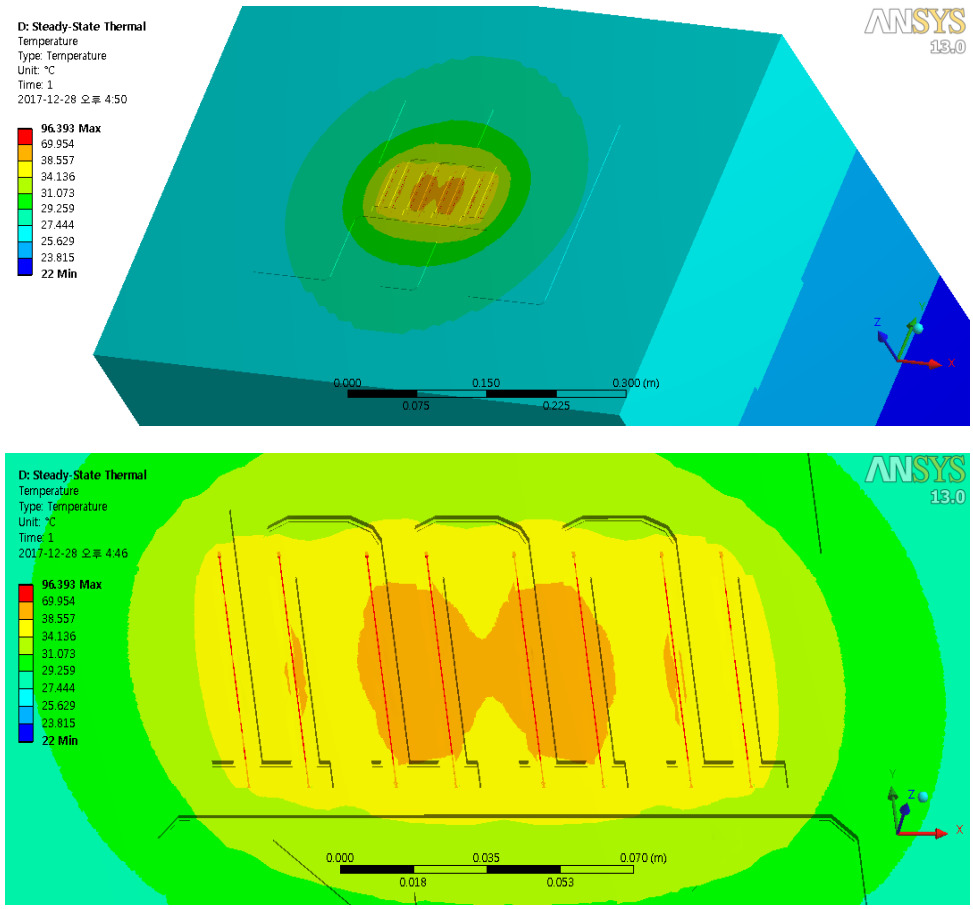


Fig. 5.40 Thermal simulation of 8 × 50 μm device in second stage (output stage) of the fabricated GaN-on-Si MMIC.

However, the long-term stress such as 1000 hours with almost 100 °C would not be suitable for our measurement condition, so that we estimated the power reliability of each MMIC with only 1000 sec stress to distinguish the effects of each fabrication process on their power characteristics focused on trapping effect as possible. First, Fig. 5.41 shows the power degradation of Schottky, SiN_x MIS, and dual MIS MMIC using wafer 1 with input power of 14.5 dBm at 26.5 GHZ. As we expected, the Schottky contact demonstrated substantially stable output characteristics compared with MIS structure. On

the other hand, the MIS MMIC with only SiN_x for gate insulator outperformed dual MIS MMIC like as Schottky contact with saturated degradation. This indicated the SiN_x gate dielectric has lower bulk trap density than HfON. And the PEALD process included in-situ high-density (ICP) N_2 plasma on AlGaN surface that might passivate N-vacancy which could be induced after gate recess etching process, so that better MIS interface condition was achieved [51]. The employment of high-k dielectric on the device structure is better for maximum output power, but harmful at reliability characteristics because of the larger number of trap density even though the better MIS interface quality was considered by employing thin SiN_x interface layer. The drain current density was not changed during time-stress measurement, so we could suppose that the gate leakage current through the gate insulator was not increased. The main reason of the power degradation is hot-electron trapping which causes the decrease of maximum drain current and output load-line. The result of SiN_x MIS MMIC was very meaningful for proceeding the GaN-on-Si RF MIS technology in order to improve the performances of GaN-on-Si devices with comparable reliability characteristic with the conventional Schottky contact.

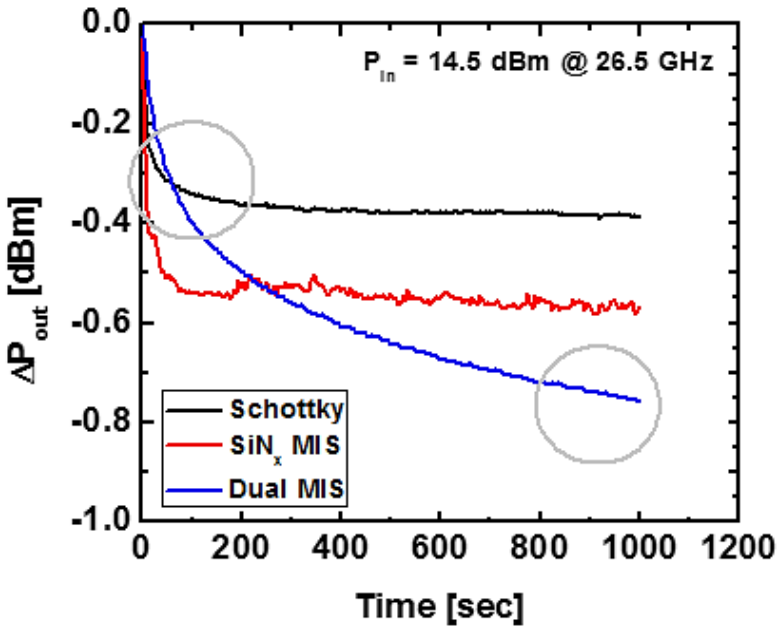


Fig. 5.41 The result of on-state time-stress of fabricated MMICs with Schottky, SiN_x MIS, and Dual MIS, respectively. The applied each DC bias was same as the bias where the maximum output power was achieved.

Figure 5.42 shows another result of reliability characteristic with the comparison of the effect of isolation process on dual MIS MMIC. The device with ion implantation demonstrated the lower off-state current and better current collapse than mesa etching by removing the mesa sidewall. Not only the improvements of instant output characteristic but also long-term reliability was enhanced by removing the additional MIS interface which can cause electron trapping and depletion of 2DEG channel. The finally fabricated dual MIS MMIC demonstrated the highest output power performance with prominent reliability characteristic despite the high-k dielectric was employed as the gate insulator, and further optimizing the thickness of SiN_x interface layer or good backside packaging will be able to present much more stable characteristic.

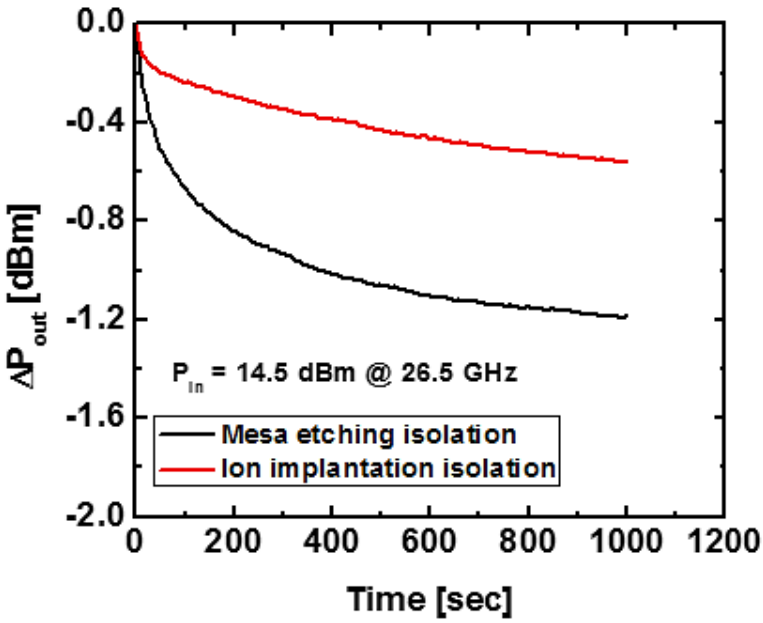


Fig. 5.42 The result of on-state time-stress of fabricated dual MIS MMICs with mesa etching isolation and ion implantation isolation, respectively. The applied each DC bias was same as the bias where the maximum output power was achieved.

5.9 References

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Chapter 6. Conclusions and Future Works

6.1 Conclusions

This work has focused on the process technologies of GaN RF FETs (field-effect transistor) which have the superior properties for the high-frequency and high-power applications. Especially, the characteristics of GaN-on-Si were researched with the fundamental values on cost and compatibility of the semiconductor device. The goal of this work was the fabrication of GaN MMIC PA using the conventional AlGaN/GaN heterostructure on Si substrate applicable on mmw with the comparable characteristics with GaN-on-SiC which is the main area of GaN RF devices.

Initially, we optimized each detail of ohmic contact, device isolation, surface passivation, the gate structure and metal stack to apply at Ka-band PA. The low resistance of ohmic contact was achieved with Si or Ge shallow doping under the Ti/Al-based ohmic metal. The device isolation was performed with two different methods, the mesa etching, and ion implantation. We made an effort to realize the low surface leakage current by etching with low plasma power additionally about 30 nm after the high plasma power was used. Ion implantation process brought the planar structure of the device which was better for RF loss through the buffer and substrate, also the sidewall effect on 2DEG channel could be removed. The passivation process was optimized in terms of parasitic component and reliability related to the

gate structure. The employed gate structure had the minimized length of field-plate to the drain side to satisfy both the low parasitic capacitance and low peak electric field at the gate edge, and the decided thickness of the passivation layer was 60 nm. The gate metal (Ni/Mo/Au) was considered to avoid thermal degradation which has the impacts on electrical characteristics such as the change of Schottky properties and gate resistance during operation with high power or thermal annealing.

Further investigation for the increase of output power of GaN-on-Si device and MMIC PA started with the evaluation of AlGaN/GaN epitaxial layer. We used the wafers with C-doped GaN buffer to compare with un-doped buffer. There were the advantages and disadvantages of the buffer doping as well known, but we decided to use the wafer with un-doped buffer for this work because of poor gate modulation for the wafers with C-doped buffers resulted in the lower gain. The reason why they exhibited such properties was diffusion of carbon into the GaN channel layer, and it was derived from PL and SIMS analysis. To mitigate the electric field at the gate edge, we utilized high-k dielectric for the passivation layer and gate insulator. This approach made possible to have the higher operating voltage and higher maximum drain current when the device and PA were operating by improvement of current collapse and breakdown voltage. The final AlGaN/GaN-on-Si recessed dual MIS-HEMT was successfully fabricated with ion implantation and SiN_x/HfON dual layer as the gate insulator. Also, the MIS structure was realized after the optimization of recess etched depth and curing process for interface damage.

With the development of passive devices for the MMIC, 2-stage common source PA was designed and fabricated on the basis of modeling of each device. The fabricated MMIC consists of the AlGaN/GaN-on-Si recessed dual MIS-HEMT of 4 × 50 μm and 8 × 50 μm. The output power

with the drain voltage of 20 V at 26.5 GHz was 28.97 dBm with PAE of 14.2 %. One process technique to obtain the higher gain of MMIC was applied with Y-gate structure, and the output power of 29.47 dBm with PAE of 16 % was achieved without employing the backside process or packaging for heat dissipation. This result indicated the GaN-on-Si technology can demonstrate a watt-level PA at mmw applications. Indeed, the higher output power could be achieved by designing PA with the larger device at the output stage, and our result was in line with the GaN-on-SiC technology. The suitable thermal packaging might bring much more stable and higher output characteristics of this work.

6.2 Future Works

Because the MIS structure has a lot of issues in terms of reliability with the interface and bulk trap densities, the further investigation on MIS structure is required to achieve more stable long-term characteristics of Schottky-level. A simple study with the change of the thickness of interfacial SiN_x layer for gate insulator can be one approach to reduce the effect of high-k dielectric. The thicker SiN_x layer can screen the electron to transport into the bulk trap in the high-k dielectric. However, the following effect of SiN_x on V_{th} must be also considered at short channel device.

Another factor that induces poor reliability at MIS structure is remained surface damage generated by recess etching process or deposition of gate insulator even though we have cured the damage by post-deposition annealing. Thus, the possible direction of RF MIS HEMT technology is suggested with a thin barrier layer and in-situ passivation process right after the growth of epitaxial layer. The thin barrier layer will be able to realize the high aspect ratio successfully without recess etching, and the thin in-situ passivation layer can be a good interfacial layer before employing high-k dielectric and can prevent surface contamination. Also, there are some considerations when the device is fabricating by this approach such as the higher Al mole fraction of AlGaN barrier layer to maintain the high density of 2DEG channel and the formation of gate structure without gate field-plate.

To conclude, the aim of GaN-on-Si technology is a substitution for GaN-on-SiC with the comparable performance which is the cost-effective way to grow up an area of GaN devices, and our research can advance the possibility of actualization.

초 록

무선 및 위성 통신, 군용 전자 장비에서 전력 증폭기의 중요성이 커지면서 주파수 대역폭의 사용량 증가에 따라 더욱 높은 주파수에서 동작하는 마이크로파 트랜지스터 및 MMIC (monolithic microwave integrated circuits) 기술이 요구되고 있다. 현재 주가 되고 있는 Si, GaAs, InP 등은 물질 한계로 인해 이러한 요구에 맞는 고출력 증폭기를 구현하지 못할 것으로 보고, 높은 밴드갭 특성과 전자 포화 속도 특성을 갖는 GaN 기반의 물질들이 지난 십 수년간 크게 발전해왔다. 특히 GaN-on-Si 기술은 큰 사이즈의 웨이퍼를 저가격에 제작할 수 있어 RF 분야에서 관심을 받고 있다.

본 논문에서는 먼저 오믹 접합, isolation, 패시베이션, 그리고 게이트 등과 같이 GaN 밀리미터파 소자의 전반적인 주요 공정 기술을 소개한다. 패시베이션 공정에서는 게이트 끝의 전기장 분산 효과와 고주파 기생 성분 증가 사이의 최적화를 통해 절연막 두께를 정하게 된다. 또한 기생 캐패시턴스 성분을 최소화 하기 위해 게이트 전계판의 길이는 전기장 분산 효과가 나타나는 범위 내에서 최소화시킨다. 밀리미터파 소자의 게이트 전극 금속층은 Au의 확산을 막기 위해 Ni과 Au 사이에 Mo층을 삽입하여 열적 안정성을 높였다.

본 연구의 최종 목표는 Si 기판 위의 AlGaN/GaN 이종접합구조를 이용하여 위의 전반적인 공정들을 바탕으로 GaN 에피 구조 연구, 고유전율 절연막 적용, 리세스 MIS (metal-insulator-semiconductor) 구조 적용을 통해 Ka-band GaN HEMT 소자와 MMIC 전력 증폭기의 출력 전력을 향상시키는 것이다. 도핑 되지 않은 GaN 버퍼층을 적용한 AlGaN/GaN 이종접합구조가 소신호 특성과 18 GHz 로드풀 측정에서

더 나은 특성을 보였고, 밀리미터파 연구에 적합하다고 판단되었다. 고유전율 절연막을 사용한 MIS 구조는 낮은 게이트 누설 전류와 낮은 전류 감쇄 현상을 동시에 구현할 수 있어 기존의 Schottky 게이트 구조에 비해 높은 출력 전력을 얻을 수 있었다.

NiCr TFR (thin film resistor), MIM (metal-insulator-metal) capacitor, 그리고 CPW (coplanar waveguide) 전송선을 포함한 수동 소자 공정을 최적화 후 능동 소자와 집적화하여 26.5 ~ 27 GHz GaN MMIC 전력 증폭기를 제작하였다. 제안된 최종적인 소자의 공정은 얇은 SiN_x 계면층을 이용한 이중 MIS 구조, 이온 임플란트 isolation 공정, 그리고 낮은 게이트 저항과 기생 캐패시턴스를 가지는 전계판 구조의 Y-게이트 구조가 적용되었고, 기존의 Schottky 게이트 소자와 비교하여 더 높은 동작 전압과 중심 주파수에서도 높은 출력 전력을 나타내었다. 본 연구 결과는 GaN-on-Si 기술이 밀리미터파 대역에서 와트 단위의 출력 전력을 얻을 수 있는 가능성을 앞면 공정의 개선 만을 통해서 보였다. 향후 열 특성 향상을 위한 패키징과 고출력, 고효율을 위한 설계 기술을 접목시킨다면 더욱 우수한 특성의 GaN-on-Si MMIC 전력 증폭기의 구현이 가능할 것이다.

주요어 : AlGaN/GaN HEMTs, GaN 에피층, 게이트 구조, 패시베이션, 고유전율 절연막, 금속-절연막-반도체 (MIS), Ka-band, 출력 전력, 전력 증폭기 (PA), 고주파 단일 집적 회로 (MMIC)
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