M.S. THESIS

Cost-effective Technique for Diagnosing Clock on FPGAs

FPGA 상에서 구현 가능한 경제적인
clock 진단 방법

BY

Seongkwan Lee

FEBRUARY 2018

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

Cost-effective Technique for Diagnosing Clock on FPGAs

FPGA 상에서 구현 가능한 경제적인
clock 진단 방법

지도교수 김 태 환

이 논문을 공학석사 학위논문으로 제출함

2017년 12월

서울대학교 대학원

전기정보공학부

이 성 관

이성관의 공학석사 학위 논문을 인준함

2017년 12월

위 원 장 : 최기영

부위원장 : 김태환

위 원 : 김재하

Abstract

A circuit for on-chip measurement of clock frequency and duty cycle for unknown clock is demonstrated. The circuit consists of variable delay, counter and AND gate, and can be implemented on FPGA that has variable delay element without any external supporting circuit and occupies a very small portion of the FPGA. The major benefit over the previous measurement technology is that statistical analysis of the duty cycle of a large number of continuous clock cycles is possible through a single measurement.

Keyword : Clock, Duty cycle, Frequency, Measurement, Delay, FPGA

Student Number : 2016-20950

Contents

List of Figures

Chapter 1

Introduction

Clock is an essential element that drives the digital circuit. If there is a quality problem in the clock, the digital circuit can make an unpredictable malfunction. Therefore, checking whether the clock is normal is an important task for driving digital circuits.

When the clock generator is manufactured, it is necessary to check the clock frequency, duty cycle, jitter etc. of the device to check whether the manufactured parts are normal. The most reliable way to measure the duty cycle is to use an expensive oscilloscope or spectrum analyzer. However, when a large number of parts are produced in the factory, this method of measurement is not available for cost reason. In such environment, an inexpensive measurement method like the one proposed in the work is more affordable.

In addition, in a device requiring high reliability, there is a case where the quality of the clock is continuously checked not only during production but also during operation. This is especially

important for automotive or medical applications, as malfunctions can result in personal injury. In applications such as motors that use pulse width modulation (PWM) control, it is very important to diagnose the duty cycle because if there is a problem in the duty cycle, mechanical damage or malfunction may occur.

In this paper, we propose a new method for measuring clock frequency and duty cycle using a simple circuit. In addition, we describe the difference between the proposed method and the existing method, and show the behavior and measurement performance in various cases by implementing the presented method on the FPGA. Note that the proposed circuit is made of very small amount of hardware resources, so it can be implemented as a small part of the ASIC or even inside the FPGA. Further, since FPGAs are suitable for small-scale production because of low initial development cost and development time, our proposed circuit that can be installed with a small amount of resource on FPGA will be very useful in practice.

Chapter 2

Previous Research

2.1 Measuring clock frequency

The easiest way to measure the frequency of an unknown clock using an FPGA is to use two counters (e.g., [1,2]); first, operating one counter with a reference clock, whose frequency has been known for a certain period of time, subsequently operating the other counter with a clock, the frequency of which we want to know. The frequency of the unknown clock will then be measured by comparing the two counter values. This method has a merit that the implementation is quite simple, but the accuracy is satisfactory only if the reference counter is operated in a sufficiently long period of time.

On the other hand, the method presented in this paper has no significant correlation between accuracy and measurement time. Therefore, when the measurement time is short, the accuracy is higher than the conventional method.

2.2 Measuring duty cycle

There are many existing methods for measuring duty cycle that can be implemented in ASIC or PCB. However, only a few are implemented on FPGA without external supporting circuits. One of those methods is that in [3]. It requires variable delay components and flip-flops in FPGA. Its strength is that it can measure the duty cycle very quickly by capturing waveform of entire clock period at once. However, this method requires too many variable delays. Since generating the variable delay in FPGA needs a costly resource, a high cost is required for implementing the method on FPGA. On the contrary, the work in [4] saves the implementation cost by performing a large number of iterations for duty cycle measurement. But in return, the method of [4] requires long measurement time. In addition, all of the above methods can measure only one duty cycle at a time.

In this work, we overcome the prior works in [3,4] in that we make use of statistical analysis of duty cycle on a large number of continuous clock cycles under a single measurement. Our method does not miss few 30% duty cycle pulses between many 40% duty cycle pulses. In addition, the proposed method can be implemented using low cost resources compared to the work in [3].

Chapter 3

The Proposed Measurement Method

Figure 1 is a simplified block diagram of the duty cycle measurement circuit.

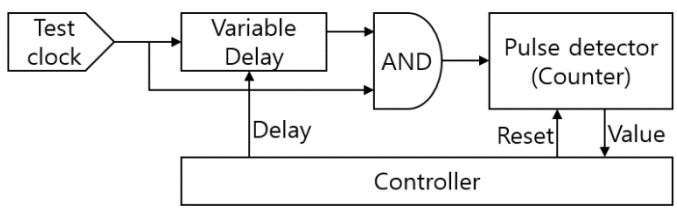

Figure 1 Block diagram of proposed circuit

In Figure 1, test clock is a clock where we want to know its frequency and duty cycle. This clock signal is split into two branches, one flowing to the variable delay element while the other flowing to the AND gate directly. The user can adjust the delay value to change the phase difference between the two clock signals inputs to the AND gate. The pulse width and the number of pulses

of the AND gate output vary depending on the duty cycle and phase difference of the two clock signals that are the AND gate inputs. The output clock synthesized at the AND gate is detected by a pulse detector. By analyzing the disappearance of the pulse according to the phase difference, the clock frequency and duty cycle can be measured. The measurement method for various cases is as follows.

3.1 Measuring clock frequency

Clock frequency can be measured by the following method.

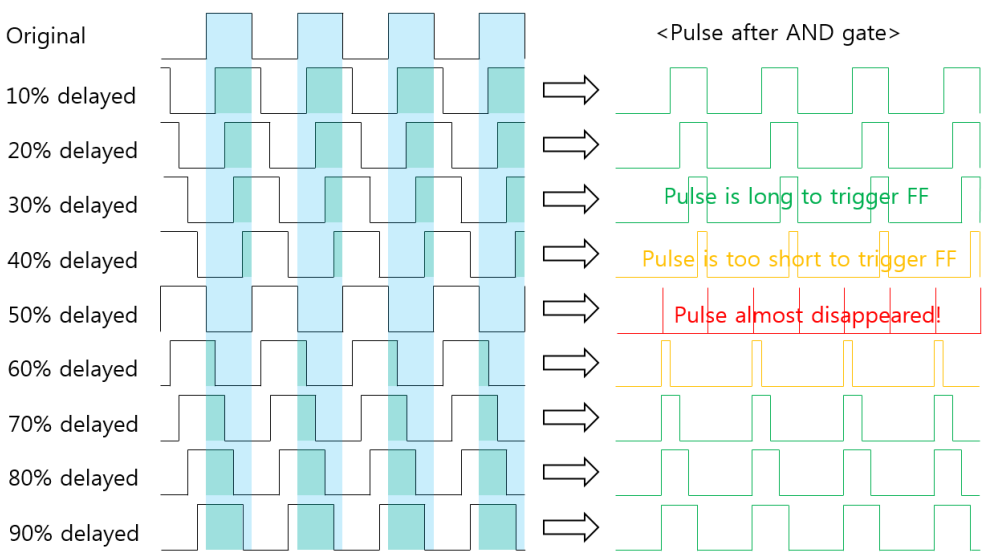

Figure 2 AND gate input output waveform according to delay.

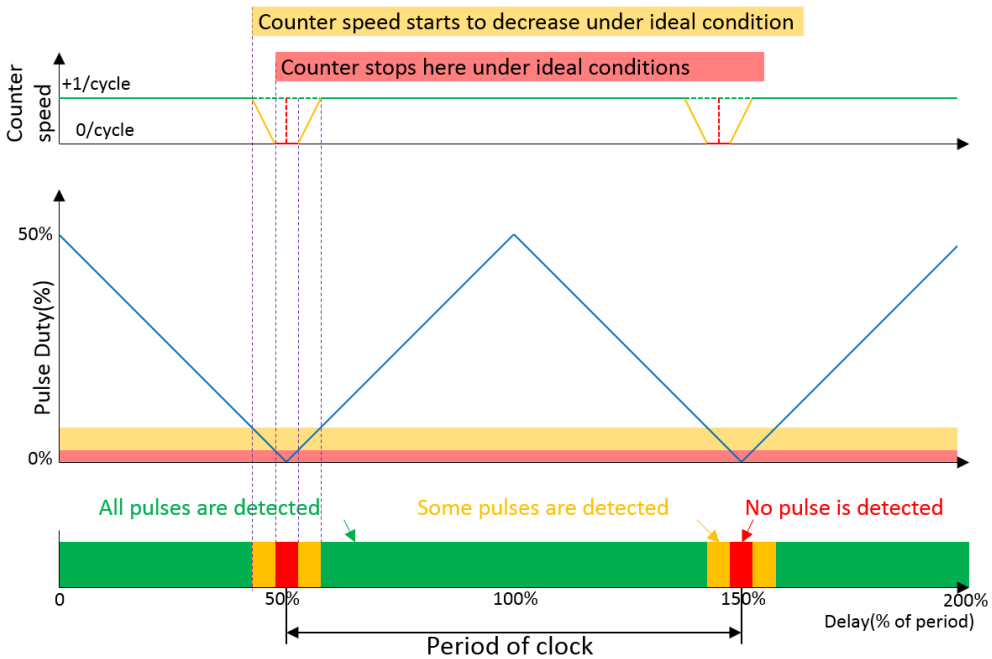

Figure 3 Changes of the width of input pulse to the counter and pulse counting speed of the counter as the delay adjustment value increases.

The left and right waveforms in Figure 2 show the AND gate input waveforms and the output waveform, respectively when an ideal clock with no jitter of 50% duty cycle passes through the measurement circuit while incrementally increasing the delay with a step of 10% of the original signal period.

As the delay difference between the original signal and the delayed signal increases, the pulse width of the AND gate output signal gradually decreases. When the delay difference becomes 50% of the period, the pulse width is theoretically zero. If the delay continues to increase, the pulse width increases again until it

reaches 100%. When the delay increase becomes 100%, the AND gate output signal becomes the same signal as the original signal. If the delay increase exceeds 100%, the pulse width becomes smaller as it starts from 0% again. If it reaches 150%, the pulse width becomes 0 again. By analyzing this behavior, it is possible to know the period of the test clock by calculating the time difference between 50% delayed and 150% delayed points where the pulse width becomes 0.

Precisely when the variable delay is equal to equation 1, the pulse should disappear under ideal condition where there is no jitter in both the test clock and the measurement circuit, and the counter can respond to an extremely short pulse.

$$(\mathrm{N} + 0.5) \times period \;\; N = 0,1,2,\cdots \qquad (1)$$

However, in real circuits, the test clock has a certain level of jitter even when it is normal, and another jitter is added through the measurement circuit. Moreover, we should consider that the counter may not detect the pulse if the pulse width is too narrow. Reflecting this phenomenon, the changes of the width of the counter input pulse and the counting rate (i.e., counting speed) of the counter with respect to the changes of delay adjustment value can be represented graphically as shown in Figure 3.

As Figure 3 illustrates, when the proposed circuit is implemented and tested on an ideal environment, the counter will

stop only when the delay is exactly 50% of clock period. This is indicated by a dotted line of counter speed graph in Figure 3.

On the other hand, under real environment, as the delay increases to a value satisfying the condition of equation 1, the pulse width gradually decreases, and the counter misses some pulses from a certain point. Therefore, pulse counting speed starts to decrease. Those points are indicated in Figure 3 with yellow bars. The points in yellow bars are caused by jitter of measurement system. Thus, if there are more jitters, the yellow bars will appear thicker. Also, when the delay becomes close to the condition of equation 1, all the pulse widths fall below the detectable value, and even if the delay is increased, the counter appears to stop counting continuously. In other words, pulse counting speed is 0 at those points. It is indicated in Figure 3 with red bars.

3.2 Measuring duty cycle

The duty cycle can be measured in the same way as the frequency measurement. By measuring the phase difference at the point where the AND gate output pulse disappears by increasing the variable delay, the duty cycle of the test clock can be known. For example, if the duty cycle is 50%, the AND gate output clock disappears only when the phase difference between the clock passing through the delay and the clock not passing through

becomes 50% as shown in Figure 4. Therefore, the duty cycle becomes the value obtained by dividing the delay difference between two clocks at the time when the output pulse of the AND gate disappears by the clock period though equation 2.

$$\frac{delay\ difference\ at\ pulse\ stop}{\text{period}} \times 100 \quad (2)$$

In addition, the duty cycle can be obtained through the following equation 3 even though the delay difference between the clock passing the delay and the clock not passing the delay is unknown, but the length of the interval in which the AND gate output pulse disappears. This method is useful when the absolute delay difference of the two input signals of the AND gate is not known due to the parasitic propagation delay present in the measurement circuit.

$$\frac{\text{period}-\text{pulseless section}}{2 \times \text{period}} \times 100 \quad (3)$$

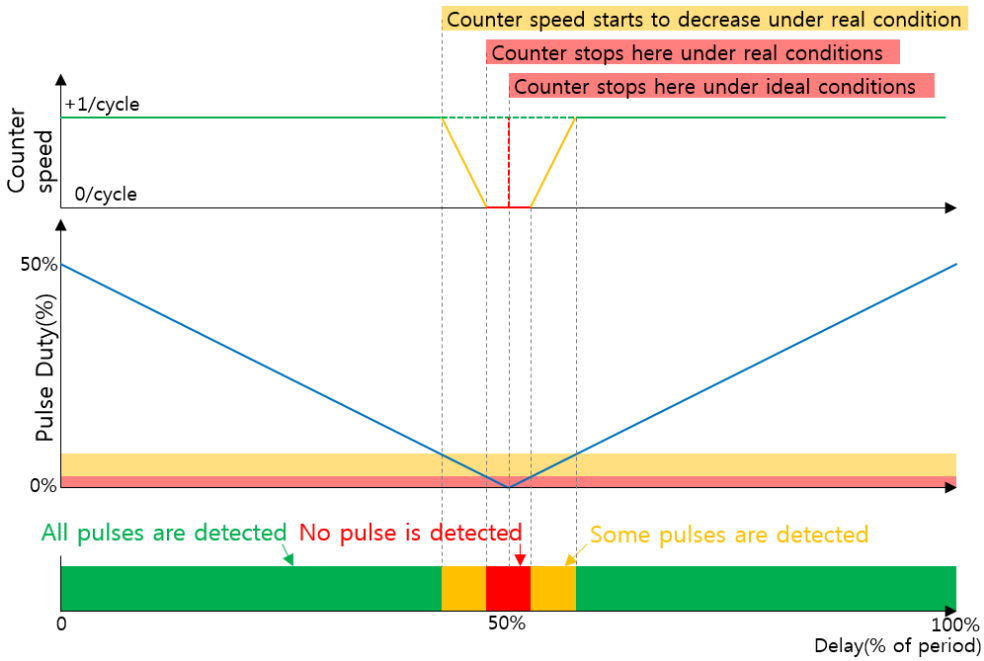

Figure 4 Changes of the width of input pulse to the counter and pulse counting speed of the counter as the delay adjustment value increases.

3.2.1 Measuring when duty cycle is less than 50%

For the sake of understanding, the measurement case where the duty cycle is 50% or less is analyzed as follows. For example, if the duty cycle is 40% and the variable delay is increased from 10% to 90% of the period of the test clock, the AND gate input and output signals are shown in Figure 5.

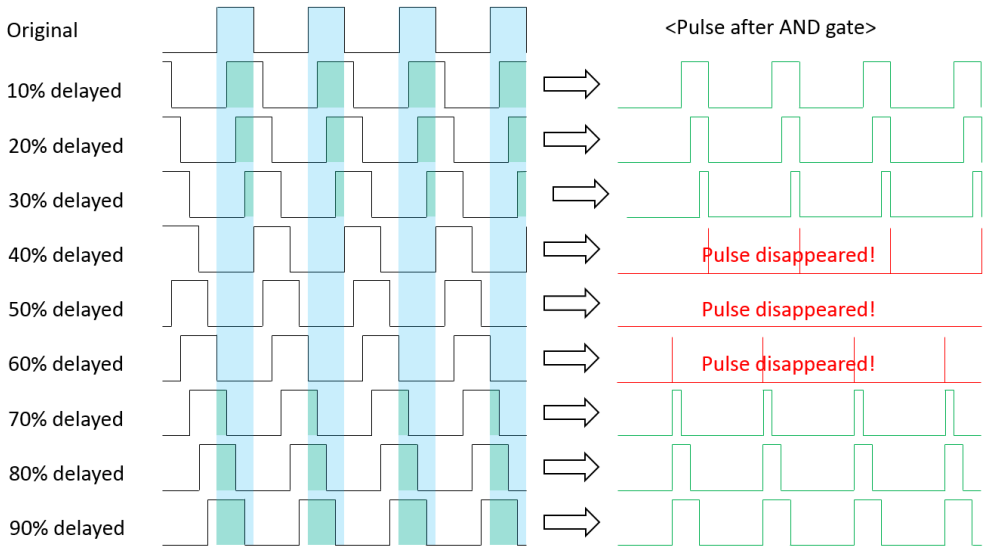

Figure 5 AND gate input output waveforms according to delay for 40% duty cycle ideal clock.

Compared to the case when the duty cycle is 50%, it can be seen that when the duty cycle is 40%, the output pulse disappears earlier (when the delay is 40% of the period). In addition, the point at which the pulse appears again is when the delay is 60% of the period. Using this phenomenon, the duty cycle of the test clock can be determined by measuring the time difference of the intervals where the pulse disappears. This phenomenon can be expressed as a graph of the pulse width and the counter increase rate according to the delay, as shown in Figure 6.

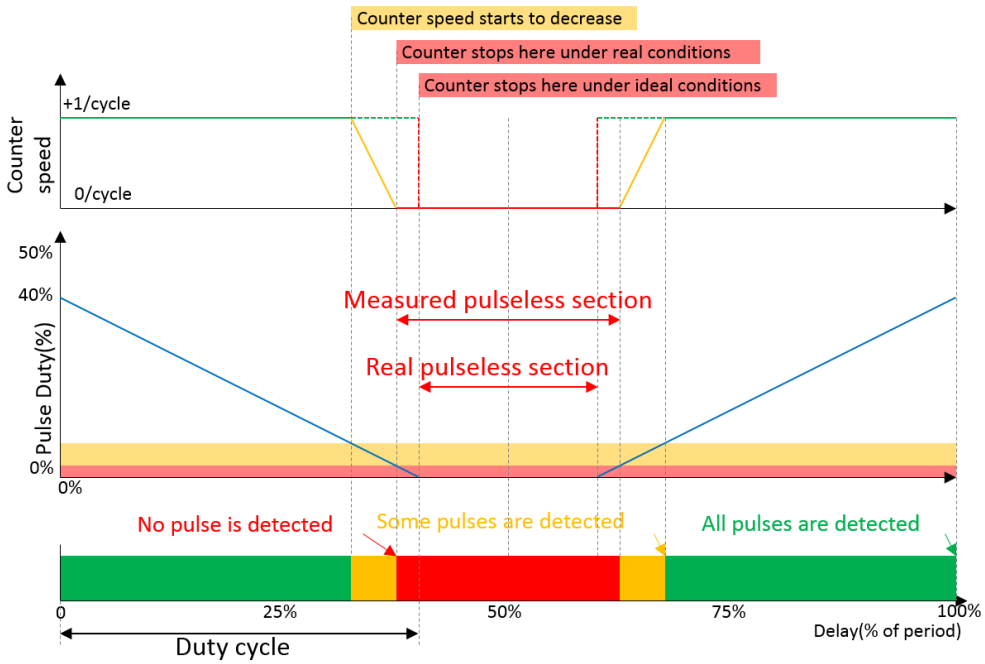

Figure 6 Changes of the width of input pulse to the counter and pulse counting speed of the counter as the delay adjustment value increases.

The duty cycle of the test clock can be calculated as equation 3 using the length of the real pulseless section shown in the Figure 6 and the period of the test clock that is known and measured in advance[1,2].

3.2.2 Measuring when duty cycle is over 50%

When the duty cycle is more than 50%, the measurement method is slightly different.

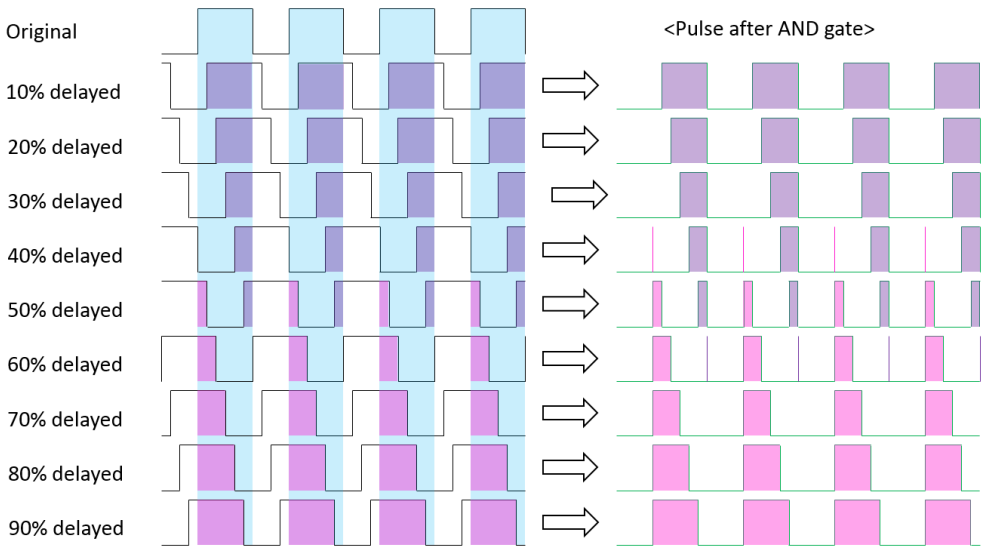

Figure 7 AND gate input output waveforms according to delay for 60% duty cycle ideal clock.

For example, if the duty cycle is 60% and the variable delay is increased from 10% to 90% of the period of the test clock, the AND gate input output signals are shown in Figure 7. If the delay increases, the AND gate output pulse width becomes smaller (purple pulses), similar to the 40% duty cycle case. However, unlike the case of 40%, when the delay exceeds 40% of the period, the new pulse is added to the existing pulse in one cycle (pink pulses). As the delay increases, the new pink pulse width becomes larger. The conventional purple pulses will disappear when the delay reaches 60% and both pulses will appear in one cycle at delays between 40% and 60%.

Therefore, the duty cycle is the phase difference at the point when the output pulse of the AND gate increases to 2 per cycle and

returns to 1. The pulse width change and the counter speed change are graphically shown in Figure 8 and the duty cycle of the test clock can be calculated by Equation 4.

$$\frac{\text{period+multi pulse section}}{2 \times \text{period}} \times 100 \quad (4)$$

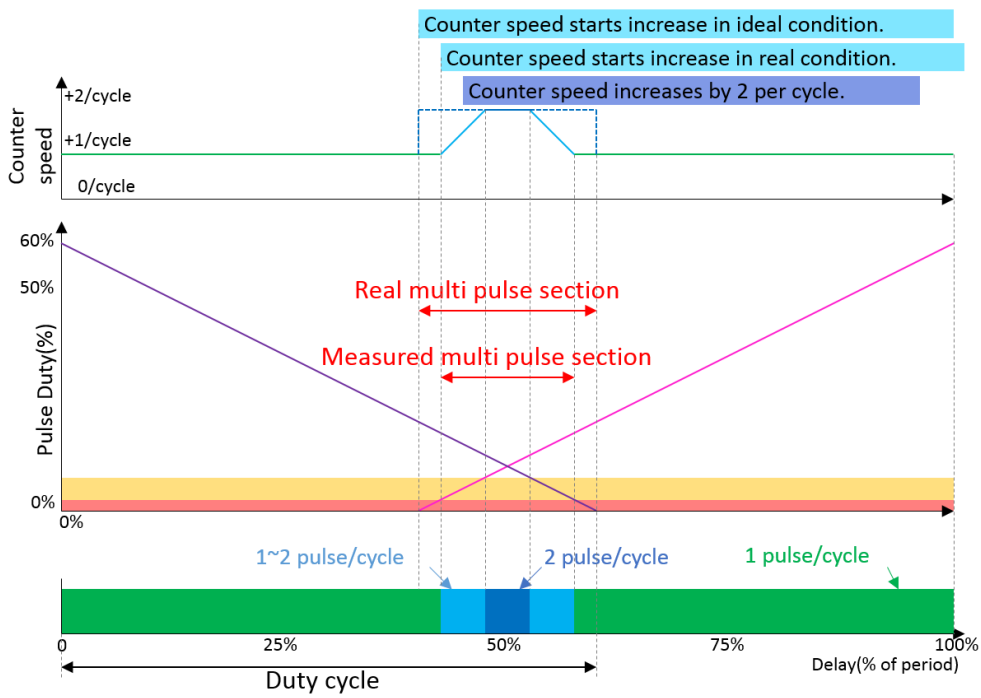

Figure 8 Changes of the width of input pulse to the counter and pulse counting speed of the counter as the delay adjustment value increases.

3.2.3 Measuring when duty cycle is fluctuating

If the PLL fails, the duty cycle may fluctuate. For example, if the duty cycle of any abnormal clock alternates between 40% and 50%, the measurement results are as follows.

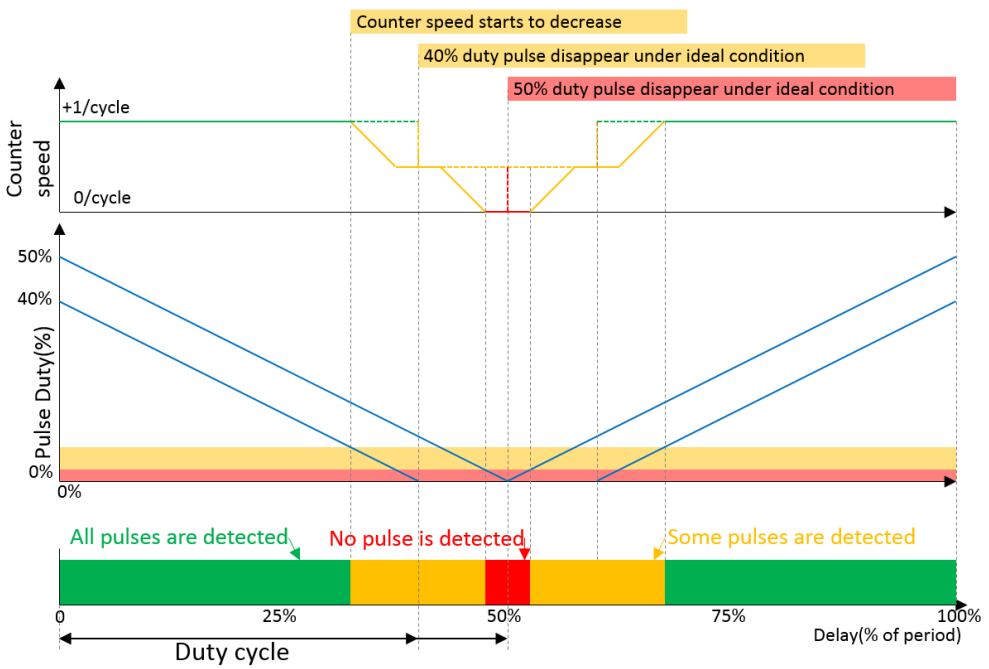

Figure 9 Changes of the width of input pulse to the counter and pulse counting speed of the counter as the delay adjustment value increases.

The result shown above indicates that 40% duty cycle pulse disappears and counter speed is reduced by half, which means 40% duty cycle clock takes up half of the clock. Since the 50% duty

cycle pulse has disappeared, the counter speed has decreased to zero, which means only the remaining half of the clock is 50% duty cycle. That is, the distribution of the clock pulse for each duty cycle can be known through the variation of the counter speed of each delay.

Chapter 4

Experiment result

The proposed circuit was implemented on a VC707 board, which is a reference board for Xilinx Virtex7 FPGAs. The variable delay we used is the IDELAY IP embedded in the FPGA. It has a resolution of about 39ps and delay range from 0 to 1.2ns. For a single IDELAY, the delay variable range is too small. Thus, to be applicable in real applications, four IDELAYs are connected in series and the delay can be varied in the range of 4.8ns. The pulse detector is implemented with an 8-bit counter and counts the number of pulses in the AND gate output for a fixed time to calculate counting speed.

The measurement was performed by sequentially increasing the variable delay from 0 to 4.8ns and counting the number of input pulses to the counter for a fixed time at each of delay values. The final counter value for each delay value is read through the ILA (Integrated Logic Analyzer) and divided by the final counter value

when the pulse width is wide enough to know the counter increment speed at the delay. The delay value signals and counter control signals are generated by controller logic. The final implementation block diagram in the FPGA is shown in Figure 10.

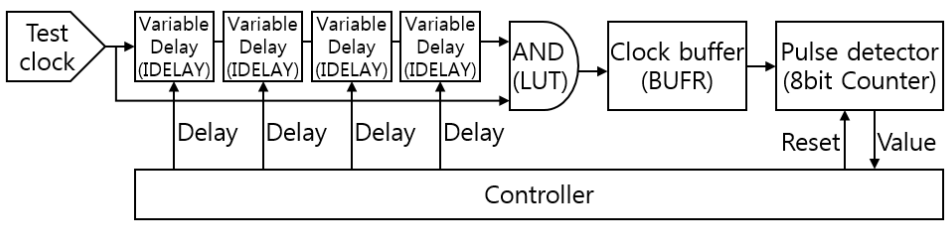

Figure 10 Block diagram of our implemented design on FPGA.

4.1 Measuring clock frequency

As a result of measuring the counter increment rate at every applied value of (increasing) delays, the graphical result shown in Figure 11 is confirmed. In the experiments, period of 2.5ns clock is used to be measured. When the width of the pulse input to the counter is wide enough, the final value of the counter is stayed at 124, which means at that point the counter speed is +1 per pulse. And, as shown in Figure 11 there are two stops of counting at a certain delay during the measurement interval.

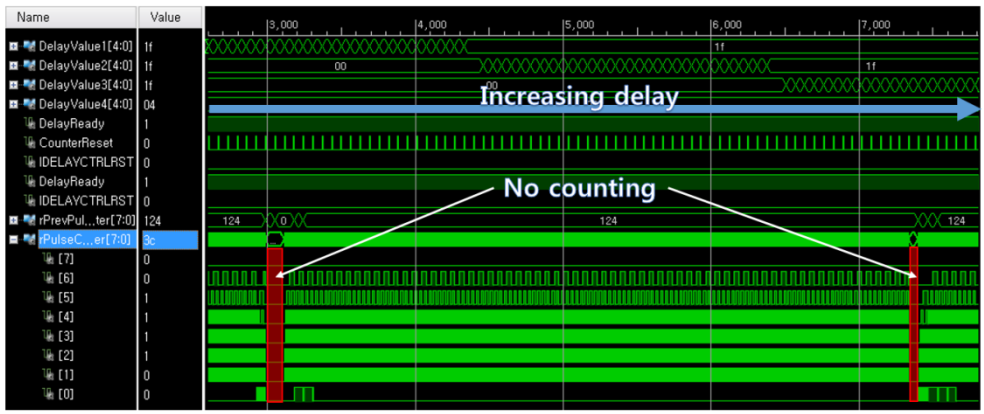

Figure 11 The operation behavior of the counter (lower part) as the delay value increases (upper part).

The change of the counting speed with respect to the delay value is shown in Figure 12.

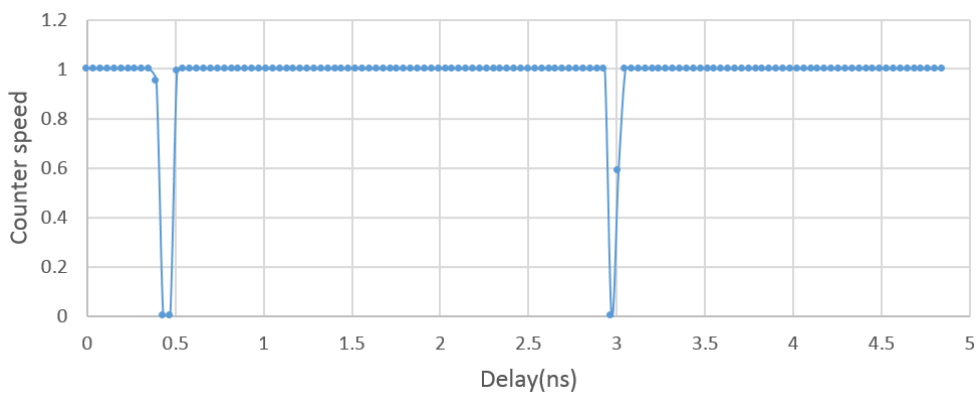

Figure 12 Changes of pulse counting speed as the delay value changes. The interval between the two sharp points is used as the measurement of the clock period of the test clock.

By analyzing the counting speed and calculating the period using the time difference of the two points where the counting stops, it is confirmed that it has a cycle of about 2.58ns. The actual period of the original signal is 2.50ns. Therefore, the measurement result has an error of 80ps.

Additional experiments were performed by changing the test clock period from 400MHz to 440MHz with a step of 10MHz. The results are summarized in Figure 13. It shows that the average error of the measurement is 70ps.

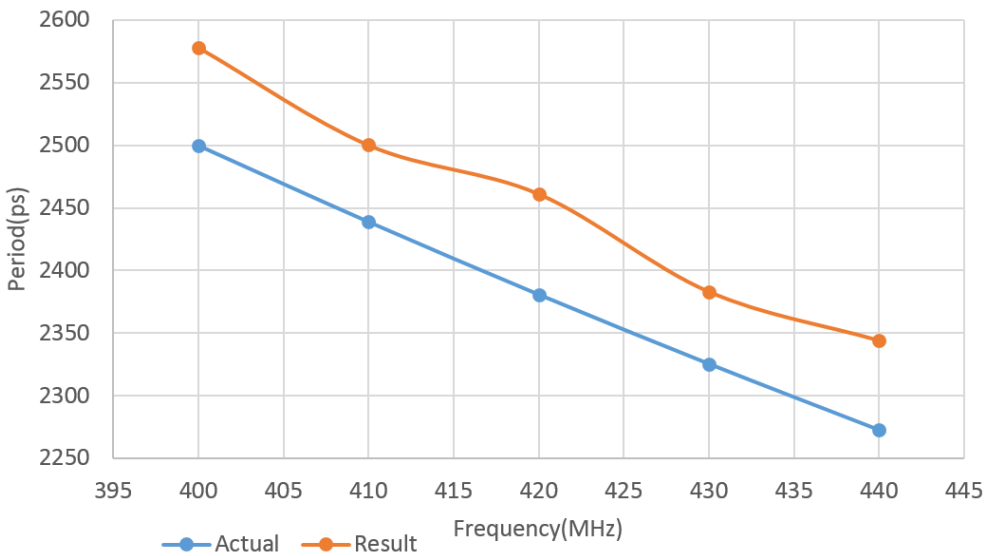

Figure 13 Comparison of actual clock period and measured clock period obtained by applying our proposed circuit to test clocks of range in between 400MHZ ~ 440MHz.

4.2 Measuring duty cycle

Using the PLL of FPGA, we generated a 400MHz test clock with 33.3% duty cycle, and then measured the duty cycle using the implemented circuit. As a result, we could observe the interval where the counter stopped, as illustrated in Figure 14.

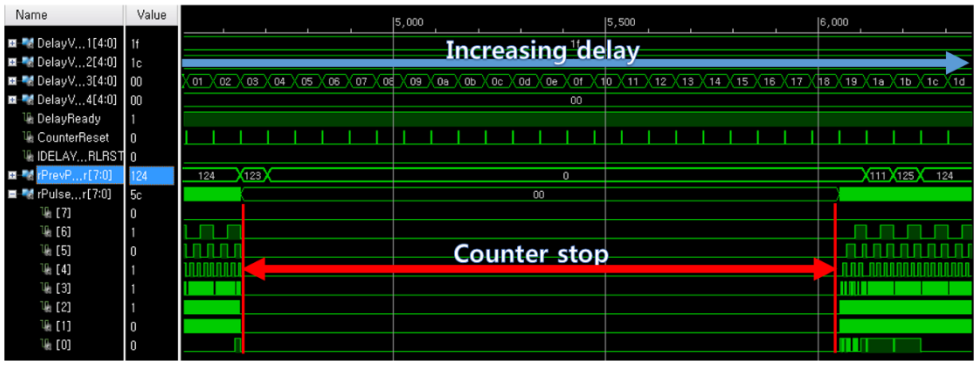

Figure 14 The operation behavior of the counter (lower part) as the delay value increases (upper part).

Using the above experimental results, we can plot the change of counter speed according to the delay as Figure 15.

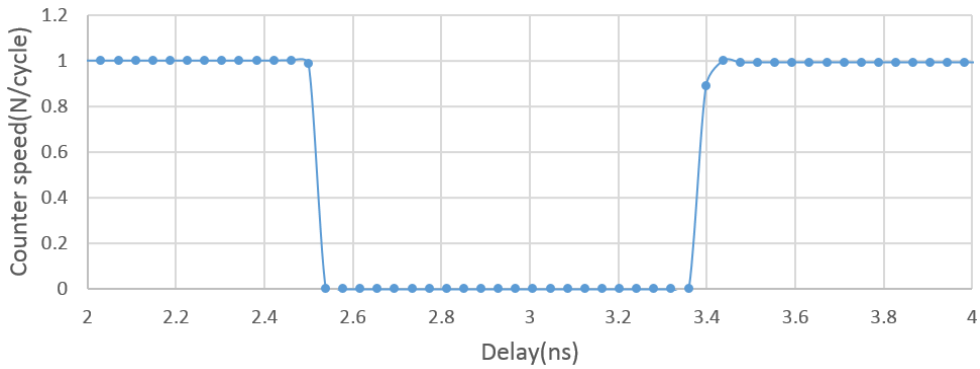

Figure 15 . Changes of pulse counting speed as the delay value changes.

The measured pulseless section is longer than the actual pulseless section because the counter used in the pulse detector does not operate when the pulse width is very small. Therefore, in order to compensate for this error, we used a 50% duty cycle clock, which theoretically should have a pulseless section length of 0, to check how the pulseless section is actually measured to compensate for measurement errors due to counter sensitivity. If we calculate the duty cycle by equation 2 with the above result, it is 33.2%.

When the test clock of 400MHz 66.7% duty cycle was generated using PLL, the following results were also obtained.

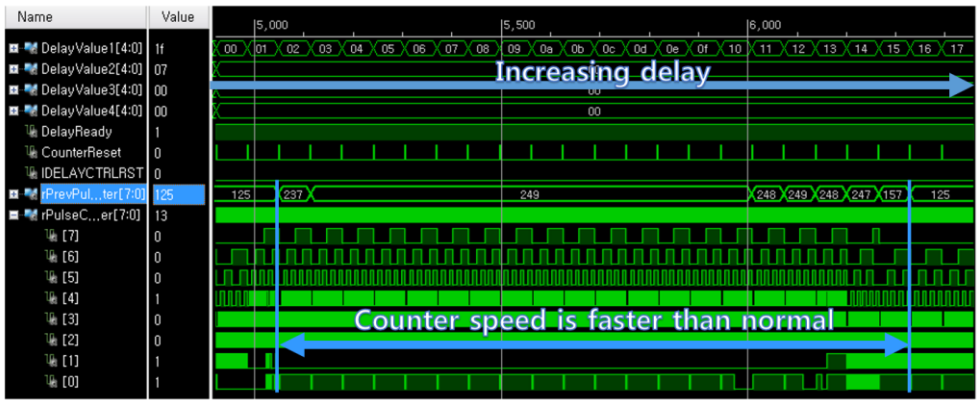

Figure 16 The operation behavior of the counter (lower part) as the delay value increases (upper part).

As shown in Figure 16, when the pulse width is sufficient, the final counter value at each delay condition is 125. However, as expected, the final value of the counter exceeds 125 in some delay values. For the counter value being converted to counter speed, the resulting graph is shown in Figure 17. If the duty cycle is obtained by substituting equation 3 for the length of the section with a counter speed greater than 1, it will be 66.0%.

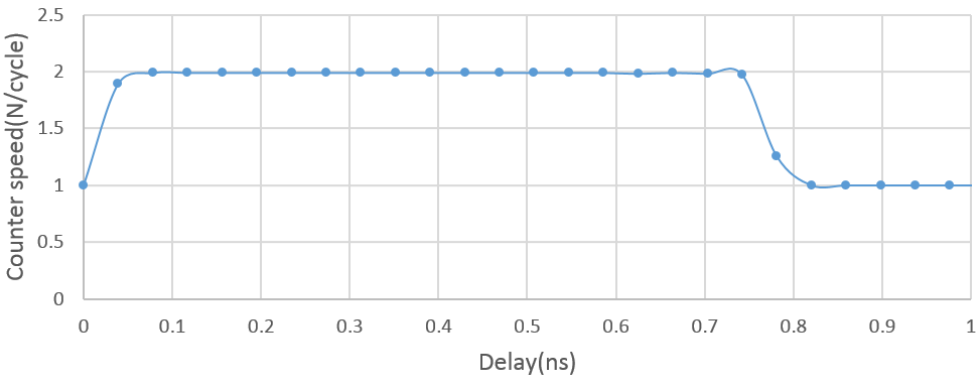

Figure 17 Changes of pulse counting speed as the delay value changes.

Chapter 5

Conclusion

Experimental results show that the proposed circuit has enough performance to measure the frequency and duty cycle of the clock in the FPGA. Therefore, this circuit can be used as a cost effective solution that can measure frequency and duty cycle in ATE (Automatic test equipment) or diagnose clock in high reliability devices. It should be mentioned that the conventional counter based frequency measurement method and our variable delay based measurement method presented in the work both have advantages and disadvantages. The conventional counter based method is applicable to wide range of measurable frequency. It is possible to measure the clock of any frequency that can operate the counter. Furthermore, the measurement accuracy is enhanced at the expense of spending more measurement time.

On the other hand, our variable delay based measurement method is limited in accuracy due to the physical resolution of the

delay element[5]. That means there is no clear way to improve the accuracy unless the delay element is improved. However, fortunately, as the FPGA technology develops, the resolution is improved continuously. The Virtex7 FPGA used in the experiment has a delay IP of resolution of 39ps, but recent UltraScale FPGAs have improved performance up to 2.5ps. Consequently, future studies using the latest FPGAs may provide better performance than the current results.

In addition, the conventional methods are not easy to perform parallel measurement to save the measurement time. However, our variable delay based method is able to measure the frequency and duty cycle in a very short time by using multiple delay elements in parallel, as illustrated in Figure 18. If N measurement circuits are used in parallel, the measurement time is reduced to 1 / N. Besides, this method can simultaneously measure frequency and duty cycle, which further shortens measurement time.

The last but might be more valuable advantage of our variable delay based method is that the analysis of the operation of the pulse detector counter can diagnose the quality (e.g., jitter, variation of duty cycle) of the clock to test. If a future research is performed on this direction and solidifies the usefulness, our variable delay based measurement can be used as a cost-effective solution that can effectively measure the clock quality beyond the measurement of clock frequency and duty cycle.

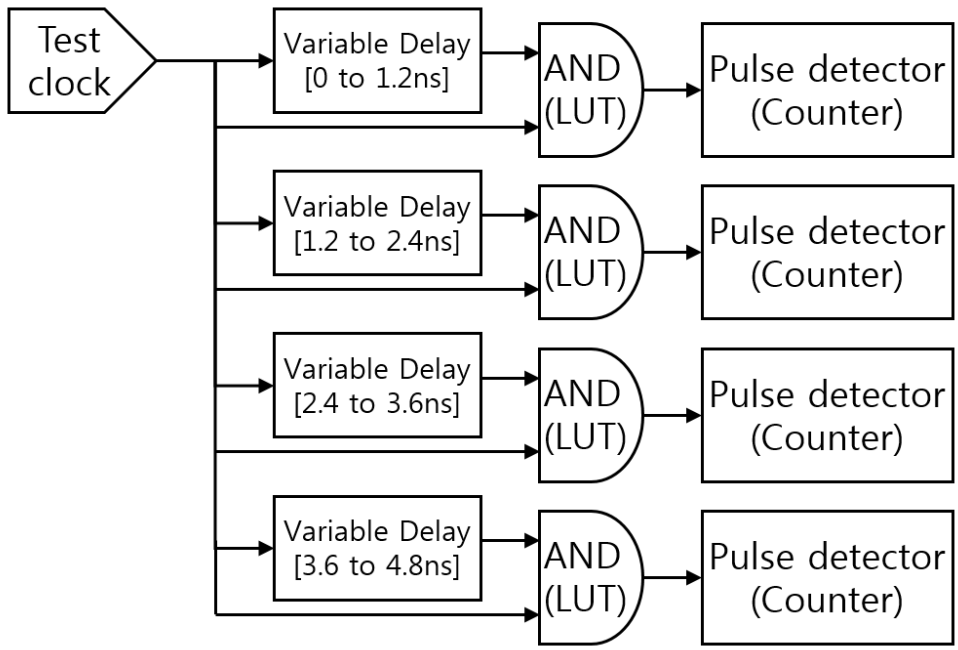

Figure 18 Parallel configuration of our variable delay based circuit to speed up the measurement.

Bibliography

[1] R. Tekumalla and P. Krishnamoorthy, “On-chip clock testing and frequency measurement”, IEEE North Atlantic Test Workshop, pp. 11-14, 2014.

[2] M. A. Syahbana, D. J. H. D. Santjojo, and S. P. Sakti, “High-resolution multiple channel frequency counter using spartan-3E FPGA”, IEEE International Seminar on Sensors, Instrumentation, Measurement and Metrology, pp. 111-114, 2016.

[3] R. Parker, “Duty cycle measurement circuit”, U.S. patent US20070075753 A1, issued April 5, 2007.

[4] A. Ramesh and T. Wari, “System and method for on-chip duty cycle measurement”, U.S. patent US20100019757 A1, issued Janurary 28, 2010.

[5] J. Li, Z. Zheng, M. Liu, and S. Wu, “Large dynamic range accurate digitally programmable delay line with 250ps resolution”, IEEE International Conference on Signal Processing, 2006.

국문초록

본 논문은 미상의 클럭에 대한 클록 주파수 및 듀티 사이클의 온칩 측정을 위한 회로를 제시합니다. 이 회로는 가변 신호 지연 소자, 카운터 및 AND 게이트로 구성되며 외부 지원 회로를 필요로 하지 않고 가변 지연 소자가 있는 모든 FPGA에서 구현 될 수 있으며 FPGA의 에서 매우 작은 자원을 차지합니다. 이전 측정 기술에 비해 큰 이점은 단일 측정을 통해 많은 연속 클럭 사이클의 듀티 사이클에 대한 통계 분석이 가능하다는 것입니다.

주요어 : 클록, 듀티 사이클, 주파수, 측정, 지연, FPGA
학번 : 2016-20950