PH.D. DISSERTATION

DESIGN AND IMPLEMENTATION OF SENSOR READOUT CIRCUITRY FOR AUTOMOTIVE ELECTRONIC SYSTEMS

차량용 전장 시스템을 위한 센서 판독 회로의 설계 및 구현

BY

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DEPARTMENT OF INTELLIGENT SYSTEMS
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2018년 8월

서울대학교 융합과학기술대학원

지능형 융합시스템 학과

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ABSTRACT

DESIGN AND IMPLEMENTATION OF SENSOR READOUT CIRCUITRY FOR AUTOMOTIVE ELECTRONIC SYSTEMS

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With the recent advances in IT technology, the demand for safe driving, convenience, economic efficiency and eco-friendliness has increased, and thus the importance of automotive electronic system has increased. The automotive electronic system uses various sensors to acquire kinds of information related to driving, in which a sensor readout circuitry is a core component.

This dissertation presents two types of sensor readout circuitries; a thermal infrared sensor readout circuitry based on an uncooled microbolometer for automotive night vision systems and a high-voltage input sensor readout circuitry based on an 8-bit embedded flash microcontroller for automotive control systems.

To readout the infrared thermal sensors, an uncooled microbolometer infrared imager is presented. The nonuniformity of the microbolometer makes such imaging systems heavily reliant on complicated calibration techniques, incurring an overhead

which is particularly significant in low-cost, compact devices. To solve the overhead, this dissertation proposes a shutter-based successive-approximation calibration loop, which avoids the need to implement correction tables in software on an external processor. Prototype imager, consisting of an 80 × 82 pixel infrared focal-plane array and readout circuitry, has been implemented, and the experimental results confirm that our on-chip autocalibration approach compensates effectively for fixed pattern noise caused by the nonuniformity of the microbolometers.

To readout the sensors with a high-voltage output, a high-voltage input interface is presented. The input interface for automotive control units requires external passive components to protect an internal logic from battery overvoltage reaching through the sensor and to adjust to signals less than 5V required by a logic process, which increases cost and size on a printed circuit board. To solve this problem, this dissertation proposes a 32-channel 12V input interface to capture battery-level inputs without external components. A 1Mbps CAN transceiver and an 8-bit embedded flash microcontroller were also integrated together, increasing cost savings. A prototype, fabricated in 0.18μm BCDMOS technology with 52V breakdown, operates reliably between -40°C and 150°C.

Keywords: Automotive, electronic system, sensor readout circuitry, infrared image, input interface.

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CHAPTER 1

INTRODUCTION

1.1 AUTOMOTIVE ELECTRONIC SYSTEMS

1.1.1 GROWTH OF ELECTRONIC DEVICES AND SYSTEMS FOR VEHICLES

Historically, automotive electronic systems have been confined to the use of the communication of AM radio and police car two-way radio system. In the 1930s and 1940s, these were important electronics, and in those days the vacuum tube was the only electronic device. The development of transistors in the late 1940s promoted the development of semiconductor electronic devices based on integrated circuits. This has provided a technology compatible with the introduction of advanced automotive electronic systems such as ignition systems. The advent of electronic fuel control systems in the 1970s made it obvious that the use of automotive electronic devices in road vehicles.

Nowadays, the demand for safe driving, convenience, economic efficiency and eco-friendliness has rapidly increased with the recent advances in IT technology, and thus the

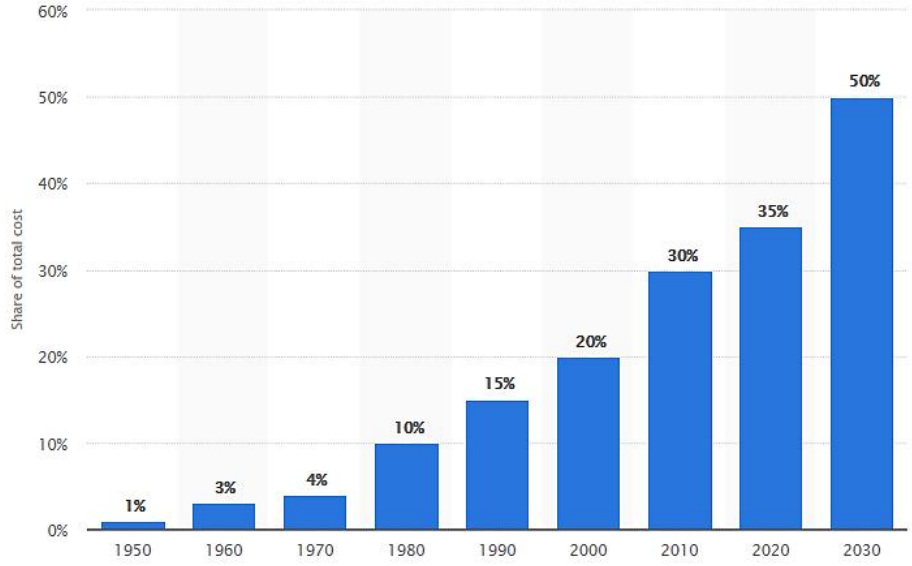


Fig. 1.1 Automotive electronics cost as a percentage of total car cost worldwide from 1950 to 2030 [1.1].

importance of automotive electronic system has increased more than ever before. Fig. 1.1 shows automotive electronics cost as a share of total car cost from 1950 to 2030. In 2010, the electronics content in cars accounted for 30 percent of an automobile's total production cost.

1.1.2 AUTOMOTIVE APPLICATIONS

In general, the automotive electronic system is classified into several functional areas as a function classification in a vehicle. For example, there are a body, connectivity, safety, infotainment, and powertrain, as shown in Fig. 1.2. Body refers to basic body controls such as door access, lighting, and windows. Connectivity consists of telematics

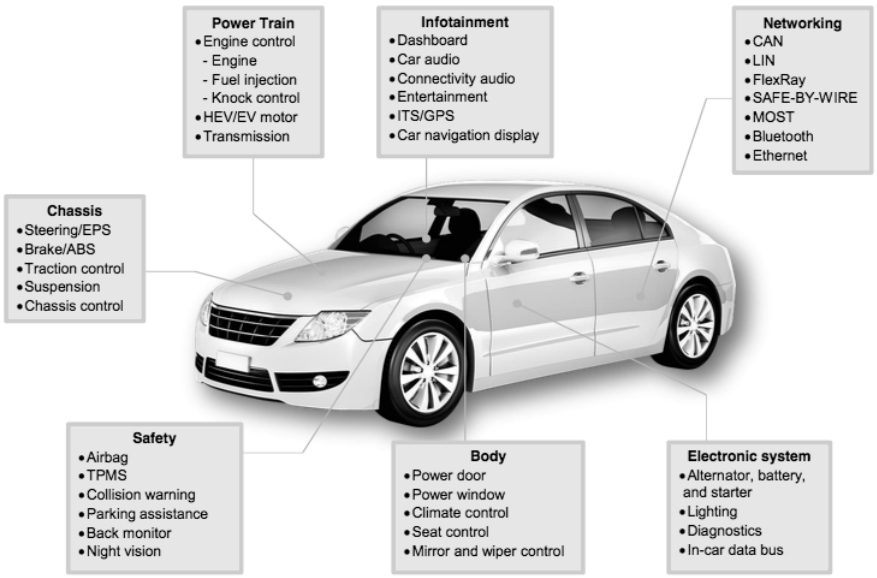


Fig. 1.2 Functional classification in a vehicle.

and wireless communications such as cellular and WiFi. Safety includes imaging systems such as night vision and rearview cameras, and LiDAR and radar for distance detection. Infotainment includes driver information and entertainment. The powertrain area includes engine controls and transmissions. There is also a chassis, such as brakes and steering, that can be included in the powertrain.

The various functional applications can be abstracted into the following system applications: control, measurement, and communication [1.2]. Figure 1.3 illustrates system applications with various sensors, in which a night vision system belongs to the measurement application and the electronic control unit (ECU) is a key block of the control system.

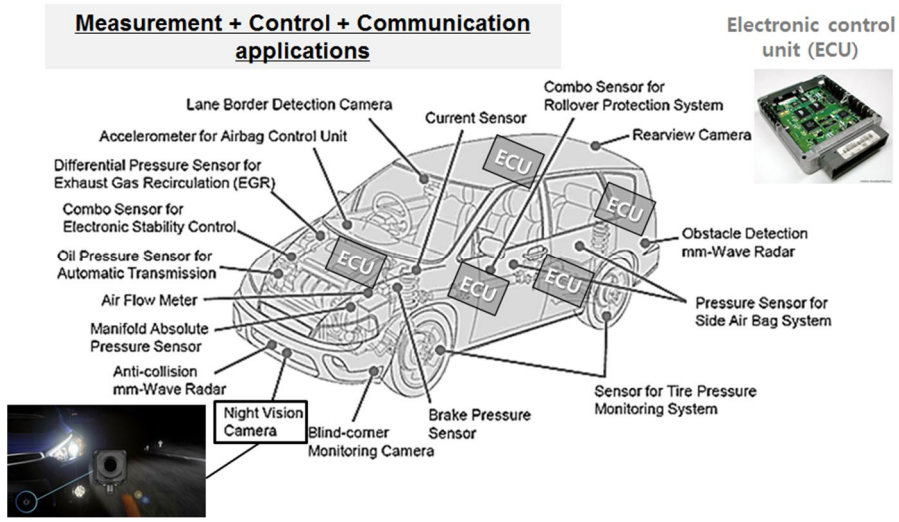


Fig. 1.3 System applications with various sensors.

The night vision system has sensors in the form of a two-dimensional array for output to an image. Calibration is necessary to improve the unevenness and image characteristics between the sensors. All of these are integrated with a sensor-specific readout IC and have a module form.

The control application has different characteristics compared to measurement application such as the night vision system. The control system based on the ECU receives inputs from multiple sensors and therefore requires high controllability to process each of them. As the power supply voltage is used as the battery voltage, it is necessary to consider the high voltage, and it is also required to operate in a wide temperature range depending on the installed position in the vehicle.

An explanation from the viewpoint of the electronic system is as follows. Fig. 1.4 shows the architecture of the electronic system for the control application. In these

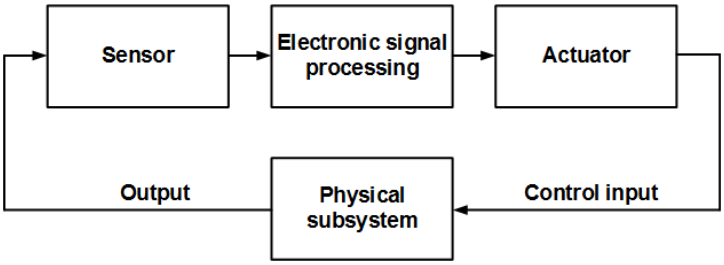


Fig. 1.4 Block diagram of control application.

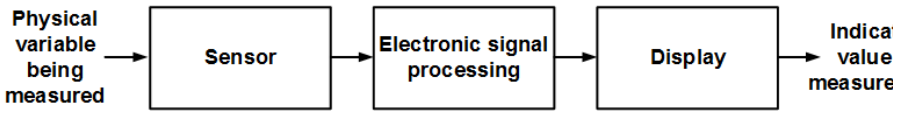


Fig. 1.5 Block diagram of measurement application.

Fig. 1.6 Block diagram of communication application.

systems, physical variables are controlled through actuators to control the physical subsystem. The actuators have electrical inputs and outputs such as mechanical, pneumatic, hydraulic, and chemical. The controlled physical subsystem depends on the change in actuator output. The control is operated by electronic signal processing based on the measurement of the sensor in response to the command by the driver.

In an electronic control system, the sensor output is an electrical signal, and the input is a physical variable for the control of the physical subsystem. Electronic signal processing is designed to provide the desired control of the physical subsystem from the

parameters measured by the sensor and generates an electrical signal that actuates the actuator.

An electronic measurement system which is shown in Fig. 1.5 is similar to a control system in terms of integrating sensor and electronic signal processing. However, the measurement architecture incorporates a display device instead of an actuator. The display means an electromechanical or electro-optical device capable of presenting numerical values to the user. Control and electronic instrumentation systems can use more than one sensor for electronic signal processing.

Fig. 1.6 is a block diagram of the communication system. In such a system, the data or message is transmitted from the source to the receiver over a communication channel. This architecture is generic enough to accommodate all communication systems, from car radios to digital data buses between multiple electronic systems in vehicles.

To further illustrate the features and trends of measurement and control systems, the following two sections describe the night vision system and the automotive control system, which are the applications that will be discussed in this dissertation.

1.1.3 NIGHT VISION SYSTEM

The night vision system is one of the most popular new features for the driver for safe driving, as shown in Fig. 1.7. The night vision system uses a thermal camera to increase driver awareness and to determine the distance the vehicle headlight cannot reach in dark or bad weather conditions. This technology was first introduced in Cadillac Deville in 2000. Since then, famous automobile manufacturers such as BMW and Mercedes have used this kind of system for production. In most cases, however, the system is offered as an option on certain premium vehicles or on new models, which is much more expensive than low-cost vehicles. Therefore, these services cannot reach all users of the product.

To reduce the product cost, the thermal camera is preferred to use an uncooled microbolometer infrared sensor because it is easy to manufacture and does not require a

Fig. 1.7 Audi A8 night vision assistant

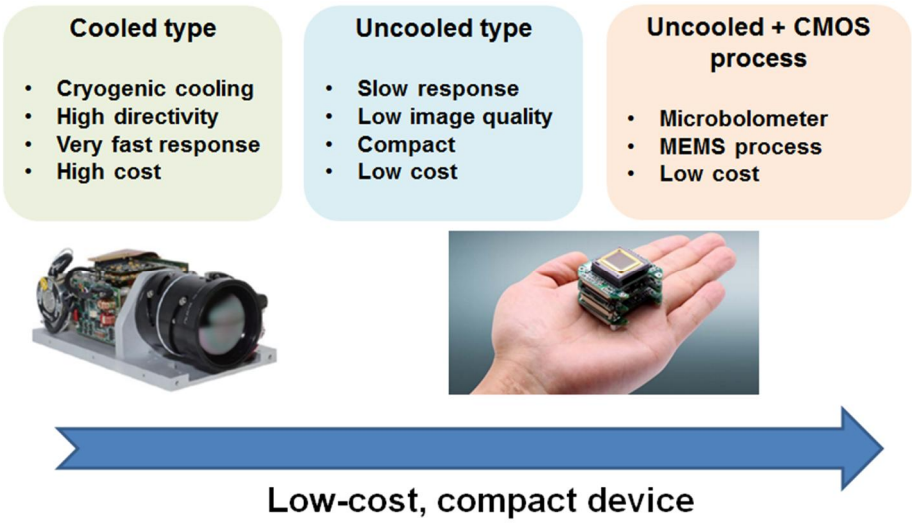


Fig. 1.8 Trends in low-cost infrared imaging systems.

cooling device like a cooling infrared sensor, which is summarized in Fig. 1.8.

However, the microbolometer is a method of absorbing the infrared rays of the object to the inside of the infrared sensor and changing the resistance of the sensor when the sensor is heated, and so the readout circuitry including the correction function for resolving the mismatch between the resistors and obtaining the minute electric signals are required. This necessitates the use of memory for calibration, external devices such as a microprocessor, and software to implement them, which increases the cost.

In this dissertation, therefore, the design and implementation of a low cost and compact infrared sensor readout circuitry is the most important goal. This will be discussed in detail in Chapter 2.

1.1.4 AUTOMOTIVE CONTROL SYSTEM

The automotive control system is operated by electronic control units (ECUs). The ECU is an embedded system in an automotive electronic device that controls one or more of the vehicle's electronic systems or subsystems, and therefore it is used in almost every part of the vehicle's functional area.

Fig. 1.9 shows a typical structure of the ECU. The basic operations of the ECU are to read various signals coming from the sensors and digitally calculate them in a microcontroller and control them through an output driver. ECUs use a closed-loop configuration to monitor the input of the system and control the output of the system, such as, for example, engine exhaust and fuel consumption management. These functions require the ECU to have several chips on the printed circuit board, as shown in Fig. 1.10.

As the number of functions continues to increase and the functionality itself becomes more complex, modern automotive systems use an architecture in which a few central ECUs communicate with each other. For example, the number of inputs of the sensors will serve as a requirement for such a centralized ECU. In Table 1.1, there are 28 sensors around the driver's seat as a body domain function. This is the case of the Grandeur of Hyundai Motors. If the inputs of the ECU are able to receive all of these, then only one ECU will control this region. On the peripherals side, the drivers (actuators) and sensors evolve into more powerful embedded MCUs with communication interfaces, voltage regulators, and other application-specific components.

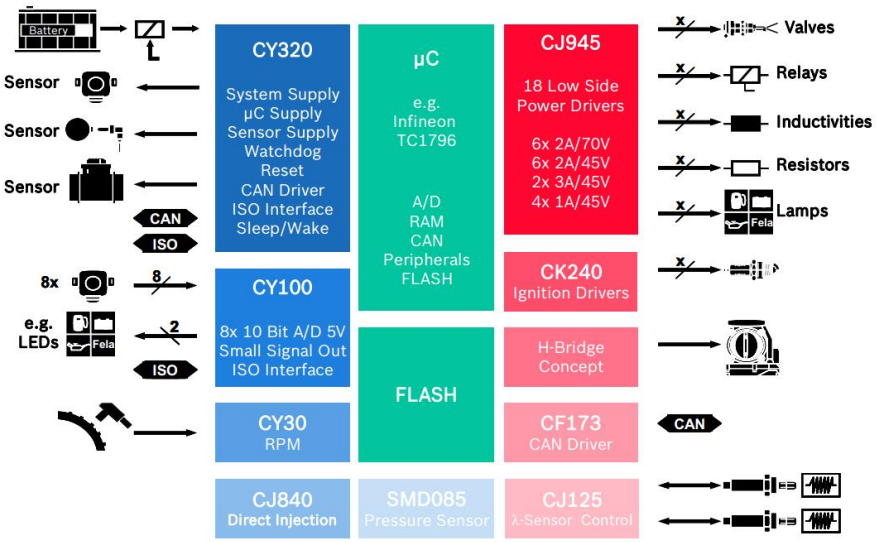


Fig. 1.10 Bosch's chip-set for the ECU.

High levels of integration of system or components such as the central ECU and the embedded ECU are certainly more than just product costs. For example, there are more direct savings: reduced number of parts, smaller PCB size, reduced design space, easier machine interface, more robust design, reduced manufacturing costs, fewer components to mount and less testing required compared to multiple ICs, improved quality by fewer solder joints.

In this dissertation, therefore, the design and implementation of a fully integrated sensor readout circuitry suitable for the concept of the central ECU is the most important goal. This will be discussed in detail in Chapter 3.

Table 1.1 Body domain sensors in Grandeur HG, Hyundai Motors.

Location in vehicle	Sensor	Functions
Driver seat	28	Door switches, steering wheel switches, buckle switches, seat belt reminder, climate control seat
Passenger seat	23	
Back seats	10	
Center fascia	16	Auto defogger, ACS, rain sensor, console switches
Front	5	Inhibitor switches, E/R fuses and
Floor	16	Power outlets
Roof	8	Map and room lamp switches

1.1.5 SENSOR READOUT CIRCUITRY

Sensors are devices that convert the energy of measurement variables into electrical signals. An ideal analog sensor produces an output voltage that is proportional to the quantity q being measured:

$$v_{sensor} = C_{sensor}\, q \tag{1.1.1}$$

where C_{sensor} is a calibration constant.

For example, the measured amount of throttle position sensor, a typical automotive sensor, is the angle of the throttle plate relative to the closed throttle. If the throttle angle changes from 0 degrees to 90 degrees and the response voltage vary from 0 to 5 volts, the sensor calibration constant C_{sensor} is expressed as $5/_{90^\circ} = 0.056$ (V/degree).

As shown in Fig. 1.11, the output of the sensor is converted by a digital output with the operation of the sample and analog-to-digital conversion. The analog-to-digital conversion is performed by an analog-to-digital converter (ADC). It is also sometimes called a quantizer. For these sensors, the output uses a binary system to calculate the electrical equivalent. The digital output has one of two possible voltages, representing 0 or 1. The array has N output terminals, which can represent 2^N values. For automotive applications, usually N ranges from 8 to 16, depending on the resolution required.

Digital signal processor outputs a numeric value to an external device in binary form once the calculation for a given function has been completed. If the analog output is required, such as for actuators for control systems, the output binary must be reconverted to analog form. This conversion is performed by a device called a digital-to-analog

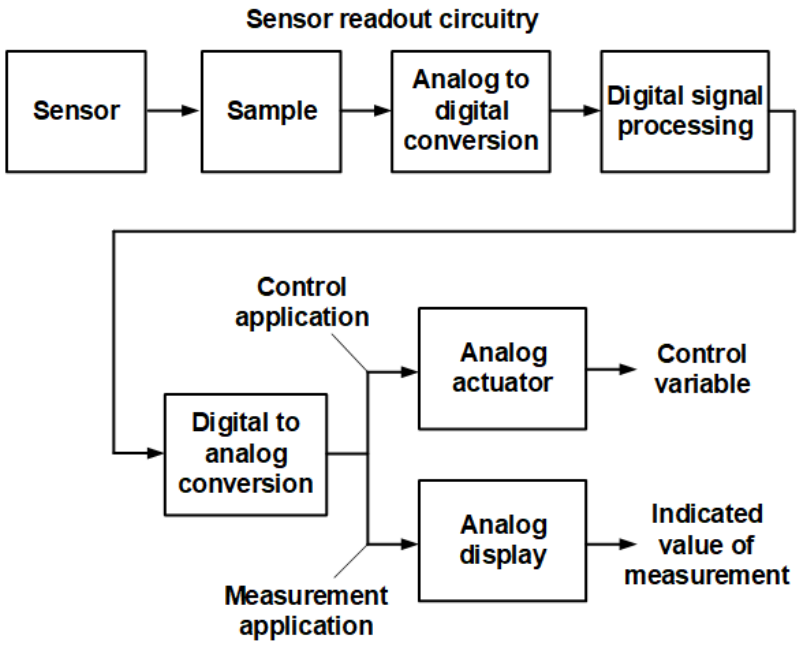


Fig. 1.11 Digital system configuration.

converter (DAC). However, sensors and actuators that are already digitally operating do not require a DAC.

In the sensor readout circuitry, the ADC is a core component. The ADC is a mixed-signal device that has both analog and digital functions. It provides an output that digitally represents the input voltage. Most ADCs convert the input voltage to a digital word, but also include the possibility of the input current.

The ADC is basically close to the function of a divider. This is because the analog output generates a digital output word where the analog input is between analog reference voltages. So the input and output transfer functions of the ADC can be expressed by the following equations.

$$D_{\mathrm{OUT}} = 2^n \frac{V_{\mathrm{IN}}}{V_{\mathrm{REF}}}, \tag{1.1}$$

where n is the number of output bits, V_{IN} is an analog input voltage, and V_{REF} is a reference voltage.

The resolution of the ADC is the output bit rate, and the resolution can be defined again as the size of the least significant bit (LSB). In the same sense, the most significant bits (MSB) are known by name in what it is. That is, it is a means of representing digital bits with least weight and most weight. For n-bit words, the MSB has a weight of $2^{(n-1)} = 2^n/2$ where the LSB has a weight of 1.

Better accuracy can be achieved by using either a higher resolution converter or using a smaller reference voltage because one LSB is equal to $V_{\mathrm{REF}}/2^n$. The problem with higher resolutions is cost. In addition, a smaller LSB means that it is actually difficult to detect a small signal when lost in the noise, and it reduces the performance of the ADC. The problem when lowering the reference voltage is the loss of the input dynamic range. As with high resolution, this results in the loss of performance due to the small signal being included in the noise.

For an ideal ADC, the maximum error is 1LSB. This is known as "quantization uncertainty" and refers to the uncertainty of where the input voltage lies in the 0 to 1 LSB. The quantization uncertainty is also called "quantization error." This error is the result of a finite resolution of the ADC. That is, the ADC cannot represent the input voltage beyond 2^n discrete values.

The performance of an ADC typically uses indicators such as signal-to-noise ratio (SNR). The SNR is the ratio of the output signal amplitude to the output noise level without harmonics or DC. For example, a signal level of $1V_{RMS}$ and a noise level of $100\mu V_{RMS}$ are represented by an SNR of 10^4 or 80dB. The maximum SNR of the ADC at the full-scale sine wave input is derived from the quantization noise and is defined as:

$$SNR_{MAX.} = 20\log\left(2^{(n-1)}\sqrt{6}\right) \approx 6.02n + 1.76\text{dB}\,. \qquad (1.2)$$

The SNR generally decreases with increasing frequency as the comparator's accuracy within the ADC degrades at higher input slew rates. This loss of accuracy appears as noise at the ADC output.

The SNR increases as the input amplitude increases until the input is close to full scale. In other words, in terms of quantization noise, the SNR increases at the same rate as the input signal until the input signal approaches full scale. This is because the step size becomes a small part of the overall signal amplitude as the signal amplitude increases. However, as the input amplitude approaches full scale, the rate of increase in SNR versus input signal gradually decreases.

Therefore, the performance improvement of the sensor readout circuitry correlates with the output amplitude of the sensor. Adding any gain stages to improve the SNR can also be an improvement. However, careful design is required to reduce an intrinsic noise generated by the added circuit.

1.1.6 SEMICONDUCTOR REQUIREMENTS

Automotive ICs work in harsh environments and must fulfill rigorous automotive quality standards, and therefore the reliability specifications of automotive semiconductors are higher than those of other industries as shown in Table 1.2. To meet the requirement of automotive semiconductor, AEC (Automotive Electronic Council) quality standard which defines reliability evaluation procedure for automotive electronic components is applied.

AEC-Q100 specifies the ambient operating temperature range as part of the stress test conditions for a given electronic device or integrated circuit (IC). It is an industry standard specification that outlines the recommended new product and major change qualification requirements. Five temperature ratings are defined as shown in Table 1.3. Grade 0 is the most stringent standard. It is also required to test whether the IC is operating at a high temperature of 150 degrees for over 1008 hours.

To help designers create robust automotive designs, global foundry vendors offer process technology that meets the automotive requirements and SPICE models with 6σ corners that reflect statistical data over extended temperature ranges. Also, package selection and PCB design must be performed accordingly.

Table 1.2 Comparing of semiconductor reliability requirement

Division	Home	Industrial	Automotive
Lifetime	1-3 years	5-10 years	> 15 years
Temperature	0ºC to +40ºC	-10ºC to +70ºC	-40ºC to +150ºC (Grade 0)
Humidity	Low	High	0-100%
Failure rate	> 10 %	< 1 %	0%
Supply period	> 2 years	> 5 years	> 30 years

Table 1.3 Part operating temperature grades at AEC-Q100

Grade	Ambient operating temperature range	Application example (Bosch product)
0	-40ºC to +150ºC	System power supply IC
1	-40ºC to +125ºC	Torque sensor steering
2	-40ºC to +105ºC	Dual axis acceleration sensor
3	-40ºC to +85ºC	Peripheral pressure sensor
4	0ºC to +70ºC	Infotainment

1.2 DISSERTATION CONTRIBUTIONS AND ORGANIZATION

The subject of this dissertation is the design and implementation of the sensor readout circuitry for the automotive electronic systems. Among the various applications utilizing the automotive electronics, a night vision system and an automotive control system are studied, which is summarized in Fig. 1.12. Each is one of the representative applications to embody the control and measurement applications discussed in the section on automotive applications. It also has different features from the design point of the sensor readout circuitry.

	Measurement application	Control application
Functional application	Automotive night vision system  Audi A8 night vision assistant	Automotive control System  Electronic control unit
Research topic	Infrared sensor readout circuitry • 2-dimensional sensors • Calibration • Sensor-specific ROIC	High-voltage input sensor readout circuitry • Multiple sensors • Controllability • High reliability (voltage, temperature, etc.)

Fig. 1.12 Research topics in this dissertation.

1.2.1 CONTRIBUTIONS

This dissertation contributes to the knowledge of analog design based on highly integrated analog signal processing in standard CMOS processes. Specifically, contributions from the dissertation are summarized as follows:

- Design of a fully-integrated infrared sensor readout circuitry based on an uncooled microbolometer sensor for two-dimensional imaging systems, which includes an 80 × 82 focal-plane array (FPA), pixel readout circuits based on a column-parallel capacitive transimpedance amplifier, analog readout circuits such as a programmable gain amplifier (PGA), a 12-bit analog-to-digital converter (ADC), a 10-bit digital-to-analog converter (DAC), a reference generator, a temperature sensor.
- Proposal of a calibration scheme, we named it shutter-based successive-approximation calibration loop (SACL), to calibrate a non-uniformity in a microbolometer array, improving cost, size, and complexity on a printed circuit board (PCB).
- Design of a fully-integrated high-voltage input sensor readout circuitry with an 8-bit embedded flash microcontroller and a 1Mbps CAN transceiver for automotive control systems, which also includes analog specific functions such as filtering by a low-pass filter (LFP) with a capacitance multiplication technique, common-mode voltage control using a 4-bit DAC, gain control using a PGA, conversion cycle control of a 12-bit ADC, and channel selection using

analog multiplexers.

- Proposal of a 12V 32-channel input interface to direct capture the outputs of the sensor up to 12V and to make the signals on 32 channels more programmable without external components, which improves size, cost, and complexity on a PCB.

1.2.1 ORGANIZATION

In Chapter 2, the dissertation describes a fully-integrated infrared sensor readout circuitry based on an uncooled microbolometer sensor: Chapter 2.1 introduces the backgrounds and challenges in the uncooled infrared imaging system and presents our approach compared to prior works. Chapter 2.2 describes the architecture of our imager, including the FPA and readout circuitry. Chapter 2.3 explains the implementation of the sensor readout circuitry in terms of analog signal path. Chapter 2.4 shows how the SACL calibrates the FPN. Chapter 2.5 analyzes experimental results from the prototype imager and assesses our approach. Chapter 2.6 summaries the specification of the infrared sensor readout circuitry and compares it with the previous designs.

In Chapter 3, the dissertation describes a fully-integrated high-voltage input sensor readout circuitry: Chapter 3.1 introduces the backgrounds and challenges in automotive electronic control systems and presents our approach compared to prior works. Chapter 3.2 introduces the overall architecture with an 8-bit microcontroller. Chapter 3.3 describes the operation of the input interface including a level-shifter, an LPF, and an analog front-

end (AFE). Chapter 3.4 describes the implementation of the key building blocks in detail. Chapter 3.5 analyzes experimental results obtained from a prototype chip and Chapter 3.6 summaries the specification of the high-voltage input sensor readout circuitry and compares it with the previous designs.

In Chapter 4, the conclusion of this dissertation is finally presented.

CHAPTER 2

INFRARED SENSOR READOUT CIRCUITRY FOR AUTOMOTIVE NIGHT VISION SYSTEMS

2.1 INTRODUCTION

2.1.1 UNCOOLED INFRARED IMAGING SYSTEM

Infrared thermal imaging evolved for military applications but has now focused on commercial and industrial uses, increasing the demand for low-cost, compact night vision devices [2.1]. The uncooled microbolometer, which can be implemented as a thin film layer of a material such as vanadium oxide [2.2], [2.3] or amorphous silicon [2.3], [2.4] is a promising device because it does not require cooling to low temperatures, and can be fabricated with its readout circuitry using a microelectromechanical systems (MEMS) process in standard CMOS technology.

Each pixel in a microbolometer produced by the MEMS process is a thermally isolated thermistor which measures temperature changes caused by the absorption of incident infrared radiation. This design has advantages regarding size, weight, cost, power consumption, and complexity; but the non-uniform response of the individual pixels

incurs spatially fixed pattern noise (FPN), which appears as in an image artifact. The FPN is caused by manufacturing process variations and self-heating by electrical power dissipation, as well as inherent variations related to the characteristics of a microbolometer, including its temperature coefficient of resistance and infrared radiation absorption coefficient. Moreover, gain stage in readout circuit increases the magnitude of these effects. Consequently, calibration is mandatory in the uncooled infrared imaging system.

2.1.2 CHALLENGE AND APPROACH

Reduction of FPN is usually achieved by a scene-based or a shutter-based approach [2.27]. The scene-based approach avoids the need for a shutter by using a statistical analysis based on histograms obtained from the neighbors of a pixel [2.5], [2.6]. However, this approach requires additional electronics to shift and filter images. Uniformity of the image is also compromised because there is no uniform reference image for calibration. Additional compensation may also be required within the pixel readout procedure to stop the FPN saturating the analog signal. The shutter-based approach allows images, the use of reference information, which leads to the cleaner. Although the periodic operation of the shutter may be unacceptable in real-time applications, the shutter is still widely used [2.30]. When the shutter is closed, the outputs of individual pixels are stored in memory, and subsequently compensated for the expected characteristics of the scene [2.7]. This can be performed by several different types of circuit. For example, a network consisting

of switches and resistors can be used to compensate the FPN [2.8]; but a resistor network requires tuning and is subject to process variations. A more popular method of compensation is to use a digital-to-analog converter (DAC) to provide a tunable voltage to adjust the bias of the pixel readout circuit, as shown in Fig. 2. 1. Tissot et al. [2.9], Arcas et al. [2.10], Kang et al. [2.11], Jo et al. [2.12], Liu et al. [2.13], Seo et al. [2.14], and Fiorante et al. [2.15] have proposed pixel readout circuits which use techniques such as current injection and bias equalization to provide compensation. These approaches require an external digital processor and memory to run a calibration algorithm which

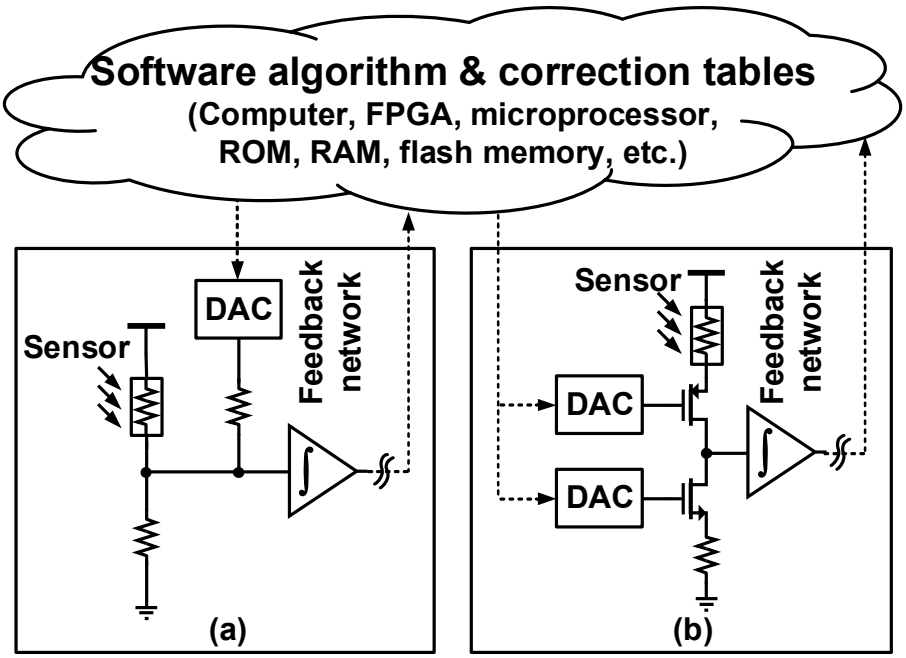


Fig. 2.1 Conventional FPN compensation scheme with two types of generic pixel readout circuits. (a) Current injection. (b) Bias equalization.

constructs a correction table, which is subsequently needed to control the DAC. In addition, this feedback network must be tightly coupled with the pixel readout circuit to provide frequent iterations, so as to accommodate changes in the condition of the microbolometer. These increase the complexity of the system on printed circuit board (PCB) and are therefore more expensive and larger.

To solve these problems, we compensate for FPN by introducing a shutter-based successive-approximation calibration loop (SACL) with a flow that follows the direction of the red arrows in Fig. 2.2. Based on this loop, we realize a fully integrated uncooled microbolometer infrared imager with an 80×82 focal-plane array (FPA) and readout

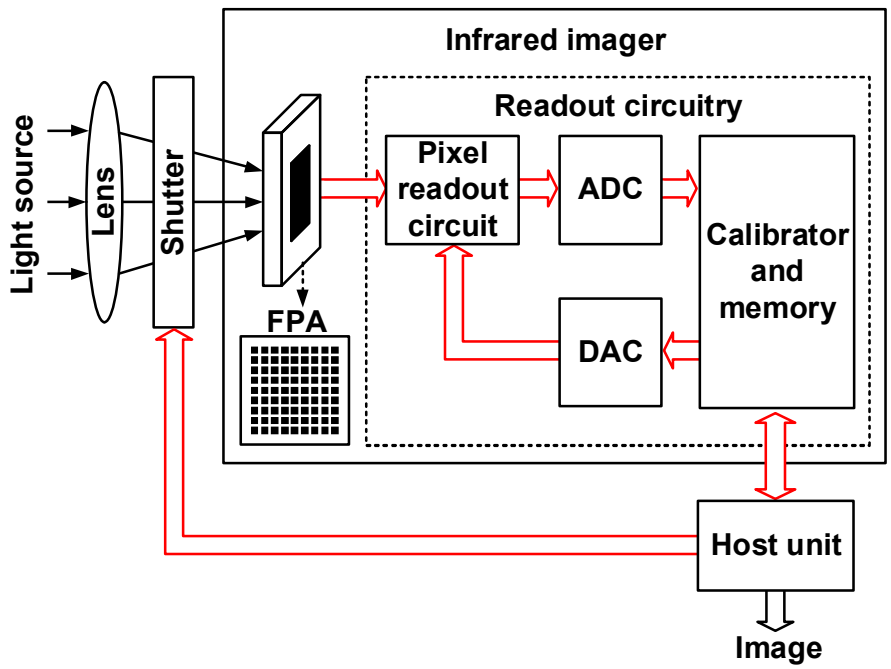


Fig. 2.2 Infrared imaging system with proposed infrared imager.

circuitry. This imager also has a twice-writable one-time programmable (OTP) memory, interface units to communicate with a host, and analog peripheral circuits, including an internal temperature sensor to monitor chip temperature, a tunable reference generator to provide current and voltage sources, and a line drop-output (LDO) regulator.

2.2 ARCHITECTURE

2.2.1 FOCAL-PLANE ARRAY

The FPA consists of active, blind, and dummy pixels, as shown in Fig. 2.3(a). The active pixels are exposed to infrared radiation and located at the center of the upper layer, in the field of the lens. The blind pixels are above and below the active pixels and shielded from radiation. Their primary function is to provide a reference resistance to compensate for any change in resistance of the corresponding active pixels. Around these, dummy pixels are placed to improve the match between the active and blind pixels during manufacture. A solder frame, consisting of solder layers, connects the substrate wafer and the silicon lid (cap) wafer. The distance between the edges of the FPA and the solder frame is 100 μm, and the width of the solder frame is 250 μm.

The FPA must be encapsulated for thermal isolation. This requires efficient vacuum packaging, and different packaging technologies are required at the chip [2.16], wafer [2.17], or pixel [2.18] level. Chip-level packaging is relatively expensive because it requires a vacuum chamber, and it is also an obstacle to miniaturization due to the large cap needed to seal the vessel containing the chip. Pixel-level packaging is cheaper but less effective. We use wafer-level packaging technology, with the cross-section shown in Fig. 2.3(b), which provides a good compromise.

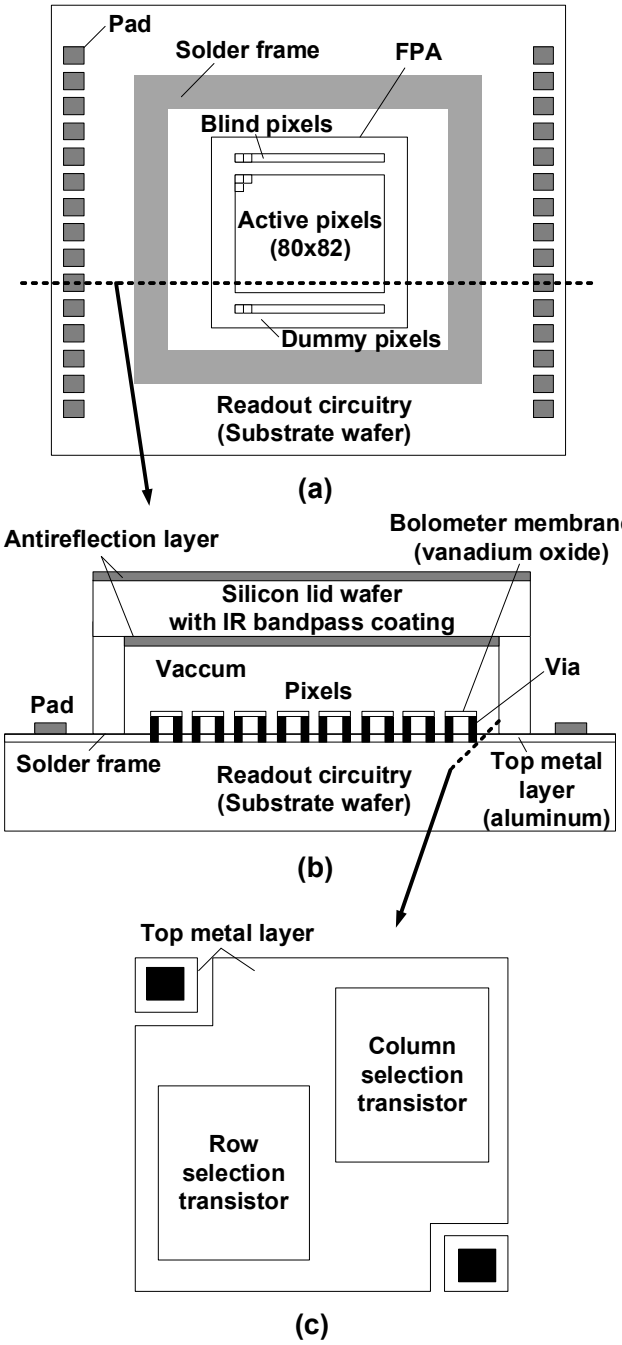


Fig. 2.3 (a) Imager configuration and (b) its cross-section; (c) pixel layout at the wafer surface.

The silicon lid wafer is a silicon-on-insulator wafer. An infrared bandpass coating passes wavelength between 8 and 14 μm, and an antireflection layer significantly improves light transmission. The incident infrared radiation crosses the vacuum and is absorbed by a thin film of vanadium oxide. This is the microbolometer membrane, and its thermal conductance is provided by a via to the metal layer. The topmost layer of the readout circuitry is aluminum, which reflects some of the infrared radiation which passes through the vanadium oxide, increasing the absorption rate.

Two nMOS transistors are located beneath each pixel to ensure that it is only addressed when both its row and column are selected, as shown in Fig. 2.3(c). Each pixel is 35μm×35μm, and each via is 10μm×10μm. The gaps between vias and between pixels are all 1 μm.

2.2.2 READOUT CIRCUITRY

The readout circuitry includes most of the blocks required by an infrared imager, as shown in Fig. 2.4. The row and column decoders, controlled by a register and a timing controller, select individual pixels in the FPA. The column-parallel readout circuits convert the change in resistance at the selected pixels into voltage levels. This circuit is explained in more detail in Section III. An analog multiplexer (MUX) sequentially transfers the voltages to an analog-to-digital converter (ADC), and the digital data output by the ADC is stored in a frame memory. The calibrator performs arithmetic operations,

which are explained in Section IV. The values output by the calibrator are stored in a memory, and these values determine the sequential voltages output by the column-parallel DACs, which calibrates the FPN.

The 128-byte OTP memory is activated for normal operation. Its function is to retain control bits used at each block even after power is removed. In general, the OTP memory is programmed once after manufacturing by fuses or anti-fuses, which has a limitation of rewriting. To improve the flexibility, we copy the same contents into three sections of 32,

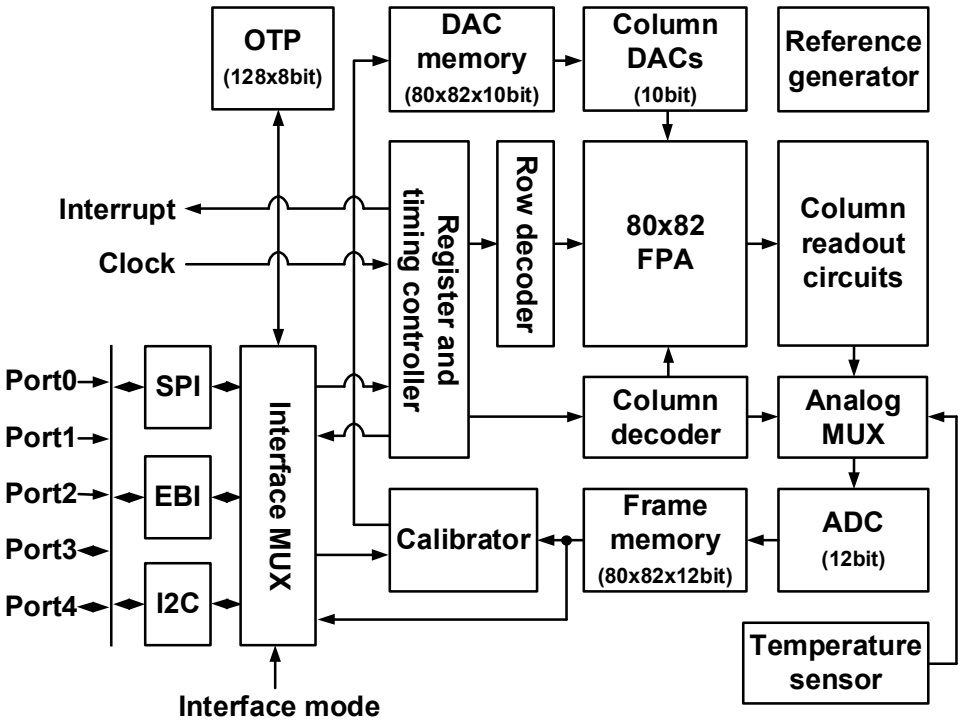


Fig. 2.4 Block diagram of the infrared imager.

Table 2.1 Interface pin description

Name	SPI	EBI	I2C
Interface mode [1]	Don't care	1	1
Interface mode [0]	0	0	1
Port 0	CS	CS	-
Port 1	SCK	D/C	SCL
Port 2	SDI	WR	-
Port 3	SDO	RD	SDA
Port 4	Frame and line sync	Data [7:0]	Frame and line sync

CS = chip select, SCK = serial clock, SDI = serial data input, SDO = serial data output, D/C = data and command, WR = write, RD = read, SCL = serial clock, SDA = serial data.

48, and 48 bytes, and include a function to select one of the three sections. This lets the two parts of 48 bytes, where 12 bytes are for the selection function, to be selected by the user, and consequently, this OTP memory is twice writable.

Extended communication is handled by the serial peripheral interface (SPI), the external bus interface (EBI), and the inter-integrated circuit (I2C) protocols. Table 2.1 shows the corresponding pin descriptions. We use 2-bit interface mode to reduce the number of pins and apply an interface MUX as a wrapper for this data format. Ports 0 to 3 each have one pin. Port 4 has eight pins for EBI parallel data output. Frame and line sync, which are synchronized frame-by-frame and row-by-row signals, share two ports.

Addresses from 0 to 6559 correspond to the digitized outputs of the 80×82 pixels in a frame. To improve the response of the output signal, the frame memory is divided into four groups, G1-G4, with the addresses shown in Fig. 2.5 (a). Whenever a group of pixels is updated, an interrupt is issued, and a series of data streams are transferred to an external host unit using the EBI or SPI protocol. This reduces the response time to a

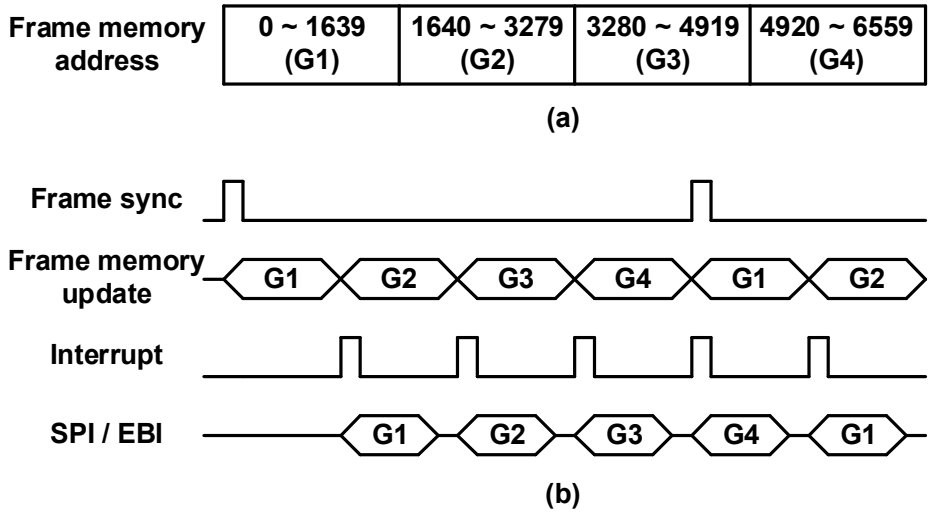


Fig. 2.5 Interface timing diagram.

quarter of the frame sync period, as shown in Fig. 2.5 (b).

When the frame and DAC memory is updated, an overrun error will occur if an attempt is made to write a new entry into a full memory, and an underrun error will occur if there is an attempt to read data from empty memory. Either of these events will cause an interrupt, which can be used to trigger a command to clear outdated data from a host unit.

2.3 IMPLEMENTATION OF SENSOR READOUT CIRCUITRY

2.3.1 PIXEL READOUT STRUCTURE

Fig. 2.6 (a) shows the pixel readout structure. The active and blind pixels are connected in columns which are two pixels wide. Each pair of pixels is separated from the pairs above and below to provide the space necessary for a DAC and a column readout circuit. Each block of two active and two blind pixels is linked by a bridge node connected to a readout circuit. The output of the DAC provides the bias voltage which is applied to the blind pixel.

Because the number of readout circuits is half the number of pixels in a row, pixel readout is timed in a similar way to an interlaced scan, and thus the line sync signal is generated twice for each row, as shown in Fig. 2.6 (b). It is also possible to increase the frame-rate by introducing a register which allows only the odd or even pixels to be output.

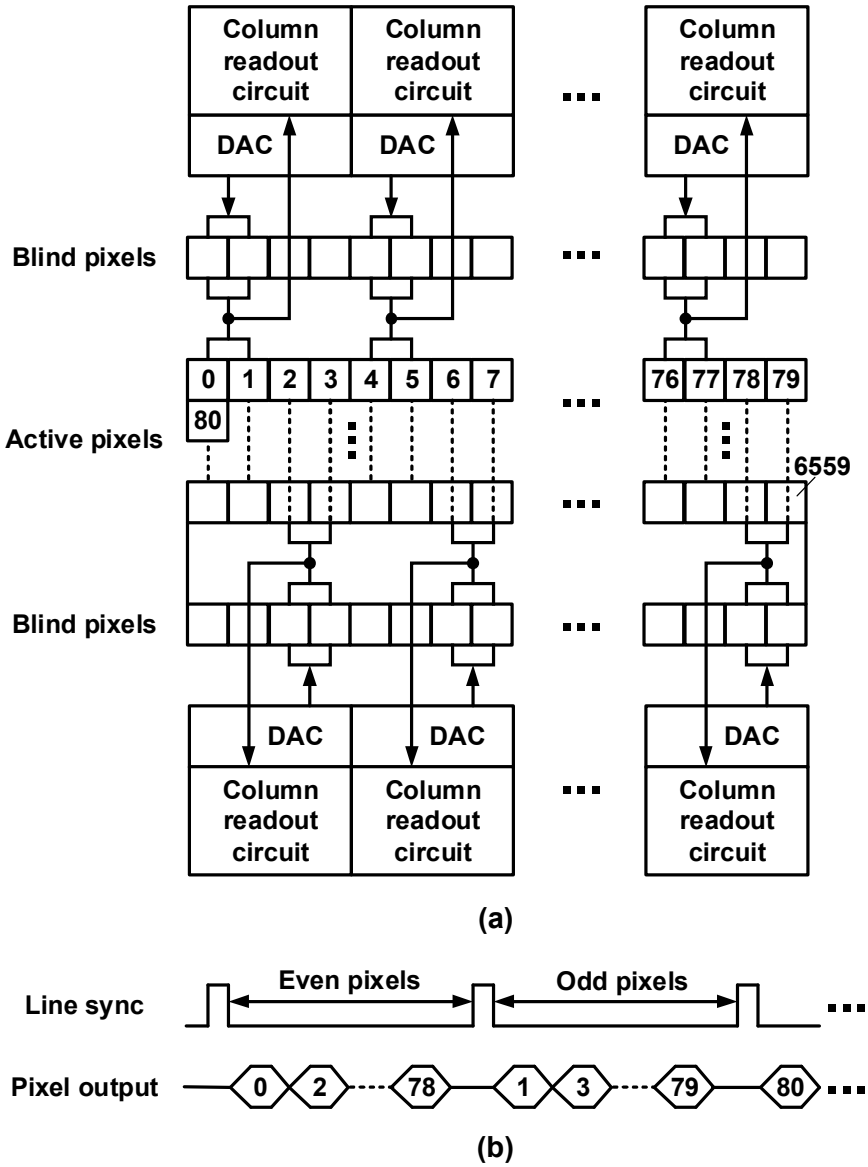


Fig. 2.6 (a) Pixel readout structure and (b) its timing diagram.

2.3.2 ANALOG READOUT STRUCTURE

Fig. 7 shows the analog signal path, which includes 40 column units and a single output stage consisting of a single-ended-to-differential programmable-gain amplifier (SD-PGA) and an ADC. In the column unit, R_{A} and R_{B} are the resistance of the active and blind pixels respectively. R_{A} and R_{B} is a resistance-to-current (R-I) converter, which produce a sensing current I_{S} and a blind current I_{B}. The net current I_{O}output by these pixels can be expressed as follows:

$$I_{\mathrm{O}} = I_{\mathrm{B}} - I_{\mathrm{S}} = \frac{V_{\mathrm{DAC}} - V_{\mathrm{COM}}}{R_{\mathrm{B}}'} - \frac{V_{\mathrm{COM}}}{R_{\mathrm{A}}}, \tag{2.1}$$

where V_{DAC} is the output of the DAC, V_{COM} is the common-mode voltage, and R_{B}' is the combined resistance of the two resistance labeled R_{B} in Fig. 2.7, which are connected in parallel.

In our design, the maximum output range of V_{DAC} is from 1.6V to 2.6V, and V_{COM} is 1.4V. The resistance R_{B} is 100kΩ, so that R_{B}' is 50kΩ, and R_{A} is 100kΩ when there is no infrared radiation. The blind pixel resistances are connected in parallel to average noise and offset, and to increase the output range of V_{DAC} by reducing the fixed DC component. If there were a single resistor, then the range of V_{DAC} would have to be between 2.2V to 3.2V, which would require a higher supply voltage than the 3.3V which is actually provided.

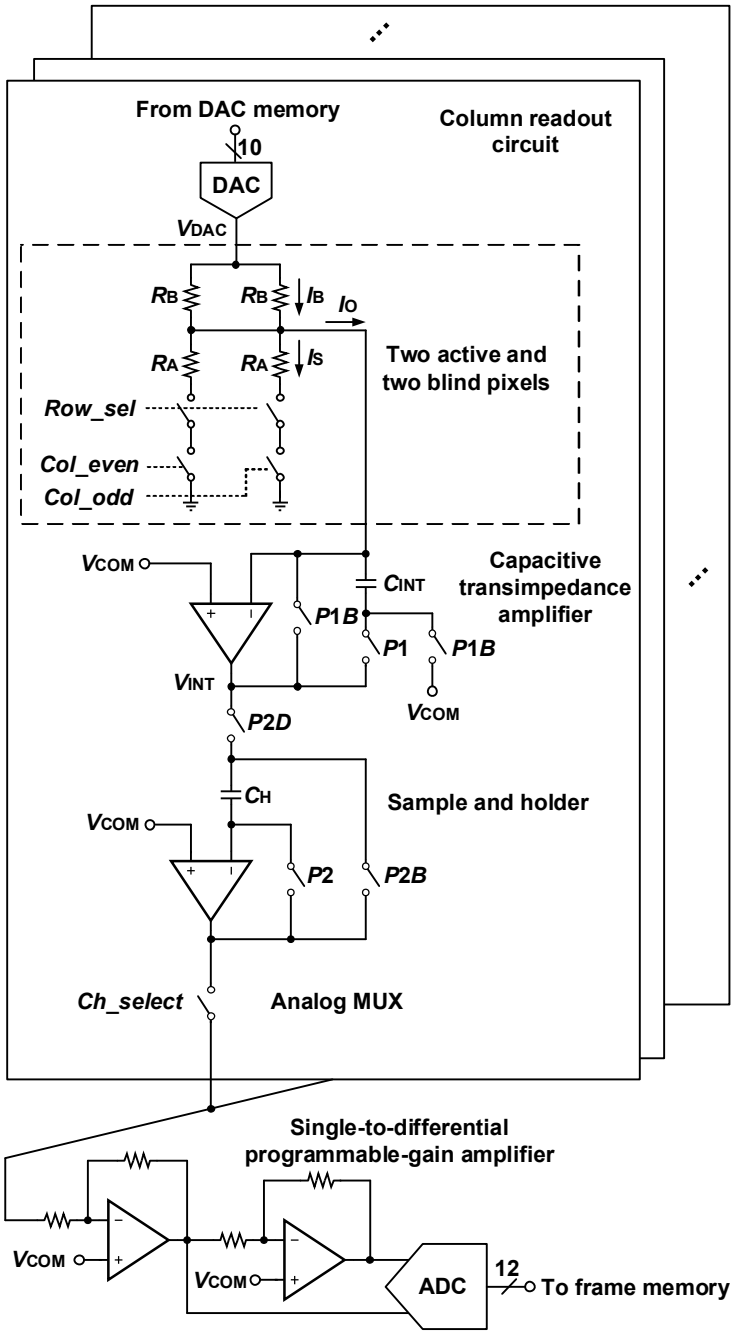


Fig. 2.7 Block diagram of the analog signal path.

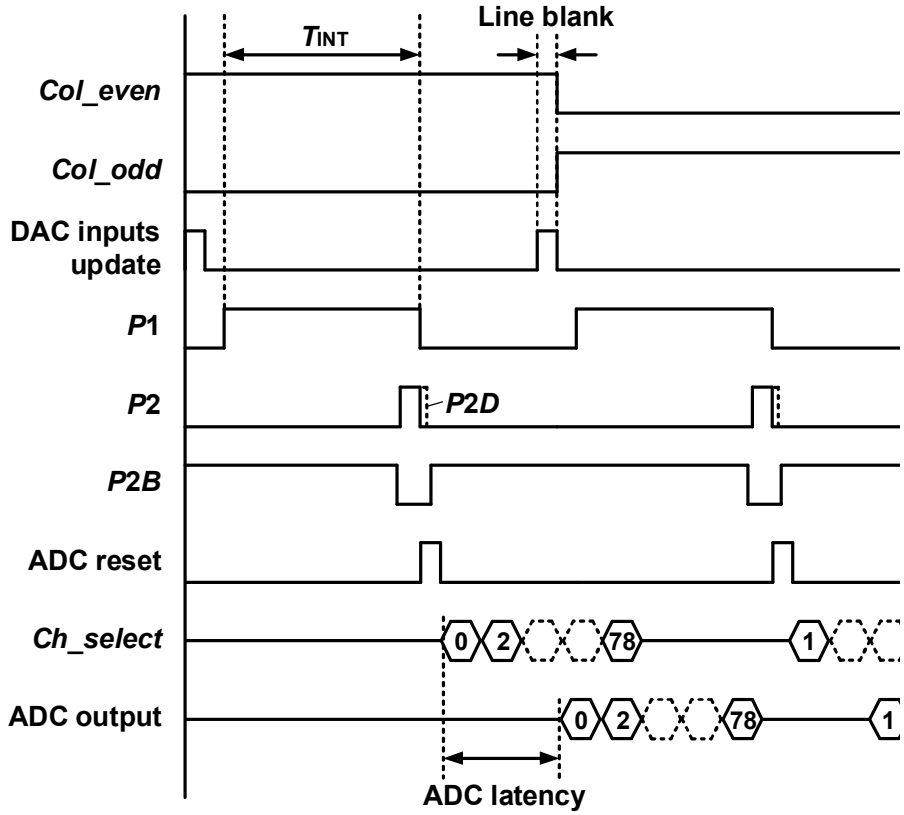


Fig. 2.8 Timing diagram of the analog signal path.

An alternative way of reducing the voltage range required from the DAC would be to insert a branch into the wire carrying I_O for calibration [2.11], and connect the blind pixels direct to the supply voltage, but that increases both the power dissipation and the calibration factor.

After R-I conversion, I_O is then integrated over a period of T_{INT}, using a capacitive transimpedance amplifier (CTIA) as a current-to-voltage (I-V) converter. A CTIA provides high gain and good noise suppression when sensing very small currents

[2.19]−[2.22]. The integrated voltage output V_{INT} can be expressed as follows:

$$V_{\mathrm{INT}} = V_{\mathrm{COM}} - I_{\mathrm{O}} \frac{T_{\mathrm{INT}}}{C_{\mathrm{INT}}}, \tag{2.2}$$

where C_{INT} is the integration capacitance.

In our design, the default values of T_{INT} and C_{INT} are 48μs and 4pF respectively, and hence the gain of the CTIA is 12×10^{6}V/A. These values can be adjusted by a gain-control register within the constraint of the frame-rate.

We use a correlated double-sampling (CDS) technique [2.23], [2.24] to reduce the systematic offset and $1/f$ noise in the CTIA. These noise sources of the CTIA are stored on C_{INT} when $P1$ is low (and $P1\mathrm{B}$ is high) as shown in Fig. 2.8. This extends the range of V_{DAC} by eliminating the unnecessary voltage headroom at V_{INT}.

After the integration of I_{O} is complete, a sample-and-hold (S/H) circuit samples V_{INT} in the 1 pF hold capacitor C_{H} at the falling edge of $P2$. A delayed version of $P2$, called $P2D$, samples the bottom plate of C_{H} to eliminate the injected charge, which is dependent on the signal range of V_{INT}. There is also an inverted version of $P2$, called $P2B$, with non-overlapping phase. The signals held by the S/H circuit are sequentially transferred into the SD-PGA under the control of the channel selection signal. The SD-PGA, which consists of two inverting amplifiers, converts the single-ended signal into a differential-ended signal to improve the noise immunity of the ADC, and the gain of this conversion can be adjusted by varying the resistance ratio.

The values arriving in the DAC memory, which is part of the SACL, are fed into the

DAC during the line-blank time. These values cause the DAC to produce a voltage V_{DAC} which forces I_{O} to zero, suppressing the FPN caused by variations in R_{A}, R_{B}', and V_{COM}, as well as the effect of the gain and offset of the column unit and the output stage, which are all part of the SACL.

The common-mode voltage V_{COM} and the tail currents for the amplifiers are generated by an internal reference generator based on a Brokaw bandgap reference circuit [2.25], which produces a temperature-independent voltage of 1.2V. A temperature sensor is implemented by measuring the proportional-to-absolute-temperature (PTAT) current within the Brokaw cell. The voltage output of the temperature sensor is from 1.25V to

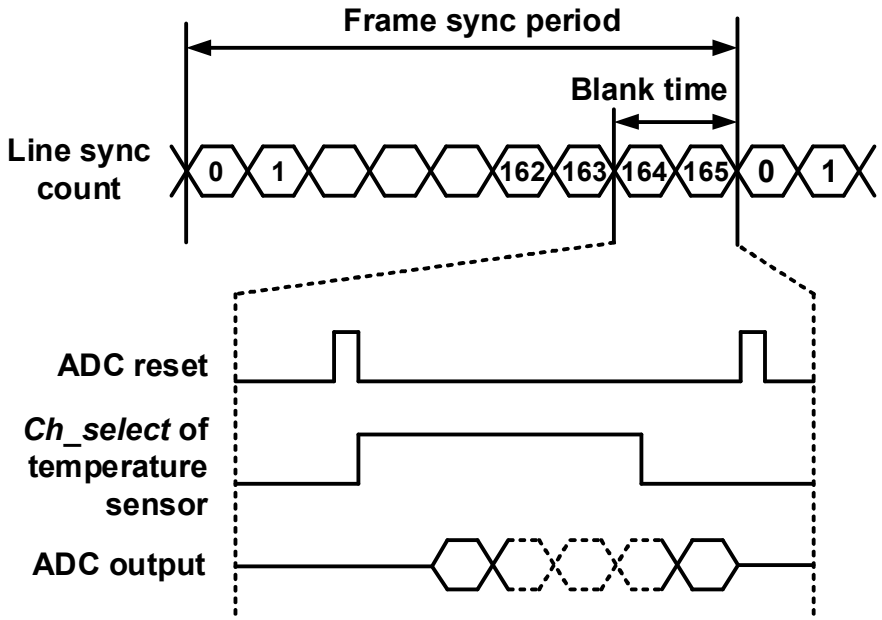


Fig. 2.9 Timing diagram for A/D conversion of temperature sensor.

2.25V at -25℃ to 75℃ respectively, and it is digitized using a dedicated channel in the analog MUX to avoid any delay to the reading of pixels during line blanking. As shown in Fig. 9, this period has the same length as two line syncs. This timing also allows the output streams of the ADC to be averaged.

Fig. 2.10 shows the block diagram of the ADC and the DAC. The 12-bit ADC uses a conventional pipelined topology of 1.5 bits per stage. The maximum sampling frequency is 1MS/s, which gives a frame-rate of 120fps with an 80×82 array size, after allowing for blanking time. The latency from V_{IN} to D_{OUT} is 8 clock cycles. The 10-bit DAC uses a conventional R-2R ladder topology. V_{REFT} and V_{REFB} are generated by the internal reference generator to adjust the range of V_{DAC}. We have not tried to match the resolution of the most up-to-date ADC and DAC designs [2.28], because our focus is on the design and verfication of the SACL. Improved noise performance should be achievable by introducing a higher-resolution ADC and DAC into our circuit, and increasing the size of the frame memory and DAC memory to suit. If our design required external correction tables, they would also have to be increased in size to accommodate a higher resolution; but this necessity is avoided because our design has eliminated these tables.

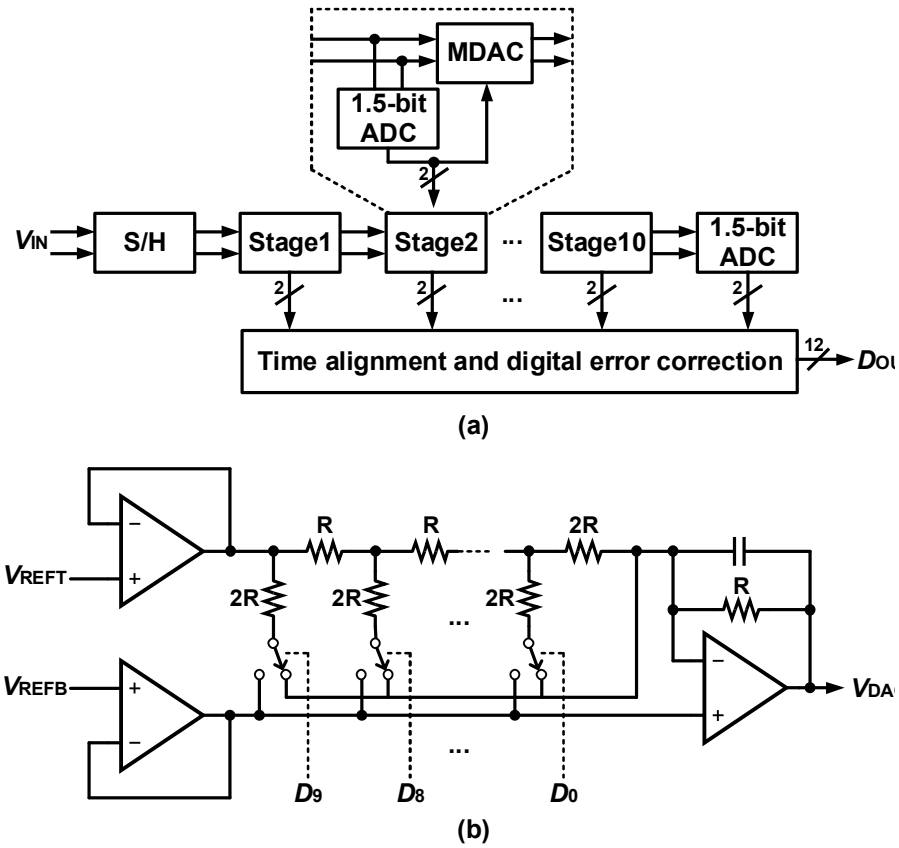


Fig. 2.10 Block diagram of (a) the ADC and (b) the DAC.

2.4 SUCCESSIVE APPROXIMATION CALIBRATION LOOP

2.4.1 OPERATION

The operating sequence of the SACL is shown in Fig. 2.11. After power on, the 128-

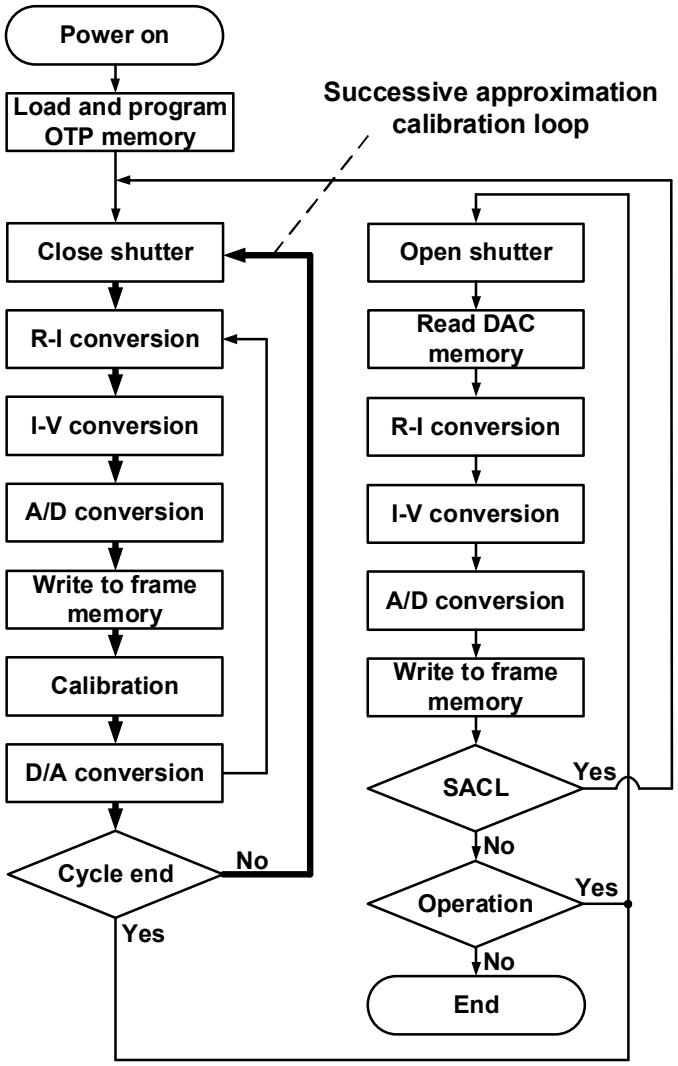


Fig. 2.11 Operating sequence of the imager with SACL.

byte OTP memory is loaded for operation. The SACL operates synchronously with the shutter. A single cycle through the SACL involves analog readout, calibration, and the reading from or writing to the frame and DAC memory. During each cycle, the values in the DAC memory are updated, and the DAC uses the new values in its memory to compensate for the FPN while the shutter is open. A cycle through the SACL is repeated at intervals which depend on the amount of time-varying FPN, which in turn depends on the thermal drift. It is also possible to predict the FPN from the temperature measured by the internal temperature sensor. This potentially allows more accurate readings with the introduction of a temperature-dependent weight and also permits the shutter to be closed less frequently.

The calibrator performs the comparison, addition, and subtraction necessary for successive approximation. Its operating sequence is shown in Fig. 2.12. The comparator first compares the value in the frame memory with a reference value from the OTP memory. Then the virtual DAC-input generator supplies digital inputs to the DAC, which does not use the values in the DAC memory while the SACL is operating. The number of cycles, n, and the cycle coefficient, C, must be chosen to suit the resolution of the DAC. With a 10-bit DAC, the maximum number of cycles is 10, and the loop coefficient for each cycle is expressed as follows:

$$C(n) = 2^{(10-n)}. \tag{2.3}$$

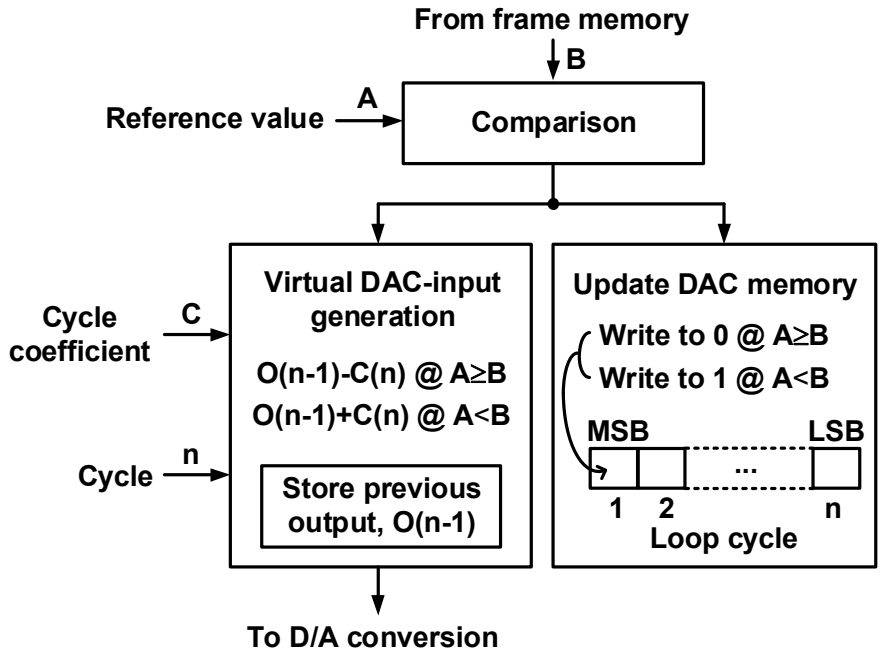


Fig. 2.12 Operation sequence of calibrator in the SACL.

If the reference value is larger than the value from the pixel in the frame memory, the output of the virtual DAC-input generator is subtracted to the cycle coefficient. Otherwise, they are added. Its result is sent to the DAC, and the calibrator puts the adjusted value into the frame memory during the next cycle. From the new result of the frame memory, the calibrator writes each bit from MSB to LSB of one word in the DAC memory.

Fig. 2.13 shows new successive cycles of the SACL compensate for the FPN caused by a change of 5kΩ in the active microbolometer with no incident radiation. From this, the resistance of the active and the blind microbolometers are 105kΩ and 100kΩ

respectively. During the first cycle, the cycle coefficient initializes the output of the virtual DAC-input generator. That value is converted to a voltage by the DAC, which has its output range set to $0.1V_{P-P}$, from 2.05V to 2.15V. The resistance change in the active microbolometer causes a change in the output current of the pixel by R-I conversion, following the equation (1). The CTIA integrates the output current of the microbolometers to produce a voltage. The gain of the CTIA is 12×10^6 V/A, and the output voltage is derived from equation (2). Because the output range of our CTIA is from 0.4V to 2.4V, a voltage outside this range is expressed as the ideal output. During cycle 1, the 12-bit ADC converts 0.4V into the digital value of 0 and transfers it to the frame memory. In this example, the SD-PGA acts as an analog buffer to drive the input node of the ADC, and thus the gain is unity. Since the stored value of 0 in the frame memory is smaller than the reference value of 2030, the calibrator updates 0 in the MSB of one word of the DAC memory. The virtual DAC-input generator subtracts the current cycle coefficient of 256 from its previous output of 512, to arrive at a new output of 256. These operations are repeated until 10 cycles have been performed. The outcome, with the reference value of 2030, is that the initial value of 0 in the frame memory, caused by FPN, becomes a calibrated value of 2032. The SACL also finds the corresponding digital input to the DAC, which is 171. This is located in the DAC memory and used during normal operation when the shutter is open. When incident infrared radiation changes the resistance of the active microbolometer to 500Ω, the final pixel value stored in the frame memory is 3599.

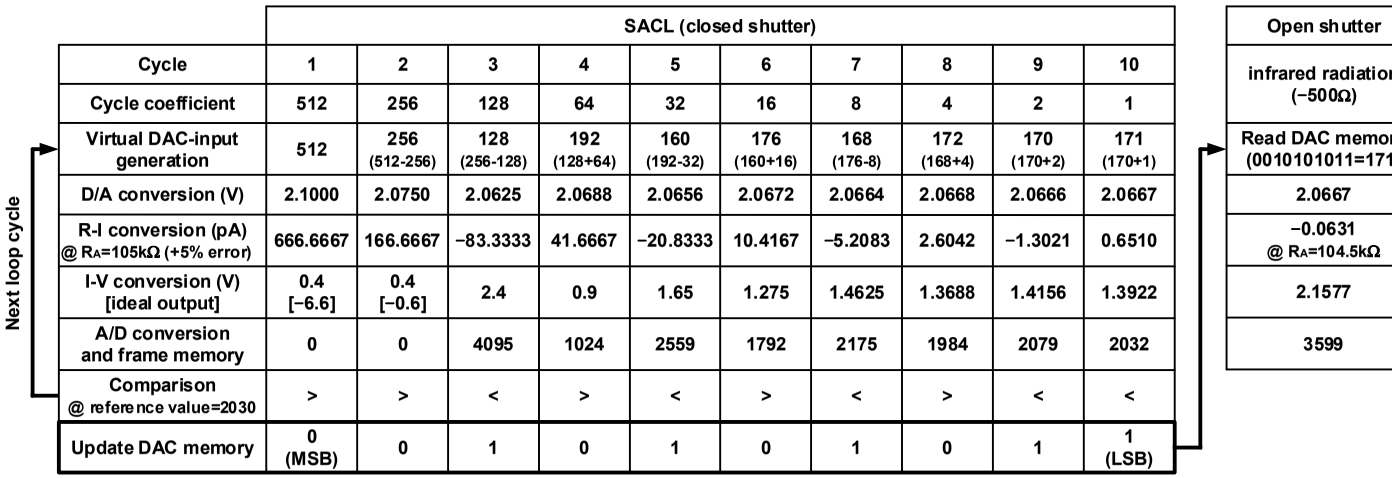


Fig. 2.13 Example operation of the SACL.

2.4.2 CALIBRATION ACCURACY AND RANGE

The calibration accuracy, which is the difference between a target reference value and a calibrated value in the frame memory, is inversely proportional to the range of FPN levels which need to be compensated, and these depend on the resolution of the DAC. Fig. 2.14(a) shows calibrated values for a variable output range of a 10-bit DAC. The change in resistance of the active microbolometer in the x-axis of this figure represents a distribution of the FPN. The SACL causes the distributed FPN to converge at the reference value of 2030. Increasing the output range of the DAC increases the calibration range and decreases its accuracy because the resolution of the DAC determines the smallest possible change of a calibrated value. For example, if the voltage increment of the DAC produced by the LSB of the input is changed from 100μV to 500μV, then the value in the frame memory changes from 40 to 240, because of the R-I and I-V conversion. This is the smallest change that can be achieved by the SACL. Therefore, the calibration accuracy is the lowest when the output range is $0.5V_{P\text{-}P}$, as shown in Fig. 2.14(b).

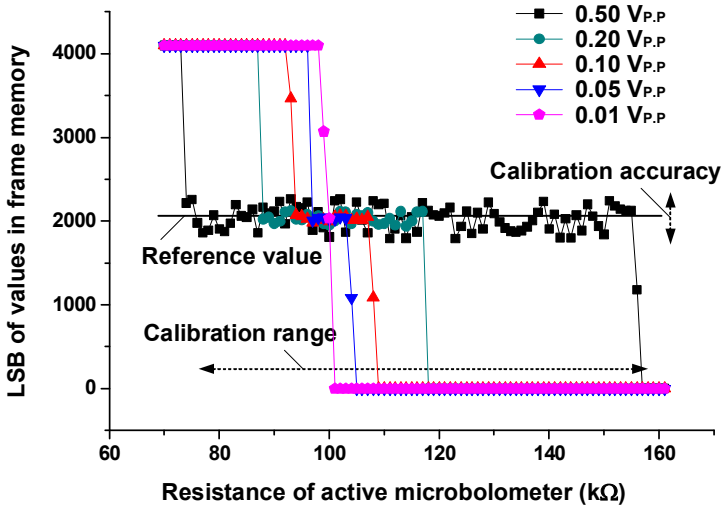


Fig. 2.14 Calibration accuracy and range (a) against output range of the DAC, and (b) its percentage values. The calibration accuracy is expressed as percentages of the ratio at the maximum output, which is 4095, and the percentage in range is the peak-to-peak variation based on a resistance of 100kΩ.

2.4.3 TIMING FOR FOCAL-PLANE ARRAY

Each cycle of the SACL has two phases, as shown in Fig. 2.15. During phase 1, the

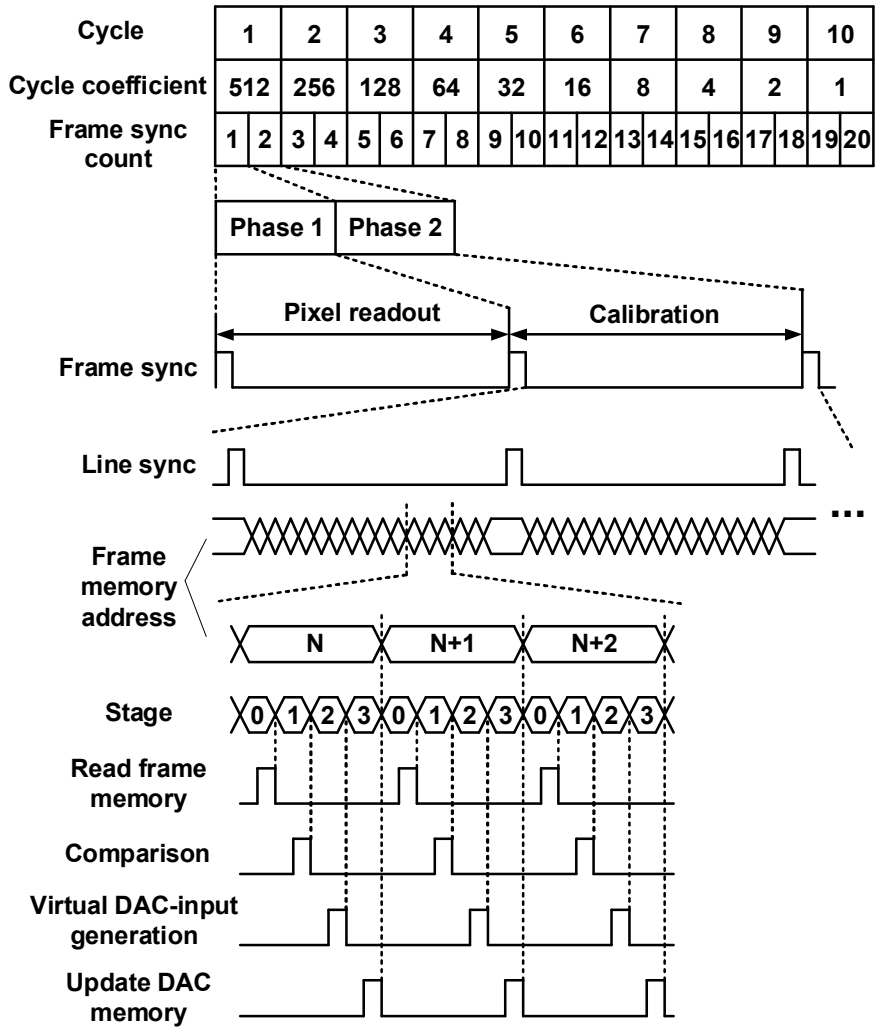


Fig. 2.15 Timing diagram for the focal-plane array.

values of the FPN in the focal-plane array are read and stored in frame memory. During phase 2, the corresponding pixels calibrated. There are four stages in this phase. In stage 0, the calibrator reads the FPN values stored during phase 1 in the frame memory. In stage 1, these values are compared with the reference value. During stage 2, the results of these comparisons are used to determine the output of the virtual DAC-input generator, which is sent to the line-buffer in front of the DAC for the next cycle. In stage 3, the DAC memory is updated. After a series of iterations have been completed, all calibration values for the FPA are stored in the DAC memory. Calibration takes 10 frames.

2.5 EXPERIMENTAL RESULTS

2.5.1 PROTOTYPE CHIP

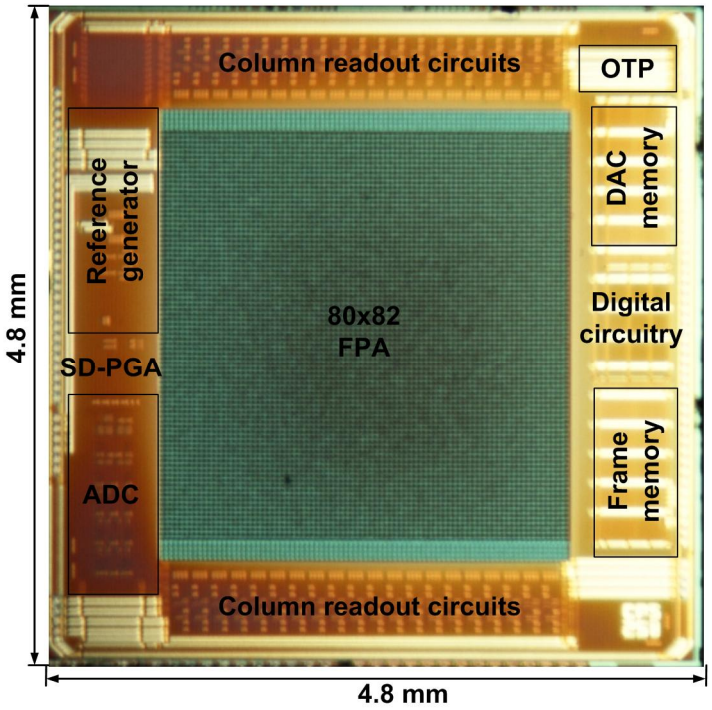


Fig. 2.16 Photograph of the imager.

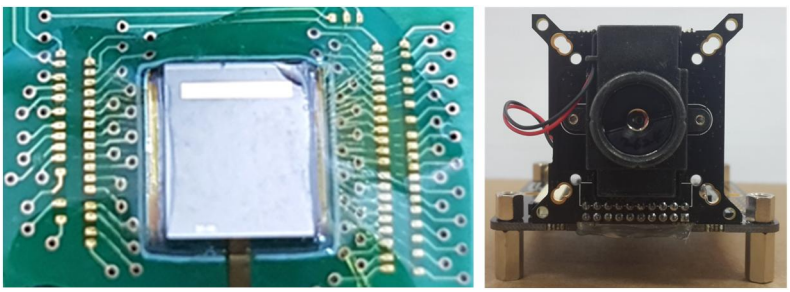


Fig. 2.17 Imager on PCB board (left) and infrared imaging system (right).

A prototype infrared imager was fabricated using a microelectromechanical systems (MEMS) process in standard CMOS technology. The size of the prototype imager is 4.8mm × 4.8mm including the I/O pads and sealing layer, as shown in Fig. 2.16. The digital circuitry includes the calibrator, interface units, and the register and timing controller; the size of the calculator in the SACL is negligible. Fig. 2.17 shows the infrared imaging system incorporating our prototype imager, and used to assess overall performance.

2.5.2 POWER DISSIPATION

The digital circuit and memories operate at a 1.8V supply voltage and have thin transistors to reduce size. The analog circuits, including the column readout circuits, DAC, SD-PGA, ADC, and reference generator, operate at a supply voltage of 3.3V and have

Table 2.2 Current consumption by (simulated) circuit blocks

Block name	Unit current (mA)	Number of units	Current (mA)
DAC	0.19	40	7.6
CTIA	0.05	40	2
S/H	0.05	40	2
SD-PGA	0.5	1	0.5
ADC	1	1	1
Reference voltage generator	0.3	1	0.3
Digital circuitry	~3 (typical)	1	~3
Total			~16.4

thick transistors for a wide signal swing range. The use of two different supply voltages requires the introduction of an external regulator, and we provide a low-dropout (LDO) regulator with a maximum load current of 10mA. This is supplied with 3.3V by a reference voltage generator.

The current consumption of individual blocks is given in Table 2.2: these are simulation results because there are insufficient pins to identify the supply voltage of every block. The current attributed to DACs includes the pixel driving current. The simulated total current consumption tallies with the measured current. The major consumers of current are the column units, which require a constant current to achieve an acceptable slew-rate. The current consumption of the digital circuitry is typically 3mA, but it can reach 5mA, depending on signal activity. This is smaller than the current consumption of the analog circuitry because the SACL requires few arithmetic operations, and the feedback network for calibration is integrated on the die. The total power consumption of the chip with a 3.3V supply to the LDO regulator was found to vary from 50 to 61mW.

2.5.3 NOISE PERFORMANCE

To confirm that the proposed SACL operates correctly, and to measure its noise performance, we tested the imager on black-body radiation and a real scene, using a reference value of 1550, a DAC output range of $0.2V_{P-P}$, an integration gain of 6×10^{6}V/A from a capacitance of 6pF and an integration time of 40 μs, and a shutter period of 15s.

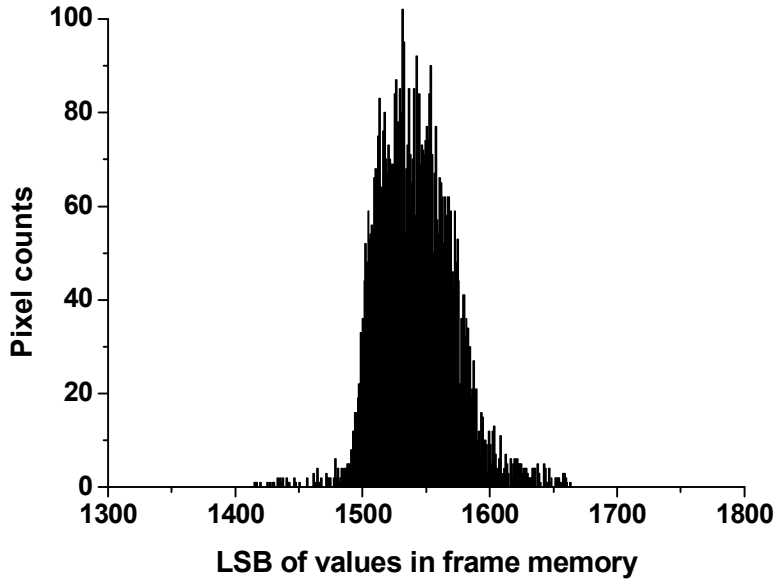


Fig. 2.18 Histogram of LSB of values in the frame memory after the SACL has run.

This DAC output range and the integration gain require a calibration range of approximately ±29% to account for the maximum variation of the manufacturing process. In this scenario, the ideal calibration accuracy is 98.9%.

The histogram in Fig. 2.18 is derived from the data in the frame memory after the SACL has completed its iterations. The x-axis is the LSB at 12-bit resolution and the y-axis is the number of pixels in the 80×82 pixel array. Some bad pixels which are permanently dead, and thus not controlled by the SACL, are excluded from this histogram. The SACL distributes the values in the frame memory around the reference value of 1550, in a range from 1410 to 1665, and so the calibration accuracy is about 93.7%. This

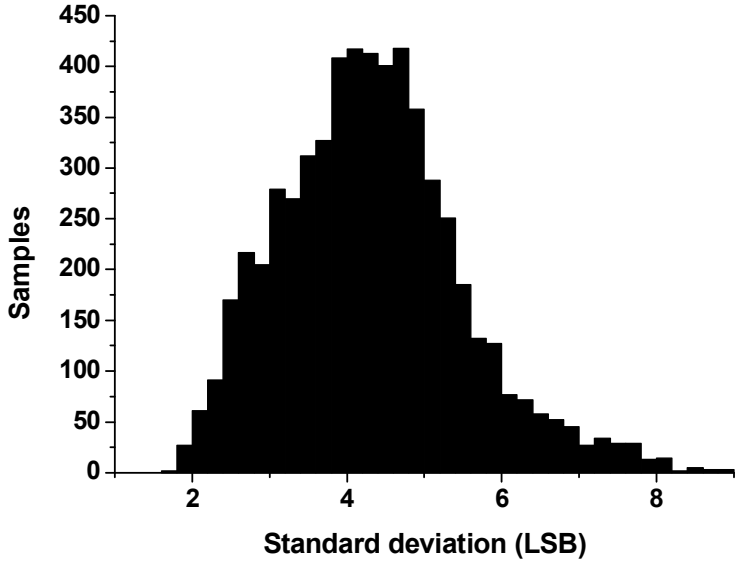


Fig. 2.19 Histogram of standard deviations of each value in the frame memory.

calibration accuracy is acceptable in the context of the effective number of bits (ENOB) of the 9-bit DAC and the effect of extrinsic noise such as supply voltage fluctuations.

The noise-equivalent temperature difference (NETD) is an important metric for an infrared imaging system, which is defined as follows [2.26]:

$$\mathrm{NETD} = \mathrm{LSB_{noise}} \times \frac{\partial \mathrm{T}}{\partial \mathrm{LSB}} . \tag{2.4}$$

Our design has an NETD of 188mK where $\partial \mathrm{T} / \partial \mathrm{LSB}$ is 40mK, and $\mathrm{LSB_{noise}}$ is 4.7. This figure was obtained from a histogram of the standard deviations of each value in the frame memory averaged over 60 frames, as shown in Fig 2.19. We consider that the

major contributors to the NETD are the quantization noise and the thermal noise of ADC because a 12-bit ADC can be expected to be a 10-bit ENOB and the resolution at 10 bits accounts for most of the measured $4.7\mathrm{LSB}_{\mathrm{noise}}$. An NETD of less than 50mK can be expected with a 14-bit ADC (with an ENOB over 12 bits) [2.28]. In addition, since the SACL is independent of the number of pixels and their pitch, higher spatial resolutions can be easily achieved through expansion of memory.

2.5.4 OUTPUT IMAGES

Fig. 2.20 shows an image of a real scene. To process this without the SACL, we set the values in the DAC memory to arbitrary values that have a different calibration range by changing the integration time from 10μs to 40μs and captured the image before the SACL runs again with an integration time of 40μs. The blurred object shown in Fig. 2.20 (a) is obtained by using the initialized values in the DAC memory with an integration time of 10μs. Most of the values in the frame memory will be 0 or 4095 if the all values in the DAC memory are set to the same value. Column-wise FPN is critical because active pixels in the column direction are shared by one blind pixel and one column readout circuit, and there is a mismatch between them. The irregularly distributed dots are the result of spatial FPN. Its dominant source is changed in the resistance of active pixels. The SACL calibrates the array against the column-wise FPN as well as spatial FPN because it modifies the whole readout path, as shown in Fig. 20 (b). Some bad pixels remain, but these can be corrected by the host unit, which also performs color mapping,

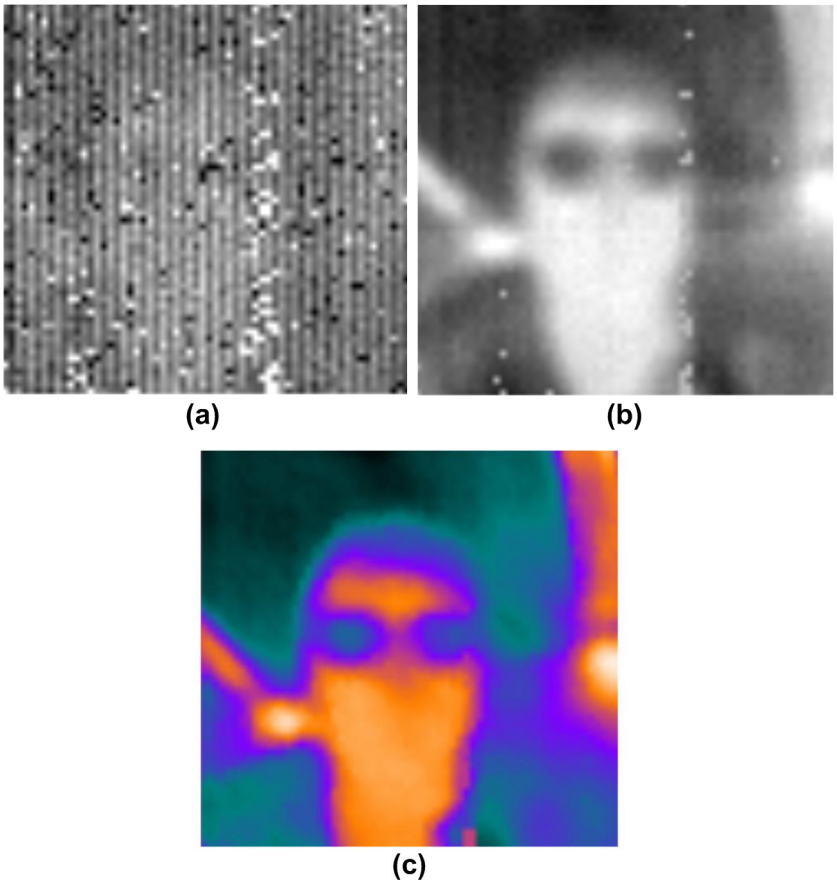


Fig. 2.20 An image captured at 30 fps (a) without the SACL, (b) with the SACL, and (c) with the SACL, and followed by image processing.

with the result shown in Fig. 2.20 (c).

2.6 SUMMARY OF KEY SPECIFICATION WITH PREVIOUS DESIGNS

Table 2.3 shows the key characteristics of the fabricated chip. Table 2.4 compares the performance of our imager with previous designs. A key observation is that our imager does not require off-chip feedback components and has the advantage of automatic control, which increases cost efficiency. Meanwhile, the NETD of our imager is worse than the others because it has the least number of bits, but we contend that there is room for developing this design. In terms of power consumption, it is difficult to compare directly because we include the entire circuit for calibration and others do not. Considering only the analog readout circuits including CTIA, S/H, and pixel current, 100 μW per column in [2.13] is similar to 116 μW per column in ours.

Table 2.3 Summary of design characteristics

Parameter	Values
Technology	0.18 μm 1P5M CMOS
Supply voltage	3.3 V (analog and I/O), 1.8 V (digital)
Active pixels	80 × 82
Pixel size	35 μm × 35 μm
Spectral response	8~14 μm
NETD	188 mK
Frame-rate	1 ~ 120 fps
Clock frequency	1 MHz (analog), Max. 32 MHz (digital)
Interface	EBI, SPI, I2C
Memory	SRAM 9.8 kbyte (for frame memory) SRAM 8.2 kbyte (for DAC memory)
Operating temperature	-20 ℃ ~ 60 ℃
Storage temperature	-50 ℃ ~ 150 ℃
Chip area	4.8 × 4.8 mm^2
Power dissipation	50 mW (typical) 2 μA (power down)

Table 2.4 Key specification with previous designs

PARAMETER		*TNS*'08 [2.10]	*ITA*'12 [2.28]	*ISSCC*'13 [2.29]	*JSEN*'15 [2.12]	*EL*'16 [2.13]	*TCAS-I*'16 [2.15]	This work
Technology		-	CMOS	0.18μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS
Sensor material		PbSe	a-Si	a-Si	TiOx	VOx	DWELL	VOx
Pixel pitch		N/A	17μm	17μm	50μm	17μm	40μm	35μm
Array size		32 × 32	384 × 384	640 × 480	N/A	640 × 512	96 × 96	82 × 80
Calibration	TEC(Thermal Electric Cooler)	N/A	No	No	No	No	No	No
	Shutter	N/A	No	N/A	Yes	N/A	N/A	Yes
	Pixel readout architecture	Current injection	Bias equalization	Differential mirror	Self-bias equalization	Differential mirror	Bias-tunable pixel	Simplified current injection
	Off-chip feedback components	FPGA (94kbytes RAM), 16-bit μcontrollers, 12-bit DAC	Gain table	4-bit offset table	μcontroller, memory, DAC	N/A	FPGA (12-bit DAC, 16Mbits flash memory)	No
	Automatic control	Yes	No	No	Yes	No	No	Yes
A/D conversion		Off-chip 16-bit	On-chip14-bit	No (analog output)	N/A	No (analog output)	No (analog output)	On-chip 12-bit
NETD		N/A	35mK	50mK	<50mK	<40mK (simulation)	N/A	188mK
Power consumption without off-chip feedback components		N/A	<60mW in analog mode, <175mW in digital mode	170mW	N/A	100μW per column (simulation)	100mW	50mW

CHAPTER 3

HIGH-VOLTAGE INPUT SENSOR READOUT CIRCUITRY FOR AUTOMOTIVE CONTROL SYSTEMS

3.1 INTRODUCTION

3.1.1 AUTOMOTIVE CONTROL SYSTEM

The amount of electronics in modern motor vehicles has increased rapidly since the introduction of electronic control units (ECUs) [3.1]. However, the integration of vehicle electronics has reduced costs and increased reliability, but many challenges remain, starting with the choice of system architecture.

As shown in Fig. 3.1, the architecture of an automotive control system can be (a) decentralized or (b) centralized [3.2]. A decentralized system typically contains heterogeneous ECUs, each connected to sensors and actuators which provide related functions. This approach facilitates incremental improvements because a new vehicle

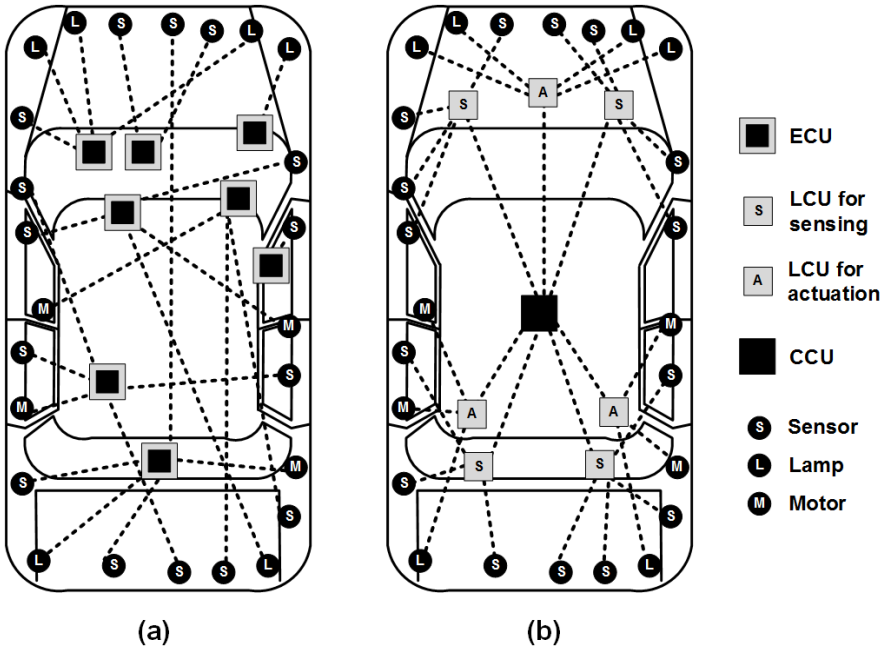


Fig. 3.1 Conceptual diagram of (a) a decentralized and (b) a centralized system architecture in a road vehicle.

function can be implemented by adding a dedicated ECU. However, the successive addition of heterogeneous ECUs increases system complexity, making development, manufacture, and maintenance more expensive. A centralized system avoids these issues to some extent by allowing new functionality to be introduced in the form of software rather than hardware. This advantage has motivated a number of proposals for advanced centralized systems with features such as a central platform computer [3.3] and centralized diagnostics [3.4]. The logical functionality of such a system is provided by a centralized control unit (CCU), in which a powerful microprocessor runs multi-source software [3.5] to process the large amount of data arriving from local control units (LCUs)

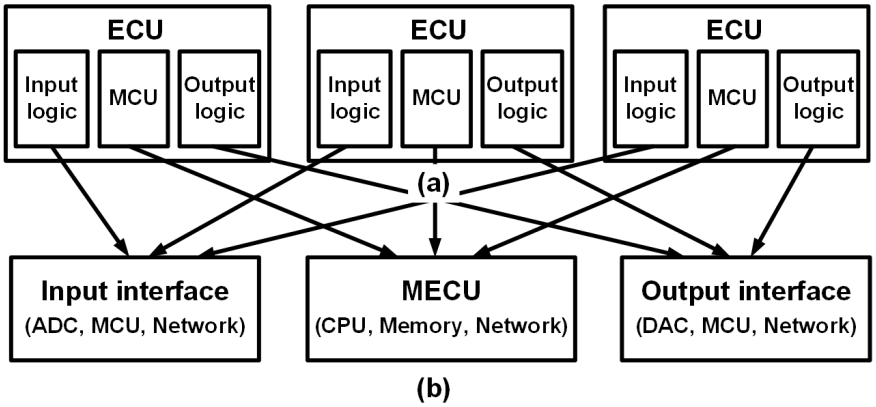


Fig. 3.2 Hardware concept: (a) the decentralized control system and (b) the centralized control system.

distributed across the vehicle, which in turn receive the outputs of sensors and control actuators.

3.1.2 CHALLENGES AND APPROACH

One of the major drawbacks on the centralized control system is additional hardware costs by LCU because they must be a terminal system that can support not only the sensing and actuation function but also control and communication function, as shown in Fig. 3.2. This means a small system with smart features such as flexible and re-configurable function without hardware modifications. The implementation of highly integrated System-on-Chip is a feasible choice to achieve the smart features as well as its cost-efficiency. The sensor readout circuitry for input interface is an obstacle to realizing it. The main cause is that the conventional structure requires many discrete components

on PCB to be individually designed according to the characteristics of the sensor especially. As an example, the level-down resistors are used for reliability of circuits from high voltage over battery level, and those values are determined by the output range and the common-mode voltage of the output of the sensor. This is also because the high-voltage transistors in automotive processes are still suitable for an I/O design rather than the design of logic gates.

An 8-bit microcontroller (MCU) is frequently adequate for an LCU since the main computational load bears the CCU and its software programmable functionality is advantageous for handling various sensors or actuators. The major challenge paved by the increasing requirements demanded by an MCU is the integration of more digital and analog functional modules and the reduction of off-chip cost. Wang et al. [3.6] presented an 8-bit MCU with a controller area network (CAN) controller, a 128 Kbyte flash memory, and a 16-channel 10-bit 1MS/s analog-to-digital converter (ADC) on the same die, but requiring external passive components to protect the MCU from battery over-voltages arriving through sensors [3.7]. Specks et al. [3.8] integrated a bus transceiver for serial communication with a sensor interface to read Hall sensors and mechanical switches, using a high-voltage flash CMOS technology that can provide 40V breakdown devices on the same die as normal 5V normal devices. The latest high-end commercial automotive MCUs simplified system design with the integration of the high-voltage analog IPs such as low- and high-side drivers, voltage regulators, CAN transceivers, and 12V input interfaces for switch monitoring.

However, if the sensor outputs are analog and pulse signals, the approach described

above still requires the use of external components to ensure that these signals are linearly scaled to signals less than 5V. For this linear scale, relatively expensive high-quality passive elements are used. It does not even provide the necessary functions such as gain control and filtering, which are essential for signal processing of these signals.

In this dissertation, we present a fully integrated high-voltage sensor readout circuitry with 8-bit embedded flash MCU, constructed with 0.18μm BCDMOS (bipolar, CMOS, and DMOS) technology. The major contributions are: (1) We integrate the essential building blocks required for the local control unit for the centralized control system into a single chip. It consists of a 32-channel input logic to read the outputs of various multiple sensors, a CAN transceiver of 1Mbps to communicate the MECU, and an 8-bit microcontroller to control and program the input logic and the CAN transceiver. (2) We propose an input interface to reduce external passive components such as resistor and capacitor. This feature is a level-down shifting that directly captures battery-level inputs and low-pass filtering to reduce high-frequency noise on the wiring harness. The LPF uses a capacitance-multiplication technique that permits the size of an internal capacitor to be reduced. (3) We propose a channel control technique to increase channel controllability. Its function enables a different operation for each selected channel. Our circuitry has also an analog front-end (AFE) that allows different common-mode voltage levels, analog gains, and digitization techniques to be applied to each channel.

3.2 ARCHITECTURE

The block diagram of our high-voltage input sensor readout circuitry is shown in Fig. 3.3. This consists of an input interface for sensors, an 8-bit microprocessor and memory for control, a CAN for communication, and peripherals.

The input interface includes a level-shifter to reduce the amplitude of sensor outputs from the battery voltage of 12V to a logical voltage below 3V. A low-pass filter reduces the high-frequency noise produced by the wiring harness. The signals from the sensor are then passed to an analog front-end for digitization. The input interface has 32 channels, one of which is dedicated to an internal temperature sensor used for thermal management [3.11].

The MCU has an 8051-compatible microprocessor with the program, data, and special function register buses. The ability of 8-bit is relatively sufficient in the centralized control system because the MECU is a major operator. The data bus combines the Idata and Xdata segments of the Intel 8051, allowing the use of a single 4 Kbyte SRAM, of which the 256 bytes from 0x0000 to 0x00FF are allocated to Idata, and the 3840 bytes from 0x0100 to 0x0FFF are allocated to Xdata. The 32 Kbyte flash memory allows the MCU to be easily upgraded, and the data is encoded using a Hamming error-correcting code (39, 32) to increase reliability. In addition, a cyclic redundancy check (CRC) can be applied to all the memory buses, and an on-chip debugger is also supported.

The MCU communicates with a CCU over a standard CAN 2.0 with a maximum data rate of 1Mbps [46], [47]. A CAN controller implements the CAN 2.0 protocol, and a

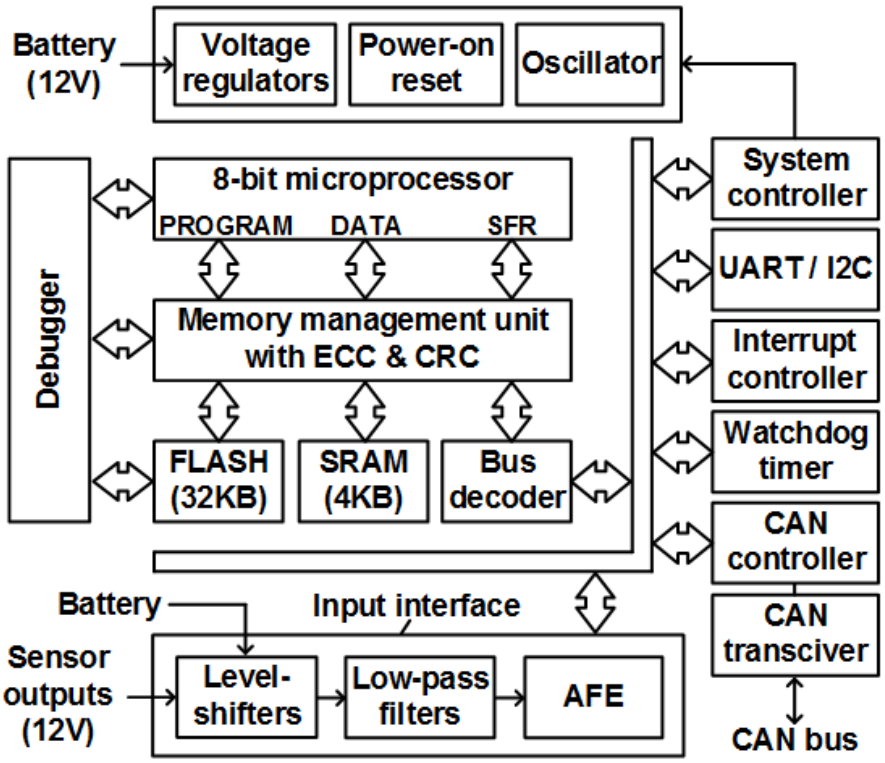


Fig. 3.3 Block diagram of our high-voltage input sensor readout circuitry based on 8-bit flash microcontroller.

CAN transceiver provides an interface between the CAN controller and a physical CAN bus.

The battery is directly connected to voltage regulators which generate 5V for the CAN transceiver, 3.3V for the analog circuits, and 1.8V for the digital logic. A power-on reset ensures that the MCU only operates when the supply voltage is stable. An oscillator provides the 8MHz clock signal for the microprocessor, and lower clocking frequencies are obtained by division. The output of the voltage regulator and the output frequency of

the oscillator can be trimmed by the system controller. The MCU also includes a universal asynchronous receiver-transmitter (UART) and an inter-integrated circuit (I2C) for serial communication to external devices such as a PC, an interrupt controller to manage interrupt signals received from the peripherals, and a watchdog timer.

3.3 IMPLEMENTATION OF SENSOR READOUT CIRCUITRY

3.3.1 INPUT INTERFACE WITH LEVEL-SHIFTER AND LOW-PASS FILTER

The sensor readout circuitry for automotive control units reads various signals coming from sensors in the vehicle. An analog, switch, and pulse signal represents a characteristic of the sensors. The analog signal is used to monitor temperature, pressure, flow rate, air quality, and etc. These sensors can include some electronic circuits for a domain conversion such as resistive-to-voltage and capacitive-to-voltage conversion. The switch signal is used to control mirror, window, truck, ignition, brake, and etc. The sensors are a form of mechanical switches and typically connected into a battery level or ground directly. The on- or off-state for a binary decision is typically determined by the combination with a pull-up or pull-down resistor. The pulse signal is used to sense the speed and position such as vehicle speed sensor, crankshaft position sensor, etc. Its duty cycle or frequency is a determinant for sensor's operation, and its amplitude and shape is varying.

The analog, switch, and pulse signals are preprocessed in an input interface. The conventional input interface [3.7], [3.9] shows in Fig. 3.4 (a). The input interface requires a capacitor $C0$ to cope with sudden surges in voltage. $R1$ and $R2$ are the pull-up and pull-down resistor. The resistor $R3$ limits the current reaching the MCU. A capacitor $C1$ is for passive low-pass filtering of the noise from the wire harness. The resistors $R3$ and $R4$ form a voltage down-shifter.

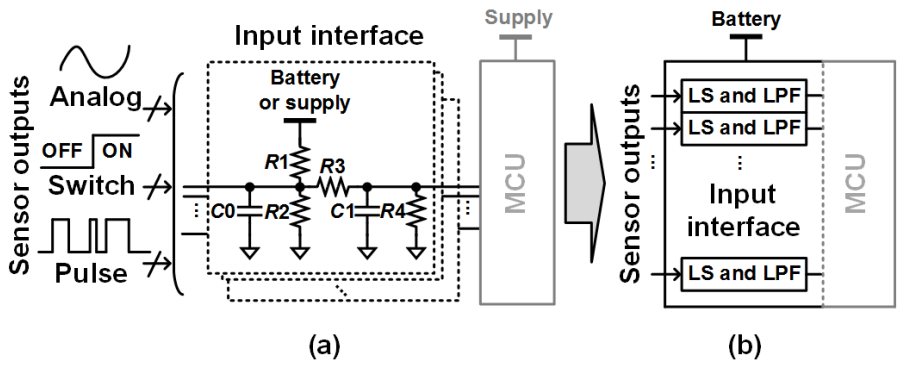


Fig. 3.4 (a) A conventional input interface acquires sensor outputs through discrete components on a PCB. (b) Our on-chip input interface replaces it.

In our readout circuitry, the function of these passive components is performed by an on-chip unit consisting of a level-shifter (LS) and a low-pass filter (LFP) for each channel, as shown in Fig. 3.4 (b).

As a design consideration, the input interface requires a low-pass filter, but the low-frequency range of the output of a typical sensor prevents this from being implemented in silicon because a metal-insulator-metal (MIM) capacitor can only provide a few $\mathrm{fF}/\mu\mathrm{m}^2$. Instead, we use a capacitance-multiplication (CM) technique that utilizes the Miller effect [3.18], [3.19]. Fig. 3.5 shows our capacitor multiplier. This approach is advantageous for inputs with different common-mode DCs because a decoupling capacitor makes "node A" independent.

Fig. 3.6 shows the circuit implementation of the capacitor multiplier, consisting of a single-stage amplifier made up of the transistors $MP1$ and $MN3$, a DC-decoupling capacitor $C2$, and a replica-bias generator comprising $R4$, $MP2$, and $MN7$. The single-

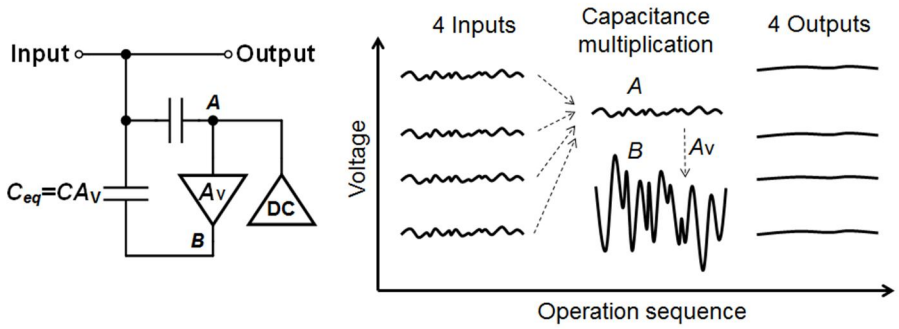


Fig. 3.5 Block diagram and its operation sequence of proposed capacitor multiplier, in which there is an example of 4 inputs with different common-mode DCs.

stage amplifier multiplies the electric charge of $C1$ by its gain. The DC-decoupling capacitor prevents DC from the sensors from reaching the amplifier. A new DC for the single-stage amplifier is generated at the replica-bias generator. The resistor $R4$ allows the gate node of $MP1$ to offer a high impedance to both the AC component of V_{IN} and the DC component generated by $MP2$ and $MN7$. The size of the transistor in the replica-bias generator is the same as that in the single-stage amplifier, and so this scheme always operates in the saturation region. The transistors $MN1$ and $MN5$ form a source follower to increase the bandwidth of the single-stage amplifier. This improves the degradation of the filtering ability at the out-of-band frequency. The CM operation of a channel is activated by the input F_EN. When $LS12V$ and F_EN are both asserted and the gain of the source follower is approximated to 1, the cut-off frequency $f_{3\mathrm{dB}}$ can be expressed as follows:

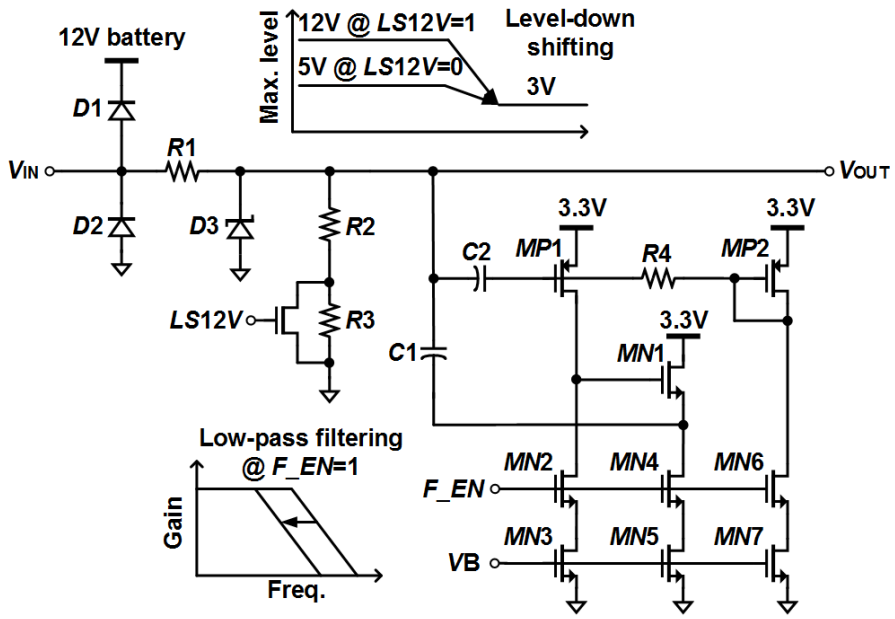


Fig. 3.6 The level-shifter and low-pass filter within our input interface.

$$f_{3\text{dB}} = \frac{1}{2\pi(R1//R2)C1\left(1 + gm_{MP1}(ro_{MP1}//ro_{MN3})\right)}, \tag{3.1}$$

where the symbol '//' indicates that the impedances to be combined are connected in parallel. The variable gm_{MP1} is the transconductance of $MP1$, and ro_{MP1} and ro_{MN3} are the output impedances of $MP1$ and $MN3$. The gain of the amplifier is $gm_{MP1}(ro_{MP1}//ro_{MN3})$.

In this design, the values of $R1$, $R2$, $R3$, and $R4$ are 79.5kΩ, 26.5kΩ, 92.7kΩ, and 35MΩ respectively. Since $R4$ is in the form of a high-pass filter in combination with $C2$, a relatively large value is required to fully receive noise on $MP1$. $C1$ and $C2$ are

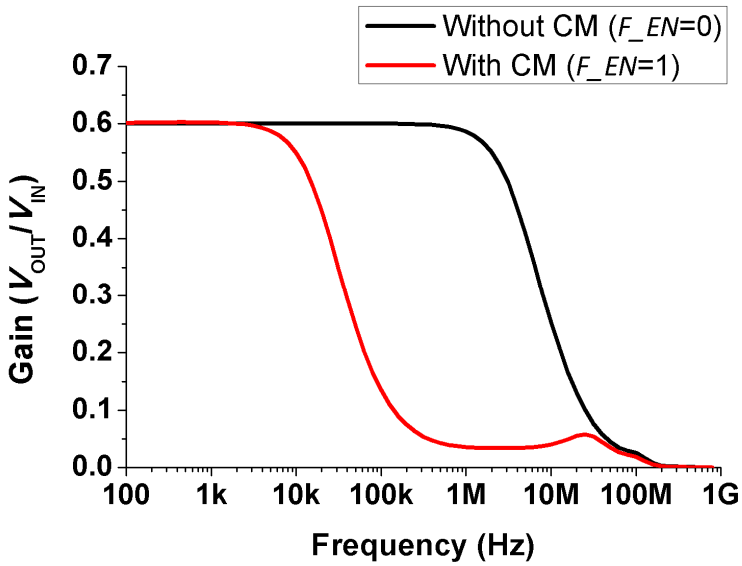


Fig. 3.7 Frequency response of the LPF.

both 2.4pF. The gain of the single-stage amplifier is 50dB. V_B is generated by using a current mirror to copy the current from an internal reference generator, and the drain current through $MN3$, $MN5$, and $MN7$ is 2μA. Fig. 3.6 shows the result of simulating an input interface unit with these parameters. It shows that our CM technique can be expected to reduce f_{3dB} from 3MHz to 10.5kHz. Without the CM technique, f_{3dB} is the result of the resistors $R1$ and $R2$ and the gate capacitances of a multiplexer and a channel buffer to be connected next.

The diodes $D1$ and $D2$ protect the MCU from a battery over-voltage. The resistors $R1$ and $R2$ form a level-shifter to reduce the voltage range of a sensor signal from 12V to the 3V required by the internal logic. The resistors $R1$ and $R2$ also act as a current

limiter and a pull-down resistor respectively. $R3$ is provided for sensors with a 5V readout circuit, and is brought into play when $LS12V$ is low. The Zener diode $D3$ is an additional safety device in case $D1$ does not work, for example, when V_{IN} and the battery have the same voltage behavior. This ensures that the voltage at V_{OUT} does not rise above the breakdown voltage of our Zener diode, 5V.

3.3.2 ANALOG FRONT-END

The main purpose of the analog front-end (AFE) is to digitalize the preprocessed output of the sensor. Traditionally, the analog-to-digital conversion typically is performed by a multiplexed ADC [40], as shown in Fig. 3.8(a). The advantage of this is that the number of ADCs can be minimized. In other words, since the output frequency of the

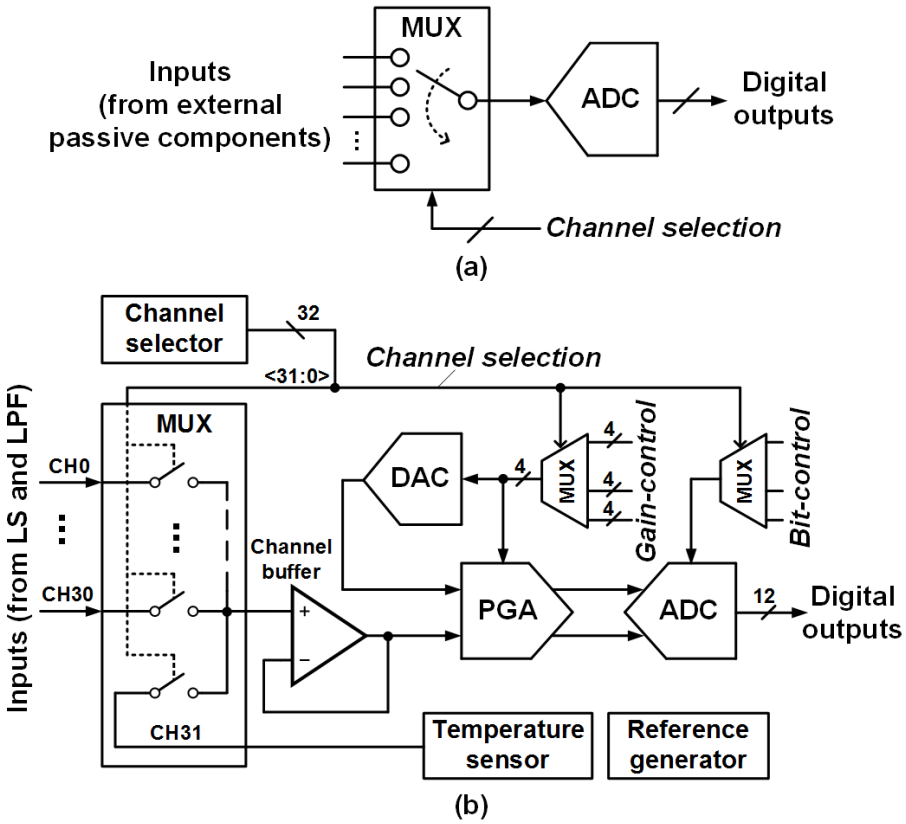


Fig. 3.8 Digitization of sensor signals: (a) conventional structure; (b) proposed analog front-end.

sensor is lower than kHz, it is possible to use a single ADC by selecting a plurality of sensor output signals. The operation is that the reproduced signals from the external components are driven by an analog multiplexer (MUX), and it routes the selected channel to the ADC. To periodically monitor activation of the sensors, a channel selection signal determines which channel is selected.

To make the channel adaptable without adding or adjusting external passive components, our circuit includes various analog building blocks, as shown in Fig. 3.8 (b). The signal flow is illustrated in Fig. 3.9. After the sensor output with a high voltage is compressed by the level-shifter, a channel-selector with an analog multiplexer selects each channel sequentially. A channel buffer sends a charging current to a programmable-gain amplifier (PGA), and a digital-to-analog converter (DAC) provides the PGA with the common-mode voltage of the selected channel, which reduces external components and voltages. The PGA amplifies the output of the channel buffer to match the input range of

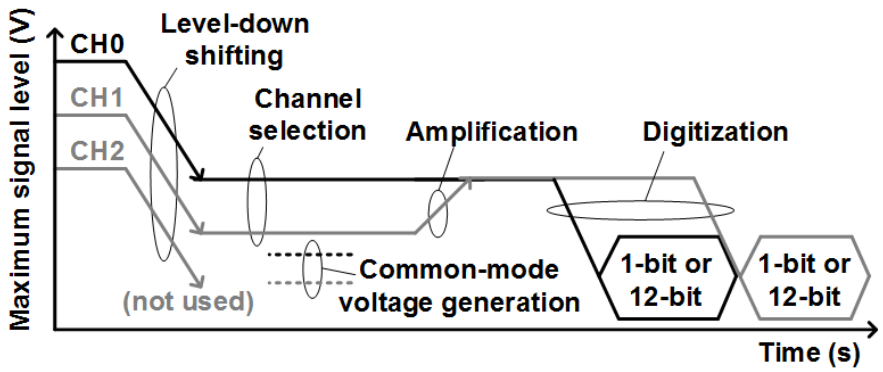


Fig. 3.9 Signal flow.

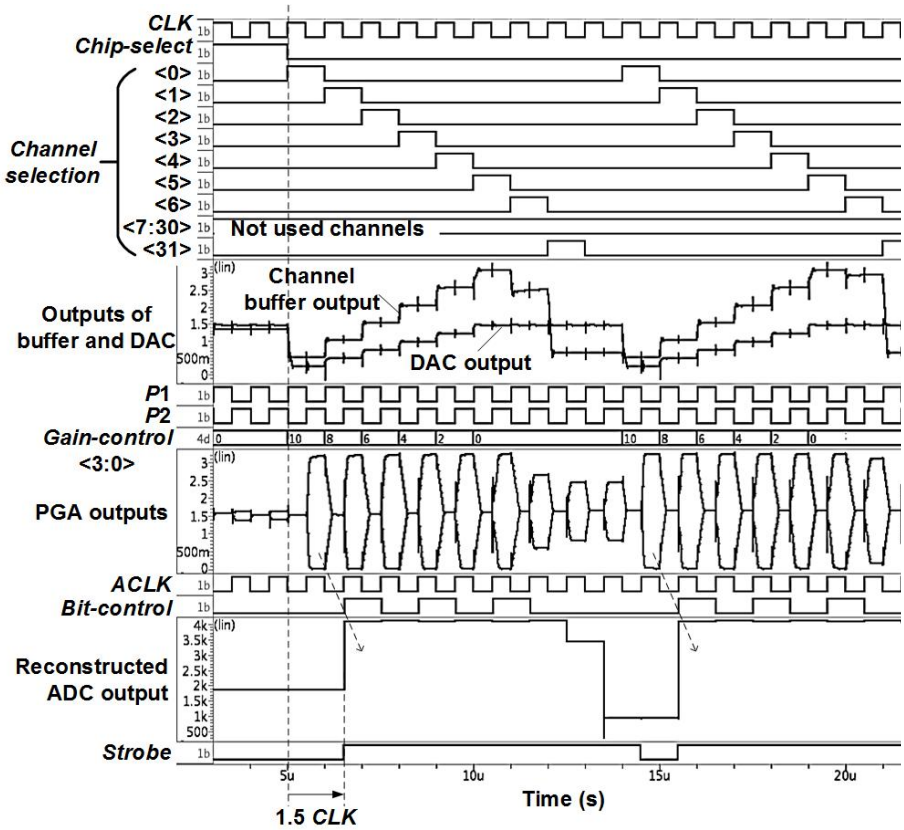


Fig. 3.10 Timing and operation of the AFE.

a 12-bit successive approximation register (SAR) ADC [42], in order to make full use of the resolution of its digital output. This resolution can be reduced to one bit by a bit-control signal, allowing the ADC to process a binary signal in a single conversion cycle. This increases the load on the channel and the MCU.

Fig. 3.10 shows the timing and operation of the AFE, derived from an HSPICE simulation. At a clock frequency of 1MHz, the channel selector operates after the chip-select signal goes low. The input signal is equal to the channel buffer output, which is

one-quarter of the amplitude of the signal reaching the level-shifter. The maximum amplitude of the PGA output of channels from <0> to <31> can be equalized by the gain control signal. $P1$ and $P2$ are non-overlapped clocks for the operation of the PGA. Here, the gain of the PGA of channels from <0> to <5> is set to the full input range of the ADC. The ADC outputs a digital code at 1.5 clock cycles after channel selection. A strobe signal to the MCU confirms the validity of the digital output of the ADC.

3.4 IMPLEMENTATION OF KEY SUB-BUILDING BLOCKS

This chapter explains the implementation of key sub-building blocks, including the circuit details of the analog front-end (AFE) and a CAN transceiver.

3.4.1 CHANNEL SELECTOR

The channel selector is to select the channel to be used. There are two modes; auto mode- and manual-mode. The auto-mode is kind of a user-programmable round-robin fashion and only needs a static selection signal for the used channel. This function would be useful for the LCU without an internal control logic. The manual-mode is controlled by a set of the external register. It needs a change of the register set according to time but has high levels of freedom for the channel selection.

Fig. 3.11 shows the block diagram of the channel selector. In auto-mode, the selection of channels begins with the activation of the signal ACT which is generated by an AND gate with a reset signal RSTB, a chip-select signal CS, and an auto-mode signal AUTO_MODE. With the operation of clock signal CLKi, the starting unit generates a signal of blank and an internal signal FO. If a channel-enable signal CH_EN<0> is high, the scanner unit generates a channel-selection signal for channel<0> by using the signal FO. In other words, the channel controller is in the form of a shift-register that only operates on the active channel. In manual-mode, the operation is simple. A binary-to-thermometer decoder passes the binary signal DIN<4:0> directly to the multiplexer.

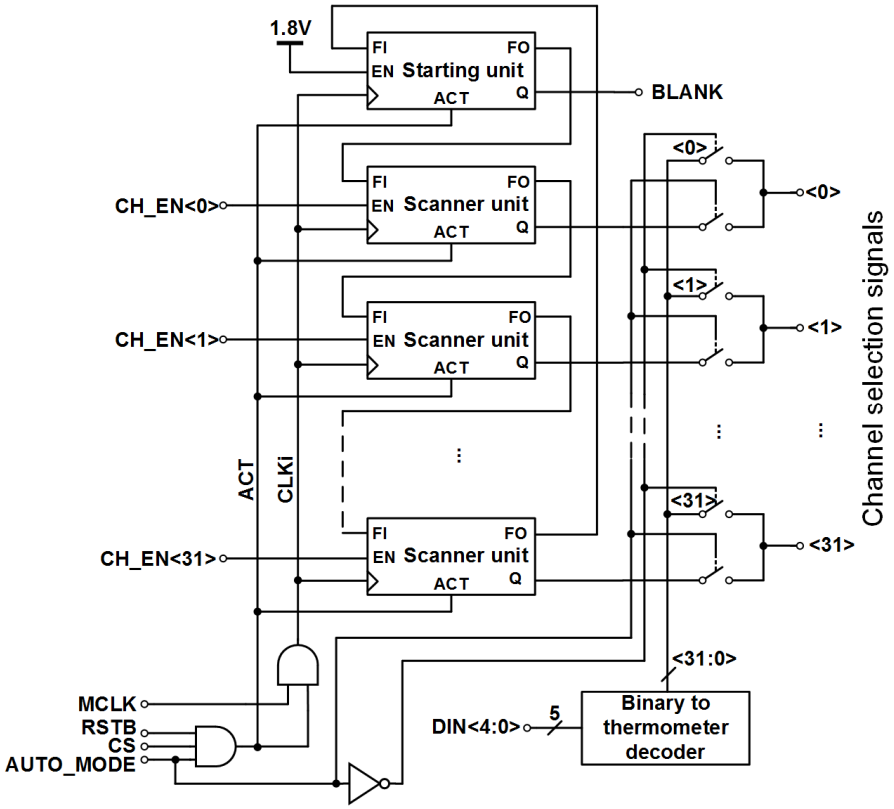


Fig. 3.11 Block diagram of channel selector.

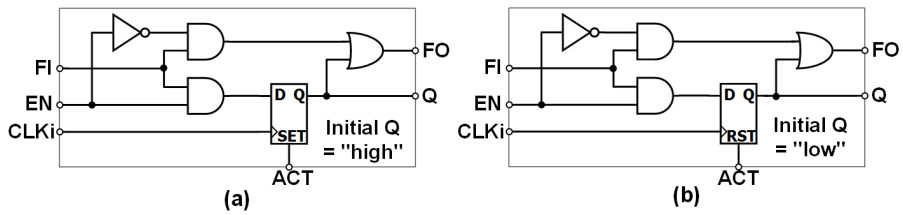


Fig. 3.12 (a) Starting unit. (b) Scanner unit.

The starting and scanner unit consists of some logic gates and a flip-flop as shown in Fig. 3.12. The difference between them is only initial state of the flip-flop. When the signals FI and EN are high, the signals FO and Q are high. When the enable signal EN is low, the output signal Q remains low, and the signal FO keeps going high for the next scanner unit.

3.4.2 CHANNEL BUFFER

In the conventional multiplexed ADC, the charging current required by the internal capacitor is directly injected by the output current of the sensor. If the output current of the sensor is too small to charge its internal capacitor, this can limit a channel conversion-rate. This will be further constrained by the reduced allocation time in the multiple sensors. Therefore, we use a channel buffer providing the charging current to a sampling

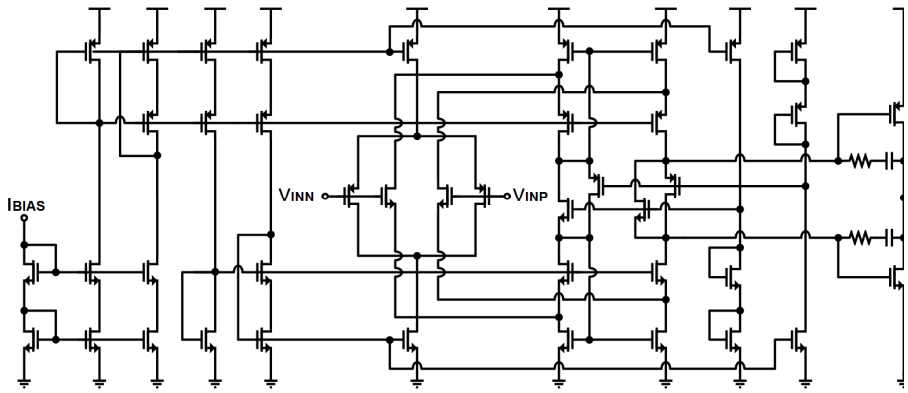


Fig. 3.13 Circuit of the channel buffer.

capacitor of PGA for the reliable operation at 1MS/s 32channels. The channel buffer uses an input/output rail-to-rail amplifier to meet the wide signal range, as shown in Fig 3.13, and its noise performance is designed to be more than 12-bit.

3.4.3 DAC AND PGA

Fig. 3.14 shows the circuit implementation of the DAC and the PGA. The DAC, which consists of a resistor ladder, a 4-to-12 decoder, and two analog buffers, can generate 12 voltages from 0 and 1.5V. The PGA uses a switched-capacitor topology so that its operation can be synchronized with the channel selector and the ADC. The switch

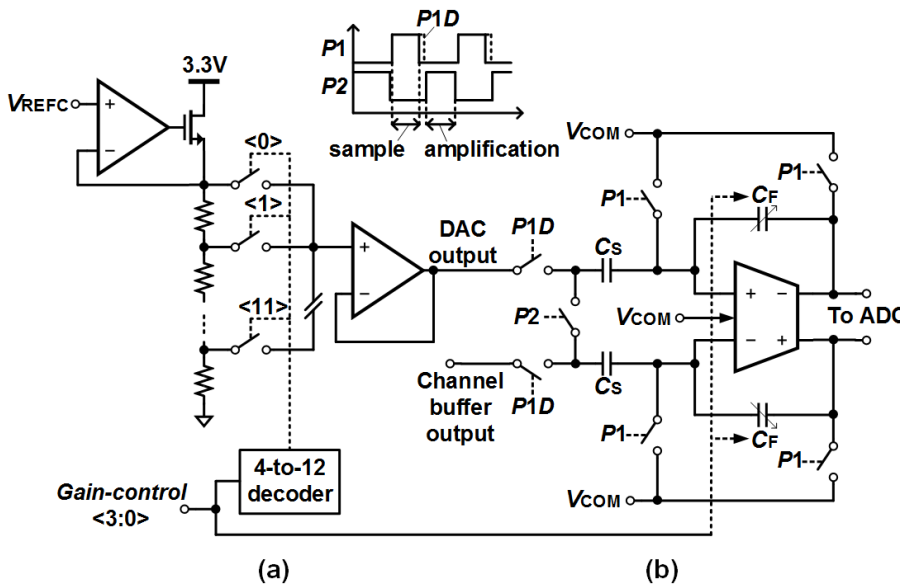


Fig. 3.14 Circuit of the (a) DAC and (b) the PGA.

$P1D$ provides standard bottom-plate sampling, which reduces the voltage offset resulting from charge injection.

Samples of both input signals are amplified as follows:

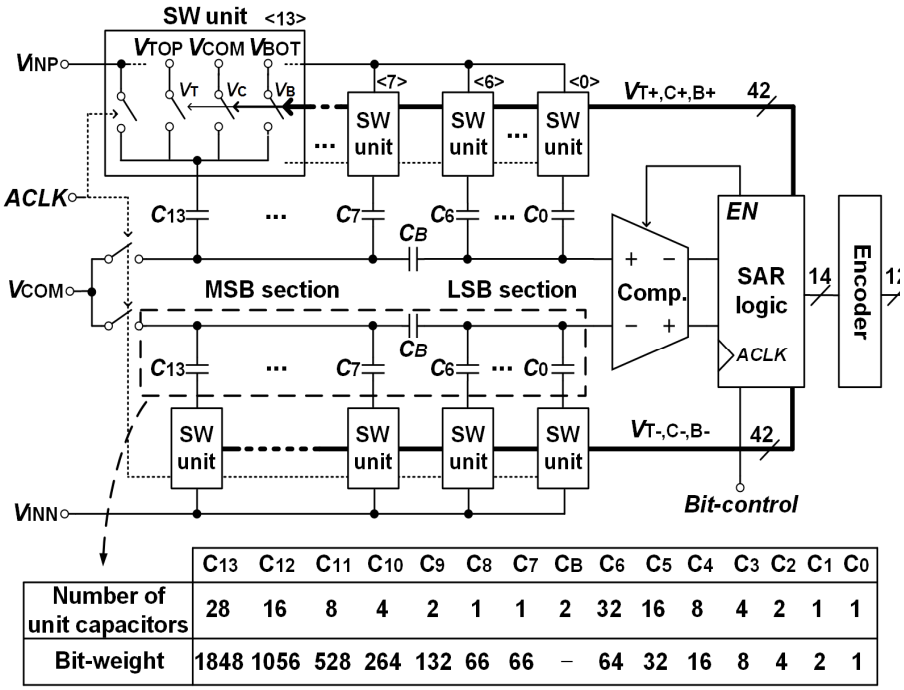
$$A_V = \frac{C_S}{2C_F} \tag{3.2}$$

where C_S is fixed at 2.4pF and C_F can be varied from 100fF to 1.2pF to provide the required gain. The output of the PGA ranges from 0.15V to 3.15V with a common-mode voltage V_{COM} of 1.65V.

3.4.4 ADC

Fig. 3.15 shows the circuit of the 12-bit SAR ADC. The bridge capacitor C_B between the MSB and LSB sections is split to reduce the number of unit capacitors required [13]. Two extra capacitors C_7 and C_8 provide the ability to cope with dynamic errors [14], and therefore the number of A/D conversion cycles for 12 bits is 14 rather than 12. The bit-weight 66 of C_7 and C_8 allows C_B to have an integer capacitance of 2, which avoids the layout issues caused by a fractional capacitance [15]. The bit-weights of the capacitors C_0 to C_6 and C_8 to C_{12} follow a geometric progression with a common ratio of 2. The bit-weight of C_{13} is 1848 instead of 2112, so that the total bit-weight does not exceed 4096

Fig. 3.16 shows the logic of the successive approximation register, which generates



	C13	C12	C11	C10	C9	C8	C7	CB	C6	C5	C4	C3	C2	C1	C0
Number of unit capacitors	28	16	8	4	2	1	1	2	32	16	8	4	2	1	1
Bit-weight	1848	1056	528	264	132	66	66	–	64	32	16	8	4	2	1

Fig. 3.15 SAR ADC.

the control signals V_{T}, V_{C}, and V_{B}, and the signal EN which enables the comparator. The SAR logic, which consists of D-type flip-flop registers that can be set or reset by asserting the S or R inputs high, uses a standard asynchronous topology to eliminate the need for a faster clock than the 8MHz for the microprocessor. Thus the clock signals for all registers come from comparator outputs: the registers connected to V_{C} are clocked by the output of an XOR gate which receives the comparator outputs, and the registers connected to V_{T} and V_{B} are clocked by the output of the registers connected to V_{C}. The A/D conversion cycle is initialized when the set signals $Ready$ and i$Ready$ are

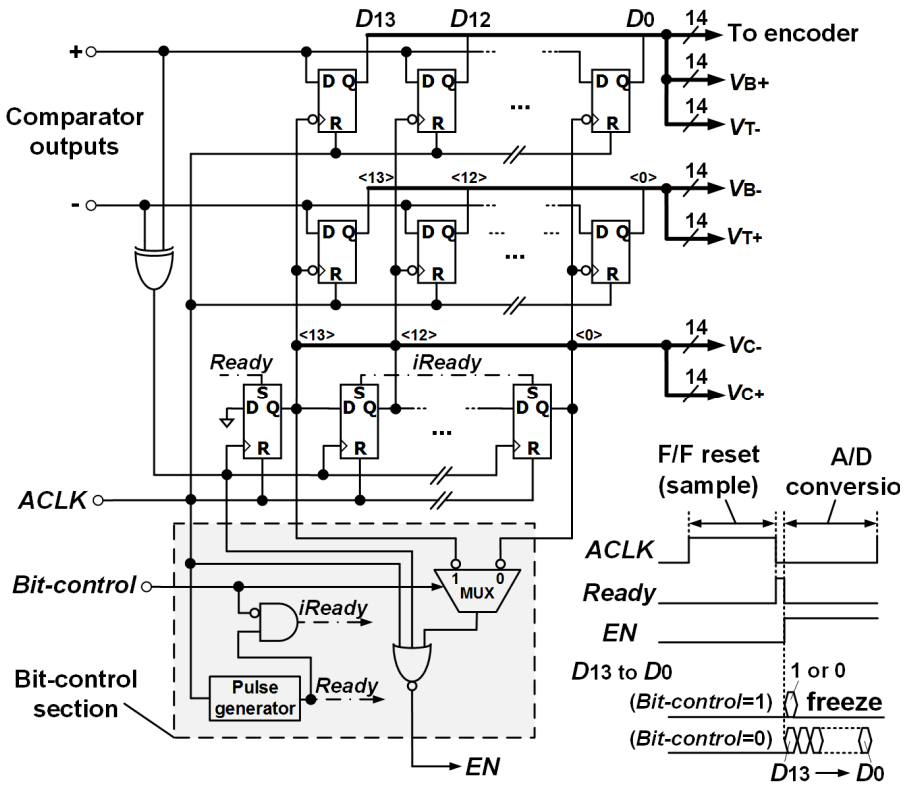


Fig. 3.16 SAR logic.

asserted low. Over the following 14 cycles the comparator outputs D_{13} to D_0 are sequentially stored in the registers connected to V_{T} and V_{B}, where they determine which of the corresponding bit-weights C_{13} to C_0 are applied. Thus the output of the ADC output can be expressed as follows:

$$D_{\mathrm{OUT}} = 1848D_{13} + 1056D_{12} + \cdots + 1D_0\,. \tag{3.3}$$

The single-cycle operation is performed by the bit-control circuit, which controls the set signals $Ready$ and $iReady$, and the EN signal. When the bit-control signal is high, $iReady$ goes low and so the registers connected to $iReady$ are not ready. The comparator is also stopped by EN after its first cycle, freezing the registers connected to D_{12} through D_0. When the bit-control signal is asserted low, both $Ready$ and $iReady$ go high, and all the registers operate as described above.

3.4.5 REFERENCE GENERATOR AND TEMPERATURE SENSOR

Fig. 3.17 shows the block diagram of reference generator and temperature sensor, consisting of a voltage generator, a current generator, a bandgap reference, and a temperature sensor. The voltage generator generates regulated voltages V_{T}, V_{C}, and V_{B} which are 3.15V, 1.65V, and 0.15V. Three amplifiers are used to buffer the sampling capacitors in the ADC. The current generator generates current sources which is used in all amplifiers. The temperature sensor utilizes the temperature coefficient of Q0 with I1.

The bandgap reference is a conventional self-biased scheme based on diode-connected bipolar transistor as shown in Fig. 3.18. The start-up circuit that typically used prevents the self-biasing into zero current at supply ramp-up. The two current bridges including Q3 and Q4 are for the bias voltage of cascade stage in main bridges of Q1 and Q2. Simulation results are in Fig. 3.19.

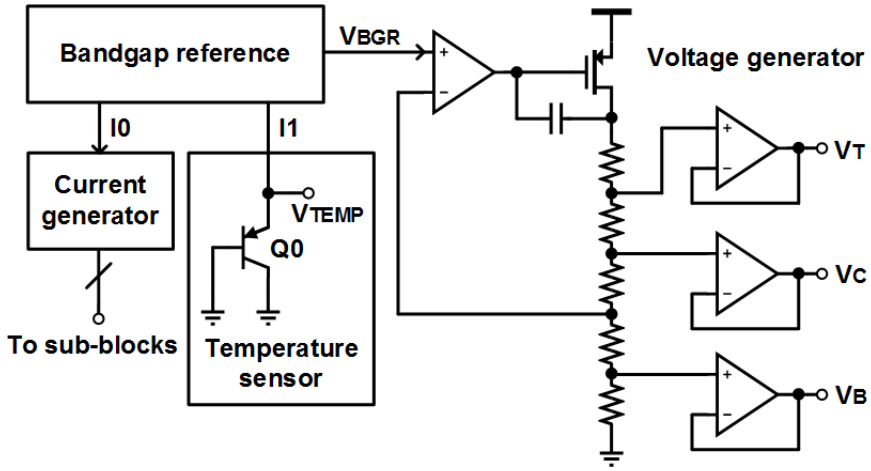


Fig. 3.17 Voltage/current reference generator and temperature sensor.

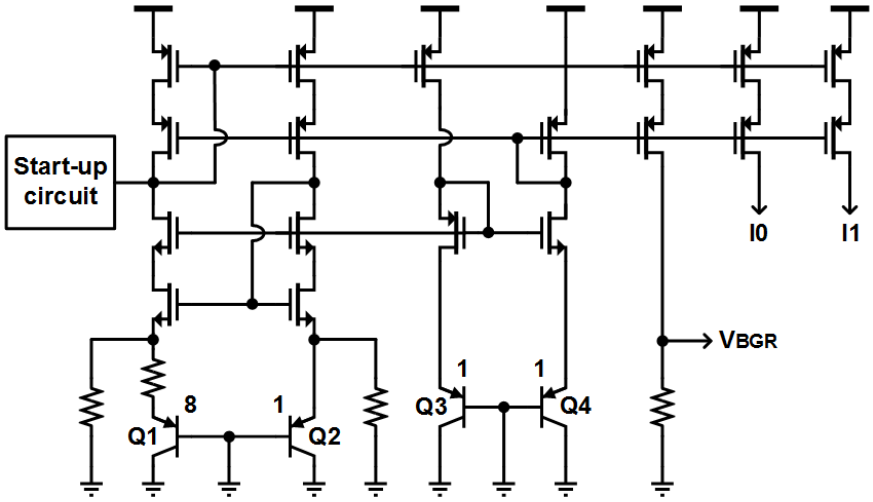


Fig. 3.18 Bandgap reference generator.

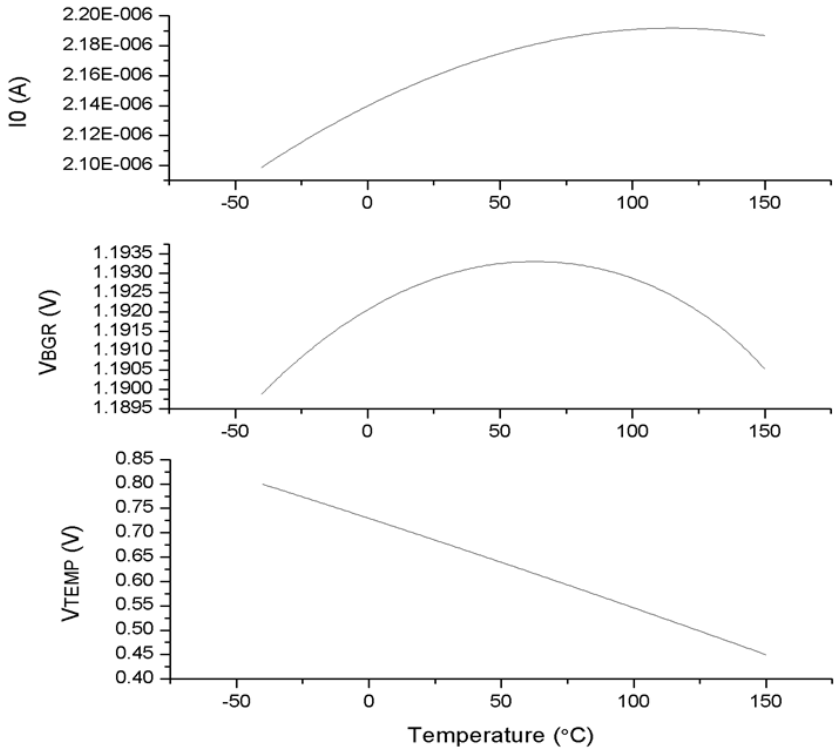


Fig. 3.19 Simulation results of the current/voltage reference generator and the temperature sensor.

3.4.6 CAN TRANSCEIVER

Fig. 3.20 shows our CAN transceiver, which must be able to deal with voltages from -27V to +40V at the output pins of the bus line in order to cope with an automotive environment [3.16]. The fabrication process that we use only provides p-type extended drain MOS (EDMOS) and n-type laterally diffused MOS (LDMOS) transistors. So, we deal with under- and over-voltages with one transistor of each type, together with two diodes $D1$ and $D2$. During high-side switching, the p-type EDMOS transistor is able to

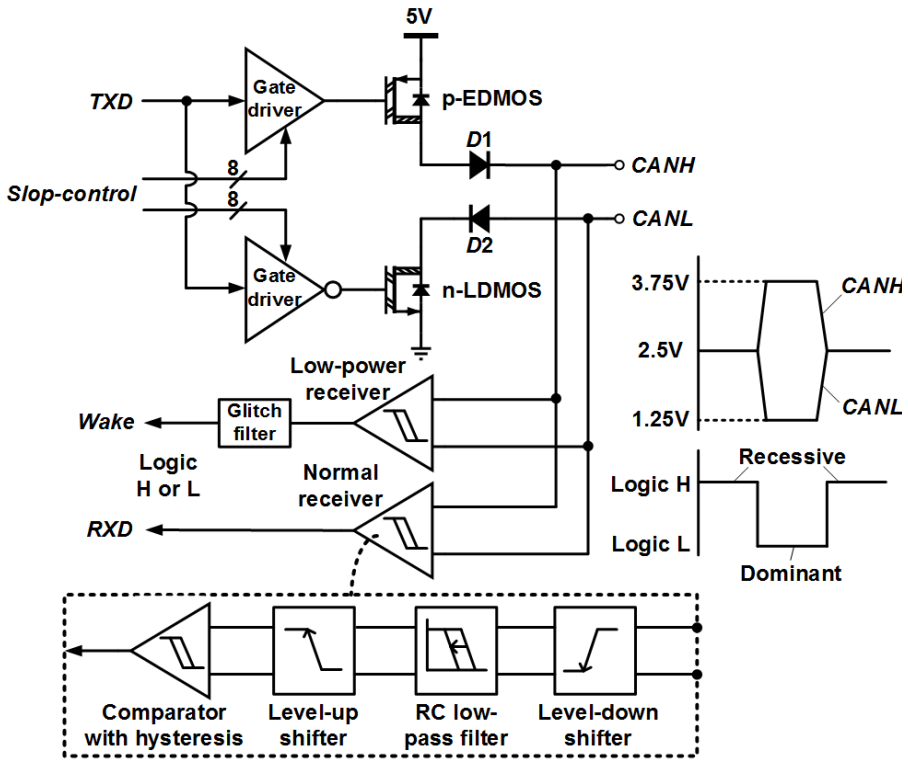


Fig. 3.20 CAN transceiver.

block current flow for negative voltages on the bus line down to -27V; and the diode $D1$ can block bus voltages up to +40V. During low-side switching, the n-type LDMOS transistor and the diode $D2$ operate similarly. We introduce 8-bit slope-control into the gate driver to compensate for the mismatch of slew-rate between EDMOS and LDMOS transistors

After the incoming bus signal has been compressed to eliminate over-voltages, it is filtered to reduce noise. The voltage of the stabilized signal is then shifted upwards to match the input range of the comparator, which converts the differential signals CANH and CANL to a single-ended logic-level signal with a range of 1.8V. The receiver operates either in normal mode or in low-power mode. In normal mode, the CAN transceiver consumes 5mA in the recessive state and 50mA in the dominant state. The consumption of low-power mode reduces to 170μA where the gate drivers are also disabled. The receiver provides a remote wake-up function, as required by ISO 11898-5, which also specifies a filtering time to prevent unwanted wake-up, and so a 1.5μs glitch filter is inserted into the output stage of low-power receiver. The glitch filter uses a counter to delay the receiver output digitally.

3.5 EXPERIMENTAL RESULTS

3.5.1 PROTOTYPE CHIP

A prototype of our MCU was fabricated in 0.18μm 1-poly 5-metal BCDMOS technology. Fig. 3.21 shows the die micrograph with the layout of the input interface. The magnified layout shows the implementation of LS and LPF with our CM technique in a

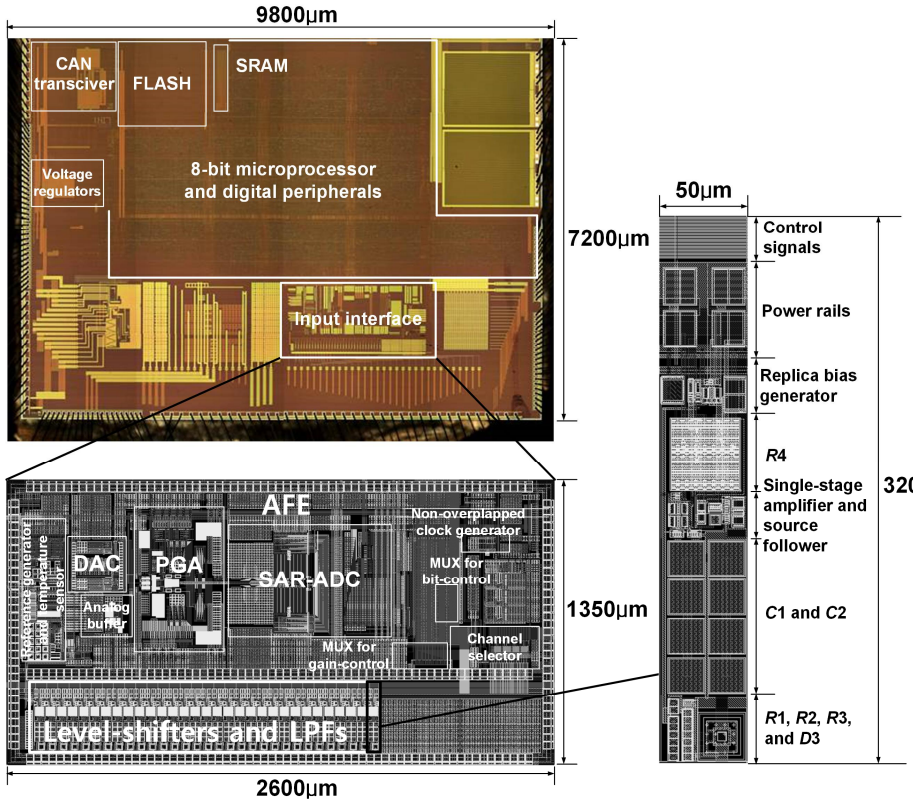


Fig. 3.21 Die micrograph with magnified layouts.

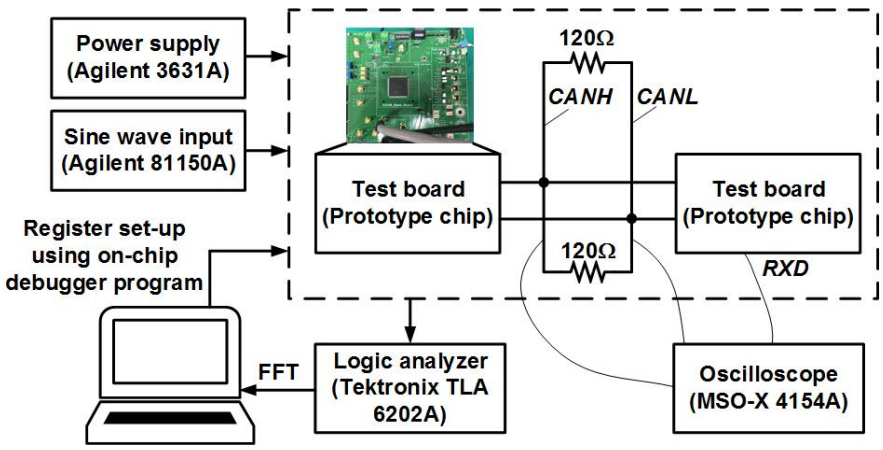


Fig. 3.22 Test environment.

small area. The MCU occupies an area of 9800μm×7200μm, including the I/O pads, the decoupling capacitors, and some test blocks. Fig 3.22 shows the test environment used to evaluate the prototype chip.

3.5.2 FUNCTION VERIFICATIONS

To verify the filtering function of the LPF, we applied a $50mV_{P\text{-}P}$ sinusoid on a 6V DC, in which the sinusoid can be regarded as noise in the current context, to one input channel and observed the reconstructed output waveform of the AFE. Fig. 3.23 shows that this noise is filtered out when the CM technique is enabled. The Nyquist theorem indicates that the *x*-axis cannot extend further than 500kHz.

We tested the channel selection function with multiple inputs by measuring the AFE output with a Tektronix TLA6202 logic analyzer. Fig. 3.24 shows how the output of the

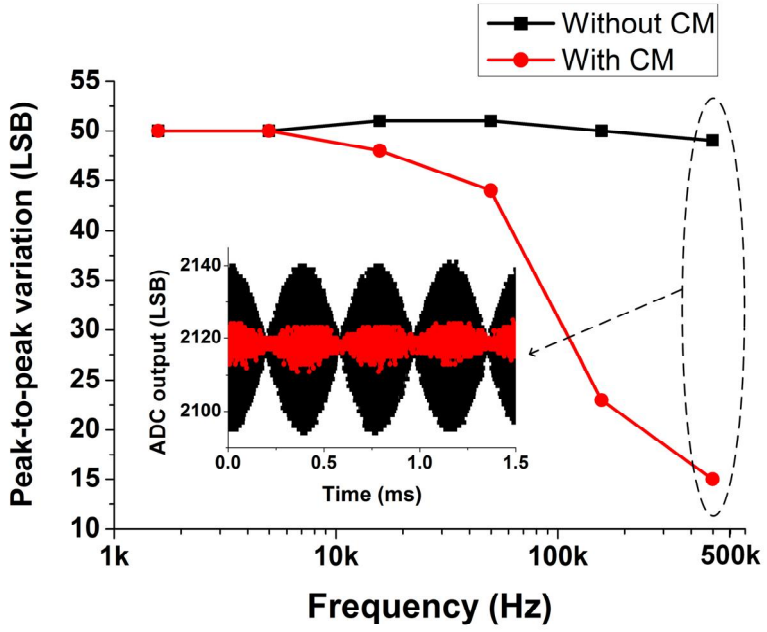


Fig. 3.23 Measured filtering function of the LPF.

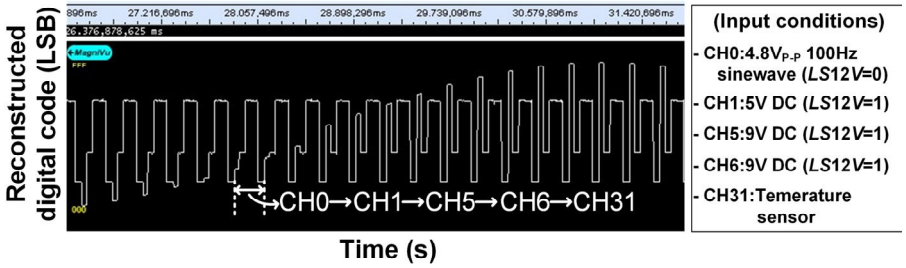


Fig. 3.24 Measured AFE output when five channels are enabled.

AFE cycles through the selected channels. The y-axis is the LSB at 12-bit resolution and represents a 12V input range when $LS12V$ is high. It can be seen that the outputs of the five channels are periodically repeated as expected.

Fig. 25 shows the measured analog output of the temperature sensor. We used the

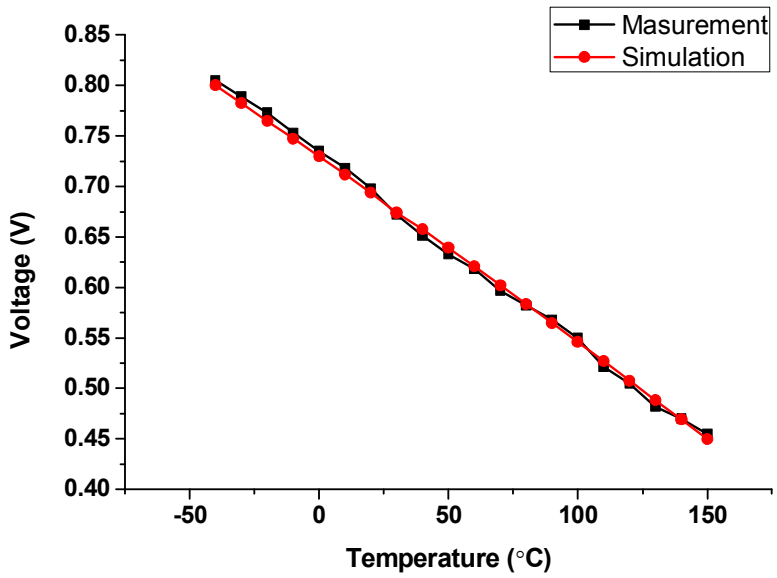


Fig. 3.25 Measured and simulated analog output of the temperature sensor.

analog output instead of the ADC output for a complete comparison with the simulation. The built-in temperature sensor has a Linear -1.84mV/°C scale factor in the range of -40°C to 150°C, and it is confirmed that it operates normally with the non-linearity of 2.65°C compared with the simulation.

We tested the CAN transceiver using the procedure specified in ISO 11898-2. Fig. 3.26 shows the measured waveforms, which were captured by a Keysight MSO-X 4154A Oscilloscope. The twisted-pair formed by CANH and CANL is used as a bus line, with a data-rate of 1Mbps. A 120Ω termination resistor at each end of the bus line is used to match its nominal impedance.

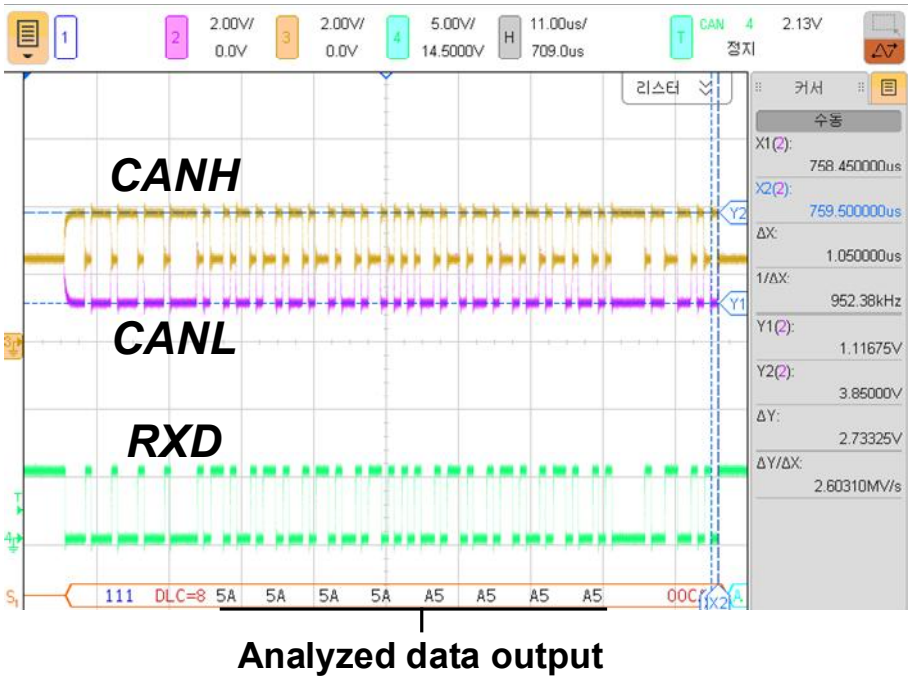


Fig. 3.26 Measured waveforms of the CAN transceiver with the hexadecimal test pattern 5A5A5A5AA5A5A5.

3.5.3 POWER DISSIPATION

The CAN transceiver is major power consumer because it has to inevitably consume 16.7mA at the termination resistor for the dominant state of $2V_{P.P.}$. If the receiver is in dominant and recessive states for the equal lengths of time, the transceiver draws 330mW on average, while the digital circuits draw 36mW and the input interface draws 37.2mW at a 12V supply voltage.

3.5.4 NOISE PERFORMANCE

The signal-to-noise plus distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are used to judge the noise performance of our sensor readout circuitry. Each SNDR and SFDR is derived from the Power Spectral Density shown in Fig. 3.27. Even harmonic tones are due to a single signal path from the level-shifter to the PGA, and white noise is acceptable in the context of the resolution of 12 bits.

The SNDR remains above 60dB up to an input frequency of 20 kHz, as shown in Fig. 3.28. Over a temperature range of -40℃ to 150℃, the measured SNDR is between 61.0dB and 62.5dB, and the SFDR is between 68.1dB and 70.1dB, as shown in Fig. 3.29,

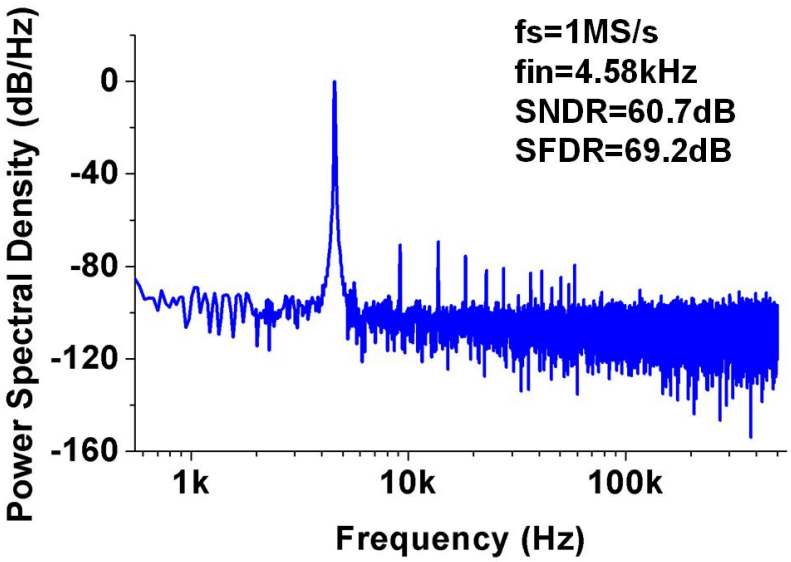


Fig. 3.27 Measured AFE output spectrum with a 4.8V_{P-P} 4.58 kHz sinusoidal input signal.

and therefore the overall temperature variation of SNDR and SFDR is less than 2dB. Fig. 30 shows the measured SNDR against the gain of the PGA, with the SNDR without the

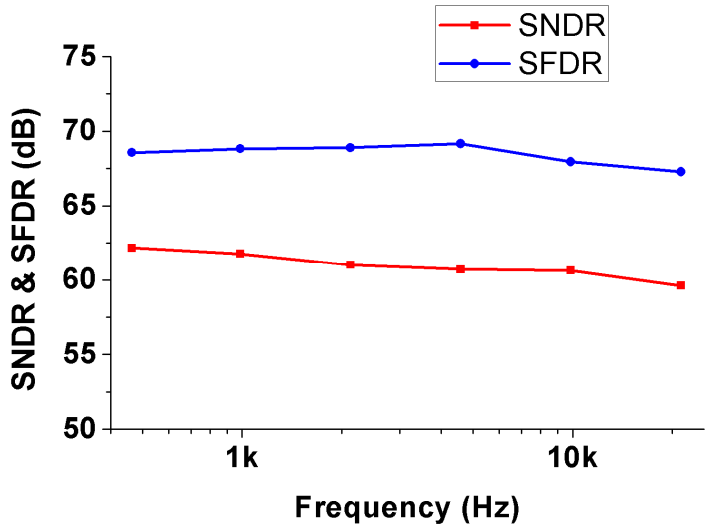


Fig. 3.28 Measured SNDR and SFDR versus input frequency.

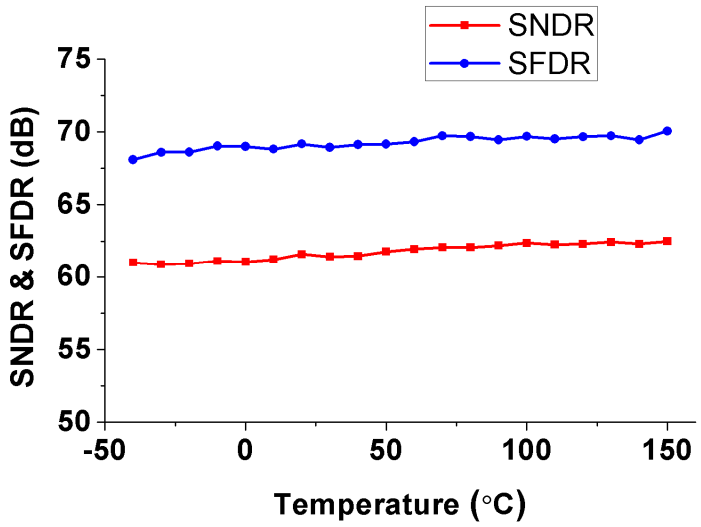


Fig. 3.29 Measured SNDR and SFDR versus temperature.

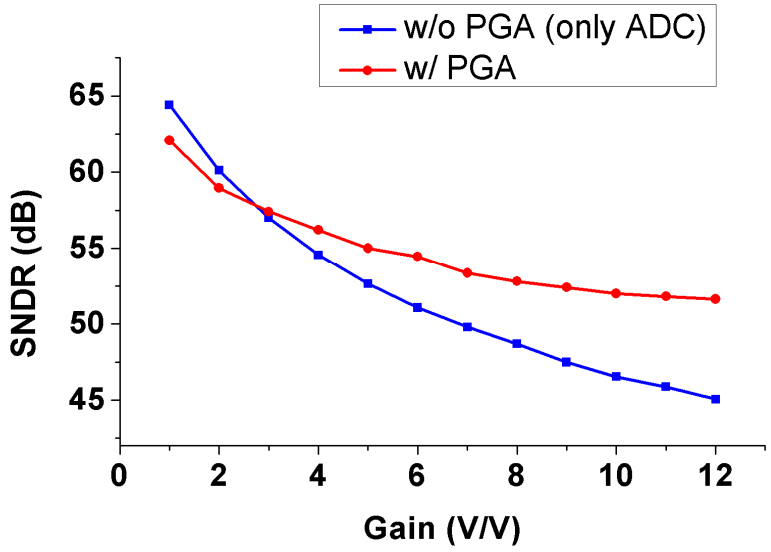


Fig. 3.30 Measured SNDR versus gain of the PGA.

PGA plotted for comparison. Over a range of 1 to 12V/V, the PGA improves the SNDR from -2.2dB to 6.6dB by reducing the ADC's quantization noise. The gain of the PGA in Fig. 27, 28, and 29 are all 1V/V.

The integral non-linearity (INL) and differential non-linearity (DNL) are used to measure the static performance. In Fig. 3.31, a rapid change in the INL in the intermediate code portion is seen. This can be understood as a general profile of capacitor mismatch in segmented CDAC using a bridge capacitor. The maximum INL and DNL were measured as +1.31/−1.69 LSB and +1.46/−0.89 LSB, respectively.

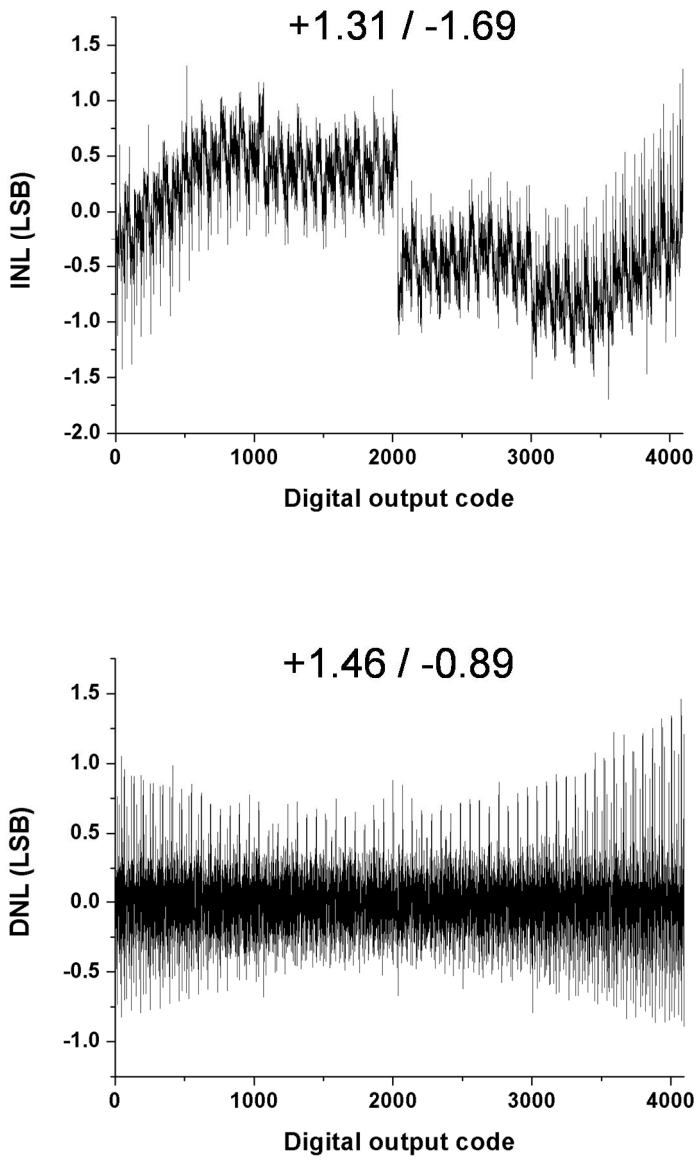


Fig. 3.31 Measured INL and DNL of the AFE output.

3.6 SUMMARY OF KEY SPECIFICATION WITH PREVIOUS DESIGNS

Table I summarizes the key specifications of our sensor readout circuitry and

Table 3.1 Key specifications compared with previous designs

	This work	MC9S12ZVC [3.21]	Wang et al. [3.6]	Specks et al. [3.8]	Murakami et al. [3.20]
Technology	0.18µm BCDMOS	0.65µm HV CMOS	0.18 µm flash CMOS	0.65µm HV flash CMOS	5µm Al gate CMOS
Break-down voltage	52V	40V	-	40V	-
Supply voltage	12V	12V	5V	14V	12V, 5V
CPU	8b 8MHz	32b 32MHz	8b 40MHz	16b 8MHz	No
Memory	32KB flash, 4KB SRAM	192KB flash, 12KB SRAM, 2KB EEPROM	128KB flash, 6KB SRAM 2KB EEPROM	60KB flash, 2KB SRAM, 1KB EEPROM	No
Input range	12V (switch, analog, pulse)	12V (switch), 5V (analog, pulse)	5V	14V (switch), 5V (analog and pulse)	12V (switch, pulse)
Input channels	32	16	16	12 (analog), 4 (pulse), N/A (switch)	6 (switch, pulse)
A/D conversion	12b 1MS/s SAR	12b SAR	10b 1MS/s SAR	10b	1b comparator
LPF	Yes (w/ capacitor multiplier)	No	No	No	Yes (passive RC)
Analog gain	Yes (Up to 12x)	No	No	No	No
Common-mode voltage	Yes (Programmable control)	No	No	No	No
In-vehicle network	CAN with transceiver	CAN with transceiver	CAN, LIN without transceiver	CAN without transceiver, LIN with transceiver	No
Power dissipation	403mW	-	105mW	750mW	-
Temperature	-40°C-150°C	-40°C-150°C	-40°C-125°C	-40°C-125°C	-

compares them with previous designs. A key observation is that our circuitry has a 12V input range about all analog, pulse, and switch signals and has an advantage of the flexibility provided by programmable processing under 32 channels, which can lead to the reduction of production and manufacturing costs.

CHAPTER 5

CONCLUSION

In this dissertation, two types of sensor readout circuitries have been presented; a thermal infrared sensor readout circuitry based on an uncooled microbolometer for automotive night vision systems and a high-voltage input sensor readout circuitry based on an 8-bit embedded flash microcontroller for automotive control systems.

The thermal infrared sensor readout circuitry is based on a fully integrated uncooled microbolometer infrared imager consisting of a 80×82 focal-plane array vacuum encapsulated at the wafer level, a OTP unit, three interface units, an SRAM divided into four groups to improve response, column-parallel readout circuits based on a CTIA with correlated double sampling, a SD-PGA, a 12-bit ADC, a 10-bit DAC, and peripheral circuits including a reference generator, a temperature sensor, and an LDO regulator.

A prototype was fabricated in 0.18-μm CMOS technology for the experiments. The ability of the proposed shutter-based successive approximation calibration loop to calibrate a microbolometer array has been demonstrated by measuring values in the frame memory and by comparison of output images.

The high-voltage input sensor readout circuitry is based on an 8-bit embedded flash

microcontroller consisting of a 32-channel 12V input interface, an 8-bit microprocessor, a 32kB flash, a 4kB SRAM, a 1Mbps CAN transceiver, and analog and digital peripheral circuits, offering lower cost than discrete circuits.

To provide the programmability of input signals, our input interface not only receives battery-level inputs, but also provides analog-specific functions such as low-pass filtering by capacitance multiplication, common-mode voltage control using a 4-bit DAC, gain control using a PGA, conversion cycle control of a 12-bit ADC by using the bit-control section of the SAR logic, and channel selection using multiplexers. The functionality of our MCU has been checked by measuring output waveforms, and spectra obtained from a prototype chip fabricated using 0.18-μm BCDMOS technology.

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한글초록

최근 IT 기술의 발전과 함께 안전주행, 편의 도모, 경제성 및 친환경성의 지속적인 요구가 확대됨에 따라 차량용 전장 시스템의 중요성이 증가하고 있다. 차량용 전장 시스템은 주행 관련 각종 정보를 획득하고 차량 내 각종 전자장치를 제어하기 위해 다양한 센서의 활용이 필수적이고 이를 판독하기 위한 반도체 회로를 핵심 부품으로 한다.

본 논문의 주제는 차량용 전장 시스템을 위한 센서 판독 회로의 설계로 차량 내 사용되는 다양한 센서 중 적외선 야간투시시스템에 사용되는 적외선 열상 센서와 배터리 수준의 고전압 출력을 갖는 센서를 대상으로 한다.

본 논문에서는 적외선 열상 센서의 판독을 위해서 셔터 기반의 축차 비교 보정 루프를 갖는 비냉각식 마이크로볼로미터 적외선 이미지 회로를 제시한다. 적외선 감지를 위한 비냉각 방식이 냉각식에 비해 크기와 소비전력을 줄일 수 있지만, 마이크로볼로미터들간의 불균일성은 복잡한 교정 기술을 필요로 하게 하여 저가의 소형 장치로의 구현을 제한하고 있다. 따라서 본 논문에서는 기존의 보정 방식에서 요구되는 외부 프로세서와 소프트웨어 적용을 위한 보정 테이블의 검출 과정을 제거하고 하나의 칩으로의 집적화 및 자동 교정이 가능한 축차 비교 보정 루프 기법을 제안한다. 80×82 픽셀의 적외선 초점 평면 배열과 판독 회로로 구성된 프로토타입 이미지 시스템을 0.18μm CMOS 공정 기술을 통해 구현하였으며, 실험 결과를 통해 제안하는 축차 비교 보정 루프 기

법이 마이크로볼로미터의 불균일성으로 인한 고정 패턴 잡음을 효과적으로 보상함을 확인하였다.

본 논문에서는 고전압 출력을 갖는 센서의 판독을 위해서 8 비트 마이크로 컨트롤러 기반의 고전압 입력 인터페이스를 제시한다. 소프트웨어 프로그램 기능이 포함된 마이크로 컨트롤러는 다수의 센서를 통합 관리하기에 용이함에 따라 차량용 전장 제어를 위한 핵심 부품으로 사용된다. 비용 절감 및 안전성 향상을 위해 더 많은 디지털 및 아날로그 기능 모듈을 통합이 지속되고 있지만, 여전히 배터리 과전압으로부터 트랜지스터의 보호하고 5V 미만의 신호로의 조정을 위해 위한 외부 수동 소자는 필수적으로 요구된다. 본 논문에서는 제기된 문제의 해결을 위해 배터리 레벨의 입력을 외부 소자 없이 판독하기 위한 32 채널 12V 입력 인터페이스를 제안한다. 또한 외부 소자의 사용을 최소화 하기 위해 1Mbps CAN 트랜시버와 8 비트 임베디드 플래시 마이크로 컨트롤러를 함께 집적하였다. 0.18μm BCDMOS 공정 기술로 제작된 프로토 타입을 통해 -40°C에서 150°C까지 안정적으로 동작함을 확인하였다.

주요어: 자동차, 전장 시스템, 센서 판독 회로, 적외선 이미지, 입력 인터페이스.

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