공학박사 학위논문

Study on uni-directional vertical current in metal-insulator-oxide semiconductor structures

금속-절연체-산화물반도체 적층 구조에서 발생하는 단방향 수직 전류에 대한 연구

2018년 8월

서울대학교 대학원

융합과학부 나노융합전공

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Abstract

Study on uni-directional vertical current in metal-insulator-oxide semiconductor structures

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The technology for electrical current flowing through an insulator thin-film between two electrodes is newly getting spotlights for substantial potentials toward advanced functional devices including a diode and a resistive switching device. However, depending on an electrode-limited conduction mechanisms of the conventional devices, a narrow processing window for a thickness of the insulator thin-film and an inability to control a magnitude and direction of the currents are challenges to overcome. Herein, I propose a new approach to enable electrical charge carriers to pass stably through a relatively-thick insulator layer. In order to pass the electrical charge carriers through the thick insulator film, we controlled the area of the electrode overlapped with the trap sites present inherently in the insulator film and adjusted the defect density in the insulator layer using varying deposition methods. And a magnitude and a polarity of the vertical currents is precisely controlled by applying an oxide semiconductor electrode in a metal /

insulator / metal structure. Moreover, it is also demonstrated that the electrical conduction in the investigated devices follows a space charge-limited conduction (SCLC) mechanism which mainly depends on the charge carriers injected from electrode contacts. Therefore, characteristics of the vertical current including a current value and a rectification ratio of input signal are precisely controlled by electrical properties of the oxide semiconductor electrode. The devices with the uni-directional vertical current flow have proven to work as thin-film diodes and the possibility of replacing the role of conventional diodes in various electronic circuits has been confirmed. The unique vertical current characteristics in metal / insulator / oxide semiconductor structures give extendable inspirations in electronic materials science, even a prominent solution for various technology areas of electronics.

Keywords : oxide thin-film diode, oxide electronics, oxide thin-tilm transistors, oxide semiconductor, thin-film diode

Student Number : 2014-30807

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List of Publications

1. “Direct electron injection into oxide insulator by cathode buffer layer”, E. Lee, **J. Lee**, J.-H. Kim, K.-H. Lim, J. S. Byun, J. Ko, Y. D. Kim, Y. Park, and Y. S. Kim, *Nature Communications* 6, pages 6785 (2015)

2. “Unidirectional oxide hetero-interface thin-film diode”, Y. Park, E. Lee, **J. Lee**, K. -H. Lim, and Y. S. Kim, *Applied Physics Letters* 107, pages 143506 (2015)

3. “Vertical transport control of electrical charge carriers in insulator/oxide semiconductor hetero-structure”, **J. Lee**, K. Yoon, K. -H. Lim, J. –W. Park, D. Lee, N. –K. Cho, and Y. S. Kim, *Scientific Reports* 8, pages 5643 (2018)

4. “Photosensitivity of InZnO thin-film transistors using a solution process”, J. Choi, J. Park, K. –H. Lim, N. –K. Cho, **J. Lee**, S. Jeon, and Y. S. Kim, *Applied Physics Letters* 109, pages 132105 (2016)

5. “Conduction mechanism change with transport oxide layer thickness in oxide hetero-interface diode”, B. –i. Nam, J. S. Park, K. –H. Lim, Y. –K. Ahn, **J. Lee**, J.-W. Park, N. –K. Cho, D. Lee, H. –B. –R. Lee, and Y. S. Kim, *Applied Physics Letters* 111, pages 053506 (2017)

6. “Strong influence of humidity on low-temperature thin-film fabrication via metal aqua complex for high performance oxide semiconductor thin-film transistors”, K –H, Lim, J. –E. Huh, **J. Lee**, N. –K. Cho, J. –W. Park, B. –I. Nam, E. Lee, and Y. S. Kim, *ACS Applied Materials & Interfaces* 9, pages 548-557 (2017)

7. “Systematic study on effect of precursors and solvents for optimization of solution-processed oxide semiconductor thin-film transistors”, K. –H. Lim, **J. Lee**, J. –E. Huh, J. Park, J. –H. Lee, S. –E. Lee and Y. S. Kim, *Journal of Materials Chemistry C* 5, pages 7768-7776 (2017)

Chapter 1. Introduction

1.1 Conduction in dielectrics

The metal / oxide / semiconductor (MOS) structure is a key component in most electronic devices. It forms a core part of a metal / oxide / semiconductor / field effect transistor (MOSFET) or thin-film transistor (TFT) that is used as the essential unit in all electronics. Therefore, the development of a MOS device is very important to realize high performance integrated circuits (ICs). Research on MOS devices has been very active over the past decades and has led current IC technologies [1]. The MOS device consists of an oxide layer, which is mainly dielectric material, sandwiched between a metal contact and a semiconductor film. The MOS device is operated by controlling the electrical charge state of the semiconductor layer in response to the voltage applied to the metal electrode; thus it is very important to control the interface state with the oxide film [2-4]. An electric field induced by the voltage applied to the metal electrode should be effectively transferred to the semiconductor interface, and the oxide layer should be effectively polarized in response to the applied electric field. Thus, the most oxide layer of the MOS device is effective and stable dielectric materials. Most dielectric materials used as the oxide layer in the MOS device have good electrical insulating property in which the energy band gap is large and the electron affinity is very low. However, many dielectric thin-films used in electronic devices often permite leakage currents, which can have serious effects on the performance and durability of the device and must therefore be accurately identified and controlled.

In typical insulator materials, valence bands are fully occupied and conduction bands are almost empty. Especially, at 0 K, the conduction bands are completely empty. Therefore, there are no electrical charge carriers that contribute to electrical conduction and electrical conduction through insulator film is negligible. As the temperature rises, electrical current increases by excited electrons and generated holes, but the contribution of the excited carriers to the electrical current is limited at a very low level so the current remains at a very low level [5, 6]. Consequently, the dielectric films and the insulator films have been mostly used to block transportation of electrical charge carriers between the metal and the semiconductor layer in the MOS device. On the other hand, when a large electric field and a high thermal energy are applied to a dielectric film, the electrical current through dielectric films is noticeably increased. The electrical conduction in dielectric films depends on various conduction mechanisms by the applied condition. Identifying the conduction mechanism through the dielectric films is very important in controlling the current. Therefore, it is important to define the relationship between the thermal energy and the electric field on the electrical current in dielectric films.

The conduction mechanism in dielectrics has been investigated by many researchers for decades. The conduction through the dielectrics is divided into two major categories depending on whether the main factor influencing conduction is the quality of dielectric film itself or the energy barrier to a contact. The first conduction mechanism is an electrode-limited conduction, which is unaffected by dielectric material properties, and the other mechanism is a bulk-limited conduction, which is highly dependent on the material properties of the dielectric

itself (Figure 1.1). Because the electrode-limited conduction is hardly affected by an electrical property of dielectric film, the injection of charge carriers from the contact is most important. There are conduction mechanisms in the electrode-limited conduction mechanism [7-11]: Schottky (or thermionic) conduction, Fowler-Nordheim (F-N) tunneling conduction, and direct tunneling conduction [12] (Figure 1.1a). Most dielectrics have low electron affinities and large energy band gaps. Therefore, an energy barrier exists at the junction interface with a contact. In order to jump over the energy barrier, the electrons in the contact material should get sufficient energy. And the excited electrons are injected into the conduction band of the dielectric material. This conduction is called Schottky conduction or thermionic conduction. Thus sufficiently high thermal energy is required to launch the charge carriers into the conduction band of the dielectric films in the Schottky conduction. However if the acquired energy of the electrons is not sufficient to overcome the energy barrier height at the contact junction, the charge carriers cannot contribute the electrical conduction and the electrical current flows hardly. On the other hand, when the thickness of the dielectric film is less than 10 nm, the charge carriers can be tunneled by quantum effect from the metal Fermi level into the conduction band of the dielectric material. In these conduction mechanisms, Fowler-Nordheim (F-N) tunneling conduction occurs when the external electric field is sufficiently large. In the F-N tunneling conduction, the effective thickness of the dielectric film which electrons in the contact metal pass through becomes thinner in a triangular shape by a sufficient electric field. Thus the reduced effective thickness of the dielectric film facilitates the tunneling conduction of electrons. Meanwhile, the F-N tunneling conduction hardly occurs when the

external electric field is small, but the thickness of the dielectric film is reduced to 10 nm or less so that electrons can be tunneled directly through the dielectric layer. This conduction is called direct tunneling conduction. Because the tunneling conduction mechanisms are due to the quantum tunneling effect, the effective thickness of the dielectric film should be less than 10 nm.

On the other hand, the bulk-limited conduction mechanism is governed by the material properties of the dielectrics. Especially, the status of trap sites existing in the dielectric layer is most important factor. Thus, the energy level of the trap sites in the dielectrics governs the bulk-limited conduction. There are conduction mechanisms in the bulk-limited conduction mechanism [12, 13]: Frenkel-Poole (F-P) conduction, hopping conduction, and space charge-limited conduction (SCLC) (Figure 1.1b). If the electrons trapped in trap sites inside the dielectric film get thermal energies, the electrons are thermally excited and jumped into the conduction band of the dielectric material. This conduction mechanism is called Frenkel-Poole (F-P) conduction. This conduction is similar to the Schottky emission. Alternatively, if the electrons do not get enough energy to overcome the energy barrier at the trap site, the electrons can be tunneled to the adjacent trap site. This conduction is called hopping conduction. In the hopping conduction, the energy potential of the trap site as well as the distance between adjacent trap sites is also important factor. Unlike the F-P conduction and hopping conduction, the space charge-limited conduction is caused by charge carriers injected from contacts into the dielectric film. The injected charge carriers from the contacts firstly fill up the trap sites, then a space charge is generated. When the injection becomes very strong, the space charges build up and the trap sites are almost filled up.

Consequently, the Fermi level of the dielectric layer nearly reaches to the conduction band minimum level, which leads a number of mobile electrons.

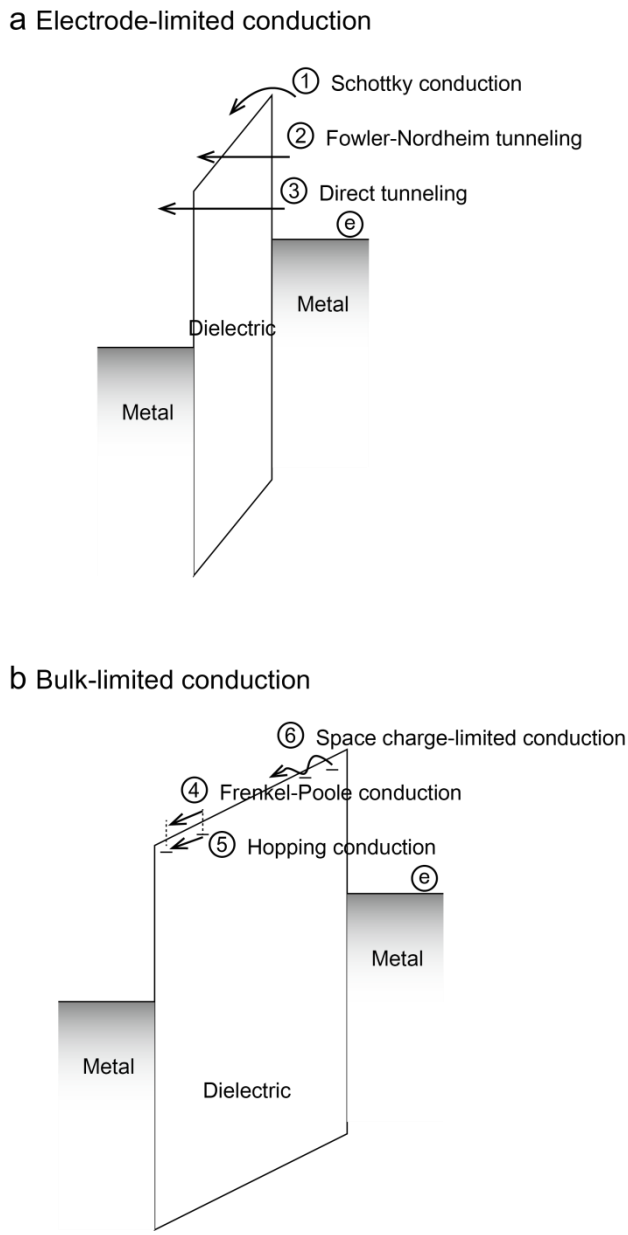

Figure 1.1. (a) Schematic image of the electrode-limited conduction mechanism. (b) Schematic image of the bulk-limited conduction mechanism.

1.2 Devices utilizing current through a dielectric film

In recent years, devices that utilize the electrical conduction flowing through dielectric films have been intensively studied. Metal-Insulator-Metal (MIM) diodes using a quantum tunneling effect or resistive switching memories using a conductive path are typical devices [14].

1.2.1 MIM diode

The MIM diode is consisted of ultrathin dielectric film positioned between two metal electrodes. The thickness of the dielectric film is a very important factor in the MIM device. The thickness of the dielectric film should generally be thinner than 10 nm because it must be thin enough to cause a quantum tunneling effect. In the MIM diode, the electrons are transported instantaneously to opposite electrodes in response to applied electric field. Therefore, in general, the electrical current in the MIM diodes flow symmetrically in both directions, which means that there is little deviation between the forward current and the reverse current. In order to increase the deviation between the forward current and the reverse current, many studies have been carried out to increase the work function difference between the electrodes or to stack two or more dielectric thin-films [15]. However, the electrical current in the MIM diode theoretically follows the tunneling conduction mechanism so that there is a fundamental limitation that it is very difficult to control a deviation or a magnitude of the current in the MIM devices.

1.2.2 Resistive switching device

A resistive switching (RS) device is also operated by an electrical current through a

dielectric film between two electrodes. In most RS devices, mobile charge carriers move through a conducting filamentary path formed in the dielectric thin-film, and therefore, the initial electroforming, which is the set process of forming the conducting filament by dielectric breakdown, should be performed. After the set process, the conducting filament connects both the top and bottom electrodes resulting in a low resistance state. The electrical current in a low resistance state follows an Ohmic conduction. Then, the conducting path is disconnected by an applied reset voltage and the RS device is changed to a high resistance state. The set and reset operations change the connecting state of the filament and leads to a transition between the low and high resistance states [16-18]. Therefore, the electrical current in the RS devices flows in both direction, and it is hard to control sophisticatedly the direction and magnitude of the current.

Meanwhile, recent studies on the leakage current through a dielectric layer demonstrate that higher defect density in a dielectric film causes a significant increase of leakage current [19, 20]. Therefore, it is expected that the current will flow steadily through the thick dielectric film as the possibility of injecting electrons into the trap sites in the dielectric film increases. In chapter 2, new conduction mechanism through a relatively-thick insulator layer is proposed. In the proposed conduction mechanism, the current is due to the injected electrons from the contact electrode into the trap sites in the dielectric layer. Therefore, increasing the density of the trap sites to which electrons can be injected is a key factor in this conduction. The electrical conduction is controlled by the injected electrons, so the magnitude and direction of the current is well controlled by using a semiconductor electrode. In chapter 3, an interference of the new electrical conduction on a

performance of oxide TFT is investigated. The bottom gate structure TFT is based on a MOS structure; thus, the electrical current through gate dielectric layer can affect the output current of the TFT. Moreover, because the interference can seriously affect the interpretation of the TFT device capability, it is very important to verify the influence of the current.

1.3 Role of thin-film diodes as ESD protection component

Thin-film diodes are electronic devices that are used as a very critical component in various electronic circuits. The most important role of thin-film diodes is to control current flow by mainly flowing current in only one direction. As a result, it is used as a core component of various electronic circuits in combination with a switching element. Electrostatic discharge is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. Electrostatic discharge is commonly caused by contact between materials or interference with devices in industry. Recently, ESD prevention circuits have become very important for improving the manufacturing yield and reliability of devices due to the increasingly complexity of circuits integrated in display panels and memory devices [21]. Especially, switching devices including TFT and MOSFET, which are the most important driving components in all electronic devices, are more vulnerable to ESD damage due to their increasing operating voltage. Therefore, the switching devices should be connected to ESD protection circuit in parallel in order to prevent ESD damage. Generally, a diode circuit is applied as the ESD protection component in thin-film technologies

because diode devices permit even more electrical current than the transistors (Figure 1.2). Thus, when the current flowing between the drain and the source electrode through the TFT is within the range allowed by the active semiconductor layer, the current stably flows through the TFT. However, if an overcurrent suddenly flows beyond the allowable range of the TFT, current will be discharged to the ground through the ESD protection diode (Figure 1.2a). In order to fabricate ESD protection diodes, stable P-N diodes are required. However, it is very difficult to implement ESD protection circuits with P-N diodes in the display panel industry where there is no stable p-type semiconductor. Therefore, an n-channel MOSFET with the gate electrode connected to the drain or source electrode is mainly used as the ESD protection diode. The connected n-channel MOSFET acts as a nonlinear resistor, so that the device can be used as a load device like a conventional diode device (Figure 1.2b).

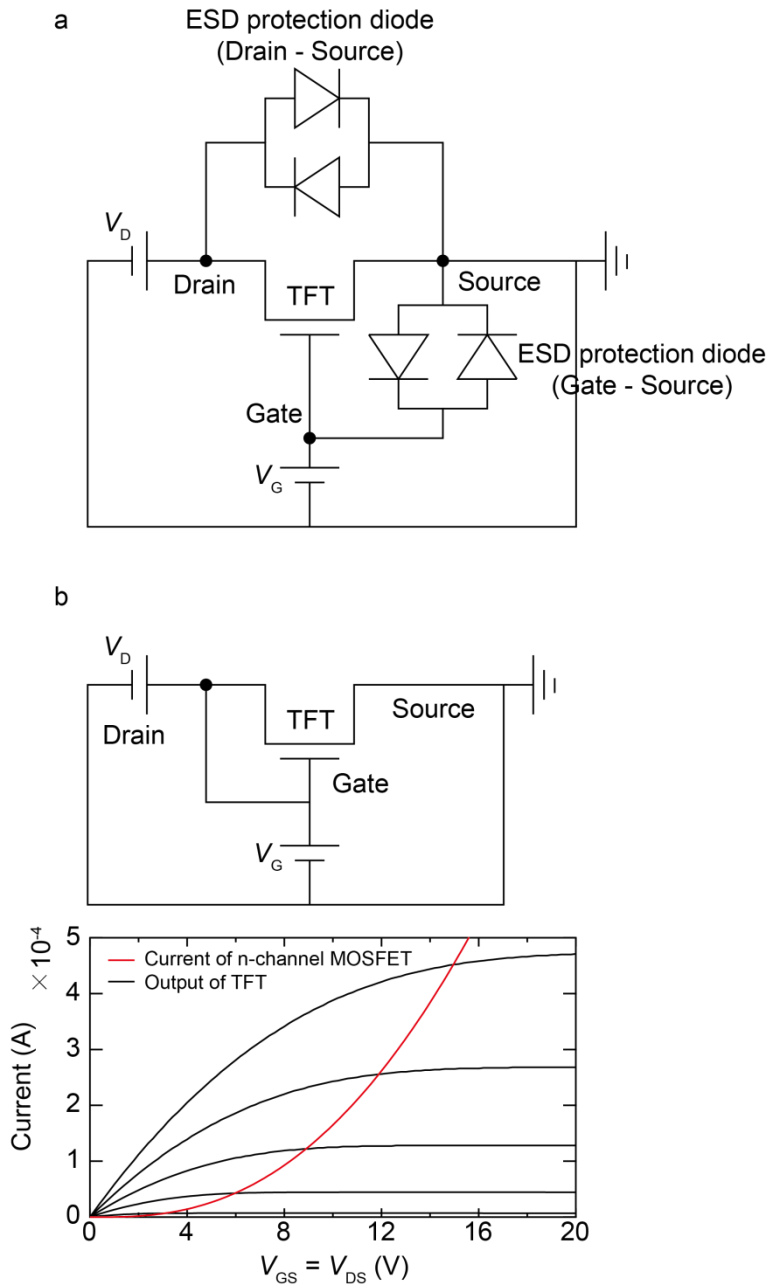

Figure 1.2. (a) An equivalent circuit of a TFT device in which ESD protection diodes are connected in the drain and gate directions. (b) An equivalent circuit of an n-channel MOSFET with the gate electrode connected to the drain, and the current of the connected n-channel MOSFET compared to output characteristic of a TFT.

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Chapter 2. Unconventional electrical vertical current characteristics in metal / insulator / oxide semiconductor structure

2.1 Overview

Transferring electrical charge carriers directly through an electrical insulator thin-film is a prominent and classical subject for various electronic devices including metal / insulator / metal (MIM) diodes and resistive switching (RS) memories [1-4]. However, most electrical insulator thin-films have small electron affinity values and large energy band gaps, which causes to form a large energy barrier at the junction with semiconductor or metal contacts [5]. The energy offset at the junctions prevents the charge carriers from flowing between contacts, thereby blocking the flow of electrical current through the insulator layer under the operating electric field. On the other hand, when a larger electric field is applied to the insulator layer, permanent damage due to a dielectric breakdown occurs and the device performance is lost. Therefore, in MIM diodes or RS devices, electrical charge carriers are transported by other conduction mechanisms than band conduction. The conduction of electrical charge carriers in MIM diodes by a quantum tunnel effect enables electrons to pass almost instantaneously through a narrowed barrier of insulator film to the opposite electrode [6]. In the case of RS devices, a conductive path for electrical charge carriers should be formed inside the insulator layer by an external forming electric field, and resistance changes of the

conductive path by set and reset voltages induce the memory characteristics [7,8]. These conduction mechanisms depend mainly on the electrical properties at the interface between an insulator / electrode contact, so these are called an electrode-limited conduction mechanism. The energy barrier height at the interface of insulator / electrode junction is a key parameter in the electrode-limited conduction mechanisms. Depending on the conduction mechanisms of MIM and RS devices, thickness of the insulator film in the devices has been limited to a few tens of nanometers or less, which narrows the processing window of the insulator films. And it has been difficult to control the direction and magnitude of the electrical currents controlled by the electrode-limited conduction mechanisms in conventional devices [9,10].

Meanwhile, there are other conduction mechanisms through insulator layers that depend on the electrical properties of the insulating film itself, which are classified as bulk-limited conduction mechanisms. The bulk-limited conductions are dominantly controlled by trap states and trap energy levels in insulator materials, and most types of leakage currents in various devices including a field effect transistor (FET) and a metal / insulator / semiconductor (MIS) junction are dependent on the bulk-limited conduction mechanisms [11]. Recent studies on the relationship between a defect density in dielectric materials and a leakage current have revealed that the dielectric defect density at a contact junction correlates directly with the leakage current through the dielectric film [12,13]. It highlights that conventional insulating films can become to transport stably electrical charge carriers without an electrical breakdown by controlling contact junctions or defect densities in the insulator layers. Precise control of the origins and densities of

defect states in insulator thin-films has been a challenging technique. Therefore, it can be an efficient approach to control the bulk-limited conduction of electrical charge carriers by adjusting junction areas with electrodes in the conventional insulator thin-film containing uniformly distributed defect states.

In this chapter, with this strategy, we have confirmed that electrical charge carriers are stably transported in relatively thick conventional insulator films in MIM structures by controlling an electrode contact area. The electrical currents due to the flow of charge carriers through insulator films flow bi-directionally in MIM structures, and the bi-directional vertical currents are changed to uni-directional vertical currents by applying an oxide semiconductor film as a top electrode in the MIM structures. Moreover, we reveal that the vertical currents through relatively thick insulator films depend on a space charge-limited conduction (SCLC) mechanism which is a type of the bulk-limited conduction mechanisms. Depending on the SCLC mechanism of the vertical currents, a direction, a magnitude, and a rectification ratio of the vertical current in the metal / insulator / oxide semiconductor (MIOS) structures are precisely controlled by electrical properties of the top oxide semiconductor electrode.

2.2 Unconventional vertical current in MIM and MIOS structures

Firstly, in order to investigate the vertical current in conventional MIM structures, we fabricated model devices that consisted of a bottom electrode / insulator / top electrode structure and characterized the output currents at the top electrode in response to an applied voltage to the bottom electrode (Figure 2.1a). A heavily doped p-type Si (P^{++} Si) was used as the bottom electrode and a substrate, a silicon dioxide (SiO_2) with a thickness of 200 nm was mainly used as the insulator, and Al metal with a thickness of 100 nm was used as the top electrode. All of the top electrodes were isolated from the edges of the device using a metal shadow mask to avoid unintended side-contacts with the bottom electrode. The area of the Al thin-film with a circle shape was varied from 0.2 mm^2 to 28.26 mm^2 (diameters from 0.5 mm to 6 mm), and we measured 40 devices for each electrode area. There are no vertical current flows in the MIM with a 0.2 mm^2 Al electrode, which confirms that the SiO_2 film has an inherently good insulating property at a junction size of 0.2 mm^2 (Figure 2.1b). However, the vertical current starts to flow as the Al area increases (Figure 2.1c-f), and most of the devices having the Al electrode of 28.26 mm^2 area allow a high vertical current over 10^{-6} A (Figure 2.1f). It should be noted that the 200-nm SiO_2 film maintains a robust pristine insulating property, but the amount of current through the 200-nm SiO_2 increases due to the size of the top electrode. As the top electrode area increases in the MIM devices, the probability of the leakage current through the 200-nm SiO_2 layer increases. The probability is summarized in the cumulative distribution graph of the leakage current values measured at 1 V in the MIM devices (Figure 2.2). The cumulative distribution

graph for the MIM devices shows that very negligible leakage current flows in the MIM devices with a top electrode of 0.2 mm^2 area. The probability of the leakage current steadily increases with the area of the top electrode and the distribution of the leakage current value in the device having the top electrode of 28.26 mm^2 becomes highly uniform to a level higher than 10^{-6} A. Consequently, the conventional 200-nm SiO_2 insulator film serves as a charge transport layer through which electrical charge carriers pass. The phenomenon for which the current increases due to the increase of the electrode area has been consistently reported in MIM structures and RS devices, which is understood to be because the superposition of the trap state in which electrons can move is proportional to the junction region [14-18].

The vertical current – voltage characteristics for the MIM using ITO top metal electrode and the MIOS using IGZO top oxide semiconductor electrode were compared (Figure 2.3a). In MIM device using a 20-nm thick indium tin oxide (ITO) metal as the top electrode, a current of 10^{-2} A, which is due to the compliance of our measurement system, flows stably in both directions through the 200-nm SiO_2. On the other hand, in MIOS device using a 20-nm thick indium gallium zinc oxide (IGZO) semiconductor thin-film as the top electrode, the vertical current stably flows under a positive voltage, but the current hardly flows and maintains an insulating level of ~ 10^{-12} A under a negative voltage (Figure 2.3b). The vertical current in only one direction in the MIOS devices using IGZO electrodes also increases proportionally to the contact size of the IGZO electrode. Thus, the MIOS devices with a 0.2 mm^2 top contact area have negligible low vertical current (Figure 2.4a), but the vertical current values increases as the contact size (Figure

2.4b-e). The vertical currents flow in the MIOS devices with various contact area is also plotted in the cumulative distribution graph, which indicates the current values measured at 10 V in the MIOS devices. The cumulative distribution graph also indicates that the MIOS device with larger contact area allows stably the uni-directional vertical current (Figure 2.5). Consequently, the current (*I*)-voltage (*V*) characteristics of the MIM and the MIOS devices show that the magnitude and direction of the vertical current is highly dependent on the top electrode material: the vertical current flows bi-directionally in MIM device using a top metal electrode; the vertical current flows uni-directionally in MIOS device using a top semiconductor electrode.

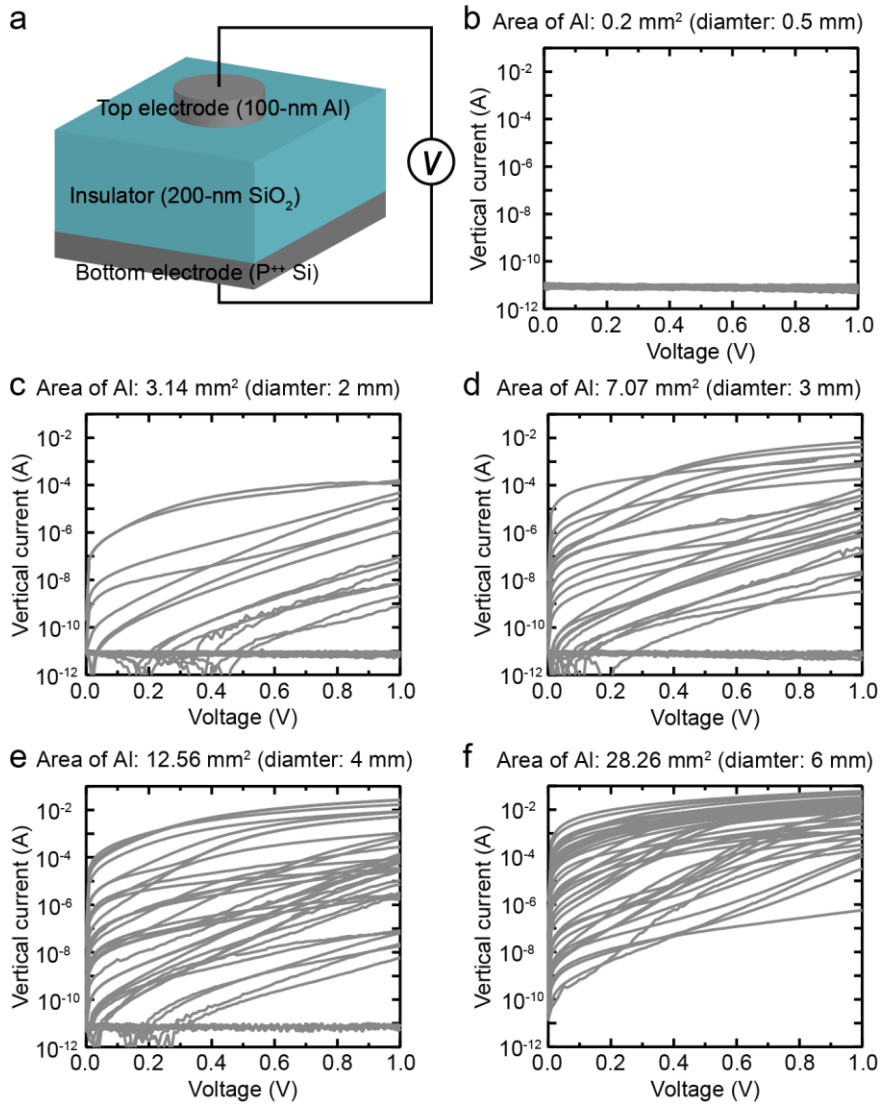

Figure 2.1. (a) Leakage current flowing in metal / insulator / metal (P^{++} Si / 200-nm SiO_2 / 100-nm Al) structures with various Al electrode area from 0.2 mm^2 to 28.26 mm^2. The Al electrodes have circular shapes in a diameter (b) 0.5 mm, (c) 2 mm, (d) 3 mm, (e) 4 mm, and (f) 6 mm. 40 devices were measured for each size.

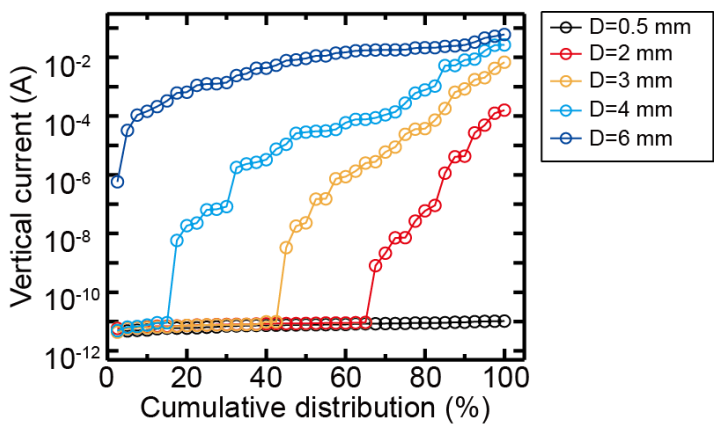

Figure 2.2. Cumulative distribution of the leakage current measured at 1 V for the MIM (P^{++} Si / 200-nm SiO_2 / 100-nm Al) devices with various junction sizes.

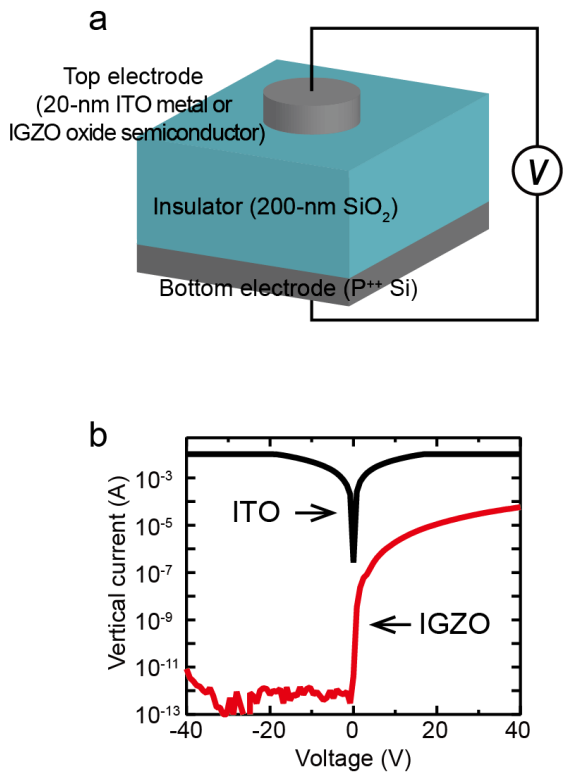

Figure 2.3. (a) Comparison of *I* - *V* characteristics in the MIM and MIOS devices (b) The vertical *I* – *V* curves for the MIM using ITO top metal electrode and MIOS using IGZO top oxide semiconductor electrode.

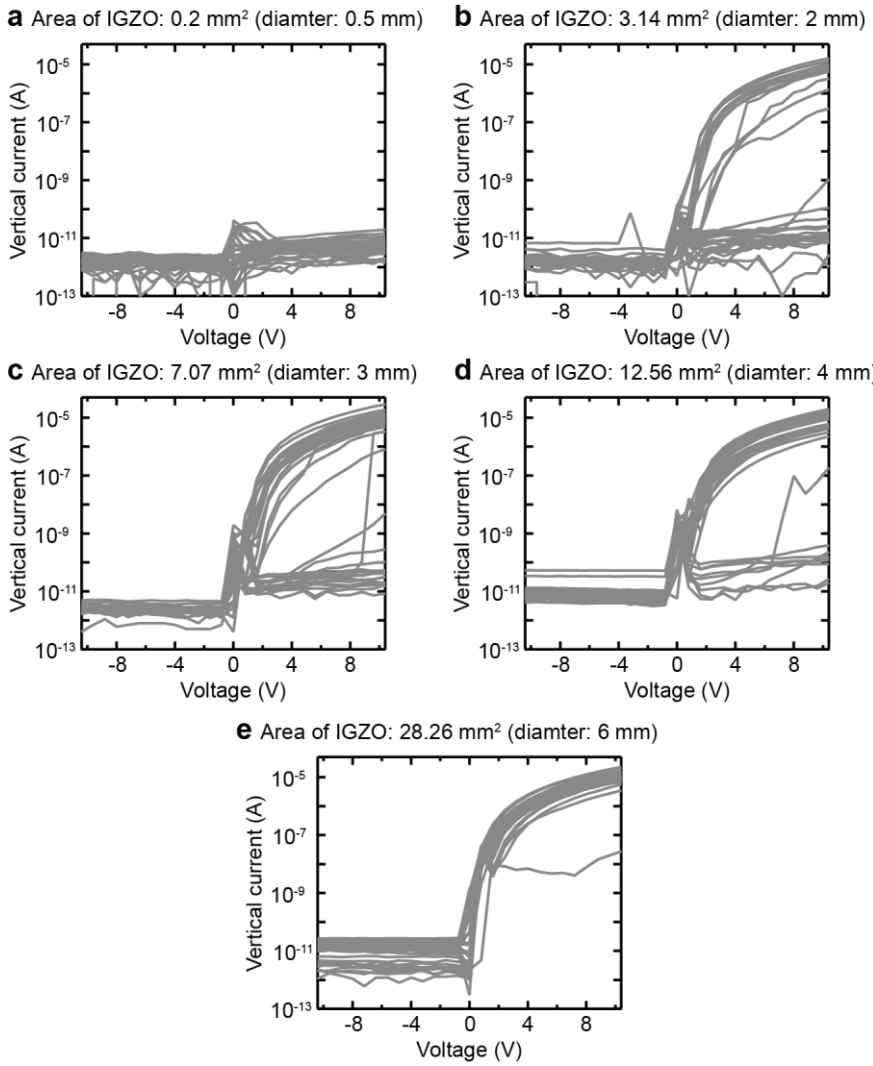

Figure 2.4. Leakage current flowing in metal / insulator / oxide semiconductor (P^{++} Si / 200-nm SiO_2 / 20-nm IGZO) structures with various IGZO area from 0.2 mm^2 to 28.26 mm^2. The IGZO layers have circular shapes in a diameter (a) 0.5 mm, (b) 2 mm, (c) 3 mm, (d) 4 mm, and (e) 6 mm. 40 devices were measured for each size.

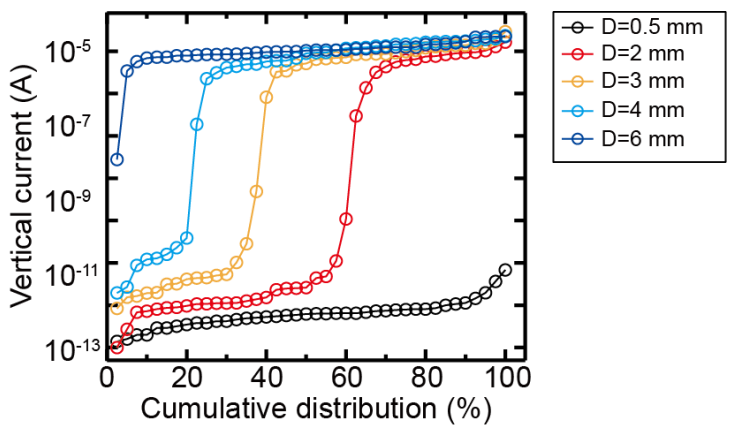

Figure 2.5. Cumulative distribution of the leakage current measured at 10 V for the MIOS (P^{++} Si / 200-nm SiO_2 / 20-nm IGZO) devices with various junction sizes.

2.3 Approach to transporting path of electrons through an insulator film

Based on the bi-directional vertical current flow in the MIM device with a metal top electrode, it can be reasonably assumed that: the 200-nm SiO_2 layer which is contacted with the metal electrode can transport the electrons injected from contacts; the SiO_2 insulator film has inherently defect-like trap sites and the trap sites can be randomly distributed inside the film; and the probability of electron injection and transport through the SiO_2 layer becomes higher as the trap sites overlapped with the metal electrode are more. In the MIM structure consisted of P^{++} Si / SiO_2 / Al, when the area of top electrode is large, the electrons are easily injected into the overlapped trap sites and moved to the adjacent trap sites (Figure 2.6a), and the path of electron transport is also the same in the reverse bias condition (Figure 2.6b). Thus, the unusual vertical current flows bi-directionally in the MIM device with large contact. However, when the top electrode size is small, there are little trap sites overlapped to the top electrode. Thus, the electrons are hardly injected into the SiO_2 layer through the trap sites (Figure 2.6c). In the MIOS structure consisted of P^{++} Si / SiO_2 / IGZO, the path for the electron transport is also equal to the MIM. The vertical current hardly flows in the MIOS structure with a small top IGZO contact, but easily flows in the case having a large top contact under forward bias condition (Figure 2.7a). The IGZO semiconductor electrode is under an electron-accumulation state when the positive voltage is applied to the bottom electrode, so the electrons are easily injected through an electron-accumulated region at the IGZO / SiO_2 interface. These results are equal to the MIM device. However, the vertical current behavior under the reverse bias is

completely different with the MIM device. When the MIOS device is under reverse bias condition, the IGZO layer is completely depleted, that is, the entire layer of IGZO is in the condition of lack of free electrons. Therefore, the electron-depleted IGZO film is like a typical capacitor, which is well-known as the depleted condition in the MOSCAP. Thus, the electrons are blocked by the electron-depleted region, and the current hardly flows under reverse bias (Figure 2.7b). Therefore, the vertical current in the MIOS device is clearly rectified and maintained at pA level at the negative biases and flows in only one direction. The results indicate that the direction and magnitude of the vertical current are controlled by the interface states of the top electrode material and the 200-nm SiO_2 film serves stable transporting states for the injected electrons.

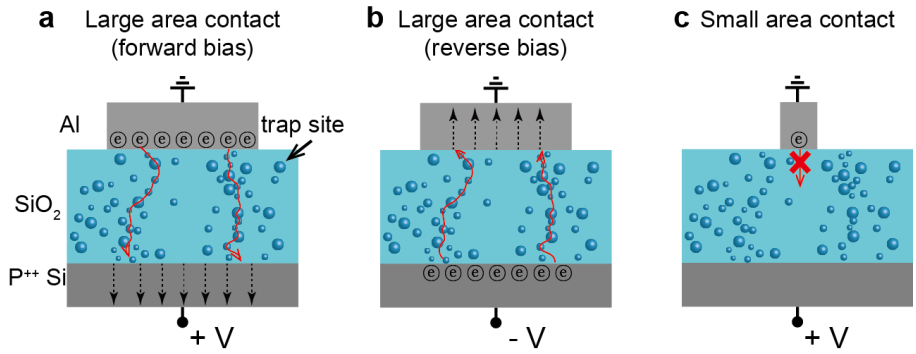

Figure 2.6. Schematic images for the electron transport in the MIM device with contact size. (a) The electron transport in the MIM device with large areal contact under forward bias. (b) The electron transport in the MIM device with large areal contact under reverse bias. (c) The electron transport in the MIM device with small areal contact.

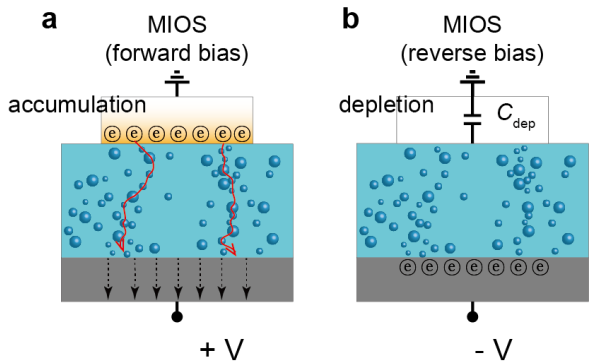

Figure 2.7. Schematic images for the electron transport in the MIOS device. (a) The electron transport under accumulation condition in the MIOS device. (b) The fully electron-depleted MIOS.

2.4 Exploring the films and interface quality

In order to explore the conduction mechanism through a thick insulator film, the quality of the interfaces and films in the MIOS device was analyzed. The film quality of the 20-nm IGZO thin-film and the interface between the IGZO and SiO_2 layers were analyzed after repeating operation of 3,000 cycles to check any damage or deterioration during fabrication processes or operation of the device. A topographical image of an annealed IGZO thin-film observed by a field emission scanning electron microscopy (FESEM) indicates that the film has a small grain size, and X-ray diffractive peaks of the annealed and as-deposited IGZO thin-films prove that the IGZO films have amorphous crystalline structures (Figure 2.8a and b). Cross-sectional high resolution transmission electron microscopy (HRTEM) images and energy dispersive spectroscopy (EDS) line scanning profiles of P^{++} Si / 200-nm SiO_2 / 20-nm IGZO structure show a clear interface of IGZO / SiO_2 without any inter-mixing layer or atomic diffusion despite thermal annealing process of 350 ℃ for 90 seconds and repeated operation (Figure 2.8c and d). Furthermore, to verify whether flow of the vertical current is caused by any dielectric breakdown due to an applied electric field, an endurance test was carried out for the MIOS device for 3,813 operating cycles. The recorded currents at 40 V and - 40 V manifest a reliable flow of current of ~ 1 x 10^{-5} A and ~ 5 x 10^{-10} A, respectively, for the repeated cycles. The results mean the 200-nm SiO_2 layer maintains an excellent insulating property without any dielectric breakdown or insulating degradation (Figure 2.8e). Consequently, the vertical currents are not caused by any severe leakage path of the insulator film, and the electrode-limited

conduction mechanisms like a quantum tunneling effect of charge carriers is almost impossible because the thickness of the SiO_2 insulator is 200 nm. Instead, it can be reasonably inferred that the electrons are injected and transported through inherent trap sites that randomly exist in the SiO_2 layer because the vertical current starts to flow near 0 V without a strong external electric field and flows more stably as the junction size increases.

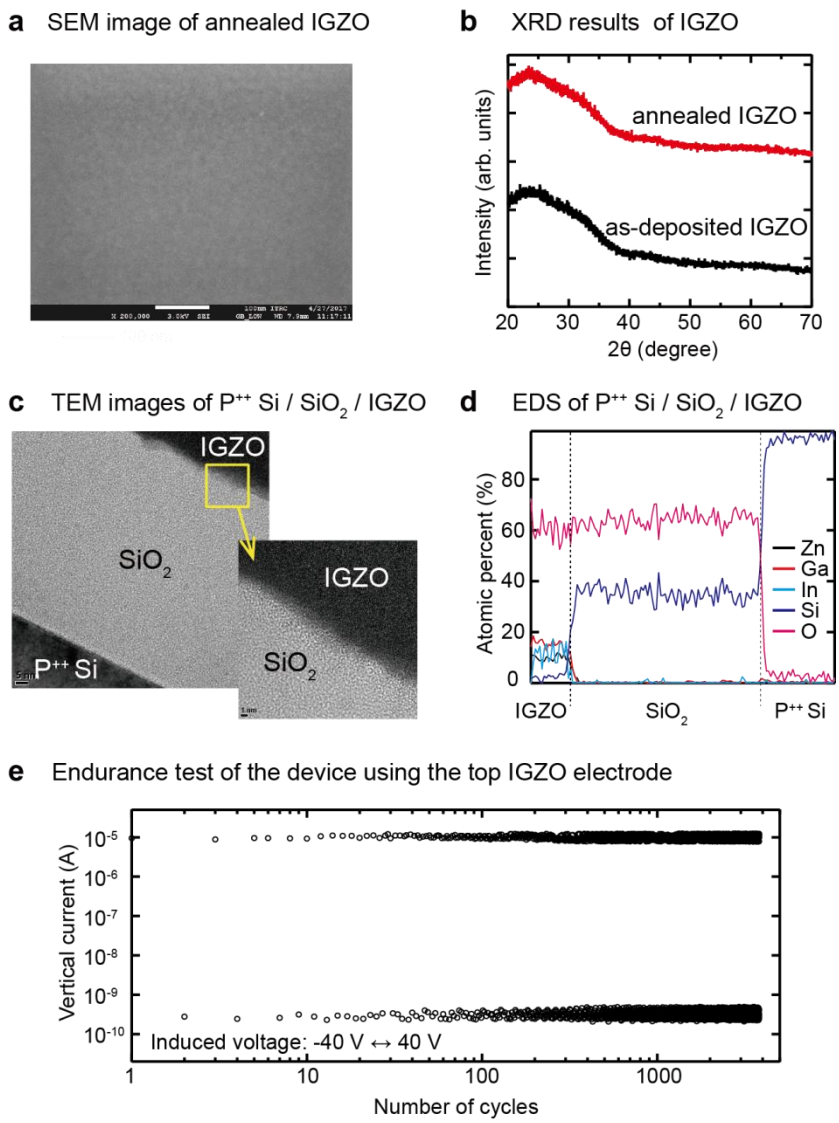

Figure 2.8. Analysis of the film qualities of the IGZO thin-films and the interface between SiO_2 and IGZO. (a) Top view image of an annealed IGZO thin-film observed using a FESEM. (b) X-ray diffraction patterns of the annealed and as-deposited IGZO thin-films. (c) A cross-sectional HRTEM image of the P^{++} Si / 200-nm SiO_2 / 20-nm IGZO structure. (d) An EDS line scanning profile of the P^{++} Si / 200-nm SiO_2 / 20-nm IGZO structure. (e) The endurance test result for the MIOS device using the IGZO electrode.

2.5 Conduction mechanism of the unconventional vertical current

2.5.1 Conduction mechanism of the vertical current

In conduction theory in dielectrics, the electrical charge carriers are transported through a dielectric film by a number of conduction mechanisms [19]. In conduction mechanisms, some mechanisms mainly rely on the electrical property in dielectric material itself. These conductions are called as bulk-limited conduction mechanisms, and include Poole-Frenkel emission, Ionic conduction, Ohmic conduction, and Space charge-limited conduction (SCLC). In ohmic conduction, electrical charge carriers including electrons and holes are transported in mobile bands, conduction band and valence band. However, the high energy barrier heights between the dielectric and the contact metal prevent the charge carriers from being implanted into the mobile bands. Nevertheless, a small number of carriers that can be excited by an external thermal energy are present in the dielectrics, which contribute to the ohmic conduction. Although the ohmic conduction partially contributes to other dielectric conductions, but in a resistive switching device that has been actively studied recently, conduction in a low resistance state, in which current flows through a conductive filament, has been found to be an ohmic conduction [20, 21]. In the ohmic conduction, the electrical current through a dielectric exhibits a linear relation to the electric field like equation (2.5.1), thus, the slope of the linearly fitted *I-V* curve is close to 1.0.

$$J = \sigma E, \tag{2.5.1}$$

where J is an electrical current density value, E is the constant electric field in a dielectric, and σ is electrical conductivity.

In the case of space charge-limited conduction, electrons are injected into the dielectrics from the contact metal with negligible resistance. When the injected electrons fill up the trap sites in the dielectric, a space charge starts to build up in the dielectric; the injected electrons then move freely within the dielectric. In the condition of very strong injection of electrons, all trap sites are filled up and the conduction becomes to be limited by the space charge density. Furthermore, the current density (J)-electric potential (V) characteristic of the space charge-limited current follows the Child's raw, and the space charge-limited current can be expressed as:

$$J = \frac{9}{8}\mu_e \varepsilon_0 \varepsilon_{ox} \frac{V^2}{t_{ox}^3}, \qquad (2.5.2)$$

where μ_e is the mobility of electron, ε_0 is the permittivity of the free space, ε_{ox} is the relative permittivity of the dielectric oxide, and t_{ox} is the thickness of the dielectric. The space charge-limited current is proportional to V^2; therefore, the I-V characteristics plotted on the log-log axis should have a linear relationship of slope of around 2.0. In our experiments, the uni-directional vertical current is proportional to V^2 (Figure 2.9a), and the slope of the linearly fitted the vertical current – voltage curve in the MIOS device is around 2.1 (Figure 2.9b), which means the unusual vertical current in the MIOS device depends on the space

charge-limited conduction. Consequently, the origin of the uni-directional current can be judged as electrons passing through the trap site present in the SiO_2, and the conduction of electron is governed by the space charge-limited conduction mechanism.

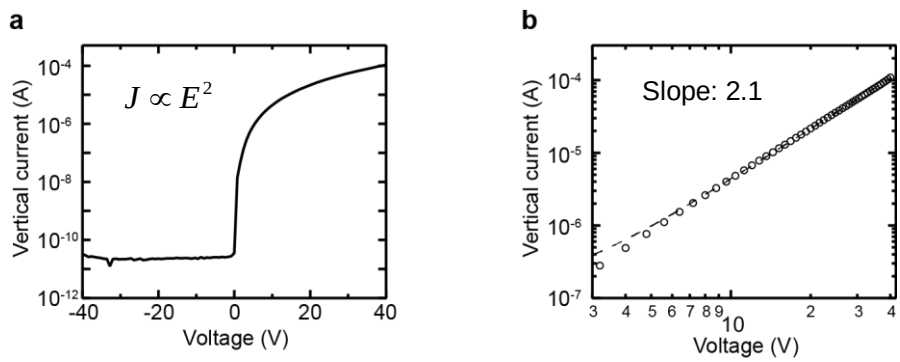

Figure 2.9. The vertical current – voltage curve in the MIOS device using IGZO top electrode. (a) The current – voltage characteristic. (b) The linearly fitted curve in log-log axes.

2.5.2 Temperature dependence of the vertical current in the MIOS device

The conduction mechanisms in dielectrics are classified by the factors that control the movement of charge carriers through the dielectric. The electrical current through the dielectric may be due to a number of different conduction mechanisms with different dependencies on temperature and electrical bias. Therefore, measuring current density (*J*)-voltage (*V*) characteristics at various temperatures is a very effective technique for identifying the conduction mechanism. In the P^{++} Si / 200-nm SiO_2 / 20-nm IGZO structure, the uni-directional vertical current increases steadily under positive voltage ranges as the temperature increases from room temperature to 450 K (Figure 2.10a). The *I-V* curves for all temperatures are linearly fitted in log-log axes, which signify that the conductions of the carriers follow a bulk-limited conduction such as an ohmic or a space charge-limited conduction (Figure 2.10b). However, because the current by the ohmic-like conduction decreases by the temperature rise, the conduction of the MIOS device is inconsistent with ohmic conduction. The slopes of all the fitted lines are around 2.0, and there is no transition of the slopes so that the conductions of the charge carriers through the 200-nm SiO_2 layer evidently are dependent on the space charge-limited conduction (Figure 2.10b) [19]. Meanwhile, in the MIOS structure, the vertical current under a negative voltage, which hardly flows at room temperature, also begins to increase sharply from 400 K, reaching ~10^{-7} A at 450 K (Figure 2.10a). The increase of the currents by temperature at both negative and positive biases can be clearly explained by excited charge carriers in the IGZO electrode. The charge carriers, electrons and holes, are easily excited by the absorbed thermal energy on

the tail-states of the top IGZO semiconductor electrode [22, 23], and the excited electrons (or holes) enter into the 200-nm SiO_2 layer by the positive (or negative) voltages (Figure 2.10c). Therefore, it can be ascertained that the current level is highly dependent on the concentration of the charge carriers injected from the contacts, which is consistent with the basic theory that the space charge-limited current is mainly controlled by carriers injected from the electrodes [24].

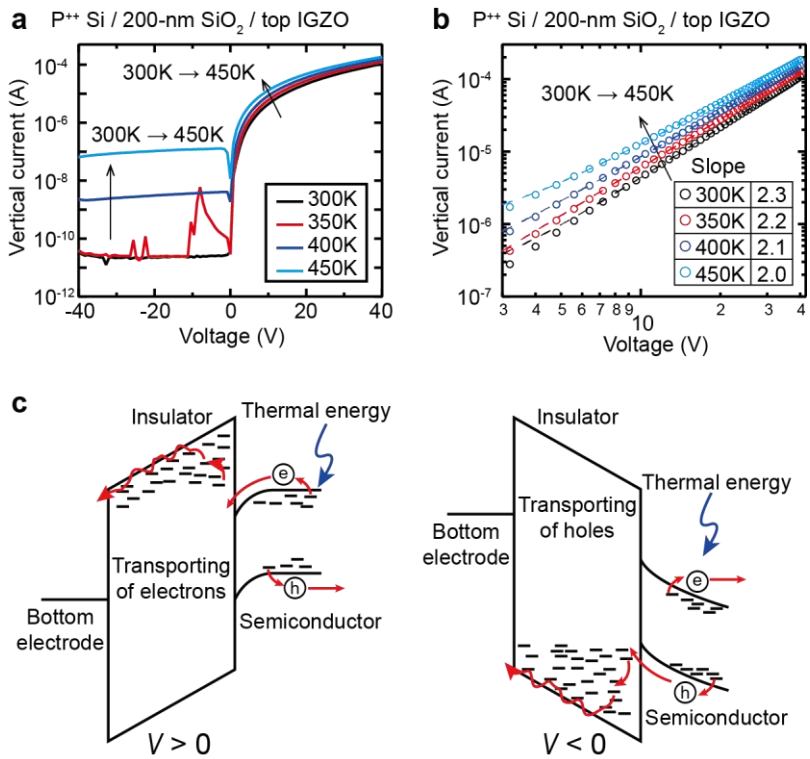

Figure 2.10. Temperature dependence of the vertical current in the MIOS structure. (a) The current increases at both negative and positive voltage ranges as the temperature rises in the MIOS device. (b) The *I-V* curves of the MIOS device are plotted linearly in log-log axes and the slopes of the curves are around 2.0. (c) The schematic images depict that the excited charge carriers in the IGZO layer by thermal energy contribute to the current rise.

2.6 Verification of the conduction mechanism of the vertical current

2.6.1 Influence of barrier heights at each interface on the vertical current

To verify whether the movement of the electrons through the SiO_2 film is due to the chemical reaction or the electrostatic charge transfer at the interfaces, the *I-V* behaviors were compared for various interfaces consisting of junctions between different materials. Theoretically, an energy level offset exists between the minimum level of the conduction bands of the top electrode and the insulator. The energy barrier prevents the free passage of charge carriers from the top electrode to the bottom electrode [25-27]. The energy level offset of 3.26 eV at the interface between the SiO_2 and IGZO layers is higher than the energy barrier of 2.06 eV at the interface between the Si_3N_4 and IGZO thin-films; although, the characteristics of the vertical current of the devices consisting of P^{++} Si / SiO_2 / 20-nm IGZO are very similar to those of devices using the Si_3N_4 insulators (Figure 2.11a and b). In addition, despite an energy barrier of 1.2 eV at the interface between the SiO_2 and the Si_3N_4 layers, the vertical current behavior for a device structure of P^{++} Si / 100-nm SiO_2 / 100-nm Si_3N_4 / 20-nm IGZO is almost equivalent to that for a device using a double insulator consisting of 100-nm Si_3N_4 / 100-nm SiO_2 (Figure 2.11c). Consequently, the energy barriers at the interface of the top electrode and the insulator and at the interface of the first insulator and the second insulator have little effect on the flow of the vertical current (Figure 2.11d). Meanwhile, in a typical metal / oxide / semiconductor junction, a difference in the work function between the top and bottom electrodes changes the space charge region at the

interfaces of the top electrode and causes an unexpected shift of the *I-V* curve [28, 29]. The P^{++} Si, a heavily phosphor-doped n-type Si (N^{++} Si), and 100-nm ITO metal on glass with different work function levels were compared as the bottom electrode. All of the measured *I-V* curves for the devices with each bottom electrode are almost the same, which shows that the injection of charge carriers into the insulator layer is independent of the work function level of the bottom electrode (Figure 2.11e). Therefore, the injection and transport of the carrier through the insulating film is not affected by the height of the energy barrier at each interface, confirming that the charge carriers are transferred through randomly distributed trap centers of the insulator layers.

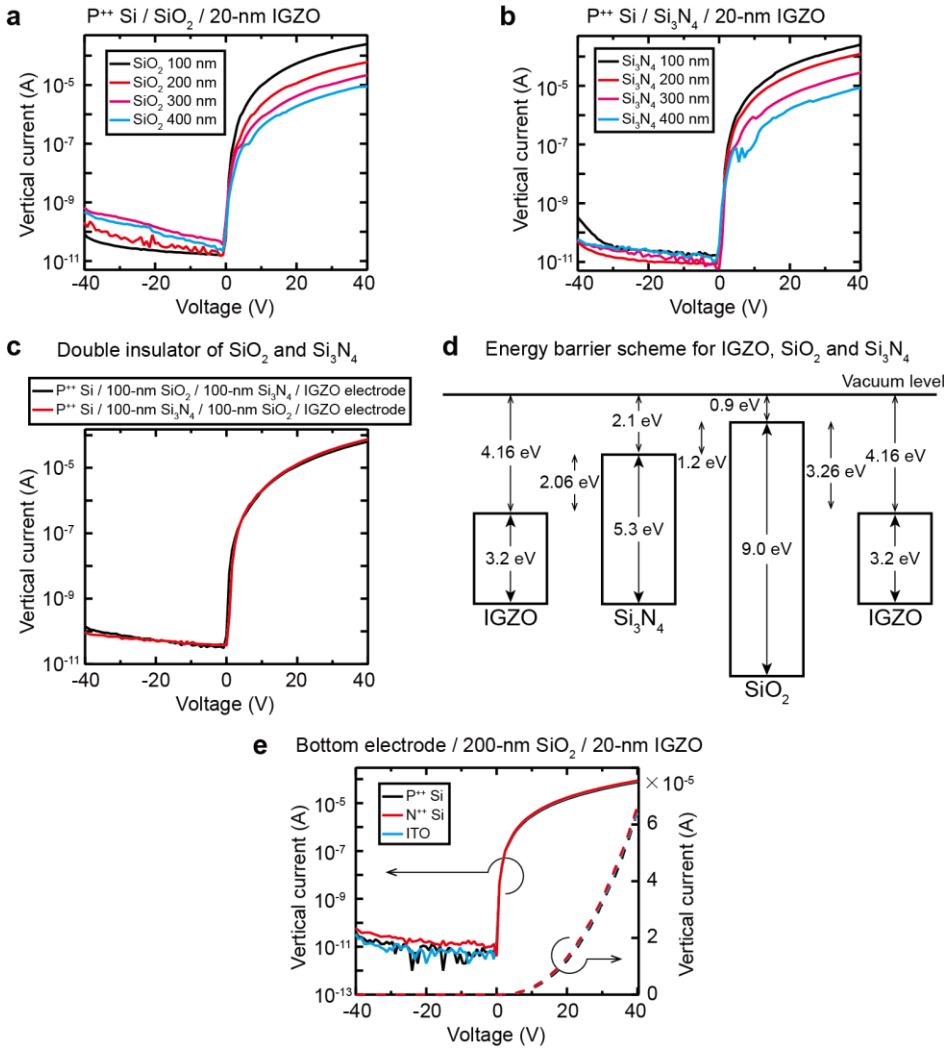

Figure 2.11. Comparison of the vertical current characteristics in the MIOS devices using different insulating materials and bottom electrode materials. (a, b) The vertical current through the (a) SiO_2 or (b) Si_3N_4 insulator films with thicknesses of 100 nm to 400 nm. (c) The vertical current characteristics for the MIOS devices composed of double insulating thin-films of SiO_2 and Si_3N_4. (d) The energy barrier schematic diagram at each interface of IGZO, SiO_2 and Si_3N_4 thin-films. (e) The vertical current characteristics of the MIOS devices using a P^{++} Si, a N^{++} Si and a 100-nm ITO metal.

2.6.2 Influence of trap density in the SiO_2 film on the vertical current

In order to investigate the effect of the trap site density of SiO_2 film on the vertical current flow, the vertical current behavior of MIM structures and MIOS devices having 50 nm thick SiO_2 insulator films with different film quality fabricated by thermal oxidation and PECVD (Plasma Enhanced Chemical Vapor Deposition) method were compared. According to many previous studies on the thin-film deposition techniques, the SiO_2 thin-film formed by thermal oxidation has very low leakage current value, and the SiO_2 thin-film deposited by PECVD has a relatively high leakage current level [30, 31]. The MIM devices with 50 nm thick SiO_2 grown by thermal oxidation at 1100 ℃ show little leakage current at the contact area of 0.2 mm^2 and 0.79 mm^2 (Figure 2.12a and b), but the leakage current increases rapidly from the contact area of 3.14 mm^2 (Figure 2.12c and d). On the other hand, in the MIM devices with the 50 nm thick SiO_2 deposited by PECVD, high leakage currents flow even at the contact area of 0.2 mm^2 (Figure 2.12e - h). The deviation of the leakage current flow due to the difference of the film quality is clearly displayed in the cumulative distribution graph in which the current value at 1 V is plotted (Figure 2.13). The cumulative distribution graphs of leakage current demonstrate that the SiO_2 thin-film deposited by PECVD permits much higher leakage current than the thermal oxidation even at the same junction size, which indicates that the SiO_2 film by PECVD has much more trap density than the film formed by thermal oxidation. Based on the difference in quality of the SiO_2 films, the *I-V* characteristics of the MIOS devices with 50 nm thick SiO_2 gate insulator films grown by thermal oxidation and PECVD were compared. The area of the

IGZO active layer in the two MIOS devices was equal to 1.5 mm^2. The thermally oxidized 50 nm thick SiO_2 insulator completely blocks the vertical current, but a high uni-directional vertical current flows through the 50 nm thick SiO_2 film made by PECVD regardless of the same IGZO area (Figure 2.14); therefore, it can be rationally judged that the unusual gate current is due to the transport of electrons flowing through the trap sites in the insulator layer. On the other hand, in Figure 2.13a and b, most devices with contact areas of 0.2 mm^2 and 0.79 mm^2 have little leakage current, while some devices allow a relatively high current above 10 nA. These results imply that the trap sites in the SiO_2 thin-film are randomly distributed, thus some small areal regions have high trap density locally.

The TEM image of the thermally oxidized SiO_2 thin-film interface reveals that the SiO_2 film has a complete amorphous phase (Figure 2.15a). This implies that Si and O are not in perfect stoichiometric binding state, and there are many defect-like trap sites in the film. It is a very difficult challenge to find the precise location of the defects in the amorphous thin-film through TEM analysis, but comparing the Si-O binding state using XPS analysis is a general method to estimate the amount of defects [32-34]. The XPS spectra of the Si 2P levels for the thermally oxidized SiO_2 and PECVD-deposited SiO_2 films were compared, and a quartz glass, a SiO_2 material of 99.95 % high purity with almost no impurities, was used as a reference. The Si 2P peak of the quartz glass is detected at a binding energy of 103.46 eV, which is consistent with preceding results of other studies [34]. On the other hand, the Si 2P peak of the thermally grown SiO_2 film is detected at lower binding energy of 103.35 eV, and that of the PECVD-deposited film is detected at 103.26 eV (Figure 2.15b). The gradual shift of the Si 2P peak toward lower binding energies

means that SiO_{2-X} state, mainly Si^{3+}, exists in both the thermally grown and the PECVD-deposited SiO_X compared to the quartz. The formation of Si^{3+} implies an increase in Si-rich bonds, such as dangling bonds or oxygen defects. This is clearly identified by each fitted peak: the peak of the quartz glass is mostly consisted of the Si^{4+}, but the Si^{3+} peak hardly exists, and comparing the area of each peak, the Si^{3+} has a very small fraction of 0.01 compared to the Si^{4+} (Figure 2.15c). On the other hand, the Si^{3+} peak occupies a larger portion in the thermally grown SiO_X film, and the area ratio of Si^{3+} is 0.18. The ratio of Si^{3+} peak in the PECVD-deposited SiO_X film is much larger and reaches 0.37 (Figure 2.15d and e). Therefore, there are more defect states including dangling bonds and oxygen deficiencies in the thermally grown SiO_X film compared to the quartz, further, the PECVD-deposited SiO_X film has even more defect states than the thermally grown film. These analyzes agree well with the result that the 50 nm thick SiO_X film deposited by the PECVD allows higher leakage current than the same film grown by thermal oxidation (Figure 2.12).

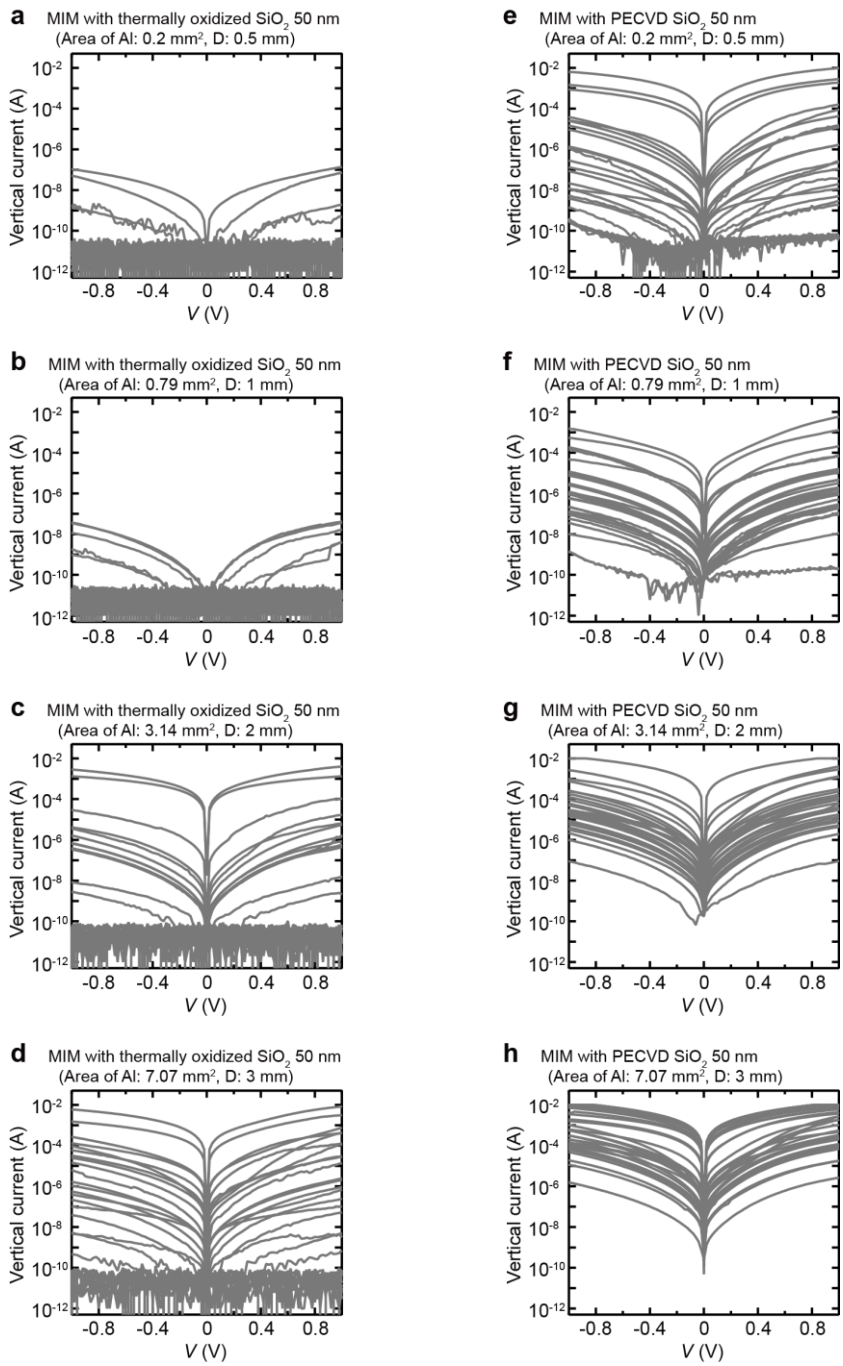

Figure 2.12. Comparison of vertical current flowing by SiO_2 deposition method in metal / insulator / metal (P^{++} Si / 50-nm SiO_2 / 100-nm Al) structures with various Al electrode area from 0.2 mm^2 to 7.07 mm^2. The SiO_2 films were formed by (a-d) thermal oxidation and (e-h) PECVD method.

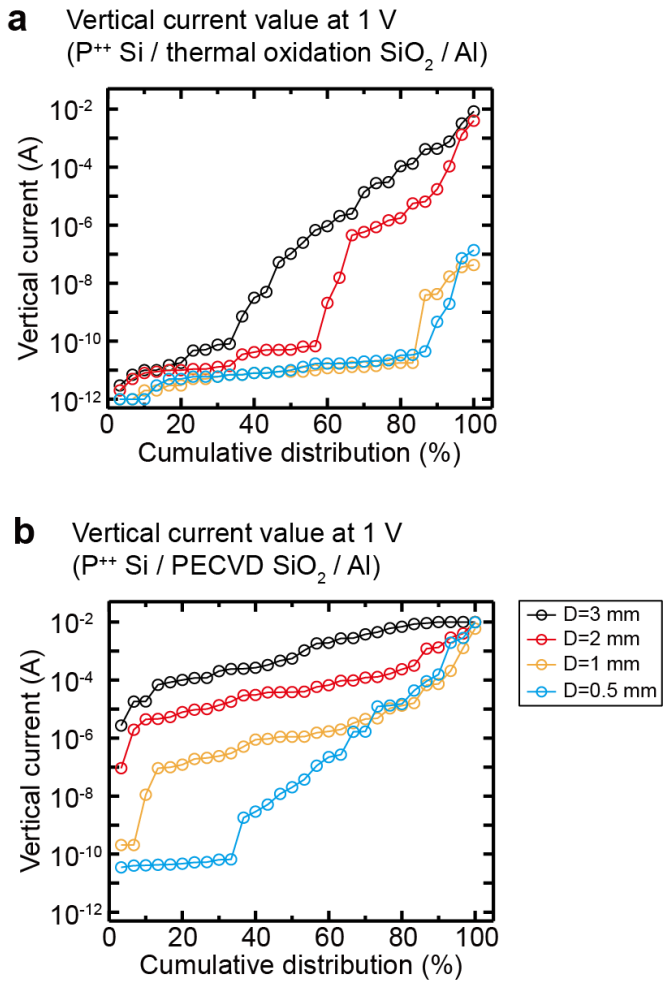

Figure 2.13. Cumulative distribution of vertical current values measured at 1 V of MIM devices with 50-nm SiO_2 layers of different film quality. (a,b) Cumulative distribution of the current measured at 1 V for the MIM devices with (a) thermally oxidized and (b) PECVD deposited 50-nm SiO_2 insulators varying junction sizes.

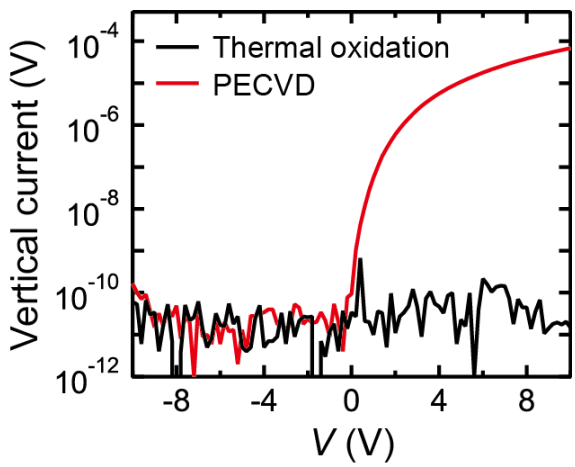

Figure 2.14. Comparison of the vertical current in the MIM devices with 50 nm thick SiO_2 films deposited by thermal oxidation and PECVD.

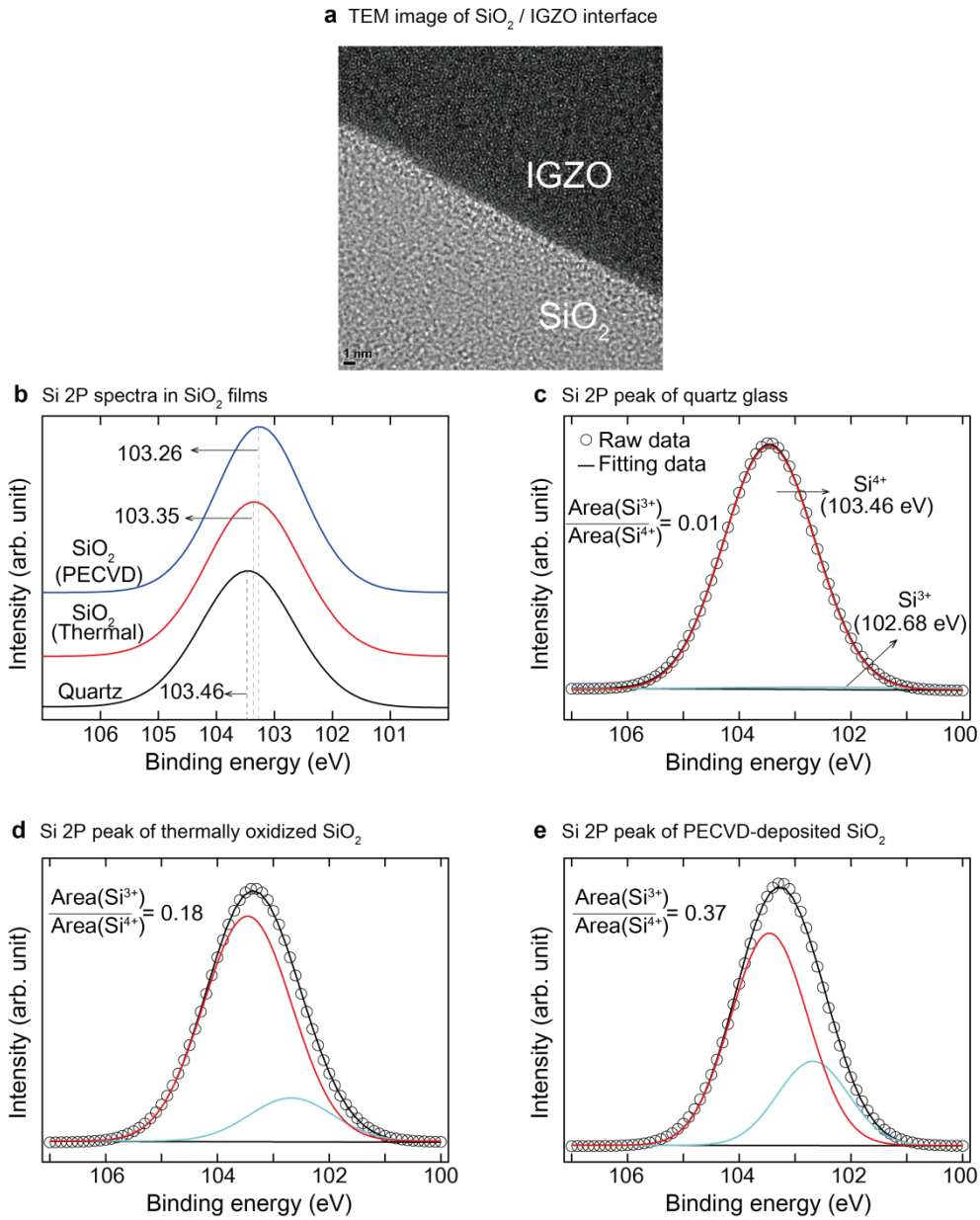

Figure 2.15. (a) TEM image of the SiO_2 / IGZO interface. (b) XPS spectra of Si 2P for a quartz glass, a thermally oxidized SiO_2, and a PECVD-deposited SiO_2. The fitted Si 2P peak of (c) quartz glass, (d) thermally oxidized SiO_2, and (e) the SiO_2 film deposited by PECVD.

2.7 Effect of electrical properties of the top semiconductor electrode on the vertical current behavior

2.7.1 Influence of conductivity of the oxide semiconductor electrode on the vertical current

Depending on the SCLC mechanism, the vertical current in the MIOS device using the top semiconductor electrode depends mainly on the concentration of charge carriers injected from the top semiconductor electrode; thus, the current level can be adjusted by controlling the electron mobility or doping level of the top semiconductor material. To explore the effect of the conductivity on the current, different n-type metal oxide semiconductor materials, IGZO, zinc tin oxide (ZTO) and zinc oxide (ZnO), were compared as the top electrode on the P^{++} Si / 200-nm SiO_2 substrate. The thickness of the semiconductor films was constant as 20 nm. We firstly fabricated thin-film transistors (TFTs) using the semiconductor thin-films as an active layer to compare the field-effect mobility of electrons for each 20-nm semiconductor thin-film. The current characteristics between a source and a drain electrode (I_{DS}), which are measured for a source to drain voltage (V_{DS}) of 0.1 V, exhibit the typical transfer curves of the n-type oxide semiconductor TFTs [35, 36]. The *I-V* curves show that the active layers are completely depleted in the negative V_{GS} regions. Because the I_{DS} is proportional to the electron mobility of the active layer, the I_{DS} increases as the electron mobility of the semiconductor active layer increases. The extracted field-effect mobility for the TFTs using the IGZO, ZTO, and ZnO active layers is 12.6, 7.7, and 4.0 $cm^2V^{-1}s^{-1}$, respectively (Figure

2.16a). Furthermore, in the MIOS devices with IGZO, ZTO and ZnO electrodes, the vertical current is also proportional to the electron mobility of the top semiconductor electrode; thus, the vertical current of the device using the IGZO is the highest, and the vertical current flowing through the ZnO is the lowest (Figure 2.16b).

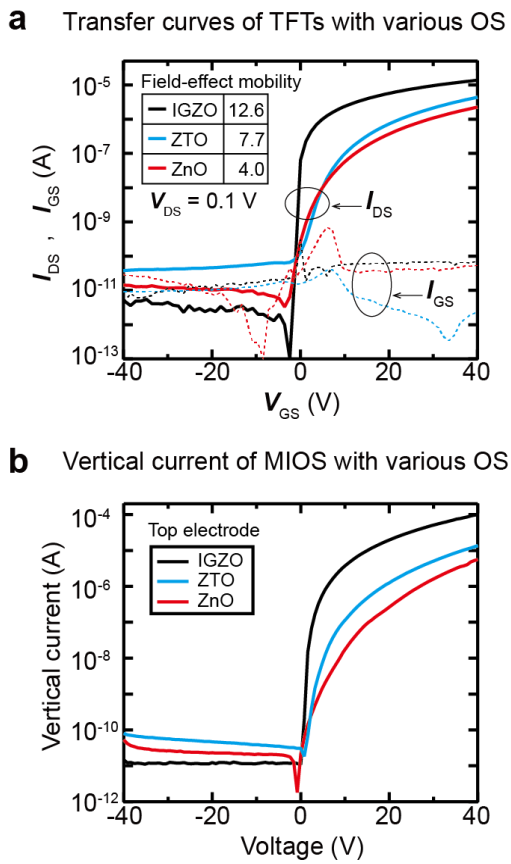

Figure 2.16. Effect of the electron mobility of the top semiconductor electrode on the vertical current. (a) The source-drain currents measured in thin-film transistors (TFTs) using 20-nm IGZO, ZTO and ZnO thin-films as an active layer. (b) The vertical current values for the MIOS structures using 20-nm IGZO, ZTO and ZnO thin-films.

2.7.2 Effect of the doping concentration of the top semiconductor electrode on the current behavior

By the polarity of the applied voltages in the MIOS devices, the top semiconductor electrode becomes fully electron-accumulated or depleted at the interface with the insulator inducing the uni-directional vertical current. However, it is noted that increasing the doping concentration makes a semiconductor thin-film less depleted at a constant negative voltage. It implies that the vertical current level at the negative voltage can be controlled by the doping level of the top semiconductor electrode. To verify the effect of the doping level on the current direction, the doping level of the IGZO thin-film was varied using a co-sputtering method of simultaneously depositing the IGZO and the ITO materials from each sputtering target. The sputtering power applied to the IGZO target was fixed to 90 W, and the power applied to the ITO target was varied from 0 to 100 W, and all compositional ITO-doped IGZO (hereafter denoted as ITGZO) thin-films were deposited to a thickness of 20 nm. From the resistivity values and charge carrier concentrations analyzed by the Hall measurement system, increasing the power applied to the ITO target results in a higher doping state of the ITGZO thin-film enhancing the carrier concentration and lowering the resistivity of the thin-films (Table 2.1 and Figure 2.17a). The change of the depleted state due to the increased doping was confirmed by the capacitance (*C*)-voltage (*V*) characteristics for metal / oxide / semiconductor capacitors (MOSCAPs) with the ITGZO layers. The continual increase of the *C* value under the negative biases indicates that the depletion region width is substantially extended due to the increased doping (Figure 2.17b). The transfer

curves (I_{DS}-V_{GS}) of the TFTs using the ITGZO layers as the active layer also show that the ITGZO thin-films are partially depleted and are becoming a degenerated semiconductor as the doping level increases (Figure 2.17c). In fact, because the characteristic of a semiconductor thin-film approaches the characteristic of a conductor as the doping is increased, the *I-V* characteristic of the MIOS device becomes close to that of the MIM device. Therefore, the higher doping level of the top ITGZO electrode in the P^{++} Si / SiO_2 / ITGZO structure enables the higher vertical current at the positive voltage and also causes a significant increase in the vertical current at the negative voltage region (Figure 2.17d). These results prove that the polarity and magnitude of the vertical current passing through a thick insulator film are sophisticatedly controlled by the doping concentration of the top semiconductor electrode. To test the potential of the MIOS device whether it can be adopted in real electronic circuits, a sine wave with amplitude of 20 V and a frequency of 100 Hz was applied to the device, and the output waves were measured varying the doping of the top ITGZO electrode. The output wave passing through the MIOS device with the pure IGZO electrode is clearly rectified, enabling a reduced wave of 12.6 V for the positive input sine waves and blocking most of the negative input signals. Moreover, the passed positive output wave steadily increases due to the enhanced conductance of the top ITGZO electrode as the doping level is increased, thereby reaching 93 % of the input wave amplitude in the most highly doped device. Furthermore, the amplitude of the rectified negative waveform significantly increases with a higher doping concentration, and the passing ratio of the negative input wave is controlled precisely from 3 % to 89 % in the regime of the doping levels (Table 2.2 and Figure 2.17e).

Table 2.1. Resistivity and charge carrier concentration of ITGZO in Figure 2.17

IGZO power (W)	ITO power (W)	Resistivity (Ωcm)	Carrier concentration (cm^{-3})
90	0	2.74	3.3×10^{17}
90	25	1.48	6.1×10^{17}
90	50	0.46	1.5×10^{18}
90	75	0.20	8.3×10^{18}
90	100	0.05	1.5×10^{19}

Table 2.2. Rectified values of the sine wave in Figure 2.17

ITO power (W)	Output voltage (positive) (V)	Output voltage (negative) (V)	Output ratio (positive) (%)	Output ratio (negative) (%)
0	12.6	-0.6	63	3
25	13.0	-1.8	65	9
50	15.4	-4.2	77	21
75	17.0	-11.0	85	55
100	18.6	-17.8	93	89

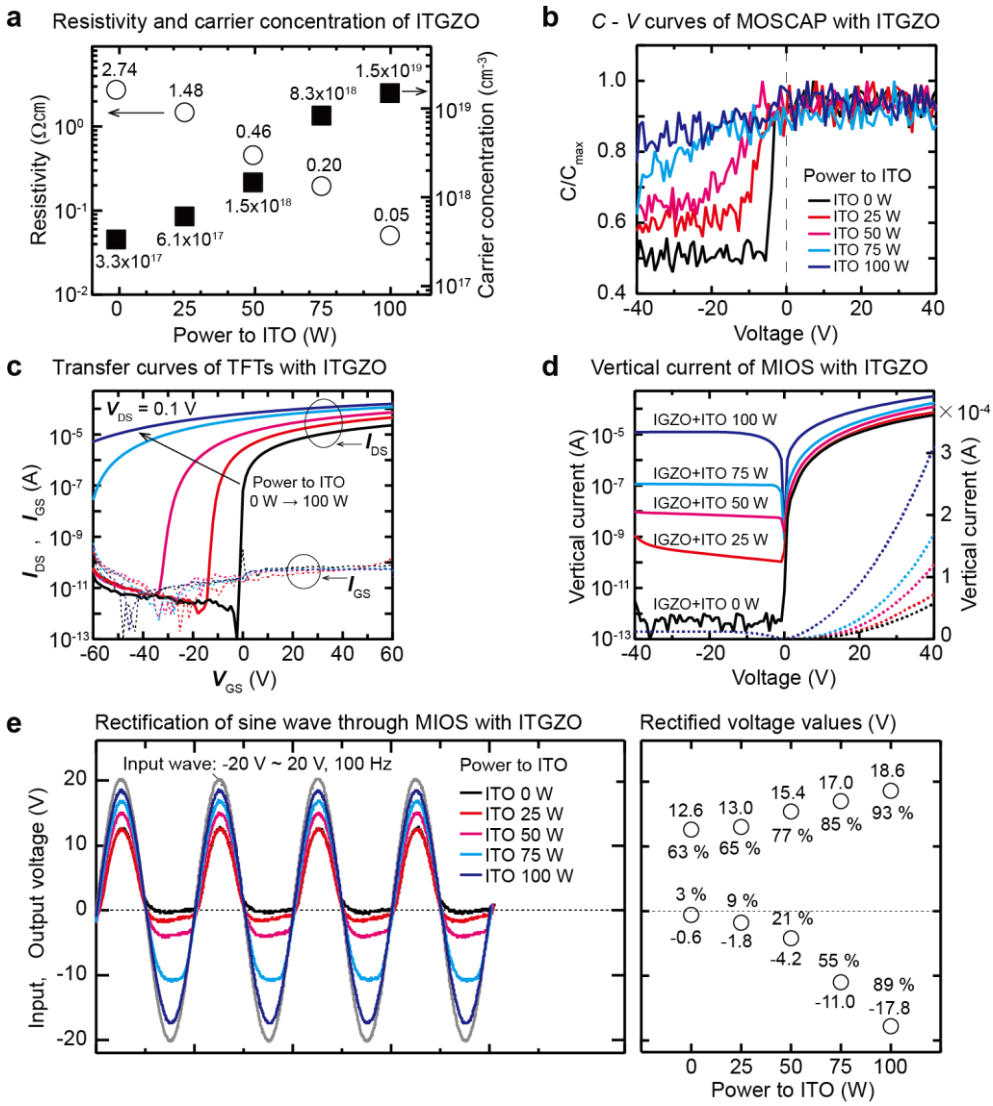

Figure 2.17. Effect of the doping concentration of the top semiconductor electrode on the current behavior. (a) Charge carrier concentration and resistivity of the 20-nm ITO-doped IGZO (ITGZO) thin-films. (b) The *C-V* characteristics of MOSCAPs using the ITGZO thin-films. (c) The source-drain currents measured in the TFTs using the ITGZO thin-films. (d) The vertical current values for the MIOS structures using the 20-nm ITGZO thin-films. (e) The output sine waves through the MIOS device of P^{++} Si / 200-nm SiO_2 / 20-nm ITGZO.

2.8 Conclusion

In conclusion, we have shown that the vertical current can flow reliably through a thick insulating film of the MIM structure by controlling the junction size with the electrode and a defect density of the insulator film. The current is due to the charge carriers passing through the trap centers inherently present in the insulating film and is dominated by the space charge-limited conduction mechanism. The current through the insulating layer in the MIM structure flows bi-directionally, but a MIOS structure with an oxide semiconductor as the top electrode causes the current to flow in only one direction with a high rectification ratio of 5×10^6 at a voltage range between -40 V and 40 V. Because the surface charge of the top oxide semiconductor at the insulator interface changes depending on the polarity of the voltage, the current flows through the fully electron-accumulated surface by the positive voltage, but the fully electron-depleted surface at the negative voltage cuts off the current flow. Then, the vertical current levels can be easily modulated by varying the electron mobility of the top semiconductor electrode, and the rectified signal polarity and rectification ratio of the AC wave passing through the device can be controlled very precisely by the doping level of the top semiconductor electrode. Our new approach to the current flow through insulator films is a simple and universal technique that can be easily used in various electronic devices.

2.9 Experimental details

2.9.1 Deposition of various metal oxide, metal electrodes and insulator thin-films

All of the metal oxide films with a thickness of 20 nm, IGZO, ZTO, ZnO and ITO were sputtered by a RF magnetron sputtering system using an indium gallium zinc oxide (In:Ga:Zn:O = 1:1:1:4 at%), a zinc tin oxide ($ZnO:SnO_2$ = 2:3 mol%), a zinc oxide (ZnO) and an indium tin oxide ($In_2O_3:SnO_2$ = 9:1 wt%) targets, respectively, under 10^{-6} Torr at room temperature. The ITO-doped IGZO thin-films were co-sputtered using the IGZO and ITO targets simultaneously. The RF sputtering power of the IGZO target was fixed to 90 W and the DC sputtering power of the ITO target was varied from 0 W to 100 W. Thickness of all compositional ITO-doped IGZO thin-films was 20 nm. After deposition process, all of the metal oxide thin-films were annealed at 350 ℃ for 90 seconds in air using a rapid thermal annealing method. The Al electrode with a thickness of 20 nm was deposited via a vacuum thermal evaporation at 10^{-6} Torr. The 200-nm SiO_2 layer was grown onto the highly boron-doped p-type silicon (P^{++} Si) by a thermal oxidation process. The SiO_2 and Si_3N_4 layers were deposited by plasma enhanced chemical vapor deposition (PECVD) with SiH_4, N_2O and NH_3 gases. All of the top electrodes including semiconductor and metal thin-films were patterned by metal shadow masks in order to avoid unexpected side-contacts with the bottom electrode.

2.9.2 Preparation of substrate

The highly boron-doped p-type Si (P^{++} Si), highly phosphor-doped n-type Si (N^{++} Si) wafers and soda-lime glass substrates were sequentially cleaned with detergent,

de-ionized water, acetone, and isopropyl alcohol. And the size of all specimens was 2 x 2 cm^2.

2.9.3 Fabrications of the TFT devices

The TFTs have a bottom gate structure with the P^{++} Si (gate) / 200-nm SiO_2 (gate insulator) / 20-nm IGZO (active) / 100-nm Al (source and drain). The oxide semiconductor active layers were annealed before the source and drain process. The width and length of the channels in the TFTs are 1000 μm and 50 μm, respectively. The active layers were patterned with the same size as the source and drain electrodes in order to block the source-gate leakage current, which begins to flow through the gate insulator film when the active layer area exceeds 12.56 mm^2. The source-drain voltage was fixed to 0.1 V, and all of the transfer curves were measured at room temperature in a dark.

2.9.4 Fabrications of the MOS capacitors

The metal / oxide / semiconductor capacitors were fabricated with P^{++} Si / 200-nm SiO_2 / 20-nm ITO-doped IGZO semiconductors / 100-nm Al electrode structure. The area of the semiconductor and Al electrode layers was patterned in the same circle shape with a diameter of 1 mm in order to block the vertical current due to the large area semiconductor layer. The capacitance (*C*) values were measured at a frequency of 20 Hz small signal at room temperature in a dark and each *C* value was normalized by the maximum *C* value.

2.9.5 Characterization of the fabricated devices

The current-voltage characteristics for all devices were measured using the Agilent 4155B semiconductor parameter analyzer in a dark. The capacitance-voltage curves were analyzed using the Agilent 4284A precision LCR meter in a dark. The sine wave with a frequency of 100 Hz and amplitude of 20 V was input by the Agilent 33500B waveform generator and a voltage amplifier, and the output voltages were detected by the Tektronix DPO-2024 oscilloscope.

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Chapter 3. Influence of uni-directional gate current on the performance of oxide thin-film transistors

3.1 Overview

A thin-film transistor (TFT), which is one type of the metal-oxide-semiconductor field-effect transistor (MOSFET), is a key component for thin-film technology and its most important application is a switching element on display products. Recently released display products have used oxide semiconductor TFTs with high electron conductance in order to realize high resolution and transparency [1-4]. Most conventional oxide TFTs have a bottom gate structure consisting of a gate electrode, dielectric insulator, oxide semiconductor, and source and drain electrodes [5-7]. The oxide semiconductor active layer of the oxide TFTs designed for commercialization should be patterned to have a size similar to that of the source and drain electrodes in order to avoid fringe electric fields or parasitic capacitances [8-10]. These days, many research and development on the oxide TFTs have focused on improving manufacturing processes including solution coating technology [11-16]. The oxide TFTs in such a research stage are often fabricated with large pattern sizes or without a patterning process of the oxide semiconductor layer for their ease of research and manufacture [17, 18]. Theoretically, gate leakage currents are completely blocked in conventional bottom gate structure

TFTs regardless of the area size of active junction because a thick gate dielectric layer electrically insulates a gate electrode from a source electrode and a drain electrode. However, unconventional results of high gate leakage currents flowing in only one direction in the oxide TFTs with a large area of oxide semiconductor layer have been steadily reported by many groups [19, 20]. The unconventional gate leakage currents are normally reduced after patterning process in their reports [21]; however, the exact origins and the details of the uni-directional gate leakage current are still unknown. Herein, we study the origin of the unconventional gate leakage current and the effect of the gate current on the electrical performance of conventional oxide semiconductor TFT devices. We have, then, demonstrated that the gate current flowing in only one direction can be utilized as an electrostatic discharge diode (ESD) path to protect the oxide TFT from unexpected gate electrostatic shocks.

3.2 Interference of abnormal gate current to oxide TFT performance

To confirm an effect of the junction area size on the gate current phenomenon in bottom gate structured oxide TFTs, we compared oxide TFTs consisting of oxide semiconductor active layers with different areas (Figure 3.1a). Highly doped p-type silicon (P^{++} Si) was used as a substrate and a gate electrode, and thermally oxidized SiO_2 with a thickness of 200 nm was used as a gate insulator. The IGZO (In:Ga:Zn:O = 1:1:1:4 at%) oxide semiconductor with a thickness of 20 nm, which is used in most display products, was deposited on the SiO_2 using an RF magnetron sputtering system, and the IGZO layer was patterned on its sides to prevent inadvertent lateral contact with the gate electrode. Source and drain electrodes of Al metal with a thickness of 100 nm were formed on the oxide semiconductor film using a thermal evaporator, and a channel width and length of the electrodes are 1000 μm and 50 μm, respectively. In the oxide TFT with an active area of 1.5 mm^2, the oxide semiconductor layer has a similar area to the source and drain electrode area, whereas the compared oxide TFT has an IGZO area as wide as 36 mm^2. The electrical characteristics for the both TFTs were measured using a probe station at a source-drain voltage (V_{DS}) of 0.1 V to 40 V with the source-gate voltage (V_{GS}) sweeping from -40 V to 40 V. The transfer curves for the TFT with 1.5 mm^2 IGZO exhibit typical n-type oxide semiconductor TFT characteristics [22, 23]. A drain current (I_D) at a positive V_{GS} region, which is measured at the drain electrode, increases proportionally as the V_{DS} increases from 0.1 V to 40 V, and the off-state currents at a negative V_{GS} range remain very low levels of 10 pA (Figure 3.1b). Source current value (I_S), which is measured at the source electrode, equals to

amounts of the drain currents (I_D) escaped from the drain electrode (Figure 3.1c). The gate currents (I_G), commonly referred to as a leakage current, are negligible under ~ pA level at the entire V_{GS} range (Figure 3.1d). Therefore, it is verified that the SiO_2 gate insulator layer blocks well the transportation of any electrical charge carriers including electrons, holes, and ionized carriers between the gate and the source or drain electrodes. The results demonstrate that the operation of the oxide TFT with 1.5mm^2 IGZO active layer agrees well with the basic TFT operating principle that the channel conductivity is controlled in proportion to the V_{GS}.

On contrary, the drain currents of the TFT with 36 mm^2 IGZO area show completely different behavior with the TFT with 1.5 mm^2 IGZO film. In the off-state under a negative V_{GS} range, the I_D are almost the same as the I_D for the TFT with 1.5 mm^2 IGZO; however, the on-state I_D at a positive V_{GS} range appears to be distorted in a log scale, and the degree of distortion becomes serious as the V_{DS} decreases toward 0.1 V (Figure 3.1e). The drain current curves in a linear axis show that the drain current begins to decrease from a specific V_{GS}. Furthermore, the I_S values are much higher than the I_D values flowing out from the drain electrode (Figure 3.1f), which implies that another current flows in or out at both the drain and source electrodes. The significant difference of the *I-V* characteristics with the oxide TFT having 1.5 mm^2 IGZO layer is clearly shown in the gate current curves. The gate current of the oxide TFT having 36 mm^2 IGZO active layer hardly flows in the negative V_{GS} region but begins to increase sharply at V_{GS} = 0 V, and a very high current of 1.5×10^{-4} A flows at V_{GS} = 40 V (Figure 3.1g). The unusual gate current characteristic indicates that electrical charge carriers are actively transported through the 200-nm SiO_2 layer between the gate electrode and the drain

or source electrodes at a positive V_{GS}. This result is in contradiction with the result of the TFT with a 1.5 mm^2 IGZO in which 200-nm SiO_2 maintains good insulating property and completely blocks the leakage current; thus, it can be deduced that the contact size at the active / gate insulator junction directly affects the gate leakage current flow. The high I_G and the distorted I_D characteristics are also measured in the oxide TFTs having 36 mm^2 active layer using a 20 nm thick n-type oxide semiconductors including zinc oxide (ZnO), Al-doped ZnO (AZO), zinc tin oxide (ZTO) and indium zinc oxide (IZO) (Figure 3.2). All of the TFTs using ZnO, AZO, ZTO, and IZO active layers also exhibit a typical n-type oxide semiconductor TFT curve pattern: drain currents hardly flow at a negative V_{GS} and increase in proportion to a positive V_{GS}. However, the drain current begins to decrease at a specific V_{GS} due to the uni-directional gate currents, and the influence of the gate current on the drain current increases as the V_{DS} decreases toward 0.1 V. The ZnO, AZO and ZTO films were deposited by an RF sputtering method, and the IZO layer was coated through a solution coating process; thus, it can be also confirmed that the deposition technique has little effect on the flow of the unconventional gate current.

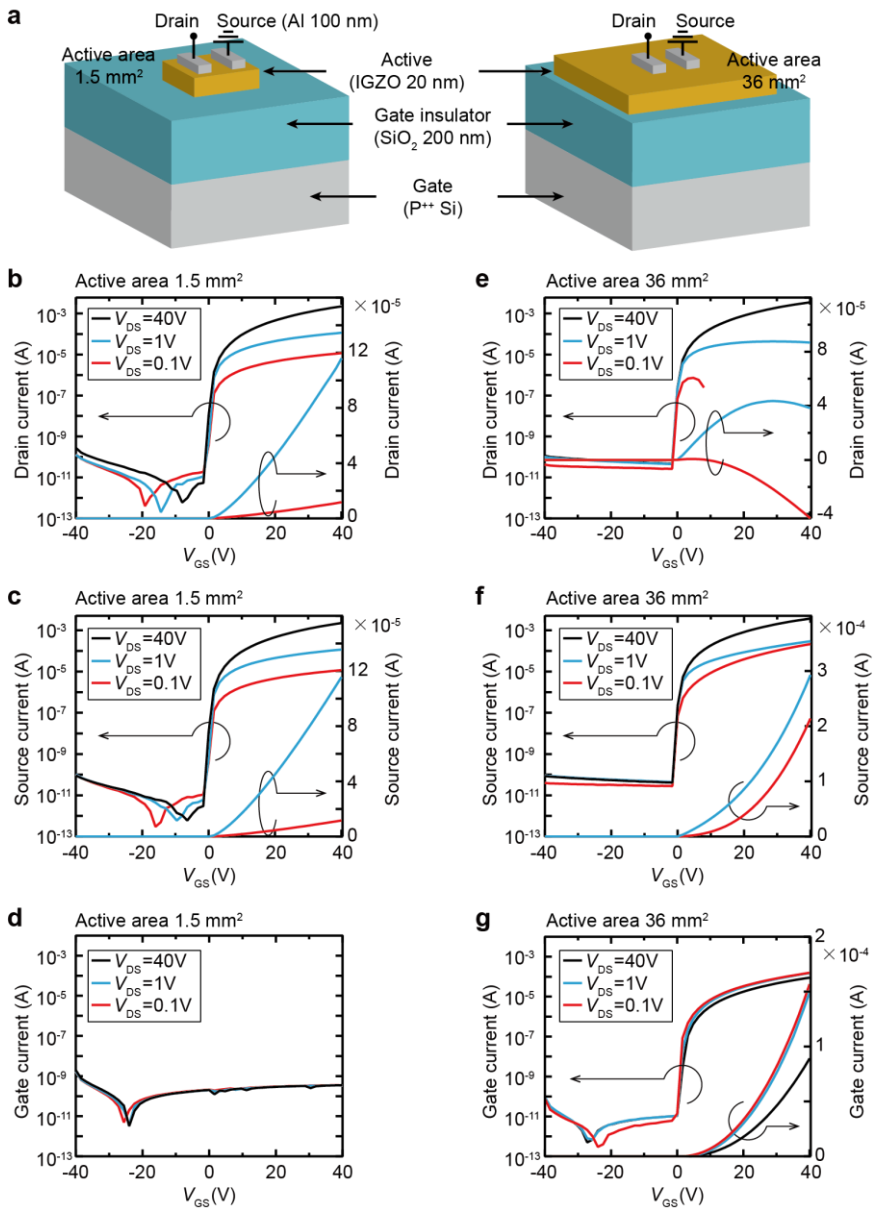

Figure 3.1. The electrical characteristics of the two oxide TFTs with different active layer area. (a) Schematic structures of the TFTs with different active layer area of 1.5 mm^2 and 36 mm^2. (b-d) Electrical currents measured at (b) drain, (c) source and (d) gate electrodes in the TFT with 1.5 mm^2 IGZO active layer. (e-g) Electrical currents measured at (b) drain, (c) source and (d) gate electrodes in the TFT with 36 mm^2 IGZO active layer.

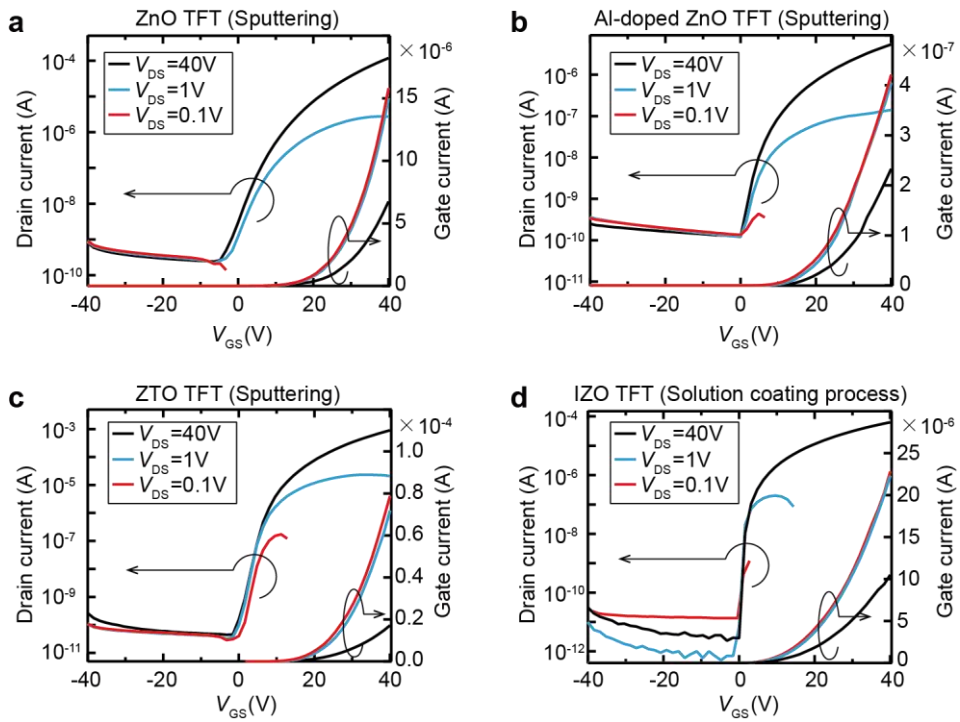

Figure 3.2. Drain current and gate current characteristics in bottom gate oxide TFTs using 20-nm (a) ZnO, (b) Al-doped ZnO, (c) ZTO and (d) IZO as active layers.

3.3 Flowing direction of each current in the oxide TFTs

To confirm clearly flowing direction of each current in the oxide TFTs, the output source (I_S) and gate (I_G) currents were measured at the source and gate electrodes, respectively, in response to the input drain current (I_D) of 10^{-10} A to 10^{-2} A (Figure 3.3a). In the TFT with 1.5 mm^2 IGZO active layer, the I_S (solid lines) linearly increases in proportion to the I_D, and the saturation value of the I_S increases depending on the V_{GS}, but the I_G (dashed lines) is kept at a very low value of ~ 10 pA (Figure 3.3b). The I_S-I_D relation shows a typical channel conductance behavior controlled by the V_{GS} value in a conventional TFT device, and there are no leakage current through the SiO_2 insulator film toward the gate electrode. The equivalent circuit of the oxide TFT is depicted as shown in Figure 3.3c, and the only current path in the TFT with 1.5 mm^2 IGZO active layer is the channel layer consisting of the 20-nm IGZO. On the other hand, in the oxide TFT with the IGZO channel layer of 36 mm^2 area, the very high I_G flows out toward the drain electrode and the source electrode (Figure 3.3d). The output I_G and I_S at V_{GS} of 0 V exhibit equivalent values as that of the TFT with 1.5 mm^2 IGZO film (red lines): the I_S is proportional to the applied I_D and the I_G is very low level. However, as the V_{GS} increases to 4 V, the I_G and I_S output the same current level of 9×10^{-7} A in the input I_D range from 10^{-10} A to 10^{-6} A, and the I_S begins to linearly proportional to the I_D from 10^{-6} A. The output current characteristics demonstrate that unexpected currents flow from the gate electrode to both the drain electrode and the source electrode. The applied V_{GS} induces a vertical electric field between the source and the gate electrodes, and the vertical electric field causes the unconventional gate current to flow through the

200-nm SiO_2 layer to a constant current value of 9×10^{-7} A, despite the low current levels of the input I_D. Therefore, in the I_D range where the amount of current from the drain electrode to the source electrode (I_{DS}) is less than 9×10^{-7} A, which is the amount of vertical current from the gate to the source electrode (I_{GS}), the I_S depends on the I_G value. Because the induced I_{GS} by the vertical electric field between the gate and the source electrodes is constant, the I_S approaches a linear proportion to the I_D from 10^{-6} A level. To verify the portion contributed by the I_G to the I_S values, the difference between I_S and I_G was extracted and plotted along the I_D (Figure 3.3e). The extracted curves exhibit a linear relationship with the I_D as same to the TFT with no gate current in Figure 3.3b, which proves that the measured I_S contains both the I_D from the drain electrode and the I_G from the gate electrode. Consequently, in the TFT having a large active area (36 mm^2), there are three current paths: between the drain and source electrodes (I_{DS}); between the drain and gate electrodes (I_{GD}); between the source and gate electrodes (I_{GS}). The equivalent circuit for the TFT with the uni-directional gate current can be described as including the vertical current paths like a diode (Figure 3.3f). As can be expected from the equivalent circuit, the I_D begins to decrease from the operating region where the I_{GD} injected into the drain electrode is larger than the I_{DS} flowing out from the drain electrode, therefore, the I_D curve in log axis seems to be distorted in Figure 3.1e.

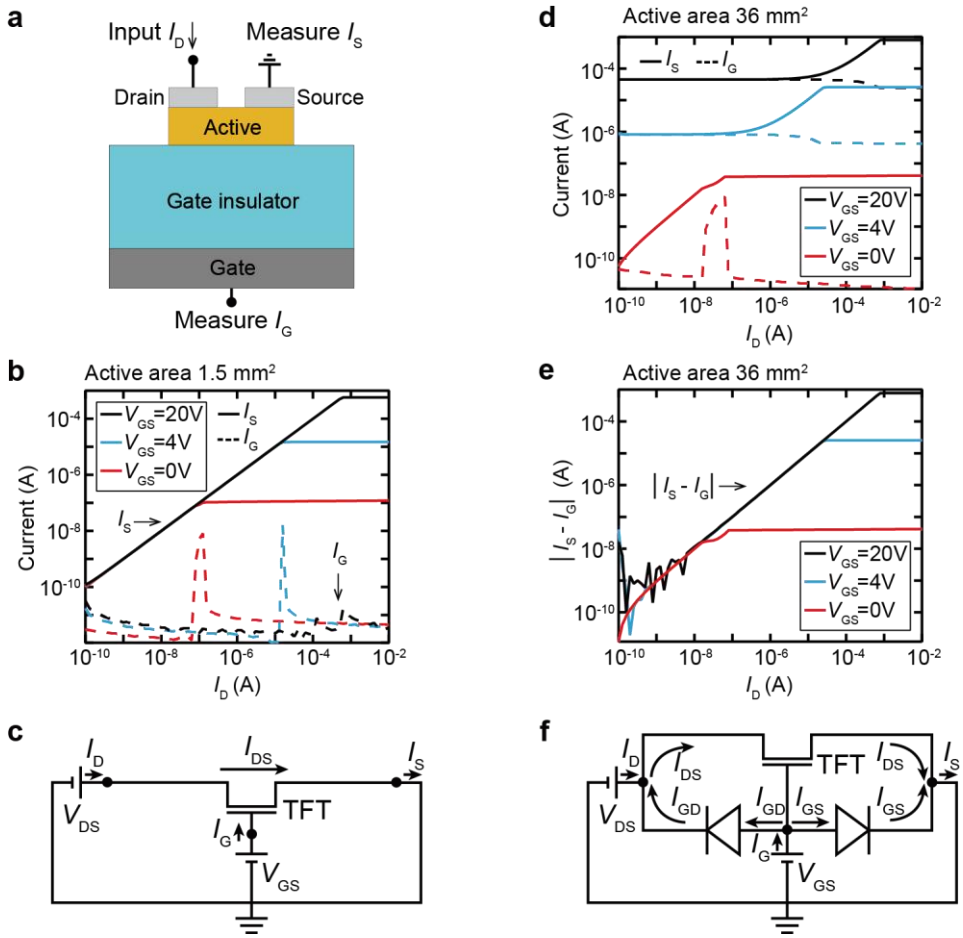

Figure 3.3. Current flowing direction in the TFTs with 1.5 mm^2 and 36 mm^2 IGZO active layers. (a) Schematic image of induced and measured currents. (b, c) Results of the TFT with 1.5 mm^2 active layer. (b) The source and gate currents measured at the source and gate electrodes in response to the applied drain current. (c) Direction of the current flowing in an equivalent circuit. (d-f) Results of the TFT with 36 mm^2 active layer. (d) The source and gate currents measured at the source and gate electrodes in response to the applied drain current. (e) Calculated difference between the source and gate currents. (f) Direction of the current flowing in an equivalent circuit.

3.4 Origins of the uni-directional gate current in the oxide TFT

In Chapter 2, we have found that the unexpected vertical current can flow stably as the electrode contact size increases in the MIM and MIOS devices even with thick insulating films. Especially, the investigated MIOS device in Chapter 2 has the same structure as the bottom gate oxide TFT consisted of gate electrode / gate dielectric / active semiconductor / source or drain electrode. Therefore, the uni-directional vertical current flows also in the bottom gate structured oxide TFT as the area of the oxide semiconductor layer increases. In the bottom gate oxide TFT, uni-directional gate current flows only in one direction from the gate electrode to the drain or source electrode, as the uni-directional vertical current flows from the bottom electrode to the top electrode in the MIOS device. The uni-directional gate current is caused by electrons in the bottom gate oxide TFT. Therefore, the gate leakage current flows only when the gate voltage (V_G) is higher than the voltage of the source electrode or the drain electrode. The conduction mechanism of the vertical current follows the SCLC mechanism. Therefore, the I_G - V_{GS} characteristics plotted on the log-log axis should have a linear relationship of slope of around 2.0. In our experiments, the slopes of the linearly fitted I_G - V_{GS} curves are around 2.3 (Figure 3.4), which demonstrates the unusual gate current in the oxide TFT depends on the space charge-limited conduction. Consequently, the origin of the uni-directional gate current in the oxide TFT can be judged as electrons passing through the trap sites present in the SiO_2 gate dielectric film, and the conduction of electrons is governed by the space charge-limited conduction mechanism.

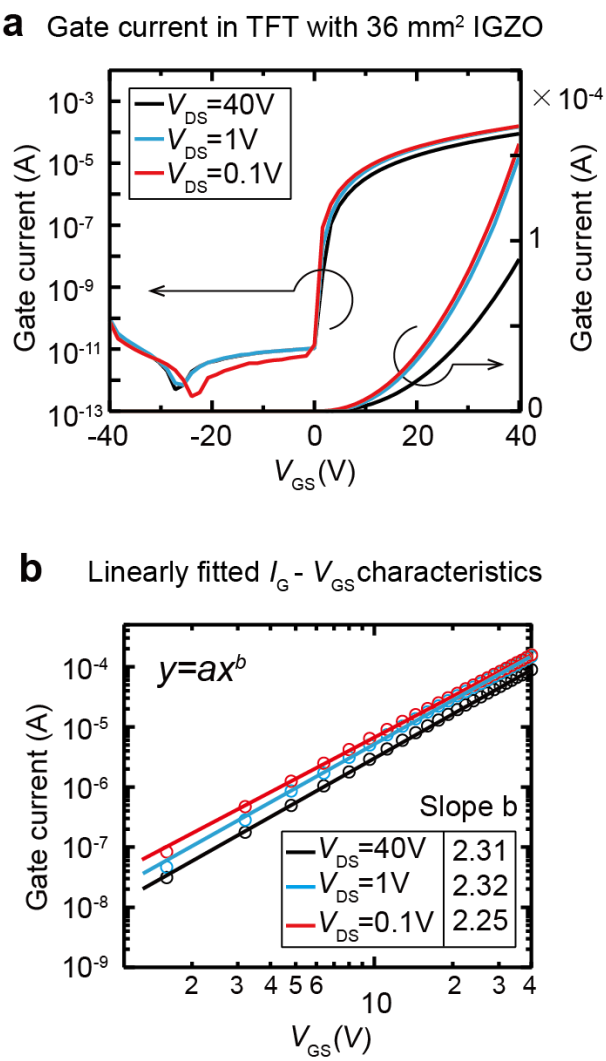

Figure 3.4. (a) Gate current flows in the TFT with 36 mm^2 IGZO active layer. (b) The linearly plotted gate current – gate voltage curves in log-log axes.

3.5 Investigation the vertical current phenomena through AlO_X dielectric films

In order to verify whether the abnormal vertical current flow through the dielectric films is limited to the SiO_2 material, we investigated a representative gate dielectric material, AlO_X. The AlO_X thin-films were deposited by atomic layer deposition (ALD) method and solution coating method in order to confirm the influence of the growth process of dielectric thin films. The thickness of AlO_X films is equal to 20 nm. The 100 nm thick Al film was used as top electrode in the investigated MIM devices. The Al top electrode size with circle shape was compared from 0.5 mm diameter to 2 mm diameter. We measured and compared 15 devices for each condition. In the MIM devices with the smallest Al contact area of 0.5 mm diameter, the vertical current hardly flows in the both AlO_X dielectric films formed by ALD method and the solution process (Figure 3.5a and d). However, as the contact area increases, the bi-directional vertical current begins to flow and the probability of high current flow increases significantly in both AlO_X films (Figure 3.5b, c, e and f). The cumulative distributions clearly show that the tendency of the vertical current flowing in the MIM device is equal even if the AlO_X film is deposited in different process (Figure 3.5g and h). Further, the MIOS devices using AlO_X dielectric films, which are deposited by ALD and solution process, exhibit the same *I - V* characteristics: the vertical current flows in only one direction from the bottom electrode to the top electrode (Figure 3.5i). Therefore, it is confirmed that the abnormal vertical current flowing through the dielectric film is a universal electric phenomenon that can occur in the MIM or MIOS structure regardless of the insulator material or the growing method.

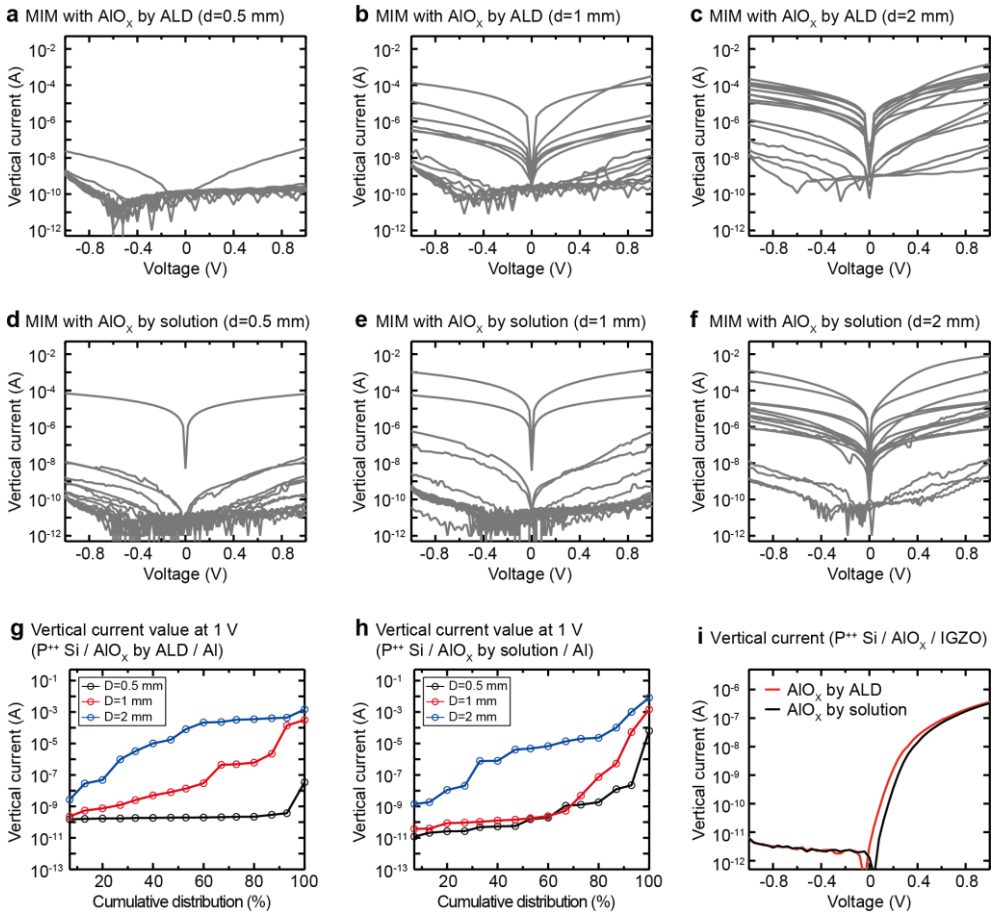

Figure 3.5. Comparison of leakage current through AlO_X films by grown ALD method and solution process in the MIM (P^{++} Si / 20-nm AlO_X / 100-nm Al) structures. The AlO_X films were formed by (a-c) ALD and (d-f) solution process. The Al electrodes have circular shapes in a diameter (a,d) 0.5 mm, (b,e) 1 mm, and (c,f) 2 mm, and 15 devices were measured for each size. The cumulative distribution graphs for the leakage current value measured at 1 V for the MIM structures with (g) ALD-deposited AlO_X and (h) solution-coated AlO_X. (i) The *I-V* curves for the MIS devices using AlO_X dielectric films.

3.6 Electrical charge states at the interface of the SiO_2

The capacitance (*C*)–voltage (*V*) characteristics were measured at 20 Hz for the metal (P^{++} Si)-oxide (200-nm SiO_2)-semiconductor (IGZO)-metal (source electrode) capacitor (MOSCAP) structures in each TFT with 1.5 mm^2 and 36 mm^2 IGZO active layers to compare the charge states at the SiO_2 interface. The capacitances of two MOSCAPs measured in a negative V_{GS} range exhibit the same minimum values (Figure 3.6a), which means that electrons, majority carriers in the IGZO layer, are fully depleted from the SiO_2 interface. The fully depleted IGZO layer at the interface with the SiO_2 creates an additional depletion capacitance (C_{dep}) that is connected in series with the insulator capacitance (C_{ox}). The C_{dep} values are the same regardless of the area of the IGZO layer; therefore, the depletion states of the two MOSCAPs are the same (Figure 3.6b and c). However, in a positive V_{GS} region, the *C* values of two MOSCAPs exhibit exactly the opposite behavior. The *C* value for the MOSCAP having 1.5 mm^2 area IGZO layer is maintained at 3.9×10^{-8} Fcm^{-2}, which indicates that the electrons in the IGZO layer are accumulated at the interface and the total capacitance value corresponds to C_{ox} of 200 nm thick SiO_2 (Figure 3.6d). On the other hand, the *C* of the MOSCAP with 36 mm^2 area IGZO film increases steadily with the positive V_{GS} and reaches 1.7×10^{-5} Fcm^{-2} at 5 V. The increasing *C* behavior demonstrates that the electrons flow steadily from the accumulated IGZO interface into the gate electrode through the SiO_2 film. The SiO_2 layer serves not only as a gate dielectric in the TFT structure, but also as an electron transport layer such as a diode (Figure 3.6e). Therefore, when a bottom gate TFT operates at a positive V_{GS}, electrons flow from the source electrode to the

drain electrode through the IGZO channel layer and also flow into the bottom gate through the SiO_2 layer, resulting in the flow of the uni-directional gate current. Furthermore, in the operating region where the vertical field due to V_{GS} is larger than the transverse field due to V_{DS}, electrons flow from the drain electrode toward the gate electrode, and the I_D characteristic begins to decrease (Figure 3.1e).

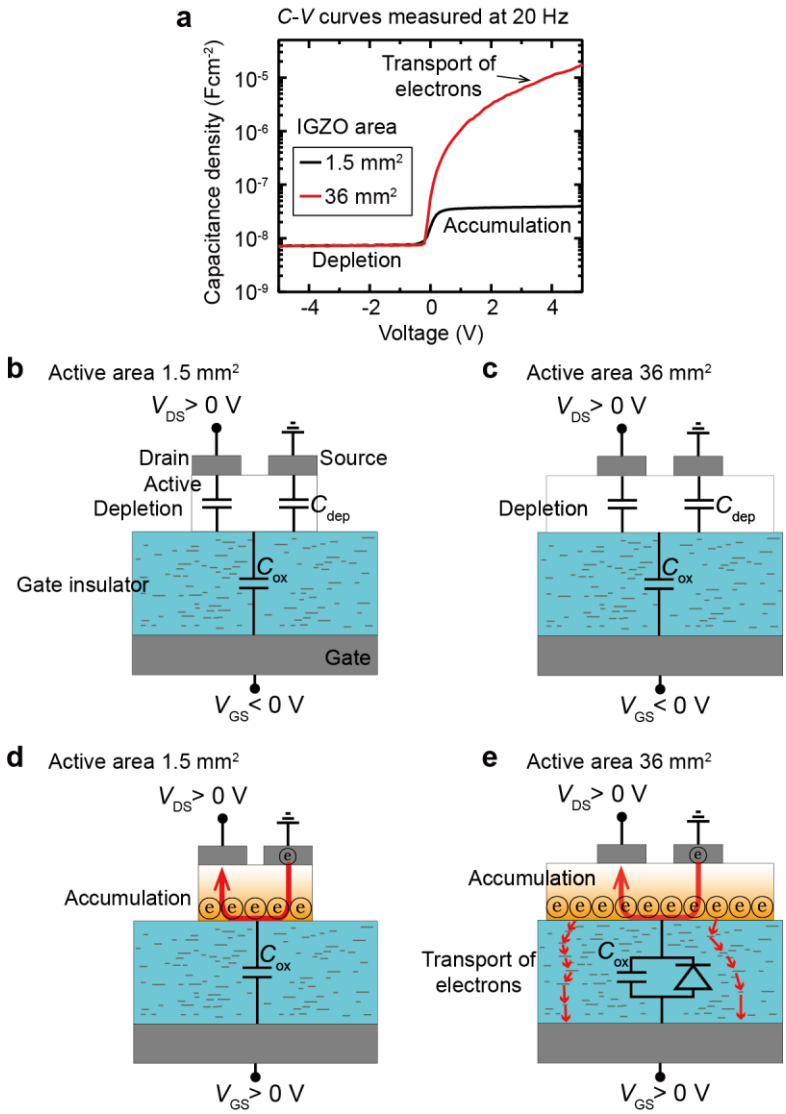

Figure 3.6. Capacitance density (*C*)–voltage (*V*) curves and schematic images for the transport of electron in each TFT device. (a) *C-V* characteristics of MOSCAP in each TFT device with different IGZO size of 1.5 mm^2 and 36 mm^2. (b, c) Depletion states and capacitances for turn-off condition of the TFTs with (b) 1.5 mm^2 and (c) 36 mm^2 IGZO area. (d, e) Accumulation states and electron transport for turn-on condition of the TFTs with (d) 1.5 mm^2 and (e) 36 mm^2 IGZO area.

3.7 Influence of the structural parameters of TFT on the gate current

The uni-directional gate current in the oxide TFT is due to the transport of electrons between the gate electrode and the drain or source electrodes. Therefore, the gate current is influenced by the magnitude of electric fields in the oxide TFT and is controlled by the structural parameters of the oxide TFT including the thickness of gate dielectric, the channel length, and the thickness of active layer. The gate current depends on the vertical electric field applied to the SiO_2 gate dielectric, and the vertical electric field varies with the thickness of the SiO_2 gate dielectric. Because the vertical electric field between the gate electrode and the source electrode increases as the thickness of the SiO_2 decreases, the gate current through the SiO_2 gate dielectric increases steadily as the thickness of the gate dielectric decreases from 200 nm to 50 nm (Figure 3.7a). The uni-directional gate current flows stably in the oxide TFT with a large area (36 mm^2) IGZO active layer, but there is absence of the gate current in the oxide TFT with a small area (1.5 mm^2) IGZO active layer. Therefore, the drain current proportionally increases with the V_{GS} in a TFT having an active layer of a small area, whereas in a TFT with a large area active layer, the drain current starts to decrease from a low V_{GS} due to the influence of the gate current (Figure 3.7b). In order to control the transverse electric field between the drain electrode and the source electrode, the channel length varied from 5 μm to 50 μm. The investigated TFTs have a IGZO active layer of 36 mm^2 area and a SiO_2 dielectric layer of 200 nm thickness. The vertical electric field through the SiO_2 layer is invariant regardless of the channel length, therefore, the uni-directional gate currents are equivalent for all channel legnths

(Figure 3.7c). On the other hand, as the channel length increases from 5 μm to 50 μm, the transverse electric field decreases and the drain current through the channel layer decreases; thus, as the channel length increases, the gate current value becomes larger than the drain current value, and the drain current is seriously affected by the gate current and decreases at a smaller V_{GS} (Figure 3.7d). We also investigated the effect of IGZO thickness on the gate current flow in the oxide TFT. The uni-directional gate current is due to the accumulated electrons at the interface with the SiO_2 insulator, and the accumulated surface electron state is similar for all thickness of IGZO layer; thus, the gate current values are similar regardless of the IGZO layer thickness from 10 nm to 80 nm, and the thickness of IGZO active layer has little effect on the change in the gate current (Figure 3.7e and f).

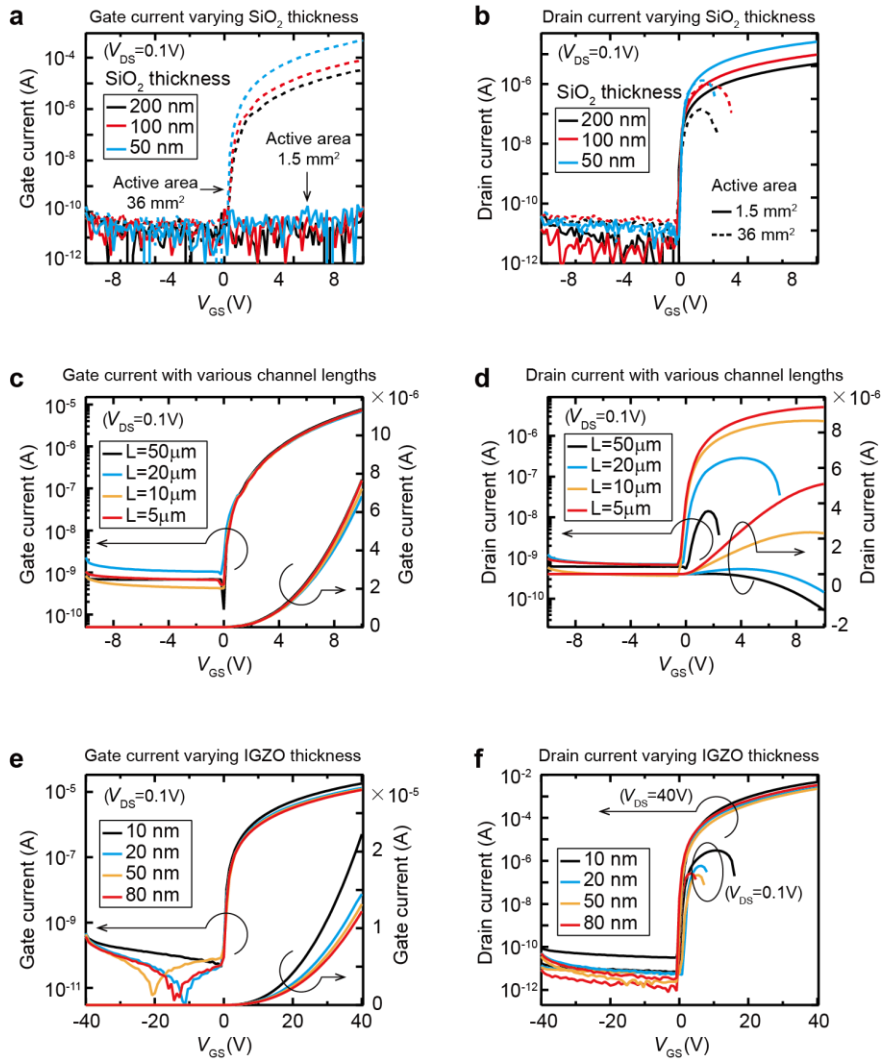

Figure 3.7. Gate and drain current behavior with variation of structural parameters of the oxide TFT. (a,b) The electrical characteristics of the TFTs with various thick SiO_2. (a) Gate current and (b) drain current behavior for the TFTs with 1.5 mm^2 and 36 mm^2 IGZO area. (c) Gate current and (d) drain current of the TFTs with various channel lengths. (e) Gate current and (f) drain current values of the TFTs with various thick IGZO layers.

3.8 Demonstration of gate current path as an ESD diode component

Although the high gate current path increases the power consumption of the TFT, it has a potential as an electrostatic discharging (ESD) diode of a driving circuit. Therefore, we demonstrated that the stable gate current path through the thick SiO_2 layer prevents a dielectric breakdown of SiO_2 film from an excessive static charge coming in the gate direction. The oxide TFTs having 100 nm thick SiO_2 gate dielectric were investigated. The I_D, I_S, and V_G outputs in response to the applied I_G were measured at the drain, source, and gate electrodes, respectively, while the I_G of 10^{-10} A to 10^{-3} A was applied to the gate electrode. The drain voltage was maintained at 0 V. In the TFT with a small area (1.5 mm^2) IGZO layer, the applied I_G causes a sharp increase in V_G because electrical charge carriers cannot move vertically; thus, V_G reaches about 80 V at the I_G of 10^{-7} A (Figure 3.8a). Then, a sudden voltage drop in V_G occurs near the I_G of 2×10^{-7} A, and the I_D begins to increase linearly with I_G, while I_S maintains the low current states. The result indicates that an excessive vertical electric field between the gate and drain electrodes, which is induced by the I_G, leads to a sudden dielectric breakdown of the SiO_2 film, and most of the I_G is leaked to the drain electrode. With the dielectric breakdown, the TFT characteristics before and after the I_G stress drastically changed: both of the I_G and I_D exhibit an Ohmic-like conduction due to electrical shorting (Figure 3.8b). In contrast, in the TFT with a large area (36 mm^2) IGZO layer, the I_D and I_S increase linearly in proportion to the I_G, which indicates that the input I_G escapes simultaneously to the drain and source electrodes. The I_G-induced potential V_G is lower than that of the TFT with a small area IGZO and reaches

about 40 V at the I_G of 10^{-3}A (Figure 3.8c). Thus, the path of the gate current through the SiO_2 insulator functions as a diode for discharging the electrostatic overcurrent, and the TFT is protected from an electric breakdown and maintains its output capability before and after the I_G stress (Figure 3.8d).

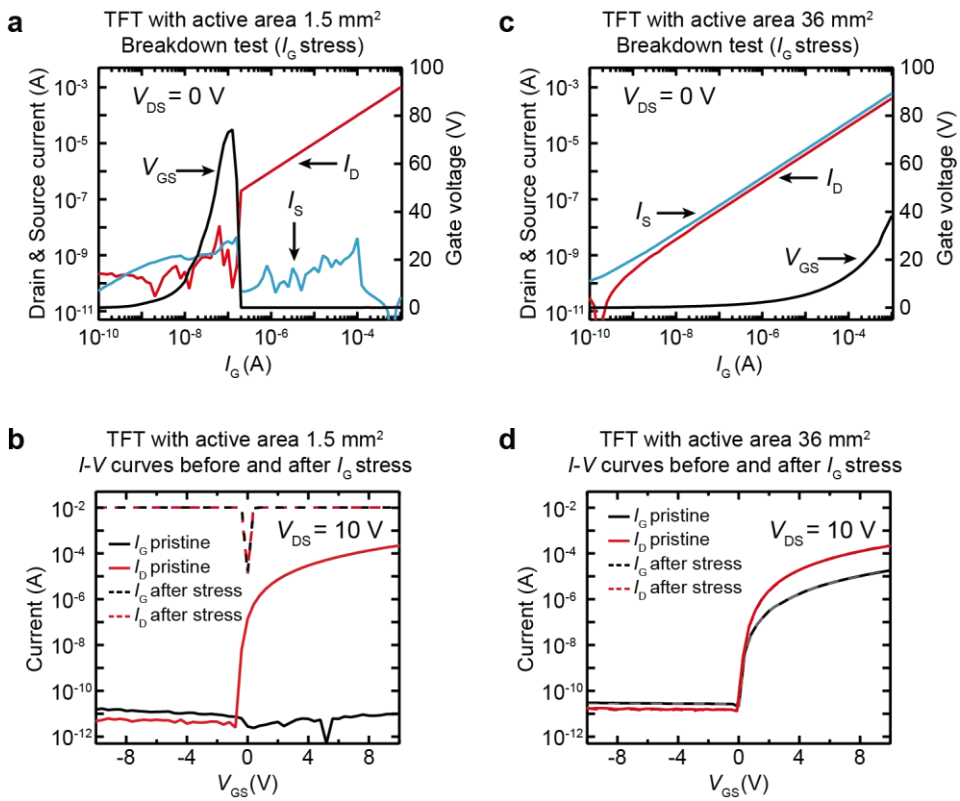

Figure 3.8. Demonstrating applicability of the unusual gate current paths as an electrostatic protection circuit. (a, b) Results of I_G stress test for the TFT with 1.5 mm^2 active layer. (a) Dielectric breakdown occurs between the gate and drain electrodes as I_G increases. (b) An electrical shorting occurs between the gate and drain electrodes due to the dielectric breakdown by I_G stress. (c, d) Results of I_G stress test for the TFT with 36 mm^2 active layer. (c) The gate current flows to the drain and source electrodes at the same time without a dielectric breakdown. (d) The TFT output values exhibit the same value before and after I_G stress.

3.9 Conclusion

In summary, it is studied that a high leakage current flows very reliably through a thick gate dielectric film between a gate and source or drain electrodes without any dielectric breakdown in a conventional oxide TFT with a bottom gate structure. The origin of the high gate leakage current is due to the transport of injected electrons from the source and drain electrodes, and the electrons are transported through trap sites inherently present in the dielectric layer. The uni-directional leakage current in oxide TFTs interferes with the electrical performance of the oxide TFTs, thus, the oxide semiconductor active layer should be patterned to prevent the interference of the gate current. Although the unconventional gate current increases the power consumption of the TFT, the uni-directional gate current path can efficiently discharge the excessive charges and protect the TFT from the permanent breakdown when an excessive electrostatic charge is applied in the gate direction. Our study of the origins of abnormal gate currents provides a clear interpretation and simple solution for unknown factor in oxide TFT structures and oxide-insulator junctions.

3.10 Experimental details

3.10.1 Deposition of various oxide semiconductors

The depositions of the oxide semiconductor layers were done as follows: 20-nm ZnO, ZTO, AZO and IGZO films were deposited by RF magnetron sputtering system using zinc oxide, zinc tin oxide ($ZnO:SnO_2$ = 2:3 mol%), aluminum doped-zinc oxide (Al:ZnO = 2:98 at%) and indium gallium zinc oxide (In:Ga:Zn:O = 1:1:1:4 at%) targets, respectively, under 10^{-6} Torr in room temperature. High purity Ar gas was the only reactive sputtering gas. After deposition process, ZnO and IGZO films were annealed at 350 ℃ for 90 seconds in air, ZTO film was annealed at 500 ℃ for 600 seconds, and AZO layer was annealed at 200 ℃ for 180 seconds in air through a rapid thermal annealing (RTA) method. The IZO (0.2 M $In_{0.7}Zn_{0.3}O$) of 20 nm thickness was coated using a sol-gel coating process: the precursor solution was synthesized by dissolving 0.84 g of indium nitrate hydrate ($In(NO_3)_3 \times H_2O$, Aldrich, 99.999%) and 0.36 g of zinc nitrate dihydrate ($Zn(NO_3)_2 \times H_2O$, Aldrich, 99.999%) in 10 ml of 2-methoxyethanol. After coating the IZO solution, the coated film was annealed at 200 ℃ for 1 hour in a hot plate.

3.10.2 Deposition of dielectric films

The silicon dioxide (SiO_2) was oxidized onto P^{++} Si wafer at 1100 ℃ by a conventional thermal oxidation process, and deposited by PECVD using SiH_4 and N_2O gases. The aluminum oxide (AlO_X) dielectric films were deposited by atomic layer deposition (ALD) technique and solution process which is to dissolve 0.2 M aluminum nitrate nonahydrate in 10 mL of the 18.2 MΩ deionized water at 25 ℃.

3.10.3 Fabrication of thin-film transistors (TFTs).

Highly Boron-doped p-type semiconductor substrate with resistivity of 0.005 Ωcm. The SiO_2 dielectric films were formed onto P^{++} Si wafer, and the oxide semiconductor films were patterned as an active layer, then the source and drain electrodes of 100 nm thickness were grown by a thermal evaporation tool under 10^{-6} Torr in room temperature. The width and length of the channel in TFTs are 1000 μm and 50 μm, and the narrower channel lengths of 5, 10, 20, and 50 μm were patterned by a conventional photolithography and wet etching process. Most of the source and drain electrodes and all of the oxide semiconductor films were patterned by metal shadow masks in order to avoid unexpected side-contacts with gate electrode.

3.10.4 Characterization of the fabricated TFTs

The current - voltage and capacitance - voltage characteristics for all devices were measured using the Agilent 4155B semiconductor parameter analyzer and the Agilent 4284A precision LCR meter in a dark.

3.11 Reference

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Chapter 4. Directional characteristics of vertical electrical current in oxide multilayer thin-film devices

4.1 Overview

In recent, various devices using novel metal oxides have been developed as a prominent candidate of post-Si electronics [1-4]. Metal oxide thin-films have been mainly adopted as an active layer for the purpose of high electron transportation [5, 6], while most insulator films such as SiO_2, HfO_2 and Al_2O_3 have long been considered only electrical insulating layers because of their intrinsic low electron affinities [7, 8]. Very high energy barriers built at the interfaces of insulator / semiconductor and insulator / metal have been a major cause preventing electron transfer through the insulator films [9, 10]. Thus, conventional insulators, which are located between metal and oxide semiconductor films, block a leakage current in various metal / insulator / oxide semiconductor structures. In contrast, we previously revealed that unconventional vertical electrical current phenomena at the hetero-interface between insulator and oxide semiconductor thin-films [11]. In the explored metal / insulator / oxide semiconductor (MIOS) structures, the electrons pass through the insulator / oxide semiconductor hetero-junction uni-directionally, and high current flows vertically in the MIOS structures. The results mean that the energy barrier at the interface of insulator and oxide semiconductor

becomes nearly negligible and the electrical conduction follows a bulk-limited conduction mechanism. Thus, the insulator layers in the MIOS structures can transport a great amount of electrons, which ask fundamental questions about the fixed concept of oxide insulators.

Here we report that the vertical current characteristics flowing in the metal / insulator / oxide semiconductor / insulator / metal (MIOSIM) structures. In the MIOSIM structures, the vertical current have directional characteristics of unidirectional or bidirectional flowing. The uni-directional and bi-directional characteristics of the vertical currents are controlled by the junction sequences of oxide semiconductors and insulators. The vertical current in the integration of single insulator / oxide semiconductor junction is uni-directional, on the other hand, that in the sequential integration of insulator / oxide semiconductor / insulator junctions is bi-directional. These findings imply that the traditional insulator films can be stable electron-transporting layers with inherent insulating properties and the conventional oxide multilayer thin-film structures have a huge potential to be a novel vertical electronic device.

4.2 Directional characteristics of vertical currents in MIOSIM structures

To investigate the vertical electric characteristics at the junctions in the MIOSIM structures, we fabricated the representative structures consisting of metal electrode (P^{++} Si) / 1st insulator (100-nm thick SiO_2) / oxide semiconductor (30-nm thick indium gallium zinc oxide) / 2nd insulator (100-nm thick SiO_2) / metal electrode (50-nm thick Al), namely MIOSIM devices (Figure 4.1a). The 1st and 2nd SiO_2 layers were deposited via plasma enhanced chemical vapor deposition (PECVD) process on the highly doped p-type silicon substrate and the oxide semiconductor (OS) layer, respectively. The OS layer was grown by RF magnetron sputtering system. Each of the insulator and OS layer was patterned to avoid unintended side-contacts. Patterned Al metal electrodes on the insulator and the OS layers completed the fabrication process. When the positive voltage is applied to the bottom electrode (P^{++} Si) and the Al electrode on the IGZO layer is grounded in the P^{++} Si / 1st SiO_2 / IGZO / Al (MIOSM) structure, the electrical current flows very highly. Conversely, when the bottom electrode is negatively biased, the current hardly flows (red line in Figure 4.1b). This means that the electrical charge carriers flow only one direction through the 1st SiO_2 layer with 100 nm thickness. This current flow is well consistent with the recent result that our group revealed: the electrical charge carriers can be transferred uni-directionally through the overlapped trap sites of the SiO_2 layer in the MIOS structure and the electrical current mechanism is dependent on a space charge-limited conduction mechanism [11]. Meanwhile, the uni-directional current phenomenon also occurs in the junction structure of Al / IGZO / 2nd SiO_2 / top Al (MOSIM). When the Al

electrode on the IGZO layer is biased positively and the top Al electrode on the 2nd SiO_2 layer is connected to ground, electrical current hardly flows. However, the high electrical current flows very stably in reversed bias condition: the Al on the IGZO film is grounded and the Al on the 2nd SiO_2 layer is positively biased (blue line in Figure 4.1b). The uni-directional electrical current flow is the same to that of the Al / IGZO / 1st SiO_2 / P^{++} Si junction structure but the direction of electrical current is opposite. This result verifies that the junction sequence between the IGZO semiconductor layer and the SiO_2 insulator layer controls the directional of the uni-directional vertical current. In addition, the SiO_2 layers stably vertically transfer large amount of electrical charge carriers in the MIOSIM structure, which indicates that the 100 nm thick SiO_2 layers act an electron-transporting layer between the electrodes and the IGZO semiconductor layer. Based on the transporting characteristic of the SiO_2 layer, the vertical current flows bi-directionally in the system of the MIOSIM junction: when the positive voltage is applied to the bottom electrode (P^{++} Si) and the top Al electrode on the 2nd SiO_2 layer is grounded, the electrons are transferred from the top Al layer through the 2nd SiO_2, IGZO, and 1st SiO_2 layers into the P^{++} Si electrode; when the negative voltage is applied to the bottom electrode and the top Al electrode is connected to ground, the electrons flows in opposite direction.

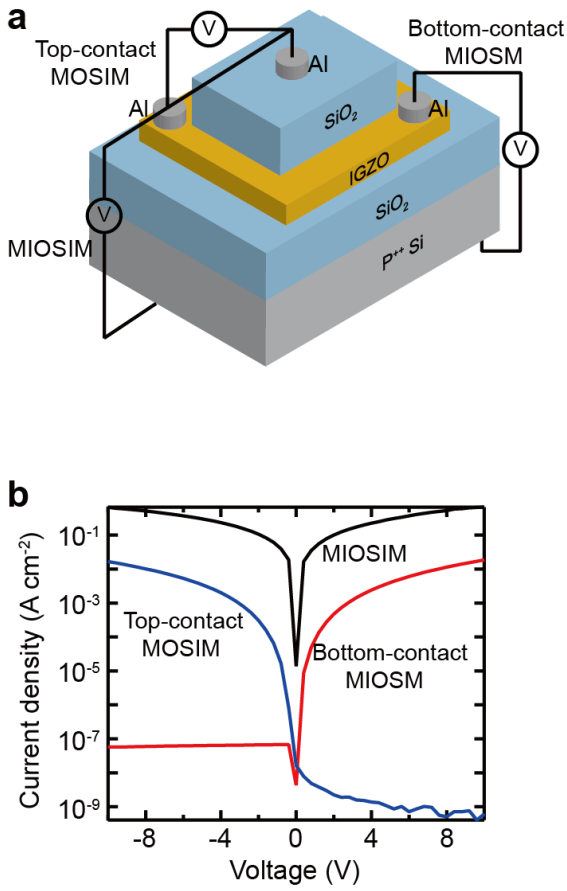

Figure 4.1. Current density (*J*)-voltage (*V*) characteristics in MIOSIM structure. (a) Schematic structure of the MIOSIM device consisting of bottom electrode (P^{++} Si) / bottom 100 nm thick SiO_2 / 30 nm thick IGZO / top 100 nm thick SiO_2 / top electrode (50-nm Al). (b) The *J*-*V* characteristics of the bottom-contact MIOSM, top-contact MOSIM, and the MIOSIM structures.

4.3 Analyses of the junction interfaces

A change of electrical characteristics in the MIOSIM structure after etching the top SiO_2 layer and the IGZO film was explored to check whether or not any deformation or damage of the layers during manufacturing processes affects the directional electrical conductions. The top SiO_2 film and the IGZO layer were masked through a conventional photolithography method and etched by a dry plasma etching technique and a wet etching process, respectively (Figure 4.2a). After removing the top SiO_2 layer, the initial bi-directional electrical current of the MIOSIM device is changed to uni-directional current, which is consistent with the electrical characteristic of the MIOS device. Following etching process of the IGZO film leads a clear absence of electrical current since the processed structure is same to conventional metal / insulator / metal (MIM) device (Figure 4.2b). These results are manifest proof that the inherent properties of the SiO_2 layers in the MIOSIM device are not damaged during the fabricating processes. In addition, to confirm the distinct boundaries at interfaces in the MIOSIM device, a cross-sectional transmission electron microscope (TEM) analysis was conducted. Any critical atomic diffusion or inter-mixing layers were not observed at every boundary in the device (Figure 4.2c), especially, the IGZO layer was well-grown and sandwiched between top and bottom SiO_2 (Inset of Figure 4.2c). Moreover, a high resolution energy dispersive spectroscopy (HR-EDS) elemental line profile proves that the distributions of In, Ga, and Zn atoms are limited at the localized area between top and bottom SiO_2 (Figure 4.2d).

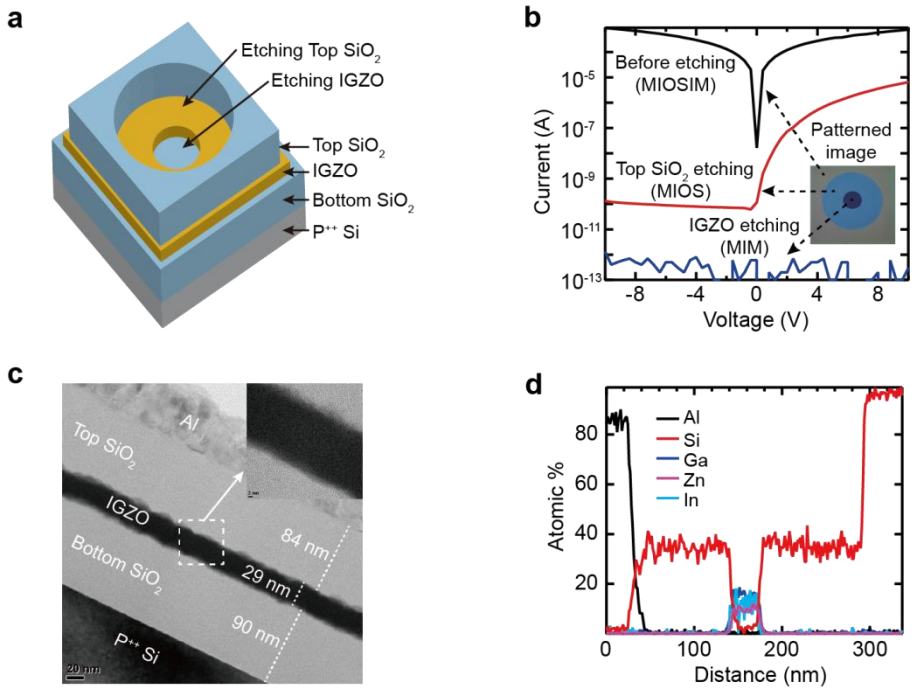

Figure 4.2. Analyses of film qualities of the MIOSIM structure. (**a**) Schematic image of patterned MIOSIM device via etching techniques. (**b**) Verification of the IGZO and the SiO_2 film properties in the MIOSIM device through comparing the current-voltage curves measured: before etching process, after etching top SiO_2, and after subsequently etching IGZO. (c) Cross-sectional transmission electron microscope (TEM) image of the MIOSIM device and the inset image indicate the cross-sectional TEM image of the squared area in SiO_2 / IGZO / SiO_2. (d) A high resolution energy-dispersive x-ray spectroscopy (HR-EDS) elemental line profile.

4.4 Repetitively changed directions of vertical current in multiple junctions

The electrical properties of the integrated structures with alternately deposited SiO_2 layers and IGZO layers were also investigated. The fabricated multilayer structure is composed of four SiO_2 layers with 100 nm thickness and three IGZO layers with 30 nm thickness (Figure 4.3a). The SiO_2 layers were deposited by PECVD technique and the IGZO films were alternately sputtered onto SiO_2 films to design three layers of IGZO layers sandwiched between SiO_2 layers. Circle-shaped Al electrodes were constructed on each layer. As expected, first, there is no noticeable electrical conduction in bottom metal (P^{++} Si) / insulator (1^{st} SiO_2) / metal (Al) structure, which means the 1^{st} SiO_2 retains an intrinsic good insulating quality. Next, the hetero-junction formed at the 1^{st} SiO_2 / 1^{st} IGZO interface results in uni-directional current-flowing from bottom electrode to the Al on the 1^{st} IGZO when positive voltages are applied to the bottom electrode. And then the sequentially constructed junction at the 1^{st} IGZO / 2^{nd} SiO_2 boundary causes bi-directional symmetric current-flowing between bottom electrode and the Al electrode on the 2^{nd} SiO_2. Interestingly, after fabricating the 2^{nd} IGZO on the 2^{nd} SiO_2, the uni-directional current between bottom electrode and the Al on the 2^{nd} IGZO becomes again to the same level of the current density for the preceding bottom electrode / 1^{st} SiO_2 / 1^{st} IGZO / Al electrode MIOSM device. On the other hand, the deposited 3^{rd} SiO_2 on the 2^{nd} IGZO makes the current flow bi-directionally again across the entire device. These directional *J-V* tendencies are reproduced for the structures depositing the 3^{rd} IGZO and the subsequent 4^{th} SiO_2 (Figure 4.3b). These results indicate that the directional characteristics of electrical current in the MIOSIM

devices depend on the sequence of SiO_2 / IGZO junctions in the integrated structures.

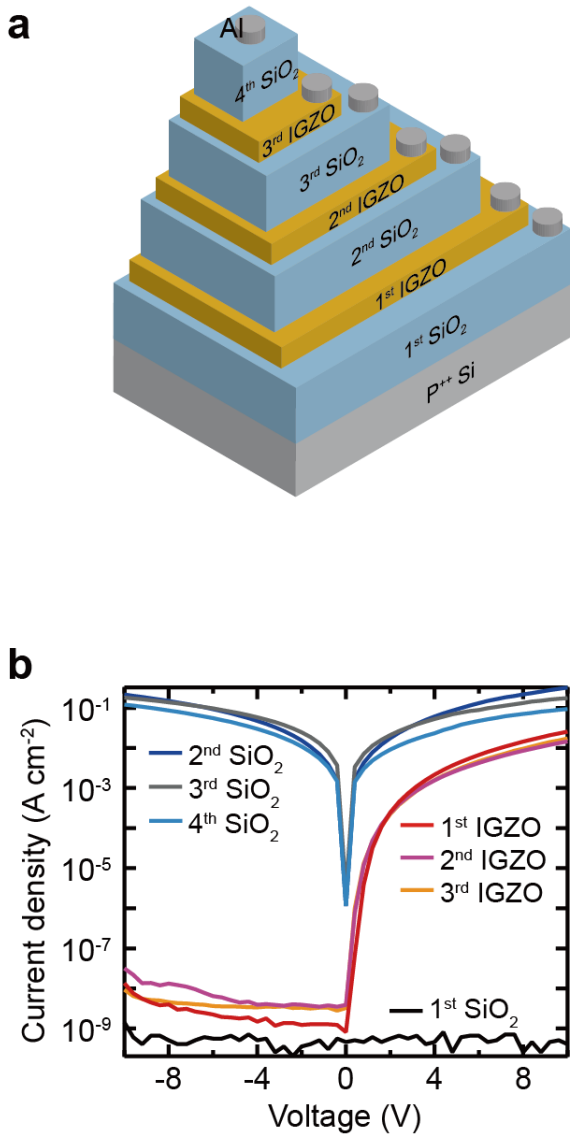

Figure 4.3. Examining the directional nature depending on the sequence of oxide junctions in alternately designed MIOSIM structures. (a) Schematic structure of alternately deposited SiO_2 layers and IGZO layers in the MIOSIM structure. (b) The *J-V* characteristics of alternately deposited SiO_2 and IGZO layers demonstrate that electrical currents of the MIOSM junction structures flow in only one direction and those of the MIOSIM junction structures flow in both directions regardless of the stacked numbers of SiO_2 layers and IGZOs.

4.5 Discussion

Herein, it was revealed that the oxide semiconductor thin-films can launch directly large amounts of electrons into top- and bottom-contacted insulator layers and the hetero-junctions of insulators with contacted oxide semiconductors make the bi-directional electrical current. The uni-directional and bi-directional properties of vertical current are controlled by the sequence of the semiconductor and insulator junctions. These findings offer completely different perspectives to traditional idea about insulators and oxide multilayer structures. The insulator thin-films are not only well-known electrical blocking components but also electrical transporting layers in oxide multilayer structures.

4.6 Experimental details

4.6.1 Experimental design

The research objective is to check that the oxide semiconductor films can inject electrons into the top-contacted insulator layers like into the bottom-contact insulator. The criteria of uni-directional vertical operation were that the vertical current increases as positive voltage increases and the off state should be equivalent to the intrinsic insulating level of the insulator. The criterion of bi-directional vertical operation was that nearly symmetric vertical currents flow at the range of voltages.

4.6.2 Preparation of substrate for all devices

All devices were fabricated on highly boron-doped p-type Si (P^{++} Si) wafer substrates, which were sequentially cleaned with detergent, de-ionized water, acetone, and isopropyl alcohol.

4.6.3 Depositions of semiconductor, insulator, and metal electrodes

30 nm thick IGZO was sputtered by RF magnetron sputtering system using indium gallium zinc oxide (In:Ga:Zn:O = 1:1:1:4 at%) target under 10^{-6} Torr in room temperature. After deposition process, IGZO film was annealed at 350 ℃ for 90 seconds in through a rapid thermal annealing method. All of the SiO_2 layers were grown by plasma enhanced chemical vapor deposition (PECVD) with SiH_4 and N_2O gas. Al electrodes were fabricated via vacuum thermal evaporation at 10^{-6} Torr. The all of films including IGZO, SiO_2, and metals of the devices were patterned by

metal shadow masks in order to avoid unexpected side-contacts with each other.

4.6.4 Etching of MIOSIM device

The top SiO_2 layer was etched by dry plasma etching method with CF_4 and O_2 gas. The IGZO layer was removed by wet etching process with the liquid crystal display etchant-12 (LCE-12).

4.6.5 Characterization of the fabricated devices

The current density-voltage characteristics for all devices were measured using the Agilent 4155B semiconductor parameter analyzer in the dark.

4.7 Reference

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Vertical transport control of electrical charge carriers in insulator/oxide semiconductor hetero-structure. *Scientific Reports* **8**, 5643 (2018).

Chapter 5. Conclusion

I have investigated the non-conventional vertical current in a MIM and a MIOS device. Typical dielectric materials have been used as barrier layers for charge carriers in most electronic devices due to their large band gap and low electron affinity. However, the insulating film is also used as a layer capable of transporting electrical charge carriers in devices such as a tunneling diode or a resistive memory. So far, limited conditions have been required for electrical charge carriers to pass through the insulating film: the very thin thickness of the insulating film that a quantum tunneling effect can occur; the presence of an Ohmic conductive path in the insulating film through which charge carriers can move. In addition, the currents flowing in these devices have the disadvantage that the direction and magnitude of the current are difficult to control. On the other hand, the vertical currents in a MIM and a MIOS device explored in this study follow different conduction mechanism with conventional charge transporting dielectric films. The vertical current is varied by the defect density in the dielectric layer or the area of the contacted electrode, and the energy barrier height at any junction in the device has little effect on the vertical current. Further, the vertical current is proportional to the square of the applied voltage. Therefore, it can be reasonably judged that the unconventional vertical current in our devices depends on a charge-limited conduction (SCLC) mechanism. The vertical current is caused by electrons injected from the contacted electrode; thus, the current flows bi-directionally in the MIM devices. However, the vertical current flows only in one direction when the top electrode is an oxide semiconductor layer because the charge state at the interface

between an insulator and an oxide semiconductor is varied as accumulation or depletion state by the applied electric field. Depending on the conduction mechanism of the vertical current, the magnitude and the direction of the vertical current are precisely controlled by electrical properties of the oxide semiconductor electrode. The vertical current behavior is similar to the conventional diode device. Thus, applicability as a thin-film diode device like a current rectifier or an ESD discharging diode has also been confirmed. Our new approach to the current flow through insulator films is a simple and universal technique that can be easily used in various electronic devices and is also a prominent solution for such applications as a rectifier, switching device, amplifier, and thin-film diode in oxide electronics. In conclusion, the advantages and disadvantages of my research results and future research directions can be summarized as follows.

■ Advantages

-. Simple structure of the device: vertical junction of insulator and semiconductor thin-films.

-. Common commercial insulator and oxide semiconductor materials: SiO_2, Al_2O_3, HfO_2; IGZO, ZnO, ZTO.

-. Stable reliability of operation: amorphouse phase of the insulator films enhances reliability of the operation for the device.

-. Realizing thin-film diode without P-N junction.

-. Wide process window of insulator thickness for conduction: conduction also occurs in insulator films with a thickness of 200 nm or more.

-. Simple engineering for controlling magnitude and direction of vertical current

through controlling electrical properties of semiconductor layer.

■ Disadvantages

-. Need large junction area for stable conduction: more than 3 mm^2 for 100 nm thick SiO_2 layer.

-. Not fast enough operation depending on the conduction mechanism compared to other thin-film diodes including MIM or Schottky diodes.

■ Future research direction

-. Identification clear energy levels for the trap sites in insulator layers by appropriate analytical methods.

-. Requires reduction in junction size for high-density integrated circuit implementation through control of trap density in the insulator and thickness control of the insulator.

-. Need to verify the possibility of thin-film diodes by comparing with existing diode devices.

요 약 (국문초록)

금속-절연체-산화물반도체 적층 구조에서 발생하는 단방향 수직 전류에 대한 연구

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전기적 전류가 절연체 박막을 통해 흐를 수 있게 하는 기술은 다이오드나 저항성 스위칭 소자와 같은 차세대 소자들에서 새롭게 주목 받고 있다. 하지만, 이러한 소자들에서 전류 흐름은 전극 제한 전도 이론 (electrode-limited conduction mechanisms)을 따르기 때문에 절연체의 두께가 매우 얇아야 한다는 공정 제약 사항이 있고 전류의 크기나 방향을 조절하기 어렵다는 단점이 있다. 이 논문에서는 상대적으로 두꺼운 절연체 막을 통해서 전기 전하들이 안정적으로 흐를 수 있는 새로운 접근 기술을 소개한다. 이는 절연막 내에 존재하는 결함 위치들 (trap sites)과 중첩되는 전극의 면적을 조절하거나, 다양한 증착법을 통해 절연막 내의 결함 농도를 조절하는 전략으로 달성하였다. 그리고 금속 / 절연막 / 금속 구조에서 상부 전극을 산화물 반도체 물질로 변경하여 전류의 크기와 극성을 정교하게 제어하였다. 또한 이 때 흐르는 전류는 외부 전극으로부

터 주입되는 전하에 의존하는 공간 전하 제한 전도 이론 (space charge-limited conduction mechanism)을 따른다는 것을 입증하였다. 따라서, 수직 전류의 크기나 외부 신호를 정류하는 정류비는 산화물 반도체 전극의 전기적 특성에 따라 정교하게 제어할 수 있다는 점이 증명되었다. 이러한 수직 전류를 나타내는 소자는 기존의 다이오드처럼 동작함이 확인되었고, 다양한 전자 회로에서 다이오드가 하는 역할을 대체할 수 있는 가능성을 확인하였다. 금속 / 절연막 / 산화물 반도체 구조에서 발견한 이 특이한 수직 전류 현상은 재료과학이나 전자공학 분야에 활용될 수 있는 다양한 잠재력을 지니고 있다고 기대된다.

주요어 : 산화물 박막 다이오드, 산화물 전자공학, 산화물 박막 트랜지스터, 산화물 반도체, 박막 다이오드
학 번 : 2014-30807