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M.S. THESIS

A Broadband High-Power Amplifier
Design for Remote-Controlled
IED Jammer Applications

무선 제어 IED Jammer 적용을 위한 광대역
고출력 전력 증폭기 설계

BY

JOONHO JUNG

AUGUST 2018

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

Abstract

Nowadays, the demand for broadband high-power power amplifier (PA) is on the rise due to electronic warfare (EW) applications such as remote-controlled improvised electronic device (IED) jammer and active electronically scanned array (AESA) radar.

In this thesis, hybrid-type multi-octave high-power PAs using Gallium nitride (GaN) –high electron mobility transistor (HEMT) are designed for IED jammer application. In order to realize both high-power and broadband characteristics, 2 broadband PAs with lower power level are combined in parallel to compensate for power degradation due to bandwidth enhancement.

In the first phase of the design process, 1-way broadband PA was designed using harmonic resistive loading for bandwidth enhancement. The fabricated 1-way module exhibited more than 45 dBm saturated output power across 2.5 to 6.5 GHz bandwidth, verifying that the employed topology is suitable for S/C-band high-power applications for IED jammer.

In the final stage of the design process, 2-way broadband high-power PA was designed by combining 2 1-way PAs designed from the previous stage. Instead of employing conventional Wilkinson combiner for power combining, multi-section Wilkinson combiners including matching networks within are employed for the reduction in the overall size and bandwidth enhancement. In addition, it has been confirmed that inevitable removal of some shunt resistors inside Wilkinson combiners due to limitation in line bending does not lead to serious degradation in isolation characteristics, making it possible to remove some resistors. The fabricated 2-way module exhibited more than 42 dBm saturated output power across 2.0 to 7.0 GHz bandwidth, showing great improvement in bandwidth over conventional PA combining

method using 1-section Wilkinson combiner.

Keywords: GaN, Multi-octave, High-power power amplifier, Hybrid implementation, Multi-section Wilkinson combiner

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Chapter 1 Introduction

1.1 Broadband High-Power Power Amplifier (PA)

Broadband high-power power amplifier (PA) is a critical component inside electronic warfare (EW) applications such as radar system and jamming device. Active electronically scanned array (AESA) radar and improvised explosive devices (IED) jammer are typical examples of these applications (Fig. 1.1). Moreover, the demand for broadband high-power PA is increasing as the modern wireless communication systems require the use of multiband/broadband radio frequency (RF) transceivers to support emerging communication standards such as 5G and IoT.



Figure. 1.1 Photograph of (a) AESA radar and (b) IED jammer

MMIC is a common way to implement broadband high-power PA for these applications, especially for military use. However, the required expenditure and long lead time of a MMIC run cannot be easily justified for prototyping or low volume sales. On the other hand, the hybrid

implementation has many advantages over MMIC approach such as a faster design cycle, reduced production time, easier tuning capability, lower cost, and easier implementation. In this thesis, a hybrid approach was used to implement a broadband high-power PA suitable for these applications.

1.2 Broadband High-Power PA Topology

Gallium Nitride (GaN) device is the most prominent technology available nowadays for the design of reliable high-performance PA due to its excellent properties.

Although other compound semiconductors, such as GaAs, are widely used for military applications, they are not sufficient to fulfill the high-power requirement of a jamming system. On the other hand, GaN device is suitable for this application due to its high power density and high voltage operation.

TABLE 1.1 Performance Comparison of Si, GaAs, and GaN Device

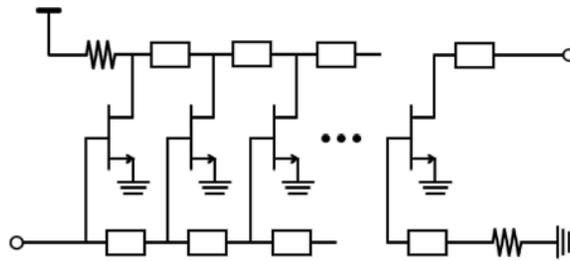
Property	Si	GaAs	GaN
Energy Gap (eV)	1.11	1.43	3.4
Critical Electric Field (MV/cm)	0.3	0.5	3.5
Charge Density ($\times 10^{13}$ /cm ²)	0.3	0.3	1
Mobility (Cm ² /V/s)	1350	8000	1500
Saturation velocity ($\times 10^7$ cm/V)	1	1.4	2.7

Table 1.1 compares the performance of GaN devices with Si and GaAs. GaN devices have high breakdown voltage due to its high energy gap and critical electric field properties. Therefore, high voltage operation over 28 V is possible. In addition, due to high breakdown voltage, GaN device has large load impedance, which is a great merit for broadband implementation. Although there are problems such as thermal and trap effects, other superb properties such as mobility and saturation velocity compensate for these disadvantages. Therefore, in this thesis, all PAs are fabricated using GaN-HEMT device for high-power, broadband performance.

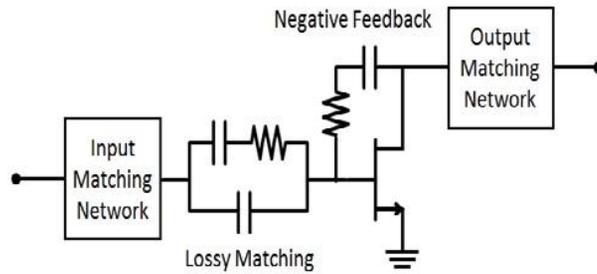
Technology aside, decisions on PA architecture will affect the overall bandwidth and power performance of the designed PA. Distributed amplifier (DA) is a commonly used topology for high-power PA with multi-octave bandwidth (Fig. 1.2 (a)). The input and output capacitances are absorbed into the artificial transmission line to implement broadband performance [1]. However, DAs suffer from small gain and requires large number of transistor devices, which leads to larger size and more expenses when implementing a hybrid-type module.

Reactively matched power amplifiers (RMPA) are also widely used as multi-octave PAs (Fig. 1.2 (b)). However, it has the bandwidth problem coming from Bode-Fano criterion [2,3]. To achieve broadband characteristics, lossy matching and negative feedback method are used to lower the Q-factor. This results in low power and efficiency, introducing power-bandwidth limitation.

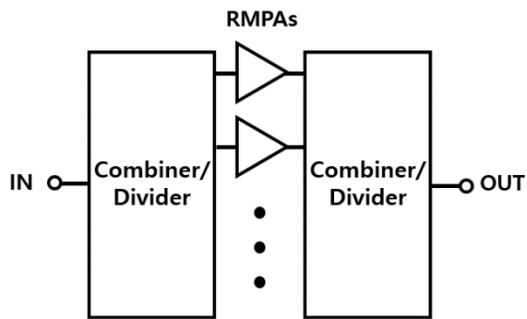
In order to implement both high-power and broadband characteristics within limited physical size and expenditure, combining more than one broadband RMPA in parallel can compensate for power degradation due to increased bandwidth (Fig. 1.1 (c)).



(a)



(b)



(c)

Figure. 1.2. Multi-octave PA structures of (a) DA, (b) RMPA, and (c) Parallel-combined RMPA

1.3 Power Combining Method

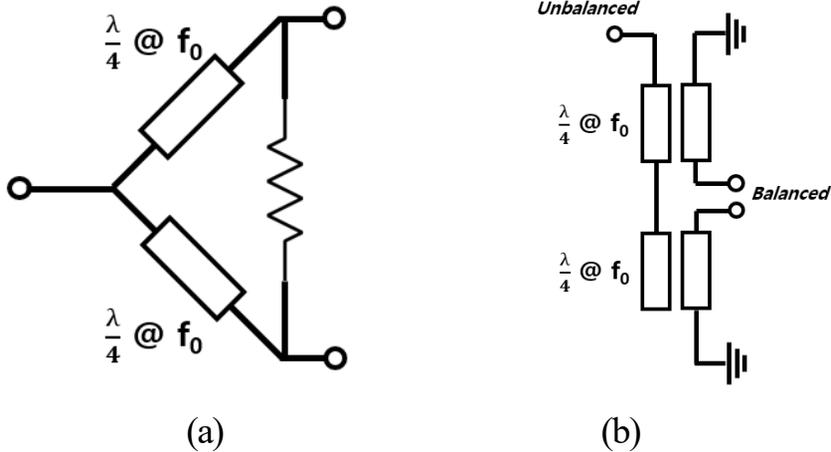


Figure. 1.3. Power combining method of (a) Wilkinson combiner, and (b) Marchand balun

Aside from determination of the 1-way PA topology, use of power combiners to increase power level is necessary to implement a broadband high-power PA. For this purpose, power combiners such as Wilkinson combiner, and Marchand balun can be utilized (Fig. 1.3.).

After each RMPA is matched to 50 ohms at both input and output, Wilkinson combiner can be used to combine multiple RMPAs to enhance power level. Therefore, the overall PA architecture exhibits the similar input/output reflection coefficient within the targeted bandwidth as each RMPA. However, the use of Wilkinson combiner introduces increased module size and additional insertion loss due to its presence.

Marchand balun is a type of balun which can be implemented with distributed elements, and therefore, suitable for push-pull PA topology. In addition to combining 2 1-way PAs, push-pull

PA topology using balun offers enhanced efficiency by separating the terminations of the fundamental frequencies from the second harmonic frequencies. However, the attempt to improve the bandwidth and balance of the balun by enhancing coupling coefficient increases complexity of the balun combiner, which means difficult implementation and more fabrication cost.

Previous works using these types of combiners for power combining have proven to be suitable for the implementation of broadband high-power PA [4, 5]

1.4 Motivation

As previously mentioned, in order to implement broadband high-power PA in hybrid type, both broadband PA topology and power combining method must be considered. In addition, other factors such as bond wire inductance, accuracy in models of capacitors, resistors, and GaN-HEMT devices must be also taken into account for the reliable implementation.

There have been many works to overcome the power-bandwidth limitation in hybrid-type PA, addressing the issue of enhancing both power and bandwidth characteristics through various topologies. This thesis is in line with the previous works to overcome these issues.

Based on previous works, a hybrid-type broadband high-power PA is designed using one GaN-HEMT bare die to verify performance improvement of the proposed topology over previous works. In addition, based on this 1-way design, a hybrid-type PA with greater output power is demonstrated by combining 2 1-way PAs.

Table 1.2 lists the performance specification of broadband high-power PA for IED jammer application. The PAs in this thesis are designed to satisfy this target.

TABLE 1.2 Target Specification of Broadband High-power PA for IED Jammer Application

	Target
Frequency (GHz)	2.5 ~ 6.5 (S/C-band)
Output power (dBm)	> 47
Drain Efficiency (%)	> 20

1.5 Chapter Overview

This thesis is organized as follows: In chapter II, the design of a hybrid-type, S/C-band, high-power PA using one GaN-HEMT bare die is presented. By maintaining resistive loading condition at higher harmonics, a high-power PA with power bandwidth greater than 100 % was implemented at the cost of efficiency degradation. From power measurement, the design topology proved to be suitable for IED jammer applications due to its broadband, high-power characteristics. Chapter III presents the design of 2-way combined, broadband, high-power PA, where matching networks of each PA is designed based on topology used in Chapter II. By combining power combiners and matching networks from each 1-way PA, not only were powers from each PA well-combined, but also bandwidth improvement over conventional topology using Wilkinson combiner is observed. Chapter IV concludes the thesis with future works to be done.

Chapter 2 Design of a 1-way S/C-band High-power PA

2.1 Design Considerations

2.1.1 Overall PA Structure

In order to meet the target specifications listed in table 1.2, the selection of proper transistors for the design of broadband high-power PA must be preceded. GaN-HEMT bare dies offered by Wolfspeed Inc., were used for hybrid implementation in this thesis [6]. Since the designed PA must cover broad frequency range and possess high-power capacity, 2 high-power GaN-HEMT transistors with relatively large load impedances are considered for the design: CGHV60170 (170 W Peak output power) and CGHV1J070 (70 W Peak output power). Considering output power degradation due to bandwidth enhancement, 1 CGHV60170 bare die alone can be used to design the PA, while 2 CGHV1J070 bare dies are required for the implementation.

Figure 2.1 shows the load-pull contours of 2 GaN-HEMT transistors at 4.5 GHz, which is the center frequency of the target band. The load-pull simulation was done at Class-A bias condition when the source impedance was conjugate-matched at 4.5 GHz. The input power was set to 40 dBm and 37 dBm for 170 W and 70 W transistor respectively, due to the required system specification for IED jammer application.

From load-pull contours, the maximum output power delivered by one 170W device is twice that delivered by one 70W device (3 dB difference in the P_{max}). On the other hand, the load impedance of 70 W device is larger than that of 170 W device, which means larger bandwidth

can be achieved with one 70 W device at half the power level of one 170 W device. From this observation, it can be expected that the ideal combination of 2 broadband PAs designed with 70 W devices can exhibit larger bandwidth than 1 PA designed with 170 W device at the similar output power level.

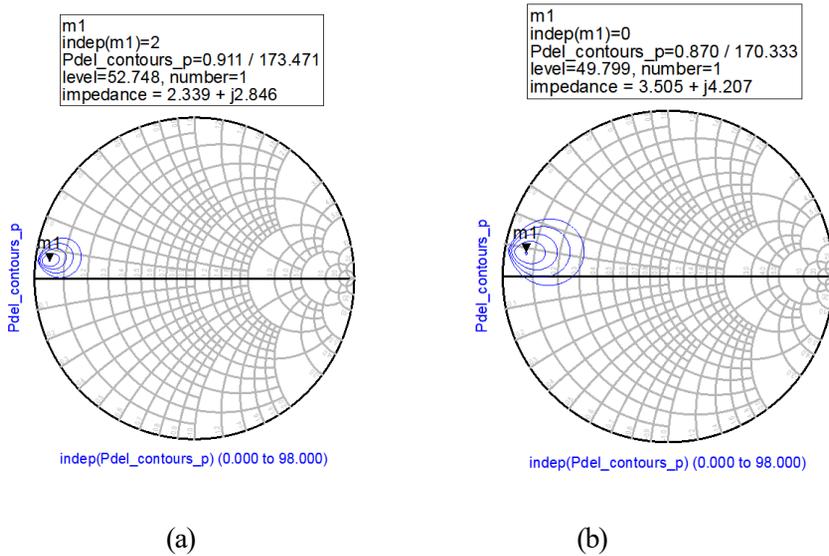


Figure. 2.1 Load-pull contours of (a) CGHV60170 and (b) CGHV1J070.

Therefore, in this thesis, two CGHV1J070 devices (70 W device) are used to design the broadband high-power PA in parallel-combined structure for IED jammer application. The overall PA structure is shown in Figure 2.2.

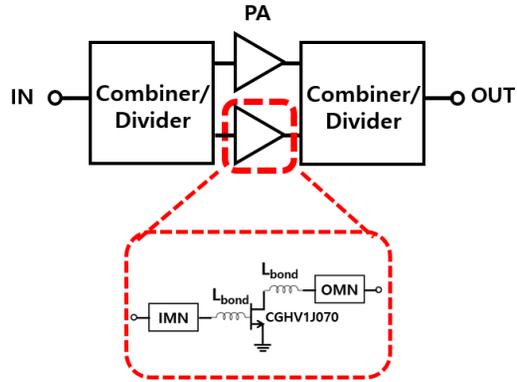


Figure. 2.2 Overall PA structure

Before moving on to the design phase of parallel-combined structure in chapter III, this chapter presents the design of a 1-way broadband PA using only one 70 W device for the investigation of the broadband topology and its verification by implementing a hybrid-type module.

Table 2.1 shows the target specification of a 1-way broadband PA, which was determined based on the performance specification listed in Table 1.2.

TABLE 2.1 Target Specification of a 1-way Broadband PA

	Target
Frequency (GHz)	2.5 ~ 6.5 (S/C-band)
Output power (dBm)	> 45
Drain Efficiency (%)	> 20

2.1.2 Broadband PA Topology

In order to implement multi-octave PA, tradeoff between PA bandwidth, power, and efficiency must be considered. Enabling high-efficiency operation over broad bandwidth is difficult due to difficulties in maintaining appropriate harmonic loading conditions over multi-octave bandwidth. For example, in broadband Class-B design, the highest fundamental frequency will overlap the lowest second harmonic frequency, making it difficult to maintain high-efficiency operation over more than one octave of bandwidth. Moreover, delivering the maximum output power is the bigger priority than any other target specs in implementing a broadband high-power PA for IED jammer applications. For this reason, Class-A bias is chosen for the design of broadband high-power PA at the cost of efficiency degradation. The output power and DC-power consumption at the maximum voltage swing under class-A bias can be expressed by the Equations 2.1. From these equations, the maximum achievable efficiency of 50 % at class-A bias can be derived as shown in Equation 2.2.

$$P_{out} = \frac{V_{DD}^2}{2R_L}, P_{DC} = V_{DD} \times I_D = \frac{V_{DD}^2}{R_L} \quad (2.1)$$

$$\text{Efficiency} = 100 (\%) \times \frac{P_{out}}{P_{DC}} = 50 \% \quad (2.2)$$

In this chapter, the broadband high-power PA is designed based on resistive loading at the higher harmonics, equal to that at the fundamental. The efficiency of this type of implementation is lower than that of other high-efficiency designs. However, by not maintaining special load conditions at higher harmonics, bandwidth limiting harmonic overlap issues can be avoided, leading to broadband characteristics [7].

In the adopted broadband resistively loaded topology, the goal of the output matching network is to present a resistive load by a conjugate-matched load admittance (Y_L) over a designed bandwidth, i.e.

$$Y_L(\omega) = \frac{1}{R_L} - j\omega C_{out}, \quad (2.3)$$

where R_L is the load resistance, and C_{out} is the transistor output capacitance.

2.2 Design of broadband high-power PA with resistively loaded topology

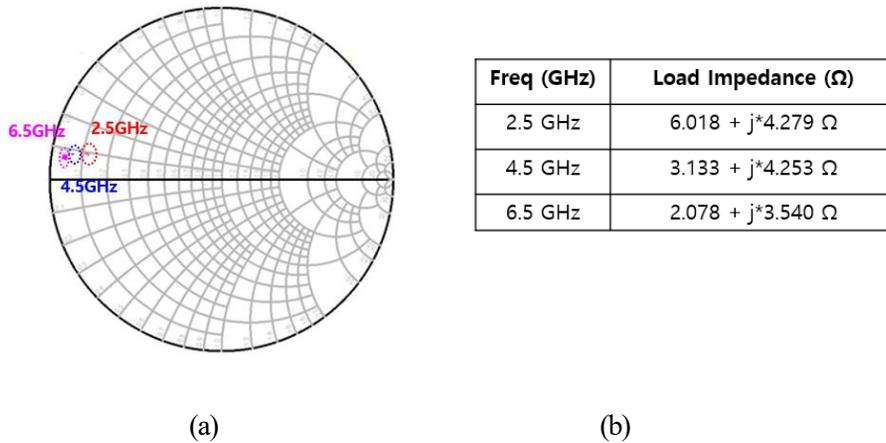


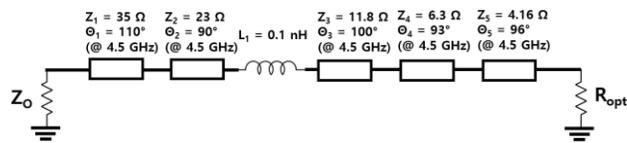
Figure. 2.3. Z_{opt} for P_{max} at 2.5, 4.5, 6.5 GHz

As shown in Figure 2.3, load-pull simulations across the targeted band were done to obtain the optimum impedance (Z_{opt}) for the maximum output power (P_{max}). From these simulations and the datasheet offered by the manufacturer, the optimum load resistance (R_{opt}) and the output capacitance (C_{out}) that yield the maximum output power in the targeted band are estimated to be $2.5 \sim 4.5 \Omega$ and 4.2 pF respectively.

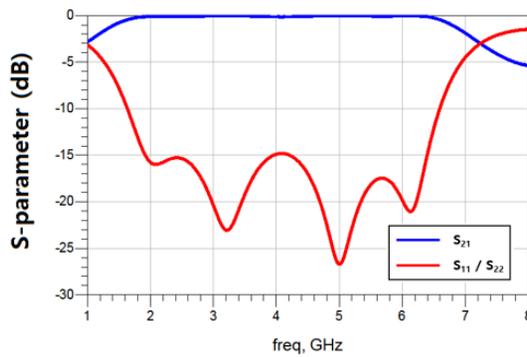
The design goal for output matching network (OMN) is to realize a broadband load network capable of resonating C_{out} .

The first step in this OMN design procedure is to synthesize a broadband 50Ω -to- R_{opt} Chebyshev transformer to act as a broadband R_{opt} -load. Figure 2.4 shows the required length and impedance of each line in the designed 5-section Chebyshev transformer, and the insertion

loss(S_{21}) and return loss (S_{11}/S_{22}) of it from ADS simulation. Bonding inductance (L_1) is introduced in the transformer due to a fabrication reason as will be explained later in the next section. Insertion loss and return loss are maintained greater than -1 dB and less than -15 dB within 2.5 ~ 6.5 GHz band respectively, acting as a broadband R_{opt} -load.



(a)



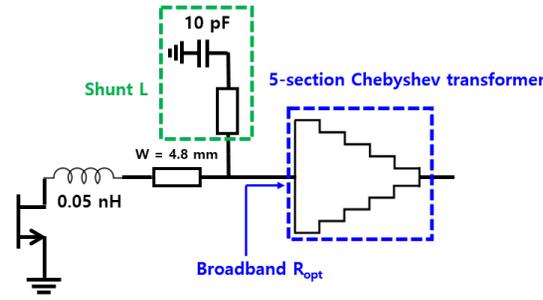
(b)

Figure. 2.4 (a) The designed Chebyshev transformer and (b) its insertion / return loss

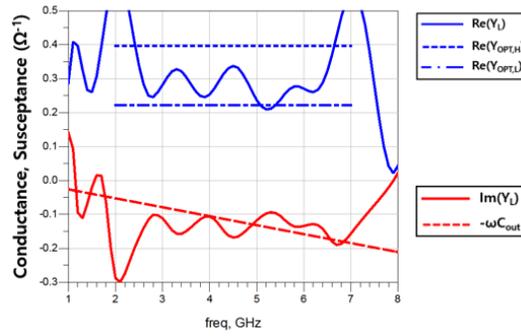
Given this wideband load, the rest of the network was designed to induce the negative susceptance needed for cancelling out C_{out} . A shunt stub connected to 10 pF capacitor is introduced for this purpose.

Figure 2.5 shows a simplified schematic of the load network and the load network results obtained from ADS simulation. The ripple of the real component of the load impedance is

maintained within $0.22 (\text{Re}(Y_{\text{opt,L}})) \sim 0.4 (\text{Re}(Y_{\text{opt,H}})) \Omega^{-1}$ across the bandwidth, and the imaginary component of the load network follows that of an ideal 4.2 pF capacitor.



(a)



(b)

Figure. 2.5 (a) Schematic of the proposed load network and (b) load network results

The input network was designed based on source-pull simulations done with the designed load network connected. Based on the P_{max} results, a broadband source resistance of 1.8Ω was chosen, and realized using a broadband, 4-section, 50-to- 1.8Ω Chebyshev transformer. In addition, a parallel combination of a 5Ω resistor and a 4.3 pF capacitor was connected in series with the matching network for stability enhancement. Figure 2.6 shows a simplified schematic of the input matching network, and the broadband constant source resistance of 1.8Ω realized

by the source network.

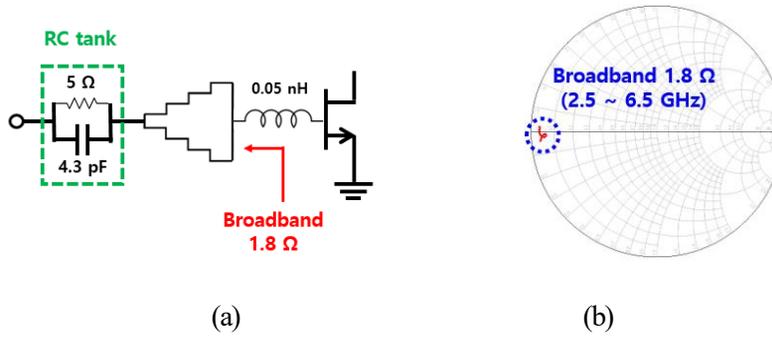


Figure. 2.6 (a) Schematic of the source network and (b) a source network result

2.3 Measurement results

2.3.1 Fabrication Details

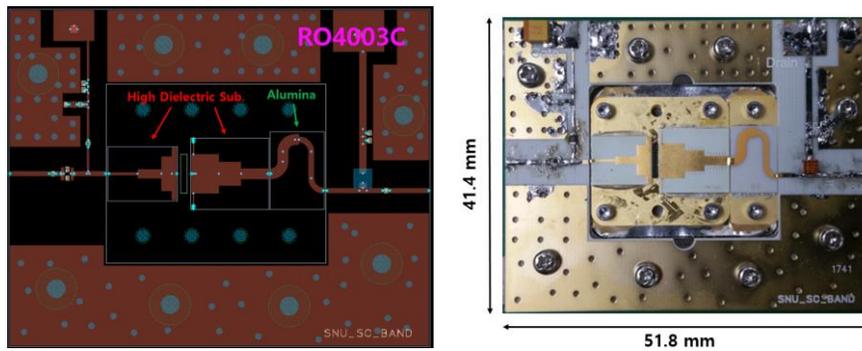


Figure 2.7 (a) Layout of the designed PA and (b) photograph of the module

The layout and photograph of the 1-way hybrid-type S/C-band PA is shown in Figure 2.7. Table 2.2 lists the substrate information on 3 different types of substrates used for the implementation. The high dielectric substrate with the dielectric constant of 40 was used for the input/output matching network. Due to its high dielectric property, the overall size of the circuit was greatly reduced. Since the last 2 sections of the load network are high-impedance line, which is difficult to be realized in high dielectric substrate due to their narrow widths, some part of output matching network was implemented in Alumina substrate. The rest of the PA is implemented in RO4003C. Ball-bonding was employed to connect the CGHV1J070 transistor and the input/output matching networks, while conductive copper tape was used to connect different substrates, leading to low inductance.

TABLE 2.2 Information of the Substrates for Fabrication

Type	Thickness	Dielectric Constant
High Dielectric	15 mil	40
Alumina	15 mil	9.8
RO4003C	12 mil	3.55

2.3.2 Measurement Details

The fabricated module was measured at the bias of $V_{gs} = -2.57$ V, $V_{ds} = 40$ V, $I_{dq} = 360$ mA, which is the class-A bias, determined for the maximum extraction of output power.

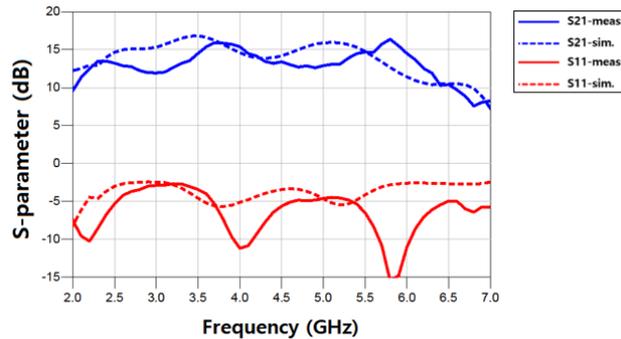


Figure 2.8 Simulated and measured S-parameters

Figure 2.8 shows both simulated and measured S-parameters of the fabricated module, which show good agreement across the bandwidth. Because 20 dB attenuator is connected to the

output of the module for the protection of the measurement devices from potential damage, output return loss (S22) was not measured. The mismatch of the small-signal gain (S21) between simulation and measurement is mainly due to additional substrate loss not predicted in simulation. In addition, the slight deviation of the implemented bond wire inductance from the predicted value caused slight degradation in the high frequency range.

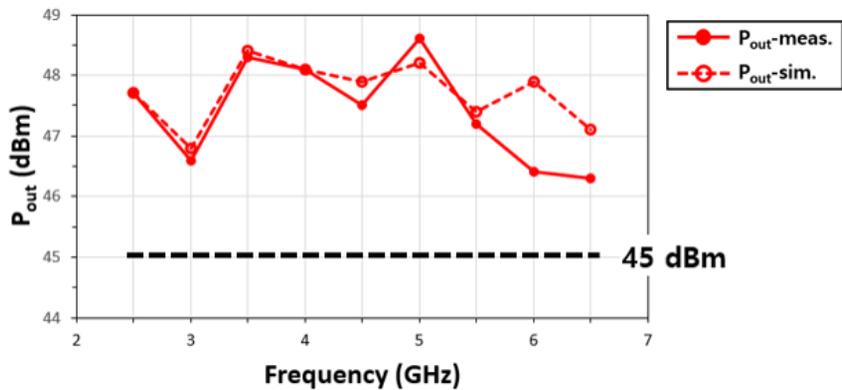


Figure 2.9 Simulated and measured saturated output power (P_{sat})

Figure 2.9 shows the simulated and measured saturated output power (P_{sat}) of the fabricated module. The P_{sat} was measured using a driver amp (CMPA2060025D), which can supply up to 43 dBm input power to the module across the bandwidth (2.5 ~ 6.5 GHz). The measured output power is greater than 45 dBm across the bandwidth, satisfying the target specification. Both the simulated and measured saturated output power show good agreement across the bandwidth except at the high frequency range, which is the tendency also observed in the small-signal gain measurement. This is mainly due to the larger-than-expected bond wire inductance between the CGHV1J070 transistor and the PCBs. Figure 2.10 shows the simulation of P_{sat} when sweeping both input and output bond wire inductances from 0.08 nH (the value used for the design) to

0.12 nH. From this simulation, it can be expected that larger-than-expected bond wire inductance causes power degradation in the high frequency range, and proper tuning of the bond wire inductance can bring improvement in this region.

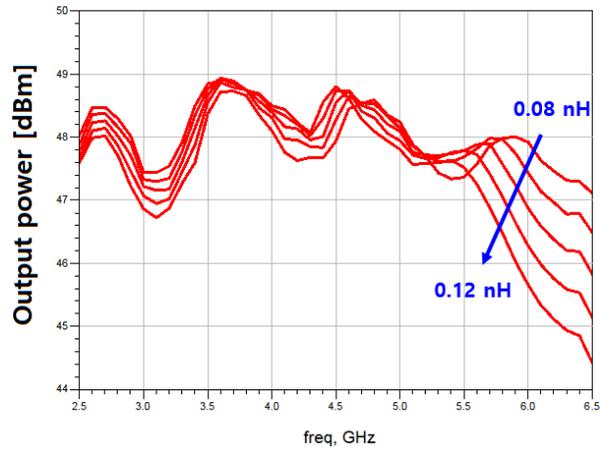


Figure 2.10 The simulated variation of saturated output power (P_{sat}) when sweeping bond wire inductance

2.4 Conclusion

In this chapter, a 1-way hybrid-type S/C-band high-power PA using one CGHV1J070 transistor was designed for IED jammer application. Before moving on the design phase of 2-way PA, a 1-way hybrid-type PA was fabricated for the investigation on the broadband topology and its verification by actual implementation.

The 1-way broadband high-power PA is designed based on resistive loading at the higher harmonics, equal to that at the fundamental. The efficiency of this type of implementation is lower than that of other high-efficiency designs. However, by not maintaining special load conditions at higher harmonics, bandwidth limiting harmonic overlap issues can be avoided, leading to broadband characteristics.

The designed PA satisfied the broadband target specification, exhibiting more than 45 dBm saturated output power across 2.5 ~ 6.5 GHz bandwidth (S/C-band). Therefore, the PA topology using harmonic resistive loading is suitable for high-power broadband implementation in S/C-band.

Chapter 3 Design of a 2-way Hybrid-type S/C-band High-power PA using Multi-section Wilkinson Combiner as a Matching Component

In chapter II, a 1-way S/C-band high-power PA was implemented using the topology of harmonic resistive loading, leading to broadband characteristics of the adopted approach. However, due to power-bandwidth limitation, the saturated output power exhibited by 1-way PA was slightly insufficient to fulfill the high-power capability required by IED jammer application. Therefore, more than one 1-way PA need to be combined in parallel to compensate for the power degradation due to bandwidth enhancement.

This chapter presents the design of 2-way hybrid-type S/C-band high-power PA, where multi-section Wilkinson combiners were used as both power combiners and matching networks. While the previous chapter demonstrated the design of 1-way PA using CGHV1J070 (70W) device, 2-way PA in this chapter is designed using 2 CGHV1J025D (25W) devices to verify the validity of the concept at low cost.

3.1 Design Considerations

3.1.1 Use of Combiners in the Implementation of 2-way PA

One of the most widely used, conventional power combiner is Wilkinson combiner. Depending on the substrate to be used for implementation, Wilkinson combiner can be designed to have low insertion loss, leading to minimized gain degradation due to its presence. However, since it is composed of $2 \cdot 70.7 \Omega$ lines with the electrical length of 90° at the center frequency of its bandwidth, the combiner has inherent bandwidth limitation. Therefore, Wilkinson combiner limits the overall bandwidth of the parallel-combined PA using it.

Although this bandwidth limitation of Wilkinson combiner can be overcome by increasing the number of $\frac{\lambda}{4}$ sections inside it [8] as shown in Figure 3.1, the increase in the size of the overall PA architecture is inevitable.

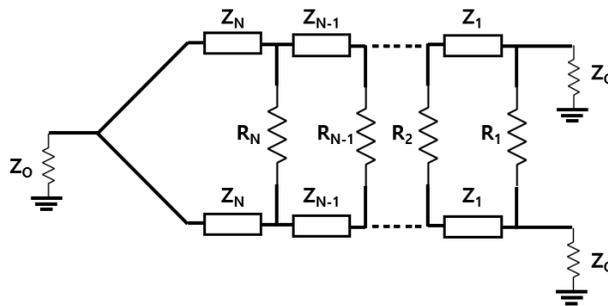


Figure 3.1 Multi-section Wilkinson Combiner with Wider Bandwidth

On the other hand, by using a multi-section Wilkinson combiner as both a power combiner and a matching network, the increase in the size of the overall PA architecture can be minimized.

The validity of this proposed concept is intuitively plausible, because each bi-section of a multi-section Wilkinson combiner at even mode can be seen as a $2Z_0$ -to- Z_0 transformer. By combining 2 matching networks based on harmonic resistively loading, where Chebyshev transformer structure was used, multi-section Wilkinson combiner that includes the matching networks within can be designed. The detailed analysis on this procedure will be provided in the next sub-section.

3.1.2 Theoretical Analysis on the Design of Multi-section Wilkinson Combiner as a Matching Component

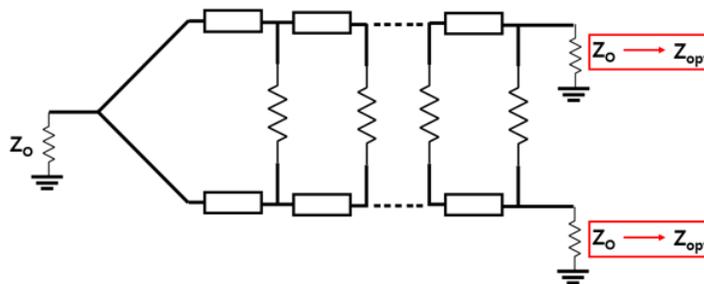


Figure 3.2 Multi-section Wilkinson Combiner as Output Matching Networks

Multi-section Wilkinson combiner used as output matching networks for 2 transistors can be conceptually visualized as shown in Figure 3.2. The proposed concept is exactly the same with the conventional multi-section Wilkinson combiner except for the fact that the load impedances at the balanced ports are replaced with Z_{opt} . The following analysis ignores the reactive component of the load for conciseness; the reactive component can also be taken into account in the actual design process as will be explained in the later chapters.

The first step in this design process is to determine the characteristic impedances of each section of the combiner from the even-mode analysis. The bisected half-circuit of the combiner is shown in Figure 3.3 (a).

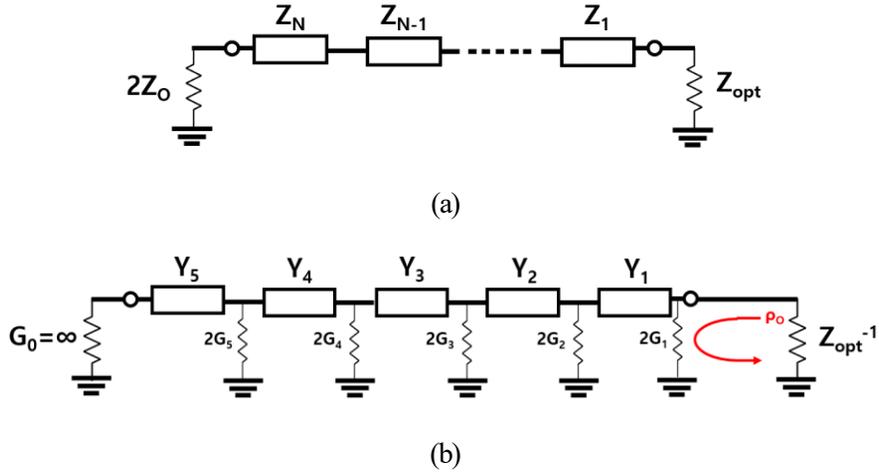


Figure 3.3 Bisection of the proposed combiner in (a) even-mode excitation and (b) odd-mode excitation

By even-mode analysis, the bisection of the proposed combiner reduces to $2Z_0$ -to- Z_{OPT} transformer. Various topologies can be employed for wideband $2Z_0$ -to- Z_{OPT} transformer, among which are binomial transformer (maximally flat) and Chebyshev transformer (equal-ripple). Since Chebyshev transformer can maximize bandwidth at the expense of passband ripple [9], it is used to design the even-mode bisection of the proposed combiner.

The next phase is to determine the values of shunt resistors in the combiner. Figure 3.3 (b) shows the odd-mode bisection in admittance/conductance representation. The conductance of the first section is determined by the admittance of the first section in equation (3.1). Then, the conductance from 2 to N section are determined from iterations based on equations (3.2) and

(3.3). These equations for obtaining approximate values of shunt resistors are derived in [8] to minimize ρ_0 , the reflection coefficient from the balanced port of the odd-mode bisection.

$$G_1 = 1 - Y_1 \quad (3.1)$$

$$G_k = \frac{Y_{k-1} - Y_k}{Y_{k-1} T_1 T_2 \cdots T_{k-1}}, \quad k=2 \text{ to } N-1 \quad (3.2)$$

$$\text{where, } T_k = \frac{4Y_{k-1}Y_k}{(Y_{k-1} + Y_k + 2G_k)^2}, \quad k=1 \text{ to } N$$

$$G_N = \frac{0.5Y_{N-1}^2}{-2G_{N-1} + \frac{Y_{N-2}^2}{-2G_{N-2} + \frac{Y_{N-3}^2}{\ddots \frac{Y_1^2}{-2G_2 + -2G_1 + 1 + 0.7(S-1)}}}} \quad (3.3)$$

$$\text{Where, } S \text{ (VSWR at port 1)} = \begin{cases} 1, & N \text{ odd} \\ S_e, & N \text{ even} \end{cases}$$

3.2 Design of Broadband High-power PA using Multi-section Wilkinson Combiner as a Matching Component

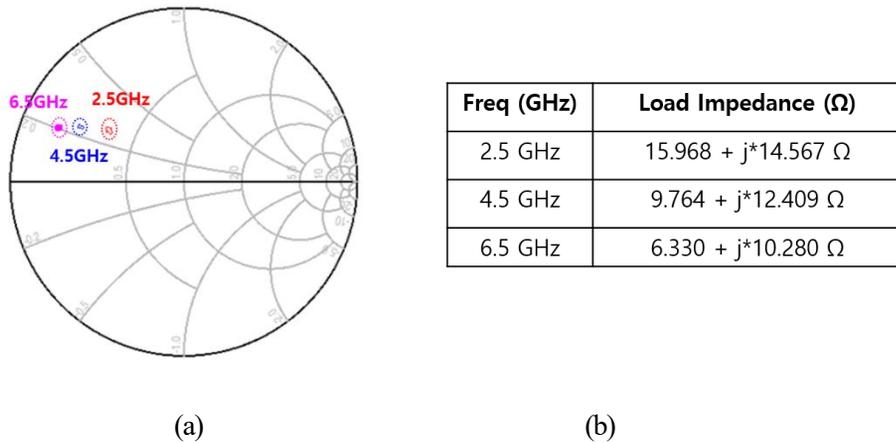


Figure 3.4 Z_{opt} for P_{max} at 2.5, 4.5, 6.5 GHz

As shown in Figure 3.4, load-pull simulations of CGHV1J025D (25W) device across the targeted band were done to obtain the optimum impedance (Z_{opt}) for the maximum output power (P_{max}). From these simulations and the datasheet offered by the manufacturer, the optimum load resistance (R_{opt}) and the output capacitance (C_{out}) that yield the maximum output power in the targeted band are estimated to be $5.0 \sim 17.0 \Omega$ and 1.2 pF respectively. Based on this load-pull data and the design steps explained in sub-section 3.1.2, the characteristic impedances (Z_k) and electrical length (θ_k) of each section, and the resistances (R_k) of each resistor have been determined as shown in Figure 3.5.

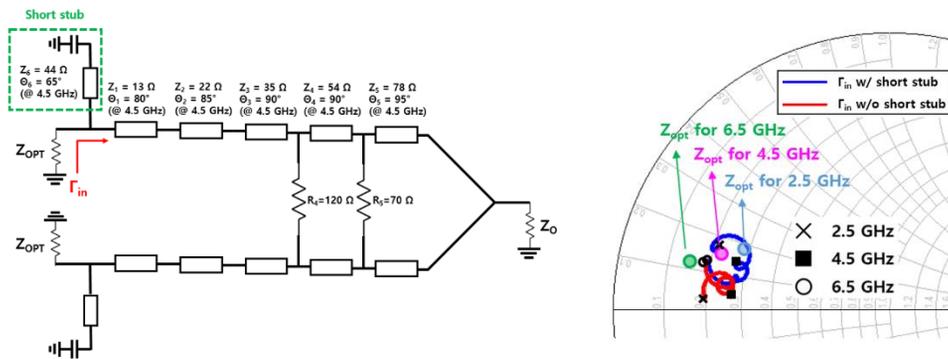


Figure 3.5 Output Matching Network Schematic and Effect of Short Stub on Γ_{in}

Some shunt resistors (R_3 , R_4 and R_5) have been omitted, because line bending for the connection of shunt resistors is impossible for some line sections. As shown in Figure 3.6, it has been confirmed that removal of less than 4 shunt resistors are not detrimental for isolation characteristics, maintaining better than -20 dB isolation within the targeted bandwidth. In addition, a shunt stub connected to 15 pF capacitor is employed to induce the negative susceptance needed for cancelling out C_{out} , enabling broadband load matching within the targeted bandwidth as shown in Figure 3.5.

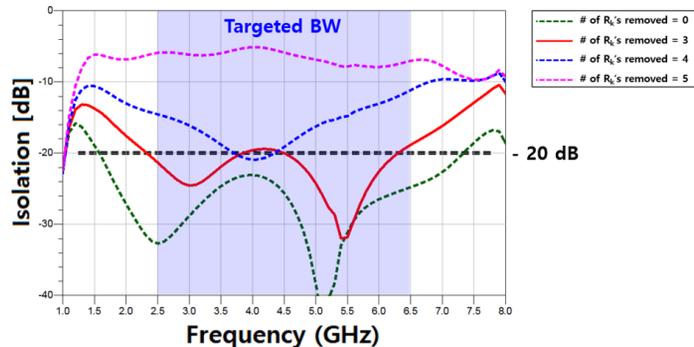


Figure 3.6 Output Matching Network Isolation when Shunt Resistors (R_k) are removed
(Consecutive removal from R_1)

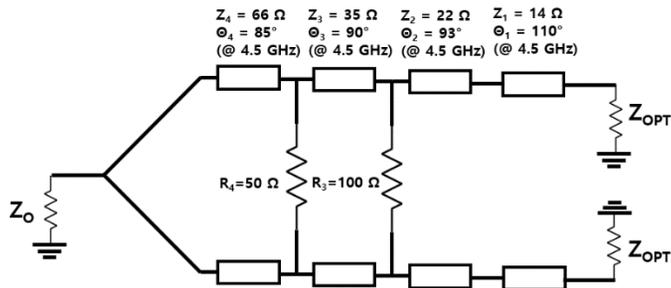


Figure 3.7 Input Matching Network Schematic

The input network was designed based on source-pull simulations done with the designed load network connected. Based on the P_{max} results, a broadband source resistance of 5.5Ω was chosen, and realized in the multi-section Wilkinson combiner. Figure 3.7 shows a simplified schematic of the input matching network.

3.3 Measurement results

3.3.1 Fabrication Details

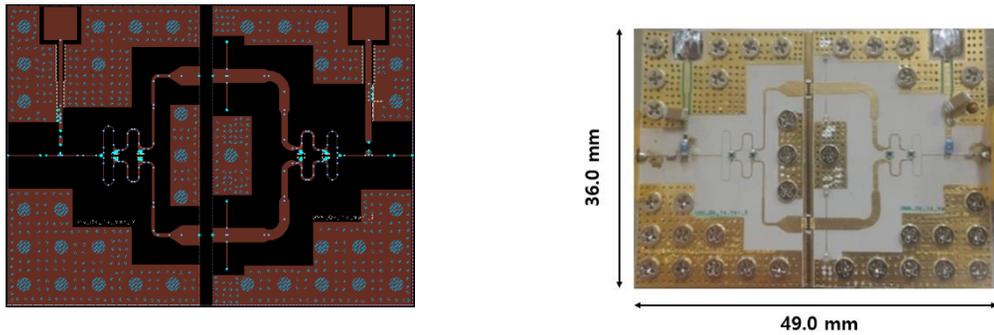


Figure 3.8 (a) Layout of the designed PA and (b) photograph of the module

The layout and photograph of the 2-way hybrid-type S/C-band PA is shown in Figure 3.8. RF-10 organic-ceramic substrate by Taconic with the dielectric constant of 10 was used for the input / output matching network. Wedge-bonding was employed to connect the CGHV1J025D transistor and the input/output matching networks.

3.3.2 Measurement Details

The fabricated module was measured at the bias of $V_{gs} = -2.4$ V, $V_{ds} = 40$ V, $I_{dq} = 674$ mA, which is the class-A bias, determined for the maximum extraction of output power.

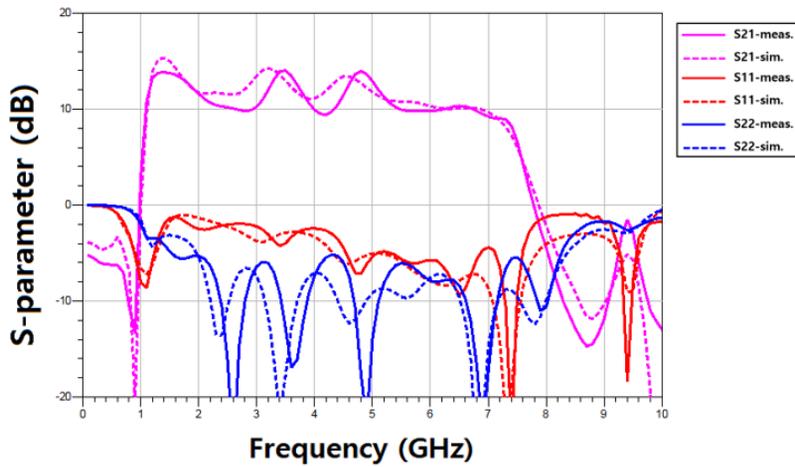


Figure 3.9 Simulated and measured S-parameters

Figure 3.9 shows both simulated and measured S-parameters of the fabricated module. The slight mismatch of the small-signal gain (S21) between simulation and measurement is mainly due to the process errors in the PCB fabrication. Width variation as large as 50 μm was observed in the fabricated PCB.

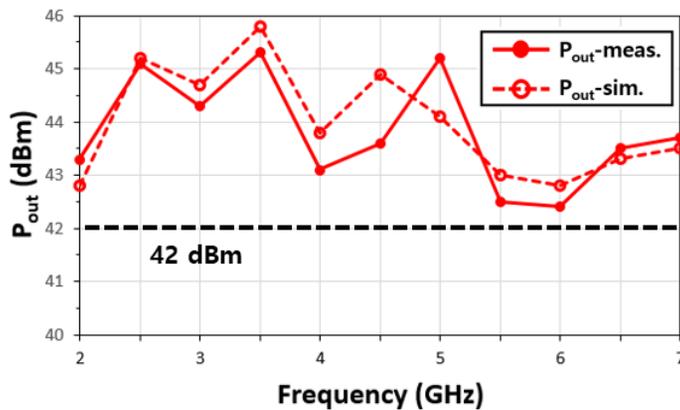


Figure 3.10 Simulated and measured output power (P_{sat})

Figure 3.10 shows the simulated and measured output power (P_{sat}) of the fabricated module. As shown in Figure 3.10, the output power is greater than 42 dBm across the 2.0 ~ 7.0 GHz bandwidth, exhibiting larger bandwidth than the previously designed 1-way PA. Since the output power was measured under CW condition, output power greater than 43 dBm across the 2.0 – 7.0 GHz bandwidth is expected to be observed under pulsed measurement. Figure 3.11 shows the simulated and measured result of drain efficiency (DE) at saturation power (P_{sat}). Drain efficiency greater than 20 % across the 2.0 – 7.0 GHz bandwidth is measured, closely following the simulation result.

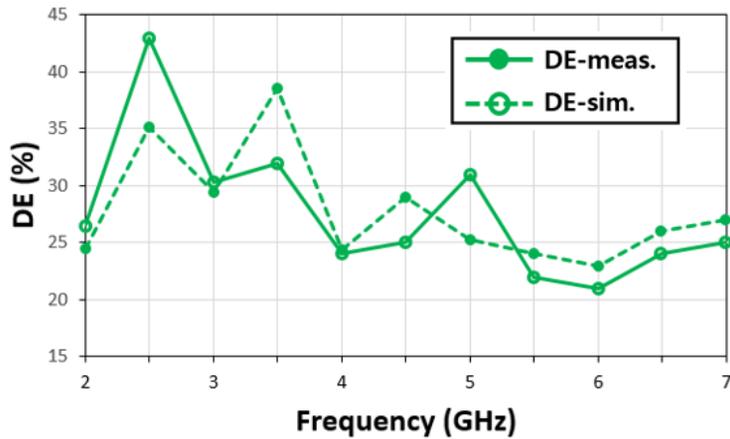


Figure 3.11 Simulated and measured drain efficiency (DE)

3.4 Conclusion

In this chapter, based on the 1-way PA implemented in Chapter II, a 2-way hybrid-type S/C-band high-power PA using two CGHV1J025D transistors was designed for IED jammer application. By using multi-section Wilkinson combiners as both a power combiner and a matching network, not only is the increase in the size of the overall PA architecture minimized, but also the bandwidth of the PA is greatly enhanced compared to the conventional topology using 1-section Wilkinson combiners at both input and output.

The validity of this proposed concept is theoretically analyzed by even-odd mode analysis. It has also been confirmed that removal of some shunt resistors inside the proposed matching networks are not detrimental to the isolation characteristics.

Broadband high-power characteristics have been observed, exhibiting more than 42 dBm saturated output power (CW condition) across 2.0 ~ 7.0 GHz bandwidth. Therefore, the PA topology using multi-section Wilkinson combiner as a matching component is suitable for the high-power broadband applications required by IED jammer. In addition, output power greater than 43 dBm across 2.0 ~ 7.0 GHz is expected under pulsed measurement.

Chapter 4 Conclusion

In this thesis, hybrid-type broadband high-power PAs using GaN-HEMT transistors are designed for IED jammer application. In order to realize both high-power and broadband characteristics, 2 broadband PAs with lower power level are combined in parallel to compensate for power degradation due to bandwidth enhancement.

In the first phase of the design process, 1-way broadband PA was designed using harmonic resistive loading for bandwidth enhancement. The fabricated 1-way module exhibited more than 45 dBm saturated output power across 2.5 to 6.5 GHz bandwidth, verifying that the employed topology is suitable for S/C-band high-power applications for IED jammer.

In the final stage of the design process, 2-way broadband high-power PA was designed by combining 2 1-way PAs designed from the previous stage. Instead of employing conventional Wilkinson combiner for power combining, multi-section Wilkinson combiners including matching networks within are employed for the reduction in the overall size and bandwidth enhancement. In order to verify the proposed concept at low expenditure, the 2-way PA was implemented using 2 CGHV1J025D transistors. The fabricated 2-way module exhibited more than 42 dBm saturated output power across 2.0 to 7.0 GHz bandwidth, showing great improvement in bandwidth over conventional PA combining method using 1-way Wilkinson combiner.

Future works include the implementation of hybrid-type S/C-band high-power PA using CGHV1J070 transistors to satisfy the performance specification (Table 1.2) required for IED jammer applications.

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Abstract (In Korean)

최근 원격 조정 급조폭발물 (IED) jammer 나 능동 전자주사식 위상배열 (AESA) 레이다 와 같은 전자전 (EW) 적용을 목표로 광대역, 고출력 전력증폭기에 대한 요구가 증대되고 있다.

본 논문에서는 IED jammer 적용을 목표로 질화갈륨 (GaN) 고전자이동도 트랜지스터 (HEMT) 를 이용하여 하이브리드 유형의 광대역, 고출력 전력증폭기를 설계하였다. 고출력 광대역 특성을 구현하기 위해 2개의 낮은 전력 수준의 광대역 전력증폭기를 병렬로 연결하여 대역폭 증가로 인한 전력 감소를 보상하였다.

첫번째 설계 단계에서는 대역폭 증가를 위해 고조파 저항 부하 구조를 이용하여 1-way 광대역 전력증폭기를 설계하였다. 설계된 1-way 광대역 증폭기는 2.5 에서 6.5 GHz 대역 내에서 45 dBm 이상의 포화 출력 전력을 나타내어 제안된 구조가 IED jammer 적용을 위한 S/C 대역 고출력 설계에 적합함을 검증하였다.

마지막 설계 단계에서는 앞서 설계한 1-way 전력증폭기 2개를 결합하여 2-way 광대역 고출력 전력증폭기를 설계하였다. 전력 결합을 위해 기존에 쓰이는 Wilkinson 결합기를 쓰는 대신에 정합단을 내부에 포함하는 다단 Wilkinson 결합기를 사용하여 전체 크기의 감소와 대역폭 증가를 확인하였다. 뿐만 아니라 선 구부림의 제약으로 인한 Wilkinson 결합기 내 일부 병렬 저항의 제거가 분리 특성 악화에 큰 영향을 주지 않음을 확인하여 일부 저항을 제거할 수 있었다. 제작된 2-way 모듈은 2.0 에서 7.0 GHz 대역 내에서 42 dBm 이상의 포화 출력을 나타내어 제안된 구조가 1 단 Wilkinson 결합기를 사용하는 기존 방법 보다

대역폭이 넓음을 확인하였다.

주요어 : 질화갈륨, 광대역, 고출력 전력 증폭기, 하이브리드 구현, 다단 Wilkinson 결합기

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