Master's Thesis

Design and Analysis of Low Dropout Regulator using Ground Regulation Technique

그라운드 제어 방법을 이용한 Low Dropout Regulator의 설계와 분석

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Abstract

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With a continuously high demand for portable electronic devices and System-on-Chip (SoC) devices in market, which uses Li-ion batteries, design of a low dropout regulator (LDO) with a high power supply rejection (PSR) is crucial to reject deterministic output ripple of a DC-DC converter, which is in between the battery output and a low dropout regulator, at the switching frequencies.

In response, this thesis presents a low dropout regulator with high unity gain bandwidth using ground regulation technique. The proposed low dropout regulator targets to have wide loop gain unity gain bandwidth to have the power supply rejection to be high even at high frequency (~ 1 MHz). Because wide bandwidth implies high quiescent current for an LDO, ground regulation technique with a reference change has been applied to reduce the current dissipation.

The proposed low dropout regulator is intended to be fabricated in 65 nm CMOS technology, achieves power supply rejection of -50.5 dB at 1 MHz, and dissipates quiescent current of 212 μA, which is a number that is reduced by 3 times from its complementary conventional LDO design with similar LDO performance.

Keywords : Low Dropout Regulator (LDO), Portable Electronic Devices, System-on-Chip (SoC), Ground Regulation, Power Supply Rejection (PSR), Quiescent Current

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Chapter 1. Introduction

1.1 Backgrounds

Low dropout regulators (LDO) have been an attractive solution with supplying power to many different things including, but not limited to, portable electronic devices, individual voltage domains in system-on-chip (SoC) [1,2] and display driver ICs (DDIs) [3,4]. All three systems share a common trait of having a DC-DC converter or switching regulators, usually in a form of a buck converter, in between the main power source (usually a Li-ion battery) and the LDO to step down the DC voltage closer to the operating voltage of the core system. DC-DC converters, however, have a deterministic ripple at its output with its magnitude inversely proportional to the values of inductors and capacitors in the DC-DC converters. Those ripples are at the frequency of the switching converters switching frequencies, which can be from few kilohertz to a few megahertz [5]. Because integrated circuits (ICs) are supply sensitive devices, it is important to provide a clean power supply to circuits, which implies that an LDO with a high power supply rejection (PSR) from low frequency to high frequencies, at least up to a few megahertz, needs to be designed.

To have a high PSR up to high frequency, an LDO needs to have high loop gain unity gain bandwidth, which means that the bias current of the error amplifier needs to be high. While most of the reported LDOs dissipate

about 10’s of microamperes, dissipating enough current to have a good high frequency PSR may require hundreds of microamperes, or even at miliampere range, which may degrade the efficiency of the LDO severely. Therefore, it is important to design an LDO that drives the pass transistor up to high frequency while dissipating small amount of current.

1.2 Motivation

There has been few cases reported that uses an architecture of LDO flipped upside-down [6,7]. While the configuration is used to overcome the ground bouncing noise issue and to control an oscillator’s frequency respectively, this architecture can be applied to a general LDO.

An LDO generally uses PMOS as the pass transistor and has an error amplifier that drives the pass transistor. PMOS, however, has a lower mobility than NMOS, usually in the range of 2.5~3 times lower. This implies that to have same amount of drain current given equal condition, size of the PMOS needs to be 2.5~3 times bigger than the complementary NMOS. From LDO’s perspective, this implies that the error amplifier can dissipate smaller amount of current to drive the NMOS to have same unity gain bandwidth as driving the PMOS. Change in reference is required as while the conventional LDO has the ground as reference and regulates the supply noise, the “flipped LDO” will need to set the power supply as the reference and treat the ground having the noise.

1.3 Thesis Organization

This paper proves the ideas described in the previous section. This paper describes an LDO with high gain bandwidth using ground regulation technique. This work is motivated from the need for a power efficient, a fine high frequency PSR. In addition, mathematically, this work rigorously proves that the noise effect from supply and the ground essentially becomes the same when the reference is changed. Furthermore, it compares the proposed architecture and the conventional architecture to experimentally prove the idea of increasing efficiency.

To demonstrate the idea, this paper starts by introducing basics of LDO in chapter 2. The chapter gives the architecture of a conventional LDO and explains few important specifications of LDO. It then provides few different types of LDOs to examine pros and cons of each architectures.

The design consideration of the proposed ground regulating LDO, proposal and few analyses are done in chapter 3. The chapter considers reference change and frequency response, provides a block diagram and schematic of the proposed architecture, compares the proposed architecture with the conventional architecture, and analyzes load transient of the proposed architecture.

The analysis is followed by simulation results in chapter 4. It gives alternating current (AC) simulations and transient simulations to verify the initial motivation. Chapter 5 concludes the thesis.

Chapter 2. Basics of Low Dropout Regulator

2.1 Architecture of Low Dropout Regulator

A block diagram of what is required for an LDO can be shown as Fig. 2.1; it is composed of a bandgap reference (BGR), an error amplifier (EA), and a pass element. Bandgap reference generates a voltage, temperature invariant voltage reference and gives it to the EA, which amplifies the difference between the reference and the output and calibrates the pass element until the reference and the output are matched. While EA and pass element work together to generate a clean supply, pass element also does a job of providing current into a load.

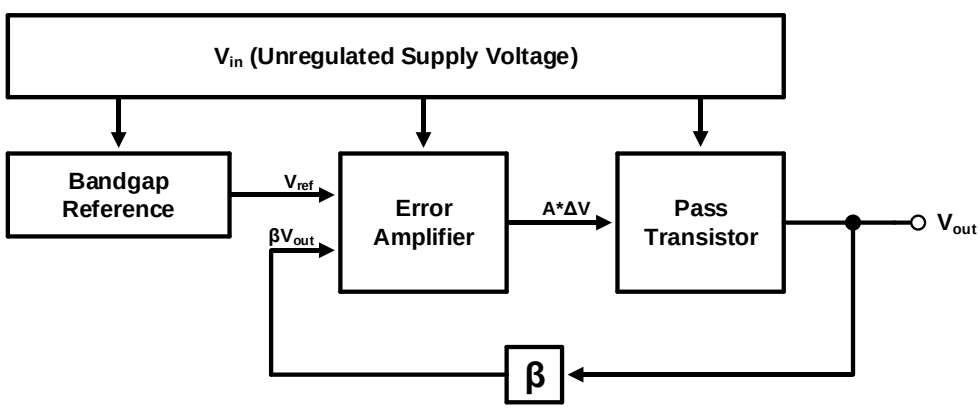

Fig. 2.1 Block Diagram of Low Dropout Regulator

Using this idea, a basic schematic of an LDO can be implemented as Fig. 2.2, an operational amplifier (op-amp) as error amplifier, and a p-

channel MOSFET (PMOS) as pass element. Bandgap reference is a thing that is required for LDO to generate a voltage reference but is generally not considered as part of LDO.

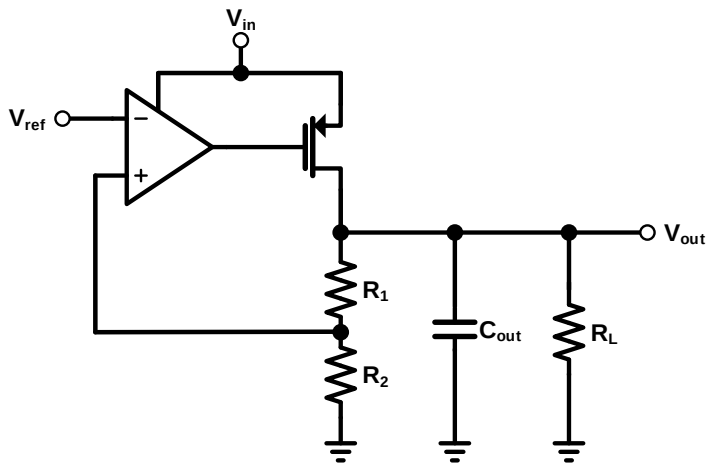

Fig. 2.2 Schematic of Low Dropout Regulator

A capacitor minimizes output voltage fluctuation due to change in the load current. To maximize efficiency (explained in detail in 2.2), V_{out} is desired to be close to V_{in}, but due to the challenges of generating V_{ref} close to V_{in}, the two resistors (R_1 and R_2) are present to increase the value of V_{out} as the following equation:

$$V_{out} = \frac{V_{ref}}{\beta} = \frac{R_1 + R_2}{R_2} \tag{2.1}$$

where β is the feedback factor of the loop.

2.2 Specifications of Low Dropout Regulator

There are several specifications need to be considered when designing an LDO. Line regulation and PSR specifies the extent of how much the output voltage varies with change in input voltage at DC and AC respectively. Load regulation specifies the amount of output voltage difference with change in load current. Transient response of output voltage when a step input of load current from minimum to maximum is applied needs to be considered. How the designed LDO meets all the specifications efficiently is also considered. While there are additional specifications such as die area and quiescent current, those are either secondary specifications that does not directly relate to the performance of LDO or has a close relation to one of the four criteria mentioned.

First and foremost important specification in LDO design is line regulation because low dropout regulator's primary purpose is to reduce supply noise. Line regulation is defined as circuit's ability to maintain the specified output voltage with varying input. In other words, line regulation is defined as

$$\text{Line Regulation} = \frac{\Delta V_o}{\Delta V_i} \tag{2.2}$$

and can be calculated using the following equation [8]:

$$\frac{\Delta V_o}{\Delta V_i} = \frac{1}{\beta A_{OL}(R_L + R_{on}||R_1 + R_2)} \tag{2.3}$$

where A_{OL} is the open loop gain for the error amplifier and R_{on} is the on resistance of the pass element. The equation shows that to improve line regulation performance, the error amplifier needs to have a high open loop gain. One can design PMOS and feedback resistor values such that the resistance values are high to further improve the line regulation but the optimum on resistance depends on the required dropout voltage and the load current, and increasing the R_1 and R_2 values increase noise generated by the two resistors and the die area. Line regulation is a steady state parameter; change in output voltage with respect to change in input voltage as a function of frequency is defined as power supply rejection (PSR) which this thesis has focus on.

Another purpose of low dropout regulator is to provide enough current to the load. Low dropout regulator has shown to not exactly stay at a constant output voltage with varying load conditions. To quantize the degree of such change, line regulation is defined as change in output voltage with change in load current, i.e.:

$$\text{Load Regulation} = \frac{\Delta V_o}{\Delta I_L} \tag{2.4}$$

and can be calculated using the following equation [8]:

$$\frac{\Delta V_o}{\Delta I_L} = \frac{R_{on}}{1 + \beta A_{OL}} \tag{2.5}$$

Just like line regulation, load regulation is a steady state parameter. Output voltage variation with dynamical change in load current is analyzed in transient response, which is another important specification. In LDO design, transient response has a specific meaning of looking at the maximum allowable output voltage change for a full step of load current change. The worst-case occurs when the load current steps from its specified minimum value to the maximum value. The change in the output voltage can be calculated by the following equations [9]:

$$\Delta V_{out} = \Delta I_{out} * \frac{\Delta t}{C_{out}} \tag{2.6}$$

where,

$$\Delta \mathrm{t} \approx \frac{1}{BW_{CL}} + t_{SR} \tag{2.7}$$

and

$$t_{SR} = \frac{C_p \Delta \mathrm{V}_p}{I_{SR}} \tag{2.8}$$

Last specification to be considered is efficiency. Low dropout regulator is a circuit that sacrifices the voltage level to get a cleaner supply, which such sacrifice should be kept minimum. In addition, while LDO provides a large amount of current to the load, LDO itself dissipates non-negligible amount of current, which is defined as quiescent current. While it is important to keep quiescent current low itself, it is more logical to look at the ratio of quiescent current to the total current LDO draws from the supply. These two ideas combined lead to define the efficiency (η) of LDO to be as following equation:

$$\eta = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{(V_{in} - V_{DO})I_{out}}{V_{in}(I_Q + I_{out})} \quad (2.9)$$

2.3 Different Types of Low Dropout Regulator

Before a new architecture is proposed, previously proposed architectures need to be examined. While this thesis does not cover an exhaustive list of different LDOs, it covers different types of LDOs and its respective pros and cons. Types of LDOs that are covered are LDO with multi-stage amplifiers, rail-to-rail regulating LDO, supply regulating LDO with NMOS as pass transistor and digital LDOs. One big classification of LDO is LDO with an external capacitor and LDOs without an external capacitor, but the comparison of the two types of LDO is done and analyzed

in the later part of the thesis. Comparison of the proposed architecture and a conventional LDO is done in later part of the thesis as well.

2.3.1 LDOs with Multi-Stage Amplifier

First group of LDOs to be examined is LDO with multi-stage amplifiers. Because both the load regulation and line regulation depend on the DC gain, multi-stage amplifier can be used to further increase the DC gain of the amplifier. An example circuitry can be shown as figure 2.3 [10].

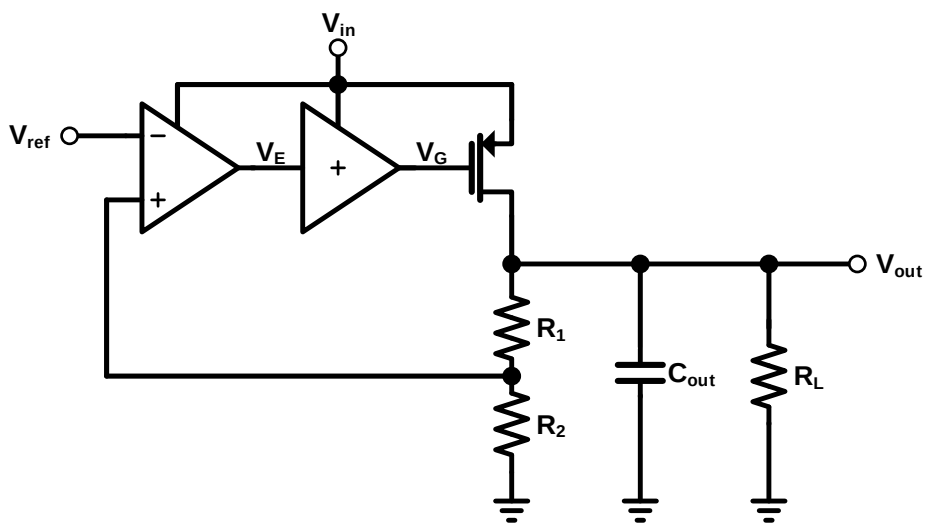

Fig. 2.3 Typical LDO with Two Amplifier Stages

Having multiple gain stages increase the overall DC gain of the amplifier but it introduces additional pole at V_E. While there are few classical frequency compensation techniques such as Miller compensation technique [11] or nested Gm-C compensation technique [12] that can be

applied to the circuit to push poles to higher frequencies, there is a trade-off between compensating capacitor values and the amount of frequency that the pole is being pushed.

2.3.2 Rail-to-Rail Regulating LDOs

Second group of LDOs to be examined is rail-to-rail regulating LDOs. As shown in figure 2.4 [13], it regulates noise from both V_{DD} and ground by having a fully differential amplifier with two pass transistors and some additional circuitry for common mode feedback (the load is a VCO). Regulating both the supply and the ground has a benefit of the circuit not requiring as much size of decoupling capacitor in between the supply and the ground [4,13].

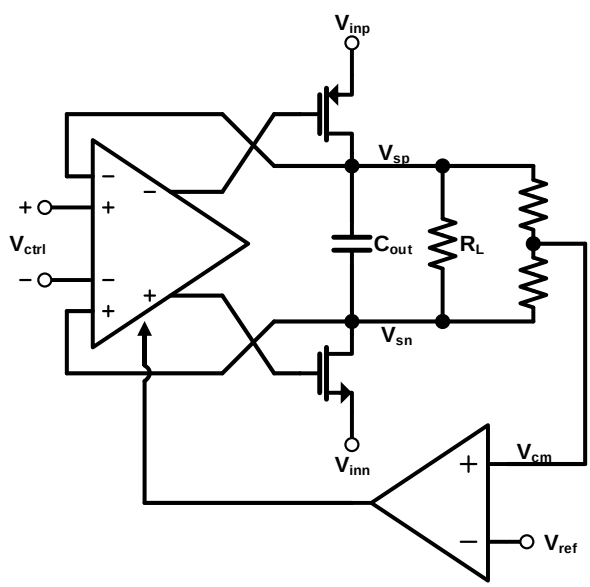

Fig. 2.4 Schematic of a Rail-to-Rail Regulating LDO

However, such architecture has a critical problem of the load having reduced voltage headroom by doubling the amount of dropout voltage and ends up compensating the loads performance as a result. In addition, from the perspective of the unity gain bandwidth of the LDO's loop gain, the V_{DD} regulating part with PMOS pass transistor becomes the bottleneck as this LDO needs to have both V_{SP} and V_{SN} settled, so the bandwidth essential becomes the same as the conventional LDO. Lastly, such architecture increases design complexity by having a fully differential amplifier, a common mode feedback, and a floating point bandgap reference. Therefore, rail-to-rail regulating LDOs may reduce the overall area but ends up compensating circuit's performance metrics.

2.3.3 Supply Regulating LDO with NMOS as Pass Transistor

Third group of LDOs to be analyzed are LDOs with NMOS as pass transistor. Having an NMOS as the pass transistor can benefit with the fact that NMOS has higher mobility, which this thesis also exploits. However, regulating V_{DD} with an NMOS requires additional circuitry for bootstrapping with switched capacitor and charge pump to have a voltage level above V_{DD} to overcome the threshold voltage of the NMOS. An example of this is demonstrated in figure 2.5 [14].

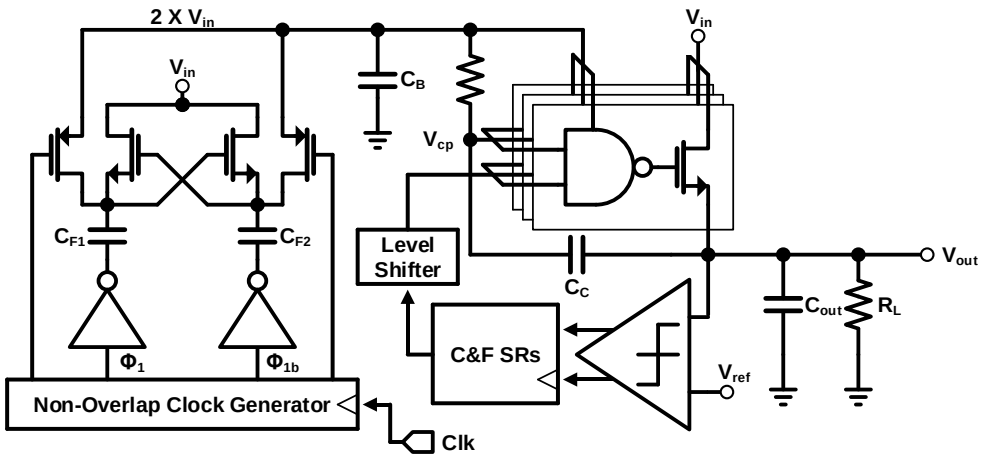

Fig. 2.5 LDO with NMOS Pass Transistor with Bootstrapping Circuitry

If the V_{out} is at 1.0 V and V_{DD} is at 1.2 V, then the required gate voltage of the pass transistor is 1.0 + V_{th_pass} V to start turning on the pass transistor, and the bootstrapping technique provides a voltage level that is twice of V_{DD} to have the drivers of pass transistors (NAND gates in the figure) to be able to drive the pass transistors above the input level.

Such circuitry, however, requires special clock for ϕ_1 and ϕ_{1b} as the two clocks need to be operating at non-overlapping times to avoid charge sharing of two capacitors, which circuitry shown includes. In addition, threshold voltage of the pass transistors is at much higher than its average threshold voltage because the NMOS also experiences body effect. Therefore, LDO with NMOS as pass transistor are not suitable for design.

2.3.4 Digital LDOs

Last group LDOs to be considered is digital LDOs. As shown in figure

2.11 [15], digital LDOs include a comparator, a controller with bi-directional shift registers and n-many pass transistors. General digital LDO works as follows: the comparator compares the output with a given voltage reference and outputs either 1 or 0 and the bi-directional shift registers shift either left or right, depending on the comparator output, to control the number of pass transistors to be turned on. Digital LDOs give an extremely small amount of dropout voltage (~ 50 mV).

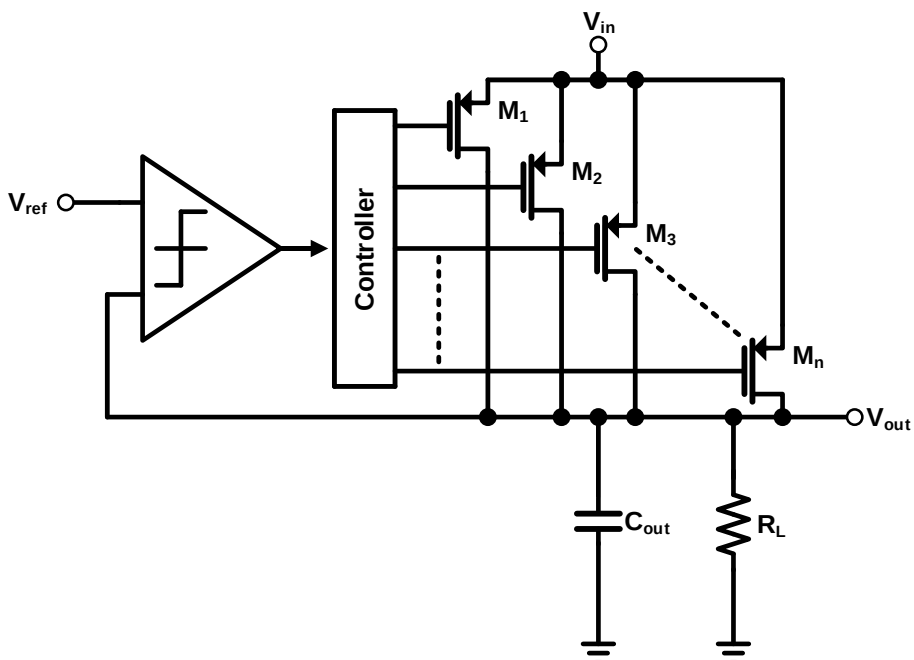

Fig. 2.6 Schematic of a Digital LDO

However, digital LDOs has a tradeoff between resolution & speed and power. In addition, it requires a clock to continuously regulate the input voltage. Such clock dissipates a large amount of current. To reduce the

amount of current dissipated in the LDO, designers generally use clock in MHz frequency, but it is not feasible to regulate a noise in MHz range. In addition, PSR is generally not considered as a specification due to the nature of its operation.

Chapter 3. Design of Ground Regulating LDO

3.1 Analysis on Reference Change

This thesis adopts a new notation '=|=' to mean 'voltage difference of.' For example, a nominal V_{DD} =|= V_{SS} would equal to 1.2 V for a general 65 nm technology and 1.8 V for a general 180 nm technology.

Due to non-idealities, V_{DD} and V_{SS} does not stay at their nominal values. In other words, the system works with following power supplies:

$$V_{DD} + n_D(t) = | = V_{SS} + n_s(t) \tag{3.1}$$

where $n_D(t)$ and $n_S(t)$ are noise in V_{DD} and V_{SS} respectively. Circuit designers conventionally used node V_{SS} as ground reference and treat it as the 'absolute zero' and measure with negative side of a probe connected to the V_{SS} node. This would give

$$V_{DD} + n_D(t) - n_s(t) = | = V_{SS} \tag{3.2}$$

and $n_D(t) - n_S(t)$ would be treated as a total noise seen in V_{DD}. This is valid as V_{DD}, V_{SS}, $n_D(t)$ and $n_S(t)$ are simple numbers/variables/functions, algebraic manipulation can be applied.

On the other hand, subtracting $n_D(t)$ from both sides of equation 3.1

gives

$$V_{DD} = | = V_{SS} - (n_D(t) - n_s(t)) \tag{3.3}$$

which means that V_{DD} is clean and $-(n_D(t) - n_S(t))$ is the noise seen in V_{SS}. This may not mean anything if the reference is V_{SS} but would mean something if V_{DD} is chosen as the reference node. Equations 3.2 and 3.3 are numerically valid but the fact that changing the reference does not change the performance of the load needs to be shown. To prove that changing the reference does not change the performance of all systems, the following circuit shown in figure 3.1 is analyzed.

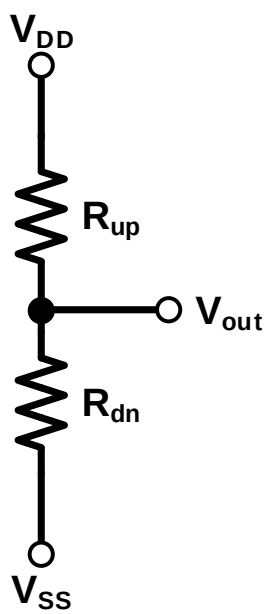

Fig. 3.1 A Circuit to be Analyzed

Using Kirchhoff's Laws and Ohm's Law gives

$$V_{out} = \beta_{DD} V_{DD} + \beta_{SS} V_{SS} \tag{3.4}$$

where,

$$\beta_{DD} = \frac{R_{dn}}{R_{up} + R_{dn}}, \qquad \beta_{SS} = \frac{R_{up}}{R_{up} + R_{dn}} \tag{3.5}$$

If V_{DD} has a noise n(t) with V_{SS} as a reference, that noise is amplified by a factor of $\beta_{DD} < 1$ and be shown to V_{out}, and if V_{SS} has a noise with V_{DD} as a reference, that noise is amplified by a factor of $\beta_{SS} < 1$. With supply noise n(t) present, V_{out} sees β_{DD}*n(t) but with V_{DD} as reference, β_{DD}*n(t) needs to be subtracted by n(t), resulting in $-\beta_{SS}$*n(t) (note that $\beta_{DD} + \beta_{SS} = 1$) which is equivalent as seeing the same amount of noise from V_{SS}. Then, the amount of V_{DD} noise with V_{SS} as a reference becomes equal to the amount of V_{SS} noise with V_{DD} as a reference when R_{up} and R_{dn} are switched.

While the example is shown with resistors for understanding purpose, this idea not only applies with resistors but also applies to any impedances, as long as the system is linear, without loss of generality. However, because most of analog circuits are analyzed using small signal model, which assumes linearity, this idea can be applied to most of those circuits. Therefore, changing the reference does not change the performance of the circuit.

3.2 Frequency Response Analysis

To have a high PSR up to high frequency (~ 1 MHz), an LDO needs to have a high unity gain bandwidth (UGB) while maintaining a good stability. While LDO is generally considered as a 2-pole system with low UGB, introduction of third pole cannot be neglected in the proposed design with UGB in 100's of mega-hertz range. To demonstrate, figure 3.2 shows a typical loop gain frequency response of an uncompensated 3-pole system.

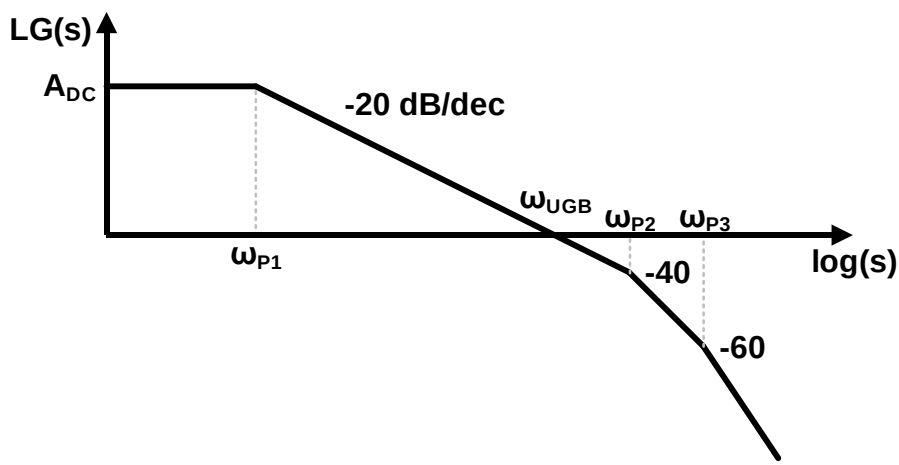

Fig. 3.2 Frequency Response of a typical 3-Pole System

Since phase of the response as a function of frequency is given as

$$\phi_{LG}(s) = -tan^{-1}\left(\frac{s}{\omega_{p1}}\right) - tan^{-1}\left(\frac{s}{\omega_{p2}}\right) - tan^{-1}(\frac{s}{\omega_{p3}}) \qquad (3.6)$$

to meet f_{UGB} = 100 MHz and phase margin (ϕ_M) of 45°, second pole of the

system can be calculated and required to be at a frequency greater than 141 MHz while the third pole of the system needs to be much greater than 100 MHz (at least greater than 10 times f_{UGB}). While the location of the first pole can be adjusted based on the DC gain (A_{DC}) of the system and the location of the desired UGB, second pole and third pole need to be kept at high frequencies in order to have high UGB with good enough phase margin.

Two different types of LDOs can be considered with frequency response in mind: an LDO with an external (off-chip) capacitor, and an LDO without an external capacitor (cap-less LDO). The difference is that off-chip cap. LDO has an external capacitor in the microfarad range, while a cap-less LDO only has an on-chip capacitor in 100's of picofarad range. Because pole at the gate stays constant for both LDOs, the difference of the output pole's frequency location needs to be considered. However, output pole of the LDO with an off-chip capacitor is at much lower frequency (typically, output pole of an LDO with an off-chip capacitor is considered and designed to be dominant), making such architecture not applicable for an LDO with high loop gain unity gain bandwidth.

3.3 Proposed Architecture

Figure 3.3 shows a schematic of the proposed system. Similar to the conventional LDO, the proposed LDO includes an error amplifier and a pass

element. Unlike the conventional LDO, however, the proposed LDO takes the idea of switching R_{up} and R_{dn}, and has routing of the conventional LDO flipped upside-down with the load being supplied between VDD and regulated V_{SS}. This architecture takes V_{DD} as the reference and regulates noise from the input. A compensation capacitor (C_c) and a nulling resistor (R_z) are included to push the second pole of the system to higher frequency by introducing a left hand side zero based on the following equation [16]:

$$f_z = \frac{g_{mpass}}{2\pi C_c(\frac{1}{g_{mpass}} - R_z)} \tag{3.7}$$

The values of R_z and C_c are determined to be equal such that f_z is equal to f_{p2}. Since f_{p2} is a load dependent constant, once f_{p2} is determined, R_z and C_c can be determined. A conventional charge pump phase locked loop (PLL) is tied as the load.

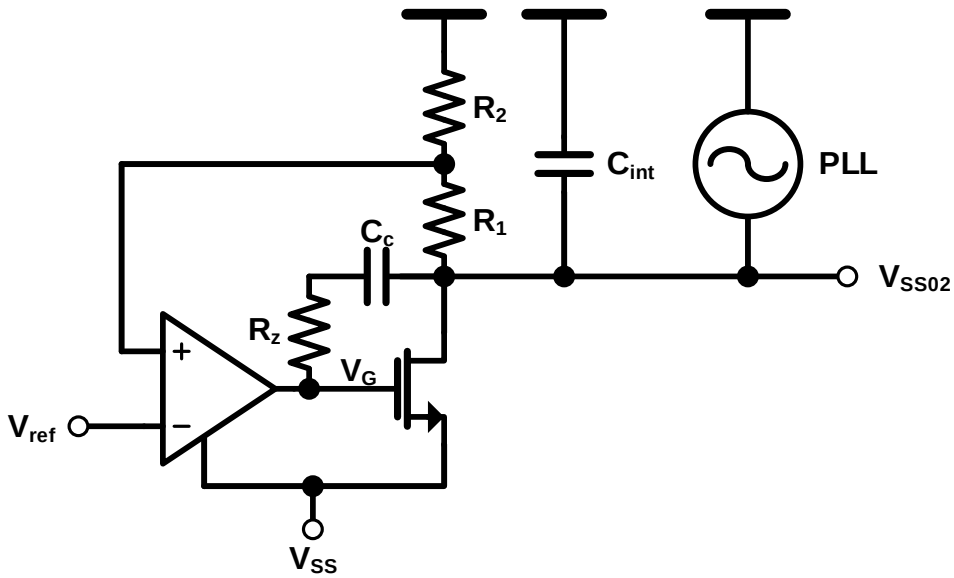

Fig. 3.3 Schematic of the Proposed Architecture

The LDO is designed to regulate supply noise for a PLL. A block diagram of the designed PLL for a test is shown in figure 3.4. Loop filter is tied between V_{DD} and V_{ctrl} to adopt the reference change. In addition, because of the reference change, PFD's up signal is tied to the bottom switch and the dn signal is tied to the upper switch. Further explanation is done with circuit implementation.

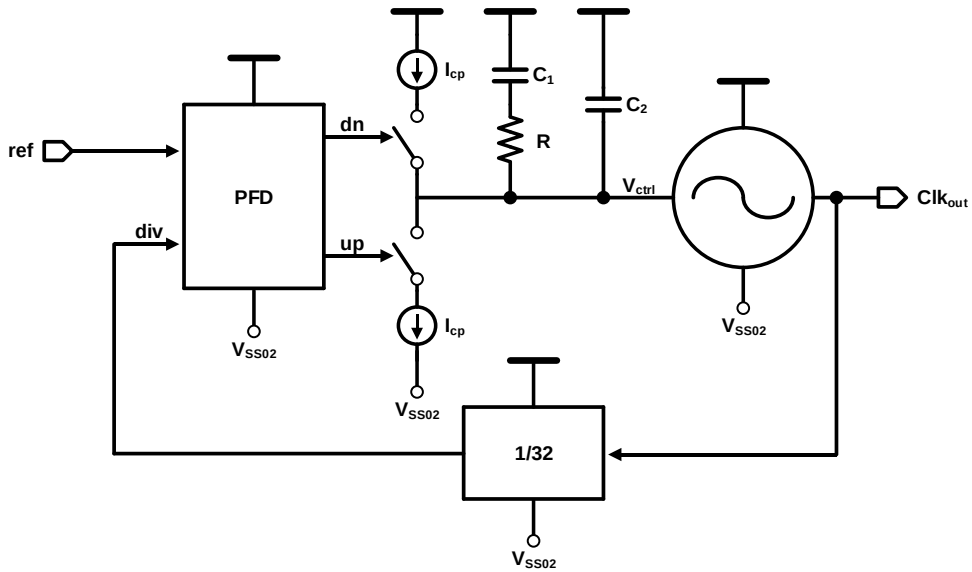

Fig. 3.4 Block Diagram of the Designed PLL

The designed PLL targets to output a 3 GHz clock from 93.5 MHz reference clock. The values of R, C_1, C_2 and I_{cp} are 50 kΩ, 1.93 pF, 62.8 fF, and 9.7 μA, which are chosen to meet unity gain bandwidth of the PLL to be 9.35 MHz and phase margin of 70°.

3.4 Circuit Implementation

The implemented error amplifier of the LDO is shown in Figure 3.5. It is a Class-A type telescopic amplifier. A single stage amplifier is implemented to exclude any additional pole in the system to increase bandwidth of the LDO.

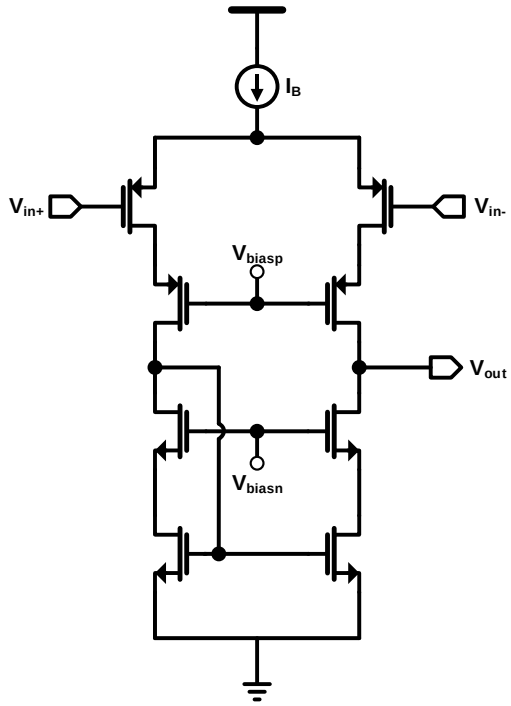

Fig. 3.5 Circuit Diagram of the Implemented Error Amplifier

The implemented phase-frequency detector (PFD) and VCO are shown in figures 3.6 and 3.7 respectively. The VCO is an 8-phase differential current starved ring VCO. While an NMOS receives control voltage in a conventional VCO, PMOS receives VCO's control voltage in the implemented VCO to adopt the change in reference. As a result, PFD is implemented with up and down_bar signals as opposed to a conventional PFD with up_bar and down signals because lower control voltage makes the implemented VCO run faster while higher control voltage makes conventional VCO run faster. Charge pump and divider are implemented using conventional blocks.

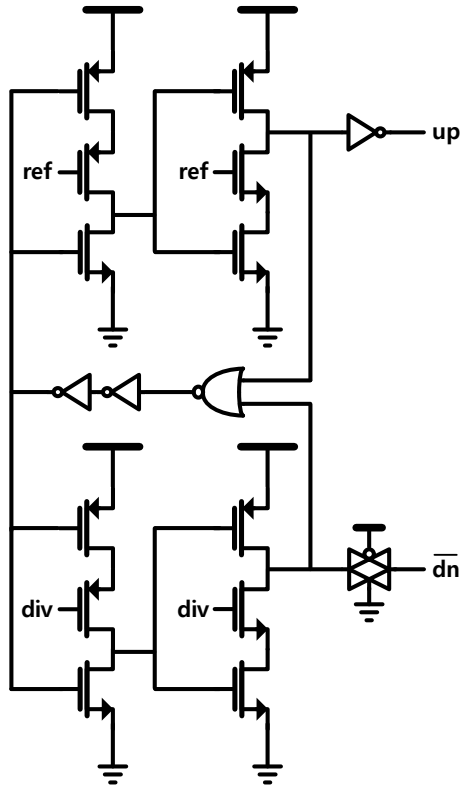

Fig 3.6 Circuit Diagram of the Implemented Phase-Frequency Detector

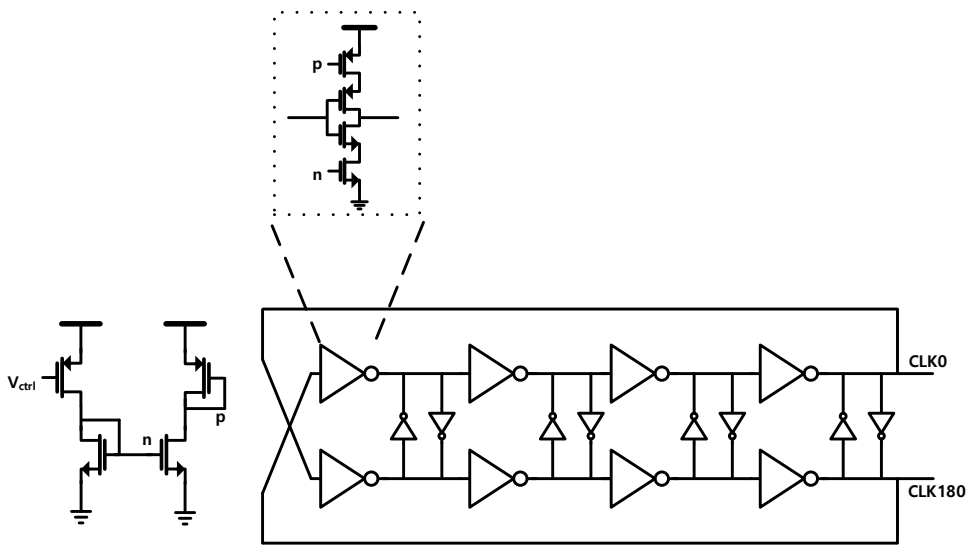

Fig 3.7 Circuit Diagram of the Implemented Voltage Controlled Oscillator

A typical NMOS in a technology has its body tied to the substrate. However, because this thesis aims to regulate the ground noise, the body of the NMOS of the load PLL needs to be separated from the substrate. This requires a triple-well process, which is also known as deep N-well process. A cross sectional view of an NMOS using this process is shown in figure 3.8.

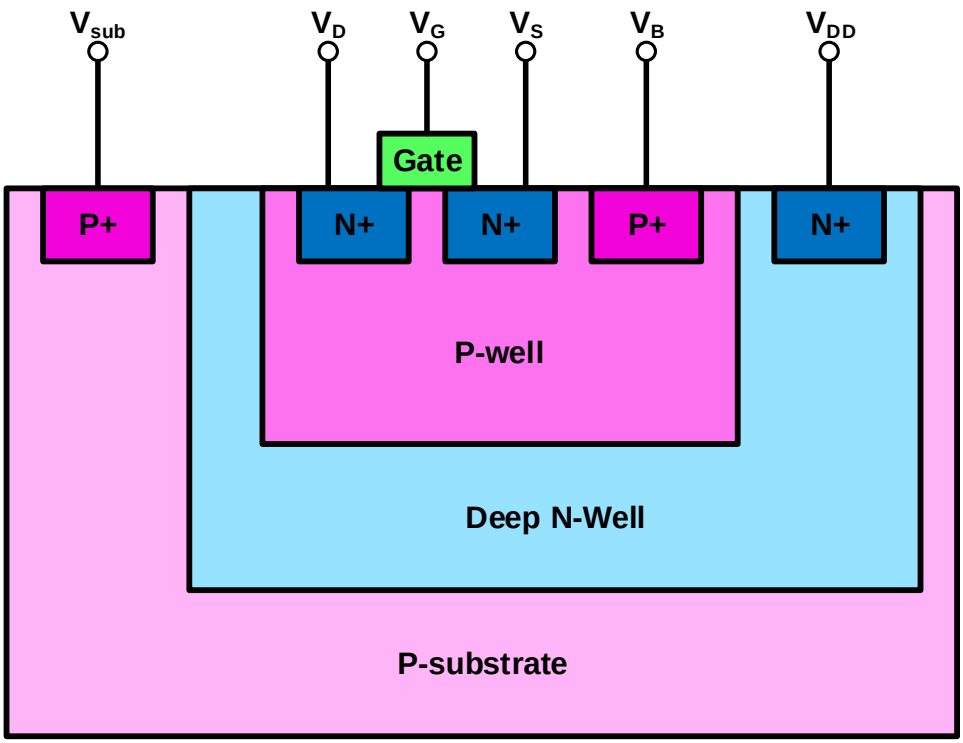

Fig. 3.8 Cross Sectional View of an NMOS using Deep N-Well Process

V_{sub} is the substrate potential (generally tied to V_{SS}), V_D, V_G, V_S, and V_B are voltages of the drain, gate, source and body of the NMOS respectively. As the figure shows, deep N-well layer separates the P-well layer and the P-substrate layer, enabling the NMOS' body to have an

independent voltage from P-substrate. To prevent latch up from occurring between P-well and N-well, N-well potential is connected to the highest given potential, which is V_{DD}. All of the bodies of NMOS' in the designed PLL are connected to the regulated ground output voltage, which is V_{SS02}.

3.5 Comparison of a Supply Regulating LDO and Ground Regulating LDO

Schematics of basic supply regulating LDO (V_{DD}-LDO) and ground regulating LDO (V_{SS}-LDO) are shown together in figure 3.9 for comparison purpose. While a V_{DD}-LDO uses PMOS as pass transistor to provide regulated supply voltage to a load (VCO in the figure), V_{SS}-LDO uses NMOS as a pass transistor to provide regulated ground voltage to the load. To provide same supply conditions to the load, both pass transistors need to have same amount of dropout voltage and drain current (note that the two V_{ref}'s need to be different for this specific schematic).

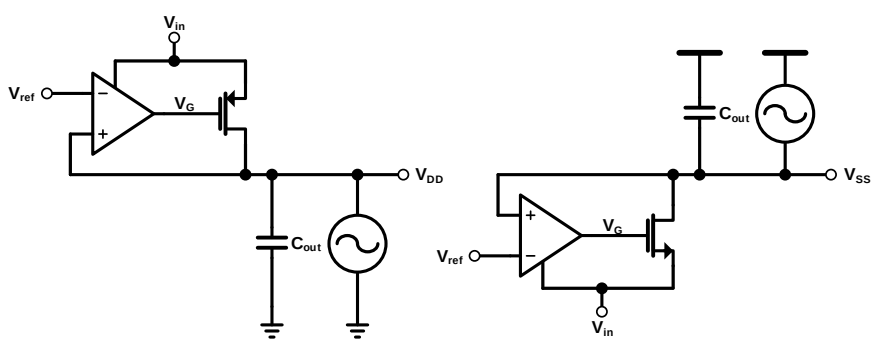

Fig. 3.9 Schematics of Supply and Ground Regulating LDOs

To equate the operations of the two LDOs, the drain current (I_D) of the pass element needs to be equal given same overdrive voltage (V_{ov}) from equation 3.8,

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2 \tag{3.8}$$

which is the equation of a MOSFET in saturation region. Channel length modulation effect has been neglected because the two drain to source voltages (V_{ds}) are equal, namely V_{DO}. However, because the mobility of the two pass elements are different, W/L of the two pass transistors need to be different, namely, the following equation needs to be satisfied:

$$\frac{(\frac{W}{L})_n}{(\frac{W}{L})_p} = \frac{\mu_p}{\mu_n} \tag{3.9}$$

Because mobility of NMOS (μ_n) is typically around 2.5~3 times the mobility of PMOS (μ_p), width of the PMOS pass transistor is expected to be 2.5~3 times bigger than the width of the NMOS pass transistor. This would result in gate capacitance of the pass transistor to be different by a factor of 3, and in cap-less LDO, which has its dominant pole at the gate of the pass transistor, error amplifier of the V_{SS}-LDO can reduce current consumption

by a factor of 3, making the V_{SS}-LDO more favorable.

3.6 Load Transient Analysis

Last specification to be considered is load transient. Because PLL is a dynamic system that does not dissipate static current, analysis of load transient is essential. Consider figure 3.10, which shows a transistor-level schematic of a 3-stage single-ended ring oscillator. Transistor numbers are labeled such that transistors are turned on in the order of increasing number. Understanding of this ordering can start by assuming that the voltage of the gate node of transistors 1 and 4 is 0. This would mean transistor 1 is turned on which pulls up the voltage of gates of transistors 2 and 5 to V_{DD}, which turns on transistor 2 and pulls down the voltage of gates of transistors 3 and 6 to ground, and so on. Continuing this and lastly having transistor 6 turned on and having gate voltage of transistors 1 and 4 to zero goes back to the initial condition. This completes one clock cycle and the oscillator continues the cycle and oscillates.

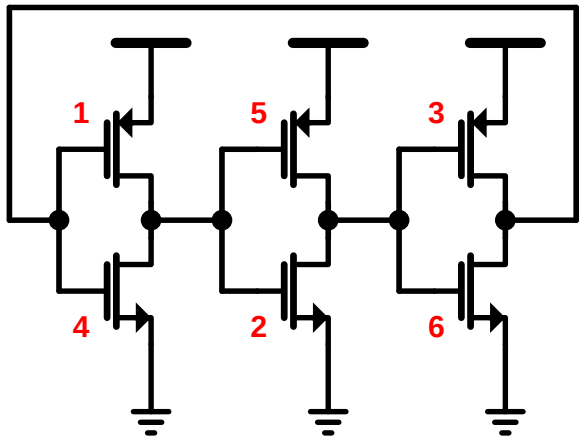

Fig. 3.10 Schematic of a 3-stage single-ended ring oscillator

In one clock cycle, all transistors are turned on and off once. The number of times this oscillator sinks current into the ground is equal to the number of NMOS in the oscillator, which is 3. This means that with an LDO attached, it will see 3*3 GHz = 9 GHz of deterministic noise at the LDO output. Similarly, for a 4-stage differential ring oscillator, number of times the oscillator sinks current into the ground is 8. For a 3 GHz VCO, the LDO sees 24 GHz of deterministic noise at the LDO output. While differential ring oscillator has 4 additional NMOS' in latches, those simply help the complementary nodes to stay complementary and works together with the NMOS in the stages.

A simulated verification of this idea is shown in figures 3.11 and 3.12 for 3-stage single-ended oscillator and 4-stage differential oscillator respectively. Simulation is done with ideal voltage source attached with sizes of transistors to be such that the oscillator oscillates near 3 GHz, and

the current into the ground has been measured (i_{vss}). Counting the number of rising edges of current in between two consecutive rising edges of the highlighted (in red) clock output gives 3 and 8 for 3-stage single-ended oscillator and 4-stage differential oscillator respectively, which means that current sunk into the ground is periodic with 9 GHz and 24 GHz frequency.

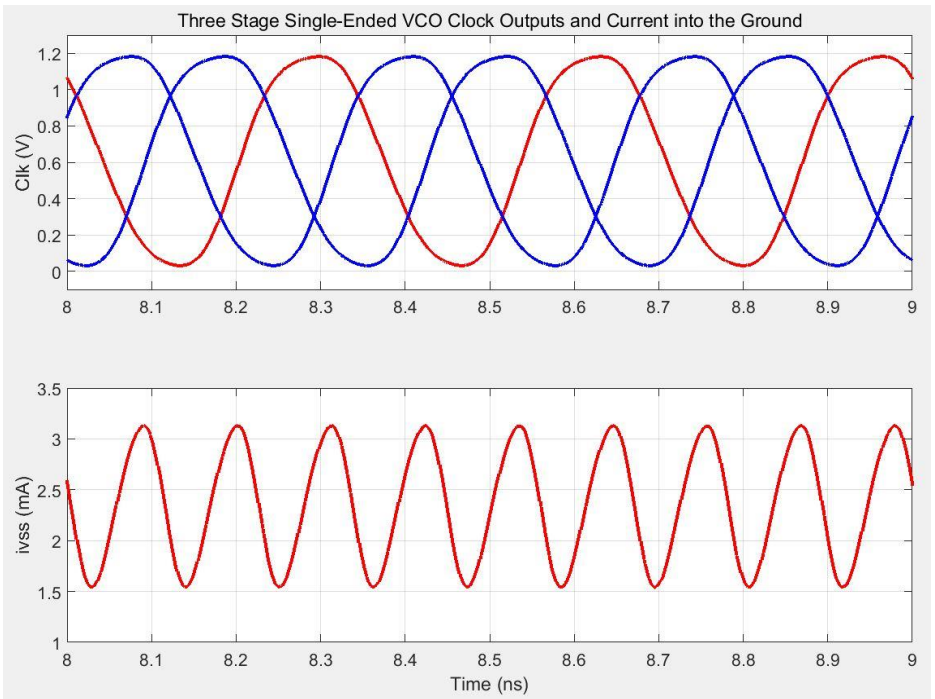

Fig. 3.11 Waveform of simulated 3-stage single-ended ring oscillator clock output and current sunk into the ground

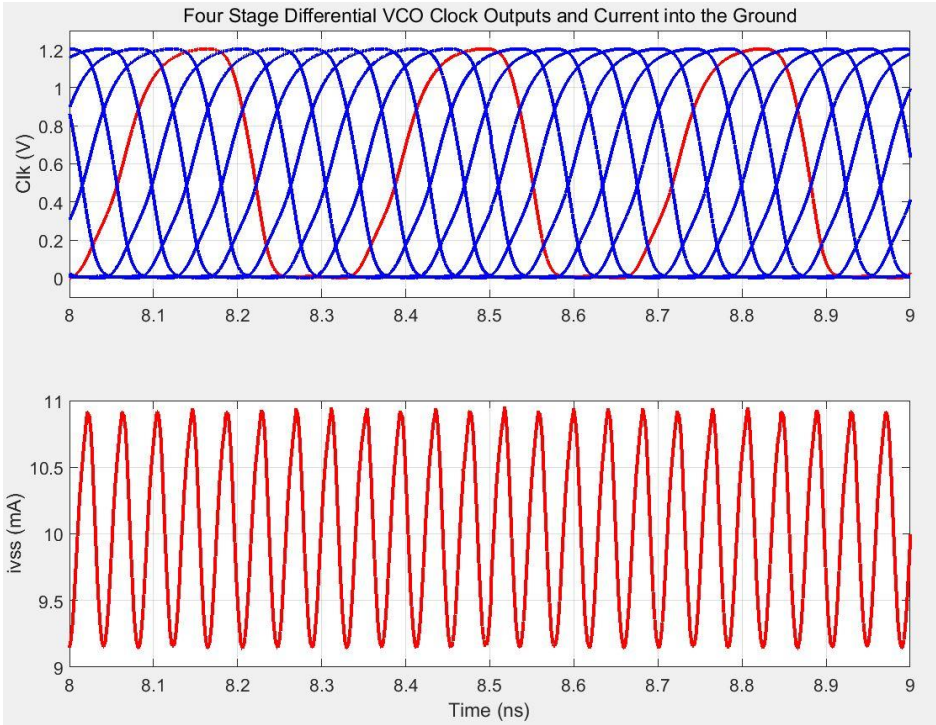

Fig. 3.12 Waveform of simulated 4-stage differential ring oscillator clock output and current sunk into the ground

The implemented LDO not only sees VCO as a load, but also sees other blocks of PLL. However, by designing it to have the current in VCO to be dominant, the 24 GHz of deterministic noise becomes the dominant noise source to the LDO output. Not only that the 24 GHz noise is a self-induced noise from VCO and does not affect the phase noise of the clock output, but also the noise is at such a higher frequency compared to the designed of the PLL UGB (by a factor of 24 GHz/9.35 MHz = 2567) and the noise gets filtered eventually.

While the current is pulled from V_{DD} as well, considering only the

current sunk into the ground is sufficient as the V_{DD} is considered as reference and current into the ground is what changes the regulated ground voltage.

3.7 Level Shifter

Because the designed LDO outputs a voltage above 0 V, namely 200 mV, the load PLL is required to have a level shifter to bring the output low of 200 mV down to 0 V before the load PLL is used in a digital system. A level shifter is required for two main reasons. First reason is to prevent the 200 mV to turn on the NMOS' in the digital system, which then the system may not operate properly, depending on NMOS' threshold values. The second reason is to prevent any subthreshold leakage current with input not being pulled down completely. Because PLL generates a clock, such level shifter can be as easy as a simple CML-to-CMOS converter, which a schematic can be shown as figure 3.13:

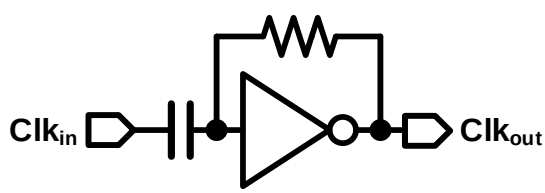

Fig. 3.13 Schematic of a CML-to-CMOS Converter

Chapter 4. Simulation Results

4.1 Layout

The designed LDO-PLL is intended to be fabricated in 65 nm CMOS technology. Figure 4.1 shows the layout micrograph of the designed system. It includes a 3.5 pF of an on-chip capacitor between V_{DD} and LDO output to suppress the deterministic 24 GHz output ripple that comes from VCO. Few MIM capacitors are present near VCO to keep the power supplied to the VCO as intended. A capacitor is used in the charge pump block to keep the single compensation to stay stable. The die has active area of 0.02851 mm^2.

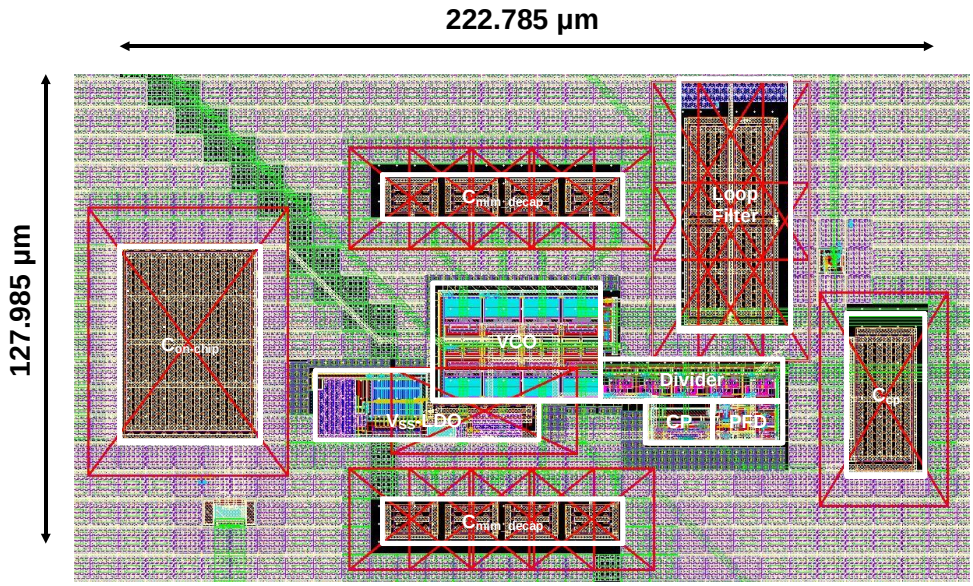

Fig. 4.1 Layout Micrograph

4.2 Alternating Current Simulations

Figure 4.2 shows the alternating current (AC) simulations of PSR, loop gain magnitude, and loop gain phase for 3 process corners (SS, TT, FF) of the proposed V_{SS}-LDO. The worst cast DC PSR is -58.1 dB (FF), PSR at 1 MHz is -50.5 dB (SS), DC loop gain is 46.5 dB (FF), loop gain unity gain bandwidth is 231 MHz (SS) and the phase margin is 45.4° (FF).

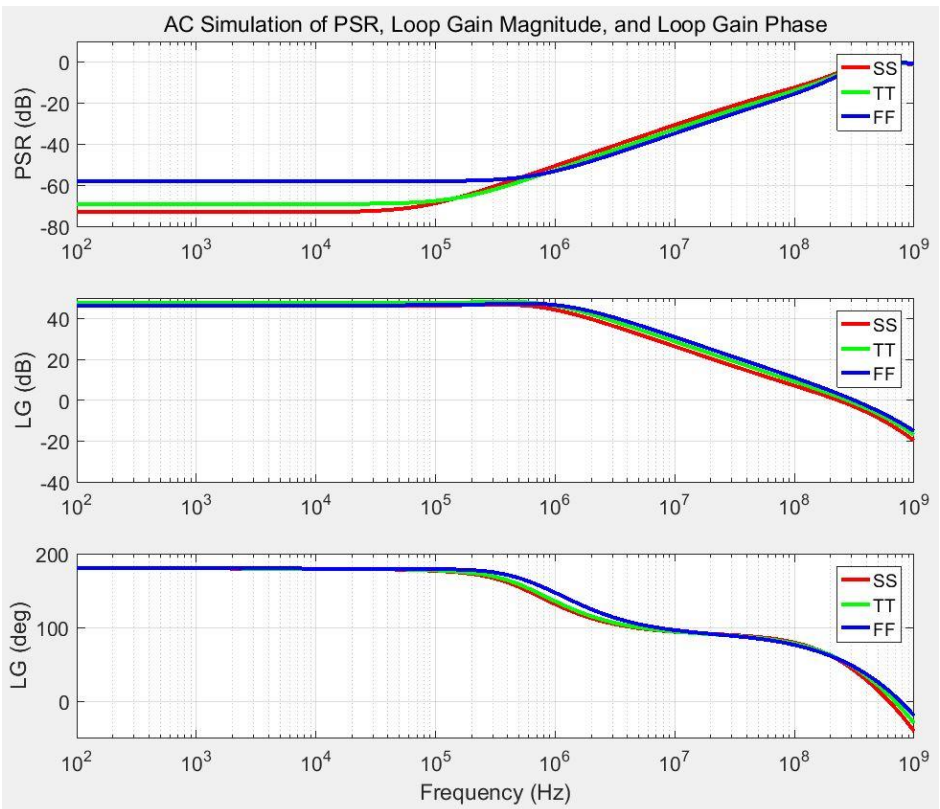

Fig. 4.2 AC Simulation of PSR and Loop Gain

Figure 4.3 shows the schematic of implemented complementary V_{DD}-LDO for comparison purpose. The V_{DD}-LDO is designed to match the unity

gain bandwidth and PSR at 1 MHz with the proposed V_{SS}-LDO. The ratio of the sizes of the pass transistors of V_{DD}-LDO and V_{SS}-LDO is 4, which the simulation has shown that ratio of 4 makes the two pass transistors to have the same overdrive voltages. The remaining other parameters and components remain the same except for the error amplifier which is implemented as a telescopic amplifier with NMOS input as opposed to proposed telescopic amplifier which uses PMOS as the input.

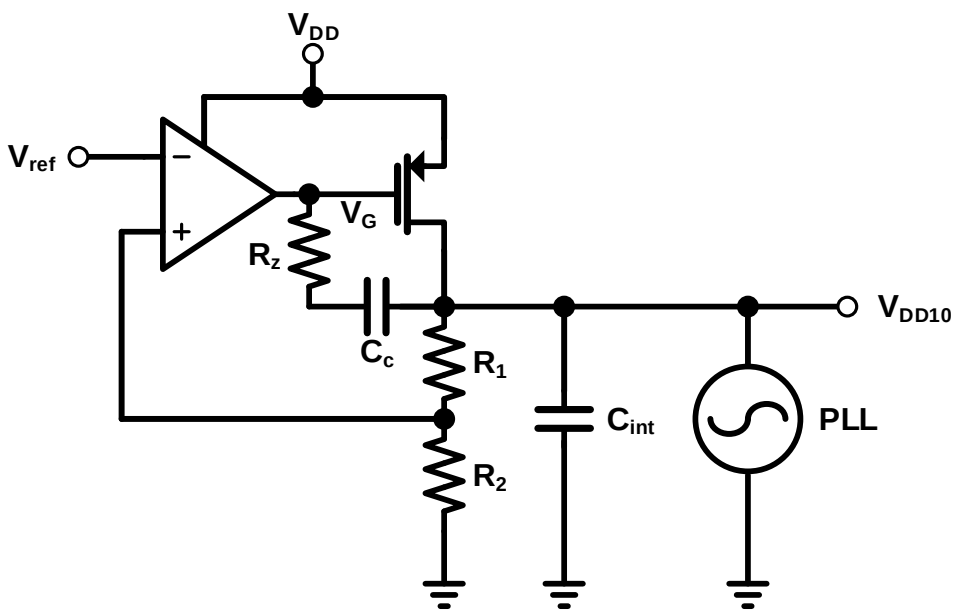

Fig. 4.3 Schematic of the Designed Complementary V_{DD}-LDO for Comparison

Figure 4.4 shows the AC simulations of PSR and loop gain magnitude of the proposed V_{SS}-LDO and designed V_{DD}-LDO at TT process corner for comparison.

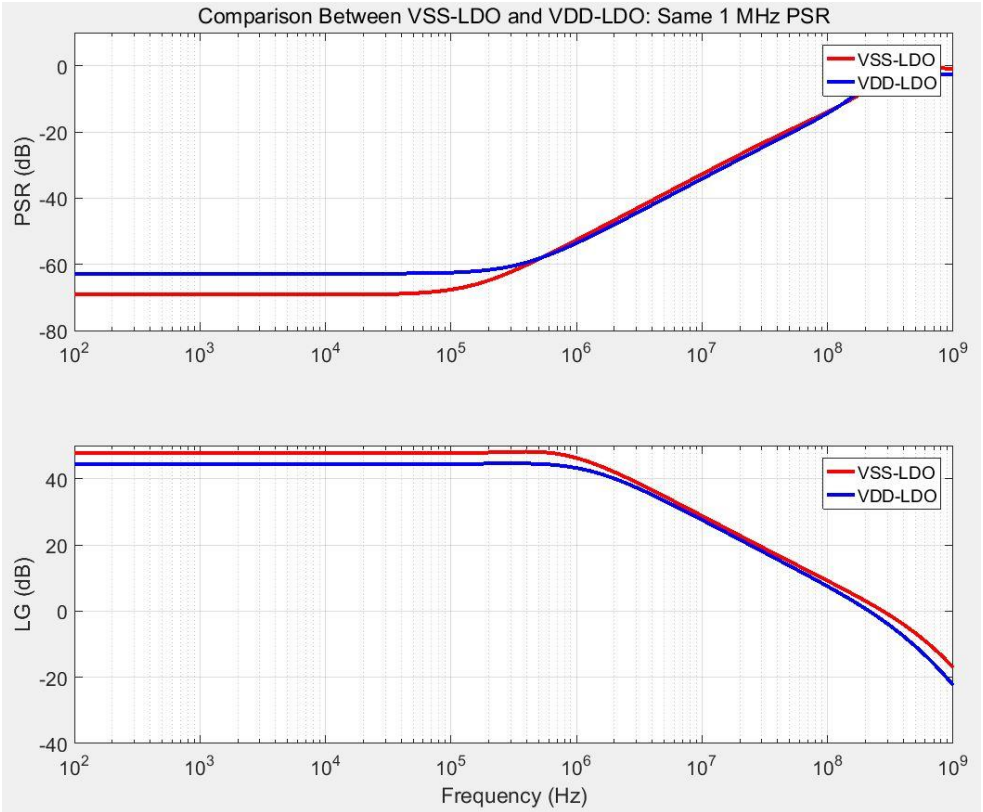

Fig. 4.4 PSR and Loop Gain Magnitude Simulations of the designed V_{SS}-LDO and V_{DD}-LDO with Same PSR at 1 MHz

While matching the DC gains of PSR and loop gain more would have given better comparison (the difference comes from lack of accuracy in matching the DC gain with designing the NMOS input complementary part of the telescopic amplifier), it suffices to only match the PSR at 1 MHz and loop gain unity gain bandwidth because the focus is on comparing the quiescent current. The simulated quiescent current for V_{SS}-LDO is 212 μA, while the simulated quiescent current for V_{DD}-LDO is 657 μA. The expected

power ratio of the two quiescent currents was four but the simulation results show the power ratio to be close to three because while the bias currents of the main amplifiers of the error amplifier is different by factor of four, the biasing circuitry of the amplifier and the feedback resistors dissipate same amount of current. The simulation result demonstrates the initial hypothesis of V_{SS}-LDO having reduced quiescent current without any additional circuitry or technique.

Figure 4.5 shows the simulation comparison result of the proposed V_{SS}-LDO and designed V_{DD}-LDO, which is the same architecture as the previous V_{DD}-LDO but with same quiescent current for 1 MHz PSR comparison. The simulation result shows that the 1 MHz PSR of V_{SS}-LDO is -52.4 dB, while the designed V_{DD}-LDO has 1 MHz PSR of -42.8 dB, which is approximately 10 dB worse than the proposed architecture given the same amount of quiescent current.

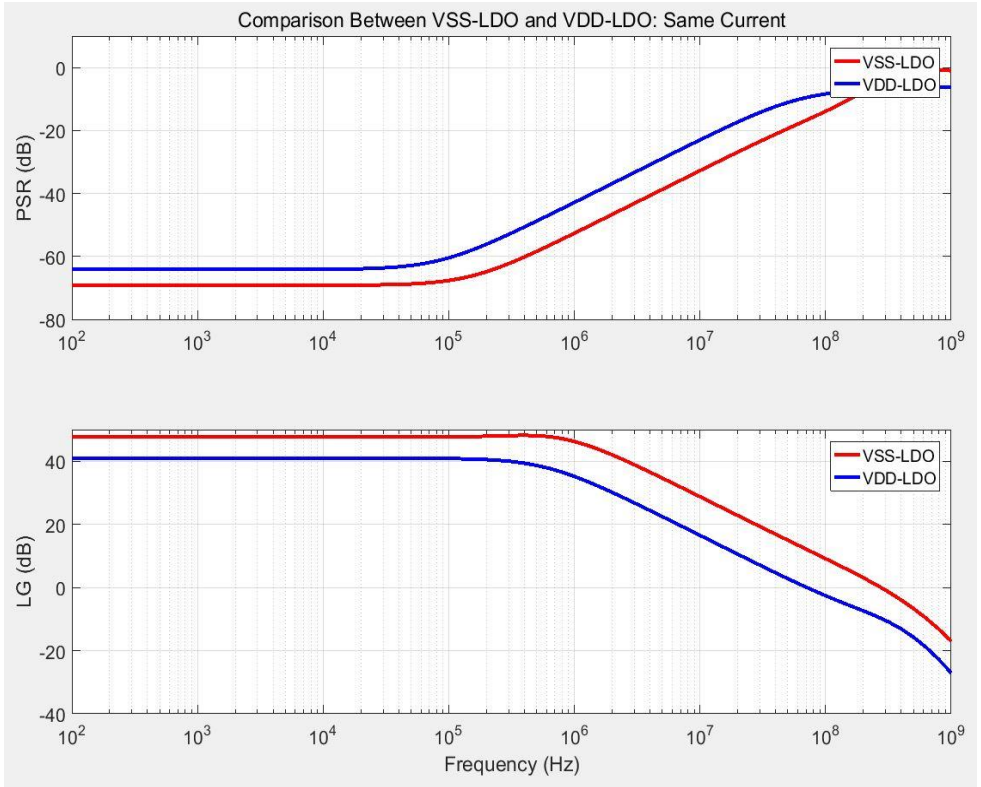

Fig. 4.5 PSR and Loop Gain Magnitude Simulations of the designed V_{SS}-LDO and V_{DD}-LDO with Same I_Q

4.3 Transient Simulations

Transient simulation results are as important as AC simulation results as transient simulation confirms that the proposed architecture operates as expected in time domain. Note that the following transient simulation are different from transient simulation considered in LDO.

A transient response showing the LDO output (VSS02), and control voltage of the VCO (Vctrl) with the ground node (VSS) oscillating at 1 MHz 100 mV amplitude after PLL locks is shown in figure 4.6. The

following results show that even with a large signal, and high frequency input noise source, the LDO outputs a fine 200 mV output and the PLL stays locked.

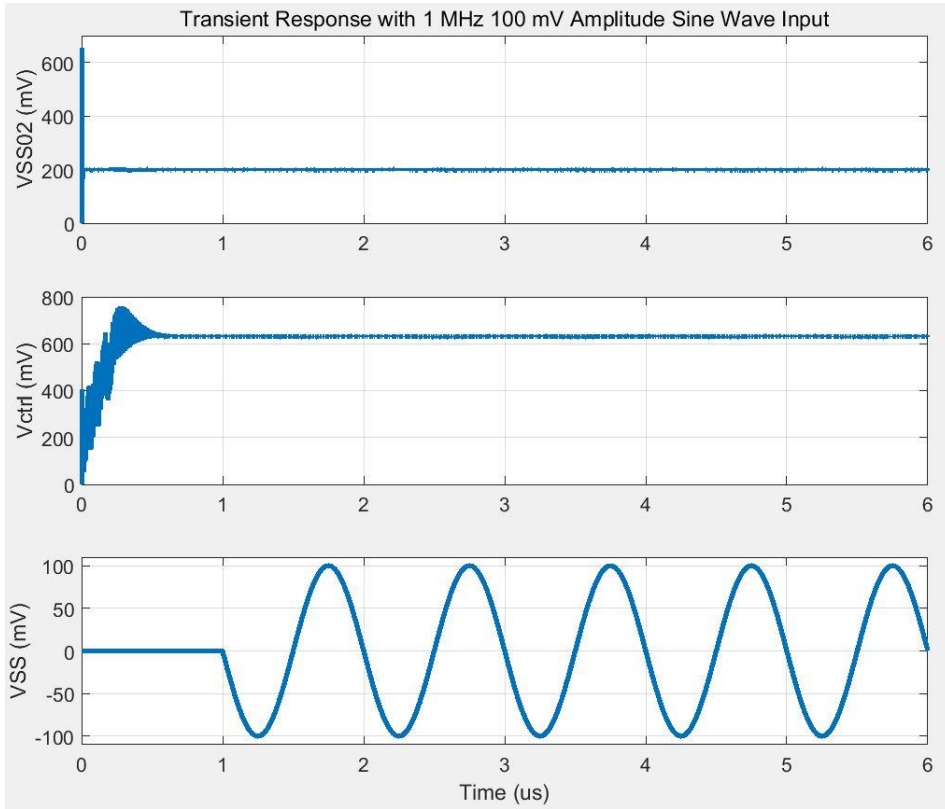

Fig. 4.6 Simulated Line Transient Response with 1 MHz 100 mV Amplitude Sine Wave Input

To demonstrate that the LDO not only regulates 1 MHz sine input, figures 4.7 and 4.8 are shown which shows the same transient simulation results but with input noise frequency being changed to 10 kHz and 100 MHz, respectively. Only one clock cycle after locking has been simulated

for the 10 kHz sine wave input because it is essentially unnecessary to look at a same transient response multiple times (what needs to be seen is that the Vctrl and VSS02 stays locked through the entire cycle of VSS oscillation), and due to simulation time and simulation output file size.

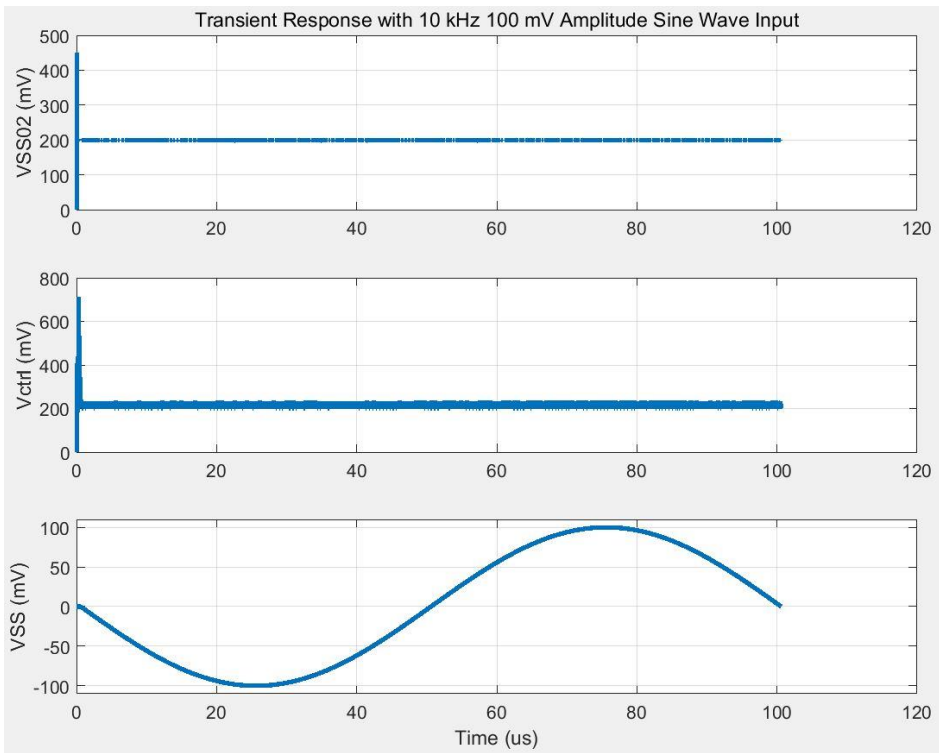

Fig. 4.7 Simulated Line Transient Response with 10 kHz 100 mV Amplitude Sine Wave Input

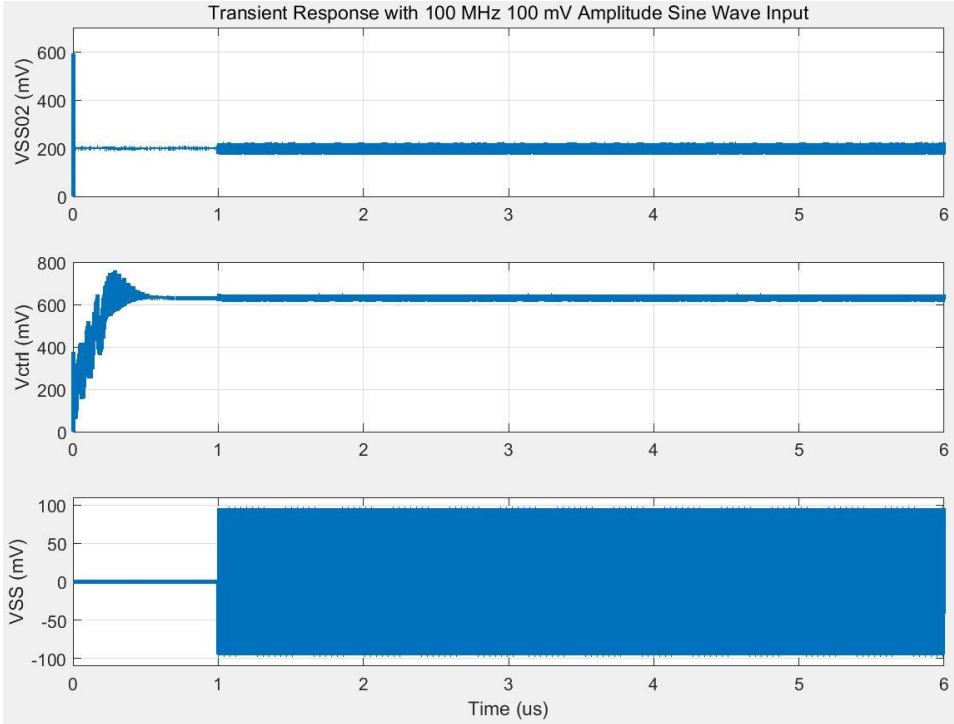

Fig. 4.8 Simulated Line Transient Response with 100 MHz 100 mV Amplitude Sine Wave Input

The following results show that the LDO regulates 10 kHz noise well as opposed to the 100 MHz sees some noise. Such noise comes from the fact that the designed LDO has a PSR of -13.9 dB. Zoomed-in plot of figure 4.8 is shown in figure 4.9, which shows that the noise comes from the 100 MHz noise.

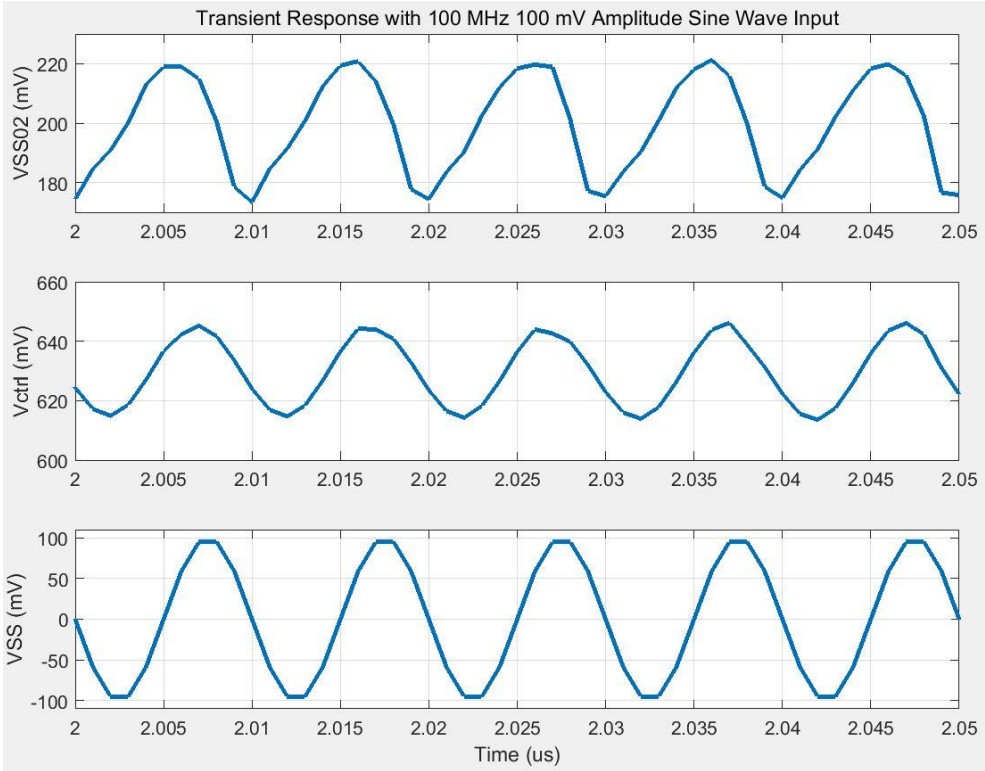

Fig. 4.9 Zoomed in Plot of Fig. 4.8

For completeness of LDO simulation, a load transient simulation is done with a full load step from 2 mA to 30 mA with rise and fall time being 1 ns, which is shown in figure 4.10. The simulation result shows that that LDO output changes by 253 mV but fully (< 0.1 %) settles within 7 ns.

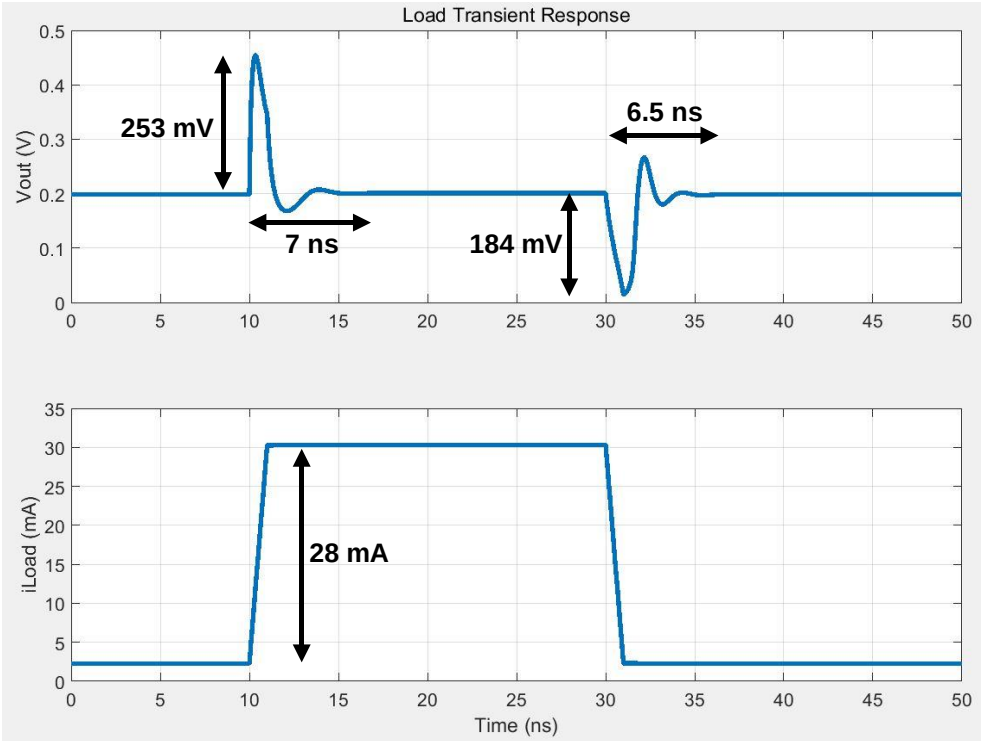

Fig. 4.10 Simulation Result of Load Transient Response

To verify that the system operates properly after the system is turned on, a transient response when the system turns on is shown in figure 4.11. The simulation verifies that the system goes to proper state when the system is powered on.

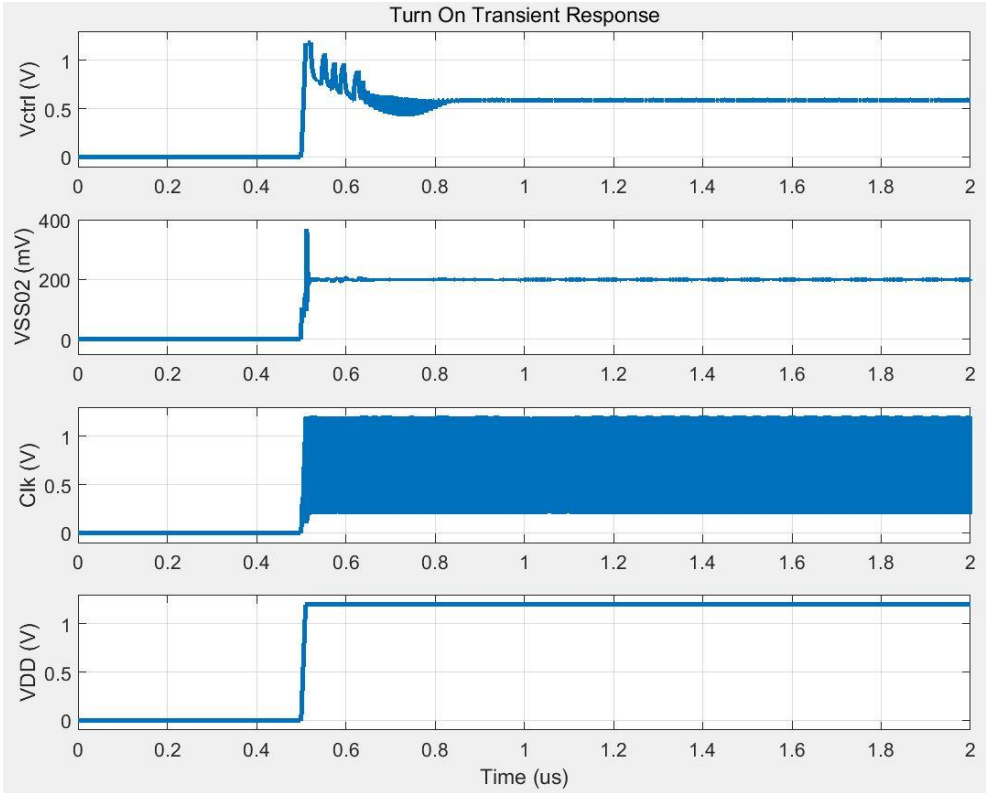

Fig. 4.11 Transient Response of Different Nodes when the System is Turned On

4.4 Performance Summary & Comparison

In conclusion, LDO performance summary of the proposed architecture is shown in Table 1, and the performance comparison with similar supply regulated PLLs is shown in Table 2. Asterisks in Table 1 denotes that the simulation is done with PLL turned off and have test PMOS array tied as load instead. In addition, N/P in Table 2 stands for not provided.

	This Work
Type of Regulator	LDO
Regulated Supply	V_{SS}
Technology	65nm CMOS
Active Area	0.002477 mm^2
V_{in}	-0.1 to 0.1 V
V_{DD} & V_{out}	1.2 & 0.2 V
I_L	2 to 30 mA*
Line Regulation	0.576 mV/V
PSR @ 1 MHz	-50.5 dB
Load Regulation	73 mV/A*
ΔV_{out} @ T_{edge}	253 mV @ 1 ns*
T_R	7 ns*
$C_{on\text{-}chip}$	3.5 pF
$I_{Q\_VSS\_LDO}$ & $I_{Q\_VDD\_LDO}$	212 & 657 µA
Current Efficiency @ I_L = 10 mA	97.9 %

Table 1 Performance Summary of the Designed LDO

	JSSC'06 [13]	JSSC'09 [17]	ISCAS'11 [18]	TCAS-II'13 [19]	VLSI-DAT'15 [20]	Elec. Letters'15 [4]	This Work
Technology	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	65 nm CMOS	65 nm CMOS	0.18 µm CMOS	65 nm CMOS
Supply Voltage	N/P	1.8 V	1.8 V	1 V	1 V (PLL) / 2.5 V (LDO)	1.8 V	1.2 V
Regulated Supply	V_{DD} & V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD} & V_{SS}	V_{SS}
PLL Frequency	0.5-2.5 GHz	0.5-2.5 GHz	0.24-2.4 GHz	1.6 GHz	693-933 MHz	200 MHz	1-3.5 GHz
Jitter @ f_{PLL} w/o supply tone / phase noise	2.36 ps_{rms} @ 2.4 GHz	15 $ps_{p\text{-}p}$ @ 1.5 GHz	1.3 % ± 0.2 % of VCO period	38 ps @ 1.6 GHz	-96dBc/Hz @ 1 MHz	N/P	13.4 $ps_{p\text{-}p}$ @ 3 GHz
Jitter @ f_{in} supply tone	14.8 ps_{rms} @ 1 MHz 50 mV	25 $ps_{p\text{-}p}$ @ 8.85 MHz 200 mV	N/P	98 $ps_{p\text{-}p}$ @ 1 MHz 50 mV	N/P	N/P	33.5 $ps_{p\text{-}p}$ @ 1 MHz 200 mV
Power Dissipation	25 mW	3.9 mW	18 mW	990 µW	11.1 mW (PLL)	9.18 mW	11.3 mW
Active Area	0.15 mm^2	0.093 mm^2	0.18 mm^2	0.2394 mm^2	1.12 mm^2	12.96 mm^2 (total interface)	0.02851 mm^2

Table 2 Performance Comparison with Similar Works

Chapter 5. Conclusion

A ground regulating low dropout regulator has been designed to achieve a high power supply rejection at high frequency with reduced amount of quiescent current. The proposed LDO combines the pros of different types of LDO discussed and eliminates the cons of those LDOs.

To confirm that the reference change can be done without a penalty, a rigorous proof with a noise as a variable showing that the noise from V_{DD} seen from V_{SS} is exactly equal to the noise from V_{SS} seen from V_{DD} once the architecture is flipped upside-down has been done.

The proposed LDO is intended to be fabricated in 65 nm CMOS technology and dissipates 212 μA of quiescent current. Although designed LDO has large current consumption compared to other reported LDOs, it only dissipates one-third of the complementary V_{DD}-LDO without using any additional technique, and without compensating any other performance parameters. The LDO achieves -50.5 dB of PSR at 1 MHz which proves that the proposed architecture can be used to regulate noise from switching regulators and/or DC-DC converters with reduced amount of quiescent current without compensating any performance metrics.

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초 록

시장에서 리튬 이온 배터리를 사용하는 휴대전자기기와 시스템온칩 (SoC) 기기의 높은 수요를 맞춰 스위칭 주파수에 있는 DC-DC 컨버터의 출력 리플을 잡아주는 높은 전원 공급 제거 (PSR)를 가진 low dropout regulator (LDO)의 설계는 중요하다.

이에 따라, 이 논문은 그라운드 제어 방법을 이용해 높은 unity gain bandwidth를 가진 low dropout regulator를 소개한다. 제안된 low dropout regulator는 고 주파수 대역 (~ 1 MHz)에서도 높은 전원 공급 제거를 갖기 위해 높은 loop gain unity gain bandwidth를 갖는 것을 목표로 한다. 넓은 대역폭은 LDO에서 높은 정동작 전류를 암시하기에 전류 소모를 줄이기 위해 기준을 바꾼 그라운드 제어 방법이 적용 되었다.

제안된 low dropout regulator는 65nm CMOS 공정에서 제작되길 의도하고 1 MHz에서 -50.5 dB의 전원 공급 제거를 달성하고 비슷한 LDO 성과를 가지게 설계된 상호 보완적인 일반 LDO에 비해 3배 낮은 숫자인 212 μA의 정동작 전류를 소모한다.

주요어 : Low Dropout Regulator (LDO), 휴대전자기기, 시스템온칩 (SoC), 그라운드 제어, 전원 공급 제거 (PSR), 정동작 전류

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