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공학박사 학위논문

**Multi-color Photodetectors via Wafer
Bonding and Epitaxial Lift-Off of III-V
Compound Semiconductors**

3-5족 화합물 반도체의 웨이퍼 접합과 에피택셜
리프트 오프를 통한 다중 파장 광 검출기

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Abstract

Multi-color Photodetectors via Wafer Bonding and Epitaxial Lift-Off of III-V Compound Semiconductors

Dae-Myeong Geum

Department of Materials and Science and Engineering

College of Engineering

Seoul National University

Group III-V compound semiconductors, having a band gap from ultraviolet to infrared regions, have been widely used as imagers to visualize a single band. With the recent arrival of the Internet-of-things (IOTs) era, new applications such as time of flight (TOF) sensors, normalized difference vegetation index (NVDI) and night vision systems have gained interest. Therefore, the importance of multicolor photodetectors is raised. To implement multicolor photodetectors, an epitaxy method has been commonly used with III-V compound semiconductors. For example, quantum wells, quantum dots and type-II based structures and metamorphically grown bulk heteroepitaxial structures have been employed. Although an epitaxy method seems to be quite simple, there are several problems including limitation of

material choice due to the discrepancy of lattice constants between thin films and substrates, performance degradation originated from internal defects and complexity of growth. Therefore, to avoid these disadvantages of the epitaxy method, a heterogeneous integration method has been an alternative because the integration of devices grown on different substrates is possible. Thus, it has been considered to be a promising method to combine photodetectors with simple bulk structures. However, although there is a significant advantage to the heterogeneous integration method, current multicolor photodetectors have exhibited limitations regarding pixel density and vertical misalignment due to problems related to conventional integration methods. Therefore, in this thesis, the heterogeneous integration of III-V compound semiconductors was investigated for fabricating multicolor photodetectors with high pixel density and highly accurate alignment.

Firstly, a research on heterogeneous integration of GaAs based thin film devices with other substrates was carried out. We studied wafer bonding and epitaxial lift off process which have advantages including large area transferability, cost-effectiveness and high quality of layers compared with wafer splitting and transfer printing methods. To fabricate multicolor photodetectors on single substrates, a stable rigid-to-rigid heterogeneous integration method is highly required. However, there have only been few reports regarding rigid-to-rigid transfer by using epitaxial lift off due to the difficulty involving byproducts and gas bubbles generated during the wet etching of the sacrificial layer for wafer separation. This has been a hindrance compared with thin film on flexible substrates which can accelerate wafer separation by using strain and external equipment. In order to overcome this problem, high throughput epitaxial lift off process was proposed through a

pre-patterning process and surface hydrophilization. The pre-patterning process can maximize the etching area of the AIAs sacrificial layer and rapidly remove bubbles. In addition, acetone, which is a hydrophilic solution, was mixed with hydrofluoric acid in order to reduce the surface contact angle and viscosity. It resulted in an effective penetration of the etching solution and the suppression of byproducts. Consequently, it was possible to transfer GaAs thin films on rigid substrates within 30 minutes for a 2 inch wafer which has been the fastest compared with previous reports. Also, using this template, electronic and optoelectronic devices were successfully fabricated and operated.

Secondly, we have studied to overcome restrictions of bulk photodetector for InSb binary material including the detection limit and cryogenic operation. To extend the detection limit of bulk InSb toward the LWIR range, the ideal candidate of III-V bulk materials is indium arsenide antimonide (InAsSb) material due to its corresponding band gaps ranging from SWIR to LWIR. By combining bulk InAsSb with other bulk materials with previously developed integration methods, we could ultimately fabricate a multicolor photodetector ranging from ultraviolet to LWIR with only bulk structures. Thus, in order to verify the viability of this material, a p-i-n structure based photodetector with an $\text{InAs}_{0.81}\text{Sb}_{0.19}$ absorption layer was grown on a GaAs substrate. To enhance an ability to be operated at a high temperature, an optimum InAsSb barrier layer was designed by technology computer aided design (TCAD). Also, InAsSb/InAsSb heterojunction photodetector was grown by molecular beam epitaxy (MBE). As a result, we have demonstrated the first room temperature operation of heterojunction photodetectors in MWIR range among InAsSb photodetectors with similar

Sb compositions. Additionally, it has a higher responsivity of 15 mA/W compared with commercialized photodetectors. This MWIR photodetector with room temperature operability could help the reduction of the volume for final detector systems due to the elimination of Dewar used in InSb photodetectors. In other words, from this experiments, it is suggested that there is a strong potential of InAsSb bulk structures for detecting LWIR.

Finally, the study on the monolithic integration was carried out to verify the feasibility of multicolor photodetectors by integration of bulk structures. Among procured photodetectors with detection ranging from visible to MWIR at room temperature operation, visible GaAs and near-infrared InGaAs photodetector were used for establishing the optimized fabrication process due to material's process maturity. By using previously developed high throughput ELO process, GaAs photodetectors were transferred onto InGaAs photodetectors to form visible/near-infrared multicolor photodetectors. It was found that top GaAs PD and bottom InGaAs PD were vertically well aligned without an off-axis tilt in x-ray diffraction (XRD) measurement. Also, similar dark currents of each photodetector were observed compared with reference photodetectors. Finally, with incidence of laser illumination, photoresponses were clearly revealed in visible band and near-infrared band of material characteristics, respectively. These results suggested high throughput ELO process enables the monolithic integration of bulk based multicolor photodetectors on a single substrate with high pixel density and nearly perfect vertical alignment. In the future, depending on the target applications, photodetectors with desired wavelengths could be simply grown as bulk structures and fabricated for multicolor imagers.

Key Words:

Heterogeneous integration, III-V compound semiconductors, Epitaxial lift off, Photodetectors, Multicolor, imager,

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Contents

List of Figures	i
Chapter.1 Introduction	1
1.1 Photodetectors based on III-V compound semiconductors	1
1.2 Imaging applications	4
1.2.1. Single color imaing	4
1.2.2. Multicolor imaing	4
1.2.3. Development trend of photodetectors	5
1.3 Approches for forming multicolor photodectors	9
1.3.1. Epitaxy	9
1.3.2. Heterogeneous integration	17
1.3.3. Summary of each method	21
1.4 Overview of heterogeneous integration technology	23
1.4.1. Introduction	23
1.4.2. Direct bonding	24
1.4.3. Cold-weld bonding	26
1.4.4. Eutectic bonding	26
1.4.5. Adhesive bonding	28
1.4.7. Wafer splitting	31
1.4.8. Epitaxial lift off (ELO)	33
1.4.9. Benchmark of differencet heterogeneous intergration methods	35
1.5 Thesis overview	37
1.6 Bibliography	40
Chapter. 2 Method for heterogeneous integration of III-V compound semiconductors on other substrates	45
2.1 Introduction	45
2.1.1 The origin of low throughput in conventional ELO	46

2.1.2	Previous works for enhancement of ELO throughput ...	48
2.1.3	Approach: high-throughput ELO process	53
2.1.4	Experimental procedure	55
2.2	Results and discussion	57
2.3	Summary	65
2.4	Bibliography	66
Chapter. 3	Verification of thin film devices by using a high throughput heterogeneous integration method	70
3.1	Introduction	70
3.2	Growth of device structures and heterogeneous integration 72	
3.2.1.	Device structures	72
3.2.2.	Wafer bonding and ELO	74
3.3	Y₂O₃ bonded HEMTs on Si substrate	75
3.3.1	Fabrication process	75
3.3.2.	Material characterization of HEMTs on Si	76
3.3.3.	Electrical characterization of HEMTs on Si	80
3.3.4.	Investigation of wafer reusability by using HEMT structure	83
3.4	Pt/Au bonded optoelectronic devices	86
3.4.1.	Fabrication process of solar cells and HPTs on Si	86
3.4.2.	Evaluation of Pt/Au metal bonding	88
3.4.3.	Characterization of solar cells and HPTs	91
3.5	Estimation of production cost via recycling III-V wafers	95
3.6	Summary	101
3.7	Bibliography	102
Chapter. 4	Design and characterization of III-V based photodetectors	105
4.1	Introduction	105

4.1.1.	The potential of Indium arsenide antimonide (InAsSb) ..	105
4.1.2.	Challenges of InAsSb p-i-n PDs for compact detector systems ..	109
4.2	Barrier layer design and material characterization for growing HJPDs.....	112
4.2.1.	Simulation of an optimum barrier layer for InAs _{0.8} Sb _{0.2} ..	112
4.2.2.	Growth of a high quality InAsSb layer with an AlGaSb buffer layer grown on GaAs substrates ..	114
4.2.3.	Ohmic contact formation with metal species.....	119
4.2.4.	Growth and fabrication of InAsSb based HJPDs	125
4.3	Analysis of electrical and optical characteristics for fabricated PDs	128
4.4	Summary.....	137
4.5	Bibliography	138
Chapter. 5 Monolithic integration of visible/near-infrared photodetectors 144		
5.1	Introduction	144
5.2	Fabrication process and material characterization of multicolor PD.....	147
5.3	Analysis of the electrical and optical characteristics of the fabricated multicolor PDs	153
5.4	Summary.....	162
5.5	Bibliography	163
Chapter. 6 Conclusions		
166		
국문초록	169

List of Figures

Figure 1 band gap energy and wavelength versus lattice constant.....	2
Figure 2 wavelength coverages of various materials such as group-IV, group III-V and group II-VI [4].....	3
Figure 3 imaging applications with different wavelengths, a) ultraviolet, b) infrared, c) near-infrared, short wavelength infrared, and long wavelength infrared region.....	7
Figure 4 applications by using multicolor detection, a) time-of-flight (TOF) sensors, b) nomalized difference vegetation index (NDVI), c) woldview-3 by DigitalGlobe.....	8
Figure 5 history of the development of infrared detectors and systems.....	9
Figure 6 schematic of photon absorption mechanicsm for III-V quantum wells and quantum dots.....	12
Figure 7 a) structure of a two-color stacked QWIP, b) simultaneous images with optical filter and the soldering iron from 256 x 256 MWIR/LWIR QWIP FPA's [14].....	13
Figure 8 schematic of band alignment in InAs, GaSb and AlSb material systems with similar lattce constants. There are three types of band alignmenet of type-I (nested), type-II (staggered and broken) [17].....	14
Figure 9 schematic of triple bands (SWIR-MWIR-LWIR) photodiode structure in type-II superlattices [15].....	15
Figure 10 a) schematic of nBnBN layer structure consisting of InAsSb and GaSb grown on GaAs substrate with interfacial misfit array (IMF) technique, b) simulated band diagram of above structure at 300K (left)	

and fabricated device with three contacts for testing each absorption region [16].	16
Figure 11 a) schematic of concept for multispectral detection system consisting of GaAs and InGaAs absorption materials on Si substrate, b) Optical image of fabricated thin-film MSM detectors on contact pads [21].	18
Figure 12 bonding interface of the sample with good and bad bonding states. Void existing at the interface in the bottom SEM image [22].	19
Figure 13 a) conceptual image of Si pixels transferred onto InP substrate for 4 colors detection, b) optical image of unit cell of 4 colors absorption, c) 4 x 4 array of Si//InGaAs detector unit cells [23].	20
Figure 14 photograph of commercialized Si//InAsSb two-color detector [24].	21
Figure 15 SEM image of direct bonded GaAs//Si with surface activation bonding at room temperature (top), high resolution TEM image of GaAs//Si bonding interface with an interfacial layer (bottom) [26].	25
Figure 16 Schematic of cold-weld bonding mechanism [28].	27
Figure 17 schematic of transfer printing process by using elastomeric stamp with variation of peel-off speed [30].	30
Figure 18 fabrication process flow for integrating InAs on Si substrates by transfer printing method [31].	30
Figure 19 schematic of wafer splitting method for fabricating silicon-on-insulator (SOI) called as SMARTCUT [32].	32
Figure 20 a) process flow of solar cells on flexible substrates by using cold-weld bonding and epitaxial lift off, b) photograph of transferred GaAs	

thin film on PET film and parent GaAs substrate (donor wafer) [36]. ...	34
Figure 21 schematic of objective of this thesis	39
Figure 22 problems of conventional ELO process.....	47
Figure 23 diffusion and reaction model for ELO process	48
Figure 24 WI-ELO [11, 12].	50
Figure 25 advanced WI-ELO [12].	50
Figure 26 internal stress induced ELO [13].....	51
Figure 27 novel approach of high throughput ELO process.....	53
Figure 28 contact angles with various HF: hydrophilic substances	54
Figure 29 experimental procedures (not scalable)	56
Figure 30 a) Etching solution dependence of the ELO time as a parameter of the pre-patterning process. With the pre-patterning and the insertion of the etching acceleration solutions, the ELO time was significantly reduced, b) the photograph and SEM image for GaAs on Si substrate, c) The effect of a wafer size for the ELO process; a negligible dependence was observed, d) etching solution dependence of the residue thickness, e) kinematic viscosity of hydrophilic substances, f) the trade off relation ship of different properties.	60
Figure 31 ELO time in terms of dimension variation (top), SEM images of formed GaAs on Si (bottom).	63
Figure 32 ELO time in terms of spacing variation (top), SEM images of formed GaAs on Si (bottom).	64
Figure 33 the epitaxial structures of the III-V layers used in this study.	74
Figure 34 process flow of the wafer bonding and ELO process. a) process details of the wafer bonding and ELO with Y_2O_3 as a bonding material, b)	

process details of the wafer bonding and ELO with Pt/Au as a bonding material.....	75
Figure 35 GaAs HEMT on Si. Process details for the fabrication of the GaAs HEMTs on Si.....	76
Figure 36 GaAs-OI on a Si substrate via the wafer bonding and ELO processes. a) IR image of a GaAs-OI on Si sample after the wafer bonding. Patterned GaAs arrays were securely bonded onto the Si substrate, b) typical SEM image of a GaAs-OI on Si sample. GaAs pattern arrays are formed on the Si substrate, c) Cross-sectional TEM image of a GaAs-OI on Si sample, showing uniform GaAs HEMT layers on Si. The GaAs HEMT is composed of a GaAs contact layer, an Al _{0.3} Ga _{0.7} As barrier layer, and a GaAs channel layer, d) EDAX profiles for Ga (blue), As (pink), Y (red), and Si (Green) evaluated along the fabricated substrate, e) TED pattern of GaAs region, f) TED pattern of Si region.....	78
Figure 37 a) PL spectra and b) Raman spectra for comparison of transferred GaAs thin film quality.....	79
Figure 38 Performance of the GaAs-OI HEMTs and wafer re-usability after the ELO process. a) schematic of fabricated GaAs-OI HEMTs on Si substrate, b) optical image of GaAs-OI HEMTs with source/drain formation, c) and d) measured transfer characteristics of a reference HEMT and GaAs-OI HEMT with a L_G of 2 μm . The device exhibits a quite low S.S. of 83 mV per decade, which is close to the theoretical limit of 60 mV per decade at room temperature, e) Output characteristics of the same device shown in a, showing clear current saturation, f) I_D - V_G	

curves for different V_B ; the electrical characteristics of the GaAs-OI HEMT can be controlled by V_B after the device fabrication.	82
Figure 39 AFM image for wafer reusability with process steps.	84
Figure 40 a) Raman spectra for as-grwon, GaAs-OI HEMTs, donor wafer and regrown HEMT structure, b) comparison of Hall measurement results for HEMT structure using fresh and re-used substrate.	85
Figure 41 GaAs solar cell on Si. Process details for the fabrication of the GaAs solar cells on Si.	86
Figure 42 InGaP/GaAs HPT on Si. Process details for the fabrication of the InGaP/GaAs HPT on Si.	87
Figure 43 photograph and SEM image of 2 inch GaAs thin film transferred on 4 inch Si substrate with Pt/Au metal bonding layer.	88
Figure 44 a) AFM image of Pt/Au surface deposited on GaAs solar cells, b) AFM image of GaAs solar cell on Si substrate after ELO process, c) TEM image of GaAs/Pt/Au/Au/Pt/Si structure with an interfacial layer.	90
Figure 45 GaAs solar cells and InGaP/GaAs HPTs on Si, a) $J-V$ characteristics of the GaAs solar cell on Si (blue) and GaAs (red, control) under AM 1.5 G, 1-sun measurement condition. The inset is a top view SEM image showing the fabricated GaAs solar cell on Si, b) EQE spectra of the GaAs solar cell on Si (blue) and GaAs (red), c) I_{Cdark} and I_{Cph} characteristics of the InGaP/GaAs HPT on Si as a function of VCE, d) Incident optical power dependence of the G_{opt} of the same device shown in c.	94
Figure 46 Estimation of the production cost III-V/Si wafer, a) Production cost	

as a function of N, b) Production cost per one wafer as a function of N.	99
Figure 47 band gap and wavelength properties of III-V compound semiconductors as a function of lattice constants [4]	106
Figure 48 calculated $\text{InAs}_x\text{Sb}_{1-x}$ wavelengths as a function of temperatures with Vegard's law	108
Figure 49 Approach of heterojunction photodetectors with barrier layer based on p-i-n structure which shows parts of total dark current such as diffusion current, generation-recombination current, trap-assisted tunneling current and band-to-band current	110
Figure 50 a) band alignment of quantum well consisting of $\text{InAs}_{0.8}\text{Sb}_{0.2}$ with AlSb barrier layer, b) simulated band structure of $\text{InAs}_{0.8}\text{Sb}_{0.2}$ /AlSb quantum well [16-18]	111
Figure 51 a) Energy band diagram of HJPDs with different barrier layers under zero bias at room temperature, b) Table of parameters for simulating the band diagram	113
Figure 52 a) schematic of fully relaxed structure grown on GaAs substrate, b)HRXRD measurement results with various compositions of InAsSb, c) results of As compositions in terms of As to Sb ratios.	116
Figure 53 a) threading dislocation density versus buffer layer thickness calculated from the Ayers model, b) results of the Hall measurement in this work and in previous papers at room temperature as a function of the Sb composition of the $\text{InAs}_{1-x}\text{Sb}_x$	118
Figure 54 Schematic of $\text{InAs}_{0.8}\text{Sb}_{0.2}$ with AlGaSb buffer layer grown on GaAs substrate	120
Figure 55 specific contact resistivities as a function of metal species	

with/without native oxide removal process for intrinsic InAsSb.	122
Figure 56 specific contact resistivities as a function of metal species with/without native oxide removal process for n-type InAsSb.	123
Figure 57 specific contact resistivities as a function of metal species with/without native oxide removal process for p-type InAsSb.	124
Figure 58 (a) Schematic structure of HJPD with $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ grown on GaAs (b) measured θ - 2θ results of MBE-grown reference p-i-n PD and HJPD compared to EPITAXY simulation (c) Schematic of finally fabricated HJPD and SEM image of the cleaved cross-section.	127
Figure 59 a) current density (J)-voltage (V) curves for p-i-n PD and HJPD at room temperature and 100K, b) temperature dependent J-V curves for HJPD, c) temperature dependent dark current density-inverse temperature extracted at -10 mV, d) activation energy behavior for HJPD calculated by Eq.(1) in a temperature range from 220K to room temperature.	130
Figure 60 Photocurrent response measurements in FTIR system with different temperatures for a) p-i-n PD, b) HJPD, c) simulation of optical intensity distribution as a function of wavelength for HJPD structure, d) temperature dependence of cutoff wavelength for HJPD and its fit by using Varshni expression of Eq. (2).	133
Figure 61 a) responsivity measurement of p-i-n PD and HJPD with 500K blackbody radiation, b) Resistance-area product of HJPD depending on the voltages at 300K and 100K.	134
Figure 62 schematic of multicolor photodetectors concept and advantages compared with other methods	146

Figure 63 wavelength ranges of III-V materials based photodetectors and candidates of our photodetectors for the heterogeneous integration. ...	147
Figure 64 schematic of process flow for GaAs//InGaAs multicolor photodetectors.....	149
Figure 65 a) optical image of multicolor photodetectors with three terminals (top view), b) θ - 2θ measurements for reference GaAs, InGaAs photodetectors and multicolor photodetectors.....	151
Figure 66 a) cross-sectional TEM image withlow magnitude for multicolor photodetectors, b) expanded TEM image at the Y ₂ O ₃ bonding interface, c) EDAX profile in terms of each atom from A to A', d), e) and f) fast Foirier transform (FFT) patterns of InP, Y ₂ O ₃ and GaAs, respectively.	153
Figure 67 a) schematic of final structure for electrical measurements of multicolor photodetectors, b) GaAs and InGaAs photodetector current-voltage for multicolor photodetectors, c) and d) comparison of dark current between reference and multicolor photodetectors of GaAs and InGaAs	155
Figure 68 photoresponse and calculated responsivity of GaAs top photodetector as a function of laser wavelenghts. Inset figure shows the optical measurement system by using lensed fiber.	157
Figure 69 photoresponse and calculated responsivity of InGaAs bottom photodetector as a function of laser wavelenghts.	159
Figure 70 simulation of optical intensity distribution of bottom InGaAs photodetectors in full structure of multicolor photodetector.	160

Chapter.1 Introduction

1.1 Photodetectors based on III-V compound semiconductors

III-V compound semiconductors have been widely used for many applications including transistors, light-emitting diodes (LEDs), Light Amplification by the Stimulated Emission of Radiation (laser) and photodetectors (PDs) thanks to their own properties such as direct band gap, high mobility and tunability of band gaps [1]. These compound semiconductors can correspond to the various band gaps ranging from 0.17 eV of indium antimonide (InSb) to 6.2 eV of aluminum nitride (AlN) with binary structures as shown in Figure. 1 [2]. With changing compositions, band gap properties of ternary and quaternary alloy have been changed regarding to straight and dashed line. Generally, while lattice constant normally follows a linear relationship with composition, the unusual energy band gap change is shown due to band gap bowing caused by alloy disorder [3]. By using the combination of III/V groups in the alloy, the band gap can be tuned to satisfy the requirements for above electronic and optoelectronic devices.

Among many applications based on these properties, photodetectors are one of useful devices based on III-V compound semiconductors. Photodetectors have been designed for detecting the light (or photon) regarding compound semiconductor's own energy band gaps (or wavelengths) as shown Figure.2 [4]. In typical P-N diode, its principle is based on the interband absorption of the photon in the depletion layer of a P-N diode (or

intrinsic layer of a P-I-N diode) and subsequent separation of electrons and holes by the electric field [1]. Besides, there are various types of detectors such as photoconductors, avalanche photodiodes, and metal-semiconductor-metal (MSM) photodetectors [1].

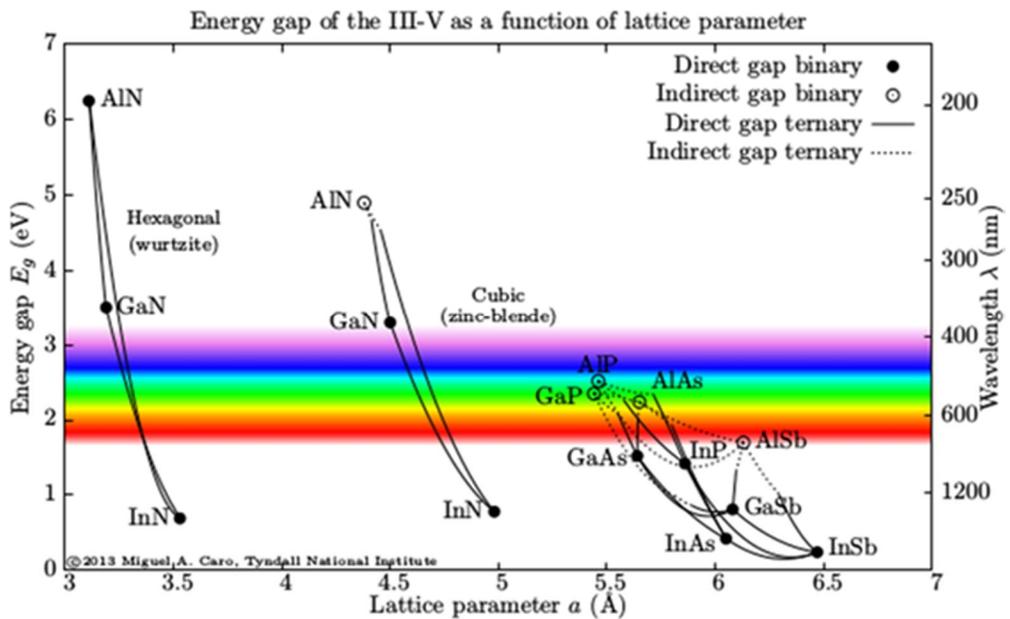
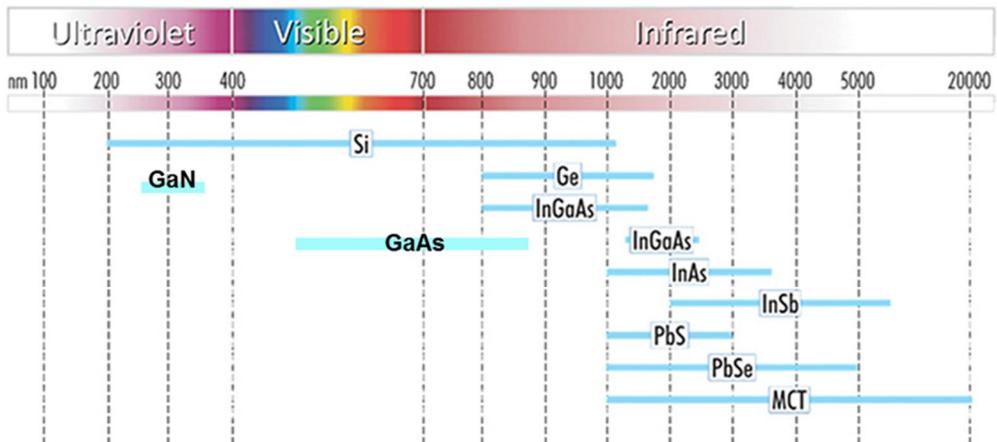


Figure 1 band gap energy and wavelength versus lattice constant.



III-V compound semiconductors based photodetectors

→ detecting from **ultra-violet (UV)** to **infrared (IR)** wavelength

Figure 2 wavelength coverages of various materials such as group-IV, group III-V and group II-VI [4].

1.2 Imaging applications

1.2.1. Single color imaging

The ability to detect photons with various energies has been extensively utilized for imaging applications. As shown Figure. 3, the cameras using the ultraviolet (UV), visible, and infrared (IR) band have been main application. By using UV band, a distribution of damaged skin from sunlight can be viewed whereas it cannot be seen in visible band as illustrated in Figure. 3a [5]. As seen in Fig. 3b [6], IR imaging is possible to unveil invisible regions in human being's eyes because the emitted thermal energy of object with specific temperatures is relevant to IR band. For example, human being with 300K temperature emits blackbody radiation of long wavelength infrared (LWIR) ranging from 8 μm to 14 μm while flame of jet engine has a radiation peak of mid infrared wavelength infrared (MWIR) region. In addition, through a combination of various bands such as visible, near-infrared (NIR), short wavelength infrared (SWIR) and LWIR, different images could be obtained in the same scene because of difference of foot-prints for gas species and emitted energies as shown in Fig. 3c [7]. Imaging applications with a single band have been mainly used as above introduced so far.

1.2.2. Multicolor imaging

In recent years, many techniques for simultaneously detecting and imaging multiple bands over a single band have been required. Multispectral detection

(or multicolor detection) of visible and infrared (IR) wavelengths has been widely attracted for emerging autonomous car in internet-of-things (IoTs) era. It demands various sensors that can visualize the objects in the light and night vision. Additionally, visible/near-infrared (IR) wavelengths detection can offer many new applications such as time-of-flight (TOF) sensors for 3-dimensional imaging, normalized vegetation differential index (NVDI) as shown in Figure. 4a, 4b [8, 9]. Fig. 4c shows the fire scene which cannot be seen by cloud and smoke [10]. At same time, by using SWIR band, thermal imaging could be acquired. With signal processing for two images, it is possible to confirm the ignition point in the mountain. Thus, according to emerging IoT era and novel applications with multicolor detection, integrating the multi-functionality into single pixel area, compact and low power consuming multicolor photodetectors (PDs) are highly required.

1.2.3. Development trend of photodetectors

Among the several candidate materials to acquire the multiple wavelengths, group IV, III-V semiconductors have been representative. While group IV materials such as Silicon (Si) and Germanium (Ge) are suitable for cost-effective and large area production, they can only tailor the wavelength to near infrared (IR) region due to their band gap property. On the other hand, III-V compound semiconductors could extend the wavelength from ultraviolet (UV) to infrared (IR) region. Furthermore, high mobility and direct band gap property of III-V materials are possible to make the photodetector with high speed and high quantum efficiency.

Figure 5 illustrates the trend in photodetector developments of III-V and

II-VI compound semiconductor for past years [11]. Although this figure indicates the development of infrared sensors, the development trend can be applicable for all wavelength ranges. In the late 1960s, first generation of linear photoconductor arrays were emerged. This scanning system does not multiplex the signal in the focal plane. In second generation, two-dimensional (2D) arrays were implemented thanks to the development of charge-coupled device (CCD) which leads the all-solid-state-electronically scanned 2D detector array. After formation of 2D array of detector, large number of pixels and two-color functionality were developed in third generation of photodetectors. Additionally, recent efforts have been extended to three or four color photodetector array on a same substrate with material development and device design. This development from linear array of single color photodetectors to multicolor array of photodetectors is coincided with the increase of a demand in IoT era.

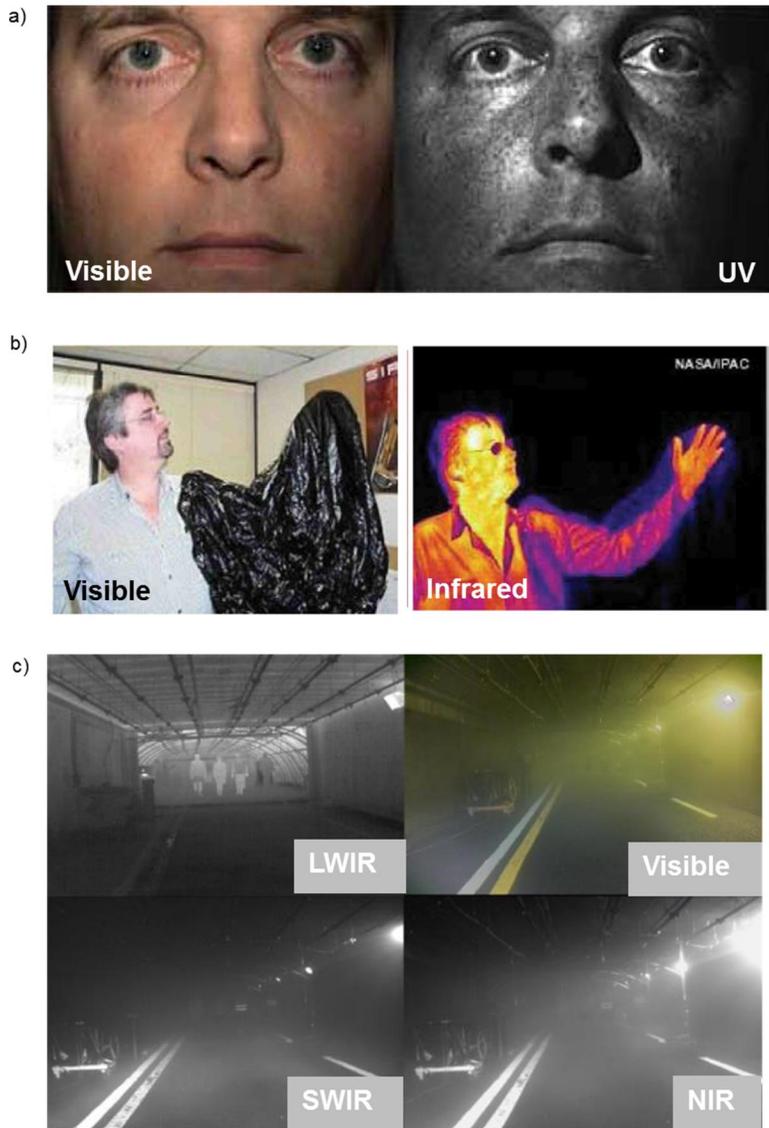


Figure 3 imaging applications with different wavelengths, a) ultraviolet, b) infrared, c) near-infrared, short wavelength infrared, and long wavelength infrared region

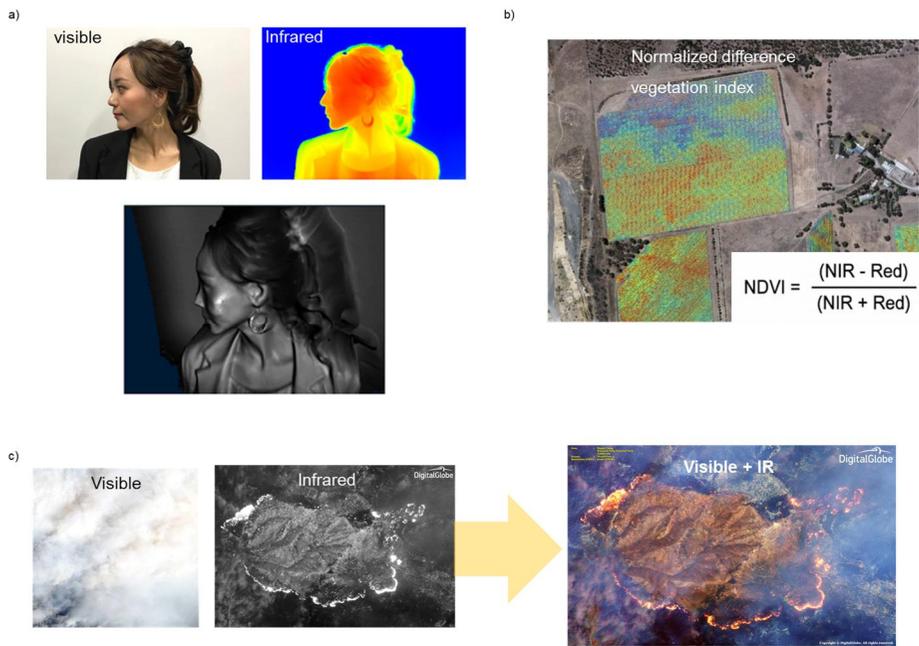


Figure 4 applications by using multicolor detection, a) time-of-flight (TOF) sensors, b) nomalized difference vegetation index (NDVI), c) woldview-3 by DigitalGlobe

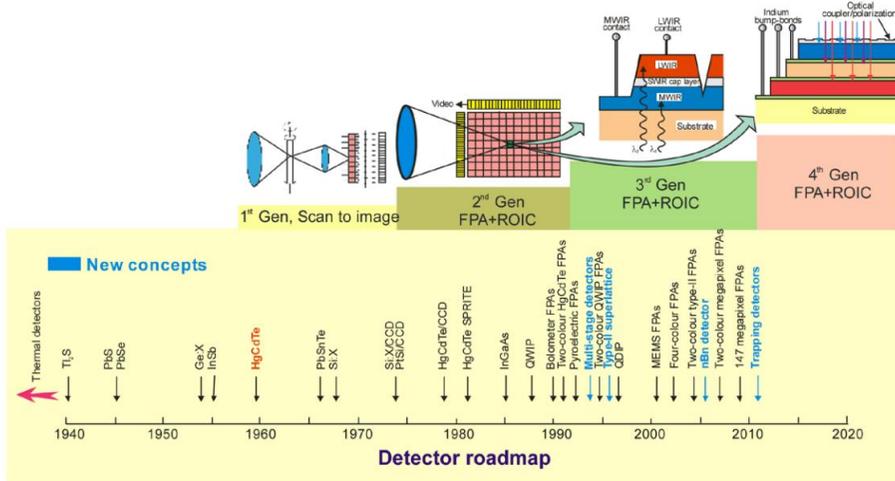


Figure 5 history of the development of infrared detectors and systems

1.3 Approches for forming multicolor photodectors

1.3.1. Epitaxy

Epitaxy means the growth of a single crystalline film on a crystalline substrate [12]. The substrate serves as a seed and provides crystal structure information for growing films during epitaxial growth. On the other hand, one major limitation of substrates is lattice matching between the epitaxial layer and substrates. To solve this problem, pseudomorphic growth and metamorphic growth technologies have been developed [13]. Pseudomorphic growth demonstrates the growth of strained crystalline epitaxial layer when a film thickness would be below critical thickness. Metamorphic growth describes the growth of thicker layer than critical thickness with relaxation

process beyond pseudomorphic growth range. From these techniques for epitaxial growth for thin film layers, many researchers have investigated the multicolor photodetectors grown on single crystalline substrates such as quantum well infrared detectors (QWIPs), quantum dot infrared photodetectors (QDIPs), type-II photodetectors, and nBnBn photodetectors with the multiple sensing regions [14-16]. These QWIPs and QDIPs consist of multiple quantum well and quantum dot regions for sensing different colors. In these classes of detectors, the photons are absorbed within active region which lead to activate the carriers from ground state to higher state as shown in Figure.6. These activated carriers are collected with an internal or external electric field which generates photocurrent. Figure.7a shows the actual structure of GaAs based QWIPs with multiple absorption regions which has three terminals for apply biases to each active region [14]. By using these QWIPs, first FPA were fabricated with operability of 97 % and the excellent imagery in different colors was shown in Fig.7b. It was included that the appearance of the filter and soldering iron. QWIPs and QDIPs have advantages that various absorption bands can be formed by tuning thickness and composition of quantum wells and quantum dots regarding target wavelengths. On the other hand, the total thickness should be carefully considered due to built-in strain of epitaxial layer and critical thickness. Also, to obtain the target wavelength, compositions of layers should be delicately controlled during eptiaxy.

In a similar manner, type-II superlattice (T2SL) has been developed for offering the extension of wavelength ranging from SWIR to LWIR. This type-II superlattice structure contains the nearly lattic-matched groups such as InAs, GaSb and AlSb of 6.1 Å family in III-V compound semiconductor

materials. Various band alignments can be constructed from each material as depicted in Figure .8 [17]. When GaAs/AlSb, InAs/AlSb and InAs/GaSb materials are paired, type-I nested structure, type-II staggered, and type-II broken band gap structures are formed, respectively. Among them, InAs/GaSb broken band can offer new availability of band structure like interband devices by using the InAs conduction band and the GaSb valance band, beyond the original bulk band gaps. Through this structure, many studies have been extensively reported in regards of type-II photodetectors. Figure. 9 shows the design of T2SL detectors using only two terminals which have three colors detection region of SWIR, MWIR and LWIR from top to bottom [16]. They have successfully reported the high performance detectors for different colors by applying the bias that changes the band structure. However, this voltage controlled behavior is difficult to sense the multicolor simultaneously which can lead high power consumption. Furthermore, thin film should be not only adjusted to the delicate growth of a monolayer level for each material, but also the control of doping level is significantly important to obtain designed band structures. As a result, the high complexity of type-II material based photodetectors have been main bottleneck to spread of such devices.

Unlike these complicated methods, a bulk epitaxial layer based a simple photodetector was reported [16]. The nBnBn structure based on InAsSb and GaSb was grown on GaAs substrate with novel growth technique of interfacial misfit array (IMF) shown in Figure.10a. This growth method allows direct epitaxy without buffer layers under special growth environment such as lattice mismatch and growth temperature. As shown in Fig.10a, absorption regions consisted of InAsSb for SWIR and GaSb for near-IR with

barrier layers. Simulated band structure of the photodetector can be seen as shown depicted in Fig. 10b. Clear barrier layers including AlGaAsSb (~1.3 eV) and built-in potential (~0.6eV) were shown for blocking electrons. This photodetector was fabricated with 3 terminal for top and bottom PDs. It was defined as InAsSb nBn diode (D1), InAsSb/GaSb/GaAs heterojunction diode (D2) and combined nBnBn diode (D3) for independent comparison. As a result, the device can sense the SWIR and MWIR at room temperature which could lead to 2 colors detection with bias selection. However, high dark current density still exist due to defects and dislocations in despite of barrier layer insertion which could increase the noise characteristics and deteriorate detector performances. Additionally, detection ranges have been limited to infrared region (SWIR to LWIR) for all epitaxy methods due to restriction of materials choice. Therefore, novel growth techniques which cover all wavelength ranges are highly required.

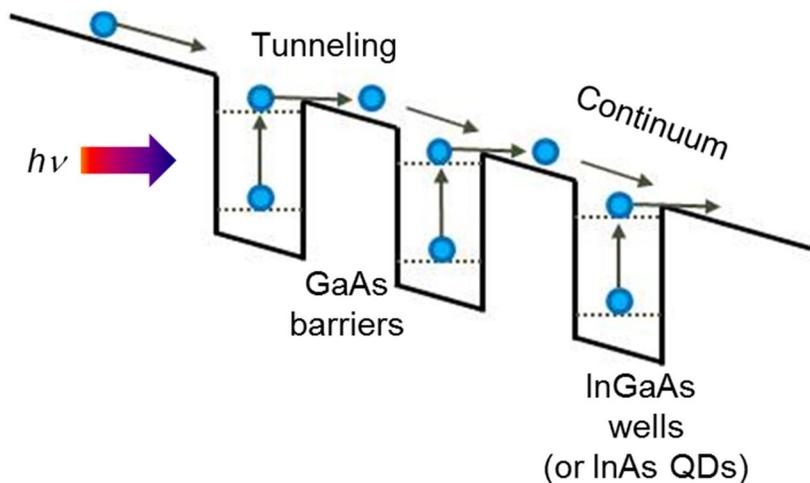
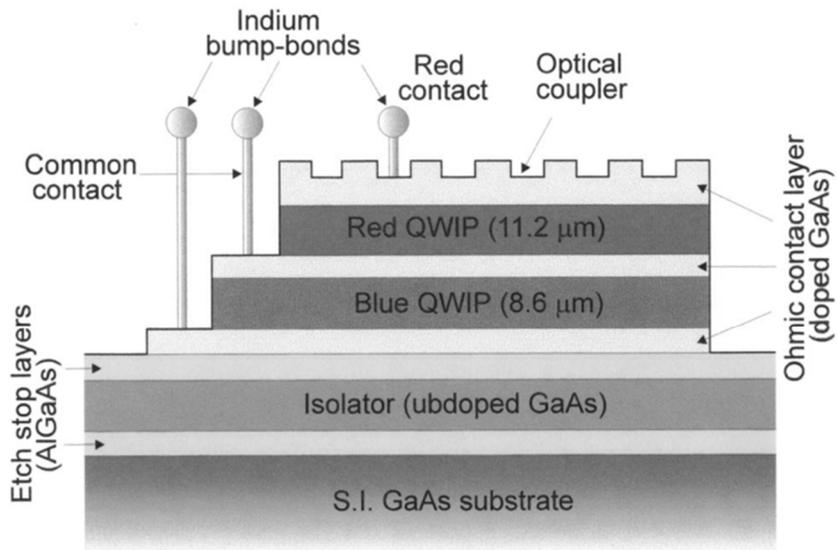


Figure 6 schematic of photon absorption mechanics for III-V quantum wells and quantum dots

a)



b)

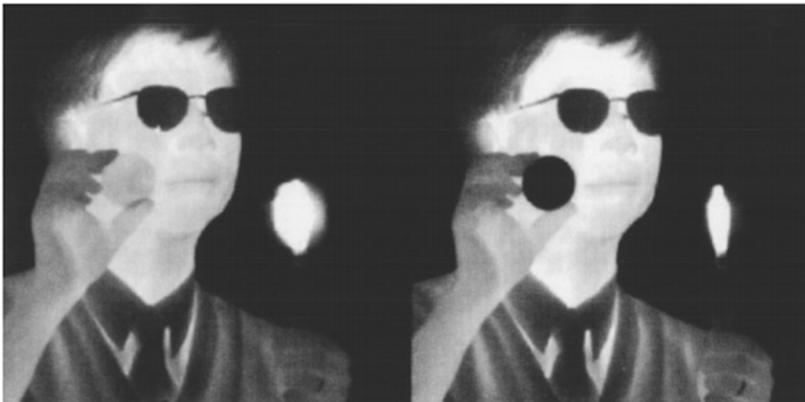


Figure 7 a) structure of a two-color stacked QWIP, b) simultaneous images with optical filter and the soldering iron from 256×256 MWIR/LWIR QWIP FPA's [14].

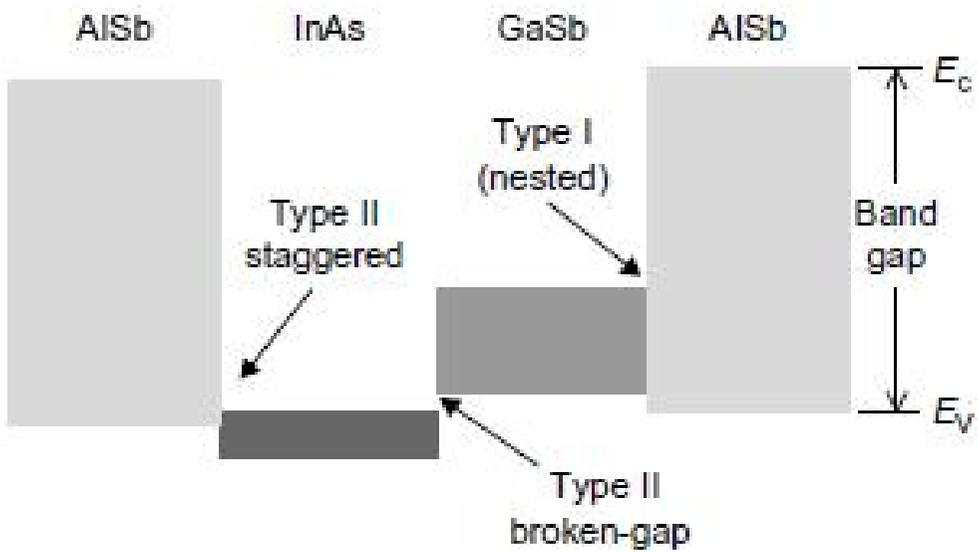


Figure 8 schematic of band alignment in InAs, GaSb and AlSb material systems with similar lattice constants. There are three types of band alignment of type-I (nested), type-II (staggered and broken) [17].

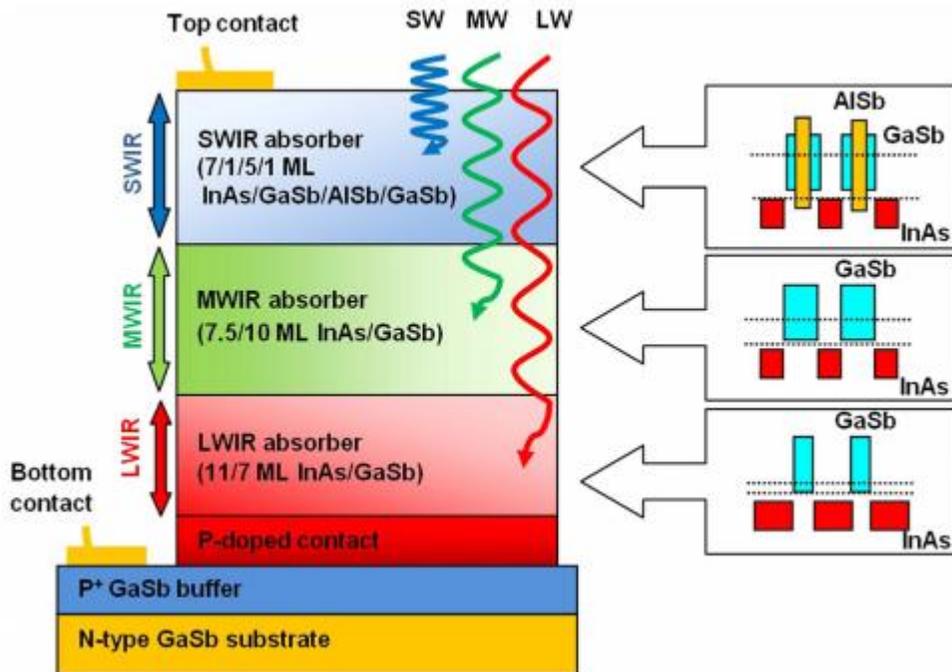
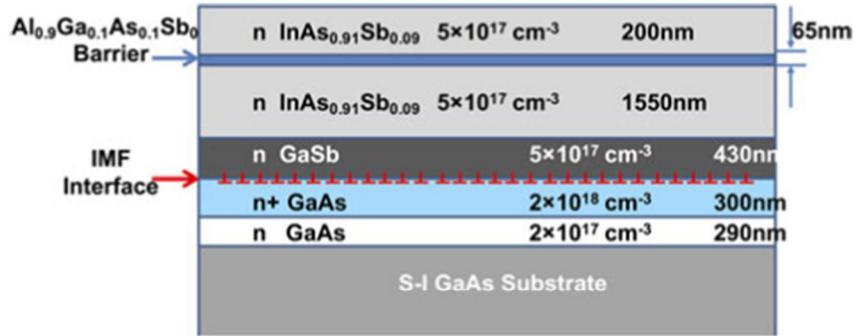


Figure 9 schematic of triple bands (SWIR-MWIR-LWIR) photodiode structure in type-II superlattices [15].

a)



b)

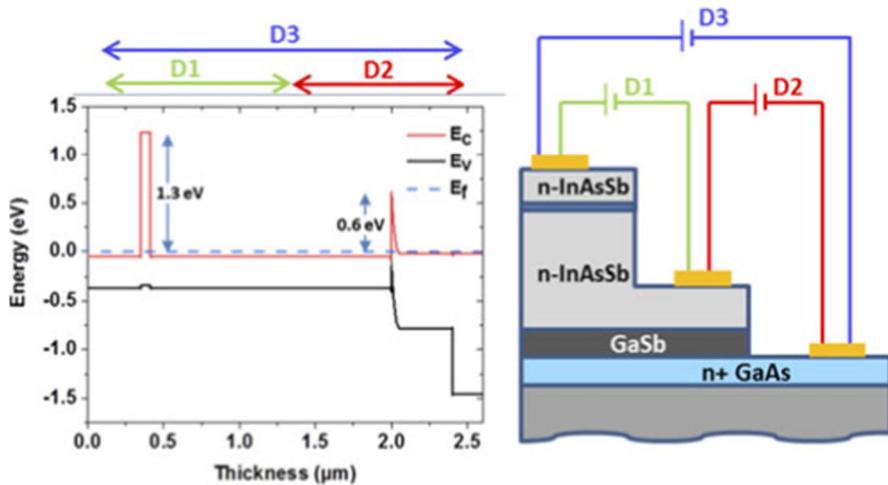


Figure 10 a) schematic of nBnBN layer structure consisting of InAsSb and GaSb grown on GaAs substrate with interfacial misfit array (IMF) technique, b) simulated band diagram of above structure at 300K (left) and fabricated device with three contacts for testing each absorption region [16].

1.3.2. Heterogeneous integration

Heterogeneous integration means the assembly and packaging of multiple separately manufactured components onto a single chip in order to improve functionality and enhance operating characteristics [18]. Recently, to circumvent above mentioned epitaxy issues, heterogeneous integration by 3-dimensional stacking has been severely investigated as one of the approaches to facilitate multicolor PDs as well as micro-light emitting diodes (LEDs), metal-oxide-semiconductor field-effect-transistors (MOSFETs) [19, 20]. The heterogeneous integration of various PDs has an important advantage for future multifunctional PDs. At first it could eliminate the external components such as splitter, filters for multicolor detection in typical optical systems which leads the compact and low power consuming detection systems [21]. Secondly, thanks to freedom of choice about stacking materials, heterogeneously integrated multicolor PDs enable the various wavelengths detection with a variety of materials having UV, visible and infrared regarding target applications. Additionally, it could decrease the complexity of epitaxial layer growth since typical bulk layer based any photodetectors could be utilized for sensing the photons.

Although these many advantages, few results about heterogeneous integration have been reported even in visible and infrared wavelength region. S. W. Seo *et al.*, demonstrated that the heterogeneous integration of GaAs metal-semiconductor-metal (MSM) PD and InGaAs MSM PD on Si substrate by using BCB adhesive bonding layer as depicted in Figure.11 [21]. Each PD was vertically integrated and operated in their absorption region. This method required highly accurate alignment and delicate post-processing conditions

for adhesive bonding when they are combined [22]. Without well-defined post processing, voids can be created at the interface between polymers as shown in Figure. 12.

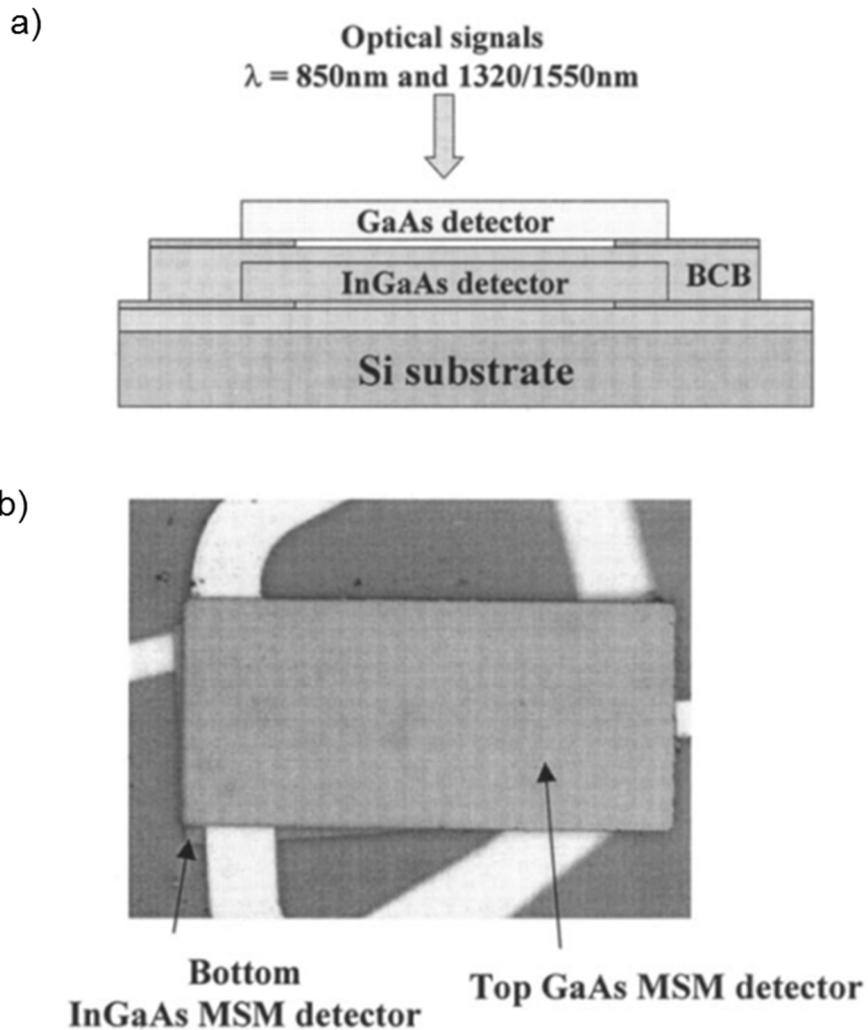


Figure 11 a) schematic of concept for multispectral detection system consisting of GaAs and InGaAs absorption materials on Si substrate, b)

Optical image of fabricated thin-film MSM detectors on contact pads [21].

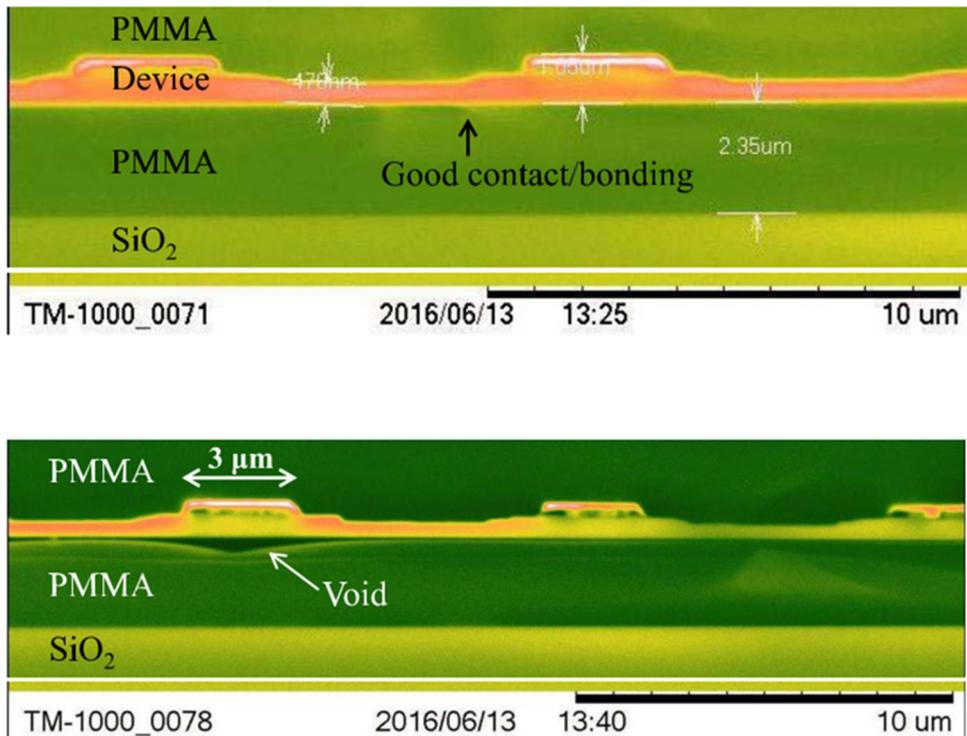


Figure 12 bonding interface of the sample with good and bad bonding states.

Void existing at the interface in the bottom SEM image [22].

L. Menon *et al.*, showed the InGaAs and Si membrane four-color photodetector arrays by using a transfer printing method [23]. Thin film Si PDs were transferred on the plane of top InGaAs PD grown on InP substrate as shown Figure.13. Its structure consisted of InGaAs PD next to the Si PDs on the same plane. Despite this planar integration could detect the multicolor by using Si and InGaAs PD, the versatility in the single pixel area and misalignment in large area process need to be improved. Therefore, top-down fabrication processes after heterogeneous integration are significantly

necessary to obtain the high resolution and multi-functionality.

Hamamatsu that is the company well known for optoelectronics devices has commercialized two color detector as shown in Figure.14 [24]. This two color detector is comprised of visible Si photodiode and MWIR InAsSb photodiode. Since dimension of two color detector is relatively large, we deduced that two color detector would be assembled by packaging process. From this reason, it cannot be applicable to make photodetector array with pitch scaling. Ultimately, in order to form multicolor PDs, the key technology is how to vertically incorporate the PDs without misalignment and degradation between top PDs and bottom PDs for forming array of photodetectors.

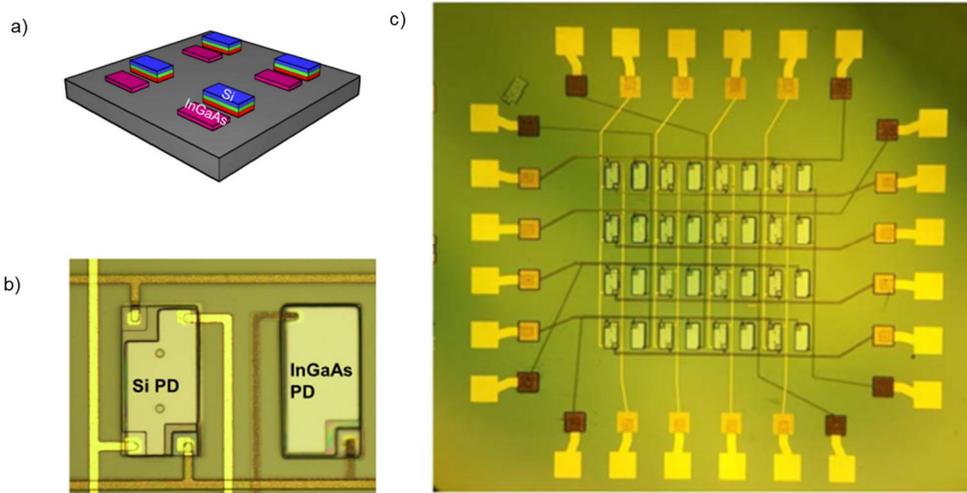


Figure 13 a) conceptual image of Si pixels transferred onto InP substrate for 4 colors detection, b) optical image of unit cell of 4 colors absorption, c) 4 x 4 array of Si//InGaAs detector unit cells [23].

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Figure 14 photograph of commercialized Si//InAsSb two-color detector [24].

1.3.3. Summary of each method

The features of the heterogeneous integration and epitaxy methods for implementation of multicolor photodetectors have been summarized in Table.1. In epitaxy method, while there is strong advantage of band gap

engineering which leads to make multicolor photodetector relatively easy, it is hard to grow the designed layer which is easily influenced by growth parameters. In contrast to epitaxy, heterogeneous integration of bulk structure, difficulty of growth is extremely low since it can be grown on crystalline substrate with very similar lattice constants. However, in order to fulfill the multicolor photodetectors, heterogeneous integration should be required with different photodetectors. Although an additional heterogeneous integration process is required for bulk structure, an integration using III-V bulk photodetectors seems to be beneficial in terms of band gap engineering, growth, cost and uniformity. Therefore we have focused on the heterogeneous integration of III-V bulk structures for relieving the various difficulties of epitaxy based multicolor photodetectors.

	Heterogeneous integration		Epitaxy	
	IV Bulk	III-V Bulk	QWIP/QDIP	Type-II
Material	Si, Ge, Si _x Ge _{1-x}	InAs, InSb, InGaAs, InAsSb	GaAs/AlGaAs, GaSb/AlSb	InAs/GaAs, InAs/InGaSb
Band gap engineering	▲ (to SWIR)	●	●	●
Cost	Low	medium	High	High
Uniformity	●	●	●	?
Multicolor	X (→ ●)	X (→ ●)	●	●
Difficulty of growth	Low	Low	High	High

Table 1 Benchmark of formation methods for multicolor photodetectors.

1.4 Overview of heterogeneous integration technology

1.4.1. Introduction

To integrate various photodetectors, lift-off technologies of single crystalline thin films from substrates have been developed which enables the production with inexpensive, lightweight and flexible substrates. In order to achieve lift-off of thin films, various approaches including epitaxial lift off (ELO), splitting by ion implantation and transfer printing have been introduced. Substantial attempts have been also tried to maintain the high quality of thin films which could keep the high performance of electronic and optoelectronic devices on other substrates.

Additionally, to complete heterogeneous integration, bonding technology is significantly needed with lift-off technologies. Lifted-off thin films should be bonded to other materials into a single substrates due to fabrication of thin film devices. To bond other materials, many researchers have investigated direct bonding, cold-weld bonding, eutectic bonding and adhesive bonding by using different intermediate layers and mechanisms.

In this chapter, heterogeneous integration methods are going to be simply introduced by using a combination of various lift-off technology and bonding technologies.

1.4.2. Direct bonding

It is one of wafer bonding which describes the adhesion between two mirror-polished semiconductor wafers [25]. For directly bonding of two wafers, there are several requirements such as smooth surface (roughness < 1nm), flat wafers (no wavy) and small different of thermal expansion coefficient which causes the fails of wafer bonding. Nevertheless, this process results in the weak adhesion of Van der Waals bonding by using attractive intermolecular forces at room temperature. This bonding force would be relatively lower than covalent or metallic bonds. In order to obtain the higher bonding strength, wafers are treated in thermal annealing process at high temperature to transform weak bonds into covalent bonds. In case of Si-Si wafer bonding, annealing temperature is usually above 500°C [25]. However, a high temperature treatment could limit the applications due to high thermal budget. Thus, surface activated bonding process have been introduced as alternative technique to gain high bonding strengths at lower temperature below 400°C. Bonding process is basically same, but surface activation process is carried out before bonding to wafers. Especially, treatments using oxygen plasma are commonly used in equipment of reactive ion etching (RIE), inductively coupled plasma-RIE (ICP-RIE) and microwaves. Through plasma activation process, high quality wafer bonding can be achieved without high temperature treatments.

Figure 15 shows the direct bonded GaAs and Si at room temperature by using surface activation process [26]. It shows a cross-sectional scanning electron microscope (SEM) of material's interface. Even without a high temperature annealing, this process avoid undesirable effects by the thermal

expansion mismatch. However, there is interfacial oxide at semiconductor interface which originated from non- vacuum process.

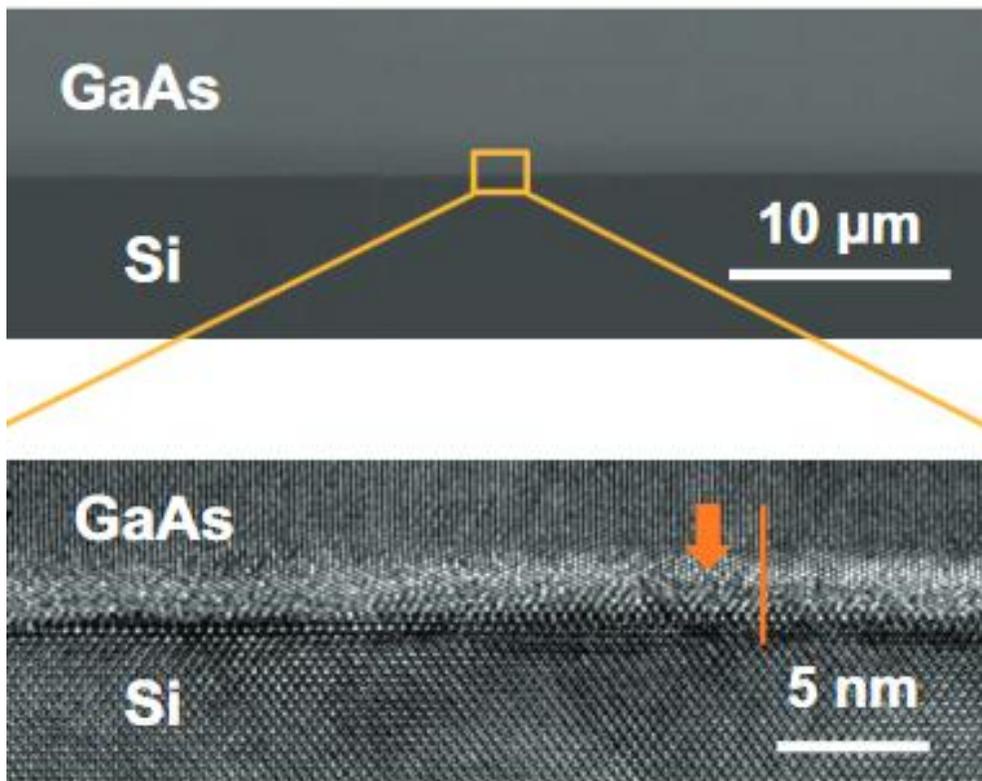


Figure 15 SEM image of direct bonded GaAs//Si with surface activation bonding at room temperature (top), high resolution TEM image of GaAs//Si bonding interface with an interfacial layer (bottom) [26].

1.4.3. Cold-weld bonding

Cold-weld bonding process is conducted for forming metallic junction which uses the soft metal species usually [27]. This cold weld bonding would require the low temperature and pressure when joining the two clean metal species. This bond is usually dependent on plastic deformation of the metal to contact closely. Previous research found that two metals can form a metallic junction if the distance between flat surfaces would be below a critical thickness as shown in Figure.16 [31]. For nickel (100), interfacial separation cannot be held when distance of two flat surfaces is below 1.9 Å. It is known that slightly larger than bulk interatomic spacing of nickel. Additionally, since a metallic junction can be formed within 100 fs under ambient conditions, applying considerable pressure should be required at interfaces to overcome surface imperfections such as contaminants. By using this cold-weld bonding, in spite of presence of contaminants, Au-Au bonding was successfully achieved even with order of μN force [29]

1.4.4. Eutectic bonding

Eutectic bonding have been attractive over other bonding methods because soldering metals such as Sn make viscosity of adhesion metals lower. It results in easy spread of bonding metals over the bonding area. Furthermore, relatively high surface roughness, contaminants and irregularities could be accommodated. By heat treatments after bonding process, eutectic alloy is formed at the interface which goes through a liquid phase. To uniformly bond

the other materials, it is important that bonder temperature uniformity and avoidance of overshooting. Therefore, depending on the bonding metal, the temperatures for eutectic alloy were noted in Table.2 [25]. These are the main reasons why AuSn20 as the solder alloy with the lowest melting point is used more often than other gold - rich solder alloys.

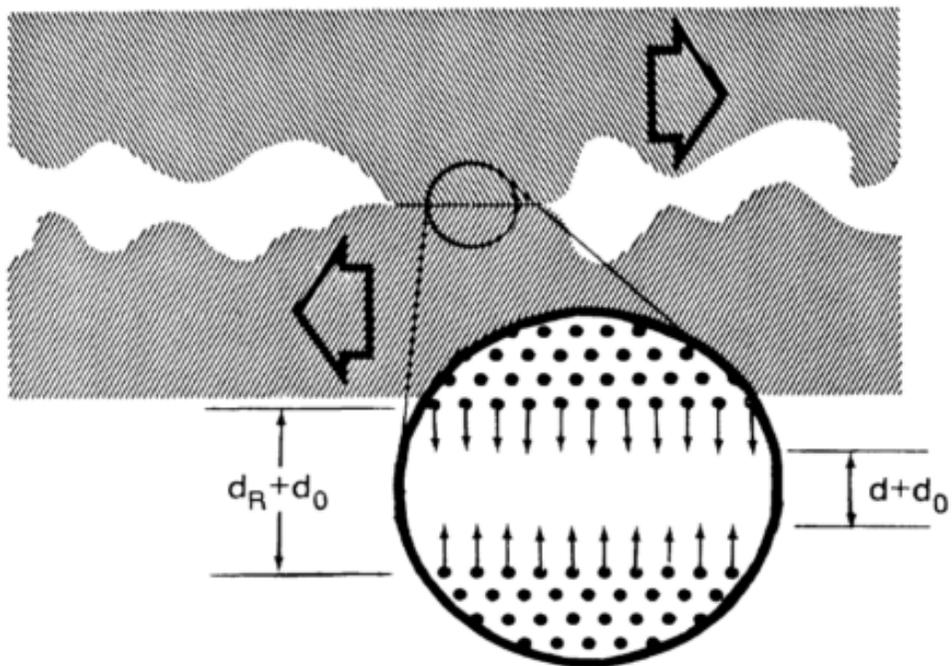


Figure 16 Schematic of cold-weld bonding mechanism [28].

Gold-rich eutectic solder alloys	Eutectic temperature (°C)	Components of microstructure
AuSn20	278	AuSn (δ) + Au ₅ Sn (ζ)
AuGe12	356	Au + Ge
AuSi3	363	Au + Si
AuIn28	450	AuIn + Au ₇ In ₃ (γ')

Table 2 Candidates of gold-rich solder alloys for eutectic bonding [25].

1.4.5. Adhesive bonding

Adhesive bonding have extensively used the polymers such as tape, wax or glue as temporary bonding method [25]. This intermediate polymer layer can hold them two wafers. After polymer layer is coated on semiconductor surfaces, applying the pressure is carried out for forming intimate contact. To make stronger the adhesive force, curing process (annealing process) should be conducted, subsequently. Adhesive bonding has a main advantage in terms of an annealing process that is relatively low temperature between room temperature to 450°C. However, it can go through the outgassing process which easily induces voids at the interface without optimal curing conditions.

1.4.6. Transfer printing

By utilizing these bonding methods, many studies have been extensively studied regarding a heterogeneous integration [ref]. Among them, transfer

printing by using polymer stamps such as polydimethylsiloxane (PDMS) is representative and popular. Transfer printing has been used with a combination of selective etching. As shown Figure.17 and Figure.18, epitaxial layer structures include the sacrificial layer for selective etching to active layers. Fig.17 illustrates the transfer printing method III-V layers from donor substrate to silicon substrate [30]. The bonding mechanism between polymer stamp and III-V layer is known for Van der Waals bonding. Thus, the yield of transfer printing method strongly depends on peel-off velocity of polymer stamps due to viscoelastic behavior of stamps. In order to separate epitaxy layers from the donor substrate, fast peel off speed would be applied. On the contrary, to adhere the epitaxial layers to other substrates, peel velocity should be slow which allows the layers to be placed in position. In a similar way, the schematic of InAs thin film transfer from GaSb substrate via AlGaSb sacrificial layer was shown in Fig.18 [31]. Moreover, a variety of handling materials including sticky tape, thermally releasable tape, Kapton tape and Black wax has been demonstrated according process windows.

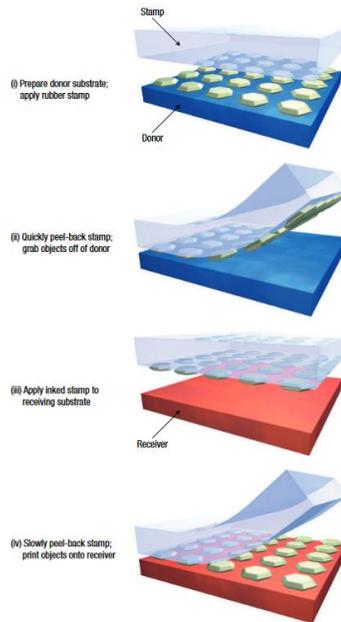


Figure 17 schematic of transfer printing process by using elastomeric stamp with variation of peel-off speed [30].

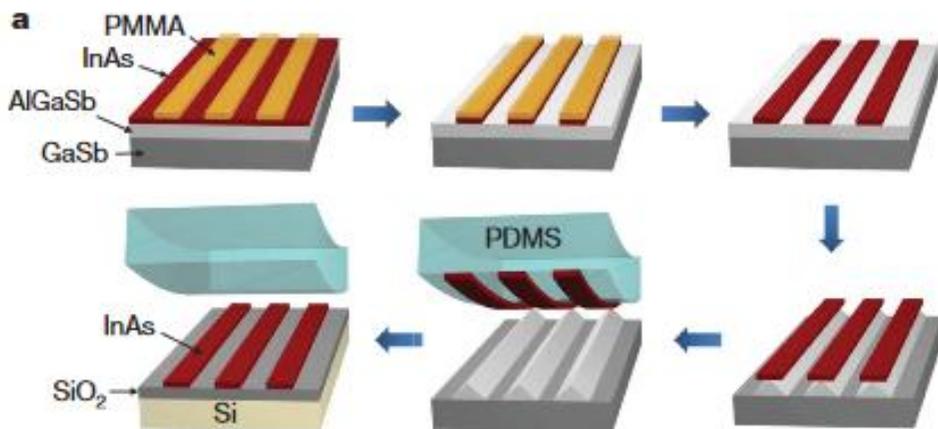


Figure 18 fabrication process flow for integrating InAs on Si substrates by transfer printing method [31].

1.4.7. Wafer splitting

Wafer splitting is one of famous technologies for epitaxial layer transfer which is also known as Smart-cut. Through a silicon layer transfer, silicon-on-insulator (SOI) wafers could be fabricated by hydrogen implantation [32]. Additionally, wafer splitting is a universal process without dependency of a type of substrates. Figure.19 shows the process flow of wafer splitting by hydrogen implantation. At first, surface of silicon wafer is oxidized for protecting the surface from the implantation damage and forming an intermediate bonding layer. Subsequently, hydrogen implantation is carried out with optimized dose and depth followed by wafer bonding to other substrates. The implanted hydrogen atoms can form the hydrogen complexes with interacting the defects which were made by previous implantation. During thermal annealing process, H₂ molecules are formed by dissociation of hydrogen complexes and diffusion producing the bubbles in a finite area. It can create micro-cracks which can increase the internal pressure and expand cracking region, leading to separation of layer and substrate. After splitting, final chemical mechanical polishing (CMP) step should be conducted due to relatively large roughness. As a result, SOI wafers can be obtained by wafer bonding and wafer splitting method.

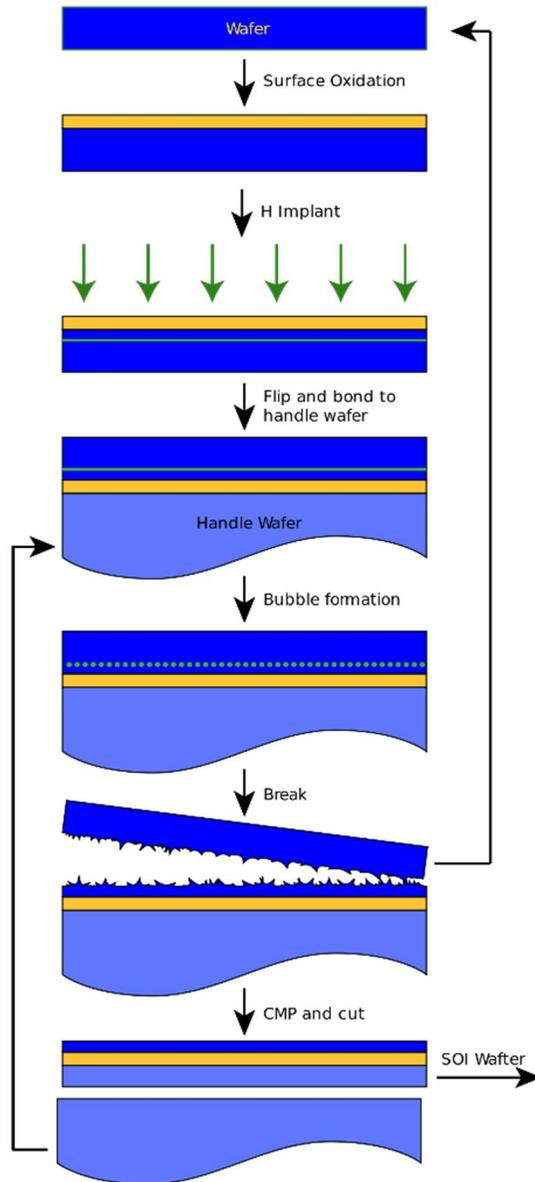


Figure 19 schematic of wafer splitting method for fabricating silicon-on-insulator (SOI) called as SMARTCUT [32].

1.4.8. Epitaxial lift off (ELO)

Epitaxial lift off (ELO) was developed for fabrication of GaAs thin films in 1978 by Konagai [33]. This process employed AlGaAs sacrificial layer to selectively separate the GaAs active layer. After first demonstration, ELO technology has been widely used for the integration of III-V films on other substrates thanks to their advantages such as process stability, wafer reusability and cost reduction of substrate [34,35]. When ELO is generally used with a combination of wafer bonding technology for a large area integration, it is better stability compared with a transfer printing. Figure.20a shows the fabrication process for III-V solar cells on flexible substrates by using cold-weld bonding and ELO technology [36]. At first, bonding materials were deposited on the surfaces of semiconductor and flexible substrates. In addition, bonding process was carried out with a pressure and thermal annealing. To separate the donor wafer, the bonded sample was dipped in hydrofluoric (HF) acid which can attack the AlAs sacrificial layer. Finally, III-V thin film on flexible substrates were successfully fabricated as illustrated in Fig. 20b. Additionally, to maximize the ELO advantages, various technologies including non-destructive ELO, weight-induced ELO and multiple layer release process have been introduced. By using these methods, the performances of many electronic and optoelectronics devices could be enhanced through back interface control for ultra-thin body (UTB) mosfets and photo-recycling for solar cells.

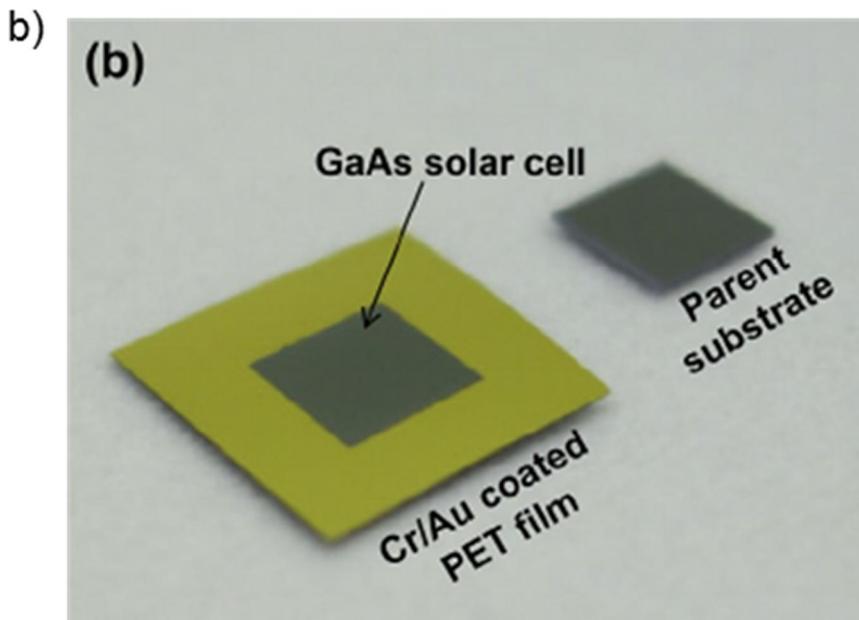
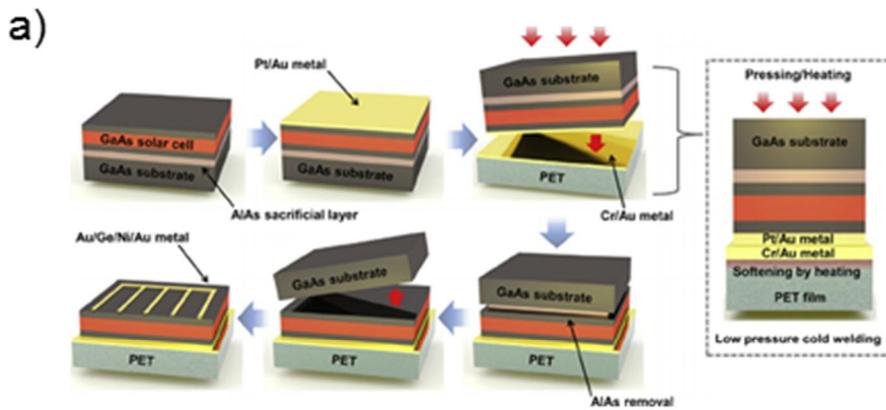


Figure 20 a) process flow of solar cells on flexible substrates by using cold-weld bonding and epitaxial lift off, b) photograph of transferred GaAs thin film on PET film and parent GaAs substrate (donor wafer) [36].

1.4.9. Benchmark of different heterogeneous integration methods

The benchmark of heterogeneous integration methods is tabulated in Table.3. In respect to possibility of large area transfer (>300mm), while splitting and ELO method could correspond to large area with a wafer scale, a transfer printing method leaves the question about it. In the same vein, ELO and splitting can be used for formation of multicolor photodetectors array regardless of the number of matrix. However, transfer printing has a drawback for array formation due to dependency of experimental conditions sensitively. In terms of cost, the key problem with splitting method is extremely high cost since ion implantation and additional CMP process for wafer separation and reduction of roughness are costly. In contrast to wafer splitting, transfer printing and ELO do not contain costly processes.

Additionally, recovery of epitaxial layer quality has been a main issue originating from the ion implantation process. Although wafer bonding and ELO process has a lot of advantages such as large area transfer, cost, array formation and layer quality for fabricating multicolor photodetectors, one major drawback of this approach is low throughput for producing heterogeneously integrated structures. While wafer splitting takes a few minutes to a few hours for separating donor wafers, ELO process takes 3 hours at least to a few days in previous reports [ref]. Considering pros and cons regarding each method, wafer bonding and ELO method has more advantages than transfer printing and wafer splitting if low throughput of ELO process could be improved to a few minutes. In order to fabricate the high performance multicolor photodetectors easily, the improvement of

throughput should be conducted.

	Selective etching +Transfer printing	Wafer bonding + splitting	Wafer bonding +ELO
Large area transfer >300mm	?	●	●
Cost	Low	High (Ion implantation, additional CMP)	Low
Array formation	▲	●	●
Layer quality	●	▲	●
Throughput (process time)	▲ (3hrs~a few days)	● (1min ~ a few hrs)	▲ (3hrs~a few days)

Table 3 benchmark of different heterogeneous integration methods

1.5 Thesis overview

The major goal of this study is to fulfill the multicolor photodetectors based on III-V bulk p-i-n structures by using heterogeneous integration. As shown in Figure.21, a proposed structure of multicolor is comprised of short wavelength top photodetector and long wavelength bottom photodetector through an intermediate bonding layer. As we discussed above, improvement of low throughput for wafer bonding and ELO process are crucial to enhance the layer quality and array formation for high yield. Thus, development of high throughput heterogeneous integration is significantly needed. Furthermore, in order to secure the bulk p-i-n photodetectors for various wavelengths, design and characterization of III-V based photodetectors are important. Ultimately, via a combination of high throughput heterogeneous integration with III-V bulk photodetectors technology, multicolor photodetectors could be realized in this study. Therefore, this thesis contains three parts as research subjects for heterogeneously integrated III-V photodetectors array.

1. In chapter2 and chapter3, it describes a high throughput ELO process that involves a pre-patterning step before the wafer bonding and the use of etching acceleration solutions. Furthermore, it demonstrates that the III-V based various electronic optoelectronic devices such as high electron mobility transistors (HEMTs), solar cells, heterojunction phototransistors (HPTs) and photodetectors on rigid Si substrates. After the transfer of III-V device layers, it is further

studied that donor wafer can be re-used after the wafer bonding and ELO process at least once. These approaches enable a high-throughput fabrication of GaAs on other substrates with a high-quality film of GaAs, which lead to a dramatic cost reduction as estimated.

2. In chapter 4, to fulfill bulk type based photodetectors ranging from ultraviolet to long wavelength infrared, narrow band gap semiconductors should be investigated. Instead of complex layer structures like quantum wells, quantum dots and type-II, an alternative bulk material of $\text{InAs}_x\text{Sb}_{1-x}$ can correspond to band gaps ranging from short wavelength to long wavelength infrared region. To confirm the feasibility of InAsSb materials, we have investigated the InAsSb based heterojunction photovoltaic detectors.
3. In chapter 5, there are many critical issues regarding conventional bulk layers based multicolor photodetectors including alignment accuracy along to (001) direction of top and bottom photodetectors, possibility of top-down fabrication process and pitch scaling for high pixel density. To overcome these critical issues, a monolithic integration of visible and near-infrared photodetectors has been carried out in order to establish the optimized fabrication process and confirm the feasibility of proposed multicolor photodetectors.

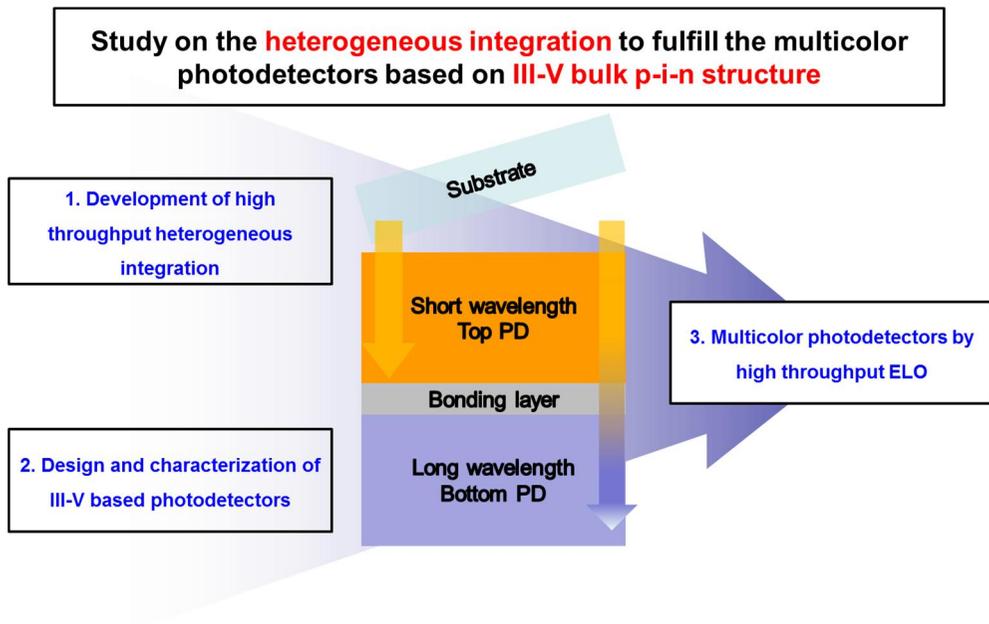


Figure 21 schematic of objective of this thesis

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Chapter. 2 Method for heterogeneous integration of III-V compound semiconductors on other substrates

2.1 Introduction

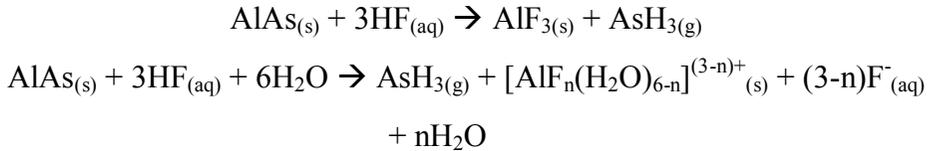
To implement monolithic integration of multicolor photodetectors, the key technology is how to vertically and rapidly incorporate the Photodetectors (PDs) without misalignment and degradation on rigid substrates. Historically, epitaxial lift off (ELO) was developed in the 1980s and 1990s after Konagai *et al.* first proposed the method, in which the device film and donor wafer are split by the selective etching of the AlGaAs layer located between the device film and the donor wafer [1]. However, ELO was not popularly used at the time due to very long process time of up to several days. Recently, a reduction of the processing time for the ELO process has been developed by introducing a flexible carrier substrate and a different sacrificial layer; however, the handling of the flexible carrier increases the process complexity and still requires a long processing time of several hours [2-7]. Additionally, despite it can be possible to transfer the thin films onto flexible substrates, it is still hard to transfer thin films on other rigid substrates vertically for our aims. Therefore, for the practical use of the ELO technique, it is important to reduce the processing time and produce a high-quality film on rigid substrates at the same time.

In this chapter, we describe a high throughput ELO process that involves a pre-patterning step before the wafer bonding and the use of etching

acceleration solutions. Furthermore, we demonstrate that the III-V donor wafer can be re-used after the wafer bonding and ELO process at least once. These approaches enable a high-throughput fabrication of GaAs/Si substrate with a high-quality film of GaAs, which lead to a dramatic cost reduction.

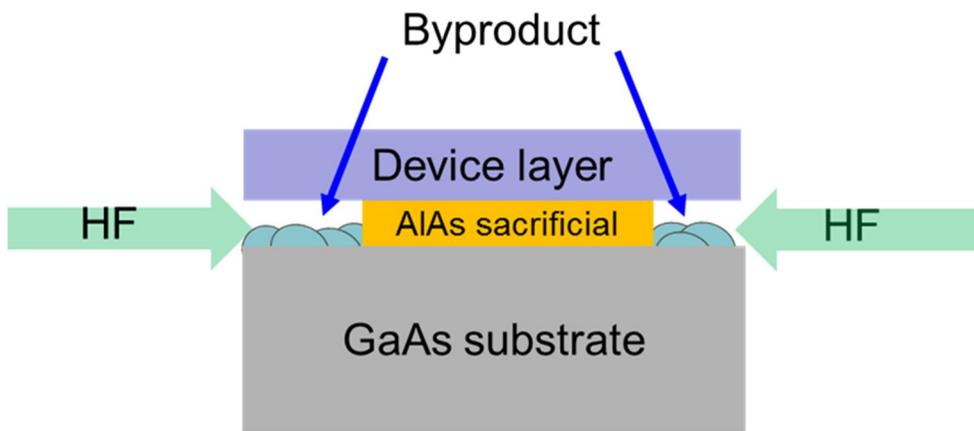
2.1.1 The origin of low throughput in conventional ELO

In the GaAs based devices, AlAs has been widely used for sacrificial layer for separating the donor wafer because the high etch selectivity of a hydrofluoric acid (HF) solution for AlAs with respect to GaAs (10^6) [7]. Thus, it is critical to comprehend chemical reaction between AlAs and HF for improving the conventional ELO process. A. T. J. Niftrik showed the chemical reaction as follows, [8]



In ELO process, when AlAs layer is etched in HF solution, which results in the formation of solid aluminum fluoride ($\text{AlF}_3 \cdot 3\text{H}_2\text{O}$) and arsine (AsH_3) gas, and dissolved aluminum fluoride complexes as byproducts. As described reaction model, solid byproduct and the out-diffusion of AsH_3 related gases through the narrow etch opening can be attributed to the lateral etching rate as shown in Figure. 22. Moreover, since it is contaminate the substrates after

ELO process, the substrate should be treated by using chemical etchant and chemical mechanical polishing (CMP) process.



Conventional : 😞 Slow

Figure 22 problems of conventional ELO process

2.1.2 Previous works for enhancement of ELO throughput

On the basis of these reactions, ELO process was explained by a diffusion and reaction related model (DR-model) considering the etch rate dependence on the aluminum fraction, HF concentration and the strain of the layer as depicted in Figure. 23 [9]. It is noted that etch rate (V_e) is determined by HF diffused resistance (R_d), reaction related resistance (R_r) and HF concentration in the bulk of the solution in below Equation.1 [9].



Figure 23 diffusion and reaction model for ELO process

$$V_e = \frac{[HF]}{R_d + R_r} \quad \text{Equation.1}$$

In previous work, reaction related resistance is linearly dependent on temperature, and HF concentration. On the other hand, diffusion limited resistance is associated with the thickness of the sacrificial layer, aluminum composition of sacrificial layer, temperature, diffusion coefficient and activation energy for the HF diffusion. Thus, the reduction of a diffusion

related resistance plays an important role to increase the high lateral etching rate. To optimize each parameter, systematic studies were carried out regarding thickness, composition and HF concentration. Nevertheless, it cannot be prevented that lateral etching rate is reduced when the AlAs layer is steadily etched.

To boost and maintain HF diffusion, various approaches have been introduced such as weight induced ELO and the use of flexible carriers, strain induced metals [11-13]. Figure.24. shows the proposed weight-induced ELO which indicated the effect of radius of curvature on lateral etch rate. The bending of the substrate can help the HF diffusion by preventing the diminution of opening region near the etching interface. However, this weight on flexible carriers provides excessive bending radius which can induce the crack in the epitaxial layer. To reduce excessive bending, advanced weight induced ELO was developed. It can apply a constant curvature near etch front by using a guided cylinder as shown in Figure.25. As a result, epitaxial thin film was successfully lifted of without making cracks. Recently, stresses in metal films such as Ir/Au or Cr/Au have been used for reducing the ELO time [5]. Moreover, the influence of the internal stress in the thin film III-V solar cells on ELO time was investigated. By adjusting the layer stress in epitaxial layer growth, the enhancement of lateral etch rate was achieved and transferred on flexible metal foil as shown in Figure.26.

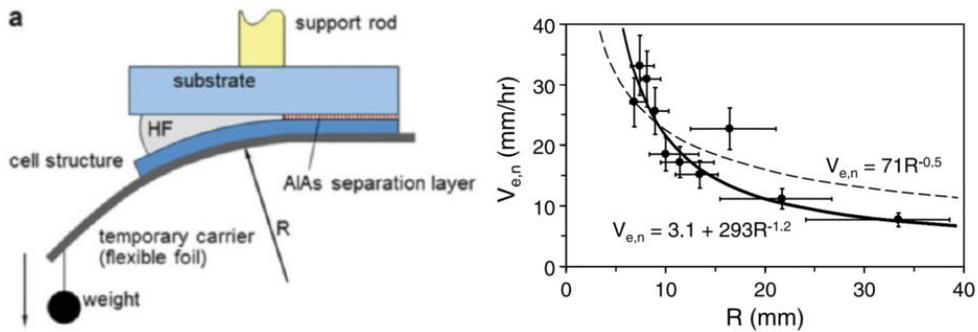


Figure 24 WI-ELO [11, 12].

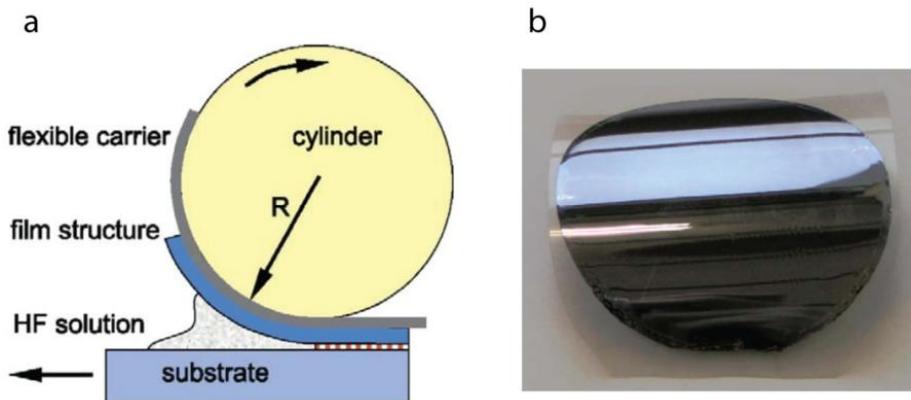


Figure 25 advanced WI-ELO [12].

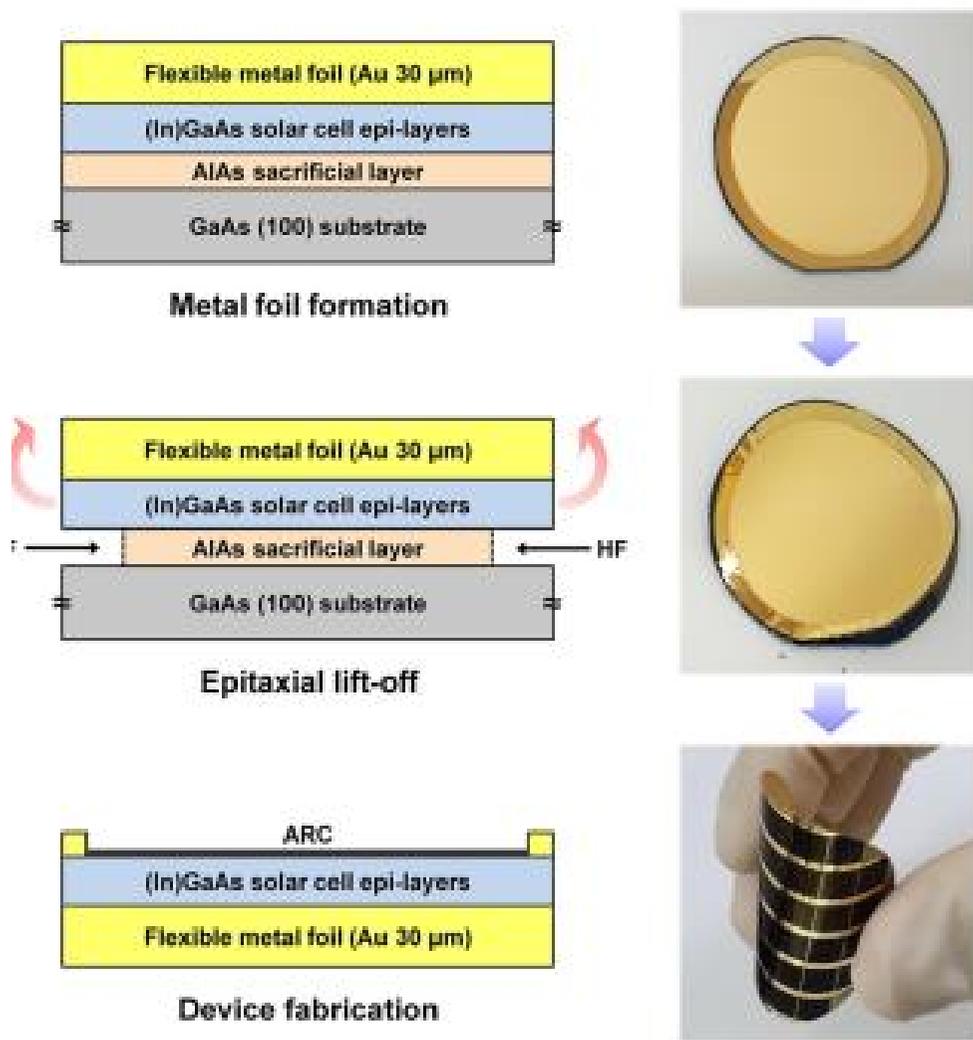


Figure 26 internal stress induced ELO [13].

Although many research groups have an effort to increase the diffusion of HF and reduce the ELO time, it still takes 3 hours to separate the donor wafers as tabulated in Table.4 [2-7]. Additionally, most studies have utilized

the flexible carriers and special techniques which are not suitable for vertically stacking the different layers for fabricating multicolor PDs.

Because of these reasons, there is a few studies regarding heterogeneous integration of III-V epitaxial layers on rigid substrates with short ELO time. It finally induces low throughput and hinders the utilization for potential of III-V layers. Therefore, heterogeneous integration of III-V epitaxial layer on rigid substrate with high quality and large scale is highly required.

Research institutes	Univ. of Illinois at Urbana-Champaign (USA)	Univ. of Michigan (USA)		National Ching Hsing Univ. (Taiwan)	MicroLink Devices, InC. (USA)	IBMT. J. Watson Research Center (USA)
Application/ time /Temp	GaAs solar cell, NIR detector, MESFET / - / -	GaAs solar cell / 48 hours / -	GaAs solar cell, LED, MESFET / 5 hours / RT	GaAs solar cell / 3 hours / RT	GaAs solar cell / 12 hours / -	LED / 8 hours / 60°C
Sacrificial layer	AlAs					InAlP/60°C
Published paper	Nature(2010)	Journal of Applied Physics (2012)	Advanced Functional Materials (2014)	Solar Energy Materials & Solar cells (2014)	IEEE-ICSE2014 (2014)	Nature Communications(2013)
Feature	Epoxy bonding	Only reuse	175°C metal bonding	Electroplating copper substrate	Flexible carrier	Not use for Indium based III-V

Table 4 Previous reports regarding epitaxial lift off technologies.

2.1.3 Approach: high-throughput ELO process

To improve the low throughput problem of heterogeneous integration on rigid substrate, we have proposed the modified ELO process called as ‘high throughput ELO’. As shown in Figure.27, instead of conventional ELO, we introduced the pre-patterning process and surface hydrophilization using hydrophilic substance. The main cause of the long processing time for the ELO was known to be the formation of H₂ bubbles and the etching residues generated during the ELO process [8-10]. To encourage H₂ bubble release and increase the accessible etching areas, a pre-patterning step that breaks the III-V layer into smaller pieces was added between the growth of III-V layer and the wafer bonding.

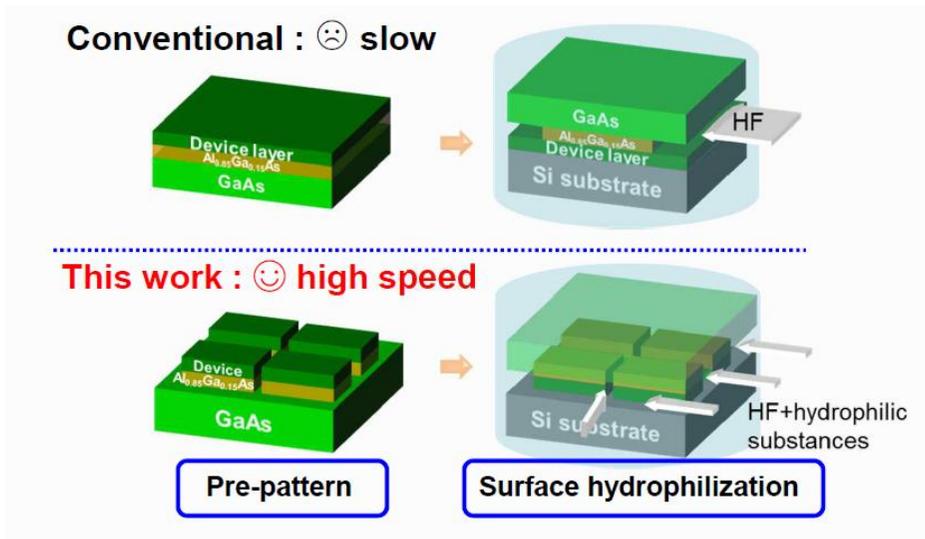


Figure 27 novel approach of high throughput ELO process

In addition, we inserted hydrophilic solutions into HF, which is typically used for the etching of the $\text{Al}_{0.85}\text{Ga}_{0.15}\text{As}$ sacrificial layer in the ELO process. Hydrophilic solutions were deionized water (DI), isopropanol (IPA) and acetone (Ace), which accelerate to penetrate the HF solution to etch front of $\text{Al}_{0.85}\text{Ga}_{0.15}\text{As}$ sacrificial layer by enhancing capillary force. Figure 28 showed the contact angles on GaAs surface with respect to HF adding the hydrophilic solutions. Initially, only HF solution exhibited the 86° of contact angle which indicated hydrophobic property on GaAs surface. When the ratio of mixed solutions were 1:1 (HF: hydrophilic solution), the surface contact angle was decreased from DI, ACE and IPA in order. In this fundamental experiment, HF: IPA solution recorded the lowest contact angle of 17° . From this result, it can be found that the species of hydrophilic solutions lead etching rate increase of sacrificial AlAs layer.

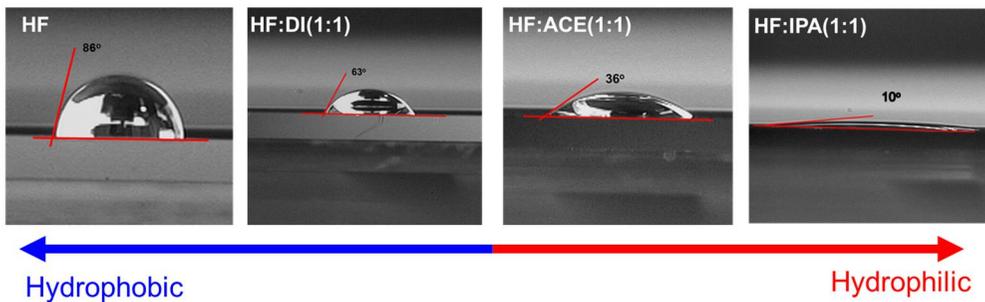


Figure 28 contact angles with various HF: hydrophilic substances

Here, one possible concern is the surface contamination during the patterning and etching. Therefore, for the high yield bonding, the careful surface preparation before the wafer bonding is needed. In our experiment, overall transfer yield was higher than 95 %.

2.1.4 Experimental procedure

Figure 29 shows a schematic of experimental process of high throughput ELO process. Initially, GaAs based epitaxial layers with sacrificial and etch stop layer for substrate protection and recycle were grown by molecular beam epitaxy (MBE). GaAs epitaxial layers and Si wafers were cleaned by NH_4OH and HF solutions, respectively, to remove the native oxides. Next, bonding materials, i.e., Y_2O_3 or Pt/Au in this study, were deposited via electron beam (E-beam) evaporation. A pre-patterning process was performed using H_3PO_4 - and HCl-based solutions for the etching of Al(Ga)As and InGaP, respectively. Subsequently, the wafers were cleaned by acetone in an ultra-sonic bath, followed by surface plasma treatment using O_2 and Ar for Y_2O_3 and Pt/Au, respectively. The surface-treated wafers were bonded to each other in the air, followed by uniaxial pressure. The ELO process was performed in HF-based solutions until the separation of the III-V/Si and the GaAs donor wafer was completed. The completion of ELO was determined when III-V/Si wafer and III-V donor wafer were separated. Here, we observed the sample separation on every 1 min after dipping the samples in HF-based solutions. Next, the wafer bonding was conducted at room temperature, followed by the device fabrication. To reduce the unfavorable effect due to the difference of the thermal expansion, a processing temperature including wafer bonding and device fabrication should be minimized. After this series of steps of the process, the donor wafer was re-used for another epitaxial growth using a flat and fresh surface formed by a highly selective etching of an etch stop layer (InGaP) using HCl: H_3PO_4 solutions.

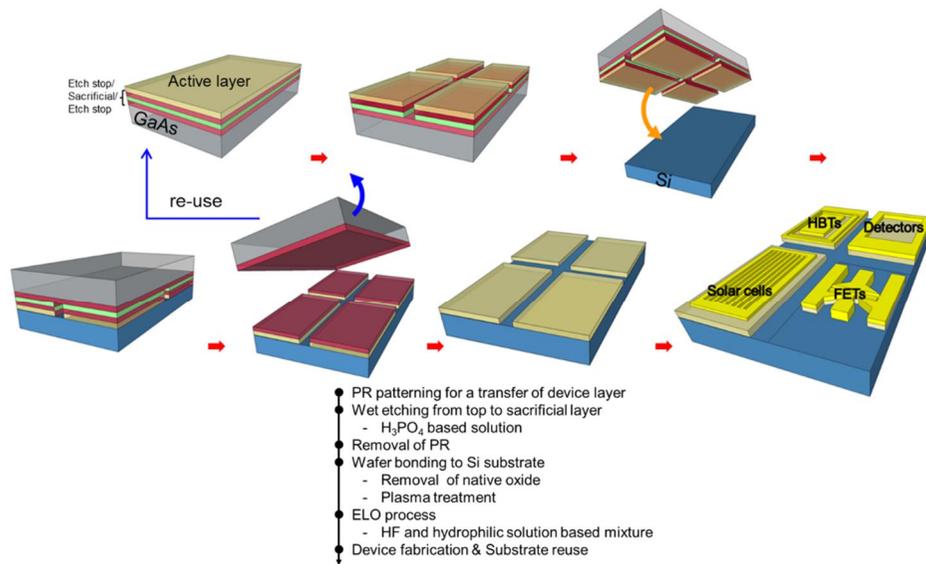


Figure 29 experimental procedures (not scalable)

2.2 Results and discussion

To investigate the effect of the pre-patterning step and the etching acceleration solutions, we compared the ELO process for various etching conditions. Figure.30a illustrates the ELO time for different etching conditions. Here, pieces of the bonded substrate of GaAs/Al_{0.85}Ga_{0.15}As/GaAs/Y₂O₃/Si with a size of 1.5×1.5 cm² were used for these experiments. For the pre-patterning, a mesa size of 670×620 μm² and spacing of 230 μm were used as standard dimensions. Without a pre-patterning step, the ELO process takes 30 hours in HF:DIW (1:5) solutions, which directly shows the difficulty of the use of a conventional ELO process. With a pre-patterning step, the ELO time was significantly reduced to 6 hours in the same solutions. This reduction is attributed to the increase of an exposed surface area of an Al_{0.85}Ga_{0.15}As layer due to the pre-patterning, which enabled the efficient gas bubbles release, resulting in the reduction of the ELO time [14-17]. To further reduce the ELO time, we changed the HF concentration and added etching acceleration solutions of isopropanol (IPA), acetone (Ace). Here, organic solutions, such as IPA and Ace, are known to produce hydrophilic surfaces, which can prevent H₂ bubbles from becoming large. This process promotes the rapid release of H₂ bubbles from the samples. With increasing HF concentration and the addition of etching acceleration solutions, the ELO time was significantly reduced down to approximately 20 min. When comparing to that of other study with a channel release of 110 min, the ELO time achieved in this study was quite short [18]. These results strongly suggest that a pre-patterning step and the addition of etching acceleration solutions facilitate high-throughput III-V/Si wafer

fabrication. As a result, simply, we would be able to regard the enhancement factor of the pre-patterning and the insertion of the solution as $5\times$ (30 hours/6 hours) and $18\times$ (6 hours/20 min), respectively. Fig. 30b shows the photograph of successfully transferred GaAs thin film on Si substrate with $1 \times 1 \text{ cm}^2$. In this scanning electron microscope (SEM), GaAs islands were well bonded to Si substrate without visible degradation. Next, the wafer size dependence was investigated for our ELO process. Although slight run-to-run variations were observed in our experiments, the ELO time was almost constant with increasing the wafer size as depicted in Fig. 30c, whereas a typical ELO process requires an exponential increase in the processing time with increasing the wafer size. The pre-patterned mesas promote the flowing of etching solutions during the chemical reactions. Further ELO time reduction will be possible by making mesa pattern with longer perimeter and also using the solution circulation and/or vapor phase etching scheme, which is typically used in micro electro mechanical systems (MEMS) technology to promote an etchant flowing [19].

However, it is noted that discrepancy for ELO time versus contact angle regarding the hydrophilic solutions as expected. Although contact angle of HF:IPA was shown as the lowest value, HF:ACE recorded the fastest ELO time in this experiment. To understand the physical origin of the effect of the etching acceleration solutions, we measured the residue thickness via an ellipsometry measurement after the immersion of the samples in various solutions. The measurement was conducted after 6 hours of immersion in each solution. In many studies, the residues, during the ELO process was known to be the reaction barrier for a succeeding lateral etching, because it makes solution flowing difficult [8-10]. Consistently, with the results of the

ELO time, the residue thickness decreases in the order of HF:DIW>HF:IPA>HF:ACE as shown in Fig.30d. Various residue thicknesses can be associated with kinematic viscosity of hydrophilic solutions. Because kinematic viscosity is defined as a fluid's resistance to flow, a high kinematic viscosity means high resistance to flow. Fig.30e exhibited kinematic viscosity of water, IPA and ACE [20]. While water and ACE solutions have approximately $1 \times 10^{-6} \text{ m}^2/\text{s}$ and $4.1 \times 10^{-7} \text{ m}^2/\text{s}$ respectively, IPA shows relatively high value of $4.2 \times 10^{-6} \text{ m}^2/\text{s}$. Kinematic viscosity of IPA is 10 times higher than that of ACE. Therefore, HF: IPA solution cannot suppress the re-deposited byproducts on surface which induced the longer ELO time than HF: ACE. Fig.30f summarized the characteristics such as contact angle and kinematic viscosity of different solutions. When we select adding solutions to HF etchant, both contact angle and kinematic viscosity should be considered. The optimum condition for both aspects would be low values since it can result in high HF diffusion to etch interfaces and suppression of re-deposited byproducts on an opening region.

etching solution dependence of the residue thickness, e) kinematic viscosity of hydrophilic substances, f) the trade off relationship of different properties.

Here, it is an important issue in our technology to investigate the dependence of the size of the transferred structure. Figure.31 showed ELO time of various dimensions ranging from 40 μm to 400 μm with fixed 100 μm spacing. ELO time was measured with same condition as mentioned above. While a sample with 400 μm dimension showed the approximately 70 minutes, ELO time was significantly reduced in 5 minutes for the sample with 40 μm dimension. In SEM images of samples, GaAs islands were clearly transferred on Si substrate. An experiment for spacing variation with fixed dimension of 40 μm was conducted for minimizing ELO time as illustrated in Figure.32. When Spacing of channels ranged from 10 μm to 100 μm , all samples resulted in approximately 5 minutes of ELO time. Also, SEM images showed the successful transfer of GaAs thin film regardless of channel spacing. In this experiment, significant ELO time reduction was obtained with a decrease of the mesa size due to an increased exposed surface area, whereas there was almost no spacing dependence of the ELO time, indicating that more dense packing will be possible by choosing appropriate mesa and spacing size.

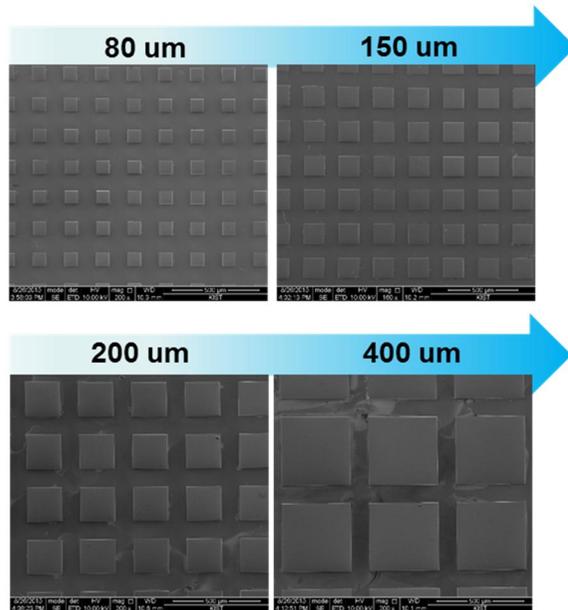
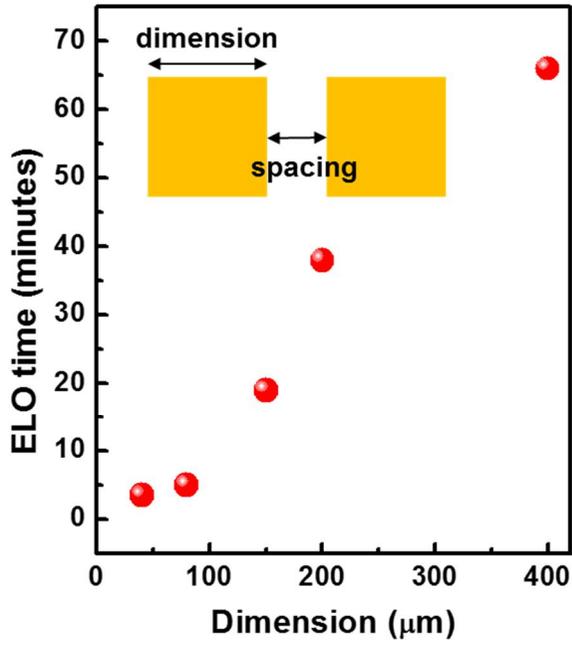


Figure 31 ELO time in terms of dimension variation (top), SEM images of formed GaAs on Si (bottom).

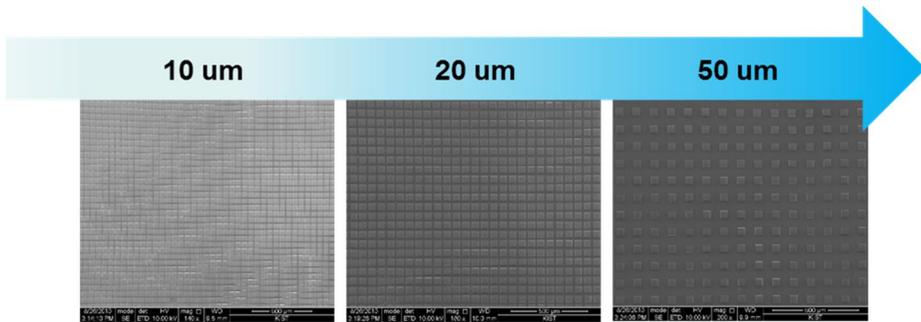
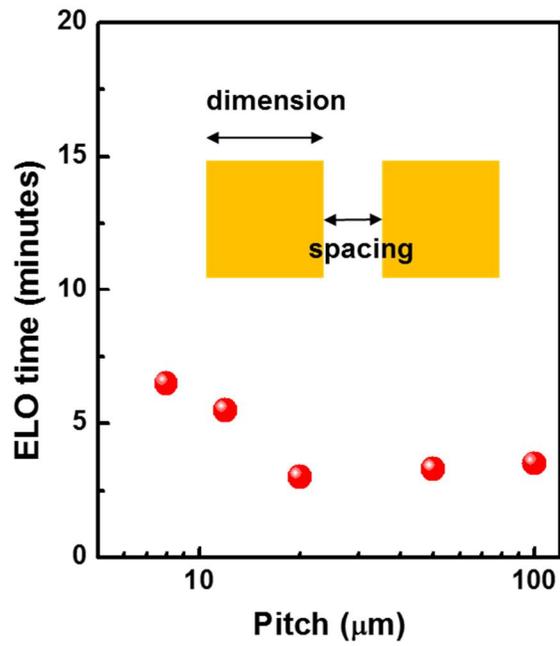


Figure 32 ELO time in terms of spacing variation (top), SEM images of formed GaAs on Si (bottom).

2.3 Summary

In this chapter. 2, we have developed the high throughput ELO process based on wafer bonding and epitaxial lift off process to overcome the limits of conventional ELO including low throughput and a direct transfer onto rigid substrates. Here, we have introduced the pre-patterning process and surface hydrophilization which resulted in a notable improvement of ELO time within 30 minutes. It is the fastest ELO time which ever reported. Also, through investigating a dependency of a dimension and spacing, ELO time was significantly reduced to 5 minutes. Additionally, the yield of the high throughput ELO process recorded approximately 95 % in all experiments. It can be attributed the high quality wafer bonding process with little voids and good uniformity in spite of room temperature process. Therefore, these results would be significantly meaningful to transfer the thin films on rigid substrates in large scale.

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Chapter. 3 Verification of thin film devices by using a high throughput heterogeneous integration method

3.1 Introduction

Recently, high-quality heterogeneous integration methods based on wafer bonding have been rapidly developed by many research groups, with the successful production of high-quality III-V films on foreign substrates [1-6]. However, in many cases, these demonstrations are only feasibility studies, because they involve etching of an entire donor substrate after the heterogeneous integration. Such etching is extremely costly and cannot be directly used in a mass-production process. Several trials to re-use the donor wafer via hydrogen-induced wafer splitting have been conducted; however, this approach leaves many defects in the III-V film, which is harmful to device reliability [3, 7]. While epitaxial lift off technology was emerged instead of previous methods, low throughput originating from long ELO time would be a main bottleneck to fully utilize the potential of III-V compound semiconductor.

To circumvent these issues, high throughput ELO process was developed and demonstrated in chapter. 2. To verify feasibility of developed method for electronic and optoelectronic devices, we have investigated actual devices including high electron mobility transistors, photovoltaic cells, heterojunction phototransistors and array of photodetectors on Si substrates. Next, in order to evaluate the transferred epitaxial layer quality, a variety of

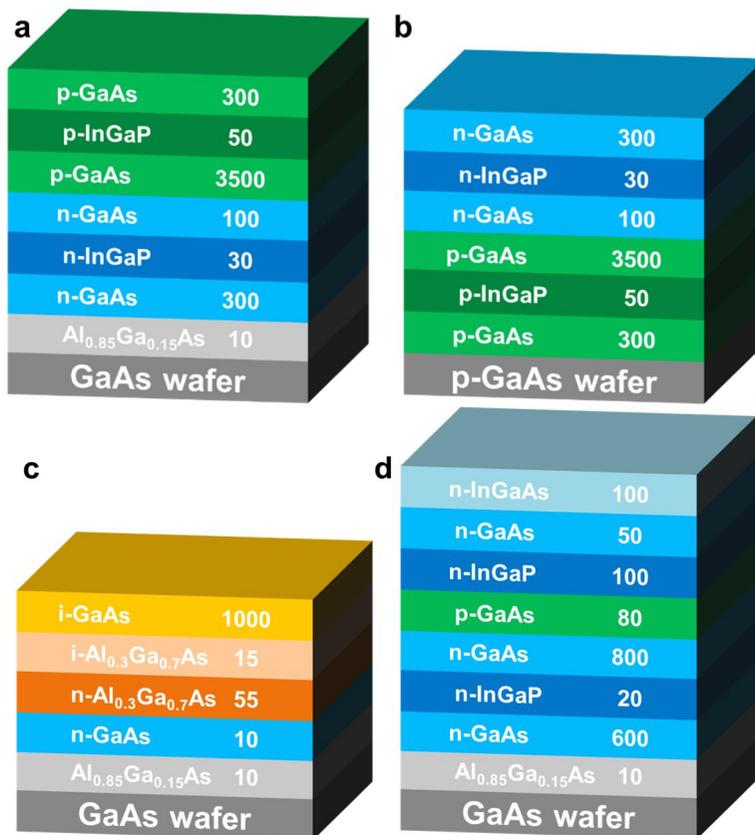
measurements were carried out. Finally, a wafer reusability which can reduce total cost was investigated in this chapter 3.

3.2 Growth of device structures and heterogeneous integration

3.2.1. Device structures

A 2-inch GaAs wafer (001) was prepared for an epitaxial growth for all experiments as shown in Figure. 33. The epitaxial layers of the GaAs HEMTs and InGaP/GaAs HPTs were grown by solid source molecular beam epitaxy (MBE) with the use of Si and Be cell as sources of n- and p-type dopants. GaAs HEMTs were composed of an n-type contact layer, an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ barrier layer, and a GaAs channel layer. InGaP/GaAs HPTs were composed of an n-type GaAs collector contact layer, an n-type InGaP etch stop layer, an n-type GaAs collector, a p-type GaAs base, an n-type InGaP emitter, an n-type InGaP subemitter, an n-type GaAs emitter contact layer, and an n-type InGaAs capping layer. GaAs p-i-n photodetectors consisted of AlAs sacrificial layer/ n+GaAs layer /intrinsic GaAs absorption layer /p+ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer /p+GaAs layer from the top to bottom. The epitaxial layers of GaAs solar cells were grown by metal-organic chemical vapour deposition (MOCVD) with AsH_3 , PH_3 , TMGa, TMIn, and TMAI as the precursors. SiH_4 and DMZn were used for n- and p-type dopants. The GaAs solar cells were composed of a p-type GaAs contact layer, and a p-type InGaP back surface field layer, a p-type GaAs base, an n-type GaAs emitter, an n-type GaAs window layer, and n-type GaAs contact layer. For the ELO process, an $\text{Al}_{0.85}\text{Ga}_{0.15}\text{As}$ sacrificial layer was inserted between the device layer and the GaAs donor wafer. Optionally, an etch stop layer of

InGaP/GaAs was also inserted between the $\text{Al}_{0.85}\text{Ga}_{0.15}\text{As}$ layer and the device layer and also between the $\text{Al}_{0.85}\text{Ga}_{0.15}\text{As}$ layer and the GaAs donor wafer. To check the quality of the epitaxial film, Hall measurement was carried out with $0.7 \times 0.7 \text{ cm}^2$ pieces at 0.55 T magnetic field using HMS 3000 system, Ecopia. During the measurement, no bias gating was applied.



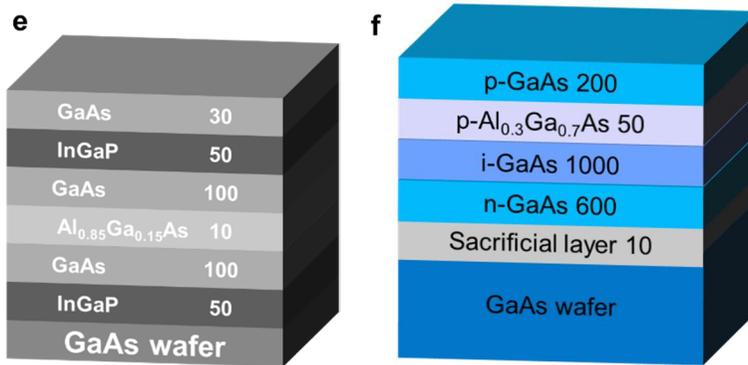


Figure 33 the epitaxial structures of the III-V layers used in this study.

- a) schematic epitaxial structure of the inverted GaAs solar cell for the ELO,
- b) schematic epitaxial structure of the GaAs solar cell on GaAs (control),
- c) schematic epitaxial structure of the inverted GaAs HEMT for the ELO,
- d) schematic epitaxial structure of the inverted the InGaP/GaAs HPT for the ELO,
- e) schematic epitaxial structure for the ELO with a double etch stop layers. The layer thickness is shown in the right side in each layer with nm scale,
- f) schematic epitaxial structure of the p-i-n photodetector for the ELO

3.2.2. Wafer bonding and ELO

The wafer bonding and ELO processes were carried out following the process flow shown in Figure 34. Here, two types of a bonding material are shown. Fig. 34a, 34b show the case of Y_2O_3 and Pt/Au as a bonding material, respectively.

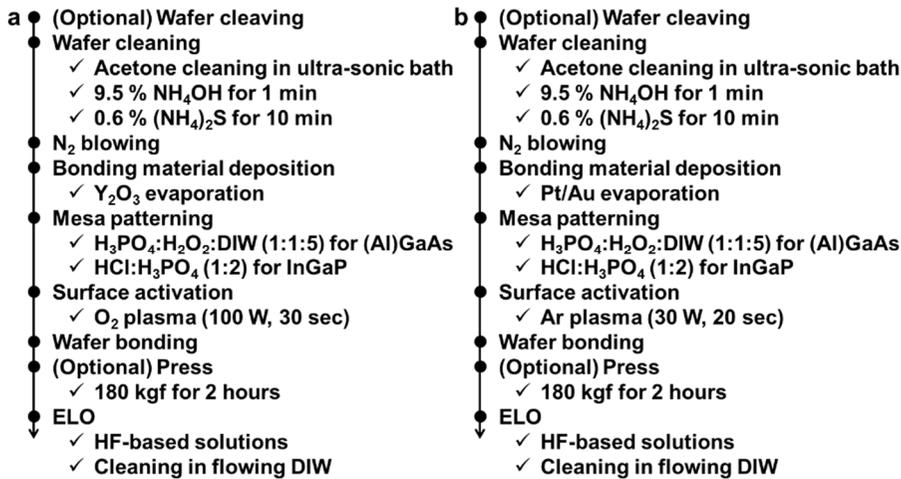


Figure 34 process flow of the wafer bonding and ELO process. a) process details of the wafer bonding and ELO with Y₂O₃ as a bonding material, b) process details of the wafer bonding and ELO with Pt/Au as a bonding material.

3.3 Y₂O₃ bonded HEMTs on Si substrate

3.3.1 Fabrication process

After a heterogeneous integration, fabrication process was started as shown in Figure 35. Mesa etching was performed using a H₃PO₄-based solution, followed by Y₂O₃ field-oxide deposition. source/drain contacts were formed by Pd/Ge/Au deposition and rapid thermal annealing (RTA) at 150°C for 3 hours. Next, the contact layer was selectively etched by citric acid:H₂O₂ (3:1 volume ratio) solutions for the gate electrode formation. Finally, the gate electrode of Ti/Pt/Au was deposited. . Through the back-gate of Si, device characteristics can be controlled after the device fabrication. Each device was

characterized using a semiconductor parameter analyzer (Hewlett Packard, 4156A) in the dark.

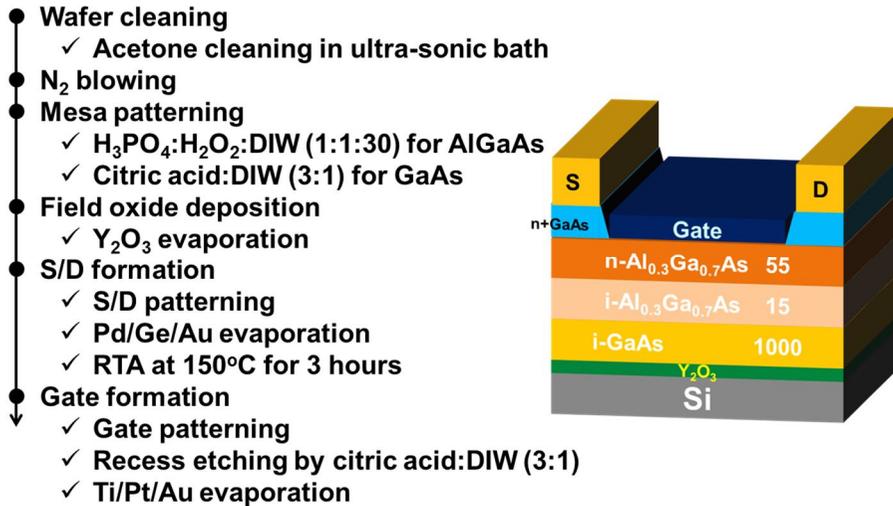


Figure 35 GaAs HEMT on Si. Process details for the fabrication of the GaAs HEMTs on Si.

3.3.2. Material characterization of HEMTs on Si

Figure 36a shows the infrared (IR) photograph of GaAs on insulator (-OI) on a Si wafer after the wafer bonding with a pre-patterning step. Here, Y₂O₃ was used as the bonding material [8]. Clear bonding behaviors were observed in the IR image over the 2-inch full wafer scale. The top-side view of the scanning electron microscopy (SEM) image of the GaAs/Si wafer after the ELO is shown in Fig. 36b. The image confirmed that the GaAs pattern arrays were bonded onto the Si wafer with the same shape as defined in the pre-

patterning step. A cross-sectional transmission electron microscopy (TEM) image in Fig. 36c reveals that the GaAs high electron mobility transistors (HEMTs) was bonded onto the Si with good uniformity and without any voids at the bonding interface. Here, the active layer for GaAs HEMT was considered; however, this approach is not limited to HEMT devices and can be expanded to any possible set of active layers. Energy dispersive x-ray (EDAX) spectroscopy in Fig. 36d shows the abrupt interfaces between GaAs, Y_2O_3 , and Si. Fig. 36e and 36f depict the transmission electron diffraction patterns in the bonded GaAs and the Si, respectively. The patterns show that both GaAs and Si are single crystals in structure, and crystalline structures of the bonded III-V layer were maintained during the wafer bonding and ELO process. Also, from the lattice spacing (d), the lattice constant of GaAs and Si was well-matched to the crystallographic data of GaAs and Si, respectively.

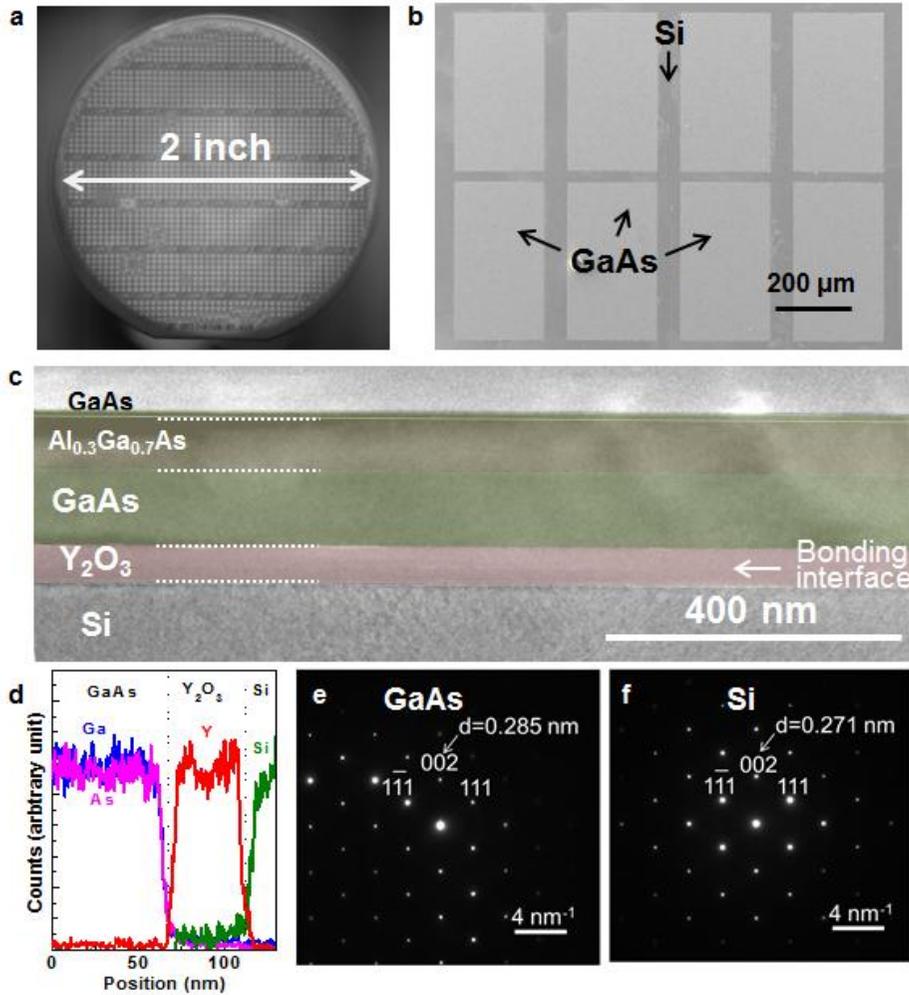


Figure 36 GaAs-OI on a Si substrate via the wafer bonding and ELO processes. a) IR image of a GaAs-OI on Si sample after the wafer bonding. Patterned GaAs arrays were securely bonded onto the Si substrate, b) typical SEM image of a GaAs-OI on Si sample. GaAs pattern arrays are formed on the Si substrate, c) Cross-sectional TEM image of a GaAs-OI on Si sample, showing uniform GaAs HEMT layers on Si. The GaAs HEMT is composed

of a GaAs contact layer, an Al_{0.3}Ga_{0.7}As barrier layer, and a GaAs channel layer, d) EDAX profiles for Ga (blue), As (pink), Y (red), and Si (Green) evaluated along the fabricated substrate, e) TED pattern of GaAs region, f) TED pattern of Si region.

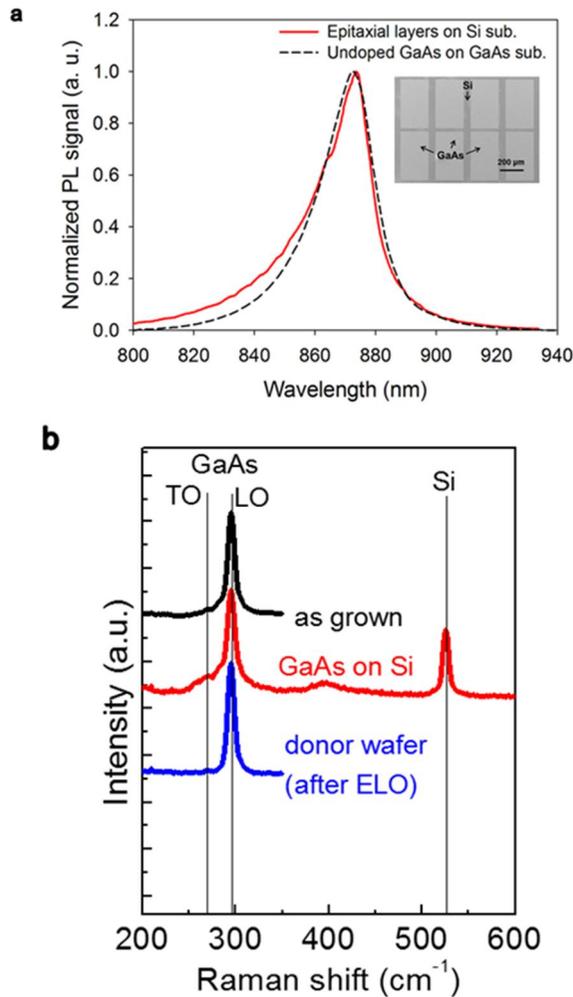


Figure 37 a) PL spectra and b) Raman spectra for comparison of transferred GaAs thin film quality

To evaluate the transferred epitaxial layer qualities, we carried out optical characterizations such as μ -photoluminescence (μ -PL) setup and Raman spectroscopy. From these measurements, we could obtain the state of strain and defects for epitaxial layer. Figure 37a showed a position of normalized PL peak wavelength and full-width-half-maximum (FWHM) of the both samples were almost same as around 873 and 21 nm which indicated that the quality of transferred GaAs layer were similar to GaAs epitaxially grown layer. Raman spectra for three samples of as-grown HEMTs, HEMTs on Si and separated donor wafer were shown in Fig.37b. The FWHM of samples were also constant after ELO process which revealed the layer quality is not deteriorated during ELO process. Moreover, negligible Raman peak shift of GaAs on Si sample was observed which indicated there was no strain. These results strongly indicate that the wafer bonding and ELO techniques produced a high-quality III-V layer on the Si substrate.

3.3.3. Electrical characterization of HEMTs on Si

Figure 38a, 38b shows schematic and optical image of fabricated HEMT device on Si substrate. Top gate of HEMT was not formed yet as shown in optical image. The typical drain current (I_D)-gate voltage (V_G) characteristics of the reference HEMT and GaAs-OI HEMT with a gate length (L_G) of 2 μm as illustrated in Fig. 38c, 38d. Clear transfer curves were obtained with a steep subthreshold slope ($S.S. = dV_G/d[\log(I_D)]$) of 83 mV per decade and high on/off ratio ($I_{\text{on}}/I_{\text{off}}$) of 10^7 . To the best of our knowledge, the achieved $S.S.$ and $I_{\text{on}}/I_{\text{off}}$ are record values among the reported III-V-OI transistors [3-

6]. In addition, I_{off} was found to be a very low value of $< 1 \text{ pA}/\mu\text{m}$, which is lower than that required for an ultra-low power (ULP) transistor ($10 \text{ pA}/\mu\text{m}$) by the International technology roadmap for semiconductors (ITRS). The clear current saturation was also observed in the I_{D} -drain voltage (V_{D}) characteristics in Fig. 38e. From the structural specialty of having a back-gate structure through the Y_2O_3 insulating film, the electrical properties of the fabricated GaAs-OI HEMT can be modulated by the biasing of the back gate (V_{B}) of the Si substrate. Since GaAs channel layer and underlying Si substrate are electrically isolated, a channel potential can be modulated via V_{B} biasing without a leakage current. Fig.38f shows the $I_{\text{D}}-V_{\text{G}}$ curves with changing V_{B} from 0.5 to -0.5 V. The $I_{\text{D}}-V_{\text{G}}$ curves were intentionally shifted with changing V_{B} , indicating that the device characteristics can be controlled after the device fabrication, which provides additional functionality for a circuit design.

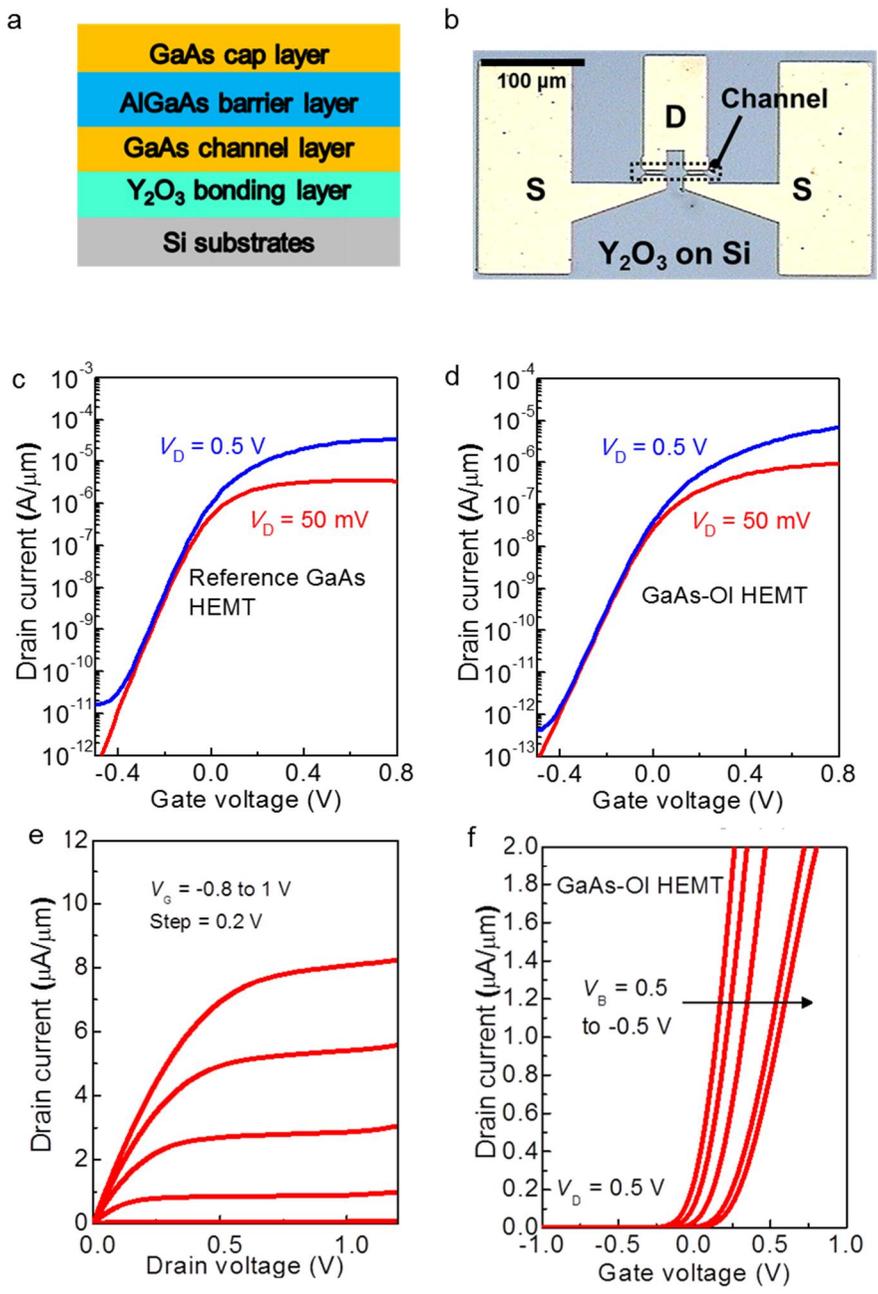


Figure 38 Performance of the GaAs-OI HEMTs and wafer re-usability after

the ELO process. a) schematic of fabricated GaAs-OI HEMTs on Si substrate, b) optical image of GaAs-OI HEMTs with source/drain formation, c) and d) measured transfer characteristics of a reference HEMT and GaAs-OI HEMT with a L_G of 2 μm . The device exhibits a quite low S.S. of 83 mV per decade, which is close to the theoretical limit of 60 mV per decade at room temperature, e) Output characteristics of the same device shown in a, showing clear current saturation, f) I_D - V_G curves for different V_B ; the electrical characteristics of the GaAs-OI HEMT can be controlled by V_B after the device fabrication.

3.3.4. Investigation of wafer reusability by using HEMT structure

Figure 39 shows the surface morphology of the GaAs surface at each of the process steps characterized using atomic force microscopy (AFM). A bare epi-ready GaAs wafer shows a flat surface with a root mean square roughness (R_{rms}) of 0.16 nm. After the ELO process, the R_{rms} of the surface was increased up to 2.52 nm and etching residues with dot shapes were observed over the entire wafer. After the cleaning using HCl and the etching of the etch stop layer, the AFM images illustrate the excellent surface morphology that is comparable to that of the epi-ready surface. The AFM image of the surface after re-growing the GaAs layer confirmed a high process stability with a flat and smooth surface.

To investigate the layer quality and the possible strain in the regrowth HEMT, we collected Raman spectra for all samples, as shown in Figure. 40a.

Even after the re-growth on the donor wafer formerly used in the ELO process, the Raman spectra was still sharp and no strain was observed in the re-grown layer. However, the Raman spectra after re-growth seems to be broader than that of the initially grown GaAs layer, indicating the crystal quality of re-grown GaAs layer seems to be not perfect. It is possibly because that the surface treatment including wet and thermal treatment before the regrowth has not been optimized, whereas surface chemistry strongly impacts the crystal quality of III-V films [9, 10].

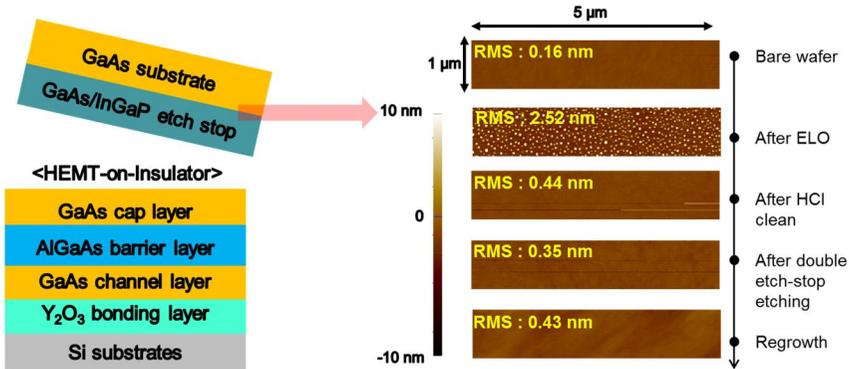


Figure 39 AFM image for wafer reusability with process steps.

Even though the re-grown GaAs layer on the donor wafer after the ELO process was evaluated by AFM and Raman spectra, these results do not guarantee the re-use of the donor wafer because these measurements do not fully reflect the epitaxial quality. Here, the best way to show the wafer-reusability is to fabricate and compare each types of device. However, for the simple examination, Hall mobility is the one of the best figure-of-merit to evaluate the crystal quality of grown epitaxial film, which is typically used to check/confirm the status of the growth chamber. Therefore, we have

investigated the electrical properties of re-grown HEMTs. Fig. 40b shows the Hall mobility and charge carrier density (N_s) of fresh and re-grown GaAs HEMTs at 80 K and 300 K. Hall measurement was carried out with 0.7×0.7 cm² pieces at 0.55 T magnetic field using HMS 3000 system, Ecopia. During the measurement, no bias gating was applied. The mobility and N_s behaviors were almost the same between the two sets of devices, which indicates the high quality of the re-grown GaAs HEMT layer, whereas the Raman spectra was slightly broader. These results strongly suggest that the epi-ready surface of the GaAs donor wafer can be recovered after the ELO process, thereby enabling the donor wafer to be re-used at least once. Further development will be expected via the optimization of the surface treatment condition before the re-growth with a quality evaluation by the Raman spectra, Hall mobility, and each device performance.

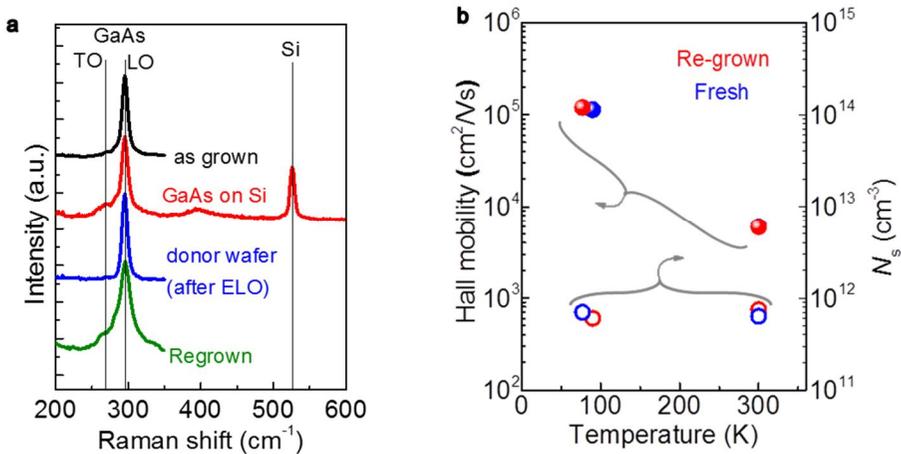


Figure 40 a) Raman spectra for as-grown, GaAs-OI HEMTs, donor wafer and regrown HEMT structure, b) comparison of Hall measurement results for HEMT structure using fresh and re-used substrate.

3.4 Pt/Au bonded optoelectronic devices

3.4.1. Fabrication process of solar cells and HPTs on Si

The GaAs solar cells were fabricated with the process shown in Fig. 41. After the wafer bonding with a Pt/Au bonding material, the Pt/Au layer acted as a bottom electrode for the GaAs solar cells. Because GaAs and Si substrate were electrically conductive unlike the case of using Y_2O_3 bonding material. The top electrode of Ni/Au/Ge/Ni/Au was deposited, followed by RTA at $400^\circ C$ for 40 sec. Next, the n-type GaAs contact layer was selectively etched using H_3PO_4 -based solutions through the top electrode as a mask. Each device was characterized using a solar simulator (McScience, XES-301S), IPCE (McScience, K3100 Spectral IPCE Measurement system). Figure S5 also shows the final schematic device structure. Here, device isolation process by the mesa etching could be skipped due to the use of the ELO with a pre-patterning.

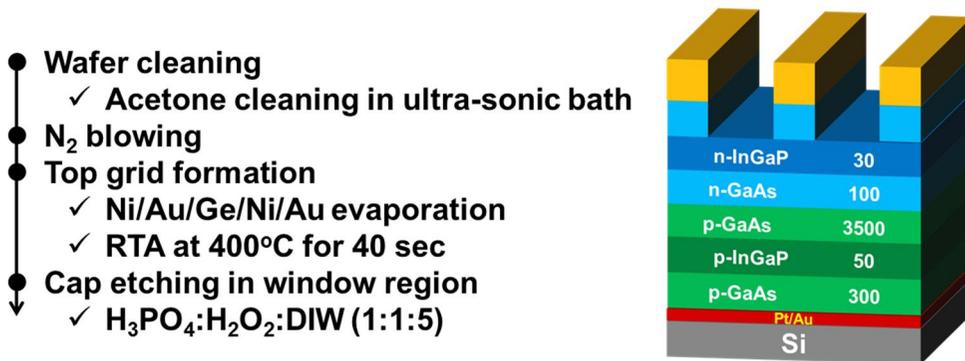


Figure 41 GaAs solar cell on Si. Process details for the fabrication of the GaAs solar cells on Si

The InGaP/GaAs HPTs were fabricated with the process shown in Fig. 21. Similar to the GaAs solar cells, the Pt/Au layer acted as an emitter electrode (located at the bottom) after the ELO process. The top electrode of Ni/Au/Ge/Ni/Au was deposited, followed by RTA at 400 °C for 40 sec. Next, the n-type GaAs collector contact layer was selectively etched using H₃PO₄-based solutions through the top electrode as a mask. The optical performances of the fabricated devices were characterized utilizing a 635-nm laser diode and a semiconductor parameter analyser (Hewlett Packard, 4156A). For laser power calibration, the incident optical power through a lensed fiber was measured using an optical meter (Newport, 1835-C) equipped with a silicon photodetector (Newport, 818-UV/DB) in the dark. Figure 42 also shows the final schematic device structure. Metal of Pt/Au used as a bonding material also roles as a back mirror for the photon recycling.

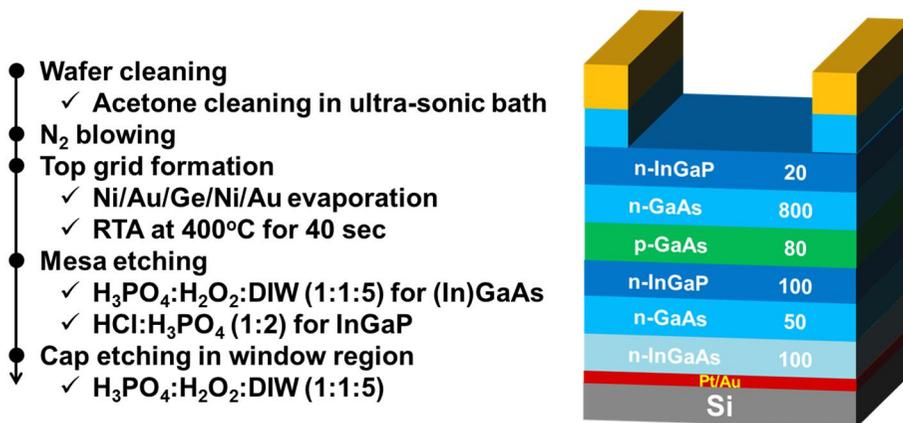


Figure 42 InGaP/GaAs HPT on Si. Process details for the fabrication of the InGaP/GaAs HPT on Si

3.4.2. Evaluation of Pt/Au metal bonding

For optoelectronic devices, we demonstrated GaAs single-junction solar cells and InGaP/GaAs HPTs on Si substrate. We carried out heterogeneous integration of 2inch GaAs based solar cells on 4inch Si substrate. Figure 43 shows the photograph of integrated structures with Pt/Au bonding. Although there are some failed regions due to particles, wafer edge and etc, this process exhibited the above 95% yield in room temperature bonding and imperfect clean room environment considering the original donor wafer observed in inset figure. Array of solar cells is well formed on Si substrate in SEM image.

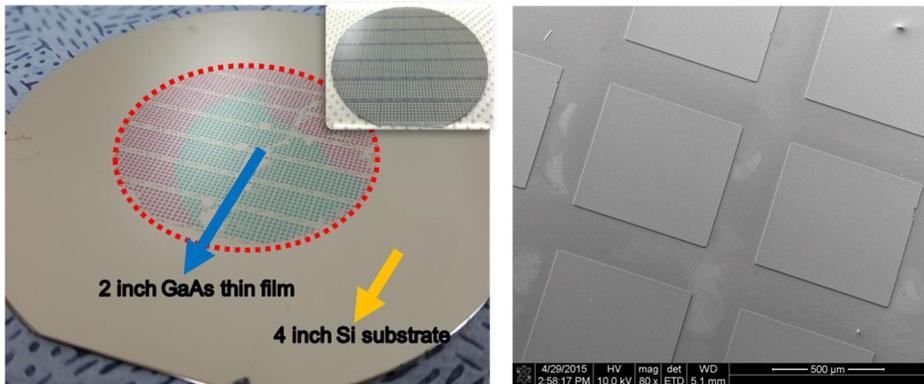


Figure 43 photograph and SEM image of 2 inch GaAs thin film transferred on 4 inch Si substrate with Pt/Au metal bonding layer

To clarify the quality of Pt/Au based metal bonding, AFM and TEM analysis were carried out for these integrated structure as illustrated in Figure 44. While Fig. 44a depicted the AFM image for Pt/Au metals on top surface of GaAs solar cells before wafer bonding, Fig. 44b shows top surface of

GaAs solar cells after ELO process. The rms roughness of both surfaces was found to be below 0.3 nm which indicated that an initial bonding condition and ELO process are highly stable and appropriate. Additionally, TEM analysis of a Pt/Au bonded interface was conducted as shown in Fig. 43c. GaAs was well bonded to Si substrate with Pt/Au intermediate layer. However, at Au-Au interface, a thin amorphous layer was formed in spite of expedite wafer bonding process. It can be caused by ex-situ bonding process in air environment. However, it was found that device characteristics would not be degraded from our previous study (ref, solar energy material direct bonding).

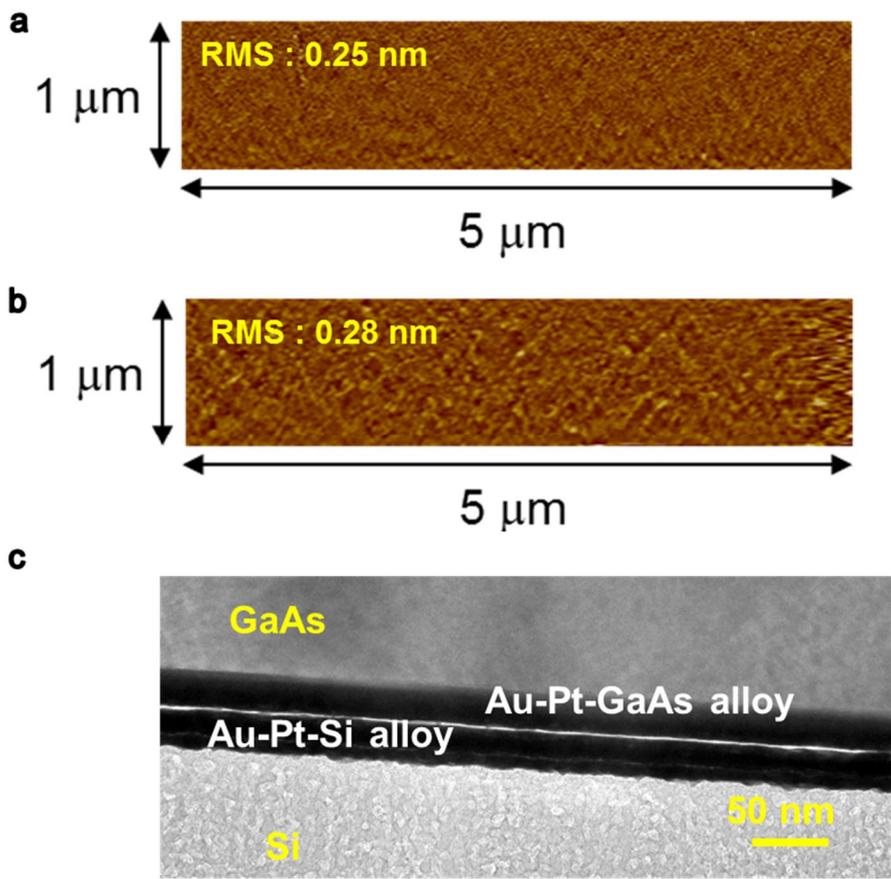


Figure 44 a) AFM image of Pt/Au surface deposited on GaAs solar cells, b) AFM image of GaAs solar cell on Si substrate after ELO process, c) TEM image of GaAs/Pt/Au/Au/Pt/Si structure with an interfacial layer

3.4.3. Characterization of solar cells and HPTs

Here, we fabricated micrometer-scale solar cells, as shown in the inset of Figure 45a, which is suitable for the developed ELO process in this study. One cell was defined as a pre-patterned mesa before the wafer bonding process, resulting in process simplification by using the pre-patterned mesa for the device isolation. One concern of the use of our ELO method for solar cell fabrication is the limitation of the size of devices for the large-scale solar panel. After forming solar cell arrays on the Si, an electrical connection of each cell arrays through the metal contact on the pre-patterned mesa spacing will be efficient way for the scale-up of the panel size [11, 12]. Placing the metal contacts on the pre-patterned mesa spacing, additional space penalty can be released.

Fig. 45a shows the current density (J) – V curves of the GaAs solar cell on Si under air mass (AM) 1.5 G, 1-sun measurement conditions. As a control device, the data of a GaAs solar cell grown on GaAs is also shown. Even considering approximately 30 % reflection of the incident light due to the absence of an anti-reflection coating, the energy conversion efficiency (η) and the open-circuit voltage (V_{oc}) of the solar cell on Si was as high as 14.05 % and 0.89 V, respectively. The performance of the solar cell on Si was almost same as that of the control device with an even higher short-circuit current (J_{sc}). The external quantum efficiency (EQE) of both devices in Fig. 45b shows no substantial difference, whereas J_{sc} value is different between the two. We believe that light reflection from the back side enhances photo recycling of the light once reached to the back-side, leads to higher J_{sc} in the

solar cell on Si. However, since the intensity of an incident light to the sample was very small in EQE measurement, the data could not catch the light response reflected from back side metal. These results strongly suggest that the developed wafer bonding and ultra-fast ELO techniques provide a high-quality III-V film on Si substrate without material degradation during these processes.

GaAs HPTs on Si were also fabricated using similar procedures. After growing an epitaxial layer comprising a GaAs collector, a GaAs base, and an InGaP emitter, the III-V and Si wafers were bonded to each other using a Pt/Au bonding layer, followed by the ELO. Next, the fabrication of HPTs was completed with the steps of the ohmic metallization (Ni/Au/Ge/Ni/Au) for the collector and the mesa etching. Fig. 45c shows the collector dark current (I_C^{dark}) and the collector photocurrent (I_C^{ph}) characteristics of a fabricated InGaP/GaAs HPT on Si as a function of the bias voltage across the collector and the emitter (V_{CE}). I_C^{ph} was measured with an incident optical power (P_{in}) of 1.2 μ W at a wavelength of 635 nm. The data from the HPTs fabricated by both the developed ultra-fast ELO and the conventional ELO without the pre-patterning and accelerant addition are shown. For both devices, I_C^{dark} was very low, with a value down to approximately 10^{-13} A over the entire V_{CE} range. This low I_{Cdark} confirms the defect-free crystal quality after the wafer bonding and ELO processes. In contrast to the I_C^{dark} characteristics, the I_C^{ph} characteristics were quite different between the two devices. At a high bias condition of $V_{CE} > 0.25$ V, I_C^{ph} of the HPT

fabricated using the ultra-fast ELO process was almost twice as high as that of the HPT fabricated using the conventional ELO process. This difference is attributed to the small amount of etching residues for the ultra-fast ELO process, which enables a lower contact resistance of the collector contact. Fig. 45d shows the optical gain ($G_{\text{opt}} = h\nu\Delta I_c/qP_{\text{in}}$, where $h\nu$ and ΔI_c are the incident photon energy and the difference between I_C^{ph} and I_C^{dark} , respectively) of the two devices. As estimated from the I_C^{ph} characteristics, the G_{opt} of the HPT fabricated using the ultra-fast ELO process shows higher values, demonstrating another benefit of the developed ELO process besides the time reduction. Furthermore, array formation with each HPTs using the developed process can be expanded to the focal plane array for the high resolution and wide angle detectors [13, 14].

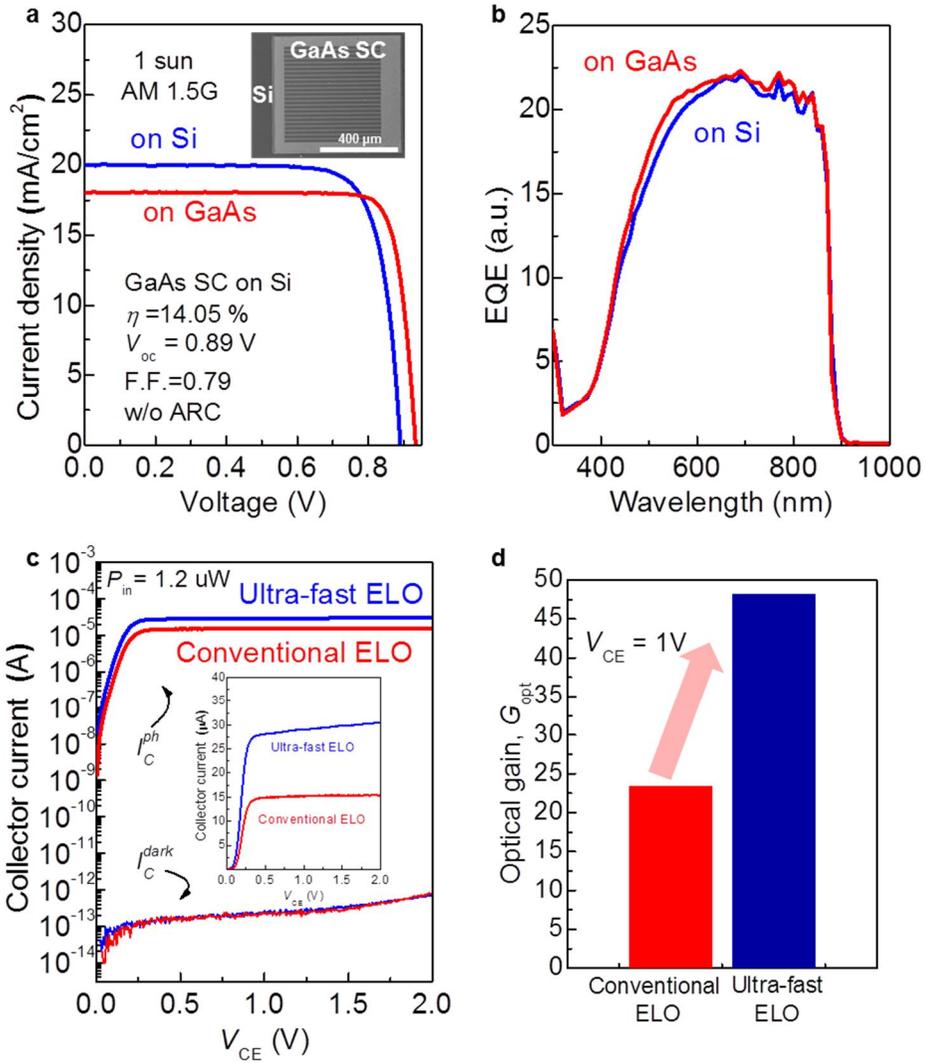


Figure 45 GaAs solar cells and InGaP/GaAs HPTs on Si, a) J - V characteristics of the GaAs solar cell on Si (blue) and GaAs (red, control) under AM 1.5 G, 1-sun measurement condition. The inset is a top view SEM image showing the fabricated GaAs solar cell on Si, b) EQE spectra of the GaAs solar cell on Si (blue) and GaAs (red), c) I_{Cdark} and I_{Cph} characteristics

of the InGaP/GaAs HPT on Si as a function of VCE, d) Incident optical power dependence of the G_{opt} of the same device shown in c.

3.5 Estimation of production cost via recycling III-V wafers

To examine the cost efficiency of our transfer approach, we calculated the expected cost reduction comparing to conventional wafer bonding/donor wafer etching and selective growth (aspect ratio trapping (ART)) approach.

First, we assumed that the total cost (C_t) is composed of the wafer cost (C_{wafer}), the system cost (C_{system}), and the material cost ($C_{material}$).

$$C_t = C_{wafer} + C_{system} + C_{material}$$

To estimate the cost and throughput of III-V/Si wafer using our wafer bonding and ELO techniques, we defined parameters as follows :

T_{lo} : Time to load and unload a substrate in the growth chamber (min)

T_{act} : Time to grow an active layer (min)

T_{sac} : Time to grow a sacrificial layer (min)

T_{buffer} : Time to grow a buffer layer (min)

T_{etch} : Time to etch all donor substrate (min)

T_{elo} : Time to complete ELO process (min)

R_{op} : Running operation cost per time (\$/h)

C_{act} : Cost of source materials to grow an active layer (\$)

C_{sac} : Cost of source materials to grow a sacrificial layer (\$)

C_{buffer} : Cost of source materials to grow a sacrificial layer (\$)

C_{donor} : Cost of a GaAs donor wafer (\$)

C_{sil} : Cost of a Si substrate for layer transfer (\$)

$C_{\text{re-use}}$: Cost of processing to re-use the donor wafer (\$)

N : Number of the production wafer

Here, we consider three kinds of integration method of III-V/Si, which are our approach of wafer bonding/ELO, the wafer bonding/donor wafer etching approach, and selective epitaxy approach (ART). To estimate the C_t to produce the same amount of wafers, we calculated the processing time of each approaches.

$$T_{\text{our}} \text{ (Time for our approach of wafer bonding /ELO)} = T_{\text{lo}} + T_{\text{act}} + T_{\text{sac}} + T_{\text{elo}}$$

$$T_{\text{con}} \text{ (Time for conventional approach of wafer bonding/etching)} = T_{\text{lo}} + T_{\text{act}} + T_{\text{sac}} + T_{\text{etch}}$$

$$T_{\text{ARC}} \text{ (Time for ART approach)} = T_{\text{lo}} + T_{\text{act}} + T_{\text{lo}} + T_{\text{buffer}}$$

Here, T_{ARC} include the double of T_{lo} . It is because that ARC approach needs chemical mechanical polishing between the growth of buffer layer and the growth of active layer [15]. Therefore, we assumed T_{ARC} need the double of T_{lo} . Then, C_{system} , C_{wafer} , and C_{material} can be expressed by following Table.5.

	Our approach	Conventional wafer bonding/donor wafer etching	ART
C_{system}	$T_{\text{our}} \times R_{\text{op}}$	$T_{\text{con}} \times R_{\text{op}}$	$T_{\text{ARC}} \times R_{\text{op}}$
C_{wafer}	$C_{\text{donor}} + (C_{\text{re-use}} + C_{\text{sil}}) \times N$	$(C_{\text{donor}} + C_{\text{sil}}) \times N$	$C_{\text{sil}} \times N$
C_{material}	$(C_{\text{act}} + C_{\text{sac}}) \times N$	$(C_{\text{act}} + C_{\text{sac}}) \times N$	$(C_{\text{act}} + C_{\text{buffer}}) \times N$

Table 5 the estimated equation of cost for different approaches

As the key parameters, we defined the time and cost as follows from Yoon *et al* [16].

$$T_{\text{lo}} = 60 \text{ min}$$

$$T_{\text{act}} = 1.67 \text{ min (thickness} = 100 \text{ nm, growth rate} \sim 1 \text{ nm/sec)}$$

$$T_{\text{sac}} = 0.17 \text{ min (thickness} = 10 \text{ nm)}$$

$$T_{\text{buffer}} = 2.5 \text{ min (thickness} = 150 \text{ nm)}$$

$$T_{\text{etch}} = 120 \text{ min (Etch rate} = 5 \text{ } \mu\text{m/min, wafer thickness} = 700 \text{ } \mu\text{m)}$$

$$T_{\text{elo}} = 20 \text{ min}$$

$$R_{\text{op}} = 125 \text{ \$/hour}$$

$$C_{\text{act}} = 0.21 \text{ \$ (GaAs } 100 \text{ nm, } 2.11 \text{ \$/}\mu\text{m)}$$

$$C_{\text{sac}} = 0.022 \text{ \$ (AlGaAs } 10 \text{ nm, } 2.20 \text{ \$/}\mu\text{m)}$$

$$C_{\text{buffer}} = 0.3165 \text{ \$ (} 150 \text{ nm, } 2.11 \text{ \$/}\mu\text{m)}$$

$$C_{\text{donor}} = 150 \text{ \$ (6 inch GaAs)}$$

$$C_{\text{sil}} = 10 \text{ \$ (6 inch Si)}$$

$$C_{\text{re-use}} = 10 \text{ \$}$$

With the parameters described above, we calculated the production cost using each integration approaches as shown in following Figure 46. Total production cost is shown in the left figure and the production cost per one wafer is shown in the right figure as a function of N. Even though cost benefit is not so high with small N, the cost benefit of our approach (wafer bonding and ELO) increases with increasing N. Even just for one wafer production, our approach is still economical comparing to the conventional wafer bonding/donor wafer etching approach due to the time reduction via developed ELO process. With increasing N, cost reduction is more efficient by reducing wafer cost via the re-use of the donor wafer. Even comparing to ART approach, our approach will be more economical at high N due to the processing time reduction and the cut of the wafer cost. At large N, cost reduction factor reaches 0.35 and 0.71 comparing to conventional wafer bonding/donor wafer etching approach and ART approach, respectively.

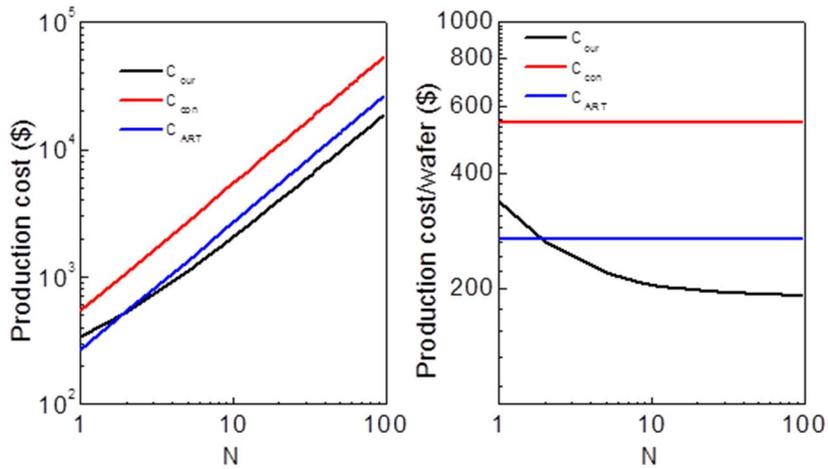


Figure 46 Estimation of the production cost III-V/Si wafer, a) Production cost as a function of N, b) Production cost per one wafer as a function of N.

Not only the cost reduction, there is one more significant benefit using our approach. Reciprocal value of T_{our} , T_{con} , T_{ARC} correspond to the throughput of each approach. Using our approach, 2.25 and 1.52 times higher production throughput can be achieved comparing to the conventional wafer bonding/donor wafer etching approach and ART approach, respectively.

Following Table.6 highlighted the enhancement factor of our approach. Through the cost reduction and throughput improvement, our approach provides the enhancement factor of about $7 \times$ and $2 \times$ comparing to the conventional wafer bonding/donor wafer etching approach and ART approach, respectively.

In our approach, further improvement is expected combining multilayer bonding technique shown from the Prof. Rogers group (J. Yoon *et al.*, Nature **465**, p. 329 (2010)) and multi wafer growth techniques using mass-

production CVD.

	Our approach	Conventional wafer bonding/donor wafer etching	ART
Cost factor (A)	1	2.83	1.40
Throughput increase factor (B)	1	0.44	0.67
Total enhancement factor (B/A)	1	0.15	0.48

Table 6 claulated enhancement factor of different approaches

3.6 Summary

In summary, we have demonstrated III-V based devices on Si substrates with different intermediate layers such as Y_2O_3 and Pt/Au by using a developed high throughput ELO process. The fabricated HEMTs on Si substrates showed a comparable performances with reference HEMTs grown on GaAs substrate. Furthermore, solar cells and HPTs on Si substrates in 2 inch scale were successfully fabricated which resulted in comparable performances without severe degradation compared with reference devices. Finally, donor wafer re-usability was also confirmed by using a HEMT structure after the ELO process. These results promise dramatic cost reduction in the production of high-quality III-V on Si structures, which expand the use of the III-V and extend the conventional Si-based semiconductor industry. Further combination with a multiple epitaxial transfer should be a strong component of technologies in the future III-V/Si device era [16].

3.7 Bibliography

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Chapter. 4 Design and characterization of III-V based photodetectors

4.1 Introduction

4.1.1. The potential of Indium arsenide antimonide (InAsSb)

For implementing III-V based multicolor photodetectors of our concept, design of short-wavelength top photodetector (PD) and long-wavelength bottom PD is significantly important. Combinations of PDs with different wavelengths can offer various functionalities of target applications. Among various wavelengths which can be integrated, infrared (IR) wavelength is one of many candidates. IR wavelength is determined as short-wavelength (SWIR, 1-3 μm), mid-wavelength IR (MWIR, 3-5 μm) and long-wavelength IR (LWIR, 8-12 μm) thanks to its low-loss transmission window in the atmosphere [1]. It is because IR wavelengths correspond to the blackbody radiation energy of jet engine has 800K blackbody radiation which emits MWIR region, LWIR matching to Human being with 300K blackbody radiation. By using these bands, thermal imaging applications have been used for surveillance system, defense and medical diagnosis for last decades [1, 2].

In many III-V based materials which can be integrated into multicolor PDs, the range from ultraviolet (UV) to SWIR can be covered by GaN, GaAs, InGaAs and InAs based p-i-n PDs. Beyond SWIR range, InSb based binary material has been conventionally utilized thanks to its small band gap of 0.17 eV at room temperature [3,29]. By using InSb PDs, to suppress excessive

thermally generated carriers caused from small band gap, Dewar should be required for low temperature operation. When InSb PD should be integrated to other wavelengths, the size of entire detector system is becoming large due to Dewar. Furthermore, another problem with this binary InSb is the limitation of wavelength expansion beyond MWIR. To simply integrate various PDs for compact system, procuring bulk layer based p-i-n PD with an ability to detect LWIR at high operating temperature is crucial.

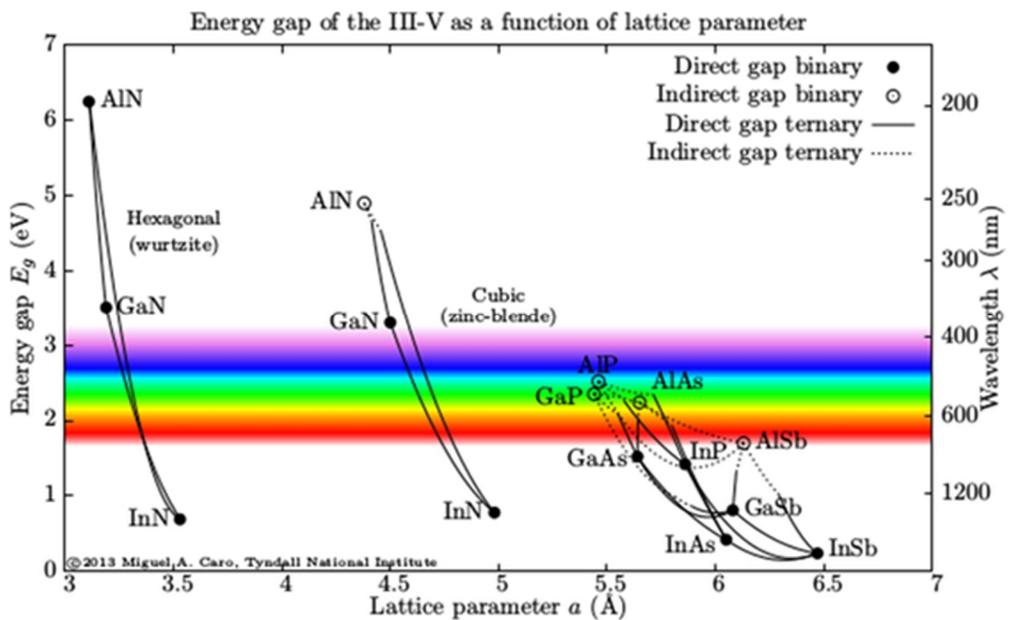


Figure 47 band gap and wavelength properties of III-V compound semiconductors as a function of lattice constants [4]

To solve these problems, $\text{InAs}_x\text{Sb}_{1-x}$ ternary material has recently been emerged from a point of materials. The band gap of InAsSb alloy can be changed with As to Sb ratio in V-group thanks to its unique property as shown Figure 47 [4]. This non-linear band gap bowing property plays an

important role to expand detection wavelengths from SWIR to LWIR. To confirm the change of band gap, wavelengths of InAsSb are calculated from the Vegard's law as following:

$$E_{g,InAs(x)Sb(1-x)} = xE_{g,InAs} + (1-x)E_{g,InSb} - bx(1-x)$$

b=bowing factor (curvature)

By using this Vegard's law, InAsSb band gap can be calculated according to As composition of V-group. Calculated values through changing band gap to wavelength were depicted in Figure 48. When As compositions are below 20% (above 80% of Sb), it is relatively lower than band gap of InSb. Above 30% of Sb composition, it can surpass a conventional wavelength of binary InSb limitation. Then, when As composition equals to Sb composition, it can be the longest wavelength of approximately 14 μm which suggests detection of LWIR range can be possible to implement bulk p-i-n based PDs without special technique such as type-II PD, QWIP and QDIP[5,6].

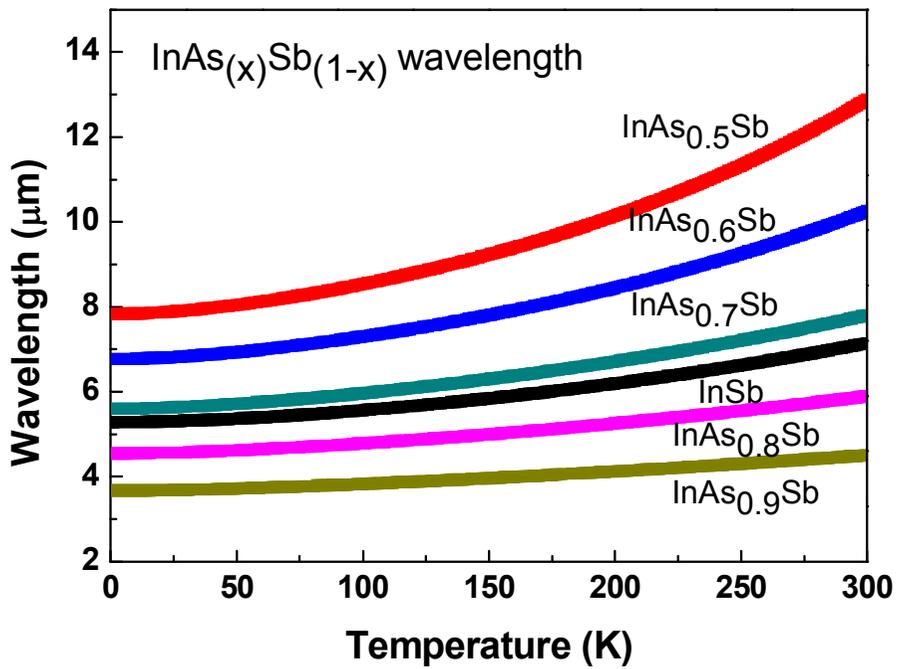


Figure 48 calculated InAs_xSb_{1-x} wavelengths as a function of temperatures with Vegard's law

4.1.2. Challenges of InAsSb p-i-n PDs for compact detector systems

From a point of detector system and unit device, in the MWIR and LWIR spectral regime, a large dark current always becomes problematic in PDs based on semiconductors due to its small band gap. This makes high temperature operation extremely difficult and results in a relatively bulky and high power consuming devices, because it typically requires an extra cooling system. Therefore, to achieve the desired purpose of compact on-chip m sensors and portable imaging devices, increasing operating temperature of MWIR/LWIR PDs is highly required.

Recently, hetero-junction PDs based on ternary InAsSb material have become one of the promising candidates thanks to its proper band gap to cover IR range, low electron effective mass and low Auger recombination rate [7-15]. Among various types of PDs, photovoltaic detectors attract a lot of attention, owing to their high response speed and zero bias operation, which mitigate self-heating and power dissipation issues present in photoconductive detectors [11-15]. However, to fully utilize the potential of InAsSb photovoltaic detectors with advantages described above, increasing the operating temperature is significantly important, and is essential to realize low power consumption on-chip sensors.

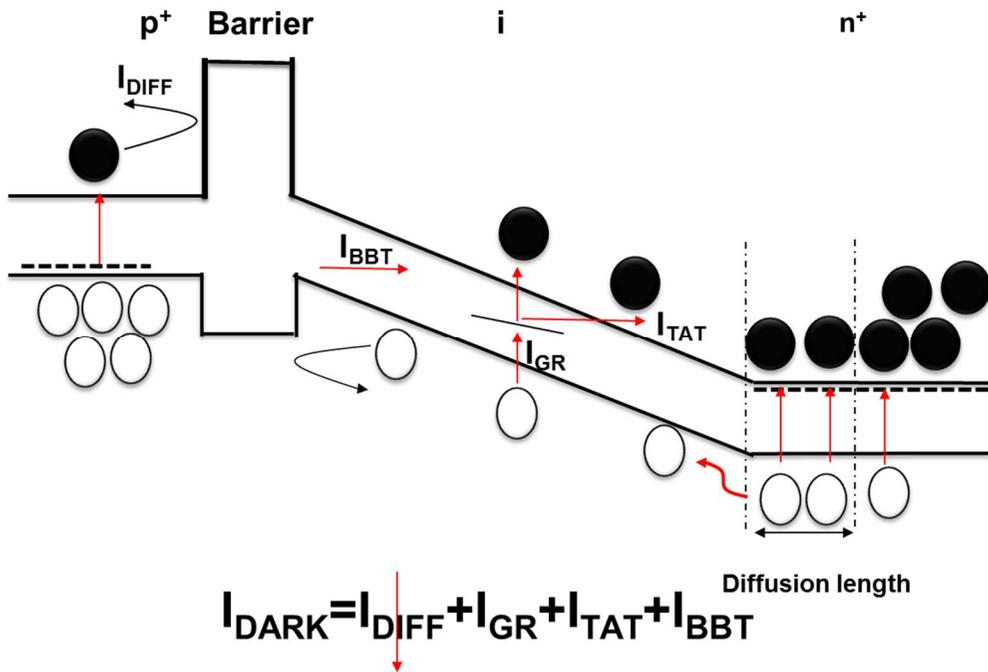


Figure 49 Approach of heterojunction photodetectors with barrier layer based on p-i-n structure which shows parts of total dark current such as diffusion current, generation-recombination current, trap-assisted tunneling current and band-to-band current

To increase the operating temperature, inserting a wide band gap material as a barrier layer between contact layer and absorption layer has been typically used in many studies as shown Figure 48 [7-9,13,14]. As a result, they reduced the excessive dark current induced by the diffusion of carriers, which leads to the increased operating temperature. To achieve this purposes, the ideal design would be a proper unipolar barrier, which does not have the undesired valance band offset (VBO) resulting in hindering the

photo-generated hole transport and have a large conduction band offset (CBO) to block dark current by electron diffusion.

In this chapter 4, to verify the feasibility of InAsSb p-i-n PDs, we demonstrated InAs_{0.81}Sb_{0.19}-based hetero-junction photovoltaic detector (HJPD) with In_{0.2}Al_{0.8}Sb barrier layer grown on GaAs substrate using Al_{0.93}Ga_{0.07}Sb metamorphic buffer layer via molecular beam epitaxy (MBE). Usually, with Sb composition above 15%, a valance band offset with type-I band alignment starts to appear for AlSb barrier (typical Sb-based barrier layer) in AlSb/InAsSb system as shown in Figure 50a and 50b [16-18]. Additional reduction of VBO could be still required for achieving an optimum barrier layer. Moreover, there are no reports regarding room temperature operation in InAsSb PD with Sb composition of 20%. Therefore, we have designed the optimum barrier structure for InAsSb with 20% Sb composition, grow specific structures and characterize the PD performances.

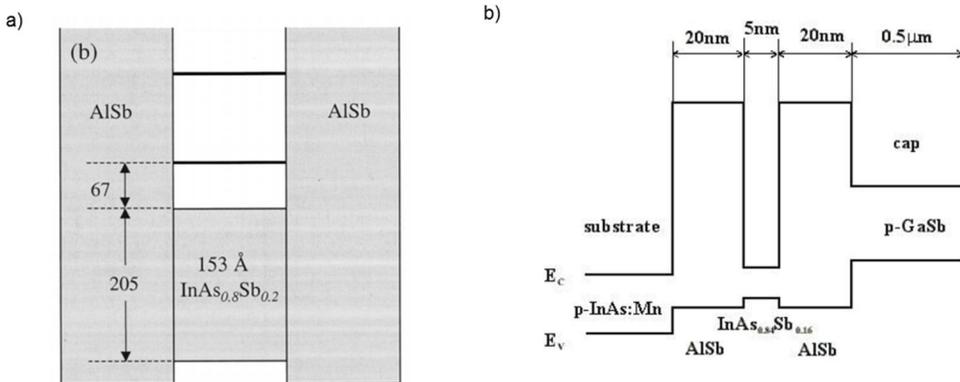


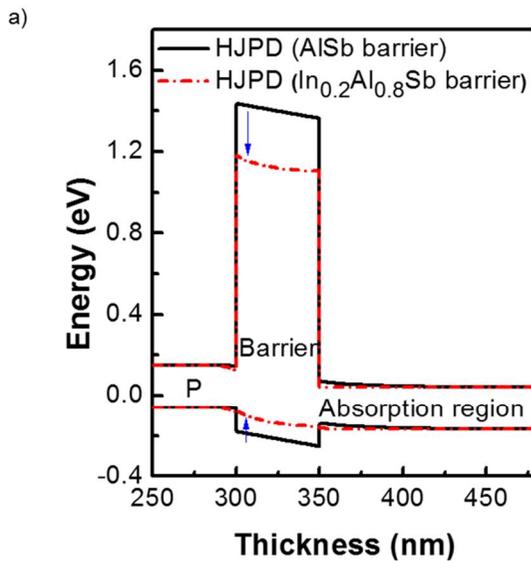
Figure 50 a) band alignment of quantum well consisting of InAs_{0.8}Sb_{0.2} with AlSb barrier layer, b) simulated band structure of InAs_{0.8}Sb_{0.2} / AlSb quantum well [16-18]

4.2 Barrier layer design and material characterization for growing HJPDs

4.2.1. Simulation of an optimum barrier layer for $\text{InAs}_{0.8}\text{Sb}_{0.2}$

In order to design a unipolar barrier for InAsSb absorption layer, simulation of the energy band diagram was done by solving 1D Poisson's and Schroedinger's equations in self-consistent manner. The simulation result via the technology computer aided design (TCAD) simulator is shown in Figure. 51a. Parameters we used are tabulated in Fig. 51b. The structure consisted of $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier layer between doped p- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ layer and unintentionally doped intrinsic $\text{InAs}_{0.81}\text{Sb}_{0.19}$ absorption layer under zero bias condition at room temperature. The nominal doping concentrations of p- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and intrinsic (lightly n) absorption layers was assumed to be 1×10^{18} and $5 \times 10^{16} \text{ cm}^{-3}$, respectively. A moderate $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ layer thickness of 50 nm was chosen, considering the critical thickness of approximately 90 nm based on the model proposed by People & Bean [21] from the lattice mismatch between $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ materials (approximately 1.09 %). At first, the simulation of a HJPD structure with a typical AlSb barrier layer was done to validate the simulation data and input parameters. Band diagram for AlSb showed the 1.2 and 0.1 eV for CBO and VBO, respectively, which is reasonable compared to previous results when considering different Sb compositions and doping concentrations [17-18]. Second, 20% of indium was added in AlSb to form unipolar barrier, resulting in a reduction of both CBO and VBO in band diagram. As intended, this

structure has high CBO of 0.9 eV and nearly zero VBO, which is possible to block the diffused electrons while naturally collecting the photo-generated carriers simultaneously. Additionally, the dark current modeling and quantum efficiency (QE) simulation based on these band diagrams will be further studied to accurately predict the performance of the InAsSb based PDs in the future.



b)

	Electron affinity (eV)	$E_g(0)$ (eV)	Bowing factor	Dielectric constant	Electron mass ($\times m_0$)	Heavy hole mass ($\times m_0$)	Light hole mass ($\times m_0$)	Electron mobility (cm^2/Vs)	Hole mobility (cm^2/Vs)
AlSb	3.6	1.7 (x-valley)	-	12	0.14	0.94	0.16	1100	700
InAs _{0.81} Sb _{0.19}	5.05	0.285	0.67	15.48	0.0243	0.542	0.0248	75125	660
In _{0.2} Al _{0.8} Sb	3.83	1.258	0.43	12.96	0.1147	0.838	0.1312	16080	730

Figure 51 a) Energy band diagram of HJPDs with different barrier layers under zero bias at room temperature, b) Table of parameters for simulating the band diagram.

4.2.2. Growth of a high quality InAsSb layer with an AlGaSb buffer layer grown on GaAs substrates

Due to the lack of substrates for homo-epitaxy, many previous efforts have been made to grow high quality InAsSb materials on various substrates such as GaSb, InSb, GaAs and Si [7-15]. Among them, GaAs substrate has advantages in terms of high quality substrate, high transmittance in IR range and monolithic integration to ROICs without flip-chip technology for image sensor array in spite of relatively high lattice mismatch between InAsSb and GaAs compared to GaSb, InAs and InSb [6,15]. To compensate the lattice mismatch between GaAs and InAsSb and to improve the crystalline quality of InAsSb, many research groups have introduced various buffer layers and growth method [11,12,19,20]. Consequently, the operation temperature of InAsSb based PDs grown on GaAs substrates differs depending on each buffer growth techniques. In spite of such advances, only a few results have been reported on photovoltaic detectors. Thus, we must firstly grow the high quality InAsSb buffer layer to guarantee performances of final HJPD structure.

At first, fully relaxed InAsSb layers were grown on GaAs substrate to confirm As to Sb ratio without strain. This film was grown by a Riber compact 21E solid source MBE system with As and Sb cracker cells. During the growth, reflection high energy electron diffraction (RHEED), and BandiT band-edge thermometry system were utilized to monitor the growth condition and temperature. First, surface oxide of GaAs substrate was desorbed by the heating at 620°C under As ambient condition. Then, 0.1 μm -thick GaAs

buffer layer was grown at 580°C. Subsequently, for growing InAsSb alloy, indium flux of 0.8ML/s, As and Sb dimer mode were used at 440°C that was optimized by several tests as shown in Figure 52a. Fig. 52b shows the high-resolution XRD (HRXRD) results for InAsSb layers with various compositions. Measurements were performed by using ATXG equipped with Cu K α 1 radiation and double crystals. The composition of Sb ranging from 10% to 74% were successfully changed while the reference peak of GaAs substrate was positioned in 66.05°. And smaller intensities than GaAs substrate were observed in InAsSb peaks because of the fully relaxed film. Fig. 52c exhibited the As composition in InAsSb layer with a variation of As dimer and Sb dimer ratio. As and Sb incorporation ratio showed a linearity with As partial pressure over total pressure of V-group with enough In flux to grow. It indicated that adjustment of a As and Sb ratio can be easily obtained by using this linearity. Therefore, from these results, we could manipulate a composition of InAsSb layer through V-group pressure.

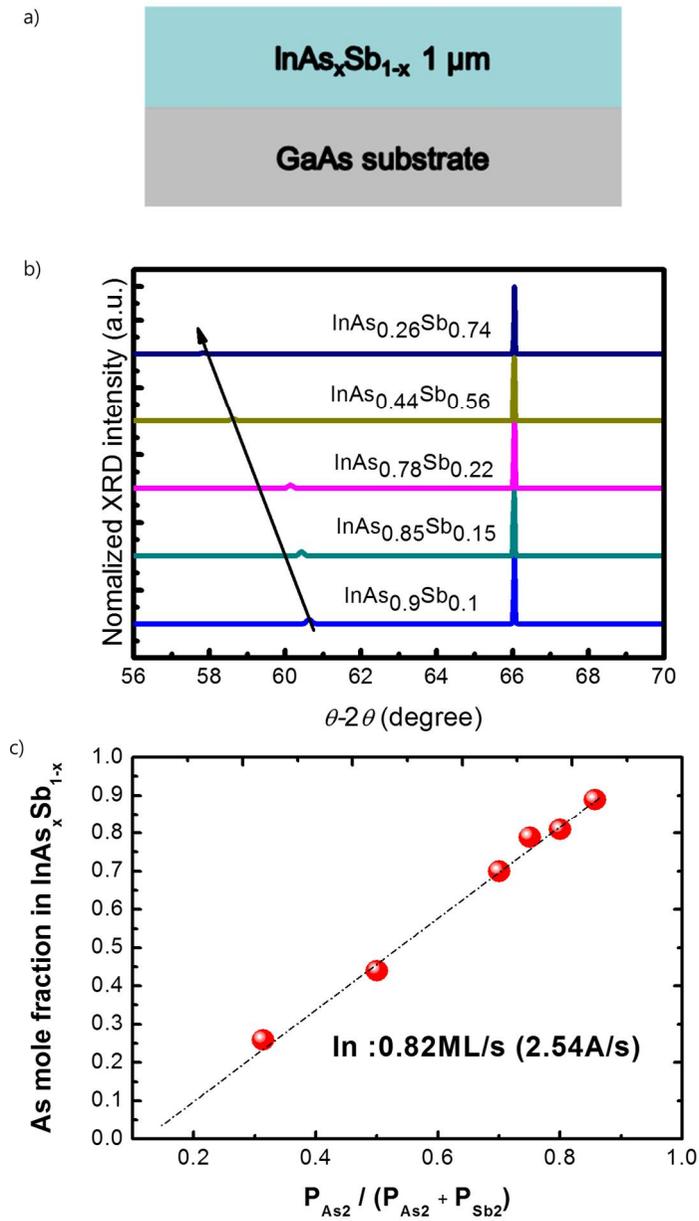


Figure 52 a) schematic of fully relaxed structure grown on GaAs substrate, b) HRXRD measurement results with various compositions of InAsSb, c) results of As compositions in terms of As to Sb ratios.

Next, we have inserted the buffer layer between active $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and GaAs substrate (the composition of $\text{InAs}_{0.81}\text{Sb}_{0.19}$ confirmed in late experiment). Buffer layer has an important role to reduce the lattice misfit induced dislocation density and defects which can lead to improve PD performances. Then, $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ buffer layer was selected thanks to their high resistivity and nearly lattice match condition to $\text{InAs}_{0.8}\text{Sb}_{0.2}$. The optimization of AlGaSb buffer layer was carried out in a same chamber in previous works. As a result, high quality buffer layer was obtained by using a fine tuning of V/III ratio. It is very important because Sb has a low surface mobility and tends to aggregate together in a low Sb-flux environment which easily induced Al and Ga anti-sites (Al_{Sb} and Ga_{Sb}) [23].

After that, The $\text{InAs}_{0.81}\text{Sb}_{0.19}$ epitaxial layer quality was analyzed using the structure consisting of $\text{i-InAs}_{0.81}\text{Sb}_{0.19}/\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ buffer (2/ 1 μm) on GaAs substrate. Surface de-oxidation of GaAs substrate was carried out at 620°C under As ambient condition. Next, 0.1 μm -thick GaAs buffer layer and 1 μm -thick $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ buffer layer were grown at 580°C and 515°C , respectively. Then, calculated indium flux of 0.8ML/s, As and Sb pressure ratios were used at 440°C for $\text{InAs}_{0.81}\text{Sb}_{0.19}$. To examine the crystalline quality, high-resolution HRXRD measurements were performed. The threading dislocation density (TDD) was calculated by using Ayer's model regarding full width at half maximum (FWHM) values of $\text{InAs}_{0.81}\text{Sb}_{0.19}$ (004) peak [22]. Figure 53a shows TDD values of InAsSb layer grown on GaAs substrate versus buffer layer thickness grown by different growth methods including metalorganic vapor phase epitaxy (MOVPE) and MBE. It is ideal for both buffer layer thickness and TDD value decrease, simultaneously. The

FWHM value of this work was found to be 396 arcsec at 60.18° from HRXRD data, which corresponds to the TDD of approximately $3.3 \times 10^8 \text{ cm}^{-2}$. Although there were only a few studies to compare the quality of InAsSb materials grown on GaAs, our $\text{InAs}_{0.81}\text{Sb}_{0.19}$ quality exhibited quite a low TDD value and comparable or even better crystallinity compared with previous reports as shown Fig. 53b.

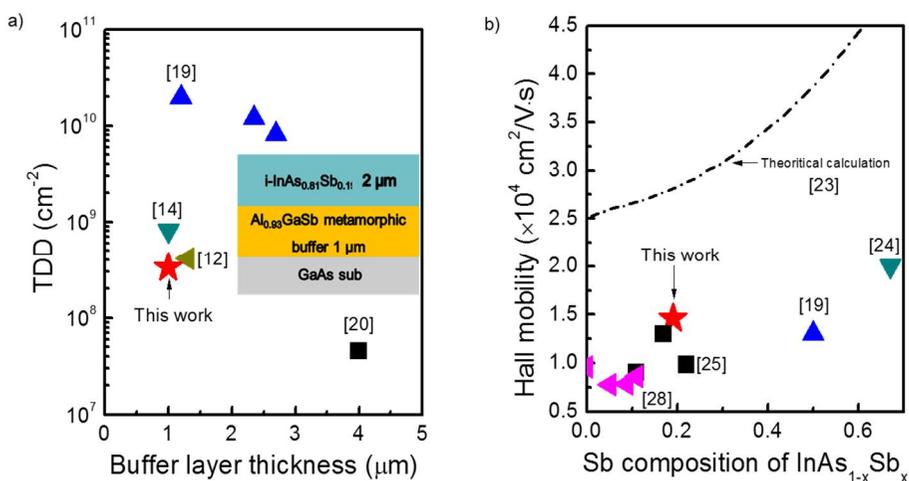


Figure 53 a) threading dislocation density versus buffer layer thickness calculated from the Ayers model, b) results of the Hall measurement in this work and in previous papers at room temperature as a function of the Sb composition of the $\text{InAs}_{1-x}\text{Sb}_x$

For electrical characterization, Hall measurement was conducted by using van der Pauw method for $\text{InAs}_{0.81}\text{Sb}_{0.19}$ layer at room temperature. Fig. 2(b) shows that previous results on InAsSb layer on GaAs substrate with different Sb compositions at room temperature [19,23-26]. Mobility of

InAs_{0.81}Sb_{0.19} was approximately 15,000 cm²/V·s, which is the best result among InAsSb with Sb composition around 20% grown on GaAs substrate. These results can be attributed to the optimization of Al_{0.93}Ga_{0.07}Sb buffer layer. The surface morphology and electrical properties of Sb-based materials are sensitive to the modulation of V/III ratio, which could significantly affect the layer quality [27]. These results strongly suggest that current InAs_{0.81}Sb_{0.19} layer is very high quality enough to grow and fabricate devices.

4.2.3. Ohmic contact formation with metal species

Before fabricating the InAsSb PD, we have carried out the studies for Ohmic contact formation which can directly affect the carrier collection at the metal/semiconductor interface. To evaluate the contact property, the epitaxial structure grown on a GaAs substrate consisted of a 1- μ m-thick Al_{0.93}Ga_{0.07}Sb buffer layer and p-type, n-type, undoped 1- μ m-thick InAs_{0.81}Sb_{0.19} from bottom to top as illustrated in Figure 54.

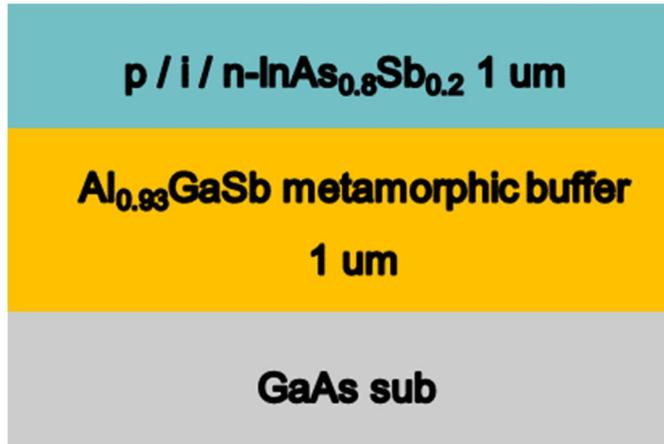
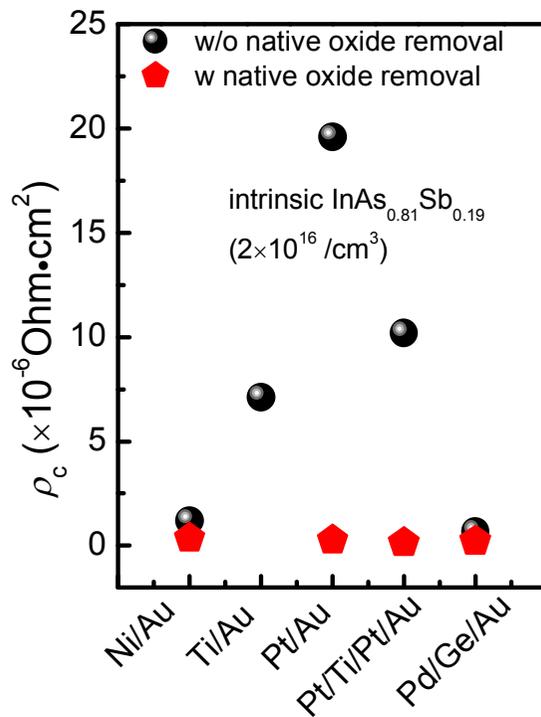


Figure 54 Schematic of InAs_{0.8}Sb_{0.2} with AlGaSb buffer layer grown on GaAs substrate

Transmission line model (TLM) patterns were used to extract the contact resistance and specific contact resistivity (ρ_c). The TLM pattern fabrication process began with mesa isolation using wet chemical etching with H₃PO₄ based mixtures to AlGaSb buffer layer surface. Prior to the metallization, HCl:DI (1:6) was used to remove the native oxide for 60 seconds. Various metallization schemes were deposited by an electron-beam (e-beam) evaporator on the TLM patterns with 2, 4, 6, 8, and 12 μm spacings. Metal species were varied into Ni/Au, Ti/Au, Pt/Au, Pt/Ti/Pt/Au and Pd/Ge/Au conventionally used for optoelectronic devices. Then, we measured the I-V characteristics at room temperature condition in air ambience.

Firstly, different metal species were deposited on intrinsic InAsSb layer with 2×10^{16} doping concentration w and w/o native oxide removal because Sb based native oxide are well known as a detrimental layer at the interface. Figure 55 shows the result of specific contact resistivity as a function of

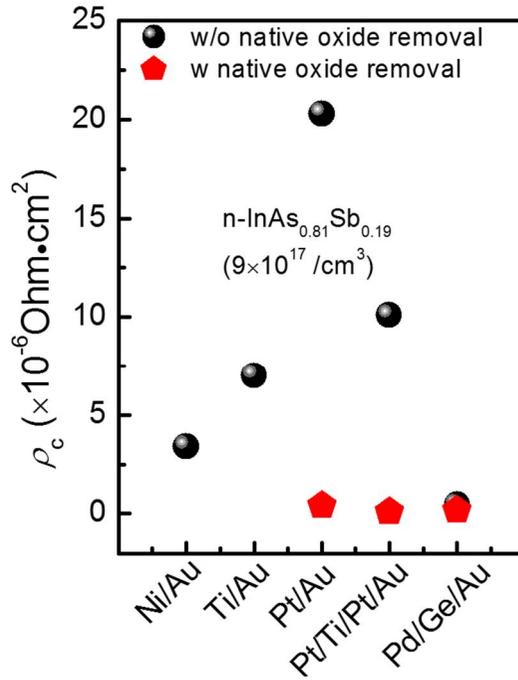
metal species according to existence of native oxide. Without native oxide removal, the deviation of specific contact resistivity were large in terms of metal species which indicated that each metal can be differently reacted with native oxide. The high specific contact resistivity of low 10^{-5} order of magnitude were observed in Pt contacts on InAsSb layer compared with Ni, Ti, Pd contacts. It could be attributed to a low ability of Pt to react with other materials. With native oxide removal process, a dramatic improvements of specific contact resistivity of 10^{-7} order were observed for all metal species. It suggests that native oxide can strongly hinder the electrical conduction which causes the degradation of PD performances.



Metal species	Specific contact resistivity (Ohm · cm ²)	
	w/o native oxide removal	w native oxide removal
Ni/Au	1.2 x 10 ⁻⁶	3.8 x 10 ⁻⁷
Ti/Au	7.1 x 10 ⁻⁶	-
Pt/Au	2.0 x 10 ⁻⁵	2.7 x 10 ⁻⁷
Pt/Ti/Pt/Au	1.0 x 10 ⁻⁵	1.5 x 10 ⁻⁷
Pd/Ge/Au	6.8 x 10 ⁻⁶	2.3 x 10 ⁻⁷

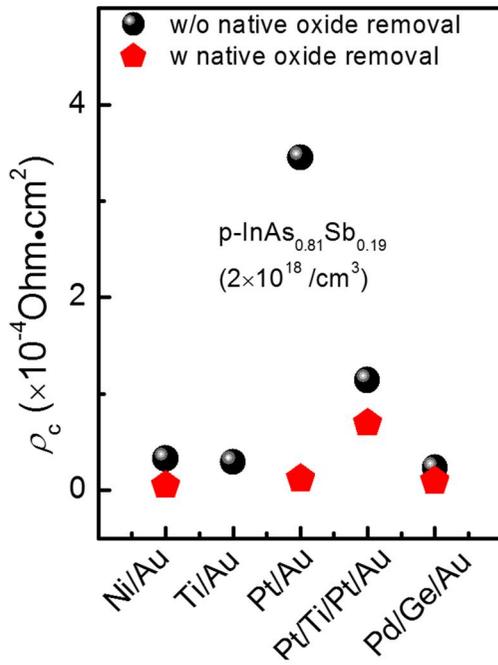
Figure 55 specific contact resistivities as a function of metal species with/without native oxide removal process for intrinsic InAsSb.

Secondly, we have investigated contact properties on doped n-type and p-type InAsSb layers. As shown in Figure 56, contacts of n-type doped layer having doping concentration of $9 \times 10^{17} / \text{cm}^3$ revealed the similar property with intrinsic InAsSb layer since intrinsic layer has naturally n-type doped layer property. For p-type doped layer ($2 \times 10^{18} / \text{cm}^3$), the experiment with same metal schemes was conducted as illustrated in Figure 57. Contact properties on p-type InAsSb showed a relatively high specific contact resistivity for all metal schemes. From these results, it was found that Ni/Au contact on InAsSb revealed the lowest specific contact resistivity on average regardless of types of doped layer. Thus, we have used the Ni/Au contact in our experiment for obtaining high performance of PDs.



Metal species	Specific contact resistivity ($\text{Ohm} \cdot \text{cm}^2$)	
	w/o native oxide removal	w native oxide removal
Ni/Au	3.4×10^{-6}	-
Ti/Au	7.0×10^{-6}	-
Pt/Au	2.0×10^{-5}	4.2×10^{-7}
Pt/Ti/Pt/Au	1.0×10^{-5}	1.2×10^{-7}
Pd/Ge/Au	4.6×10^{-7}	1.8×10^{-7}

Figure 56 specific contact resistivities as a function of metal species with/without native oxide removal process for n-type InAsSb.



Metal species	Specific contact resistivity (Ohm · cm 2)	
	w/o native oxide removal	w native oxide removal
Ni/Au	3.3×10^{-5}	5.0×10^{-6}
Ti/Au	2.9×10^{-5}	-
Pt/Au	3.5×10^{-4}	1.2×10^{-5}
Pt/Ti/Pt/Au	1.1×10^{-4}	7.0×10^{-5}
Pd/Ge/Au	2.3×10^{-5}	9.4×10^{-6}

Figure 57 specific contact resistivities as a function of metal species with/without native oxide removal process for p-type InAsSb.

4.2.4. Growth and fabrication of InAsSb based HJPDs

After examining material properties, the final HJPD structure was decided as shown in Figure 58a. This structure is composed of $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ metamorphic buffer/n- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ layer ($5 \times 10^{17} \text{ cm}^{-3}$)/i- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ absorption layer (unintentionally doped)/ $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier/p- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ ($3 \times 10^{18} \text{ cm}^{-3}$) layer from bottom to top. A reference p-i-n PD without $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier was also grown for comparison. Growth temperatures for each layer were the same as previously mentioned. After the growth of HJPD, HRXRD measurement was carried out to confirm the quality of reference p-i-n PD and HJPD. Fig. 58b shows the normal θ - 2θ scan results for p-i-n PD, HJPD and simulated spectra using EPITAXY simulator at room temperature. Only two peaks were observed for p-i-n PD at 60.24° and 66.05° corresponding to $\text{InAs}_{0.81}\text{Sb}_{0.19}/\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ and GaAs, whereas three peaks were observed for HJPD due to the existence of $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ with different lattice constant. The peak at 66.05° completely corresponded to GaAs (004) substrate. $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ peaks were combined to a single peak. In HJPD, additional $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ peak was at a smaller angle region of 58.86° than the combined peak of $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$. In EPITAXY simulation, $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and $\text{Al}_{0.93}\text{Ga}_{0.07}\text{Sb}$ can be distinguished thanks to its perfect crystallinity. However, due to their similarity of lattice constants and imperfect crystallinity, combined peak in XRD measurements could not be divided. Therefore, a composition of $\text{InAs}_{0.81}\text{Sb}_{0.19}$ was further verified through optical characterization of devices. Given this situation, the peak positions of grown samples matched well to the simulation result. These

diffraction patterns indicated that MBE grown $\text{InAs}_{0.81}\text{Sb}_{0.19}$ photovoltaic detectors are successfully formed on the GaAs substrate with a precise control of target compositions. Then, device fabrication process was carried out. After native oxide removal with HCl:DI (1:5) for 1 minutes, a top electrode of Ni/Au (30/300 nm) was evaporated by electron beam (EB), followed by lift-off process. Subsequently, mesa etching was conducted by H_3PO_4 and HF based-solutions for $\text{InAs}_{0.81}\text{Sb}_{0.19}$ and $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ etching until n- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ contact layer was exposed. A 200 nm-thick SiN_x layer was deposited on the sidewall at 120°C by plasma enhanced chemical vapor deposition (PECVD) for the surface passivation and isolation of the electrode. Then, bottom contact for n- $\text{InAs}_{0.81}\text{Sb}_{0.19}$ layer was formed by Ni/Au (30/300 nm) evaporation and lift-off process. The final devices had $500 \times 500 \mu\text{m}^2$ optical window for front illumination. Fig. 58c shows the schematic image of fabricated HJPD and cross-section scanning electron microscopy (SEM) image. SEM image shows each layer with clear interfaces in between these layers, indicating the $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ layer was well formed between $\text{InAs}_{0.81}\text{Sb}_{0.19}$ layers. Thickness of $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ were measured to be approximately 50 nm as expected.

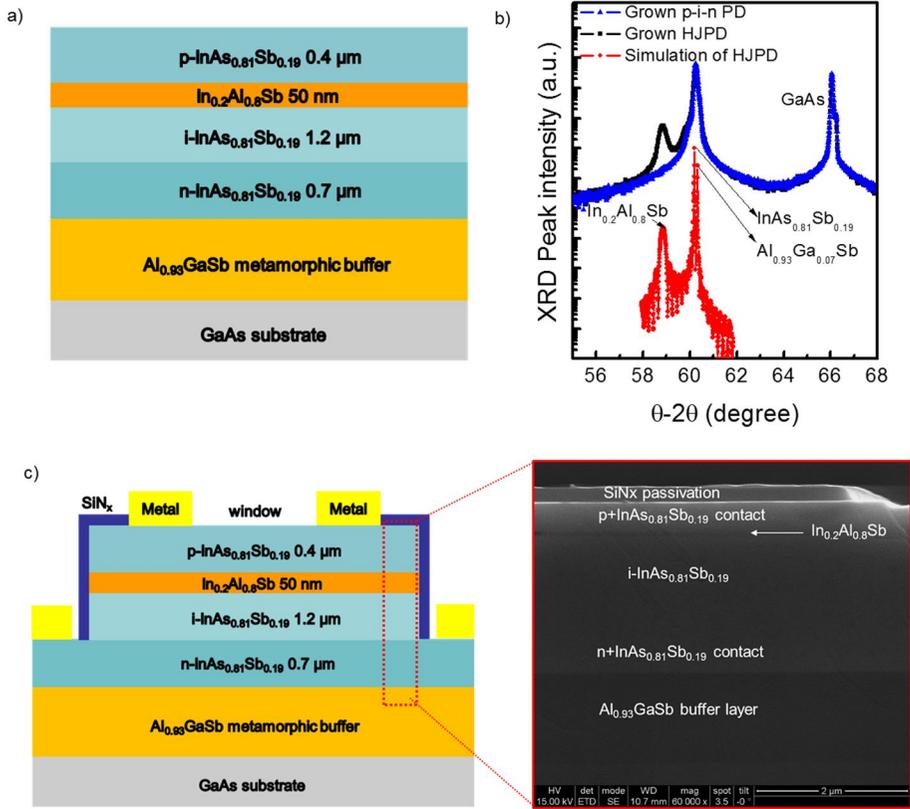


Figure 58 (a) Schematic structure of HJPD with $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ grown on GaAs (b) measured θ - 2θ results of MBE-grown reference p-i-n PD and HJPD compared to EPITAXY simulation (c) Schematic of finally fabricated HJPD and SEM image of the cleaved cross-section.

4.3 Analysis of electrical and optical characteristics for fabricated PDs

To investigate the electrical characteristics and dominant dark current mechanisms in HJPD, the current density (J) - voltage (V) characteristics of the fabricated p-i-n PD and HJPD were measured at room temperature, as shown in Figure 59a. Measurements were carried out by a Keithely 4200 in a probe station. While the p-i-n PD exhibited weak rectifying characteristic, it was found that clear improvement of rectifying property was achieved in HJPD over the whole reverse bias range. For p-i-n PD, a weak rectifying characteristic could be due to relatively large leakage current. To investigate the physical origin of large leakage current, we have characterized the surface leakage current of these devices at room temperature according to our previous report [28]. By extracting of surface leakage current from various patterns, HJPD showed the 2mA/cm and 0.2mA/cm of surface leakage current for non passivated and passivated conditions, respectively.

Nevertheless, enhancement of rectifying behavior with barrier layer is consistent with previous report of InSb photovoltaic detectors with barrier layer [29]. This significant decrease of dark current can be attributed to the blocking of the electron diffusion induced current and surface leakage current by inserting a wide band gap barrier [30]. For analysis, the temperature dependence of J from 280K to 90K was measured as shown in Fig. 59b. With decreasing the temperature, obvious suppression of dark current was observed in the diode characteristic. Fig. 59c shows the temperature dependence of the J measured at -10 mV as a function of inverse temperature for p-i-n PD and HJPD. Through extraction of activation energy (E_a) from the

slope of the Arrhenius curve, the dominant mechanism for dark current with respect to temperatures was evaluated. The E_a fittings were performed by the following expression for the diffusion limited current (J_d),

$$J_d \sim T^3 \exp\left(-\frac{E_a}{k_B T}\right) \quad \text{Equation 2}$$

where E_a , k_B , and T are the activation energy, the Boltzmann constant, and temperature, respectively. In p-i-n PD, the temperature dependence of dark current was weak. Quite small E_a of below 0.1 eV was extracted, which is due to the surface leakage current [31]. In contrary to reference p-i-n PD, extracted E_a in HJPD was found to be as high as 0.271 eV above 200K. This value closely matches with the zero temperature band gap ($E_g(T=0) = 0.276$ eV) of $\text{InAs}_{0.81}\text{Sb}_{0.19}$. The fact that the activation energy is close to $E_g(T=0)$ implies that the diffusion limited current could be dominant in this range. The small difference between E_a and intrinsic band gap suggests that potential barrier in the valance band is significantly small [32]. Therefore, it can be interpreted that $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier layer does not impede the collection of photo-generated carriers, while it still suppresses the electron diffusion and surface leakage current. Lower E_a smaller than a half of band gap from the second gradient at low temperature indicates that the current is dominated by generation-recombination in absorption region. Fig. 59d shows the bias voltage dependence of E_a , extracted from the Eq. (1). The dotted line shown in Fig. 59d is for the $E_g(T=0)$, indicating the diffusion limited behavior. In accordance to a small reverse bias range from 0 V to -0.15 V, diffusion limited behavior would be dominant for HJPD. In a larger bias range above -0.15 V, smaller E_a was obtained which implies HJPD could be seriously

affected by generation-recombination or tunneling limited behavior. From these results, we believe that the superior performance of HJPD as well as p-i-n PD can be achieved through further passivation technique optimization.

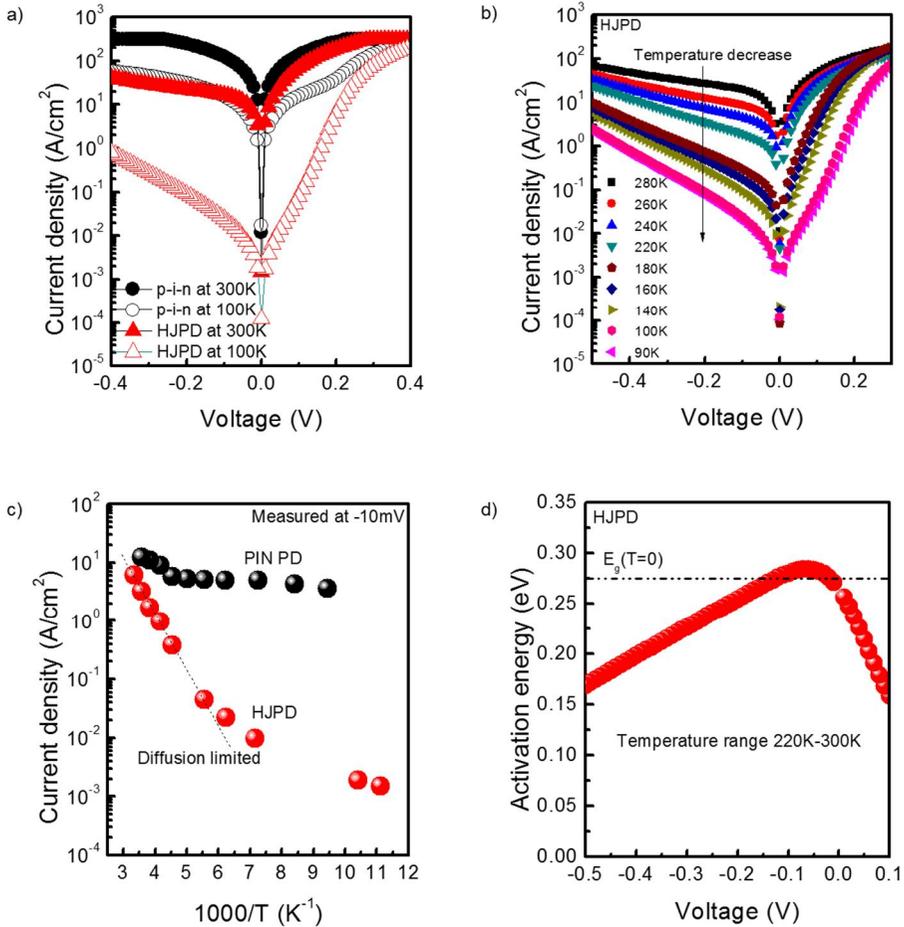


Figure 59 a) current density (J)-voltage (V) curves for p-i-n PD and HJPD at room temperature and 100K, b) temperature dependent J-V curves for HJPD, c) temperature dependent dark current density-inverse temperature extracted at -10 mV, d) activation energy behavior for HJPD calculated by Eq.(1) in a temperature range from 220K to room temperature.

Figure 60a and 60b shows the normalized photocurrent response of p-i-n PD and HJPD measured by a Bruker Vertex 80v Fourier transform infrared spectrometer (FTIR). In this FTIR system, a global source emitting MIR radiation along with a KBr beam splitter was used. Signals with various temperatures were amplified by a low-noise current amplifier (Keithley 428) and then embedded in the spectrometer. PDs were measured at different temperatures with no external bias (0V). Photocurrent responses of p-i-n PD were observed in a range from the 10K to 230K as illustrated in Fig. 60a. The band edge shift of p-i-n PD was clearly shown in the low energy regime with increasing temperature. Photocurrent response and operating temperature of our p-i-n PD are similar to the result in previous report which has $\text{InAs}_{0.8}\text{Sb}_{0.2}$ absorption layer showing maximum operating temperature up to 240K [15]. This suggests that the fabricated p-i-n PD was successfully grown and has the comparable performance with a well-matched transmission window of MIR in a spectral range of 3-5 μm .

On the other hand, the clear photocurrent responses up to room temperature were observed for the HJPD under the same measurement condition as a p-i-n PD. Its band edge was also shifted to low energy region with increasing temperature. The strong photocurrent responses for HJPD indicated that it is possible to operate the device sufficiently at room temperature. With only 50 nm-thick of $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier insertion, the operating temperature was dramatically increased from 230K to 300K. It was verified that a barrier layer can play an important role to increase the operating temperature by reducing the dark current. Interestingly, the PD characteristics show the strong photocurrent response at broad wavelength between 3-5 μm . To investigate its physical origin, optical intensity

distribution in the PD layer was simulated. Fig. 60c shows the simulated optical intensity distribution in HJPD structure as a function of the incident light wavelength. Incident light with a short wavelength is considerably absorbed near the surface, whereas long wavelength having above 3 μm is mainly absorbed in absorption region. There is still a significant amount of unabsorbed light, which reaches n-InAs_{0.81}Sb_{0.19} contact layer and Al_{0.93}Ga_{0.07}Sb buffer layer. It should be noted that there is strong resonance at 3-5 μm in the absorption region, which is definitely consistent with the photocurrent response spectra measured by FTIR. These results strongly suggest that further layer thickness optimization will be very useful to enhance the detector performances.

To accurately determine the material band gap of InAs_{0.81}Sb_{0.19} through optical measurement, the temperature dependence of the cut-off wavelength (λ_c) for HJPD was investigated when λ_c was decided by a half of the peak intensity of photocurrent response. As illustrated in Fig. 60d, λ_c is fitted by Varshni expression,

$$E_g(\mathbf{T}) = E_g(\mathbf{T} = \mathbf{0}) - \frac{\alpha T^2}{(T+\beta)} \quad \text{Equation.3}$$

where α and β are constants. The parameters obtained from previous experiments are used [33,34]. As a result, the change of λ_c from 3.7 to 5.35 μm was in a good agreement with the expectation for the Sb composition of 19% as depicted in Fig. 60d. It is a reasonable value compared with that of previous result because slightly shorter λ_c was obtained than that of

InAs_{0.8}Sb_{0.2} at the same temperature [15]. From this optical characterization, it was concluded that the composition of Sb in InAsSb alloy is 19%, confirming the result obtained by XRD measurement.

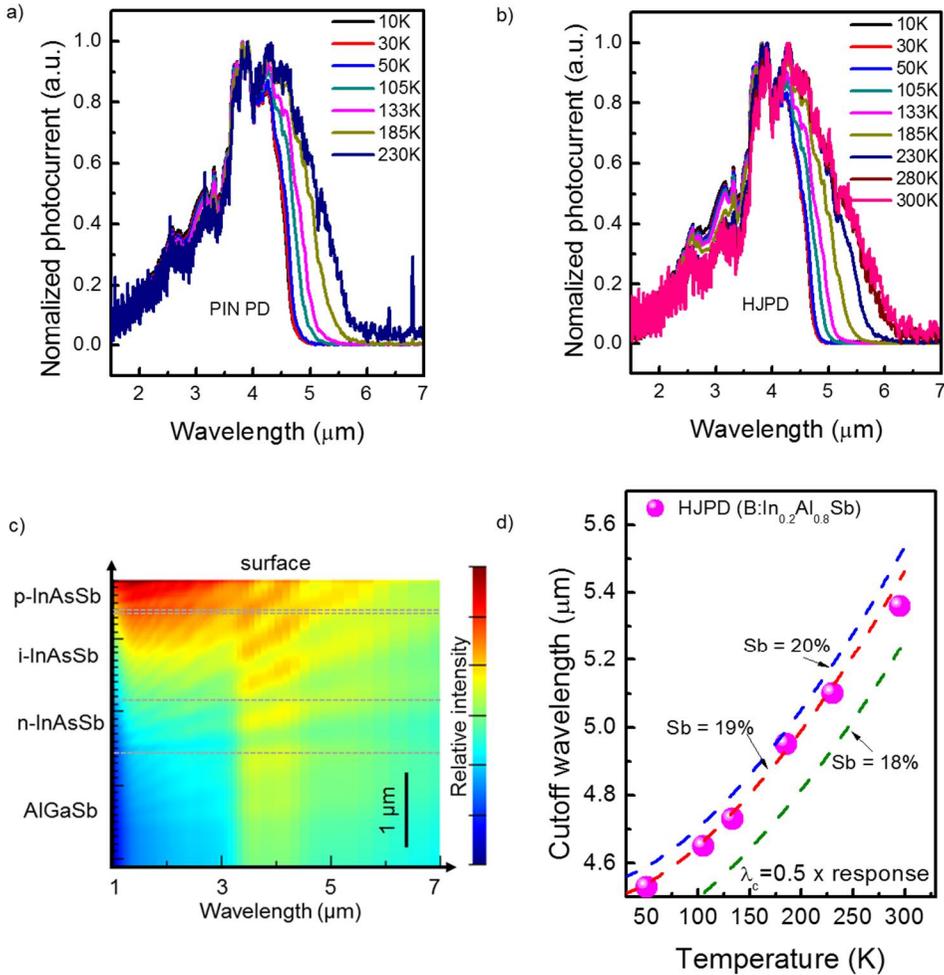


Figure 60 Photocurrent response measurements in FTIR system with different temperatures for a) p-i-n PD, b) HJPD, c) simulation of optical intensity distribution as a function of wavelength for HJPD structure, d) temperature dependence of cutoff wavelength for HJPD and its fit by using

Varshni expression of Eq. (2).

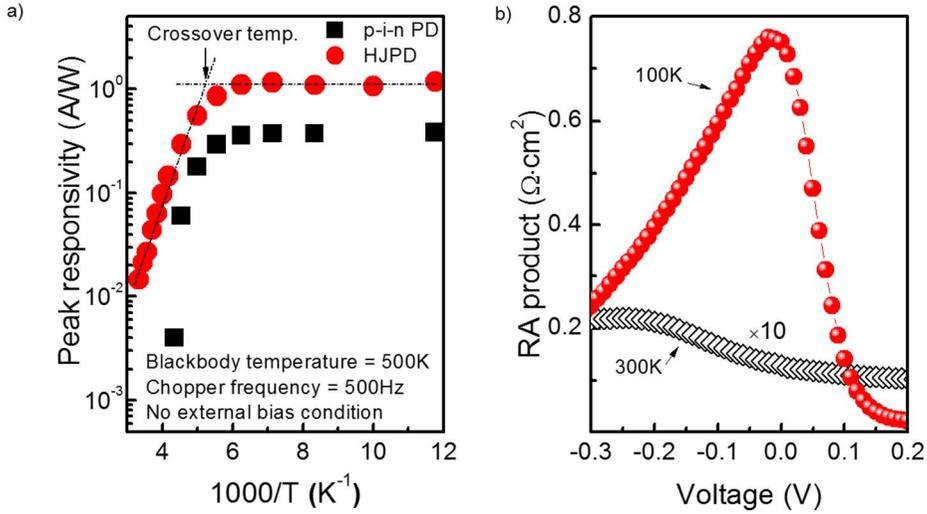


Figure 61 a) responsivity measurement of p-i-n PD and HJPD with 500K blackbody radiation, b) Resistance-area product of HJPD depending on the voltages at 300K and 100K.

Finally, the responsivity measurement was performed as a function of temperatures using 500 K of blackbody source radiation with a 0.3-inch aperture size, a lock-in amplifier and a chopper frequency of 500 Hz. From this measurement, the peak responsivity can be extracted from the Eq. (3) associated with the blackbody geometrical configuration and the λ_c for both PDs [35],

$$R_P = \frac{v_o}{\frac{hc}{\lambda_c} \int_0^{\lambda_c} M_q d\lambda \frac{A_s A_d}{\pi r^2} t F_F} \quad \text{Equation.4}$$

where R_P , M_q , σ , h , c , v_o , A_s , A_d , t , F_F and r are peak responsivity, blackbody responsivity, photon existence of blackbody, Stefan-Boltzmann constant,

Planck constant, velocity of light, output voltage produced by detector (volt), blackbody aperture area, detector area, transmittance of window, form factor for conversion, and source to detector distance respectively. In this Equation.(4), we have used the cutoff wavelength of photocurrent responses shown in Fig. 60. Figure. 61a shows that the peak responsivity of p-i-n PD and HJPD as a function of temperature. The peak responsivity was 0.38 and 1.18A/W for p-i-n PD and HJPD at 83K under zero bias. This corresponded to the quantum efficiency of 11% and 34% for p-i-n PD and HJPD. Also, HJPD recorded the 15 mA/W at room temperature, whereas p-i-n PD showed the peak responsivity 4 mA/W at 230K and could not be operated at temperatures higher than 230K. The threefold performance improvement in HJPD than p-i-n PD was achieved by inserting a 50 nm of $\text{In}_{0.2}\text{Al}_{0.8}\text{Sb}$ barrier layer only, which contributed to the decrease of dark current as shown in Fig. 59. These results on operating temperature completely coincide with photocurrent response as depicted in Fig. 60. When temperature is increased above crossover temperature of approximately 200K as described in Fig. 60c, peak responsivity is rapidly degraded for both PDs due to an increased noise current by a diffusion of holes in n-type region [13]. Furthermore, the resistance-area (RA) products for HJPD at 300K and 100K are illustrated in Fig. 61b. The HJPD showed the slightly smaller R_0A product of 0.013 and $0.75 \Omega \cdot \text{cm}^2$ at 300K and 100K under zero bias respectively compared to other papers on InAsSb PD showing approximately $0.1 \Omega \cdot \text{cm}^2$ of R_0A product at room temperature [13]. This would be attributed to the leakage current caused by the non-optimized surface passivation for HJPD. Additionally, our HJPD may have defect-assisted leakage current, since our HJPD is grown on lattice-mismatched GaAs substrate rather than lattice-

matched GaSb substrate in other works. Nevertheless, it is still very meaningful that we demonstrated room temperature operation of InAsSb PD by barrier engineering even on lattice-mismatched substrates. Moreover, these results strongly suggest that it can be further much improved by the suppression of leakage current.

Consequently, the notable improvements on operating temperature and responsivity were accomplished in the HJPD. Performance of HJPD at cryogenic and room temperature was quite good compared to commercialized photovoltaic detectors. Photovoltaic detectors produced by Hamamatsu [36] revealed the 4.5 mA/W of peak responsivity at room temperature. The obtained performance was three times better at room temperature. Furthermore, there is still room for the additional improvement of responsivity due to insufficient thickness of absorption layer for collection of light, as shown in Fig. 60c. In addition, since anti-reflection coating (ARC) and an optimal surface passivation technique were not used, performance can be further improved by employing proper ARC and passivation

4.4 Summary

To confirm the feasibility of InAsSb based bulk p-i-n structures for overcoming a wavelength coverage and a cryogenic operation of conventional InSb binary material, we proposed an InAs_{0.81}Sb_{0.19}-based photovoltaic detector with an In_{0.2}Al_{0.8}Sb barrier layer grown on GaAs substrate which has a spectral range of the MIR regime at room temperature. The band simulation showed that the In_{0.2}Al_{0.8}Sb barrier layer could minimize the VBO compared to the typical AlSb barrier. In addition, a high quality InAsSb epitaxial layer was confirmed by the XRD measurement and Hall measurement, which is significantly crucial for detector performance. From the optical characterization using FTIR and the simulation of the electric field distribution, it was shown that the absorption of the HJPD occurred in the target 3-5 μm MIR range. Finally, the responsivity measurement showed 1.18 A/W and 15 mW for the peak responsivity at 83 K and room temperature under zero bias, respectively. This is a significant improvement by at least three times compared with the reference p-i-n PD. In addition, the room temperature operability became comparable to that of commercialized InAsSb photovoltaic detectors.

4.5 Bibliography

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Chapter. 5 Monolithic integration of visible/near-infrared photodetectors

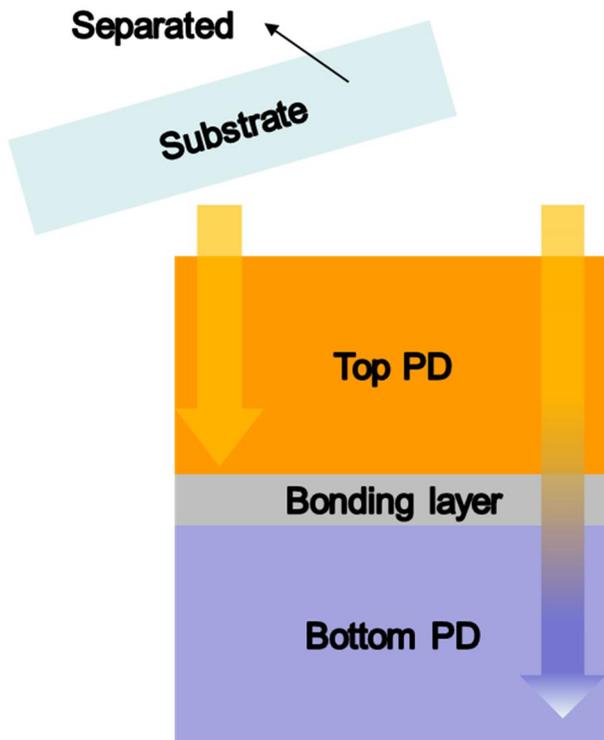
5.1 Introduction

As shown Figure 62, there are many advantages of multicolor PDs with bulk structures including difficulty of growth, layer quality, freedom of wavelength selection, cost-effective process and pixel density. Ultimately, in order to from multicolor PDs, we have developed the key technology how to vertically incorporate the PDs without misalignment and degradation between top PDs and bottom PDs. From this point of view, high throughput epitaxial lift off (ELO) would be one of possible choices instead of hydrogen splitting and transfer printing as shown in chapter. 2 and chapter. 3 [1, 2]. When compared with hydrogen splitting called as ‘smart cut’ and transfer printing, a high throughput ELO approach has advantages such as reliability, throughput and good epitaxial quality.

Additionally, it is important to secure the candidates of the bulk PDs which could be simply integrated. All PDs would be operated at high temperature (room temperature) for eliminating bulky cooling system and additional power consumption. In chapter.4, we have demonstrated the alternative InAsSb bulk structure based p-i-n PDs operating at room temperature in MWIR region. Because a simple p-i-n structure is promising since photovoltaic mode that contributes to high speed and low power consumption [3-7]. From these results, we have obtained the p-i-n structure

based visible GaAs, near-IR InGaAs, SWIR InAs and MWIR InAsSb operating at room temperature.

In this chapter.5, to verify the feasibility of multicolor photodetectos concept, we have first demonstrated monolithic integration of thin film GaAs PD to InGaAs PD in single pixel area by using above-mentioned high throughput epitaxial lift off. We have chosen the materials such as GaAs and InGaAs because PDs based on them are quite a suitable in respect of good material quality and device performances as shown in Figure 63 [8]. By utilizing GaAs based p-i-n and InGaAs p-i-n bulk structure grown on each substrate, multicolor PD with 3 terminals (top/middle common contact/bottom contact) is formed on InP substrate. 3-dimensional stacked PD makes it possible to acquire the simultaneous detection of visible and near-IR wavelengths. Also, each pixel is highly aligned from top PD to bottom PD due to their top-down fabrication process. The material quality of resulting multicolor PD were characterized by X-ray diffraction (XRD) measurement and transmission electron microscopy (TEM). In the current-voltage (I-V) measurements, it clearly showed the diode characteristics of GaAs and InGaAs depending on the bias. Also it revealed the clear photoresponse and responsivity in terms of incident wavelengths. These optical properties of multicolor PD are consistent with the simulated optical intensity distribution. From these results, we have confirmed the feasibility of the multicolor PDs formation in the single pixel area.



- ✓ **Difficulty of growth** 😊
- ✓ **Layer quality** 😊
- ✓ **Freedom of a wavelength selection** 😊
- ✓ **cost (wafer reuse)** 😊
- ✓ **Pixel density** 😊

Figure 62 schematic of multicolor photodetectors concept and advantages compared with other methods

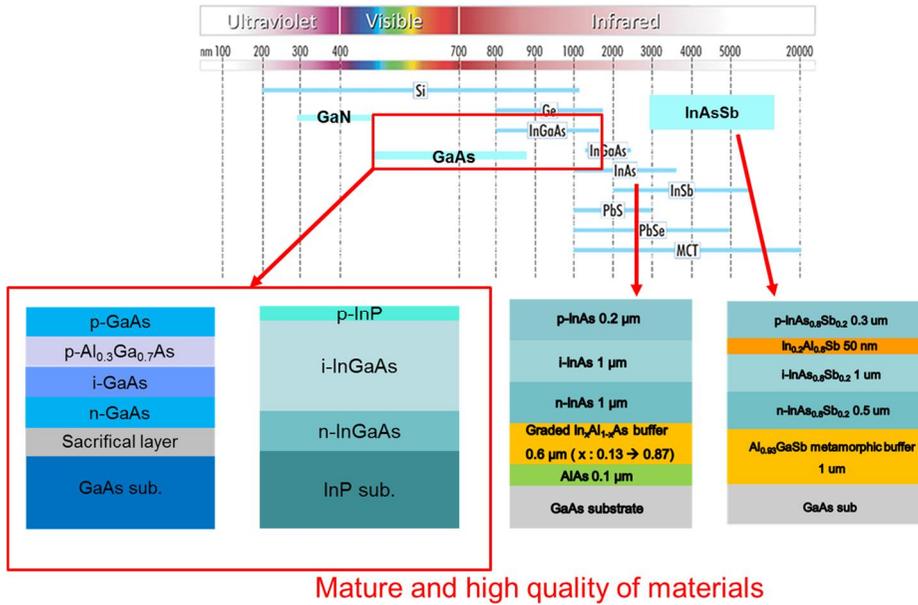


Figure 63 wavelength ranges of III-V materials based photodetectors and candidates of our photodetectors for the heterogeneous integration.

5.2 Fabrication process and material characterization of multicolor PD

Figure 64 shows the entire fabrication process of multicolor PD by using the GaAs p-i-n structure and $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$ p-i-n structure. The GaAs p-i-n structure have been grown on semi-insulating (S.I) GaAs substrate by using molecular beam epitaxy (MBE) which was comprised of AlAs sacrificial layer (10nm)/ n+GaAs layer (600nm)/intrinsic GaAs absorption layer (1 μm)/p+ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer (50nm) /p+GaAs layer (200 nm), from the top to bottom. And $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$ structure grown on S.I InP substrate consisted of n+ $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$ bottom layer (200 nm)/ n-InP etch stop layer (5 nm)/

intrinsic $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$ absorption layer (2.1 μm)/p-InP top layer (100nm) via utilizing metal organic chemical vapor deposition (MOCVD).

The fabrication process started with standard wafer cleaning process with acetone, methanol, and isopropyl alcohol. After cleaning process, 20-nm-thick Y_2O_3 was deposited on top surfaces of both GaAs and $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$ as a bonding material by electron beam (E-beam) evaporator. As demonstrated in Fig. 64b, dimension of top GaAs PDs was defined by photolithography and etched to GaAs substrate with exposed sacrificial layer by H_3PO_4 based solutions for high throughput ELO process. Then, oxygen plasma was irradiated to both Y_2O_3 surfaces for surface activation, followed by wafer bonding at room temperature with a pressure of 3.4 MPa into a wafer bonder. This sample was put in hydrofluoric acid (HF): acetone (1:1) solutions for separating the GaAs substrate. When the GaAs substrate was separated, we obtained the vertically integrated GaAs n-i-p PD on InGaAs p-i-n PD structure as shown in the Fig. 64c. After forming the integrated structure, typical PD fabrication processes were adopted for both PDs. Top electrode of Pd/Ge/Au (20/40/200 nm) was deposited on n+GaAs layer by E-beam evaporator and subsequent lift-off process shown in Fig. 64d. Mesa isolation of top PD until p+GaAs layer was carried out by H_3PO_4 based solution. Simultaneously, for metallization of common p-contact (middle contact), Y_2O_3 interlayer was removed to expose p-InP contact layer as exhibited in Fig. 64e. Fig. 64f revealed the formation of bottom contact of top PD and top contact of bottom PD with Pt/Ti/Pt/Au (20/30/20/200 nm) metallization and lift-off. Then, mesa etching until n+InGaAs layer for bottom PD isolation was conducted by using H_3PO_4 based solution. Finally, as shown Fig. 64h, bottom contact of Pd/Ge/Au (20/40/200 nm) for

n+InGaAs layer was formed and subsequent rapid thermal annealing (RTA) process at 350°C for 1minutes.

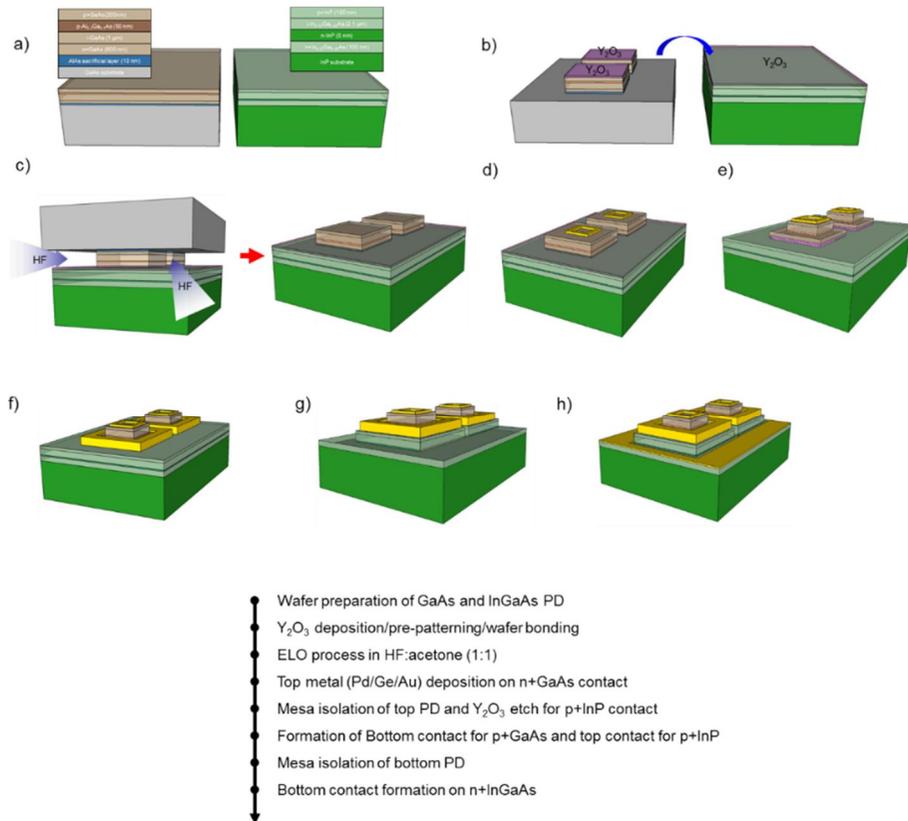
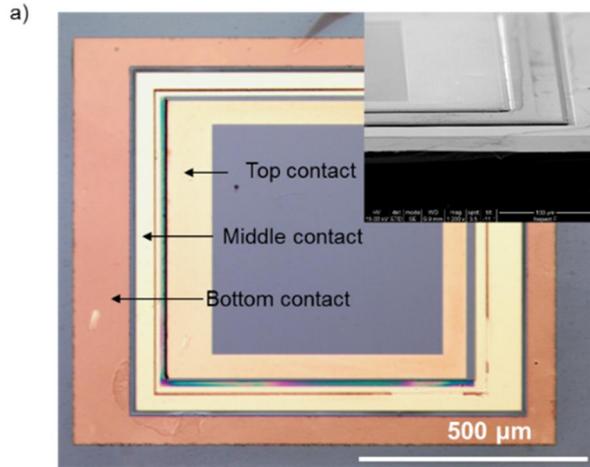


Figure 64 schematic of process flow for GaAs//InGaAs multicolor photodetectors.

Figure 65a) shows the optical microscope image of top view for the fabricated multicolor PD. Each electrode are clearly separated along to the mesa edge without any bubbles and damaged region. As shown inset of scanning electron microscope (SEM) image, obvious steps have been observed in top PD and bottom PD. Moreover, to accurately evaluate the

crystalline qualities, high-resolution XRD (HRXRD) measurement was performed using an ATXG equipped with Cu $K_{\alpha 1}$ radiation and double crystals. In Fig. 65b, θ - 2θ scan results for InGaAs PD, GaAs PD and multicolor PD. Only one peak was observed for the GaAs PD at 66.05° which corresponds to GaAs (004) peak, while two peaks were observed for InGaAs PD at 63.34° and 63.45° due with a slightly different lattice constant of $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$. The peaks 63.34 and 63.45 completely corresponds to the InP (004) InGaAs (004) peaks. Thus, XRD result of multicolor PD showed a combination of GaAs PD and InGaAs PD peaks at 63.34° , 63.45° and 66.05° which are responsible for substrate and contact layer of InP (004), InGaAs (004) and thin film of GaAs (004), respectively. These same peak positions compared with reference PD indicated that GaAs PD is successfully integrated to the InGaAs PD without strain and severe offset about vertical axis. Furthermore, the full width at half maximum (FWHM) values of InGaAs and GaAs peaks showed the 167 arcsec and 373 arcsec, respectively. It suggests that the qualities of GaAs and InGaAs PDs would be maintained during high throughput ELO process and fabrication process.



<optical microscope image of DBPD>

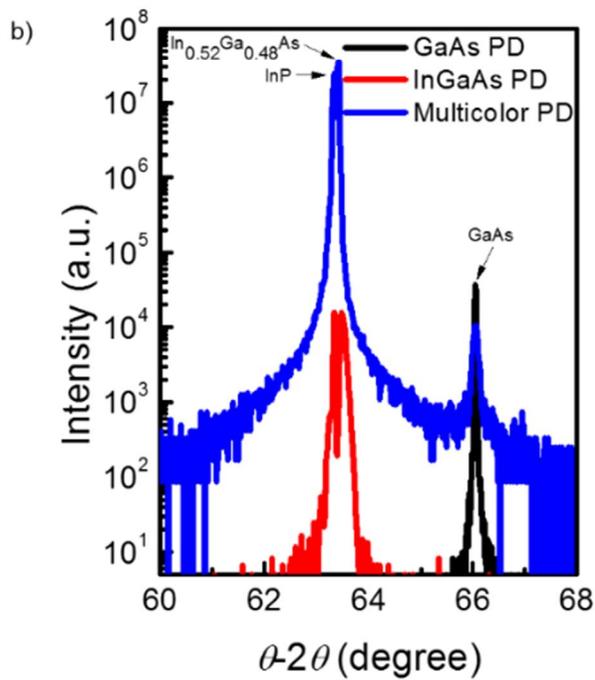


Figure 65 a) optical image of multicolor photodetectors with three terminals (top view), b) θ - 2θ measurements for reference GaAs, InGaAs photodetectors and multicolor photodetectors.

A cross-sectional transmission electron microscopy (TEM) image in Figure 66a reveals that the GaAs PD was bonded onto the InGaAs PD with good uniformity and without any voids at the bonding interface. Also, there were no visible defects and dislocations in the active layer and surfaces of both PDs thanks to the growth on proper substrates, respectively. As shown in Fig. 66b of a magnification near the bonding interface, the abrupt interfaces of GaAs, AlGaAs, Y_2O_3 , InP and InGaAs were also observed in spite of thermal annealing process. To accurately confirm the abrupt interfaces, energy dispersive x-ray (EDX) spectroscopy was carried out in associated with 6 atoms. Fig. 66c depicts the measured EDX line profile from A to A' which definitely shows boundaries of Y_2O_3 bonding layer and epitaxial layers without intermixing. While there is a concern with regard to intermixing near the different materials for epitaxy method [9], this heterogeneous integration is less considered because Y_2O_3 layer plays an important role of the diffusion barrier as well as bonding material. Fig. 66d-66e shows fast Fourier transform (FFT) patterns in reciprocal space for InP, Y_2O_3 and GaAs, respectively. The patterns of InP and GaAs strongly suggests that single crystalline quality were sustained through wafer bonding, ELO, and even in RTA process. In Y_2O_3 layer, a pattern means polycrystalline characteristic caused by partially crystallized oxides in RTA process. From these results, we have successfully fabricated the multicolor PD in single pixel area without any quality degradation. Therefore, we believe that this approach to monolithically integrate the each PD in single pixels completely permits multicolor PDs to have high material qualities, process reliability and no off-axis tilt.

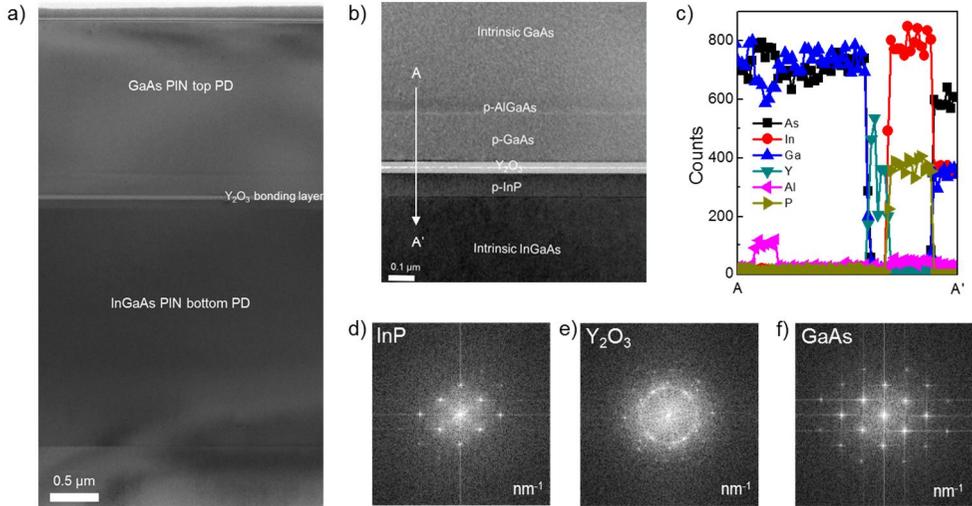


Figure 66 a) cross-sectional TEM image with low magnification for multicolor photodetectors, b) expanded TEM image at the Y_2O_3 bonding interface, c) EDAX profile in terms of each atom from A to A', d), e) and f) fast Fourier transform (FFT) patterns of InP, Y_2O_3 and GaAs, respectively.

5.3 Analysis of the electrical and optical characteristics of the fabricated multicolor PDs

To investigate the electrical characteristics of multicolor PDs, current (I) - voltage (V) characteristics of the fabricated devices were measured at room temperature shown in the schematic of Figure 67a. Measurements were conducted by a Keithley 4200 in a probe station. Because this device has a middle contact as common p-contact, sweep voltage bias directions for GaAs PD and InGaAs PD are opposite directions. Here, top GaAs PD has dimension

of $335 \times 315 \mu\text{m}^2$ and bottom InGaAs PD dimension of $425 \times 375 \mu\text{m}^2$. It was found that clear rectifying characteristics of each PD when applying the bias from -1.5V to 1.5V as illustrated in Fig. 67b. While GaAs PD exhibited $I_{\text{on}}/I_{\text{off}}$ ratio of approximately 10^7 at $\pm 1.5\text{V}$, that of InGaAs PD recorded approximately 10^4 . We made and characterized the 12 identical devices which showed the similar dark current level and $I_{\text{on}}/I_{\text{off}}$ ratio at same bias.

To compare the performances between reference and multicolor PDs, we measured the dark current properties as shown in Fig. 67c, 67d. Reference PD structures were inserted as insets. To equivalently compare performance in the dark current region of GaAs top PD, same transferred structure using GaAs PD on Si substrate was plotted. When we assessed leakage current between multicolor PD and reference PD of top GaAs, current density of 10^{-7} order of magnitude of both PDs in whole bias range [10]. The noticeable difference of both PDs cannot be observed considering slight device-to-device variations. And same comparison was performed for reference InGaAs PD and bottom InGaAs PD. Reference InGaAs PD was fabricated by using typical PD process with same metallization schemes and RTA process of multicolor PD. Although the multicolor PD went through ELO process in HF based solution, it was found that no excess dark current was not observed compared with reference InGaAs PD. Through verifying the I-V behaviors of multicolor PD, our fabrication process can be viable to make the high performance devices.

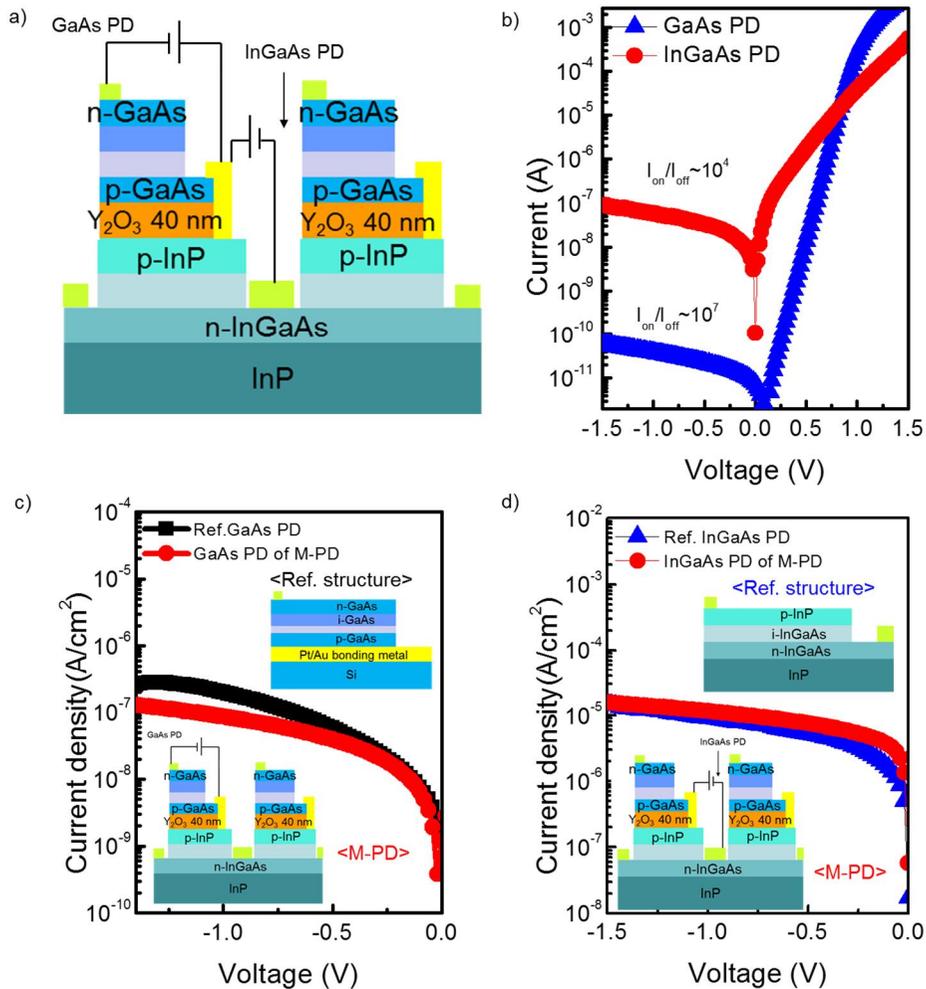


Figure 67 a) schematic of final structure for electrical measurements of multicolor photodetectors, b) GaAs and InGaAs photodetector current-voltage for multicolor photodetectors, c) and d) comparison of dark current between reference and multicolor photodetectors of GaAs and InGaAs

Then, we investigated the optical properties of the fabricated multicolor PD by using a different laser diodes such as 532nm, 638nm and 808nm and 1310 nm of tunable laser with a light coupling through lensed fiber in a

Keithely 4200 probe station as shown in inset of Figure 68 [10]. To accurately obtain the incident powers of each wavelength, all incident laser intensities are calibrated. While we have used the Si photodiode made by Thorlabs in visible wavelength ranges including 520/638/808 nm, optical intensity of 1310 nm calibration was carried out by Ge photodiode of 818-IR/CN made by Newport. Optical power meter has a resolution of nW unit. All lasers were vertically incident to the top surface of multicolor PD. Fig. 68 illustrates photocurrent characteristics of top GaAs PD with a varying the optical wavelengths. With a parameter of incident optical power of 0.9, 3, 6.5 and 10 μ W for 520 nm laser, clear photo responses were observed. Using these photo responses, we calculated the optical responsivity (R_i) of 2.2 mA/W at -1V bias through the equation as follows:

$$R_i = I_{ph} / P_{in} \quad \text{Equation.5}$$

By 638 nm laser with optical intensities of 0.47, 1.5, 4.7, 8.8 and 15 μ W, the photocurrents were linearly increased in accordance with incident powers. It corresponded to the 0.04 A/W of responsivity at -1V bias. While clear photo responses were also seen for the GaAs PD with calibrated intensities of 0.65, 1.3, 3.5, 6.5 and 12 μ W for 808 nm laser, 1310 nm laser cannot excite the any photo-carriers within the GaAs PD. It is because of a long wavelength above GaAs absorption band. The responsivity for 808 nm wavelength was calculated to be 0.15A/W. Summarized responsivity values are plotted in the Fig. 68. This top GaAs PD showed the similar performance with GaAs PD on Si reported previously. GaAs PD on Si showed the 0.06 A/W of responsivity for 635 nm wavelength. Furthermore, the relatively low

responsivity was obtained in spite of the GaAs band edge. The origin of low responsivity was caused from the n+GaAs layer of 600 nm-thick on the top surface which hindering the efficient light absorption in intrinsic region. No anti-reflection coating (ARC) have also induced the high reflectance of above 30% percent at the top GaAs PD surface. Although the loss of the incident light occurs, results related with top GaAs PD are comparable to GaAs MSM PD of multicolor PD in previous report [11].

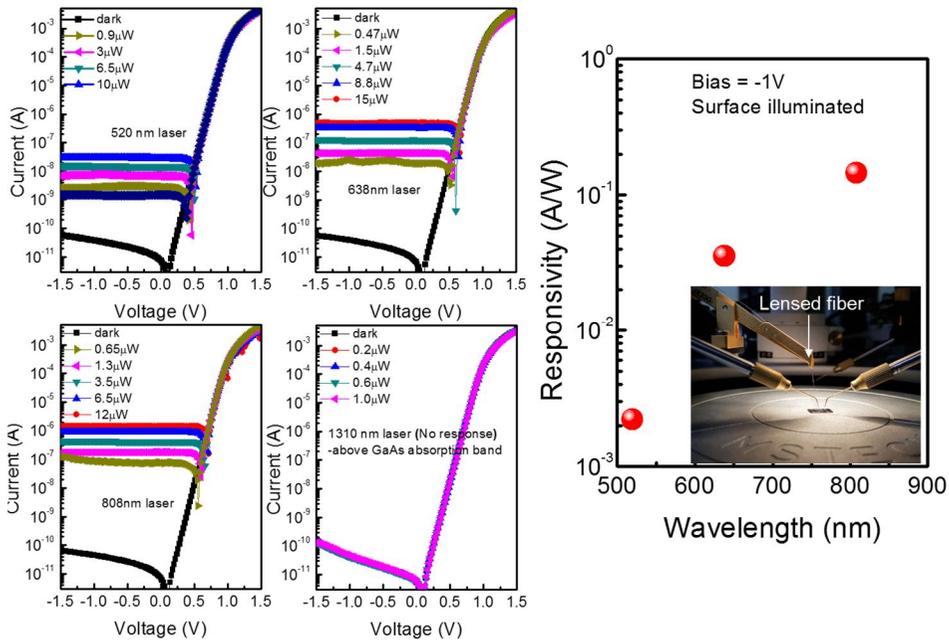


Figure 68 photoresponse and calculated responsivity of GaAs top photodetector as a function of laser wavelengths. Inset figure shows the optical measurement system by using lensed fiber.

Figure 69 shows the optical characteristics of bottom InGaAs PD as a function of incident wavelengths. When we vertically illuminated the 638 nm

and 808 nm lasers on the top GaAs PD surface, the response to the unabsorbed photons in the top GaAs PDs with same powers were observed as seen in Fig. 69a, 69b. Responsivity of 7.7 mA/W and 30 mA/W were obtained under -1V bias, respectively which suggested that the amount of unabsorbed photons in GaAs PD would be increased according to wavelength extension. In regard of a 1310 nm laser illumination, InGaAs PD showed a strong photoresponse in spite of a weak powers such as 1 μ W compared with 808 nm laser as shown in Fig. 69c. The stronger photoresponse can be attributed to adjacent laser wavelength of InGaAs band edge. And, beyond GaAs absorption edge of approximately 870 nm, a 1310 nm wavelength can pass through GaAs top PD region except for free carrier absorption originated from doped layers. As a result, the responsivity at 1310 nm was found to be 0.47 A/W which is 15 times higher than that of 808 nm.

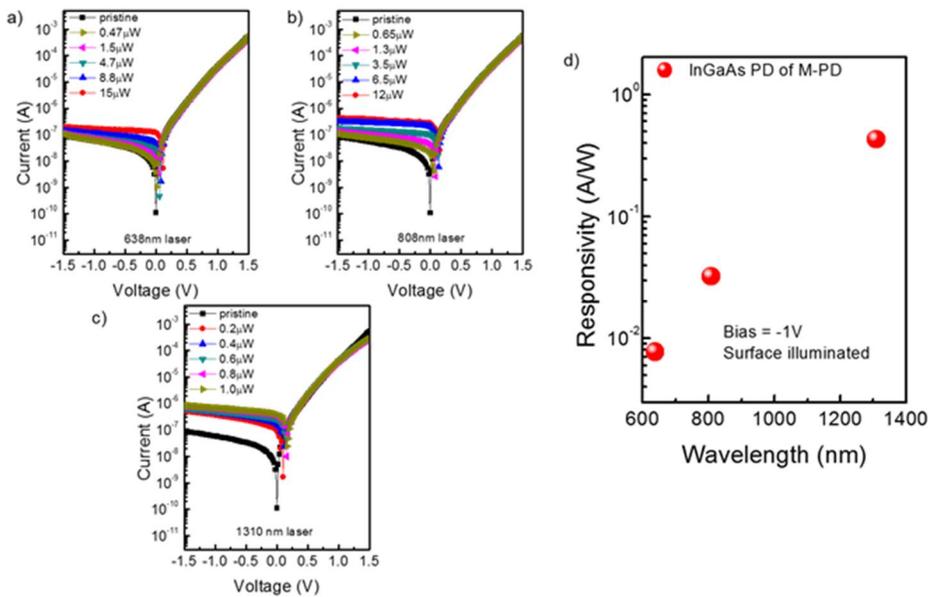


Figure 69 photoresponse and calculated responsivity of InGaAs bottom photodetector as a function of laser wavelengths.

To investigate absorption trend of bottom PD, optical intensity distribution in multicolor PD structure was simulated as seen in Figure 70. Then, Fig. 70 shows the result of optical intensity distribution for only bottom InGaAs PD region in multicolor PD structure as a function of the incident light wavelength. Incident light below 870 nm of GaAs absorption edge is considerably absorbed in top PD region, the small amount of light could be reached in intrinsic InGaAs region. That's why photoresponse can be obtained in InGaAs PD in spite of absorption loss from GaAs PD region. Between GaAs and InP absorption band, a weak absorption was observed in the top p-InP region which cannot contribute to photocurrent. However, long wavelength having above InP absorption edge is mainly absorbed in intrinsic

InGaAs region. There is still a significant amount of passed light, which reaches n-InGaAs contact layer. It should be noted that there is strong photoresponse at 1310 nm, which is definitely consistent with the higher responsivity than shorter wavelength region. These results strongly suggest that enhancement of detector performances will be further optimized through a layer thickness optimization and a selection of absorption materials.

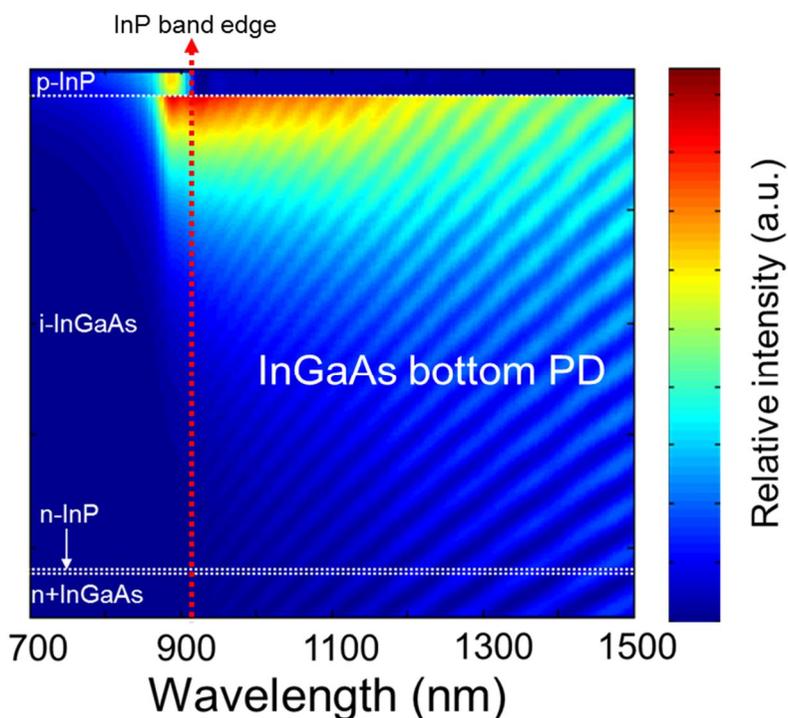


Figure 70 simulation of optical intensity distribution of bottom InGaAs photodetectors in full structure of multicolor photodetector.

Finally, we have demonstrated the electrical and optical properties of proposed multicolor PDs. For the comparison, we tabulated the benchmarks

regarding multicolor PDs which ever reported as shown in Table.7. Many researchers have reported the various formation methods for implementing the multicolor detection such as bulk epitaxy, adhesive bonding, transfer printing and packaging [11-14]. We evaluated the PDs in terms of 5 factors including material quality, vertical alignment, pixel density, array formation and freedom of wavelength selection. Even without epitaxy method, previous bonding methods have disadvantages of vertical alignment and array formation. Unlike these methods, superior characteristics especially for the increase of pixel density and array formation can be achieved from proposed formation methods. Additionally, an extra cost reduction could be obtained by using substrate recycling techniques [15, .

	GaSb//InAsSb	GaAs//InGaAs	Si//InGaAs	Si//InAsSb	GaAs//InGaAs
Integration method	Bulk epitaxy	Adhesive bonding	Transfer printing	Packaging	High throughput ELO
Material quality	▲	●	●	●	●
Vertical alignment	●	▲	▲	●	●
Pixel density	●	●	▲	x	●
Array formation	●	▲	▲	x	●
Freedom of wavelength selection	▲	●	●	●	●

Table 7 Benchmark of multicolor photodetectors which ever reported [11-14].

5.4 Summary

To verify the potential of bulk p-i-n based multicolor photodetectors, we demonstrated that the monolithic integration of visible GaAs thin film p-i-n photodetector with near-infrared InGaAs thin film p-i-n photodetector was conducted by using the high throughput ELO process. While the multicolor photodetectors showed the vertically well aligned of GaAs and InGaAs epitaxial layers confirmed by XRD measurement, good bonding interface and no visible defects were also observed by TEM image. Excellent rectifying characteristics revealed 10^7 and 10^4 on/off ratio at $\pm 1.5\text{V}$ for GaAs and InGaAs photodetectors, respectively. Additionally, similar dark currents were obtained compared with reference devices which indicated that fabrication process is well established. In optical characterization, the photoresponse cannot be observed in 1310 nm while the top GaAs photodetector showed 0.15 A/W of the responsivity at 808 nm. The responsivities of 0.47 A/W at 1310 nm and 30 mA/W at 808 nm were obtained in bottom InGaAs photodetector. These photoresponses of InGaAs photodetector in shorter wavelengths were consistent with a simulation of optical intensity distribution. These photoresponses suggest that integrated photodetectors are independently operated with each absorption region. From these results, we believe that this method can be expanded from ultraviolet of GaN material to infrared of InAsSb material for reducing the complexity of other approaches for multicolor photodetectors.

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Chapter. 6 Conclusions

In this thesis, we have concentrated on the implementation of multicolor photodetectors based on simple III-V bulk p-i-n structures with high pixel density and vertically accurate alignment. That's why multicolor photodetectors could give multi-functionality in single pixel areas. To fulfill this objective, we have investigated on three parts: 1) the development of a heterogeneous integration with high throughput to overcome conventional integration methods, 2) design and characterization of III-V bulk based photodetectors beyond conventional InSb limits, 3) a monolithic integration of bulk based p-i-n photodetectors in a single pixel via developed integration method.

Firstly, in order to heterogeneously integrate III-V thin films on rigid substrates, a low throughput of epitaxial lift off (ELO) process would be a bottleneck in spite of many advantages compared with wafer splitting and transfer printing. Thus, a high throughput ELO process was developed by using pre-patterning process and surface hydrophilization. As a result, it was found that GaAs thin films were successfully integrated on Si substrates with the fastest ELO time of 30 minutes in 2 inch wafer scale. Furthermore, with further scaling of dimensions and spacings, 5 minutes of ELO time was recorded with 95 % yield for all experiments. Then, we have fabricated electronic and optoelectronics devices to confirm actual device performances which showed the comparable performances with reference devices. It suggested that this high throughput ELO process can be applicable to fabricate various devices.

Secondly, ternary InAsSb material was proposed to cover the wavelengths ranging from SWIR to LWIR, where binary InSb material cannot be fundamentally covered. Whereas QWIPs, QDIPs and type-II photodetectors should be employed beyond MWIR range, InAsSb ternary material even in bulk layer can theoretically have 3 to 14 μm with changing As to Sb ratio in V-group. For an initial challenge, InAs_{0.81}Sb_{0.19} based p-i-n photodetector was proposed because there was no reports regarding high operating temperature photodetectors. Thus, to improve InAs_{0.81}Sb_{0.19} bulk photodetectors, the heterojunction structure with InAlSb barrier layer was designed for dark current reduction. As a result, InAsSb heterojunction photodetectors first demonstrated the higher responsivity of 15 mA/W compared with 4.5 mA/W of commercial photodetectors at room temperature. In the future, with further tuning of As and Sb ratio, LWIR photodetectors are going to be achieved.

Lastly, after securing the photodetectors with a room temperature operability ranging from visible to MWIR, monolithic integration was attempted by using visible GaAs and near-infrared InGaAs not only to prove the possibility of multicolor detection, but also to establish an optimal fabrication process. Consequently, we have achieved the successful integration of two colors with negligible off-axis along to vertical [001] direction. Additionally, multicolor photodetectors enable to independently operate for visible and near-infrared wavelengths. In multicolor photodetectors, while GaAs top PD showed the comparable responsivity of 0.15 A/W at 808 nm, InGaAs bottom PD exhibited a similar responsivity of 0.47 A/W at 1310 nm with reference photodetectors. These results suggested that bulk structure based multicolor photodetectors that fabricated by high

throughput ELO process could be expanded for various combinations of UV, visible, near-infrared, SWIR, MWIR and LWIR.

국 문 초 록

자외선부터 적외선 영역의 밴드갭을 가진 3-5 족 화합물 반도체는 단일 파장대역을 시각화하는 imager 로 널리 사용되고 있다. 그러나, 최근 사물인터넷 시대가 도래함에 따라, time of flight (TOF) 센서, 식생지수 측정, night vision 등의 새로운 응용처가 증가하고 있다. 따라서 기존의 단일파장 광 검출기가 아닌, 다중파장 광 검출기의 중요성이 증대되고 있으며, 이런 다중파장 광 검출기를 구현하기 위해서 3-5 족을 화합물 반도체의 epitaxy 방법이 흔히 사용되어 왔다. 예를 들어, 다른 격자 상수를 가진 벌크 구조를 metamorphic 성장법을 이용하여 성장하거나, 또는 양자우물, 양자점 그리고 type-II 기반의 구조가 적용되어야만 했다. Epitaxy 방법은 매우 간단한 방법처럼 보이지만, 기판과 성장하려는 물질간의 격자상수의 차이로 인해 제한되는 물질 선택, 내부 결함에 의한 성능감소 그리고 성장의 복잡함 등 여러 문제가 존재한다. 그래서, epitaxy 방법의 단점들을 회피하기 위하여, 다른 기판에서 성장된 소자의 집적을 가능하게 할 수 있는, 이중 집적 방법이 대안이 되어왔다. 이를 이용하면, 간단한 벌크 구조의 광 검출기를 결합할 수 있기 때문에 매우 유망한 방법으로 여겨지고 있다. 그러나, 이중 집적 방법의 뛰어난 장점에도 불구하고, 현재의 다중파장 광 검출기는 집적 방법의 문제로 수직 정렬 오차 및 픽셀 밀도 측면에서 한계점을 보여주었다. 따라서, 본 논문에서는

고밀도/ 고정렬된 다중과장 광 검출기 제작을 위한 3-5 족 기반의 화합물 반도체의 이중 집적 방법에 대한 연구를 진행하였다.

먼저, 3-5 족 GaAs 기반의 박막소자를 다른 기판과 이중 집적하는 연구를 수행하였다. 기존의 wafer splitting 과 transfer printing 방법과 비교했을 때 대면적 전사, 저렴한 가격 그리고 고품질 layer 등 장점들이 있는 웨이퍼 접합과 에피택셜 리프트 오프 (epitaxial lift off) 방법에 대해서 연구를 하였다. 단일 기판상에 다중과장 광 검출기를 제작하기 위해서는, rigid-to-rigid 이중 집적 방법이 반드시 필요하다. 그러나, strain 과 외부 장치를 이용하여 기판 분리를 가속화 시킬 수 있는 유연기판 상의 박막전사와 달리, 습식 식각 시 생성되는 부산물들과 가스 기포들 때문에 에피택셜 리프트 오프 방법을 이용한 rigid-to-rigid 전사에 대해서는 매우 적은 결과만이 보고되었다. 이런 문제를 극복하기 위해서, pre-patterning 과정과 표면 친수화를 통한 고속 에피택셜 리프트 오프를 제안하였다. 이 pre-patterning 과정은 AlAs 희생층의 식각 영역을 극대화 시킬 수 있으며, 기포를 빠르게 제거할 수 있다. 그리고, 친수성 용액인 아세톤을 불산과 섞어주면 점도와 표면 접촉 각을 줄일 수 있다. 이것은 식각 용액의 효과적인 침투와 부산물을 억제시키는 결과를 보였다. 결과적으로, 2 인치 크기의 GaAs 기반 박막들을 rigid 기판상에 30 분 이내로 전사가 가능했으며 이는 기존의 보고들과 비교했을 때 가장 빠른 결과이다. 또한 이 템플릿을 이용하여 광/전자 소자를 성공적으로 제작 및 동작시켰다.

두 번째로, 기존의 InSb 물질을 이용한 벌크 구조의 광 검출기가 가진 과장한계 그리고 저온동작 등의 제약들을 극복하기 위한 연구를 진행하였다. 벌크 구조의 과장 한계를 원적외선 대역까지 늘이기 위한, 3-5 족 물질 중 이상적인 물질은 인듐 아세나이드 안티모나이드 (indium arsenide antimonide) 이다. 왜냐하면 $\text{InAs}_x\text{Sb}_{1-x}$ 는 SWIR 부터 LWIR 의 해당하는 밴드 갭을 가지고 있기 때문이다. 이 물질 기반의 구조와 개발된 공정을 사용하면, 우리는 궁극적으로 자외선부터 원적외선까지의 영역을 벌크 구조만을 사용하여 다중과장 광 검출기를 구현할 수 있게 된다. 따라서, 이 물질의 가능성을 검증하기 위해서, $\text{InAs}_{0.81}\text{Sb}_{0.19}$ 의 흡수층을 가진 p-i-n 구조 기반의 광 검출기를 GaAs 기판상에서 성장하였다. 고온에서 동작 특성을 향상시키기 위하여, 최적의 InAlSb 배리어를 TCAD 로 디자인하였다. 이러한, InAsSb/InAlSb 이중 접합 광 검출기는 분자선 증착 장비를 이용하여 성장되었다. 그 결과로, 우리는 비슷한 Sb 조성을 가진 InAsSb 기반의 광 검출기들 중에서, 처음으로 중적외선 대역의 이중 접합 구조의 광 검출기를 상온 동작 하는 것을 시연하였다. 게다가, 그것은 상용화된 광 검출기보다 높은 광 응답 특성(15 mA/W)을 보여주었다. 이 상온에서 동작하는 중적외선 광 검출기는 InSb 광 검출기에 사용되는 Dewar 를 제거함으로써, 최종 검출기 시스템의 부피를 감소 시킬 수 있다. 이 실험으로부터, 벌크 구조로 원적외선 대역을 검출하기 위한 InAsSb 물질의 큰 잠재성이 있다는 것을 의미한다.

마지막으로, 벌크 구조의 집적을 통한 다중파장 광 검출기의 실현이 가능한지 확인하기 위해서 모놀리식(monolithic) 집적에 관한 연구를 수행하였다. 확보된 상온 동작이 가능한 가시광선부터 MWIR 검출 파장을 가진 광 검출기들 중에서, 최적의 제작 순서를 확립하기 위해서 물질에 관한 성숙도가 높은 가시광선 GaAs 그리고 근적외선 InGaAs 광 검출기를 사용하였다. 가시광/근적외선 대역의 다중파장 광 검출기를 형성하기 위해서, GaAs 광 검출기를 InGaAs 광 검출기 상으로 개발된 고속 에피택셜 리프트 오프 기법을 사용하여 전사하였다. GaAs 광 검출기와 InGaAs 광 검출기는 off-axis 없이 수직으로 잘 정렬되었음을 x-ray 분광법을 이용하여 확인하였다. 또한, 각각의 광 검출기의 기준 소자들과 비교했을 때 비슷한 암 전류가 나타났다. 마지막으로, 레이저 입사를 통해, 두 개의 광 검출기 대한 광 반응은 물질 특성들에 따라 가시광과 근적외선에서 각각 명확하게 나타났다. 이러한 결과들은 고속 에피택셜 리프트 오프 기법이 높은 픽셀 밀도 및 거의 완벽한 수직 정렬도를 갖는 한 기관상의 벌크 기반의 다중파장 광 검출기를 집적할 수 있다는 것을 의미한다. 미래의 목표하는 응용처에 따라, 원하는 파장들을 갖는 광 검출기를 벌크 구조로 간단하게 성장할 수 있고, 다중파장 이미징 시스템을 제작할 수 있다.

주요어:

이종 집적, 3-5 족 화합물 반도체, 에피택셜 리프트 오프, 광
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LIST OF PUBLICATIONS

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(7 first authored paper (1 in preparation), 16 co-authored paper)

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