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Ph.D. DISSERTATION

**Growth and Leakage Current Control
of High-k SrTiO₃ Thin Films Grown
via Atomic Layer Deposition**

by

Sang Hyeon Kim

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DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

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Growth and Leakage Current Control of High-k SrTiO₃ Thin Films Grown via Atomic Layer Deposition

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by

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**A thesis submitted to the Graduate Faculty of Seoul National
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Abstract

A DRAM cell consists of one capacitor and one transistor. In a DRAM cell, a transistor plays a role of selecting a cell to be read or written in a DRAM cell array, and a capacitor stores charges to record '0' and '1' data. In order to integrate DRAM devices, it is essential to develop various process element technologies including transistors and capacitors. Among them, capacitor element technology is a crucial technology for ensuring sufficient capacitance in a small area. The currently produced DRAM has a sandwich structure (ZAZ) with ZrO₂-based Al₂O₃ as a high-k film. This thesis reported the growth behavior, the low-temperature deposition method and the leakage current reduction of the high-k SrTiO₃ (STO) by atomic layer deposition.

In this thesis, Sr(ⁱPrCp)₂ and Ti(OMe)₃(CpMe₅) were used with strontium precursor and titanium precursor with ozone and water as an oxygen source, respectively. The growth behavior of the STO thin film deposition process was studied, and various thin film characteristics such as electrical characteristics analysis through the fabrication of metal-insulator-metal (MIM) structure capacitors were also evaluated.

First, the growth behavior of the upper thin film of the STO thin films deposited in two stages was studied. The annealing temperature of the 5 nm thick underlayer deposited on amorphous phase was varied from 450 to

650 °C to vary the crystallinity of the underlayer. The crystallization and growth behavior of the upper thin film was analyzed without depositing the upper thin film deposited at 650 °C at a high temperature. Amorphous and crystalline materials were mixed at a crystallization temperature of 550 °C to 600 °C, and the deposited thin film also depends on the crystallinity of the underlying thin film. Further, when Ru is deposited as a lower substrate, oxygen is diffused between the crystal grains of the lower STO thin film, and the growth rate of the upper STO thin film is increased. This excessive oxygen supply phenomenon does not occur when silicon is used as the lower substrate. When the heat treatment temperature of the lower STO thin film is higher than 600 °C, almost all of the lower STO thin film is heat treated, and the upper STO thin film is also crystallized with the same tendency. As a result, an equivalent oxide film of 0.52 nm was formed at a leakage current of 2.5×10^{-8} A/cm²

Second, the deposition temperature of the lower STO thin film was deposited at a low temperature of 230 °C. Moreover, the upper STO thin film was deposited at a high temperature of 370 °C. The STO thin film has high leakage current characteristics associated with low band gap energy and ruthenium metal having a high work function as the electrode material should be applied in order to lower the leakage current. However, reactions that are similar to chemical vapor reactions occur at ruthenium and STO interfaces with unreasonably high reactivity. This high reactivity is because the ruthenium undergoes redox process and supplies excess oxygen to the

strontium oxide film having a considerable thermodynamic forming energy. The deposition temperature was lowered by annealing at a low temperature of 230 °C, suppressing the abnormal reaction, and the microcracks of the lower STO thin film were reduced to form a denser lower STO thin film and increase the density of the STO thin film deposited on the upper side. As a result, the bulk dielectric constant increased from 101 to 167 under the conditions of deposition of the lower STO thin film at a high temperature of 370 °C. However, there is a disadvantage in that the carbon doping increases and the thickness of the equivalent oxide film at the interface increase as the deposition time increases at the low-temperature deposition.

Third, Al was doped to reduce the high leakage current of STO thin films with low bandgap energies of 3.0 to 3.2 electron volts. One cycle of Al oxide was doped into the STO thin film, and the Al doping positions were evaluated between the lower STO thin film and the ruthenium substrate and at the top of the upper STO thin film. When the bottom Al is doped, crystallization of the lower STO thin film is lowered, and the dielectric constant of the upper STO thin film is lowered from 149 to 71. When the uppermost STO thin film is doped with Al, crystallinity of the crystallized STO thin film is not significantly affected. However, in both cases, the decrease in leakage current is more than 20 times, which is a result of improvement in the relationship between the leakage current density and the equivalent oxide film. As a result, the thickness of the equivalent oxide film at 0.8 volt, which is the operating voltage of the DRAM, decreases from 0.71

nm to 0.63 nm, and the physical thickness also decreases from 10.3 nm to 8.6 nm.

In conclusion the behavior of the STO thin film deposited on the Ru electrode in two steps was analyzed to analyze the crystalline and amorphous growth behavior at the critical temperature, and the deposition temperature was lowered to suppress the non-ideal deposition phenomenon. In order to overcome the low band-gap energy of the STO film, Al was doped to reduce the t_{ox} to 0.63 nm and the t_{phy} to 8.6 nm at the operating voltage of 0.8V.

Keywords: DRAM capacitors, SrTiO₃, atomic layer depositions, seed layers, two-step growths, growth temperature, crystallization, Al-doping, leakage current

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List of Abbreviations

AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
BE	Bottom Electrode
CBO	Conduction Band Offset
CVD	Chemical Vapor Deposition
C-V	Capacitance-Voltage
DRAM	Dynamic Random Access Memory
E_g	Bandgap Energy
GAXRD	Grazing Angle incidence X-ray Diffraction
I-V	Current-Voltage
J_g	Leakage current density
MIM	Metal-Insulator-Metal
PDA	Post-Deposition Annealing
RAM	Random Access Memory
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscope
TE	Top Electrode
TEM	Transmission Electron Microscope
STO	SrTiO ₃ , strontium titanate
t_{ox}	Equivalent oxide thickness
t_{phy}	Physical oxide thickness

VBO	Valence Band Offset
XPS	X-ray photoelectron Spectroscopy
XRD	X-Ray Diffraction
ϵ_r	Dielectric constant

1. Introduction

1.1. Dynamic Random Access Memory

In modern computers, Dynamic Random Access Memory (DRAM) is a memory capable of realizing high speed and high density, and it plays the role of main memory. It is virtually impossible to replace DRAM in terms of operating speed, integration level, and device reliability in the development of various next-generation memory products (flash memory, magnetic memory, phase change memory, resistance change memory), and DRAM is still expected to function as main memory. A DRAM cell consists of one transistor and one capacitor. In the DRAM cell, the transistor plays a role of selecting a cell to be read or written in the DRAM cell array, and the capacitor stores the charge to record '0' and '1' data. In order to integrate DRAM devices, it is essential to develop various process element technologies including transistors and capacitors, among which capacitor element technology is a key technology for ensuring sufficient capacitance in a small area. For the operation of the DRAM device, a capacitance of 15 - 20 fF per cell was required regardless of the size of the device. Recently, however, introducing an air gap in the inter-level dielectric (ILD) between the bit-lines (BL) can significantly reduce the BL capacitance and significantly reduce the demand for cell capacitance. Nevertheless, the capacitance of 8 - 10 fF per cell is still

required, which is very difficult to satisfy in a DRAM having a design rule of 15 nm or less.^[1] While the capacitance is proportional to the active area occupied by the capacitor, as the degree of integration of the DRAM device increases, the area allocated to the capacitor rapidly decreases, securing the necessary capacitance is the biggest obstacle to the development of the next generation DRAM device.

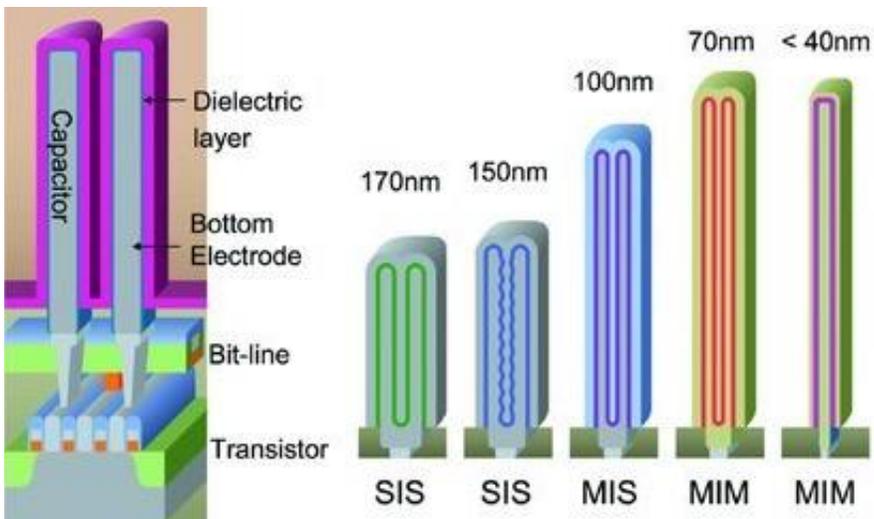


Figure 1-1 Schematic diagram of DRAM cells and a summary of the DRAM capacitor technology evolution²

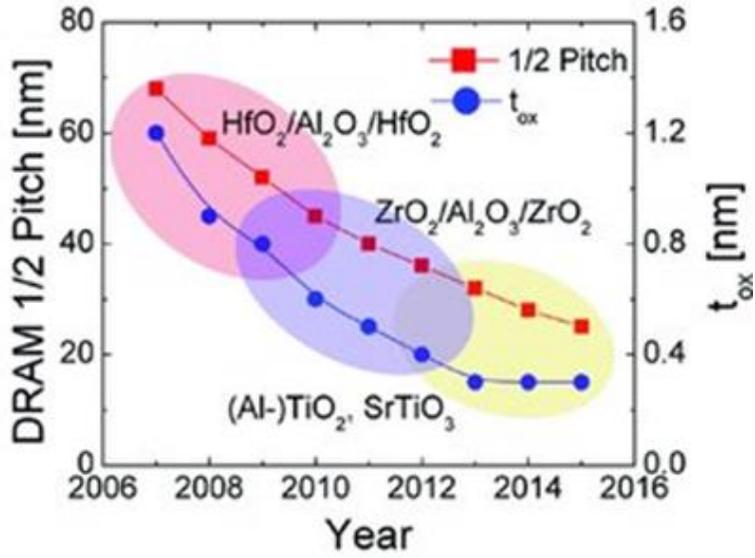


Figure 1-2 Evolution in the capacitor dielectric and electrode material ²

In order to secure the required capacitance, a three-dimensional capacitor is used to increase the active surface area. (Figure. 1-1, Figure 1-2) ². However, the application of such a three-dimensional capacitor has a limitation in increasing the effective surface area due to structural weakness. The capacitance of the capacitor is proportional to the dielectric constant of the dielectric in addition to the active surface area of the capacitor. Therefore, studies are being conducted to increase the capacitance by applying a high dielectric constant dielectric layer having a dielectric constant higher than that of conventional SiO₂, SiN_x, Al₂O₃, ZrO₂, etc.³ However, in the case of a material having a high dielectric constant, it has disadvantages of a high leakage current due to a small band gap, and development of an appropriate material and development of a new electrode material suitable for the material are required(Figure 1-3).

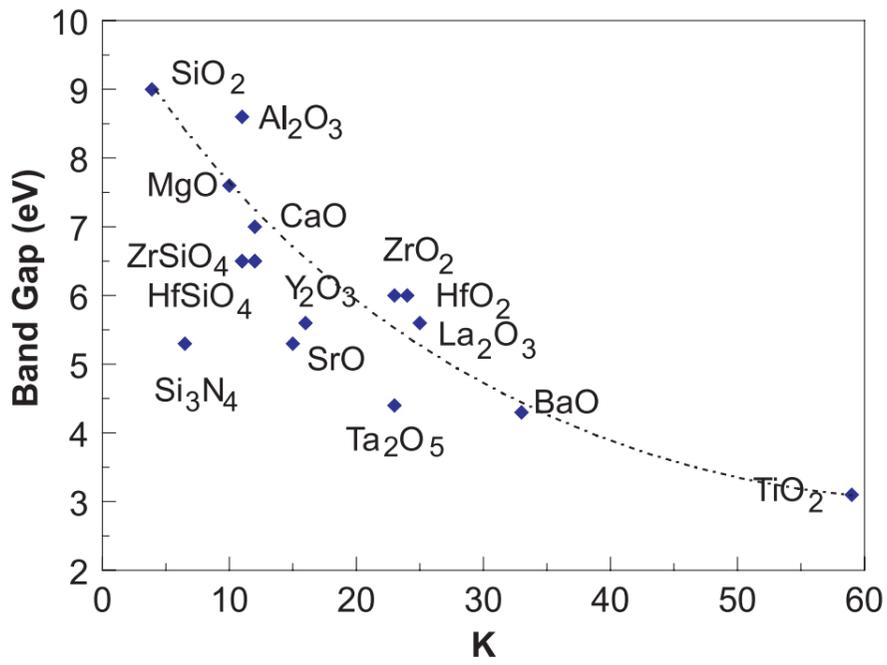


Figure 1-3 Static dielectric constant vs. band gap for high-k materials ⁴

The SrTiO₃ (STO) thin film has a high dielectric constant of 100 or more. For STO materials, the perovskite structure in which the Sr atom is located at each corner of the cube, the O atom is located at the center, and the Ti atom is located at the center of the body. (Figure 1-4) (Table 1-1)

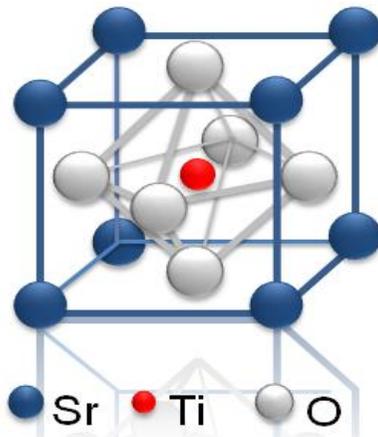


Figure 1-4 SrTiO₃ crystal structure

Property	Value	
Molecular weight [g/mole]	183.52	
Density [g/cm ³]	5.12	
Melting point [°C]	2080	
Refractive index	2.31~2.38	
Band gap [eV]	3.2	
Lattice parameter [Å]	3.905	
Crystal structure	~105K	Tetragonal
	105K~	Perovskite
Dielectric constant	300	

Table 1-1 SrTiO₃ properties⁴

1.2. Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a deposition method which is based on the chemical vapor deposition (CVD).^{5,6,7} The main difference in ALD compared with CVD is separate feeding of precursor and reactant gas to achieve a precise control over film thickness. One cycle of ALD process is consisted of four steps as shown in Figure 2: source injection, purge, another source injection, and purge. Source can be chemical precursor with reactive ligands attached to the target element or reactant such as oxidant or reductant. In ideal case, the thickness of deposited film is dependent only on the number of cycles. Sequential control of the growth in ALD is based on unique characteristics which is self-limiting mechanism between the reaction surface and source. There are two kinds of adsorption when the precursor is exposed to the substrate: physisorption and chemisorption. Physisorbed precursor has weak bonding energy with substrate involving Van der Waals force but chemisorbed precursor forms strong chemical bonds by ionic or covalent bonding with the surface.

At first step, precursor exposed on surface and surface group forms a tight binding monolayer on the surface. The following purge step removes all the physisorbed precursors from the surface. When the next reaction gas is supplied into the chamber, reactant gas faces the surface monolayer and produces the target layer with gas byproducts. The unnecessary byproducts

are purged out through the final step and consequently, only the desired layer remains on the substrate. By repeating these steps for certain cycles, the final wanted film is deposited in the target thickness. With this deposition method, due to the self-limited mechanism of process, materials grow layer by layer in the shape of substrate structure which is as complex as source molecules can reach to. It does not matter whether the target is three dimensional or not and intensely conformal film can be obtained on high aspect ratio structure.¹ However, since the process of periodically supplying the raw materials one by one and removing the excess is required to be repeated repeatedly, the deposition rate is slow and it is difficult to apply it widely to the mass production line (Figure 1-5).

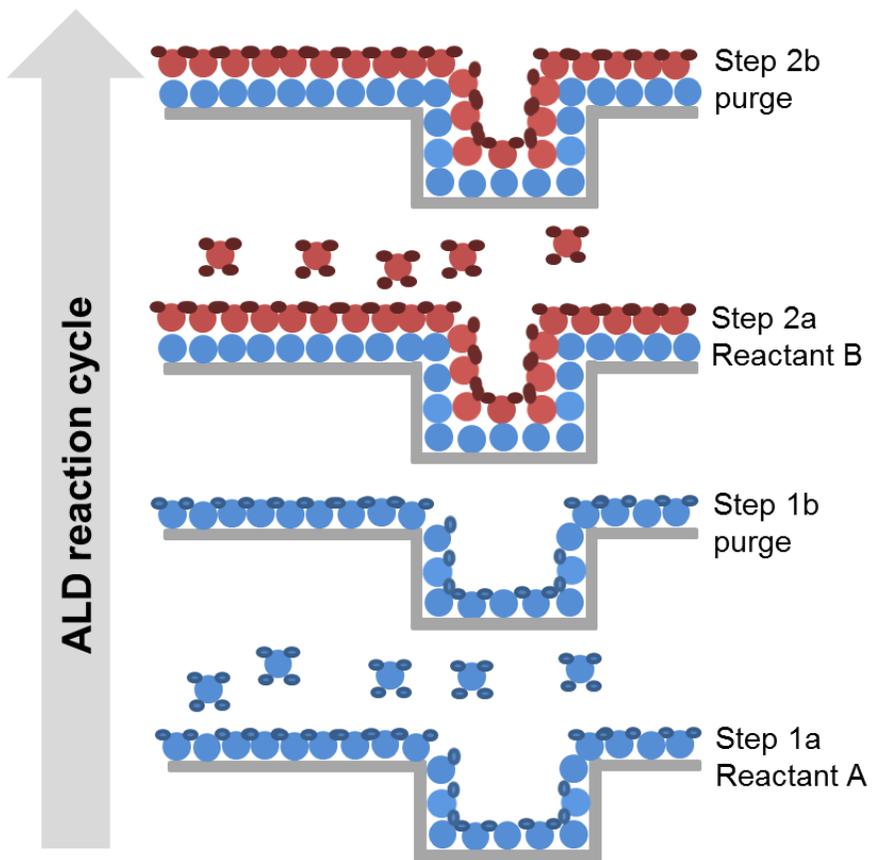


Figure 1-5 ALD reaction cycle ⁸

1.3. Development of the STO thin films

STO thin films were deposited in 1990 in Helsinki, Finland using $\text{Sr}(\text{iPr}_3\text{Cp})_2$ and $\text{Ti}(\text{O-iPr})_4$ (TTIP, iPr = isopropyl, Cp = cyclopentadienyl). Due to the high leakage current characteristics of 10^{-5} A/cm^2 (@ 1 V) in the thin film of 100 nm thickness, the required level of DRAM below 20 nm was not reached.⁶ Hwang's group reported on the results of the research that have progressed significantly more than the above results. At the beginning of STO ALD research, $\text{Sr}(\text{tmhd})_2$ (tmhd = 2,2,6,6-tetramethyl-3-5-heptanedione) as Sr precursor and TTIP as Ti precursor and H_2O plasma as an oxygen sources. Hwang's group reported a STO thin film process with excellent step coverage and composition uniformity in a three-dimensional hole structure with hole diameter of 130 nm and aspect ratio of 8.

However, TTIP with high reactivity with water (H_2O) could not raise the deposition temperature above 300 °C due to low thermal stability. The STO grown at a temperature of 300 °C or less has a very low dielectric constant of about 20 due to the formation of an amorphous phase. In order to change into a crystalline material having a high dielectric constant, microcracks are generated during annealing at 500 °C, TiCl_4 , which is another precursor, has higher reactivity and thermal stability than TTIP, but it is very difficult to remove SrCl_2 , which is formed as a by-product, and there is a problem that the concentration of Cl impurity is high. Therefore, application of a precursor capable of deposition at a high temperature of 300 °C or more was

essential for suppressing leakage current.(Figure 1-6)

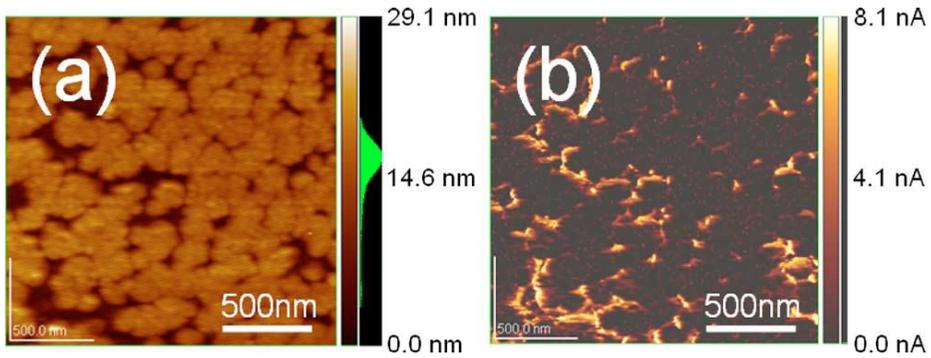


Figure 1-6 The topographic (a) images and (b) local current of the STO film without any seed layer which was post-annealed at 600 °C for 1 min in N₂ atmosphere.⁹

Therefore, it was necessary to deposit the STO thin film at high temperature to overcome the electrical characteristic degradation, especially the high leakage current phenomenon, caused by the micro-crack generated in the low film density and the subsequent heat treatment process. Ti(O-iPr)₂(tmhd)₂, which is a Ti precursor with excellent thermal stability, was introduced to raise the deposition temperature from 300 °C to 390 °C and to improve the thickness reduction during the heat treatment. The O-iPr ligand of Ti(O-iPr)₂(tmhd)₂ begins to decompose at 257 °C, but the tmhd ligand

begins to decompose at 427 °C, The two tmhd ligands have the advantage of a complete atomic layer deposition process in which Ti is adsorbed onto the surface of the film and then removed by a subsequent oxygen source.(Figure 1-7)

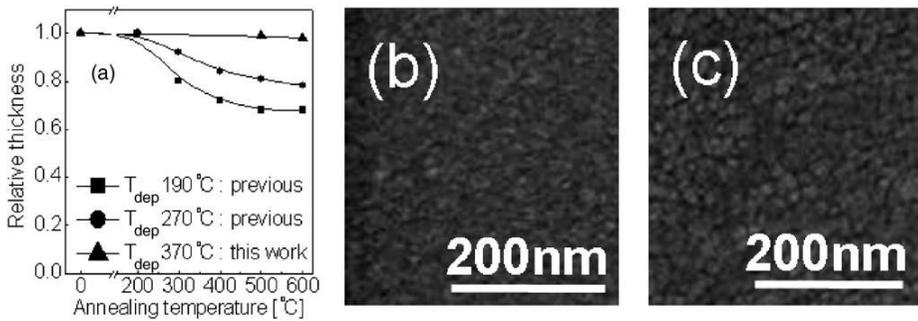


Figure 1-7 (a) The variations in the relative thickness of the STO films as a function of the PDA temperature and SEM surface morphology of (b) the as-deposited and (c) after PDA.¹⁰

Since the STO thin film crystallized by in-situ crystallization is less likely to cause micro-cracks than the ex-situ crystallization method requiring subsequent annealing and has excellent leakage current characteristics, the seed STO thin film is thinly deposited, crystallized by heat treatment, STO thin films were deposited on the crystallized seed thin film by a 2-step process. More precisely, precursors of $\text{Ti}(\text{O-iPr})_2(\text{tmhd})_2$ and $\text{Sr}(\text{tmhd})_2$ were

used. The thickness of the seed thin film in the 2-step process was set to about 3 nm, and the main thin film was grown after the crystallization heat treatment in the nitrogen atmosphere, and the subsequent STO layer was crystallized in-situ to obtain excellent electrical characteristics. (Fig. 1-8). Through this process, we found that the optimization of the 2-step process is an essential factor for obtaining excellent electrical characteristics.

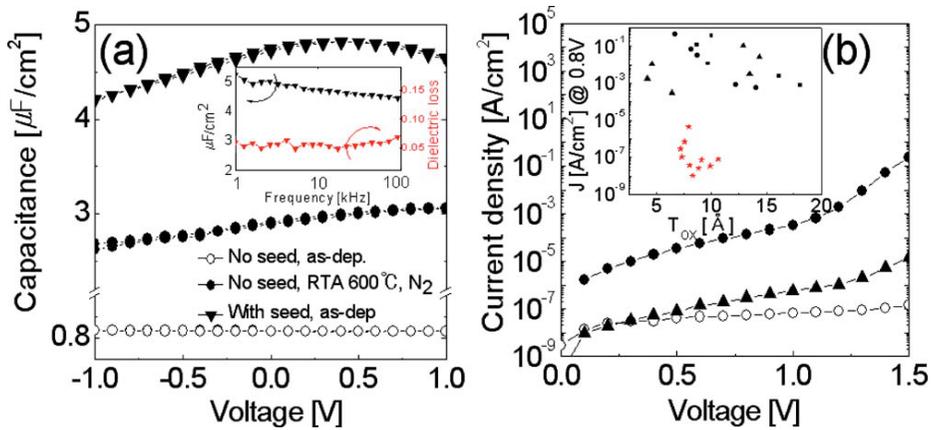


Figure 1-8 (a) Capacitance-voltage C-V and (b) current density-voltage J-V curves, respectively, of 20-nm-thick STO films grown at 370 °C on a Ru electrode. The inset Figure in (a) shows the variations in the capacitance density and dielectric loss as a function of measurement frequency of the sample with the seed layer. The inset J vs t_{ox} graph in (b) shows the superior performance of the STO films with the high deposition temperature process (red) compared with the low temperature process (black).¹⁰

However, $\text{Sr}(\text{tmhd})_2$ with β -diketonate as a Sr precursor tends to form oligomers even at room temperature and at low vapor pressures of only 0.1 Torr at 230 °C. In addition, it has a very low reactivity with water, and when it reacts with another oxygen supply ozone, SrCO_3 is formed. Due to the nature of these Sr precursors, the STO process had a very low deposition rate of 0.017 nm per cycle. $\text{Sr}(\text{iPr}_3\text{Cp})_2$ with a cyclopentadienyl (Cp) ligand, which is a more reactive Sr precursor, and $\text{Ti}(\text{O-iPr})_2(\text{tmhd})_2$ as a Ti precursor were used to improve the mass productivity. In-situ to develop a process that can meet the low leakage current characteristics of $3 \times 10^{-8} \text{ A/cm}^2$ (@ 0.8 V), high permittivity of ~146, and excellent equivalent oxide thickness of 0.57 nm at 10 nm physical thickness. (Fig. 1-9). On the other hand, the Cp ligand, which is 2.54 eV more than the β -diketonate ligand which binds to the core metal of Sr at 4.49 eV, is highly reactive with water because of its weak binding ability with the center metal. Rather, $\text{Sr}(\text{iPr}_3\text{Cp})$ Chemical vapor deposition (CVD) tends to be promoted rather than the ALD process by the hydroxyl group of water used as the surface oxygen source.

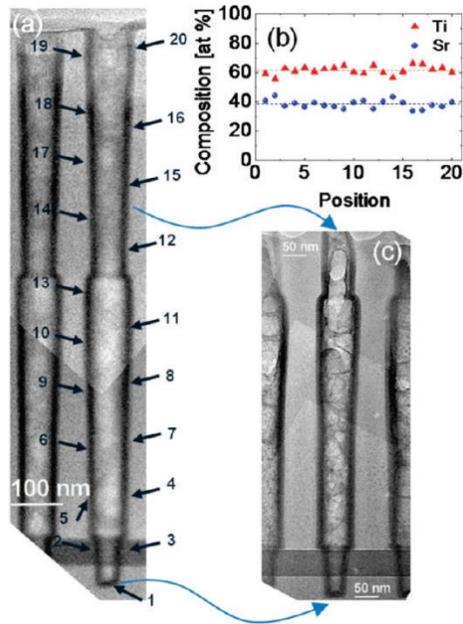


Figure 1-9 (a) (c) Cross-section transmission electron microscopy and energy dispersive spectroscopy results that show a highly conformal thickness as well as composition step coverage(> 95%) of the STO film inside a capacitorhole structure deposited at 370 °C. The open diameter is 108 nm and hole depth is 1.08 μm , giving an aspect ratio of ~ 10 .¹¹

Since STO must be deposited at high temperature, a ligand such as tmhd, which has a strong bond between the central metal and the ligand, should be used for high thermal stability of the precursor, while an oxidizing oxygen source such as ozone should be used for thin film deposition. However, ozone with strong oxidization tends to oxidize the Ru substrate used as the lower electrode in-situ to RuO₂, and in the subsequent deposition of TiO₂ or SrO, RuO₂ is reduced to Ru, It tends to promote growth, especially over-growth of SrO. (Figure 1-10). In this STO thin film Ru substrate, excessive growth of Sr element at the initial stage of growth caused not only fine control of thickness but also generation of SrCO₃ which causes deterioration of electrical characteristics in MIM capacitor fabrication. The excess growth of Sr was caused by a violent reaction between the gaseous Sr(ⁱPr₃Cp)₂ and the oxygen ions contained in the Ru substrate.

In order to prevent excessive growth of Sr, previous studies have deposited a TiO₂ layer with a thickness of 3 nm or more before STO growth to prevent direct contact between Ru electrode and Sr precursor. This method successfully suppressed the initial overgrowth of Sr. However, considering that the physical thickness of the entire dielectric film is only 10 nm, allocating it to the 3 nm or lower TiO₂ barrier layer can be attributed to the total dielectric property of the DRAM capacitor It caused a great loss. Therefore, previous studies have attempted to solve this problem by applying Al₂O₃, which has lower oxygen diffusion coefficient than TiO₂, to the barrier layer instead of TiO₂. As a result, it was found that only the 0.4 nm thick

Al_2O_3 layer can prevent the excessive growth of Sr and that the 1 nm Al_2O_3 layer has the same blocking effect as the 3 nm TiO_2 layer. In addition, STO thin films of 3 nm thickness were first deposited and then annealed to crystallize the STO thin films on the seed layer at 370 °C. The thin films grown on the top were also crystallized in-situ without further heat treatment. The STO grown on 1 nm thick Al_2O_3 / Ru has an equivalent oxide thickness and thickness. Calculated from the slope of the physical thickness graph, the bulk dielectric constant was 173. However, the adverse effect on the capacitance of the Al_2O_3 layer was judged to be more serious than the TiO_2 layer. (Figure 1-10, 1-11)

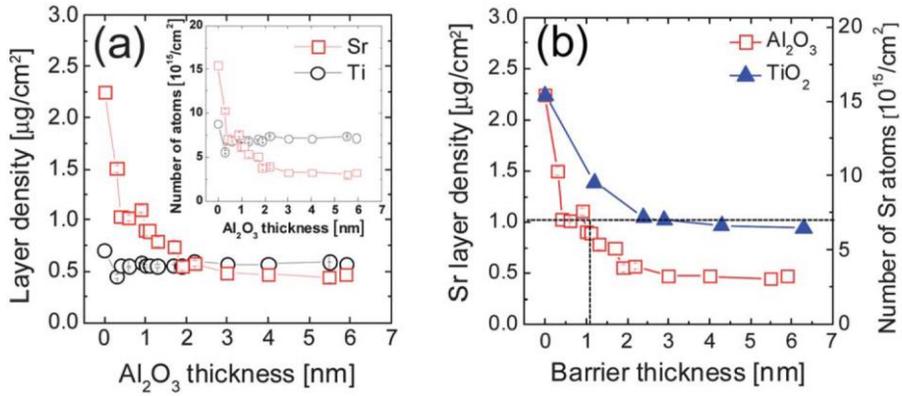


Figure 1-10 (a) Variations in the layer densities (inset numbers of Sr and Ti atoms) of the STO films deposited on Al_2O_3 barriers as a function of Al_2O_3 barrier thickness and (b) comparison between the blocking effects of the TiO_2 and Al_2O_3 barriers on Sr incorporation.¹²

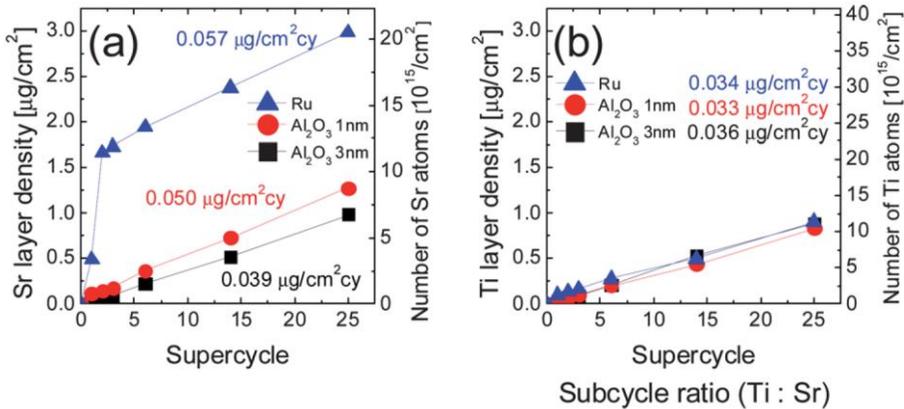


Figure 1-11 Variations in the (a) Sr layer density (number of Sr atoms), (b) Ti layer density (number of Ti atoms), as a function of STO super-cycle number on Ru, 1 nm $\text{Al}_2\text{O}_3/\text{Ru}$, and 3 nm $\text{Al}_2\text{O}_3/\text{Ru}$ substrates¹²

1.4. Bibliography

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2. Effect of the Annealing Temperature of the Seed Layer on the Following Main Layer

2.1. Introduction

With the increasing interest in higher-permittivity materials for the next-generation dielectrics of the dynamic random access memory (DRAM) capacitor, the atomic layer deposition (ALD) of SrTiO₃ (STO) films has been intensively studied.¹⁻¹⁴ To derive their advantages compared to the other high-*k* dielectric candidates, the STO films should be well crystallized into a perovskite structure to achieve a dielectric constant higher than 100 in thin films.¹⁵⁻¹⁸ The ex-situ crystallization of the STO film through the conventional post-deposition annealing (PDA) method, however, caused a serious leakage current problem.¹⁹ The authors' group suggested the use of a "two-step growth method" to achieve both a high dielectric constant and a low leakage current level,¹⁹ where a first thin STO layer (seed layer <~5 nm) was deposited and crystallized via rapid thermal annealing (RTA), and a second STO layer (main layer) was subsequently grown on the crystallized seed layer. In this way, the main layer was in-situ-crystallized without any PDA, causing fewer defects, which were the potential leakage paths.

As the seed layer acts as the template for the growth of the main layer, its properties significantly affect the properties of the main layer. In the authors'

previous study, excessively thick seed layers ($\gg 5$ nm) degraded the insulating performance of the capacitors while a 3- to 5-nm-thick seed layer showed the best electrical property when the seed layer was annealed under the optimized condition.¹⁹ The RTA temperature of the seed layer was also found to be a critical parameter influencing the performance. The RTA at 750 °C caused adverse chemical interactions between the STO seed layer and the Ru substrate.¹⁹ Also, the cooling rate after the crystallization annealing of the seed layer affected the layer's surface morphology.²⁰ These previous results show that the seed layer processing conditions have a tremendous influence on the surface morphology of the main layer, the crystallinity of the entire film, and the accompanying electrical performances. Among the relevant processing conditions, the seed layer RTA temperature was found to be the most important factor, critically affecting the main layer properties. An extensive investigation of this critical aspect is lacking, however, despite its importance. Especially, the possible growth rate difference in the main layer STO growth on the well-, less-, or non-crystallized seed STO layer has not been examined in detail.

$\text{Sr}(\text{}^i\text{Pr}_3\text{Cp})_2$ and $\text{Ti}(\text{CpMe}_5)(\text{OMe})_3$ are the most promising Sr and Ti precursors, respectively, for STO deposition at a temperature as high as >350 °C for in-situ crystallization with the aid of two-step growth (Pr, Cp, and Me are propyl, cyclopentadienyl, and methyl groups, respectively).²⁰ The large reactivity of these cyclopentadienyl precursors (especially the Sr

precursor), however, causes uncontrollable overgrowth through the oxygen supply from the O₃-oxidized Ru substrate during the initial ALD growth, where metal Ru is the most significantly studied bottom electrode (BE) for the ALD STO film.^{12, 21, 22} Therefore, accurate control of the seed layer process is crucial to achieve the promising electrical properties of the STO film. This is because the rate of oxygen permeation through the thin seed layer from the atmosphere to Ru and from oxidized Ru to the growing film surface is very dependent on the crystallinity, density, and possible involvement of the nano- or microvoids or cracks within the seed layer. This oxygen migration behavior critically influences the growth rate, film composition, and crystallization of the main layer.

In this study, therefore, the effects of the RTA temperature of the seed layer on the growth behavior of the main layer and the electrical properties of capacitors with Ru-based electrodes were carefully examined. From the results, it was found that the 600 °C RTA temperature, which was extensively adopted in the authors' research, is indeed the best condition for achieving the optimum electrical results.

2.2. Experimental Methods

STO films were deposited with a 4-inch-wafer traveling-wave-type reactor (CN-1 Co., Plus-100) via the thermal ALD method. $\text{Sr}(\text{Pr}_3\text{Cp})_2$ and $\text{Ti}(\text{CpMe}_5)(\text{OMe})_3$ (both synthesized by Air Liquide Company) were used for the growth of the SrO and TiO_2 sublayers, respectively. The canisters of the Sr and Ti precursors were heated to 80 and 70 °C, respectively, and were delivered by Ar carrier gas at 200 sccm. The working pressure was maintained within the 600-700 mTorr range, and the substrate temperature was set to 370 °C. H_2O cooled to 5°C and O_3 with a 250 gm^{-3} concentration were used for the SrO and TiO_2 depositions, respectively. 30 nm Ru/17 nm Ta_2O_5 /(100) oriented Si and bare (100) plane oriented Si (with native oxide) were employed as the substrates, where the Ru and Ta_2O_5 layers were grown via DC sputtering and chemical vapor deposition (CVD), respectively. The ALD of the TiO_2 and SrO thin films consisted of precursor feeding (3 sec), Ar purge (5 sec), oxygen source feeding (2 sec), and Ar purge (5 sec). Stoichiometric STO thin films were constructed by combining the TiO_2 and SrO subcycles. Three-time five- TiO_2 /one-SrO subcycles and ten-time three- TiO_2 /four-SrO subcycles were adopted to grow seed layers on Ru and Si substrates, respectively. The thickness of the as-deposited seed layer was ~ 5 nm. The ALD sequences for the main STO layers consisted of the 2:1 and 1:1 TiO_2 :SrO subcycle ratios for the Ru and Si substrates, respectively. For both the seed and main layer STO growth, the TiO_2 :SrO subcycle ratio was

changed to achieve the ~5:5 stoichiometric Sr:Ti ratio on both the Ru and Si substrates. RTA was performed under a N₂ atmosphere for 2 min, and the temperature was varied from 450 to 650 °C. RTA was performed only after the seed layer growth (there was no PDA after the main layer deposition). The physical thickness was measured with an ellipsometer (Gaertner Scientific Corporation, L115B) and calibrated via X-ray reflectivity (XRR; PANalytical, X'pert Pro). The layer densities (unit: μg/cm²) of Sr and Ti were measured via X-ray fluorescence spectroscopy (XRF; Thermo-Scientific, ARL Quant'X). Here, the layer density is the deposited amount in mass per unit area. The surface roughness was measured via atomic force microscopy (AFM; JEOL, JSPM 5300). The crystal structure of the deposited films was determined with glancing-angle incident X-ray diffraction (GAXRD; PANalytical, X'pert Pro, 2 ° incident angle) using Cu K α radiation and transmission electron microscopy (TEM; JEOL, 2100F). The chemical structures were analyzed via X-ray photoelectron spectroscopy (XPS; Kratos, AXIS SUPRA). 20nm RuO₂ and 50nm Pt were sequentially deposited on top of the STO films with a shadow mask having 300-μm-diameter hole patterns to form the top electrode (TE), and the Ru substrate layer was used as a BE for the capacitor structure. The area of the TE was measured with a microscope. The capacitance was measured with an HP4194A impedance analyzer at 10 kHz, and the leakage current density was measured with an HP4140 pA meter at room temperature. Electrical bias

was applied to the TE while the BE was grounded.

2.3. Results and Discussions

The growth behavior of the STO films with two-step growth was first investigated, and the results are shown in Figure 2-1. Figure 2-1(a) and (b) show the growth rates of the main layers deposited on the STO seed layers in terms of thickness (thickness growth rate, GR_t) and layer density (layer density (LD) growth rate, GR_{LD}), respectively. There were quite notable changes in both growth rate values depending on the substrate type, although the main layer ALD conditions were not varied at all for a given substrate type; only the RTA temperature of the seed layers, which were also grown under the given ALD conditions, was varied. On the Si substrate, the GR_t was kept at 0.09 nm/cy up to the 550 °C RTA temperature, and slightly decreased to 0.08 nm/cy at the higher temperatures. There was no change, however, in the GR_{LD} of both the Sr and Ti elements across the entire RTA temperature range, as shown in Figure 2-1(b) (black symbols). This indicates that the densities of the main layers grown on the seed layers annealed at temperatures higher than 575 °C were ~13% higher than those of the films grown on the seed layer annealed at temperatures lower than 550 °C. This could be related with the in-situ crystallization of the main layer STO on the well-crystallized seed layer. On Ru, however, the GR_t of the STO main layer consistently increased as the RTA temperature increased. Also, the GR_{LD} of Sr abruptly increased with the increasing RTA temperature > 575 °C, which

was also the case for the GR_{LD} of Ti, but to a lesser extent. Such abnormal overgrowth of Sr was often observed in the ALD of the STO and SrO films with the current Sr precursor in previous studies.^{12, 21, 22} When this highly reactive Cp-based Sr precursor was used with the aid of O_3 as an oxygen source at a high temperature (~ 370 °C) on a Ru substrate, the Ru substrate was (in-situ) oxidized by the pulsed O_3 , which was subsequently reduced when the Sr precursor was pulsed by the CVD-like reaction. This Ru oxidation-reduction-induced excessive deposition caused the deviation from the ideal ALD growth until the deposited oxide film became thick enough to suppress the oxygen ion diffusion through the grown film.^{21, 22} Therefore, the observed overgrowth of the main layer only on the Ru substrate shown in Figure 2-1(a) and (b) must be attributed to the loss of oxygen barrier effect of the seed layer after the RTA process at the higher temperatures.

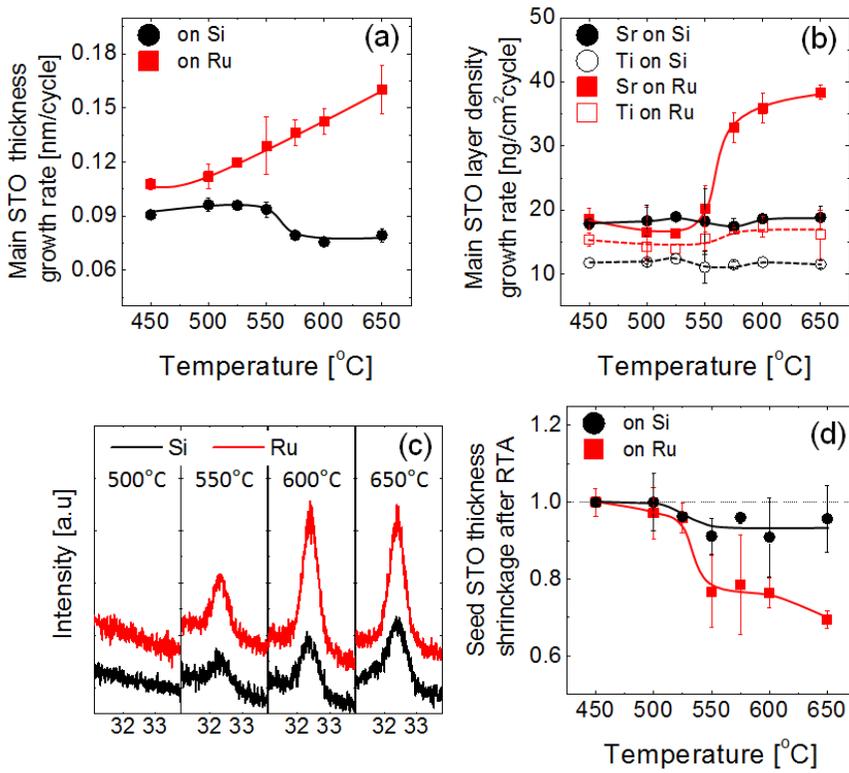


Figure 2-1 Variations in the growth rate of the STO main layers as a function of the RTA temperature of the STO seed layers on Ru and Si substrates in terms of (a) thickness and (b) layer density. (c) GAXRD spectra of the STO layer on the STO seed layer annealed at various temperatures on Ru and Si substrates. The total thickness was 18-22 nm. (d) Thickness shrinkage ratio of the STO seed layer after annealing, as a function of the annealing temperature.

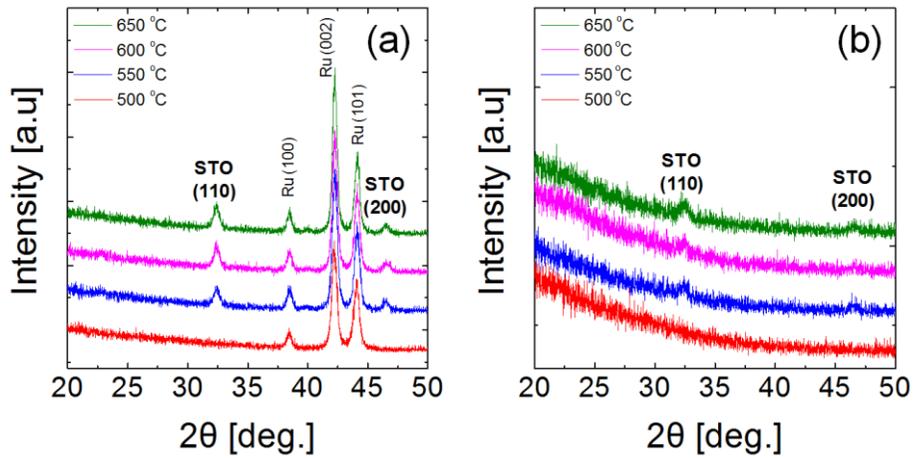


Figure 2-2 GAXRD spectra of the STO main layer on the STO seed layer annealed at various temperatures on (a) Ru and (b) Si substrates. The total thickness was 18-22 nm. The STO and Ru peaks are from perovskite (pm3m) and hcp (p63/mmc) structures, respectively

Figure 2-1(c) shows the GAXRD results of the main/annealed seed stacks with different RTA temperatures on the Si (black lines) and Ru (red lines) substrates. Consistent with the previous studies, the RTA at a sufficiently high temperature ($> 550\text{ }^{\circ}\text{C}$) after the seed layer growth induced the crystallization of the seed layer, which induced the in-situ crystallization of the main layer without any PDA.²³ The $< 500\text{ }^{\circ}\text{C}$ RTA temperature was too low to crystallize the as-deposited seed layer, and the entire main/seed stack remained in the amorphous phase. $550\text{ }^{\circ}\text{C}$ was the critical temperature, at which the film started to be crystallized, and as the RTA temperature increased, the intensity of the XRD peak at 32.4° (perovskite STO (110) plane) also increased, indicating improving crystallinity for both substrates. The GAXRD results of the wide range of 2θ were shown in Figure 2-2. As there were negligible differences in chemical state among the samples with RTA at 450 , 550 , and $650\text{ }^{\circ}\text{C}$ on the Ru substrate in the XPS analyses (Figure 2-3), it is believed that only the different-microstructure seed/main STO films affected the oxygen barrier effect shown in Figure 2-1(a) and (b). It is noteworthy that the enhanced growth rate of the main layer with RTA at over $575\text{ }^{\circ}\text{C}$ was retained up to a quite high thickness in this study (total STO thickness $< 22\text{ nm}$). As discussed in detail below, such enhanced film growth rate can be ascribed to the oxygen migration and CVD-like reaction. Therefore, the maintained high growth rate up to 22 nm means that such an adverse effect could be maintained up to this thickness, meaning there should be a macroscopic

oxygen diffusion path involved, such as micro- and nano-scale cracks or voids, in the growing films.

To check the relative densities of the seed STO films, the shrinkage of the physical thickness of the seed layer after the RTA was investigated. The shrinkage ratio (thickness after RTA/thickness before RTA measured by ellipsometry) was calculated as a function of the RTA temperature in Figure 2-1(d). The physical thickness of the STO film decreased only slightly on Si after the RTA at >550 °C, but it was very significant on Ru at the same temperature range. As the temperature for such drastic change is consistent with the crystallization behavior of the main STO film (Figure 2-1(c)), which is induced by the local epitaxial growth on the crystallized STO seed layer, the seed crystallization is accompanied by thickness shrinkage. This encompasses the possible formation of micro- and nano-scale cracks or voids in the seed films, which could be extended into the main STO layer. The drastic decrease in seed layer thickness shown in Figure 2-1(d) on Ru implied the lower density of the as-deposited amorphous seed layer compared to that on Si, probably due to the intense overgrowth.

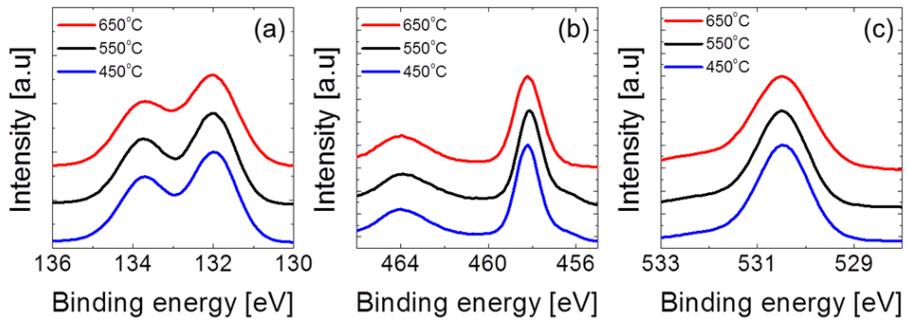


Figure 2-3 XPS spectra of the (a) Sr 3d, (b) Ti 2p, and (d) O 1s of the 18-22 nm STO films (main layer/seed layer) with different seed layer annealing temperatures

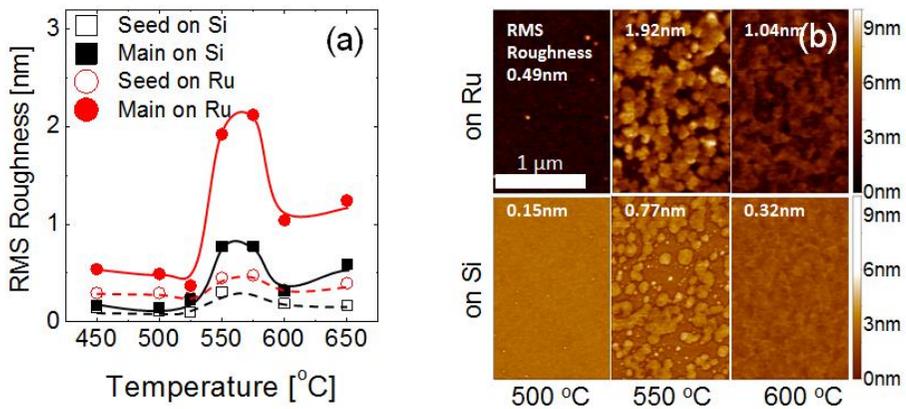


Figure 2-4 (a)RMS roughness variations and (b) AFM topographic images of the STO layers with different seed annealing temperatures.

Figure 2-4(a) shows the variations in the root-mean-squared (RMS) roughness values of the surfaces of the seed and main layers as a function of the RTA temperature for the Ru and Si substrates. On both substrates, the films were smoothest when the RTA temperature was ≤ 500 °C, due to their amorphous structure. When the seed layer was ex-situ-crystallized and the main layer was fully in-situ-crystallized with a ≥ 600 °C RTA temperature, the RMS roughness was slightly higher than in the amorphous film, but lower than in the cases with 550-575 °C RTA temperatures, where the RMS values were notably high. The roughness degradation of the films with RTA at the crystallization temperature was more apparent in the main layer than in the seed layer, and in the films grown on Ru than in those grown on Si. The RMS roughness of the main layer with 550 °C RTA on Ru was over 2 nm. The AFM topographic images of the amorphous, partial-crystalline, and full-crystalline phases on Ru and Si are shown in Figure 2-4(b) (grown on the seed layer annealed at 500 (left), 550 (middle), and 600 °C (right) on the Ru (top) and Si (bottom) substrates). It can be understood that the films with the highest RMS roughness values have two distinctive morphologies, which might be correlated with the partial crystallization.

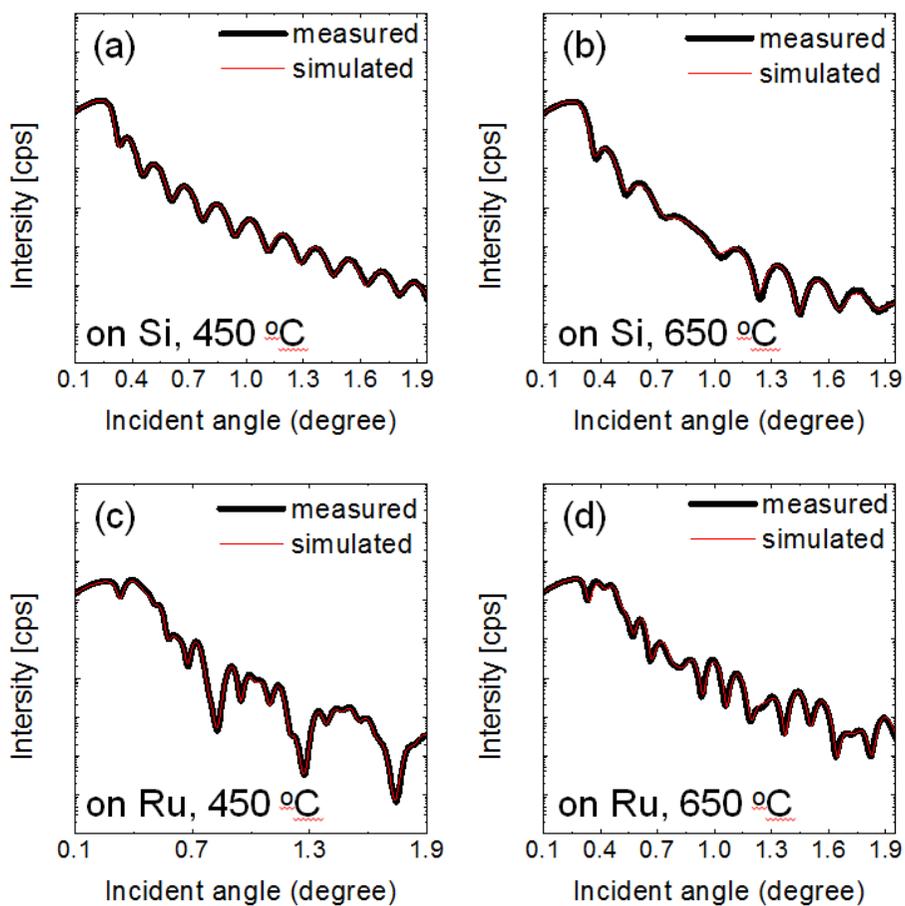


Figure 2-5 XRR spectra and simulated results of the in-situ-crystallized STO films (20-25 nm) on [(a), (b)] Si substrates and [(c), (d)] Ru substrates. The RTA temperatures were [(a), (c)] 450 °C and [(b), (d)] 650 °C.

Substrate	RTA temperature [°C]	STO density [g/cm ³]		Surface roughness [nm]	
		XRF and Ellipsometry	XRR	AFM (RMS)	XRR
Si	450	3.10	3.97	0.17	0.51
	650	3.57	4.51	0.59	0.88
Ru	450	3.40	4.16	0.54	0.87
	650	3.95	4.76	1.24	1.85

Table 2-1 Fitted values of the STO density and surface roughness with the comparison of the XRF, ellipsometry, and AFM results.

To further confirm the layer density, thickness, and surface roughness trends of the main/seed STO films, XRR analyses were performed, and the results are shown in Supporting Information. The XRR data of the stacked STO samples deposited on Si and Ru with 450 and 650 °C seed RTA temperatures are shown in Figure 2-5 with their simulated curves. The precisely fitted simulations showed that the STO films had higher densities and surface roughness when (in-situ) crystallized both on the Ru and Si substrates. Although there were discrepancies between the estimated values depending on the detailed estimation methods that were used, the trends along the processing conditions were consistent. The highest density of 4.76 g/cm³, which is close to the theoretical value, was obtained by the STO film grown on Ru with a 650 °C seed RTA temperature.²⁴ These results corroborated the trends obtained via XRF, ellipsometry, and AFM. The estimated parameters, density, and roughness are summarized in table 2-1. The film thickness fitted by XRR corresponded well to the thickness measured by ellipsometry. It should again be noted that the main STO layer was not subjected to PDA.

Figure 2-6(a) and (b) show the low- and high-magnification TEM images, respectively, of the main layer/seed layer/Ru sample with a 600 °C RTA temperature. A distinct horizontal line (marked by a blue arrow) was observed at the lower part of the STO layer in Figure 2-6(a). This is the boundary between the ~4.5-nm-thick seed layer (it was originally 5-nm-thick but shrunken during RTA) and the 18-nm-thick main layer, which was formed during the vacuum break after the RTA. It is noteworthy that even after 600 °C RTA, the seed layer was not fully crystallized, and a non-negligible portion of the amorphous region remained. Moreover, the crystal structure of the main layer exactly followed that of the underlying seed layer, as clearly shown in Figure 2-6(b). When the seed layer was in the amorphous state, the main layer grown on it was also amorphous, but when the seed layer was crystallized, the main layer on it was epitaxially crystallized, with an identical orientation. Therefore, the boundaries between the crystalline grains or between the crystalline and amorphous portions present in the vertical direction extended from the surface of the Ru BE to the surface of the STO film. The height of the grain was equivalent to the thickness of the STO layer, and the grain boundary of the in-plane direction was hardly observed. The different orientation at the upper right corner of Figure 2-6(b) indicates the polycrystalline structure of STO films due to the polycrystalline structure of seed layer after RTA. Another significant finding is that, as shown in Figure 2-6(a), the crystalline region was ~2 - 3 nm

thicker than the amorphous region, which is consistent with the previous report.²⁰ This means that the growth rate of main layer on the crystallized seed layer is higher than that on amorphous region or micro- or nano-void region of the seed layer generated by the densification annealing process. Therefore, a smaller thickness of the entire STO layer was achieved when the seed layer was not fully crystallized. The dotted line along the STO surface in Figure 2-6(a) is for eye guidance, to precisely compare the thickness difference. Figure 2-6(c) and (d) are the high-resolution TEM image and the enlarged image of the purple-squared region in Figure 2-6(c), respectively, of the STO film with 650 °C seed RTA. Although there was no difference in XRD peaks between the 600 and 650 °C RTA samples, as shown in Figure 2-1(c), a higher portion of the crystalline phase in the STO film was found when the RTA was performed at 650 °C, compared with the other case in TEM. Accordingly, more crystalline-crystalline grain boundaries were observed in this sample. Being different from the amorphous-crystalline boundary mostly seen in the 600 °C RTA sample, however, the crystalline-crystalline grain boundary appears to encompass the nanocracks along the direction perpendicular to the film surface (see the features marked by the red arrows inside the red squares in Figure 2-6(c)). These cracks, shown in the enlarged image in Figure 2-6(d), were believed to have originated from the small misalignment of the crystalline orientation to the adjacent grains.

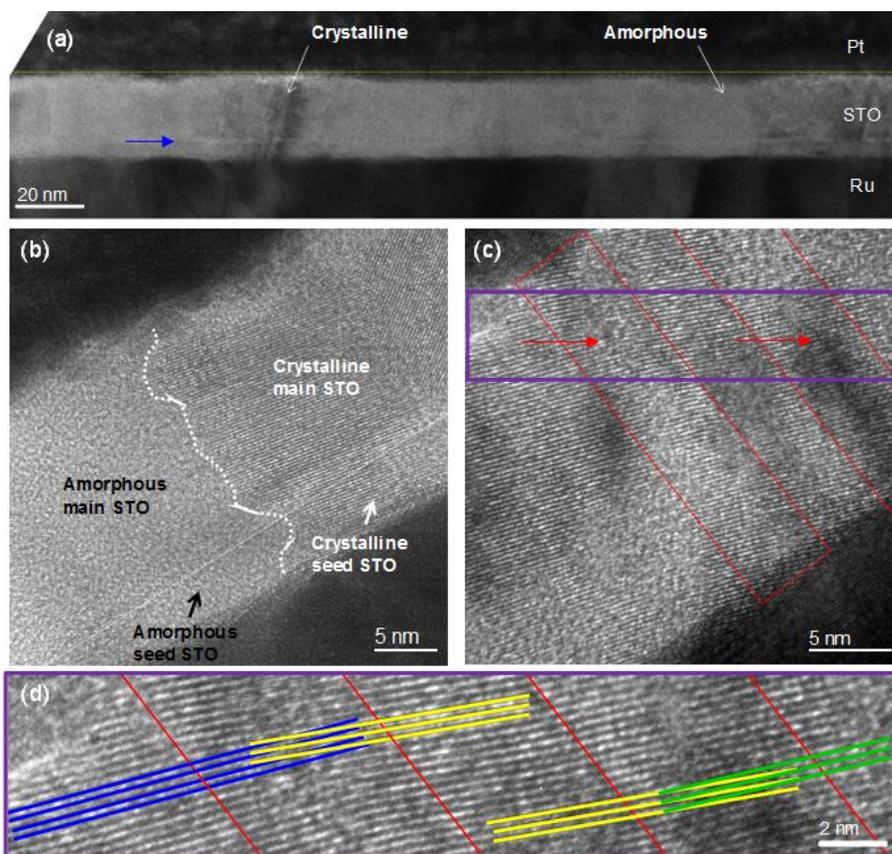


Figure 2-6 Cross-sectional TEM images of the Pt/STO main layer/STO seed layer/Ru. (a) Low- and (b) high-magnification images of the 600 °C RTA sample. (c) High-magnification image of the 650 °C RTA sample. (d) Enlarged image of the purple-squared region in (c)

Based on the growth behaviors and TEM images discussed up to this point, plausible mechanisms of the two-step growth of STO films on a Ru substrate with different RTA temperatures are suggested, as shown in Figure 2-7. When the RTA temperature was ≤ 500 °C, the seed layer mostly remained in the amorphous state, and the main layer was also grown with the same structure. When the RTA temperature was ~ 550 °C, the seed layer had mixed amorphous-crystalline phases. It can be easily understood from Figure 2-1(a) and (b) that the main layer of the crystalline structure had a higher growth rate than the main layer of the amorphous phase. Therefore, although the crystalline region of the seed layer was thinner than the amorphous region due to the densification shown in Figure 2-1(d), the crystalline region was thicker than the amorphous region after the main layer growth, and very high RMS roughness appeared. Unfortunately, the thickness difference between the crystalline and amorphous regions of the seed layer after RTA cannot be clearly distinguished in Figure 2-6(a) due to the small thickness of the seed layer. When the RTA temperature was ≥ 600 °C, a higher portion of the film was occupied by the crystalline grains. Although there remained some amorphous regions and there was still a height difference between the crystalline and amorphous regions, the portion of the thinner part is much smaller than that in the 550 °C RTA case, and the RMS roughness decreased. Due to the large difference in density of the seed layer before and after the RTA, in such cases, there can be a portion where the seed layer cannot

completely cover the Ru surface, as indicated by the schematic diagram of the seed layer after the RTA (left part of the lower figure in Figure 2-7). On this void region, the main layer directly grows on the Ru substrate, and it must be amorphous, as already studied previously.²⁰

The growth rate increase with the RTA at over 550 °C was likely to have been induced by the oxygen permeation paths generated by the columnar growth in the STO films, although the STO films were synthesized with two separate deposition steps. It is believed that the nanocracks at the grain boundary acted as the oxygen migration path during the ALD of the STO layer; that is, the active oxygen dissociated from the O₃ can reach down via such paths to the Ru surface, and can oxidize it during the O₃ pulse step. Subsequently, the Sr precursor can induce a CVD-like reaction through the reaction with the supplied-back oxygen atoms due to the reduction of the previously oxidized Ru, which are also migrated towards the growing film surface during the precursor supply step. Figure 2-1(b) suggests that such an adverse reaction is even more serious for the Sr precursor. This explains why the growth rate of the main layer in this study did not decrease, although the 22-nm-thick STO film completely covered the Ru substrate (i.e., nanocracks propagated towards the film surface).

On the other hand, the STO films deposited on Si showed a different growth behavior. As the Si substrate did not involve the reversible oxidation-reduction reactions during the O₃ pulse and precursor pulse steps, the

oxygen-related adverse CVD reaction did not occur. Therefore, the slightly higher and lower GR_t values at the low- and high-RTA-temperature regions (Figure 2-1(a)) can be attributed to the lower and higher densities of the amorphous and crystalline phases, respectively, of the STO main layer. The highest RMS roughness values of the main STO film among the films grown on a Si substrate when the RTA temperature was 550 °C can also be understood from the roughly equal portions of the amorphous (thicker) and crystalline (thinner) regions.

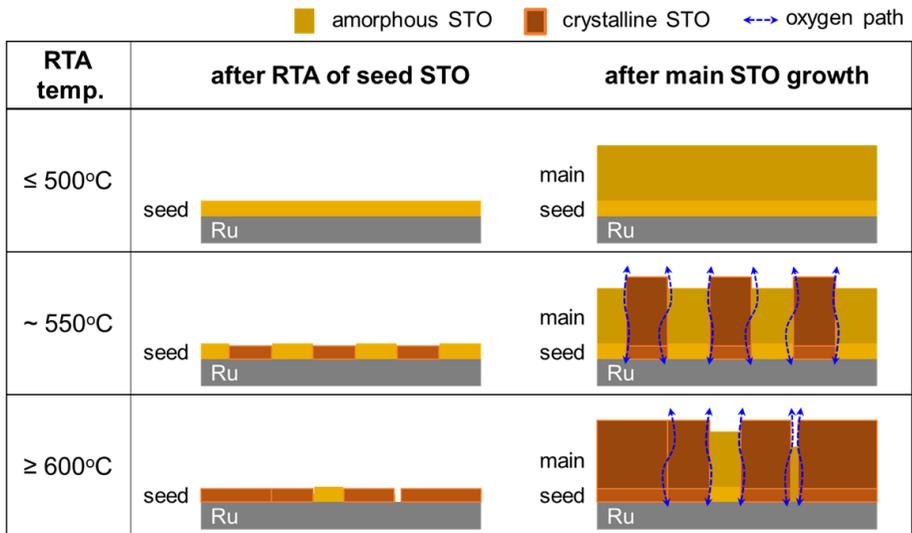


Figure 2-7 (a) Schematic diagram of the growth mechanism of the STO films according to the annealing temperature of the seed layer.

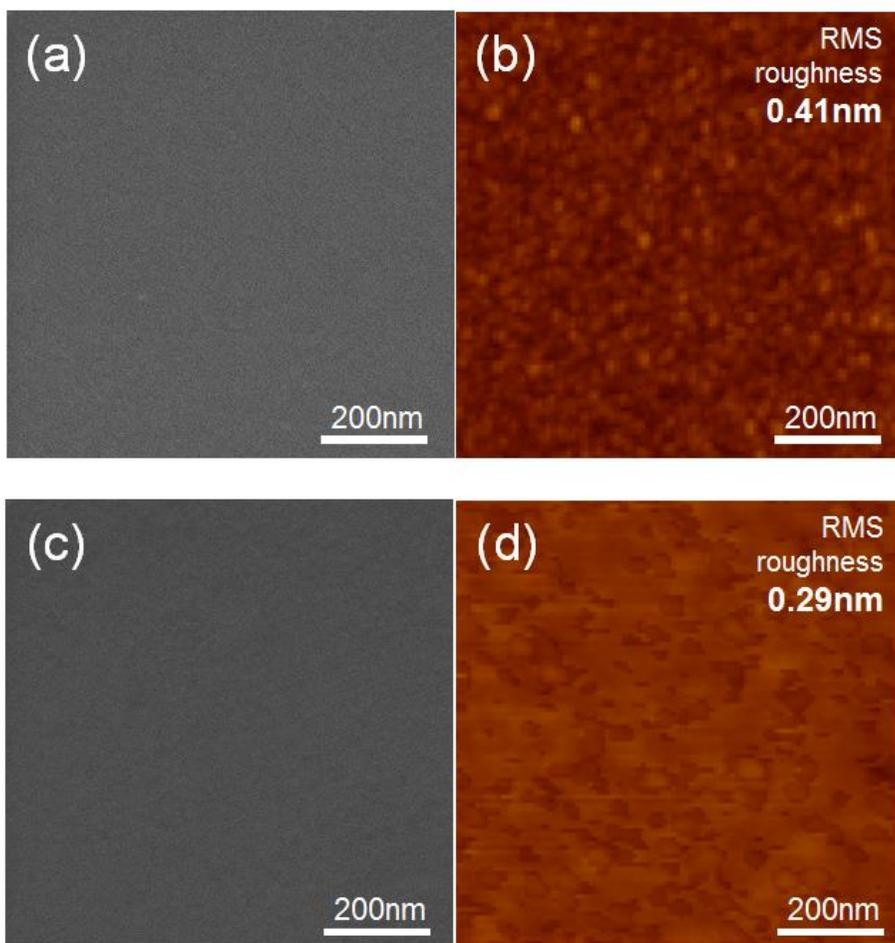


Figure 3-4 Surface morphologies of the as-deposited 4.5 nm STO seed layer grown at (a), (b) HT and (c), (d) LT. (a) and (c) are the SEM images, and (b) and (d) are the AFM images

GAXRD confirmed the crystallinity of the STO films, as shown in Figure 3-5(a). The GAXRD peak of STO was hardly observed in the annealed STO seed layer grown at LT due to the low thickness of 3 nm, while sharp peaks of the Ru (100), (002), and (101) planes from the substrate existed (blue line). This was also the case for the HT seed.²² When the STO main layer was deposited at HT on the annealed STO seed layer (total STO thickness: ~24 nm), however, distinct peaks of the STO (110), (111), and (200) planes appeared, although there was no annealing after the main-layer growth. This implies that the method of in-situ crystallization of STO films with the aid of a pre-crystallized STO seed layer also worked well with the newly developed LT process of the STO seed layer (black line), similar to the previous studies' reports on the HT seed layer process.²² The similar in-situ crystallization of the main STO on the crystallized HT seed was again confirmed in this work (red line). The peak intensity and full-width half-maximum of the STO peaks from the two samples were comparable (inset of Figure 3-5(a)). As clearly shown in the inset of Figure 3-5(a), however, the position of the STO (110) and (200) peaks from the LT seed sample shifted towards the higher 2 theta region compared with the peaks of the HT seed sample ($32.2^\circ \rightarrow 32.5^\circ$; $46.3^\circ \rightarrow 46.5^\circ$). In JCPDS #350734, the bulk STO films have the peaks of the (110) and (200) planes at 32.5° and 46.5° , respectively. This suggests that the main STO film with the HT seed had a

certain level of stress (whose precise nature can hardly be determined using the GAXRD pattern), which was well relieved when the LT seed was adopted. XRR analyses were conducted to understand the physical structure of the STO films further, as shown in Figure 3-5(b) and (c). The simulation of the spectra (red line) using the parameters related with the density, roughness, and thickness reproduced the experiment data (black line) precisely. The fitting revealed the following: HT seed and HT main - 4.40 g/cm³ density, 0.7 nm interface roughness, and 22 nm thickness; and LT seed and HT main - 4.26 g/cm³ density, 0.8 nm interface roughness, and 22 nm thickness. Therefore, the density decrease of the film through the adoption of the LT seed layer was not very high, and the interface roughness was similar. The roughness of the main layer surface, however, was obviously improved from 3.7 nm for the HT seed to 1.8 nm for the LT seed, due to the decreased voids and cracks of the STO film. This explains the growth rate difference of the main layer shown in the inset of Figure 3-3(a).

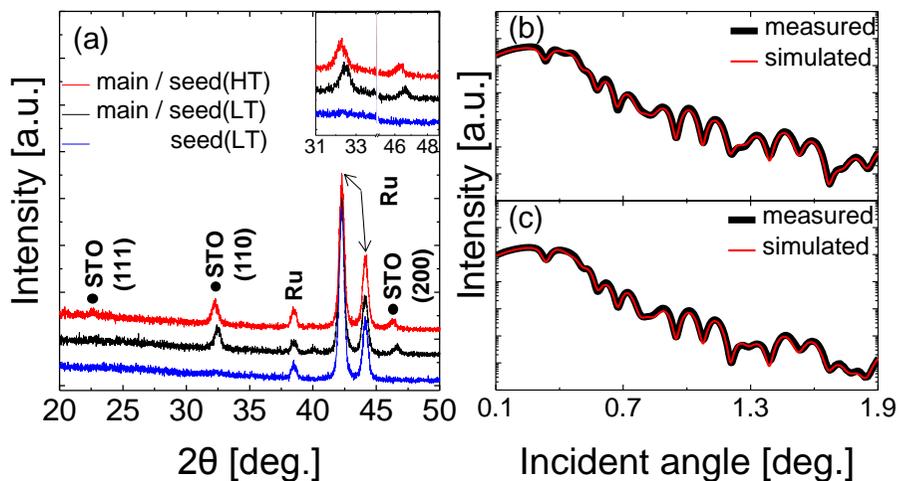


Figure 3-5 (a) GAXRD patterns of the STO films with different process temperature combinations. X-ray reflectivity spectra and simulated results of the in-situ-crystallized 22-nm-thick STO films grown on (b) an HT seed layer and (c) an LT seed layer, respectively. The inset figure in (a) shows the enlarged peaks of the perovskite STO.

The electrical properties of RuO₂/STO/Ru-structured capacitors were investigated and are shown in Figure 3-6, where STO films were grown through the two-step processes (main layer growth at HT after crystallization of the seed layer grown at LT and HT). Figure 3-6(a) shows the variation of t_{ox} as a function of the physical oxide thickness (t_{phy}) of the STO films (summation of the 3-nm-thick seed layer and the main layer). The t_{ox} of a certain sample can be calculated from the estimated capacitance density (C/A , where A is the electrode area) through $t_{\text{ox}}=3.9 \times \varepsilon_0/(C/A)$, where ε_0 is the vacuum permittivity. For the comparison, the data with the HT seed layer process from the previous report²² were included in the same graph. In Figure 3-6(a), t_{ox} could be estimated using the equation below.

$$t_{\text{ox}} = (3.9/k_{\text{bulk (main)}}) \times t_{\text{phy (main)}} + (3.9/k_{\text{seed}}) \times t_{\text{phy (seed)}} + t_{\text{ox}}^{\text{i (intrinsic)}} \quad (1)$$

Here, $k_{\text{bulk(main)}}$, $t_{\text{phy(main)}}$, k_{seed} , $t_{\text{phy(seed)}}$, and $t_{\text{ox}}^{\text{i (intrinsic)}}$ are the bulk dielectric constant of the main layer, the physical oxide thickness of the main layer, the dielectric constant of the seed layer, the physical oxide thickness of the seed layer, and the t_{ox} values by intrinsic interfacial property, such as dead layer and low-k interfacial layer. All the parameters, except for $t_{\text{phy(main)}}$, were considered constant; $t_{\text{phy(main)}}$ was the experimental variable. In the HT seed

case (main(HT)/seed(HT)), k_{seed} was close to $k_{\text{bulk(main)}}$ (shown in Figure 3-8(a)), and equation (1) can be simplified into equation (2) below.

$$t_{\text{ox}} = (3.9/k_{\text{bulk}}) \times t_{\text{phy}} + t_{\text{ox}}^{\text{i (intrinsic)}} \quad (2)$$

Here, k_{bulk} is the bulk dielectric constant of the STO film, which is similar to $k_{\text{bulk(main)}}$ (also, to k_{seed}). The best-linear-fitted line (solid red line) in Figure 3-6(a) for the HT seed case produced a k_{bulk} of 101 from the inverse slope, and a 0.02 nm $t_{\text{ox}}^{\text{i (intrinsic)}}$ was obtained at the Y-axis intercept. In the LT seed case (main (HT) on crystalline seed (LT)), however, k_{seed} could be different from $k_{\text{bulk (main)}}$ (k_{seed} must be much smaller than $k_{\text{bulk (main)}}$ by Figure 3-8(d)), and equation (1) was used to interpret the LT seed data in Figure 3-6(a). As the interface roughness between STO and Ru was identical (Figure 3-5(b) and (c)), and as the main layer surface roughness was even decreased in the LT seed layer case, it is believed that the capacitance loss due to the intrinsic interface property of the LT seed case is comparable to that of the HT seed case. Therefore, 0.02 nm was also adopted for $t_{\text{ox}}^{\text{i (intrinsic)}}$ for the LT seed case. Now, the seed and the main layer regions could be separately considered in the LT seed case shown in Figure 3-6(a). When t_{phy} is over 3 nm (main-layer region), the inverse slope of the best-linear-fitted line (solid black line) from the measured data gave a 167 $k_{\text{bulk(main)}}$. It is notable that the main layer showed such a large difference in k_{bulk} depending on the seed layer type,

although the cases were grown under identical conditions. In the previous study, it was identified that the nanovoid regions of the STO seed layer induced the amorphous-phase regions of the STO main layer due to the absence of a crystallized seed matrix, which is essential for the in-situ crystallization of the main layer.³⁴ The density of micro/nano-defects in the seed layer is directly related to the portion of the low-permittivity amorphous phase in the main layer, which must have contacted the Ru substrate film without the intervening crystallized seed layer.³⁴ Therefore, $k_{\text{bulk(main)}}$ was believed to have been enhanced by the LT seed process, due to the improved film morphology of the seed layer (the SEM images in Figure 3-3) associated with the decrease in the initial overgrowth and the longer deposition time. The lower stress in the STO film with the LT seed compared to that with the HT seed, as shown by the GAXRD results in Figure 3-5(a), might have also contributed to the improved dielectric property. In the t_{phy} range of lower than 3 nm (seed layer region), another blue-dotted linear line was plotted from the end of the main-layer data at a 3 nm t_{phy} to a 0.02 nm Y-intercept ($t_{\text{ox}}^{\text{i (intrinsic)}}$). From the inverse slope of this plot, $k_{\text{bulk(seed)}}$ was estimated to be 23, which is much lower than the expected value in crystallized STO thin films. The possible reasons for such low- k value of the thin seed layer will be discussed later (Figure 3-8).

Figure 3-6(b) shows a summary of the electrical properties of capacitors with an HT main layer on HT²² or that underwent the LT seed layer process.

Since the bottom electrode was grounded and the bias was applied to the top electrode, the leakage current is from the electrons injected from the Ru bottom electrode into the STO layer. As the thickness of the dielectric layer decreased, the t_{ox} also decreased, but the leakage current density increased in both the HT and LT seed cases. For the LT seed layer case, 0.70 nm t_{ox} was achieved with a low leakage current density (9.2×10^{-8} A/cm² @ 0.8 V), which is acceptable in DRAM capacitor application at a 10-nm- t_{phy} sample. The t_{phy} value that satisfies the low leakage current level ($<1 \times 10^{-7}$ A/cm² @ 0.8 V) was comparable to the HT seed layer case (t_{phy} : ~10 nm). The symmetric leakage current curves with different polarity of the applied voltage of the 10 nm STO samples with both LT and HT seed cases were shown in Figure 3-7. Due to the large t_{ox}^i of the LT seed layer capacitors, however, caused by the small $k_{bulk(seed)}$, the minimum t_{ox} with an acceptable leakage current was larger than that of the capacitors with an HT seed layer by ~0.39 nm, which is a critical demerit of the LT seed process. The obtained minimum t_{ox} value is still higher than the binary TiO₂-based capacitor (t_{ox} ~0.41 nm).³⁵ Since the permittivity of single crystal STO is reported about two times higher than that of TiO₂, the optimized STO ALD process is supposed to show lower t_{ox} value than TiO₂ process.³⁶⁻³⁷ In fact, the SrRuO₃/STO/SrRuO₃ capacitor fabricated by sputtering with no vacuum break between the different film growths a minimum t_{ox} of 0.35 nm with a leakage current of 1×10^{-7} A/cm² at 1.0 V has been reported.³⁸ However, the

ALD STO-based capacitor in this work showed a much inferior performance to the sputtered STO capacitor or even TiO_2 capacitor, meaning that additional research is necessary to further improve it by solving the high t_{ox} problem.³⁸

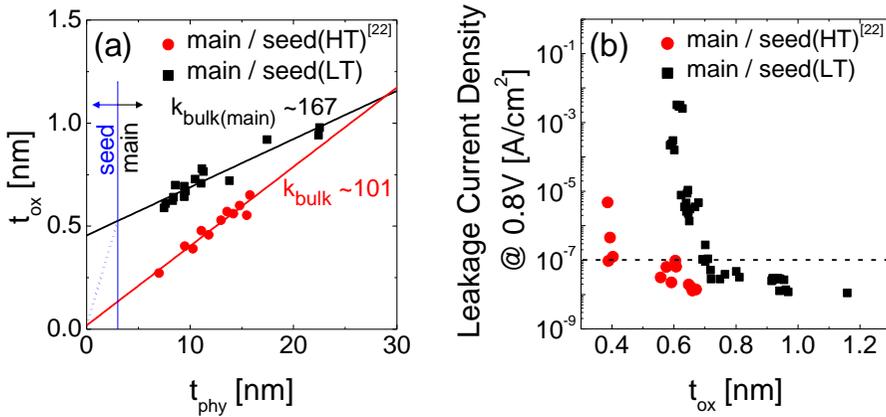


Figure 3-6 (a) Variations in the equivalent oxide thickness (t_{ox}) as a function of the physical oxide thickness (t_{phy}) of the STO films (seed and main). The main layer was crystallized in situ on the LT and HT²² seed layers. (b) Leakage current density vs. t_{ox} for the STO films with LT and HT²² seed layers. Electrons were injected from the bottom Ru electrode.

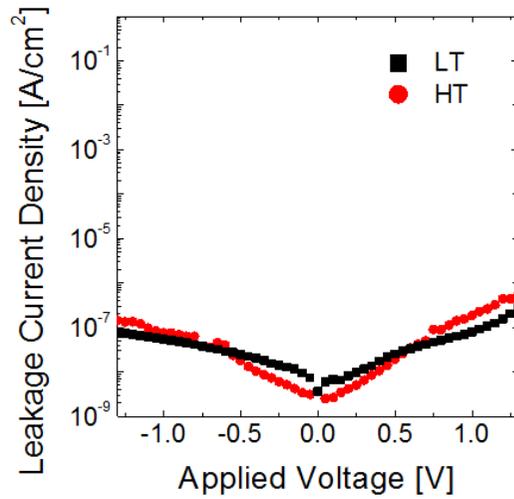


Figure 3-7 The variations of the leakage current density of 10 nm STO films with LT (230 °C) and HT (370 °C) seed processes as a function of applied voltage. The bias was applied to the top electrode while the bottom electrode was grounded.

Figure 3-8(a) and (b) show the ToF-SIMS depth profiles of the STO films on a Ru substrate deposited at HT and LT conditions, respectively. It should be noted that these films are single layers grown under the respective conditions. The STO films were annealed through the RTA process after the growth of the films for 80 and 165 cycles for HT and LT, respectively, to obtain comparable thicknesses (13-14 nm). The Sr and Ti ions showed higher and lower intensities, respectively, at the interface between the STO film and the Ru substrate than the bulk region, as expected from the initial overgrowth of Sr shown in Figure 3-3(b). In the LT case, however, the depth profiles of Sr and Ti were much more uniform compared with the HT case, which is also consistent with the data shown in Figure 3-3(b). The oxygen signals showed uniform profiles in both cases. Between the two depth profiles, the one with the most significant difference was the C ion profile. To better elucidate the difference, only the C profiles of the HT and LT samples are shown in Figure 3-8(c), in a linear Y-axis scale. Due to the absence of appropriate standards, quantitative composition analysis of C could not be done, and only qualitative comparison was made. It was shown that the C signals were first piled up within the initial growing region (indicated as "A") for both cases, which was related by the CVD-like reaction between the Sr precursor and the oxidized Ru substrate. This

interfacial C accumulation was less severe for the HT process than for the LT process, suggesting that the CVD-like reaction at HT was more efficient in removing residual carbon. This is in general agreement with the metal-organic CVD of oxide films, where the removal of the carbon-related residue is mainly proceeded with through reaction with oxygen (leading to volatile CO or CO₂ formation), which must be more active at a higher temperature.¹⁹ This phenomenon appears to have a critical influence on the electrical properties of the film. The ToF-SIMS depth profiles of TiO₂ films deposited at HT and LT was shown in Figure 3-9. In contrast to STO film case, the carbon concentration at the interface of TiO₂ and Ru was comparable between HT and LT samples, while the bulk region of HT TiO₂ film had certainly lower carbon contamination than LT case. Also, the signal intensity of carbon in the TiO₂ film was about one order of magnitude lower than that in STO film, which indicates that the large difference in carbon concentration at 'A' region in Figure 3-8(c) was mainly related to the SrO sublayer growth mechanism.

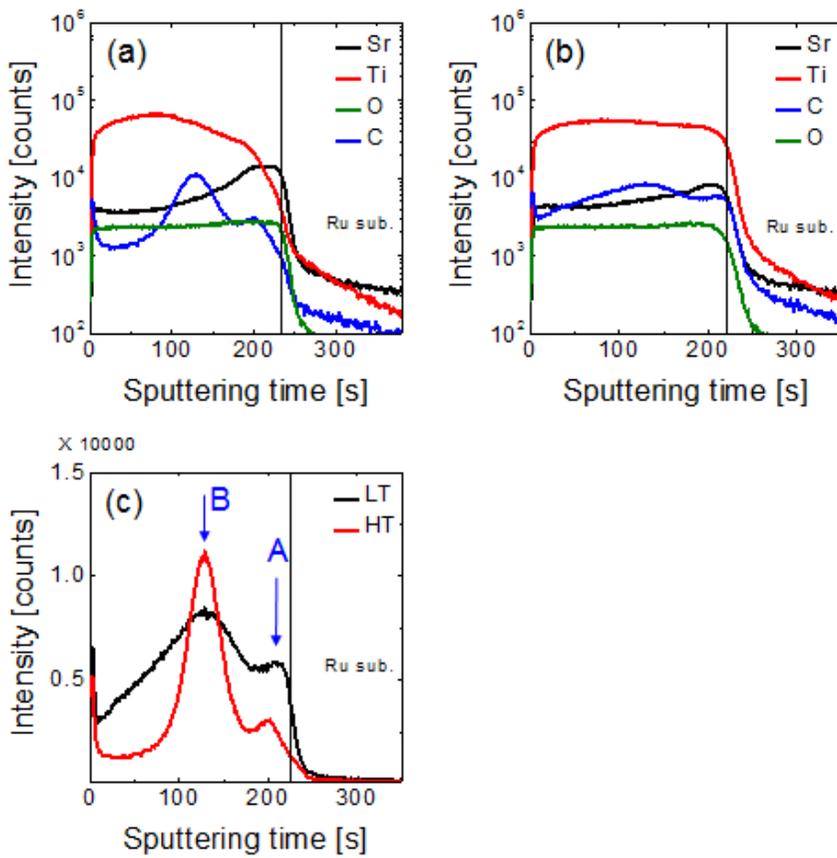


Figure 3-8 ToF-SIMS depth profiles of the annealed (a) 14-nm-thick STO grown at 370 °C (HT) and the (b) 13-nm-thick STO grown at 230 °C (LT) deposited on a Ru substrate. (c) Comparison of the ToF-SIMS depth profiles of the C element in (a) and (b) in a linear Y-axis scale

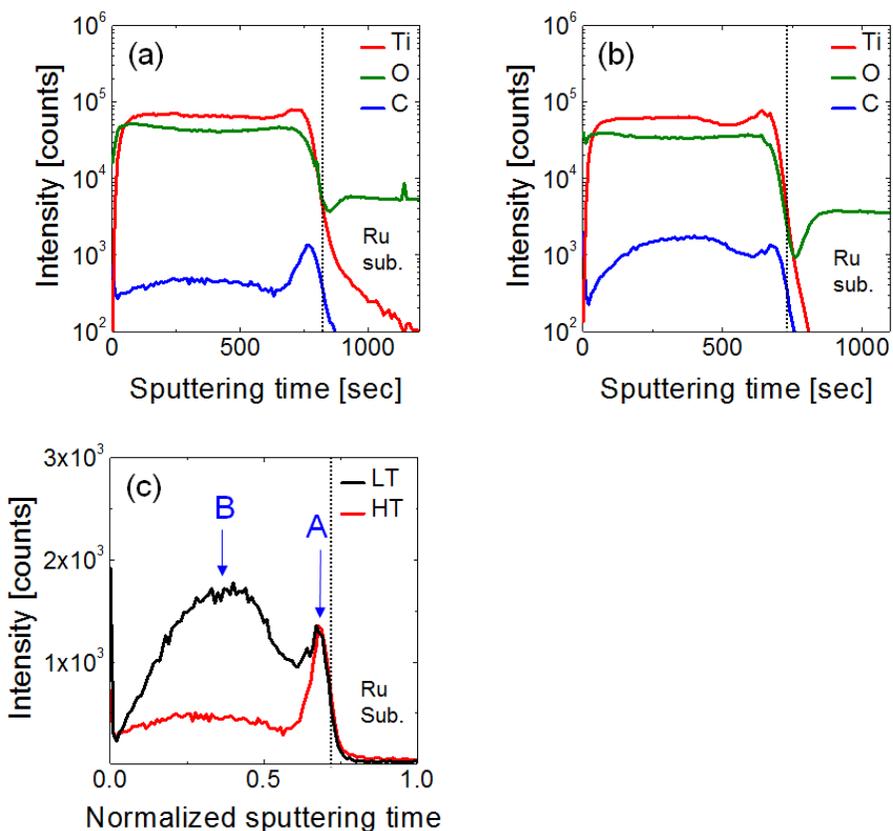


Figure 3-9 The ToF-SIMS depth profiles of (a) the 13-nm-thick TiO₂ grown at 370 °C (HT) and (b) the 12-nm-thick TiO₂ grown at 230 °C (LT) on Ru substrates. (c) Comparison of the ToF-SIMS depth profiles of the C element in (a) and (b) in a linear Y-axis scale. The X-axis was normalized to match the thickness of two samples from the small thickness difference. HT TiO₂ were deposited for 200 cycles (50 minutes), and LT TiO₂ were deposited for 400 cycles (166 minutes) to match the thicknesses of the two films.

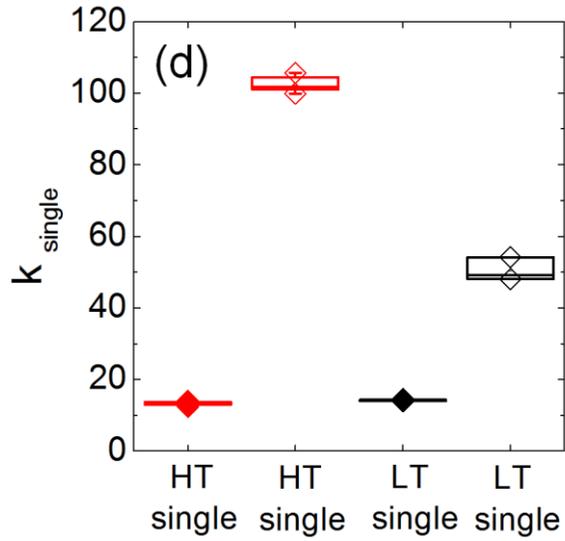


Figure 3-10 (a) Dielectric constant of the single capacitor (k_{single}) of the STO films deposited at HT and LT, before and after crystallization annealing. Every crystallization sample was annealed after the whole film growth.

Interestingly, also in both cases, there were peaks of C ions in the middle of the STO films, where the initial excess growth of Sr disappeared (indicated as “B”), which can be identified by the crossing of the black and blue lines in Figure 3-8(a) and (b). The accumulation of C intensity at position B was much higher in the HT case, whose precise origin is not yet understood. It should be noted, however, that this C peak region occurs near the middle of 13- to 14-nm-thick films, suggesting that these regions were not involved in the actual two-step film growth and electrical performance evaluations. Nonetheless, the overall higher C intensity from the LT film even over the “B” position (sputtering time: less than 100 seconds) suggested that the lower deposition temperature did not provide enough thermal energy to the system to activate the complete ligand exchange reaction. C impurity remained in the STO films even when genuine ALD was performed at LT (the film region far from the interface).

Considering that the STO seed layer, which was used for the capacitor fabrication shown in Figure 3-6, was only ~3 nm thick, the seed layer of LT must have had twofold more carbon impurity than that of HT, which may have degraded the dielectric property. Such an adverse effect was experimentally proven using thicker single layers, as shown in Figure 3-8(a). This figure shows the dielectric constants of the various STO films estimated from every single layer with a Pt top electrode, using the equation below.

$$C = k_{\text{single}} \times \epsilon_0 \times A/t_{\text{phy}} \quad (3)$$

Here, k_{single} is the dielectric constant from a single-layer capacitor. The t_{phy} values of the as-deposited HT STO, crystallized HT STO, as-deposited LT STO, and crystallized LT STO were 14, 14, 15, and 13 nm, respectively. They were deposited with a 2:1 TiO₂:SrO subcycle ratio for both the HT and LT samples to obtain a ~50% overall Sr composition ratio. It can be noted that the HT film did not show any notable change in film thickness even after RTA, while the LT film showed a certain shrinkage, which could have been induced by the low density of the as-deposited STO film grown at LT. The high C concentration in the LT film may have induced the low density. The as-deposited STO films (both HT and LT) had k_{single} values lower than 20 due to their amorphous structure. This is consistent with the previous result that the STO film directly grown on lattice-unmatched Ru has an amorphous structure even if it was grown at a 370 °C temperature.^{22,33} After RTA at 650 °C, however, both the HT and LT STO films showed crystalline peaks with a perovskite structure in GAXRD (data not shown), and k_{single} increased to 106 and 49 in the HT and LT films, respectively. It is worth noting that the HT STO film showed a much higher k_{single} value despite its higher Sr composition variation over the entire film thickness compared with the LT STO film. Therefore, the adverse effect of carbon

impurity on the dielectric property was shown to be more predominant than the cation composition effect of STO films. This result supported the lower dielectric performance of the LT seed layer shown in Figure 3-6(a). In the HT seed case, the 106 k_{single} in the annealed HT film is close to the k_{bulk} of 101 shown in Figure 3-6(a). The calculated k_{seed} of 23 in the LT seed case was only ~47% of the 13 nm k_{single} value of the LT STO single film. This indicates that crystallization was more difficult in the thinner layer. This can also be explained by the fact that the carbon concentration difference was higher in the 3-nm-thick films than in the thicker films, as can be gleaned from the ToF-SIMS results in Figure 3-7(c). Therefore, the high carbon contamination of the LT seed layer and its resulting lower dielectric constant induced the significant degradation of the capacitor performance, as shown in Figure 3-10(a). Despite the low dielectric constant of the seed layer due to the high carbon contamination and low crystallinity, the LT seed layer successfully aided the in-situ crystallization of the STO main layer in obtaining a remarkable $k_{\text{bulk(main)}}$.

3.4. Summary

In summary, the atomic layer deposition process of SrTiO₃ (STO) films at 230 °C were studied with Sr(ⁱPr₃Cp)₂ and Ti(CpMe₅)(OMe)₃ (Pr, Cp, and Me are propyl, cyclopentadienyl, and methyl groups, respectively) on Ru substrates. The growth behavior and property of STO films grown at 230 °C were compared with those deposited at 370 °C. With the limited over-reaction of the Sr precursor during the initial growth stage at a lower temperature, the cation composition was more controllable, and the surface morphology after crystallization annealing at 650 °C had more uniform grains with fewer defects. Here, the excess reaction of the Sr precursor means the chemical-vapor-deposition-like growth of the SrO component mediated through the thermal decomposition of the adsorbed Sr precursor molecules via the reaction with the oxygen supplied from the partly oxidized Ru substrate. The second STO was grown at 370 °C (main layer) on the annealed first STO layer (crystallized seed layer) to lead to the in-situ crystallization of the main layer. Due to the improved microstructure of STO films induced by the seed layer deposited at 230 °C, the bulk dielectric constant of 167 was obtained for the main layer, which was higher than the value of 101 where the seed layer was deposited at 370 °C, even though the crystallization annealing condition of the seed layer and the deposition condition of the main layer were consistent. The seed layer grown at 230 °C, however, had a lower dielectric constant of only ~49, whereas the high-

temperature seed layer had a dielectric constant of ~ 106 . Therefore, the low-temperature seed layer posed a severe limitation in acquiring an advanced capacitor property with the involvement of a low-dielectric interfacial layer.

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4. Leakage Current Control of SrTiO₃ Thin Films through Al Doping via Atomic Layer Deposition

4.1. Introduction

The atomic layer deposition (ALD) of a SrTiO₃ (STO) film has been intensely studied for the dielectric materials of the next-generation dynamic random access memory (DRAM) capacitor application.¹⁻⁴ When the (10-20 nm) STO film was well crystallized to the desired perovskite structure through (ex-situ) post-deposition rapid thermal annealing (RTA) or (in-situ) during the ALD process, the dielectric constant (k) became as high as ~150, much higher than those of the currently used ZrO₂-based dielectric materials (k ~30-40).^{2,4-7} The ex-situ crystallization of STO films, however, induced the formation of nanocracks or nanovoids due to the film shrinkage during RTA, which made it very difficult to obtain a useful insulating property.⁸⁻⁹ The two-step growth method (sequential growth of the seed and main layers with interposed crystallization annealing between them) enabled the in-situ crystallization of the main layer with the aid of a crystallized seed layer.¹⁰⁻¹⁴ Under the optimized conditions for the seed layer growth, the RTA of the seed layer, and the subsequent main layer growth, both a high k value and a

low leakage current could be achieved (the acquired minimum equivalent oxide thickness (t_{ox}) was 0.39 nm with a sufficiently low leakage current ($<10^{-7}$ A/cm² at 0.8 V)).¹³ Nonetheless, the most critical issue remaining is the physical film thickness (t_{phy}) at which such high performance could be achieved; it was ~10-12 nm, which could hardly be accommodated into the narrow gap between the storage nodes of the next-generation DRAM (<15 nm). Therefore, the scaling of t_{phy} is another impending task in this field. It can be readily anticipated that the further scaling of t_{phy} will abruptly increase the leakage current density (J), which was indeed the case.^{2, 10, 11, 15} STO is a relatively narrow band gap ($E_{\text{g}} \sim 3.0\text{-}3.2$ eV) oxide with a high probability of oxygen vacancy (V_{O}) generation, which plays the role of an n-type donor.¹⁶⁻¹⁹ Therefore, the thinner films are prone to have a high leakage current especially due to the pinning of the Fermi level at a position close to the conduction band edge (E_{c}) within the E_{g} at the interface with the electrode. Another high- k dielectric thin film, rutile-structure TiO_2 , also suffers from a similar problem.²⁰⁻²¹ It was found, however, that Al doping, which acts as the acceptor in TiO_2 , could decrease the J level by almost six orders of magnitude at a t_{ox} of ~0.5 nm, by moving the Fermi level pinning position to near the middle point of the E_{g} .²¹ A further study reported that the careful tuning of the Al doping location via ALD further enhanced the J - t_{ox} performance, and that a minimum t_{ox} of 0.38 nm could be achieved with a t_{phy} of 8.7 nm.²² Nonetheless, the Al-doped rutile TiO_2 showed a k value of

~60-70, which is much lower than that of the undoped rutile TiO_2 ($k \sim 100-150$)²³⁻²⁵ and also that of STO ($k \sim 150-160$).^{2, 26-27} Therefore, adopting a similar Al doping approach in STO to suppress the J at a smaller t_{phy} must be a feasible method, as shown in this work.

Compared with Al doping in TiO_2 , however, which could be directly in-situ-crystallized to the desired rutile phase on a Ru and RuO_2 substrate (which is also the bottom electrode, BE), the in-situ STO crystallization requires a complicated two-step film growth process. Therefore, applying an Al doping cycle in STO film growth via ALD must be much more complicated than that in the case of TiO_2 film growth. For example, when an Al doping cycle was performed after the RTA of the seed layer (i.e., immediately before the STO main layer deposition), the in-situ crystallization of the main layer was significantly interfered with, and a k value of only ~53 was achieved (preliminary study). This means that Al doping must be performed either before the STO seed layer growth (because the Al-doped STO seed layer would be crystallized by the subsequent RTA) or after the main layer growth, which may minimally impact the crystallization of the main layer. Another crucial parameter is the doping concentration. In the case of the Al-doped TiO_2 , it was found from the preliminary study that only one Al_2O_3 ALD cycle had sufficiently profound effects.²² Therefore, in this work, one Al_2O_3 ALD cycle was performed before the STO seed layer growth (b-Al-STO) or after the STO main film growth (t-Al-STO), and the electrical properties

were carefully examined. After all, the RuO₂/8.6-nm-thick t-Al-STO/Ru planar capacitor showed an improved t_{ox} (t_{phy}) value of 0.63 (8.6) nm with an acceptable J of 8.0×10^{-8} A/cm² at a 0.8 V operation voltage. A similar J level was achieved from the 10.3-nm-thick undoped STO film, which resulted in a t_{ox} value of 0.71 nm, although its bulk k value was larger (149 (undoped STO) vs. 120 (t-Al-STO)).

4.2. Experiment Methods

ALD STO thin films were deposited with a 4-inch-wafer traveling-wave-type reactor (CN-1 Co., plus-100) with $\text{Ti}(\text{CpMe}_5)(\text{OMe})_3$ and $\text{Sr}(\text{}^i\text{Pr}_3\text{Cp})_2$ (Cp: cyclopentadienyl group; Me: methyl group; ${}^i\text{Pr}$: isopropyl group; both were supplied from Air Liquide). $250 \text{ g/m}^3 \text{ O}_3$ and $5 \text{ }^\circ\text{C}$ water were used as oxygen sources for TiO_2 and SrO thin films, respectively. Al_2O_3 thin films were deposited with AlMe_3 and water, as the Al precursor and oxygen source, respectively. The canisters of Sr and Ti precursors were heated to 80 and 70 $^\circ\text{C}$, respectively. Al precursor was cooled to 5 $^\circ\text{C}$, and an orifice gasket was used to control its injection amount. 200 sccm Ar gas was delivered to the chamber as a carrier of the Sr and Ti precursors. The working pressure was 0.7 ± 0.1 Torr.

For the STO seed layer deposition at 230 $^\circ\text{C}$ on a Ru substrate (sputter-deposited 30 nm Ru/8 nm $\text{Ta}_2\text{O}_5/\text{Si}$ substrate), two TiO_2 and one SrO ALD cycles were combined for stoichiometric cation composition. One TiO_2 ALD cycle consisted of Ti source feeding, Ar purge, O_3 feeding, and Ar purge for 3, 10, 2, and 10 sec, respectively, and one SrO ALD cycle consisted of Sr source feeding, Ar purge, H_2O feeding, and Ar purge for 6, 5, 6, and 5 sec, respectively. The STO seed layer could have been grown at a higher temperature (370 $^\circ\text{C}$), as with the subsequent STO main layer growth.^{10, 13} It was found, however, that the lower-temperature seed layer produced more uniform and homogeneously fine STO seed grains, which may be more

beneficial in controlling the Al doping profile, even after the RTA of the seed layer. Therefore, in this work, the low-temperature seed process was adopted, although it resulted in a slightly lower k value compared with the high-temperature seed ALD condition.¹²

RTA was processed in an N₂ atmosphere (purity: >99.999%) for 2 min at 650 °C for the crystallization of the seed layer. An STO main layer was deposited on a 3.5-nm-thick crystallized seed layer with the combined two TiO₂ ALD cycles (with 3, 5, 2, and 5 sec time steps) and one SrO ALD cycle (with 3, 5, 2, and 5 sec time steps) at 370 °C for in-situ crystallization. There was no post-deposition annealing after the main layer growth. The detailed deposition condition of STO was reported elsewhere.¹² Al₂O₃ ALD consisted of Al source feeding, Ar purge, H₂O feeding, and Ar purge for 0.5, 5, 2, and 5 sec, respectively. Only one Al₂O₃ ALD cycle was adopted for Al doping. The temperature was 370 °C when Al was doped at the top of the STO layer (t-Al-STO), whereas it was 230 °C when doped at the bottom of the STO layer (b-Al-STO). There was no vacuum break between one ALD cycle of the Al₂O₃ at the bottom of the STO and the STO seed layer growth (b-Al-STO), or between the STO main layer growth and the final one ALD cycle of the Al₂O₃ (t-Al-STO).

The crystal structure was verified with glancing-angle X-ray diffraction (GAXRD, PANalytical, X'pert Pro) with a 2 ° incident angle, using Cu K α radiation. The layer density of Sr and Ti were measured with an X-ray

fluorescence spectrometer (XRF, ThermoScientific, ARL Quant'X). The physical thicknesses of the thin films were measured with an ellipsometer (Gaertner Scientific Corporation, L115B). The surface topographies were analyzed with atomic force microscopy (AFM, JEOL, JSPM-5200) and field emission scanning microscopy (SEM, Hitachi, S-4800). The depth profiles were investigated with time-of-flight secondary ion mass spectroscopy (ToF-SIMS, ION-TOF, SIMS-5), with detection of negative ions sputtered by a Cs⁺ ion gun. The chemical states and valence band offset were investigated with an X-ray photoelectron spectrometer (XPS, Kratos, AXIS SUPRA). The XPS peak positions were calibrated by the C 1s of C-C bonding (284.5 eV)^{10,10}. For the measurement of the electrical properties, top electrodes (TEs) were sputter-deposited for 20nm RuO₂ and 50nm Pt, sequentially using a hole mask with a 300 μm diameter. The exact area of the TE was measured with an optical microscope after deposition, and was used as the capacitor area. The leakage current density-voltage (*J-V*) curves were measured using an HP4140 pA, and the capacitance-voltage (*C-V*) curves were measured using an HP4194A impedance analyzer at 10 kHz at room temperature. The bias was applied to the TE, and the Ru BE was grounded.

4.3. Results and Discussions

To understand the effect of Al doping on STO films, three sets of STO films were prepared: undoped STO, t-Al-STO, and b-Al-STO. First, the doping or diffusion profile of Al was examined based on the ToF-SIMS depth profiles of the t-Al-STO and b-Al-STO, as shown in Figure 4-1(a) and 4-1(b), respectively. The film thicknesses of STO were 21-22 nm. When the Al doping concentration was examined with Auger electron spectroscopy, it was <~1-2%, making the precise depth profiling improbable through that method. As expected, the Al dopants were concentrated at the surface of the STO or the interface between the STO and the Ru substrate in the two cases. The t-Al-STO, however, showed a much more significant diffusion of Al into the underlying STO main layer whereas the Al was mostly confined within the seed layer region for the b-Al-STO case. This can be understood from the process steps; for the b-Al case, the (initially amorphous-like) seed layer had undergone the RTA process, during which the Al may diffuse and find stable locations within the STO layer through the high thermal energy. Therefore, during the subsequent STO main layer ALD at 370 °C, its diffusion into the main layer may be minimized. In contrast, for the t-Al-STO case, the Al atoms on top of the STO main layer may find fast diffusion paths, probably grain boundaries, and may be readily diffused into the STO layer. The total amount of Al was slightly larger in the t-Al-STO case than in the b-Al case (Figure 4-2 for the ToF-SIMS depth profiles in linear scale). This is perhaps

due to the different ALD temperature of the Al_2O_3 cycle (370 °C for t-Al-STO and 230 °C for b-Al-STO).

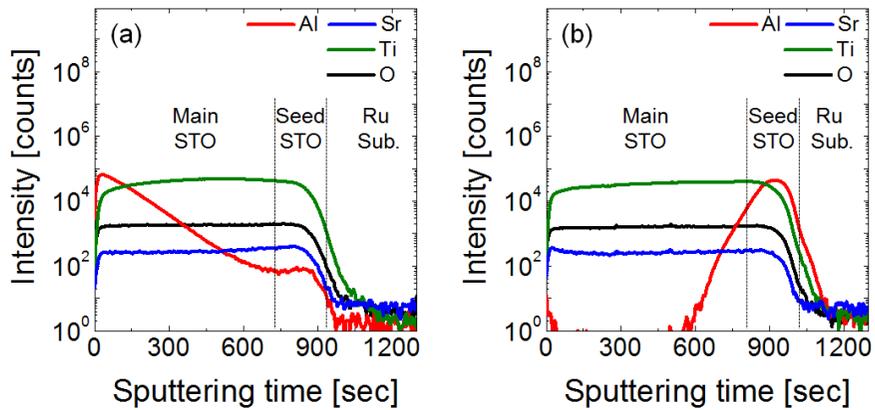


Figure 4-1 ToF-SIMS depth profiles of the 21-22 nm (a) t-Al-STO and (b)

b-Al-STO films

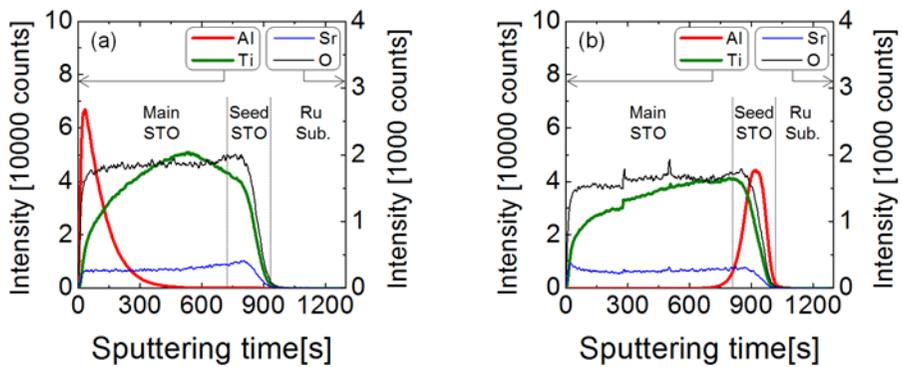


Figure 4-2 Linear-scale ToF-SIMS depth profiles of 21-22 nm (a) t-Al-STO

and (b) b-Al-STO

Figure 4-3(a) shows the GAXRD peaks of the three films, and Figure 4-3(b) shows the enlarged STO diffraction peaks of the (110) and (200) planes. The thicknesses of the three films were controlled and kept at 21-22 nm. All the three samples showed obvious STO diffraction peaks (JCPDS #350734), which is consistent with the previous reports on undoped STO films with two-step growth.¹⁰ It is worth noting that the intensity and position of the diffraction peaks of the t-Al-STO film hardly varied from those in the undoped STO case whereas those of the b-Al-STO film were certainly changed. The peaks were weakened, and their positions were shifted towards the lower 2θ region, suggesting an increase in the lattice constant. As the film properties of the main layer were intimately affected by the property of the underlying seed layer,¹²⁻¹³ these variations in the STO structure could be induced by the change in the structure of the seed layer.

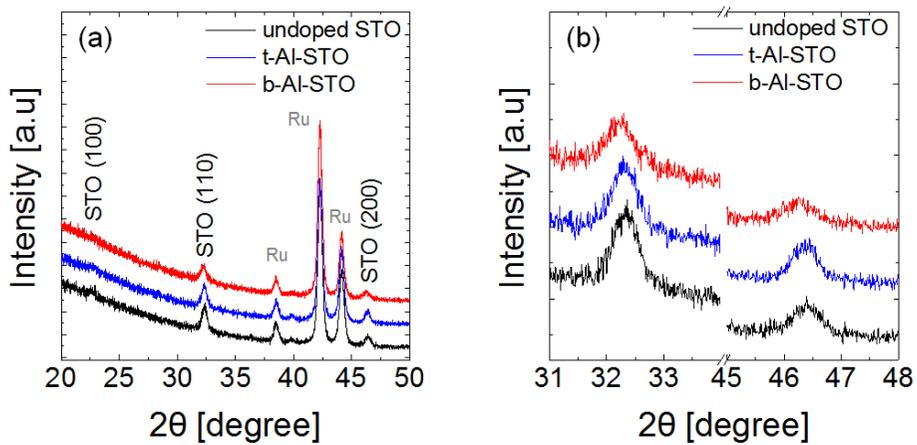


Figure 4-3 GAXRD spectra of the 21-22 nm undoped, t-Al-STO, and b-Al-STO films with an interposed seed layer annealing process. (b) Enlarged peaks of the STO (110) and (200) planes in (a).

Table 4-1 Electronegativity and ionic radius of the Al, Sr, Ti, and O elements

	Electronegativity^[33]	Ionic radius [\AA]^[33]
Al	1.61	0.68
Sr	0.95	1.58
Ti	1.54	0.74
O	3.44	1.26

Based on the electronegativity and ionic radius of the constituent ions shown in Table 4-1, the Al dopant is likely to be the substitutional defect of Ti rather than of Sr and O. As the ionic radius of Al is larger than that of Ti, the substitutional doping of Al in STO must induce lattice expansion. It should be noted that the GAXRD peaks were largely determined by the main layer rather than by the seed layer due to the much higher volume fraction of the main layer. As the main layer of the b-Al-STO sample was not doped with Al, such a peak shift indicated that the crystal structure of the main layer precisely followed that of the seed layer. The lower peak intensity indicated that the main layer crystallinity was also degraded, which implied that the crystallinity of the seed layer was also degraded by the Al doping effect. The Al₂O₃ layer on top of the STO main layer (the t-Al-STO case), however, hardly affected the crystallinity of the STO main layer because it was previously determined by the seed layer crystallinity. The crystallinity of the main layer must not be affected much by Al doping, although the Al content of the main layer was higher in this case. This is the clear evidence that the degree of crystallization of the main layer is largely determined by the crystallinity of the seed layer, not by the Al concentration. The Al concentration of the t-Al-STO film at the film surface was determined as 2.2 at% (Al/(Al+Sr+Ti) ~6.8 at%) via XPS. The surface morphologies of the seed and main layers were very uniform and smooth (root-mean-squared (RMS) roughness <1 nm), regardless of the Al doping and the doping

position (Figure 4-4).

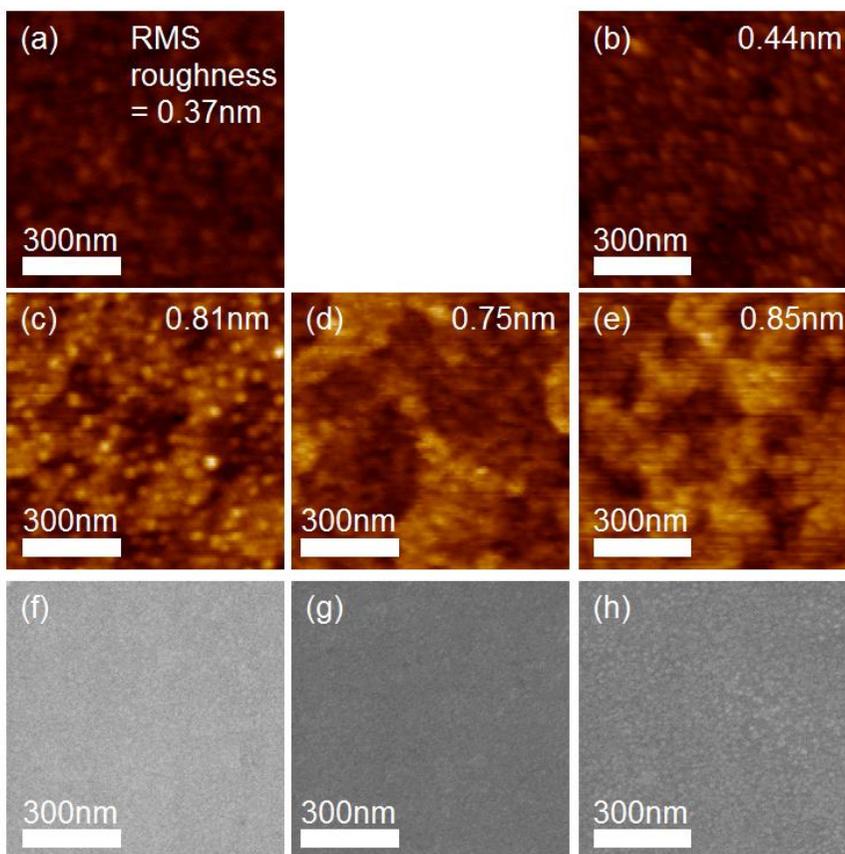


Figure 4-4 (a-e) AFM topographic and (f-h) SEM images of the surfaces of the STO films. (a) 3.5 nm undoped STO seed layer after RTA. (b) 3.5 nm b-Al-STO seed layer after RTA. (c,f) 14 nm in-situ-crystallized undoped STO film. (d,g) 13 nm in-situ-crystallized t-Al-STO film. (e,h) 13 nm in-situ-crystallized b-Al-STO film.

Planar-structured RuO₂/STO/Ru capacitors were fabricated for the undoped STO, t-Al-STO, and b-Al-STO films with different t_{phy} values, and the electrical properties were investigated as shown in Figure 4-5. Figure 4-5(a) shows the variations in t_{ox} values as a function of the t_{phy} . From the inverse slope of the best-linear-fitted lines, the bulk dielectric constants of the main layers were calculated as 149, 120, and 71 for the undoped STO, t-Al-STO, and b-Al-STO, respectively. These results corroborated the XRD results in Figure 4-3(b), where the crystallinity of the STO film was degraded for the b-Al-STO case, but t-Al-STO did not show such a large degradation. For further discussion, the following equation (1)¹² was adopted to explain the data in Figure 4-5(a).

$$t_{\text{ox}} = (3.9/k_{\text{bulk (main)}}) \times t_{\text{phy (main)}} + (3.9/k_{\text{seed}}) \times t_{\text{phy (seed)}} + t_{\text{ox}}^{\text{i (intrinsic)}} \quad (1)$$

Here, $k_{\text{bulk(main)}}$, $t_{\text{phy(main)}}$, k_{seed} , $t_{\text{phy(seed)}}$, and $t_{\text{ox}}^{\text{i (intrinsic)}}$ are the bulk dielectric constant of the main layer, the physical oxide thickness of the main layer, the dielectric constant of the seed layer, the physical oxide thickness of the seed layer (~3.5 nm), and the t_{ox} values by intrinsic interfacial property, such as the dead layer and the low- k interfacial layer (the Al-containing layer for the t-Al-STO and b-Al-STO cases). All the parameters, except for $t_{\text{phy(main)}}$, were considered constant; $t_{\text{phy(main)}}$ was the experimental variable. It was revealed

in the previous study that the k_{seed} is lower than $k_{\text{bulk(main)}}$ due to the high carbon contamination by low process temperature.¹² The k_{seed} of the undoped STO (thus, also for the t-Al-STO) was 49, and the dashed lines in the seed thickness region (<3.5 nm) in Figure 4-5(a) were drawn to make the inverse slope of these lines correspond to this value. The k_{seed} of the b-Al-STO case has not been estimated, but it can be reasonably assumed that it decreased in proportion to the decrease in the $k_{\text{bulk(main)}}$. Therefore, it was assumed to be 23, and the corresponding dashed line can also be drawn in the same figure. Then the $t_{\text{ox}}^{\text{i (intrinsic)}}$ values can be estimated from the y-axis intercepts. While the $t_{\text{ox}}^{\text{i (intrinsic)}}$ values for the undoped STO and t-Al-STO films were almost identical (~0.2 nm), that of the b-Al-STO was almost zero, suggesting that the b-Al-STO layer might improve the interface property. This is a very interesting matter, which needs further research.

Figure 4-5(b) shows the overall capacitor performances (J at 0.8 V vs. t_{ox}) of the three types of STO films. For the case of the undoped STO, a minimum t_{ox} with the sufficiently low J ($<10^{-7}\text{A/cm}^2$) of 0.71 nm was achieved, which is consistent with the previous report.¹² When the seed layer was grown at a higher temperature (370 °C), this value was smaller (~0.39 nm) due to the higher crystallinity and lower impurity concentration of the seed layer.¹² As $k_{\text{bulk (main)}}$ was severely decreased in the b-Al-STO case (149 → 71), the data should be shifted towards a higher t_{ox} direction compared to the undoped STO data for the given value of J . As can be seen from the J - V

curves shown in Figure 4-5(c) and (d), however, the leakage current decreased significantly when Al doping was done (both t-Al-STO and b-Al-STO), and the decreased $k_{\text{bulk (main)}}$ was compensated for by the decreased J . Thus, the trend line of J vs. t_{ox} data almost remained unchanged from the undoped STO films. This means that there was no improvement in the effective electrical performance. It should be noted, however, that such a comparable electrical performance could be achieved from physically thinner b-Al-STO films than from undoped STO films, which is still critical merit of the former.

In the case of the t-Al-STO films, the J - t_{ox} performance was significantly improved by the comparable $k_{\text{bulk (main)}}$ (120 vs. 149) but much lower J values, and the minimum t_{ox} was decreased from 0.71 to 0.63 nm, with an acceptable leakage current density. Figure 4-5(c) and (d) show the J - V curves of the three thin-film types with thicknesses near ~9 and ~21-22 nm, respectively. Regardless of the Al doping position, the Al-doped films showed decreased leakage current density compared to the undoped STO films (~20 times at the thinner film and ~5 times at the thicker film). Such an improvement in the J value through Al doping decreased the critical t_{phy} from 10.3 nm for the undoped STO to 8.6 nm for the t-Al-STO films with a satisfactorily low J value.

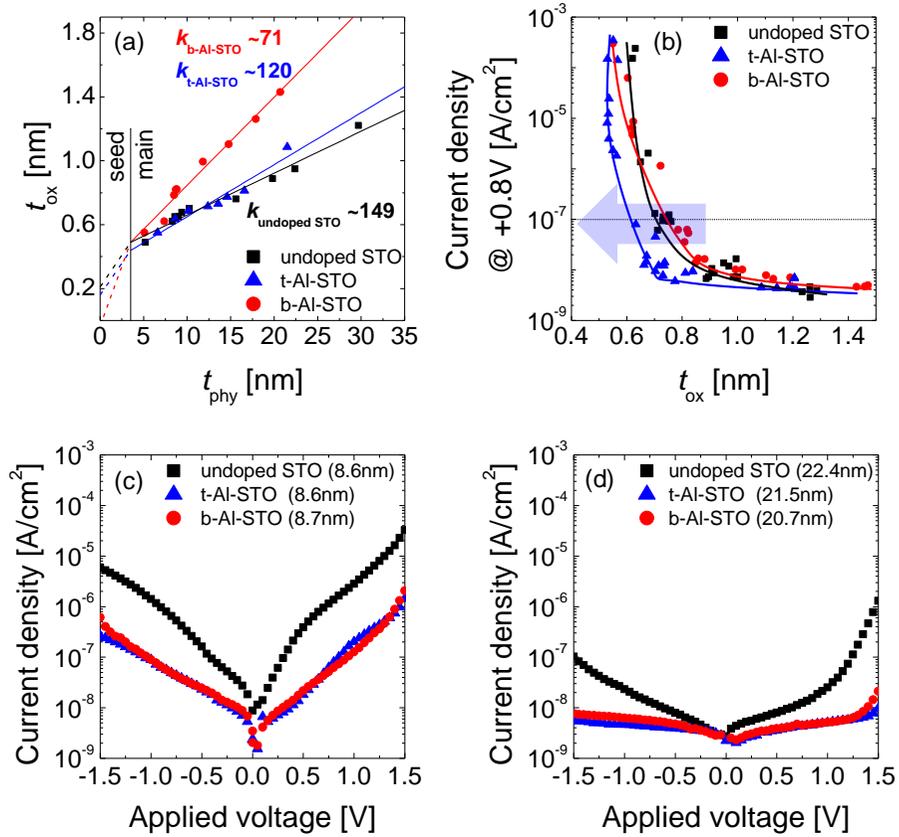


Figure 4-5 (a) Variations in t_{ox} as a function of t_{phy} and (b) variations in J as a function of t_{ox} of the undoped, t-Al-STO, and b-Al-STO films with Ru and RuO₂ as the bottom and top electrodes, respectively. Variations in J as a function of the applied voltage of the (c) 9.0 nm and (d) 21-22 nm STO films.

Figure 4-6(a) shows the valence band edge structures of the 21-22 nm undoped STO, t-Al-STO, and b-Al-STO films on the Ru substrate estimated via XPS. The energy band diagrams could be obtained from these results.²⁷ The valence band offsets (offsets between the Fermi energy level of Ru, which is equilibrated with the XPS system ground potential, and the valence band maximum) were 2.32, 2.19, and 2.32 eV for the undoped STO, t-Al-STO, and b-Al-STO, respectively. Consistent with the ToF-SIMS result in Figure 1(b), XPS showed no Al signal in b-Al-STO (data not shown), and the valence band structure was comparable to that of the undoped STO. Assuming that the E_g of STO (3.2 eV)²⁸ was not varied by the small amount of Al doping, conduction band offsets (offsets between the conduction band minimum and the Fermi energy level of Ru) of 0.88, 1.01, and 0.88 eV were obtained for the undoped STO, t-Al-STO, and b-Al-STO, respectively. The energy band diagrams of these samples are shown in Figure 4-7(a). All the STO samples were n-type even after Al doping, but the conduction band offset, which is one of the critical parameters for the leakage property, increased by ~ 0.13 eV after Al doping. Depending on the Al doping position, there could be a slight tilting of the energy band structure, as shown in the same figure. For the thinner (<10 nm) Al-doped STO films, however, the undoped portion within the film decreased so that the band structure of the entire film became as shown in Figure 4-7(b). There could be a slight

additional barrier lowering (α eV) in such a case due to the involvement of the image force effect under the bias application, which can slightly mitigate the Al doping effect and the energy band bending due to the internal bias. Nonetheless, such barrier height increase could be the major reason for the leakage current decrease by the Al doping shown in Figure 4-5(c). The asymmetry in the J - V curves due to the internal bias owing to the Al doping in t-Al-STO and b-Al-STO is not shown in Figure 4-5(d) because of the large t_{phy} and the high insulating property.

While the role of acceptor doping, such as Al doping in this work, in STO has been extensively studied in the solid-state defect chemistry field,^{29, 30, 31} it can be attributed to another factor. In the case of Al doping in rutile TiO_2 , the first-principles calculation revealed the pinning of the Fermi level at a position closer to the middle position by the Al doping (the conduction band offset increased from ~ 1.0 eV for the undoped TiO_2 to ~ 1.5 eV for the Al-doped TiO_2).³² It can be suggested that a similar mechanism worked in this case (i.e., Al doping lowered the Fermi level of the STO), where the initial position was moved from E_c towards the middle position of E_g due to the natural doping of the electrons by the V_O generation.

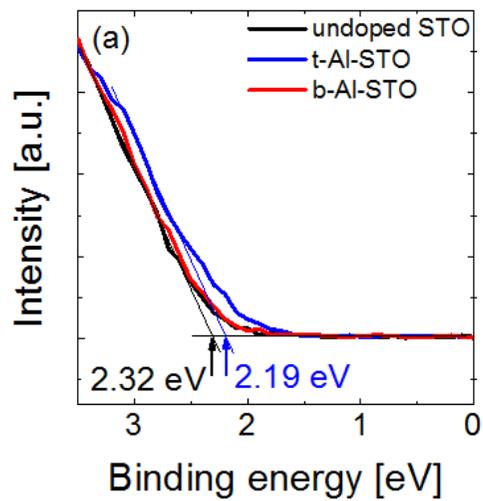


Figure 4-6 (a) Valence band structures of the 21-22 nm undoped, t-Al-STO, and b-Al-STO films on Ru substrates measured via XPS

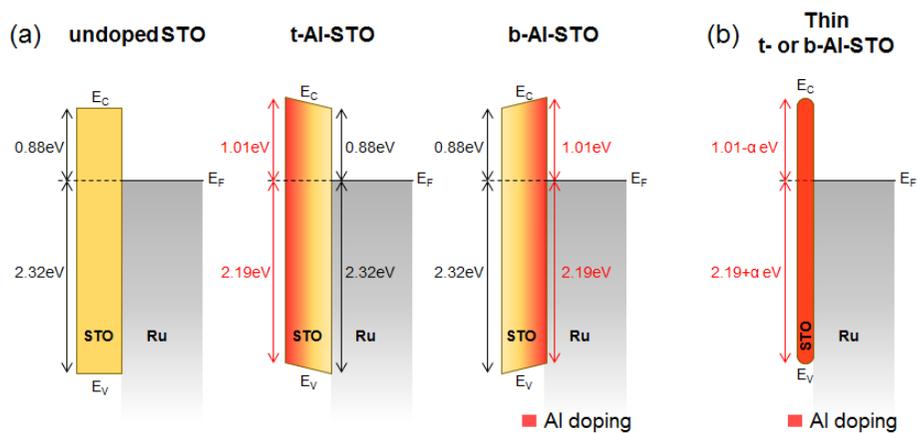


Figure 4-7 (a) Energy band diagrams of the 21-22 nm STO films. (b) Expected energy band diagram of the t-Al-STO or b-Al-STO film when the oxide film thickness is small (<10 nm).

4.4. Summary

In summary, to decrease the leakage current of a SrTiO₃ (STO) thin film grown by atomic layer deposition (ALD), Al doping was attempted. One ALD cycle of Al₂O₃ was processed either at the top or at the bottom of the STO films, and the electrical properties were compared with those of the undoped STO films. The ~3.5-nm-thick seed layer was first deposited and crystallized through rapid thermal annealing, and 5- to 20-nm-thick main layers were subsequently grown for the in-situ crystallization of the main layer. When an Al₂O₃ deposition cycle was inserted below the first seed layer, the crystallization of the STO films was disturbed, and the bulk dielectric constant was degraded from 149 (undoped STO) to 71. When an Al₂O₃ deposition cycle was performed after the STO main layer growth, however, the dielectric constant degradation was minimized (120). In both cases, the leakage current was decreased 20 times compared with the undoped STO case due to the conduction band offset increase. Consequently, the equivalent oxide thickness and physical oxide thickness decreased from 0.71 to 0.63 nm and from 10.3 to 8.6 nm, respectively, through Al doping on the top of the STO films with a sufficiently low leakage current ($<10^{-7}$ A/cm²).

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5. Conclusion

The growth behavior of the STO thin film deposition process was studied, and various thin film characteristics such as electrical characteristics analysis through the fabrication of metal-insulator-metal (MIM) structure capacitors were also evaluated.

First, the crystallization and growth behavior of the upper thin film was analyzed without depositing the upper thin film deposited at 650 °C at a high temperature. Amorphous and crystalline materials were mixed at a crystallization temperature of 550 °C to 600 °C, and the deposited thin film also depends on the crystallinity of the underlying thin film. Further, when Ru is deposited as a lower substrate, oxygen is diffused between the crystal grains of the lower STO thin film, and the growth rate of the upper STO thin film is increased. As a result, an equivalent oxide film of 0.52 nm was formed at a leakage current of 2.5×10^{-8} A/cm²

Second, the deposition temperature of the lower STO thin film was deposited at a low temperature of 230 °C. The high reactivity of the STO on the Ru is because the ruthenium undergoes redox process and supplies excess oxygen to the strontium oxide film having a considerable thermodynamic forming energy. The deposition temperature was lowered by annealing at a low temperature of 230 °C, suppressing the abnormal reaction, and the microcracks of the lower STO thin film were reduced to form a

denser lower STO thin film and increase the density of the STO thin film deposited on the upper side. As a result, the bulk dielectric constant increased from 101 to 167 under the conditions of deposition of the lower STO thin film at a high temperature of 370 °C.

Third, Al was doped to reduce the high leakage current of STO thin films with low bandgap energies of 3.0 to 3.2 eV. When the bottom Al is doped, crystallization of the lower STO thin film is lowered, and the dielectric constant of the upper STO thin film is lowered from 149 to 71. When the uppermost STO thin film is doped with Al, crystallinity of the crystallized STO thin film is not significantly affected. However, in both cases, the decrease in leakage current is more than 20 times, which is a result of improvement in the relationship between the leakage current density and the equivalent oxide film. As a result, the thickness of the equivalent oxide film at 0.8 volt, which is the operating voltage of the DRAM, decreases from 0.71 nm to 0.63 nm, and the physical thickness also decreases from 10.3 nm to 8.6 nm.

Curriculum Vitae

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I. Educations

1992. 3 - 1998. 8	B.S. Department of Chemistry Korea University, Seoul, Korea
1998. 9 – 2000. 8	M.S. Department of Chemistry Korea University, Seoul, Korea
2015. 3 – 2019.2	Ph.D. Department of Materials Science and Engineering Seoul National University, Seoul, Korea

II. Research Areas

1. Atomic Layer Deposition

- Atomic layer deposition of high- k dielectric materials and electrodes
- Atomic layer deposition of multi-component materials
- Control of non-ideal growth behavior
- Growth mechanism of dielectric thin film
- Film characterization
- Thin films deposition technique

2. Chemical Vapor Deposition

- Chemical vapor deposition of low- k dielectric materials.
- Characterization of electronic properties of thick films
- Microstructure analysis
- Control of particle of the thin film growth

3. Dynamic Random Access Memory (DRAM) devices

- Dielectric materials for capacitors (SrTiO_3 , SrO , TiO_2 , ZrO_2 , Al_2O_3)
- Electronic materials for capacitors (Ru , RuO_2)

4. Thin Film Materials and Devices

- Characterization of electronic properties of thin films
 - Microstructure analysis
 - Thin films deposition technique
-
-

III. Experimental Skills

1. Deposition methods

- ALD for dielectric material deposition (SrTiO₃, SrO, TiO₂, Al₂O₃, Y₂O₃, ZrO₂)
- CVD for material deposition (SiO₂, amorphous carbon, BPSG :Boron phosphorous silicate glass, Plasma enhanced CVD)
- SOG(Spin on glass) for thin film : PHPS(perhydropolysilazane), amorphous carbon layer.
- DC magnetron sputtering (Ru, RuO₂, Pt)
- Handling and maintenance of high vacuum equipment

2. Sample preparation

- Conventional furnace annealing for ambient and vacuum annealing
- Surface cleaning/treatment/etching : plasma treatment, HF cleaning, Dry etching, Wet etching
- SEM sampling

3. Analysis methods

- X-Ray Fluorescence Analyzer (XRF, Thermo scientific, ART Quant'X EDXRF) for analysis of composition and layer density of film
- X-ray Diffractometer (PANalytical, X'Pert PRO MPD) for measurement of

X-ray diffraction, X-ray reflection and reciprocal space mapping.

- Atomic Force Microscopy (AFM, JEOL, JSPM-5200) for analysis of the topography
- Spectroscopic Ellipsometer (SE, J.A. Woollam, M-2000) for analysis of optical properties and thicknesses of thin films
- Four point probe for resistivity measurement of metals and conducting materials
- Pulse/pattern generator (Agilent, 81110A/81111A) and digital oscilloscope for pulse switching measurement of ferroelectric materials
- HP4194A for C-V and impedance measurement of capacitors
- HP4140B and HP4145B for I-V measurement of capacitors
- Characterizing thin films by XPS, AES, TEM

List of publications

1. Refereed Journal Articles (SCI)

1.1 Domestic

1.2. International

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3. **Sang Hyeon Kim**, Woongkyu Lee, Cheol Hyun An, Dae Seon Kwon, Dong-Gun Kim, Soon Hyung Cha, Seong Tak Cho, and Cheol Seong Hwang, “Effect of Growth Temperature during the Atomic Layer Deposition of the SrTiO₃ Seed Layer on the Properties of RuO₂/SrTiO₃/Ru Capacitors for Dynamic Random Access Memory Applications” *ACS Appl. Mater. Interfaces*, **10**, 41544 (2018)
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2. Hoju Song, Cheol Hyun An, Younjin Jang, Jun Shik Kim, Dae Seon Kwon, **Sang Hyeon Kim** and Cheol Seong Hwang, “Evaluation of SnO₂ thin films to suppress reduction of RuO₂ electrode during atomic layer deposition of rutile structured TiO₂ films”, 제 24회 한국반도체학술대회, 강원도 대명비발디파크, 2017년 2월 13일-15일

3. Cheol Hyun An, **Sang Hyeon Kim**, Hoju Song, Dae Seon Kwon, and Cheol Seong Hwang, “Growth and electric characteristics of SrRuO₃/Pt bimetal electrodes for SrTiO₃ dielectric layer”, 제 24회 한국반도체학술대회, 강원도 대명비발디파크, 2017년 2월 13일-15일
4. Dae Seon Kwon, Cheol Hyun An, **Sang Hyeon Kim**, Hoju Song, Seong Tak Cho, Soon Hyung Cha, Taishi Furukawa, Teppei Hayakawa, Kazuhisa Kawano and Cheol Seong Hwang, “Atomic layer deposition of Ru thin films using ‘Rudense’ as Ru precursor”, 제 25회 한국 반도체 학술대회, 강원 하이원리조트, 2018년 2월 5일-7일
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6. Seong Tak Cho, Cheol Hyun An, **Sang Hyeon Kim**, Dong gun Kim, Dae Seon Kwon, Soon Hyung Cha, and Cheol Seong Hwang, “MIM capacitor based on ZrO₂/Y₂O₃/ZrO₂ dielectric for DRAM devices”, 제 25회 한국 반도체 학술대회, 강원 하이원리조트, 2018년 2월 5일-7일
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8. **Sang Hyeon Kim**, Cheol Hyun An, Dae Seon Kwon, Dong-Gun Kim, Soon Hyung Cha, Seong Tak Cho and Cheol Seong Hwang, “The impact of the annealing temperature of the seed layer on the growth and the electrical properties of the main layer in atomic layer deposition of SrTiO₃ films”, 제 26회 한국 반도체 학술대회, 강원 웰리힐리파크, 2019년 2월 13일-15일.

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3. Hoju Song, Cheol Hyun An, Younjin Jang, **Sang Hyeon Kim**, Min Jung Chung and Cheol Seong Hwang, “Adoption of SnO₂ thin films to prevent reduction RuO₂ to Ru during atomic layer deposition of TiO₂ films for DRAM Capacitor”, ALD 2016, Dublin, Ireland, July 24-27 (2016)

4. Cheol Hyun An, Woongkyu Lee, **Sang Hyeon Kim**, Hoju Song and Cheol Seong Hwang, “Growth and electric characteristics of SrRuO₃/Pt bimetal electrodes for SrTiO₃ dielectric layer”, ALD 2016, Dublin, Ireland, July 24-27 (2016)
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6. **Sang Hyeon Kim**, Woongkyu Lee, Cheol Hyun An, Hoju Song, Dae Seon Kwon, and Cheol Seong Hwang, “Seed layer thickness effects of atomic layer deposited SrTiO₃ thin film”, E-MRS 2017, Strasbourg, France, May 22-26 (2017)
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Abstract (in Korean)

디램 셀은 한 개의 커패시터와 한 개의 트랜지스터로 구성되어 있다. 디램 셀 내에서 트랜지스터는 디램 셀 어레이에서 특정 셀을 읽거나 쓸 수 있도록 선택하는 역할을 수행하며, 커패시터는 전하를 저장하여 '0' 과 '1' 의 데이터를 기록하는 역할을 한다. 디램 소자의 집적화를 위해서는 트랜지스터 및 커패시터를 포함한 여러 공정 요소 기술의 개발이 중요하나, 그 중 좁은 면적에서 충분한 정전용량을 확보하기 위한 커패시터 요소 기술이 가장 핵심기술이다. 현재 생산되는 디램은 고유전막으로 산화지르코늄기반의 알루미늄과의 샌드위치 구조를 채택하고 있다. 본 논문은 고유전막 스트론튬타이타늄산화막(SrTiO_3 , STO)을 원자층 증착 방법으로 증착하여 박막의 성장거동, 저온 증착방법 및 누설전류 감소를 연구하였다.

본 학위논문에는 스트론튬전구체와 타이타늄전구체로 비스 이소프로필사이클로펜타다이에닐스트론튬($\text{Sr}(\text{PrCp})_2$)와 트리메톡시펜타 메틸사이클로펜타다이에닐타이타늄 $\text{Ti}(\text{OMe})_3(\text{CpMe}_5)$ 를 각각 오존과 물을 산소 공급원으로 하여 증착하였다. 스트론튬타이타늄산화막 증착 공정의 성장거동을 연구하였으며, 금속-절연체-금속 (metal-insulator-metal, MIM) 구조 커패시터 제작을 통한 전기적 특성 분석 등 여러 가지 박막 특성 역시 평가하였다.

첫 번째로, 2단계로 증착한 스트론튬타이타늄산화막의 상부 박막 성장거동에 대해 연구하였다. 비정질상에서 증착된 5 nm 두께의 하부 박막의 열처리 온도를 450도에서 650도까지 각각의 온도조건을 다르게하여 하부 박막의 결정화 정도를 바꾸었다. 그 위에 증착된 상부 박막을 650도 고온에서 증착하여 결정화 열처리 과정을 따로 진행하지 않으면서 상부 박막의 결정화도와 성장 거동을 분석하였다. 하부 박막의 결정화되는 온도인 550도에서 600도 사이에서 비정질과 결정질이 혼재되어 있으며, 그 위에

증착된 상부 박막도 하부 박막의 결정화도에 의존하고 있었다. 또한, 루테튬 금속을 하부 기판으로 하여 증착하면, 하부 스트론튬타이타늄산화막의 결정립사이로 산소가 확산되는 통로가 되어 상부 스트론튬타이타늄산화막의 성장속도가 증가된다. 이러한 과잉의 산소 공급현상은 실리콘을 하부 기판으로 사용하면 발생하지 않는다. 하부 스트론튬타이타늄산화막의 열처리 온도가 600도 이상에서는 거의 대부분의 하부 스트론튬타이타늄산화막이 열처리되고, 상부 스트론튬타이타늄산화막도 동일한 경향으로 결정화 되면서 증착된다. 그 결과, 0.8볼트의 전압에서 2.5×10^{-8} A/cm²의 누설전류에서 0.52 nm의 등가산화막을 형성하였다.

두 번째로, 하부 스트론튬타이타늄산화막의 증착 온도를 230도의 저온에서 증착하고, 상부 스트론튬타이타늄산화막은 370도 고온에서 증착하였다. 스트론튬타이타늄산화막은 낮은 밴드갭 에너지와 관련된 높은 누설전류 특성을 가지며, 누설전류를 낮추기 위해 전극물질로 높은 일함수를 갖는 루테튬 금속을 적용하여야 한다. 하지만, 루테튬과 스트론튬타이타늄산화막계면에서 비이상적으로 높은 반응성으로 화학기상반응과 유사한 반응이 발생한다. 이러한 이상반응은 루테튬이 산화환원과정을 거치면서 열역학적 형성 에너지가 큰 스트론튬산화막에 과잉의 산소를 공급하기 때문이다. 증착온도를 230도의 저온에서 증착하여 이러한 비이상반응을 억제하였으며, 하부 스트론튬타이타늄산화막의 미세 균열이 감소하여 더 밀집한 하부 스트론튬타이타늄산화막을 형성하고 상부에 증착되는 스트론튬타이타늄산화막의 밀도를 증가시키게 된다. 그 결과, 벌크 유전율은 370도의 고온에서 하부 스트론튬타이타늄산화막을 증착한 조건에서의 101에서 167로 증가하였다. 하지만, 저온 증착 시 증착 시간이 증가하면서 탄소 불순물이 증가하고, 계면의 등가산화막의 두께가 증가하는 단점이 있다.

세 번째로 3.0 ~ 3.2 전자볼트의 낮은 밴드갭에너지의 스트론튬타이타늄산화막박막의 높은 누설전류를 감소하기 위해 알루미늄을 도핑하였다. 스트론튬타이타늄산화막에 한 사이클의 알루미늄산화막을 도핑하였으며, 하부 스트론튬타이타늄산화막과 루테튬 기판 사이와 상부 스트론튬타이타늄산화막의 맨 위의 두 가지 경우로 알루미늄 도핑위치를 평가하였다. 맨 아래 알루미늄을 도핑하면 하부 스트론튬타이타늄산화막의 결정화가 낮아져서 상부 스트론튬타이타늄산화막의 유전율이 149에서 71로 낮아지며, 스트론튬타이타늄산화막의 맨 위에 알루미늄을 도핑하면 이미 결정화된 스트론튬타이타늄산화막의 결정성에 큰 영향을 끼치지 못하여 유전율은 120으로 덜 감소한다. 하지만, 두 가지 경우 모두 누설전류의 감소는 20배 이상으로 누설전류밀도와 증가산화막의 관계에서 개선되는 결과이다. 그 결과, 디램의 동작 전압인 0.8 볼트에서의 증가산화막의 두께는 0.71 nm에서 0.63 nm로 감소하며, 물리적 두께도 10.3 nm에서 8.6 nm 로 감소하는 결과이다.

결론적으로 루테튬 전극에서 2단계로 증착한 스트론튬타이타늄산화막의 거동을 분석하여 임계온도에서의 결정질과 비정질의 증착 거동에 대해 분석하였으며, 증착 온도를 낮추어 비 이상 증착 현상을 억제하였다. 또한, 스트론튬타이타늄산화막의 낮은 밴드갭 에너지를 극복하기 위해 알루미늄을 도핑하여 0.8V의 디램동작 전압에서 증가산화막 두께 0.63nm와 물리적 두께도 8.6nm로 감소하였다.

주요어: 디램 커패시터, 유전물질, SrTiO_3 , Ru, RuO_2 , SrO, TiO_2 , 오존, 물, 원자층증착방법, 고유전율, 등가산화막두께, 정전용량, 누설전류, in-situ결정화

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