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Simple reversible energy recovery logic using NMOS switch networks with cross-coupled PMOS pair

Kipaek Kwon and Soo-Ik Chae

A simpler reversible energy recovery logic is proposed, called feedback RERL, which is based on the previously presented reversible energy recovery logic (RERL), which does not have any non-adiabatic losses.

Introduction: Since the concept of adiabatic switching was introduced, many adiabatic circuits have been proposed [1 – 6]. Besides leakage current loss, there are two types of energy dissipation in these adiabatic circuits: adiabatic and non-adiabatic [1]. Several schemes for reversible adiabatic logic have been published [1 – 4], which can be used to eliminate non-adiabatic losses and/or solve the 'retractile cascades' problem [4]. In the logic proposed by the USC ACMOS group [2], non-adiabatic losses still exist, even though the 'retractile cascades' problem is solved. SCRL (split-level charge recovery logic) [3] requires a very complex clocking scheme, so it is not suitable for implementing in a complex system, although no non-adiabatic losses occur in SCRL. We have proposed a reversible adiabatic logic [1] without non-adiabatic losses, which is referred to in this Letter as transmission-gate RERL (tRERL).

Here, we describe feedback RERL (fRERL) and compare it with other logic schemes. Although a transmission gate is used as a logic switch in tRERL, an NMOS transistor is used in fRERL. To eliminate non-adiabatic losses due to the reduced swing in the NMOS transistor network, fRERL employs a pair of extra PMOS transistors with feedback connection, as shown in Fig. 2. Because of its reduced overhead and parasitic capacitance, the energy dissipation in an fRERL circuit is reduced substantially, compared to that in a corresponding tRERL circuit.
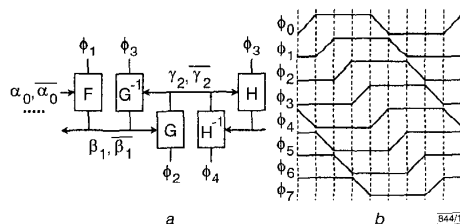

Fig. 1 *Reversible multistage pipeline scheme and waveforms of 8-phase clocked power in fRERL*

a Reversible multistage pipeline scheme
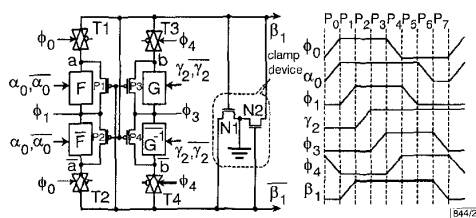*b* Waveforms

Fig. 2 *Schematic diagram and signal waveforms of fRERL*

fRERL operation: The reversible multistage pipeline scheme and 8-phase clocked power required in the fRERL are the same as those in the tRERL, as shown in Fig. 1. Fig. 2a shows a dual-rail fRERL logic gate with forward and backward logic functions F, G^{-1}, where $\bar{F}$, $\bar{G}^{-1}$ are the complementary logic functions of F and G^{-1}, respectively. Assuming that the logic F (α_0, $\bar{\alpha}_0$) is true, the output signal β_1 is high when forward inputs α_0 and $\bar{\alpha}_0$ are valid, as shown in Fig. 1b. The subscript of each signal represents the phase of the clocked power and implies that the signal becomes valid when the corresponding clocked power goes from low to high. Note that the current path of a logic block F is formed with valid inputs α_0 and $\bar{\alpha}_0$ if the logic F (α_0, $\bar{\alpha}_0$) is true.

Assuming that all internal nodes are initially grounded and F (α_0, $\bar{\alpha}_0$) and G^{-1} (γ_2, $\bar{\gamma}_2$) are true, the operation of the fRERL gate in Fig. 2 is as follows. During P_0, forward isolation switches $T1$ and $T2$ are turned on, and backward isolation switches $T3$ and $T4$ are turned off. The forward inputs α_0 and $\bar{\alpha}_0$ become valid after ϕ_0 goes high. During P_1, the output signals β_1 go high because ϕ_1 goes high, switch $T1$ is on, and the current path of the logic block F is formed. Note that node a cannot swing fully without a pair of cross-coupled PMOS transistors since an NMOS transistor is not a perfect switch. When node a goes high, β_1 goes high because switch $T1$ is on. Then, PMOS $P2$ stays off because β_1 goes high, and PMOS $P1$ is turned on because $\bar{\beta}_1$ stays at ground. Because $P1$ is on, node a goes up to peak voltage V_{dd} by following ϕ_1 exactly. Nodes $\bar{\beta}_1$ and $\bar{a}$ are grounded with $N1$.

During P_2, the backward inputs γ_2 and $\bar{\gamma}_2$, which are the outputs of the next stage, become valid after ϕ_2 goes high. The backward logic G^{-1} (γ_2, $\bar{\gamma}_2$) is then evaluated. During P_3, internal node b follows ϕ_3 exactly with the help of PMOS $P3$. During P_4, the backward switches $T3$ and $T4$ are turned on and the forward switches $T1$ and $T2$ are turned off. During P_5, the charges at node a and the internal nodes of the forward logic block F are recovered to the clocked power ϕ_1 when ϕ_1 is grounded, while the output β_1 remains high. During P_6, the inputs α_0 and $\bar{\alpha}_0$ are de-energised to ground because ϕ_2 is grounded. During P_7, the charge at output β_1 is recovered to the clocked power ϕ_3 as ϕ_3 is grounded. The charges at node b and the internal nodes of a reversing logic block G^{-1} are recovered to the clocked power ϕ_3 as well. All the internal nodes are then grounded just as in the initial conditions.
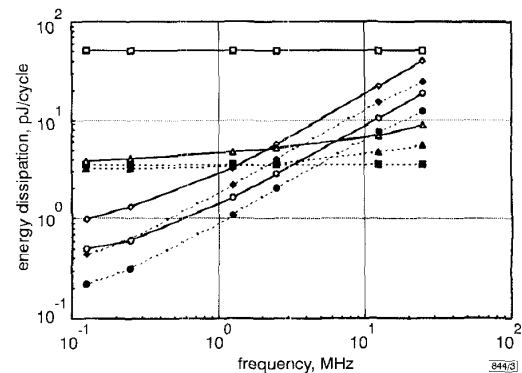

Fig. 3 *Energy dissipation in full adder against operating frequency*

—◇— original RERL (3.3 V)
—□— CMOS (3.3 V)
—△— 2N-2N2P (3.3 V)
—○— fRERL (3.3 V)
- -◆- - original RERL (2.4 V)
- -■- - CMOS (0.87 V)
- -▲- - 2N-2N2P (1.8 V)
- -●- - fRERL (2.4 V)

Energy comparison: Energy dissipation is compared for full adders implemented with a conventional static CMOS circuit and three adiabatic logic circuits: 2N-2N2P [6], tRERL, and fRERL. All circuits are designed with 0.8µm n-well CMOS technology. The threshold voltages of the PMOS and NMOS transistors are –0.87 and 0.70V, respectively. We assume that the capacitance of each output signal node is 0.1pF in simulation. To allow fair comparison, we also present two simulation results: one for a supply voltage of 3.3V and the other for a supply voltage that minimises the energy dissipation for each logic family. In particular for the CMOS full adder, the supply voltage for minimal energy dissipa-

tion is selected as the absolute value of the PMOS threshold voltage, which is the theoretical lower bound.

Fig. 3 shows the energy dissipation in a full adder against the clock frequency. In both tRERL and fRERL full adders, energy dissipation decreases as the clock frequency decreases because they consume only adiabatic losses, which are proportional to the operating frequency. In contrast, the energy dissipation of the CMOS full adder remains constant. Energy dissipation in the 2N-2N2P full adder decreases as the operating frequency decreases, but it is saturated to a lower bound, which equals its non-adiabatic loss. In low-speed operation, both tRERL and fRERL full adders consume less energy than the theoretical energy limit of the CMOS full adder.

The number of transistors in the fRERL adder is ~22% less than that in the tRERL adder, being 89 and 114, respectively. Because the load capacitance of each node in fRERL is reduced, the fRERL full adder uses only ~40% of the energy consumed in the tRERL adder.

Conclusion: Because the proposed fRERL is a simpler form of RERL, its circuit overhead is lower compared to that of tRERL. Simulation results show that an fRERL full adder consumes less energy than a CMOS adder under low-speed operation, even when the supply voltage of the CMOS logic is reduced to the PMOS threshold voltage. Furthermore, the fRERL full adder saves ~60% of the energy consumed in the tRERL adder because of its reduced capacitance. Therefore, the fRERL is another viable approach for ultra-low-energy applications.

Kipaek Kwon and Soo-Ik Chae (*School of Electrical Engineering, Seoul National University, Shinlim-dong, Kwanak-gu, Seoul 151-742, Korea*)

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Extension of FDTD method to non-uniform excitations

M.E. Potter, M. Okoniewski and M.A. Stuchly

A new representation of a line source in the finite difference time domain method has been implemented, using the total/scattered field formulation. Verification for two problems with analytic solutions showed excellent accuracy. One application is the simulation of the exposure of a human body in close proximity to a 60Hz transmission line.

Introduction: The total/scattered field formulation in the finite difference time domain (FDTD) method has previously been described for an arbitrary uniform plane wave excitation [1]. This formulation has been extended in this work to include fields from infinite line sources. The motivation is provided by the need to evaluate the exposure of humans to low frequency electric and electromagnetic fields. Such situations occur in the electric utility industry, and in low radio frequency antenna farms. Although the low frequency extensions to the FDTD are of primary interest, the technique is also applicable to high frequency problems.

For sufficiently low frequencies, quasistatic approximations can be used, as has been previously explored for uniform fields [2]. Under these conditions with a ramp excitation, very short run times (a fraction of the signal period) are sufficient for extracting meaningful results. Under quasistatic conditions, the electric and magnetic fields become decoupled.

Method: The formulation of the FDTD method in the total scattered field formulation [1] is extended by implementing the analytic expressions for excitation corresponding to infinite line sources in the TEM mode. The field magnitudes at a given point in space are inversely proportional to the distance from the line, and are aligned in the radial and circumferential direction for electric and magnetic fields, respectively. Thus, the efficient incident-field array (IFA) for the uniform plane wave excitation scheme [1] can be modified to reflect a cylindrical TEM configuration.

The IFA uniform plane wave is uniquely specified by three *fixed* angles (θ, φ, ψ) which define the direction of propagation (θ, φ) and the electric field polarisation (ψ). For the TEM configuration, the field polarisation angle ψ is no longer fixed, but becomes a variable dependent on the field point position with respect to the line. Hence the IFA algorithm connecting conditions still hold with the modification that ψ becomes a variable instead of a parameter. Assuming that the line source is oriented parallel to the x-axis, and passes through the point (yh, zh), then ψ is given as:

$$v = \begin{cases} \tan^{-1}\left(\dfrac{z - zh}{y - yh}\right) - \hat{x} \\ \tan^{-1}\left(\dfrac{z - zh}{yh - y}\right) + \hat{x} \end{cases} \qquad (1)$$

The resultant calculated incident field is scaled by the inverse of the distance to the line source. The FDTD code is further modified to allow for multiple waves from infinite line sources, which are combined at the Huygen's surface. Thus, exposure to electric or magnetic fields can be studied in isolation by creating a standing wave condition [2].

Verification: The electric and magnetic fields in the free space analytic solution were compared with the FDTD solution for a 0.2 × 1.1 × 1.1m³ computational domain, truncated by a perfectly matched layer (PML) (6, P, 40dB) on all sides [3]. An x-directed line source centred 0.5m over the domain was applied, with a smoothed ramp excitation to limit high frequency contamination:

$$E_{inc} = \begin{cases} 0 & -\infty < t \le t_0 \\ \cosh(t) - 1 & t_0 < t \le \tau \\ A(t - \tau) + h & t > \tau \end{cases} \qquad (2)$$

Excellent agreement with the analytic solution was achieved for grid resolutions of 0.02 and 0.01m, with maximum transverse relative errors of no more than 0.09 and 0.02% for the coarse and fine grids, respectively. Average relative errors were of the order of 0.008 and 0.005% for coarse and fine grids, respectively. As expected, the Cartesian mesh representation of cylindrical fields introduced longitudinal fields that were non-physical, but they were negligibly small and of the same order of magnitude as the error fields in the transverse direction.

The method was further verified for a lossy sphere of similar size and conductivity to the human body ($\sigma = 1$S/m, radius = 0.5m). The staircased sphere was centred in a computational domain of size 1.1 × 1.1 × 1.1m³, terminated on all sides by a PML (9, P, 60dB). Domain resolution was 0.01m in each direction. A standing wave was created for magnetic field excitation by applying two line sources in opposite directions centred 50cm over the sphere, with the time response of eqn. 2. Source parameters were chosen to simulate a 1A (peak) current of 60Hz. Steady state was reached after 1200 timesteps.