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**M.S. DISSERTATION**

**Spacer Optimization from Gate-Induced  
Drain Leakage Perspective in 3-nm Node  
Device**

3나노 노드 소자에서 기들 측면의 스페이서 최적화

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**August 2019**

**DEPARTMENT OF ELECTRICAL AND  
COMPUTER ENGINEERING  
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# Spacer Optimization from Gate-Induced Drain Leakage Perspective in 3-nm Node Device

3나노 노드 소자에서 기들 측면의 스페이서 최적화

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## Abstract

In this paper, structural and material optimization of gate sidewall spacer in the perspective of off-state leakage current was performed in a 3-nm node Nanoplate FET (NPFET). First, gate induced drain leakage (GIDL) current, a dominant factor of off-state leakage current, and active performance (on-current, on/off current ratio) were co-optimized according to structural correlation of gate sidewall spacer with other structural components such as gate, source, and drain length. Furthermore, by comparing structural relations between gate-spacer and S/D-spacer, a better structural optimization method was proposed. Second, structural and material optimization of asymmetric spacer structure was performed. If the spacer is designed asymmetrically, GIDL current was reduced by 72% through the optimization of the asymmetric spacer, resulting in a 67% reduction in the overall off-state leakage current. Then, the on/off current ratio got enhanced by 4.7 times. Finally, dual-k spacer structure was investigated using the variety of materials along the high-k spacer length. To verify the effect of the dual-k spacer on GIDL current, the GIDL characteristic according to the inner spacer material, which mainly affect the GIDL characteristic in dual-k spacer structure, were compared. Optimization of the gate sidewall spacer, proposed in this paper, showed effectively reduced GIDL current and enhanced active performance.

**Keywords :** Gate-Induced Drain Leakage, Spacer, Ultra-scaled device, Nano-plate FET, Spacer material, structure Optimization.

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# Chapter 1

## Introduction

Semiconductor devices have been continuously scaled down according to Moore's Law [1]. However, miniaturization of the devices was limited by the short channel effect (SCE) problem [2]-[3]. To mitigate the SCE, the device structure has been changed from a planar structure to a multi-gate structure (FinFET), which represents enhanced gate controllability [4]-[6]. Nonetheless, the FinFET still represented insufficient electrostatic gate controllability and severe parasitic components [7]. In order to compensate for this insufficiency, a gate-all-around (GAA) structure, noted as nanowire FET (NWFET), was suggested where the gate covers the entire channel but still showing poor active performance because of the small cross-sectional area [8]-[11]. To overcome the limitations of the NWFET, NPFET, a most promising candidate for future semiconductor device structure, was suggested [12]. NPFET represented superior gate controllability with improved active performance and thus reducing the SCE problem effectively. On the other hand, the enhanced gate controllability caused a high electric field at the drain junction and a significant overlap between the valence band of the channel and the conduction band of the drain extension [13]. As a result, longitudinal band to band tunneling (L-BTBT), which is a dominant component of GIDL current at off-state ( $V_{gs}=0$  V), was increased [14]. The severe increment of the GIDL current resulted in degradation of the off-state performance, becoming a serious problem in the aspect of static power consumption. GIDL can be influenced by various factors in a complex way. However, spacer optimization can be the most effective way to

suppress GIDL current. Spacer can control the gate fringe field applied to the extension region, thereby changing the energy band profile, which is the dominant factor that determines the GIDL characteristic.

Therefore, in this paper, optimization of gate sidewall spacer was performed from off-state leakage perspective in 3-nm node NPFET. First, the GIDL current was minimized by optimizing the relation between the gate sidewall spacer and the gate length and between the gate sidewall spacer and S/D length with constant contacted gate pitch (CGP). When the spacer length changes in a fixed CGP condition, mutual variation between the structures occurs and the electrical characteristic trade-off occurs accordingly, which should be considered during the miniaturization of the device. Second, optimization of asymmetric spacer structure was performed. The contacted gate pitch (CGP) was kept constant to maintain the device scale. This results to the drain spacer varying opposite to the source spacer, and this property differently affects a myriad of electrical performances, including GIDL current. Therefore, the ratio of the drain spacer to the source spacer was optimized to minimize the GIDL current. The spacer material exhibiting optimum electrical characteristics was also identified through a performance analysis based on the spacer material. Finally, dual-k spacer structure was analyzed from GIDL perspective. Dual-k spacer was suggested to minimize the parasitic components, which results in raised on-current and intrinsic delay. However, GIDL can be severely affected by spacer, designed with dual components. To co-optimize the delay performance and off-state characteristic, it is need to optimize the dual-k spacer structure.

# Chapter 2

## Simulation Setup

### 2.1. Device structure

Fig. 1 shows 3-D structure of a 3-nm node NPFET with each cross-sectional view, designed with the reference to the international technology roadmap for semiconductor (ITRS) 2015 [19]. The gate length ( $L_G$ ) was set to be 10 nm, the extension length ( $L_{ext}$ ) 4.5 nm equal to the spacer length, and the S/D length ( $L_{S/D}$ ) 6 nm, resulting in totally 25 nm of the CGP. The overlap length ( $L_{ov}$ ) was fixed at 8 % of  $L_G$  as in the reference case [19] and a graded doping profile was adopted to account for the realistic fabrication conditions. An equivalent oxide thickness (EOT) of 0.7 nm (SiO<sub>2</sub> - 0.45 nm, HfO<sub>2</sub> - 1.5 nm) was used to adjust the inversion layer thickness as 0.8 nm suitable for the 3 nm node. The gate work function was adjusted to a threshold voltage ( $V_{th}$ ) which was matched with the off-current of 100 nA/um as mentioned in [19]. The  $R_{con}$ , was set to be  $3 \times 10^{-9} \Omega \cdot \text{cm}^2$  considering the state-of-the-art process technology. The doping concentration was assumed to be  $1 \times 10^{21} \text{ cm}^{-3}$  of phosphorus in the S/D region, and  $10^{16} \text{ cm}^{-3}$  of boron in the channel to minimize the random dopant fluctuation (RDF) [20]-[21]. All these structural parameters are specified in Table 1.

### 2.2. Simulation condition

3-D technology computer aided design (TCAD) simulation was performed using Synopsys Sentaurus which is well calibrated for analyzing nanoscale devices.

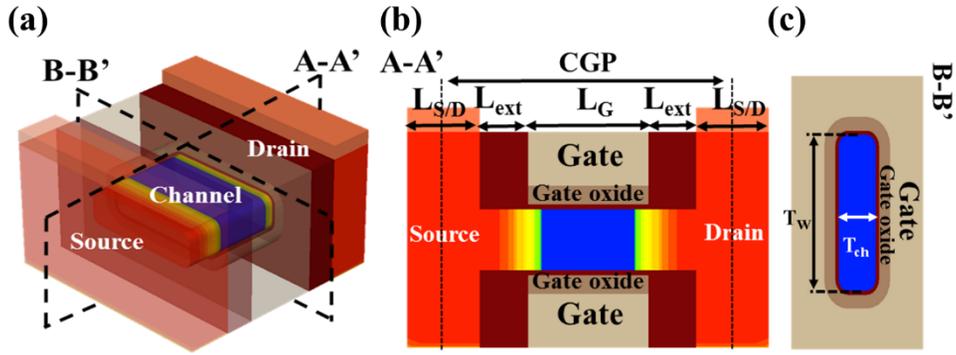


Figure 1. (a) 3-D structure of 3-nm node NPFET, (b) A-A' view, (c) B-B' view.

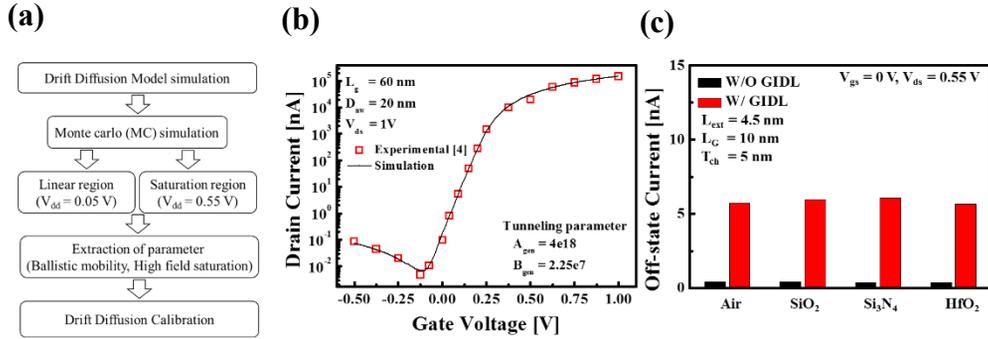


Figure 2. (a) DD approximation calibrated with Monte Carlo (MC) simulation results, (b) tunneling parameter calibration process to experimental data [14], (c) off-state current according to the GIDL condition with each spacer material.

Density gradient quantization and carrier density were accounted for using equantumpotential and Fermi-Dirac. Bandgap narrowing model and Shockley-Read-Hall (SRH) recombination model were also used. To consider mobility degradation due to impurity scattering and carrier-carrier scattering, the Philips mobility model was used and the Lombardi model was included to account for mobility degradation at interfaces. For accurate analysis of electrical characteristics of nanoscale devices, the drift-diffusion (DD) approximation was carefully calculated with the Monte Carlo (MC) simulation for the extraction of the ballistic mobility and the high-field

Table 1. Device parameters for 3-nm node NPFET

Device parameters	Value	Device parameters	Value
Gate length, $L_G$ [nm]	10	Channel doping concentration [ $\text{cm}^{-3}$ ]	$1 \times 10^{16}$
Channel width, $T_w$ [nm]	17	S/D doping concentration [ $\text{cm}^{-3}$ ]	$1 \times 10^{21}$
Channel height, $T_{ch}$ [nm]	5	Contacted gate pitch, CGP [nm]	25
Extension length, $L_{ext}$ [nm]	4.5	Supply voltage [V]	0.55
S/D length, $L_{S/D}$ [nm]	6	Contact resistance [ $\Omega\text{-cm}^2$ ]	$3 \times 10^{-9}$
Equivalent oxide thickness [nm]	0.7		

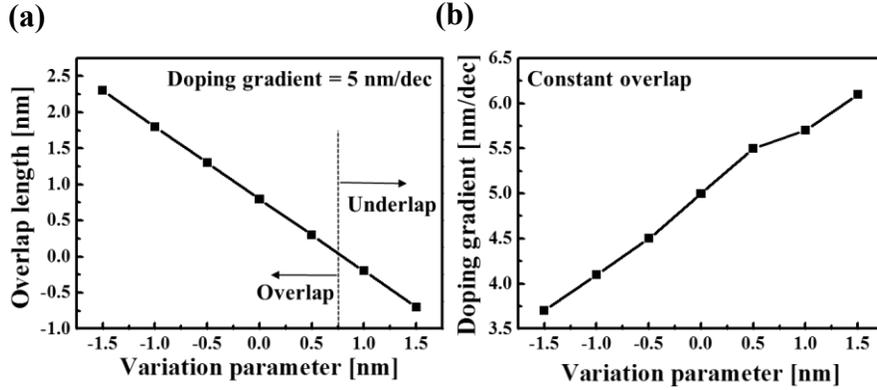


Figure 3. (a) Overlap length ( $L_{ov}$ ) according to variation parameter ( $\Delta L_{ext,G}$  or  $\Delta L_{ext,SD}$ ), (b) Doping gradient according to the variation parameter in constant overlap case.

saturation parameters suitable for a 3-nm node NPFET as illustrated in Fig. 2 (a) [22]-[23]. The Hurkx band to band tunneling (BTBT) model was used to capture tunneling process and the tunneling parameters were calibrated to the measurement data [14] for the accurate GIDL current analysis as illustrated in Fig 2 (b). In addition, in the case of nanowire FET, the bandgap of the silicon increases when the nanowire diameter is 7 nm or less due to the quantum confinement effect. To consider 5 nm channel height ( $T_{ch}$ ) of the NPFET, the input bandgap was 1.241 eV [24]. Air,  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  and  $\text{HfO}_2$  were used as a spacer material to investigate the electrical characteristics according to them, and the interface trap density of the each material was also considered with the reference to the experimental data from [25]-[27].

# Chapter 3

## Structural Relation Optimization

In this chapter, gate induced drain leakage (GIDL) current, a dominant factor of off-state leakage current as shown in Fig 2 (c), and active performance (on-current, on/off current ratio, and dynamic performance) were co-optimized according to structural correlation of gate sidewall spacer with other structural components such as gate, source, and drain length. For simulation convergence, in this chapter, doping concentration was adjusted to  $8 \times 10^{20}$ .

### 3.1. Gate-spacer relation

Fig. 4 shows a schematic view of the variation between the gate and spacer length ( $\Delta L_{ext,G}$ ). The CGP was fixed to maintain the device scale, which makes the total length of the gate and the spacer constant in most cases and the doping gradient was retained to the reference case ( $\Delta L_{ext,G}=0$  nm) as illustrated in Fig. 3 (a). Fig. 5 represents the GIDL current and the band profiles according to  $\Delta L_{ext,G}$ . Fig. 5 (a) indicates that the GIDL current decreases as the spacer length increases for all of the

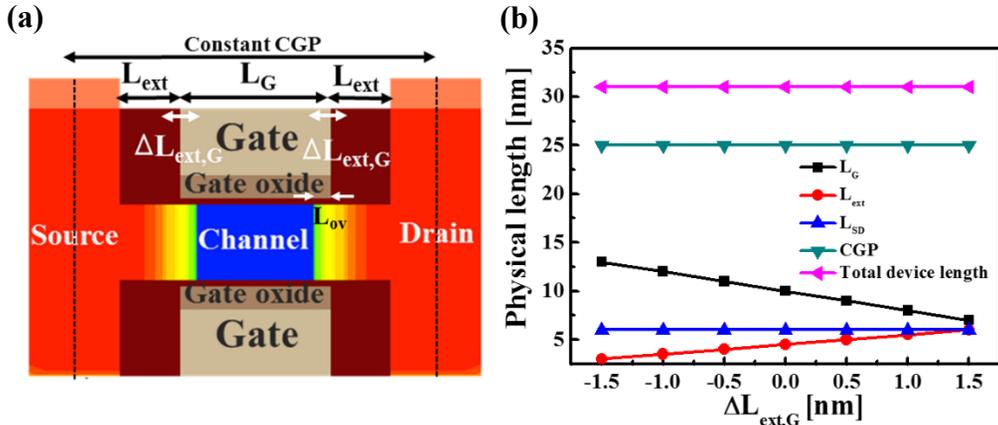


Figure 4. (a) Schematic view of length variations in gate and spacer, (b) their specific relations

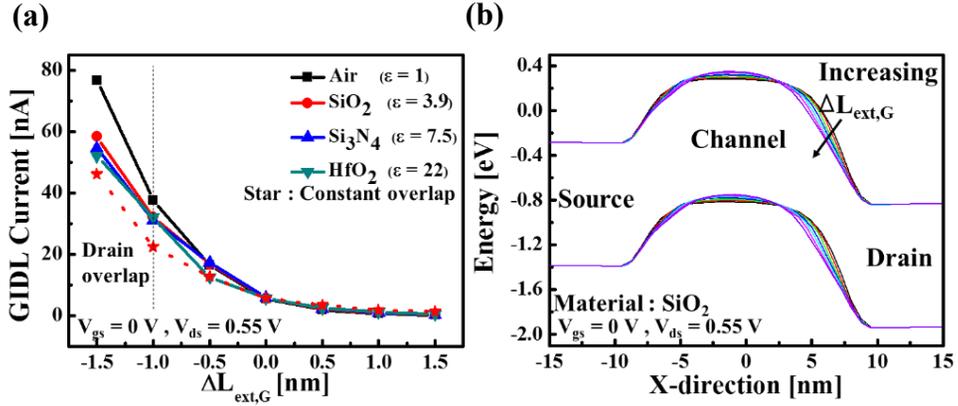


Figure 5. (a) Simulation results of gate-spacer relation for characteristics: (a) GIDL current according to variation of gate and spacer length,  $\Delta L_{\text{ext,G}}$ , (b) energy band profiles for each  $\Delta L_{\text{ext,G}}$  with  $\text{SiO}_2$  spacer material.

spacer materials. Then, as  $\Delta L_{\text{ext,G}}$  increases by 0.5 nm, GIDL current is reduced by 53 %. The shortened spacer length causes a concentrated gate fringing field in the extension region, resulting in abrupt energy band profile in the channel-drain and thus tunneling width gets shortened as verified through Fig. 5 (b). This tendency varies with the spacer material and  $\Delta L_{\text{ext,G}}$ , and can be clearly observed in the extreme cases ( $\Delta L_{\text{ext,G}} = -1.5$  or 1.5 nm). In the case of  $\Delta L_{\text{ext,G}}$  of -1.5 nm, as illustrated in Fig. 6 (a), the device turns into an extremely overlap structure. In overlap case, the higher the permittivity of the spacer material, the more the gate fringing field can be dispersed through the extension region, hence reducing the maximum electric field at the drain junction [18]. This provokes the energy bands to become gentle and the tunneling width to get larger, as shown in Fig. 6 (b). When  $\Delta L_{\text{ext,G}}$  is equal to 1.5 nm, as shown in Fig. 7, the device changes into an extremely underlap structure, where more gate fringing field can be transferred to the drain junction as the permittivity of the spacer material rises, thereby augmenting the GIDL current. But this differences of the field dispersion mechanism according to

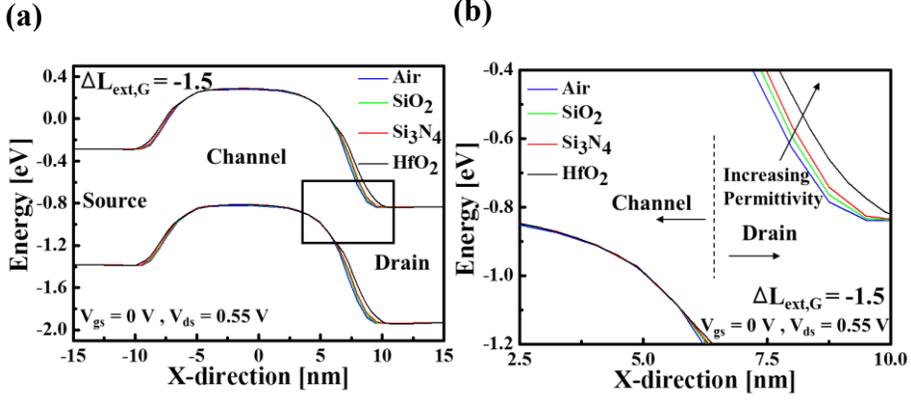


Figure 6. (a) Energy band profiles according to spacer materials for  $\Delta L_{ext,G} = -1.5 \text{ nm}$ . (b) is the black rectangle of (a)

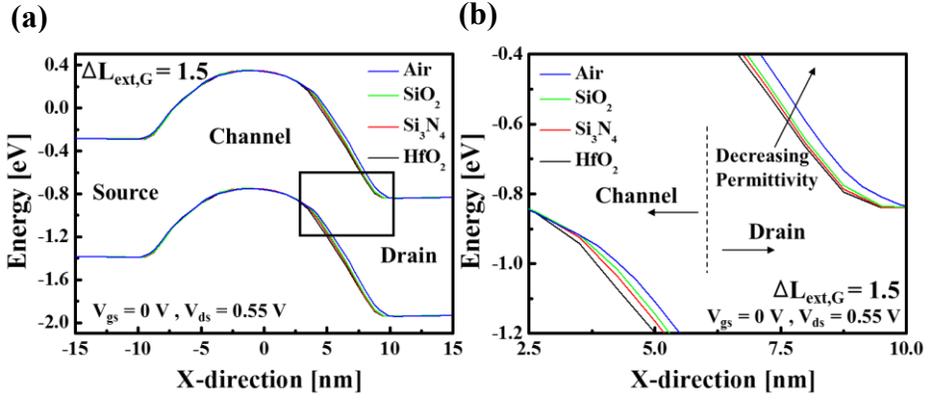


Figure 7. (a) Energy band profiles according to spacer materials for  $\Delta L_{ext,G} = 1.5 \text{ nm}$ . (b) is the black rectangle of (a)  $\Delta L_{ext,G}$  with SiO<sub>2</sub> spacer material.

the spacer material cannot be observed in the constant overlap case that the  $L_{ov}$  remains constant by adjusting the doping gradient as illustrated in Fig. 3 (b). This is the reason for the relatively small reduction rate of the GIDL current as  $\Delta L_{ext,G}$  increases. Fig. 8 and Fig. 9 represent the  $I_{on}/I_{off}$ ,  $I_{on}$ , the drain-induced barrier lowering (DIBL), and the dynamic performance, that is, the intrinsic delay, which are directly related to the physical gate length. In Fig. 8 (a), despite the decrease in  $I_{on}$ ,  $I_{on}/I_{off}$  increases by 137% as  $\Delta L_{ext,G}$  grows by 0.5 nm for each spacer material. However, the overall current reduction rate becomes smaller when the permittivity of the spacer material gets higher. This is because of the improved electrostatic

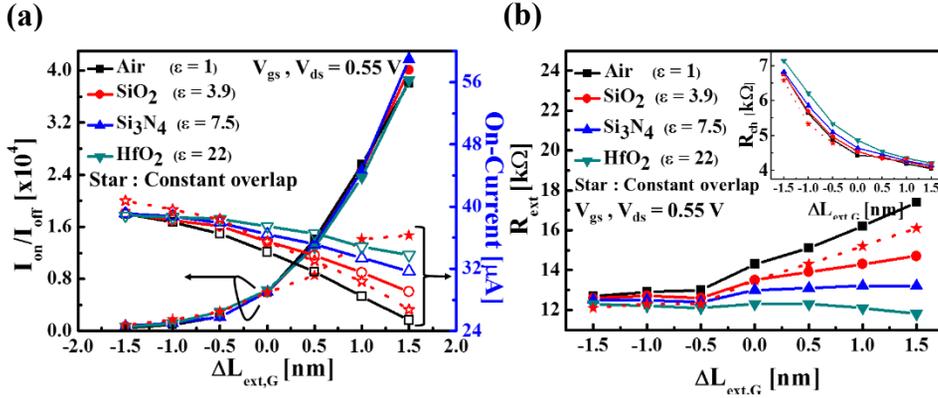


Figure 8. (a) Variation of Ion performance and parasitic resistance according to  $\Delta L_{ext,G}$ : ( $I_{on}/I_{off}$  and  $I_{on}$  with each spacer material, (b) channel resistance ( $R_{ch}$ ) and extension resistance ( $R_{ext}$ ).

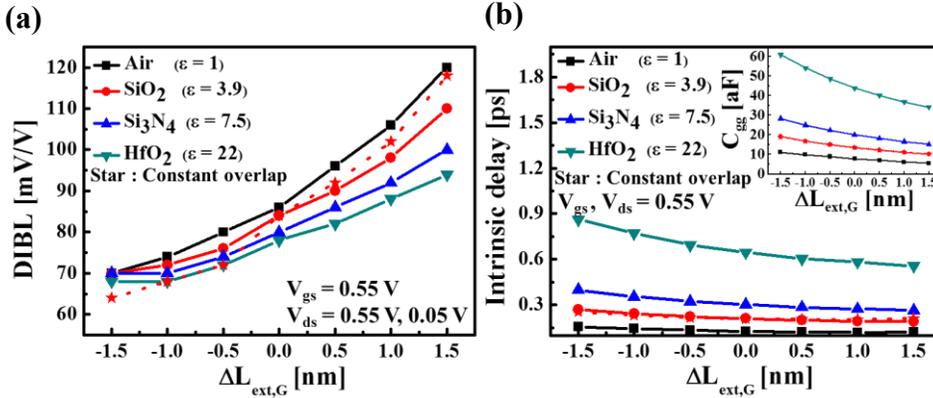


Figure 9. Variation of device characteristics with each spacer material according to  $\Delta L_{ext,G}$ : (a) DIBL (b) intrinsic delay and total capacitance.

potential in the underlap region, caused by the enhanced dispersion of gate fringing field. The above results can be verified through the analysis of the parasitic resistance as shown in the inset of Fig. 8 (b). The channel resistance,  $R_{ch}$ , decreases in all cases due to the shortened physical gate length. The higher the permittivity of the spacer material, the lower the increment rate of the extension resistance  $R_{ext}$  except for  $HfO_2$ , because the high-permittivity spacer material elevates the electrostatic potential in the extension region, causing the reduction in  $R_{ext}$ . Because of the increased  $R_{ext}$  the overall resistance gets raised, which consequently reduces  $I_{on}$ .  $I_{on}/I_{off}$  indicates similar

quantities for all the spacer materials except for the constant overlap case, representing a low  $I_{on}$  and the largest  $I_{off}$ , and is proportional to the growth of  $\Delta L_{ext,G}$  in spite of the inverse proportion of  $I_{on}$ . The reason is that the decrement rate of the off-current  $I_{off}$  is larger than that of the  $I_{on}$ . To verify the optimized point and spacer material, The DIBL and the dynamic performance are analyzed as illustrated in Fig. 9. DIBL is an important parameter for ultra-scaled devices, because it is closely related to the SCE and the device miniaturization. DIBL is significantly affected by the permittivity of a spacer material, since the gate controllability in extension region can be enhanced with a spacer material of high permittivity, which improves the DIBL characteristic. On the other hand, the DIBL tends to degrade as  $\Delta L_{ext,G}$  increases, because the shortened physical gate length weakens the gate controllability applied to the channel. Then an acceptable DIBL value (90 mV/V), which can be obtained from [28] and the data from Fig.9 (a), was represented when  $\Delta L_{ext,G}$  is below 0.5 nm for the spacer materials of SiO<sub>2</sub> and Air and  $\Delta L_{ext,G}$  is 1 nm for HfO<sub>2</sub> and Si<sub>3</sub>N<sub>4</sub>. In the perspective of the dynamic performance, the intrinsic delay was considered. The intrinsic delay was improved by 7 %, as  $\Delta L_{ext,G}$  rises by 0.5 nm, because the expanded spacer area causes the reduction of the parasitic capacitance. However, in the case of HfO<sub>2</sub>, the intrinsic delay was severely degraded by about 100~180 %, because the highest permittivity of HfO<sub>2</sub> increases the parasitic capacitance severely. Therefore, Si<sub>3</sub>N<sub>4</sub> is appropriate for a spacer material. Consequently, best performance can be obtained in  $\Delta L_{ext,G} = 0.5$  and 1 nm with the spacer material of Si<sub>3</sub>N<sub>4</sub>.

### 3.2. S/D-spacer relation

Fig. 10 shows a schematic view of the structural variation in the S/D length ( $L_{S/D}$ ) and the spacer length. In this case, the CGP varies in each variation parameter ( $\Delta L_{ext,SD}$ ), since  $L_{S/D}$  changes according to  $\Delta L_{ext,SD}$ . Nonetheless, the overall lateral length of the device was fixed, hence the device scale could be maintained, which makes the total length of the S/D and spacer constant in most cases, and the doping gradient was retained to the reference case ( $\Delta L_{ext,SD}=0$  nm) as done in gate-spacer case. The GIDL current and the band profiles according to  $\Delta L_{ext,SD}$  are illustrated in Fig. 11. Fig. 11 (a) represents the same GIDL tendency as in Fig. 5 (a). As  $\Delta L_{ext,SD}$  increases by 0.5 nm, GIDL current is reduced by 79%. This GIDL current tendency can be verified through energy band profiles illustrated in Fig. 11 (b). As  $\Delta L_{ext,SD}$  decreases, so does the spacer length, resulting in the shift of the edge of the drain's conduction band in the opposite direction of the channel's valance band and thus causing a larger tunneling width of the energy band. Fig. 12 (a) shows  $I_{on}/I_{off}$  and  $I_{on}$  according to  $\Delta L_{ext,SD}$ .  $I_{on}$  is proportional to  $\Delta L_{ext,SD}$  when  $\Delta L_{ext,SD}$  is less than 0 nm. As  $\Delta L_{ext,SD}$  becomes smaller, the effective channel length gets shortened due to the constant doping profile of the device, raising the amount of the subthreshold leakage.

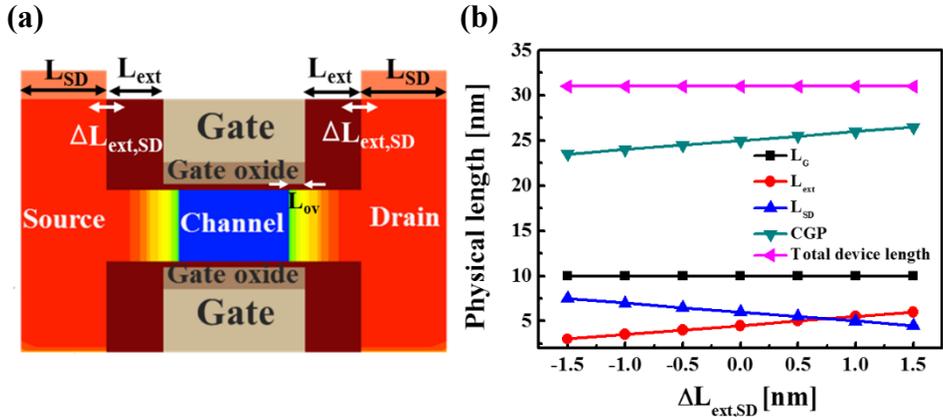


Figure 10. (a) Schematic view of length variations in S/D and spacer, (b) their specific relations.

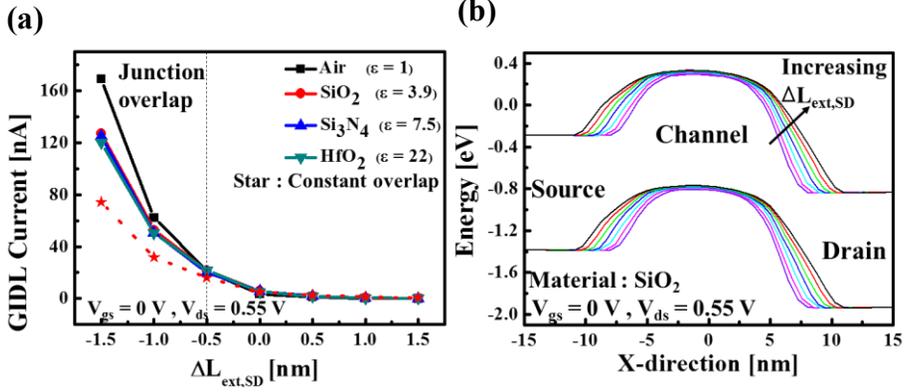


Figure 11. Simulation results of S/D-spacer relation for characteristics: (a) GIDL current according to variation of S/D and spacer,  $\Delta L_{ext,SD}$ , (b) energy band profiles for each  $\Delta L_{ext,SD}$  with  $\text{SiO}_2$  spacer material.  $\Delta L_{ext,SD}$  with  $\text{SiO}_2$  spacer material.

In order to analyze the characteristics at the same threshold voltage, during the work function (WF) tuning process, the gate WF increased further as  $\Delta L_{ext,SD}$  decreased, resulting in low  $I_{on}$ . On the contrary,  $I_{on}$  is inversely proportional to  $\Delta L_{ext,SD}$  when  $\Delta L_{ext,SD}$  is greater than 0.5 nm. This is caused by the stretched effective channel length which lowers the subthreshold leakage sufficiently and the increment of  $R_{con}$  that reduces the  $I_{on}$ . As  $\Delta L_{ext,SD}$  increases, the S/D area becomes smaller and  $R_{con}$  gets larger, as presented in Fig. 12 (b). Consequently, the most enhanced  $I_{on}$  can be obtained at  $\Delta L_{ext,SD}$  of 0.5 nm. However, it can be seen that  $I_{on}$  tends to decline in accordance with  $R_{con}$  for all the ranges of  $\Delta L_{ext,SD}$  in the constant overlap case. In the constant overlap condition, by adjusting the doping gradient as illustrated in Fig. 3 (b),  $L_{ov}$  can be kept constant. Due to the retained gate length, the effective channel length can be fixed, then resulting in a constant subthreshold leakage with varying  $\Delta L_{ext,SD}$ . Despite that  $I_{on}$  rises or falls according to  $\Delta L_{ext,SD}$ ,  $I_{on}/I_{off}$  is enhanced by 191 % as  $\Delta L_{ext,SD}$  rises by 0.5 nm, because the decrement rate the off-current is greater than the increment rate of  $I_{on}$ . Fig. 12 (c) illustrates the intrinsic delay and the total capacitance according to  $\Delta L_{ext,SD}$ . The dispersion of the gate fringing field is

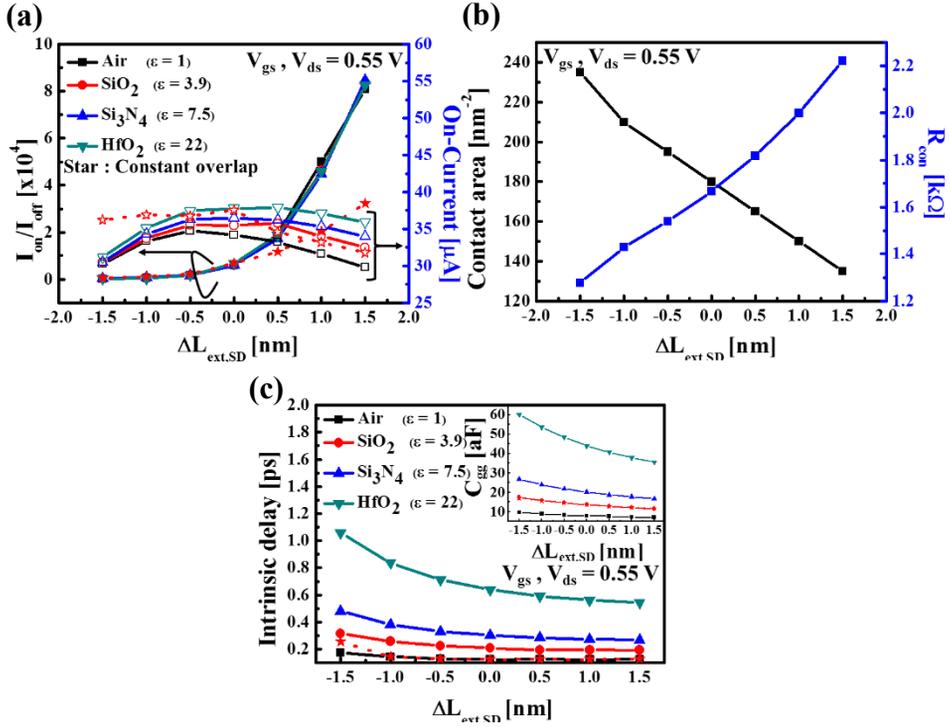


Figure 12. Variation of active performance according to  $\Delta L_{\text{ext,SD}}$ : (a)  $I_{\text{on}}$  and  $I_{\text{on}}/I_{\text{off}}$  with each spacer material, (b)  $R_{\text{con}}$  according to contact area (c) intrinsic delay and total capacitance.  $\Delta L_{\text{ext,SD}}$  with  $\text{SiO}_2$  spacer material.

enhanced in the extension region as  $\Delta L_{\text{ext,SD}}$  decreases, causing the overall capacitance becomes smaller. The higher the permittivity of the spacer material, the more the dispersion of the gate fringing field, and then the greater the decrement rate of the capacitance, resulting in the reduction of the intrinsic delay by 7.2 %, as  $\Delta L_{\text{ext,SD}}$  rises by 0.5 nm. On the other hand, in the case of  $\text{HfO}_2$ , the intrinsic delay is severely degraded by about 120 % compared with  $\text{Si}_3\text{N}_4$ . This is caused by the raised parasitic capacitance, which is the same reason as in the gate-spacer case. Then the best performance can be obtained in  $\Delta L_{\text{ext,SD}} = 0.5 \sim 1 \text{ nm}$  with  $\text{Si}_3\text{N}_4$  spacer material.

### 3.3. Comparison of structural relations

Fig. 13 shows the GIDL current and the band profiles according to the variation parameters ( $\Delta L_{ext,G}$  and  $\Delta L_{ext,SD}$ ), which indicate the best performance at 0.5 and 1 nm in the gate-spacer and the S/D-spacer case, respectively. In the both cases, the optimized dynamic performance was obtained with the spacer material of  $\text{Si}_3\text{N}_4$ , and therefore the electrical characteristics are compared based on  $\text{Si}_3\text{N}_4$ . When the variation parameter is 0.5 nm, the GIDL current in the S/D-spacer case is lower than that in the gate-spacer by about 34%, as presented in Fig. 13 (a). The reason is that the tunneling width does not change significantly in the gate-spacer case as the variation parameter increases due to the raised energy band of the channel, which can offset the energy band shifting. On the other hand, in the S/D-spacer case, the tunneling width is enlarged as the S/D length decreases. This difference of the energy band shifting mechanism, as illustrated in Fig. 13 (b), can be observed more apparently when the variation parameter is 1 nm, where the GIDL current of the S/D-spacer case is 52% lower than that of the gate-spacer. The active for the parameters of 0.5 and 1 nm, respectively. Ion is 14% higher in the S/D-spacer case. Besides,  $I_{on}/I_{off}$  is improved by about 30% at the parameter of 0.5 nm, and by about 92% at 1 nm. In the dynamic performance, there is no difference in the capacitance because of the same total spacer area, resulting in the same parasitic capacitance in the both cases. In the gate-spacer case, the improvement of the device characteristics by adjusting the variation parameter is restricted due to the performance according the variation parameter are compared in Fig. 14 (a) and (b) deterioration of the DIBL characteristic. On the contrary, in the case of the S/D-spacer, due to the fixed gate length, proper DIBL characteristics can be obtained in the all cases.

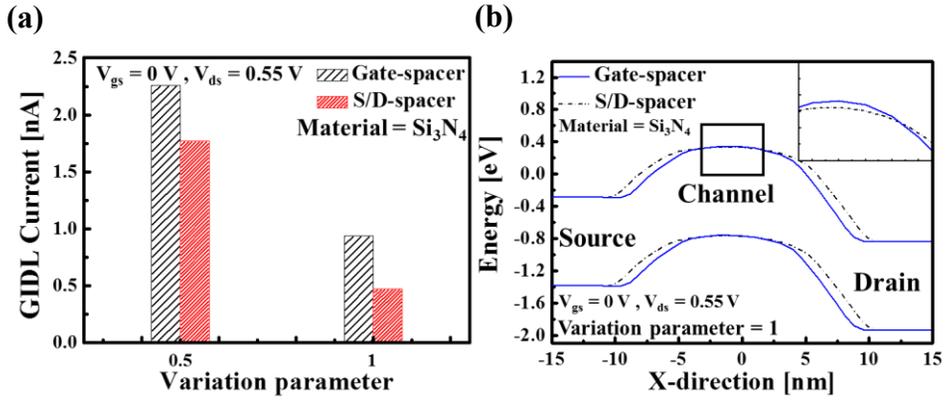


Figure 13. Comparison between gate-spacer case and S/D-spacer case: (a) GIDL current with variation parameters of 0.5 and 1 nm, (b) band profiles with variation parameter of 1 nm and inset is a black rectangle of (b).

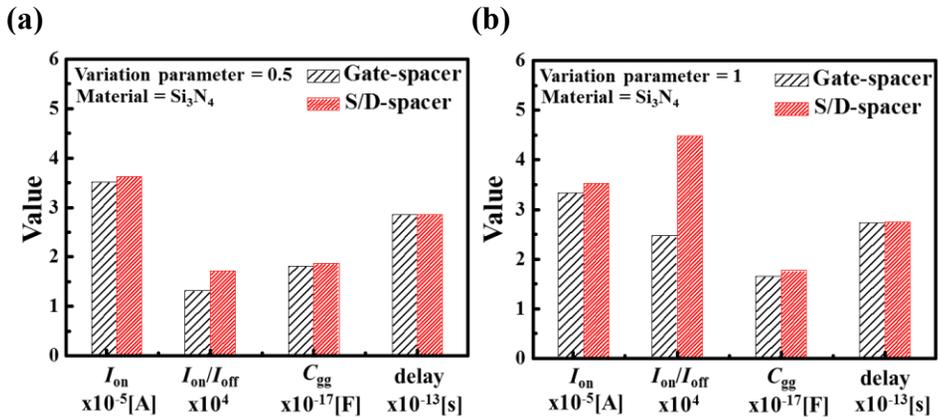


Figure 14. Comparison of active performance in each case: (a) variation parameter=0.5 nm, (b) variation parameter=1 nm.

Considering these properties, it is possible to optimize the device more effectively by utilizing the S/D-spacer case while adjusting the spacer structure.

# Chapter 4

## Asymmetric Spacer Structure

In this chapter, structural and material optimization of a 3-nm node nanoplate FET (NPFET) with asymmetric spacer was performed from a gate induced drain leakage (GIDL) viewpoint. If the spacer is designed asymmetrically, then the electrical characteristics of the device vary accordingly. The effect of the each spacer on GIDL characteristic was verified and the asymmetric spacer was optimized using asymmetric spacer ratio parameter.

### 4.1. GIDL analysis

Fig. 15 shows a schematic representation of the asymmetric spacer structure. The CGP was fixed to keep the scale of the device constant. When the CGP is maintained, the drain spacer and the source spacer are varying with opposite tendency, which cause the constant total spacer length as shown in Fig. 15 (b). Therefore, the asymmetric spacer ratio (ASR), the ratio of the drain spacer to the

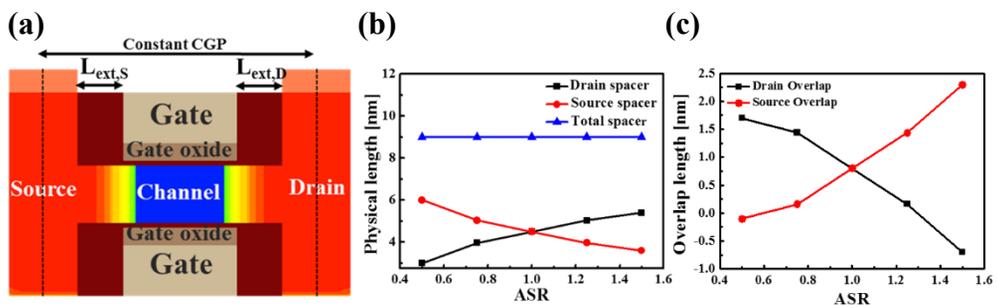


Figure 15. Schematic view of length variation of drain spacer and source spacer, (b) physical length variation of each spacer and total spacer according to the asymmetric spacer ratio (ASR) (c) overlap length according to the ASR.

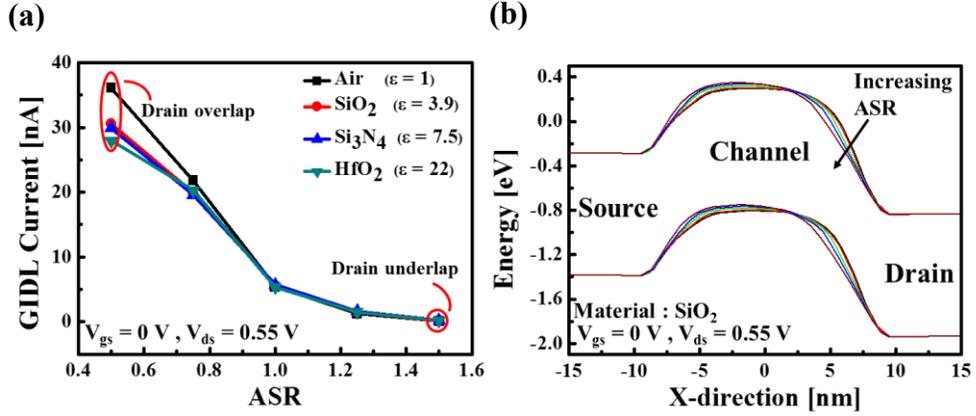


Figure 16. Simulation results asymmetric spacer for characteristics: (a) GIDL current according to variation of asymmetric spacer ratio, ASR, (b) energy band profiles for each ASR with SiO<sub>2</sub> spacer material.

source spacer, is defined as asymmetric spacer ratio ( $ASR = (L_{ext,D}) / (L_{ext,S})$ ). Assuming constant doping gradient, the overlap length of drain side and source side vary with ASR, which could affect the electric field at extension region as shown in Fig. 15 (c). Fig. 16 shows the GIDL current and band profiles based on the ASR and spacer material. As the ASR increases, the drain spacer length becomes shorter while the source spacer length is stretched. When the drain spacer is shortened, the gate-fringe field applied to the drain junction increases. As a result, the channel-drain band profile becomes abrupt, and the tunneling width becomes shorter, resulting an increase in GIDL current. The GIDL current was found to be minimized when the ASR exceeds 1.25. In case of ASR of 1.25, the GIDL current was reduced by 72% compared to the normal case ( $ASR = 1$ ) and decreased by 99.6% at ASR of 1.5. Fig. 16 (b) shows the energy band profiles according to ASR for SiO<sub>2</sub> spacer material, one of the most used spacer materials. The field dispersion characteristic vary depending on the permittivity of the spacer material. This can be clearly observed in the extreme cases ( $ASR = 0.5$  or  $1.5$ ). Fig. 17 (a) shows the electric field dispersion

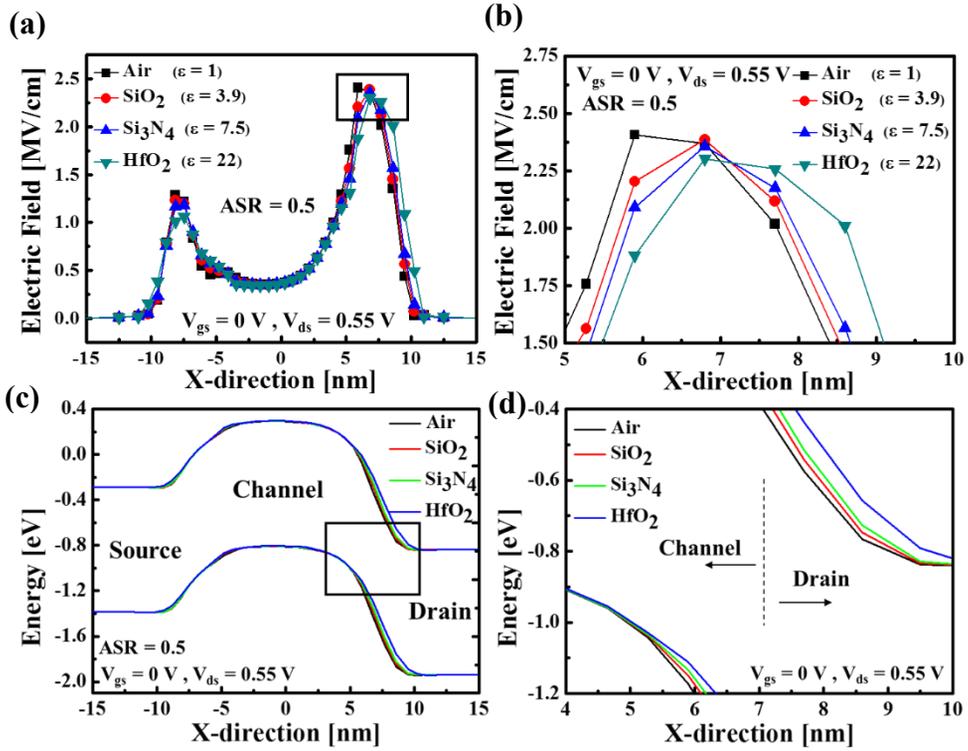


Figure 17. (a) Electric field distribution according to spacer material for ASR=0.5, (b) is a black rectangle of (a), (c) Energy band profiles according to spacer materials for ASR=0.5, (d) is the black rectangle of (c).

of the device when the ASR is 0.5, and Fig. 17 (b) is the enlarged black square of Fig. 17 (a). When the ASR is 0.5, maximum overlap length of the drain side can be formed due to the shortened drain spacer length. In the drain overlap structure, the higher the permittivity of the material, the more the gate-fringe field can be dispersed throughout the drain extension, thereby reducing the maximum electric field of the drain junction. However, the channel-drain energy band becomes abrupt as the permittivity of the spacer becomes smaller, resulting in the shortened tunneling width as illustrated in Fig. 17 (c) and Fig. 17 (d). Consequently, the GIDL current increases as the spacer permittivity decreases. Fig. 18 shows a case where the ASR is 1.5. When the ASR is 1.5, the drain extension becomes underlap as opposed to the when

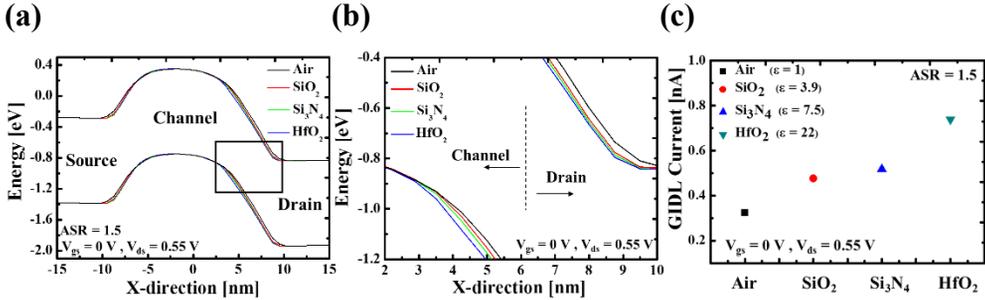


Figure 18. (a) Energy band profiles according to spacer materials for ASR=1.5. (b) is the black rectangle of (a). (c) GIDL current for ASR=1.5.

the ASR=0.5. Fig. 18 (a) shows the energy band profile when ASR is 1.5, and Fig. 18 (b) is the enlarged black square of Fig. 18 (a). Generally, concentration of the electric field from the gate to the extension region reduces in the underlap structure. However, if high permittivity material is used as a spacer material, the gate-fringe field can be transmitted to the drain junction sufficiently and the maximum electric field of the drain junction becomes larger. This makes the energy band profile of the channel-drain more abrupt, resulting a shortened tunneling width. Consequently, the larger the dielectric constant of the spacer material, the greater the GIDL current, as shown in Fig. 18 (c).

## 4.2. Active performance analysis

In order to confirm the electrical characteristics at an active region ( $V_{gs} > 0$ ), on-current, on/off current ratio, and the total capacitance ( $C_{gg}$ ), a dominant factor in the dynamic performance were analyzed. As the ASR decreases, on-current tends to decrease. This is because the larger the ASR, the shorter the source overlap length, which restricts the carrier transport due to increased conduction energy barrier of the source side. However, when the permittivity of the spacer material is high, the

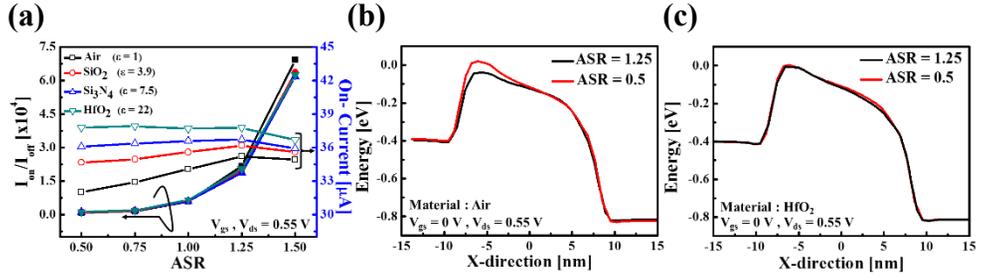


Figure 19. Variation of on-current performance and conduction band according to ASR: (a)  $I_{on}/I_{off}$  and  $I_{on}$  with each spacer material, (b) conduction band for Air as spacer material for ASR=1.25 and 0.5, (c) conduction band for HfO<sub>2</sub> as spacer material for ASR=1.25 and 0.5.

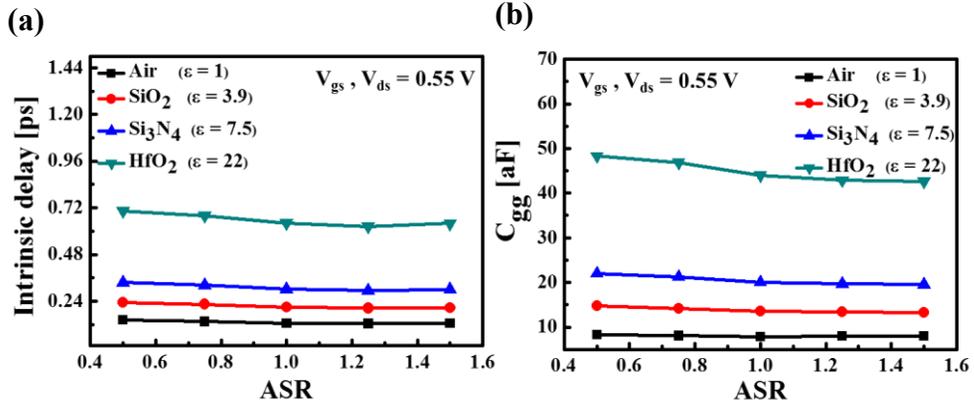


Figure 20. Variation of dynamic performance with each spacer material according to ASR: (a) intrinsic delay, (b) total capacitance.

electrostatic control of the gate to the extension region can be enhanced, which result in less effects on the source energy by the overlap length. However, when ASR is above 1.25, the channel resistance increases due to the drain underlap structure, which result in lower on-current. This is illustrated on Fig. 19 (b) and (c). As shown in Fig. 16 (a) and Fig. 19 (a), the rate of off-current decrease is larger than that of on-current with an increase in ASR, the reason for the continuously enhanced on/off current ratio despite the decrease in on-current. Therefore, the best on/off current ratio can be obtained when the ASR is 1.25 or more and the on-current damage can be minimized with the use of a high permittivity spacer material. Fig. 20 (a) shows intrinsic delay according to ASR and spacer material. The intrinsic delay is constant

while the ASR varies. This can be explained through Fig. 20 (b). Due to the fixed CGP, the total spacer area remains constant. This property result in constant fringe capacitance with varying ASR. However, in the case of HfO<sub>2</sub>, largest  $C_{gg}$ , which are caused by increased parasitic capacitance due to high permittivity, can be observed. This demonstrate an average 400% degradation of intrinsic delay. Consequently, Si<sub>3</sub>N<sub>4</sub> exhibits appropriate properties as a spacer material.

# Chapter 5

## Dual-k Spacer Structure

In this chapter, Dual-k spacer structure, suggested to enhance the current performance and dynamic performance, was investigated from gate-induced drain leakage perspective. GIDL characteristic can be severely affected by spacer material and structure. To verifying the effect of dual-k spacer on device characteristics, not only the GIDL current but also various electrical performance were analyzed according to the inner high-k spacer material.

### 5.1. Dual-k spacer characteristic

Fig. 21 shows a 3-D view and a cross sectional view of a dual-k spacer. The total spacer length ( $L_{ext}$ ) can be expressed as the sum of the inner high-k spacer length ( $L_{hk}$ ) and the outer low-k spacer length ( $L_{lk}$ ). It is known that not only the higher permittivity materials of high-k spacer enhance the on-current, subthreshold swing(S.S) and DIBL but also lower permittivity materials of low-k spacer effectively reduce the subthreshold leakage current, one of the off-state leakage

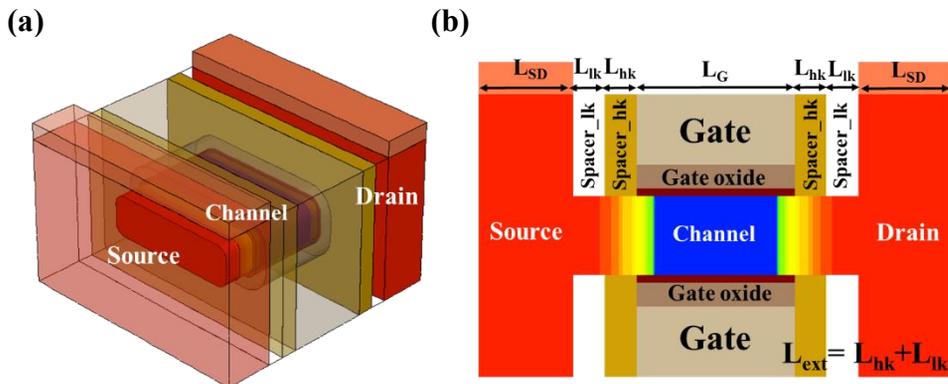


Figure 21. (a) 3-D structure of 3-nm node NPFET with dual-k spacer, (b) cross sectional view of (a).

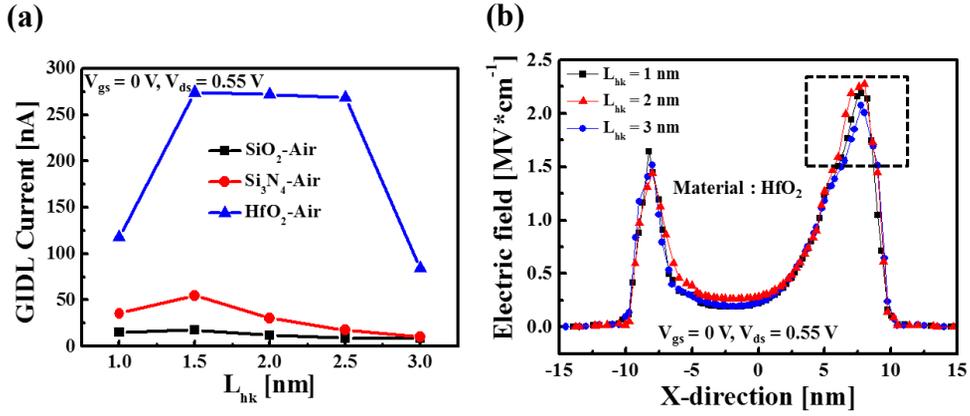


Figure 22. Variation of performance according to the inner spacer material and  $L_{hk}$  in overlap case: (a) GIDL current, (b) electric field distribution.

component [29]. However, the junction band profile (depletion region), affecting the tunneling process, is directly affected by the permittivity of the spacer. This results in a variation of the GIDL current. In dual-k spacer, due to the property of mixed spacer material, GIDL current can be more complexly influenced, which need to be verified. As can be seen in the above chapters, the larger the spacer permittivity is, the more the dispersion of the gate fringe field becomes, which result in decreased the GIDL current. In the underlap case, the larger the spacer dielectric constant, the more the gate fringe field is concentrated on the junction and the GIDL current increases. In the same way, the GIDL current is greatly influenced by the concentration and dispersion of the gate-fringe field, determined by the spacer permittivity. The dual-k spacer uses a combination of a high-k spacer and a low-k spacer and generally uses an inner high-k spacer and an outer low-k spacer as described above.

## 5.2. Overlap

Fig. 22 shows the GIDL current and electric field according to the  $L_{hk}$  and inner spacer material. In the case of overlap as shown in Fig. 22 (a), the larger the spacer dielectric constant, the greater the GIDL current. When  $L_{hk}$  is greater than 1.5, the gate-fringe field directly affects the junction band profile. Due to the partially used high-k spacer the concentration effect of gate fringe field is more than the dispersion effect, which result in increment in the GIDL current. This severely degrade the GIDL characteristic when compared to single-k spacer, which GIDL current is about 8~20 nA as can be seen in Fig. 5 and Fig. 16. There are more field dispersion effect as  $L_{hk}$  increases above 1.5 nm and GIDL current gradually decreases accordingly. After then the longer the  $L_{hk}$ , the greater the dispersion effect of the field, which result in the 52% decreased GIDL current. Since the field dependency of the spacer material becomes more clear in spacer material with high permittivity, the larger the permittivity of the spacer material, the larger the magnitude and variation of the GIDL current can be observed. Fig. 22 (b) shows the dispersion of field according to  $L_{hk}$  when the spacer material is HfO<sub>2</sub>. As described above, minimized electric field can be observed when the  $L_{hk}$  is 3 nm.

## 5.3. Underlap

Fig.23 (a) shows the GIDL current according to the material of inner spacer and  $L_{hk}$  for underlap structure. Generally, in the underlap structure, the larger the permittivity of the spacer material, the more gate fringe field can be transferred to the junction, which result in increased GIDL current. As a result of this phenomenon, the larger the permittivity of the inner spacer, the amount of gate fringe field

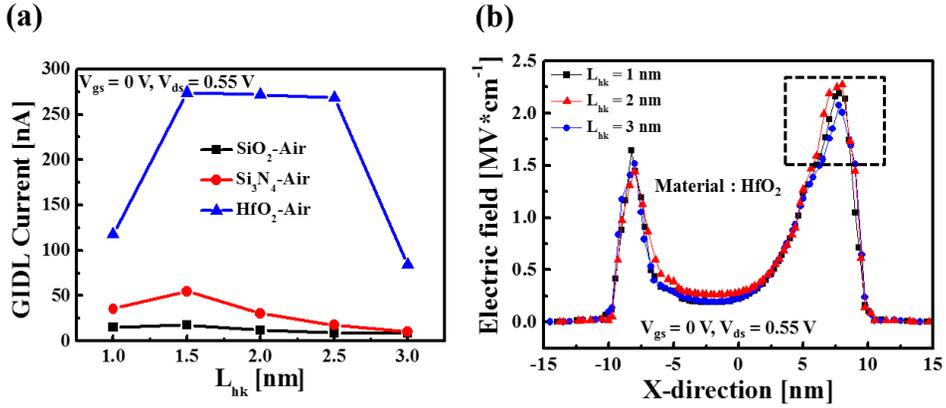


Figure 23. Variation of performance according to the inner spacer material and  $L_{hk}$  in underlap case: (a) GIDL current, (b) electric field distribution.

transferred to the junction increases, and the GIDL current gradually increases. When  $L_{hk}$  is 2.5 nm, highest GIDL current can be observed because the maximum electric field is applied to the junction. However, as  $L_{hk}$  further increases thereafter, the dispersion of the gate fringe field becomes dominant, which leads to a reduced GIDL current with  $L_{hk}$  of 3 nm. This field distribution is shown in Fig. 23 (b), and it can be seen that the largest field can be obtained when  $L_{hk}$  is 2.5 nm as described above.

#### 5.4. Active performance analysis

The dual-k spacer represents a parasitic capacitance as shown in Fig. 24 (a). Due to the complex use of spacer materials. Because of this capacitance characteristic, the total capacitance increases as  $L_{hk}$  increases. The intrinsic delay for  $L_{hk}$  and spacer materials is shown in Fig 24 (b). As  $L_{hk}$  increases, due to the enlarged area of extension length, covered with high-k spacer, the parasitic capacitance is gradually increases, which result in degradation of dynamic performance. However, because of the partially used high-k spacer, the entire parasitic component can be

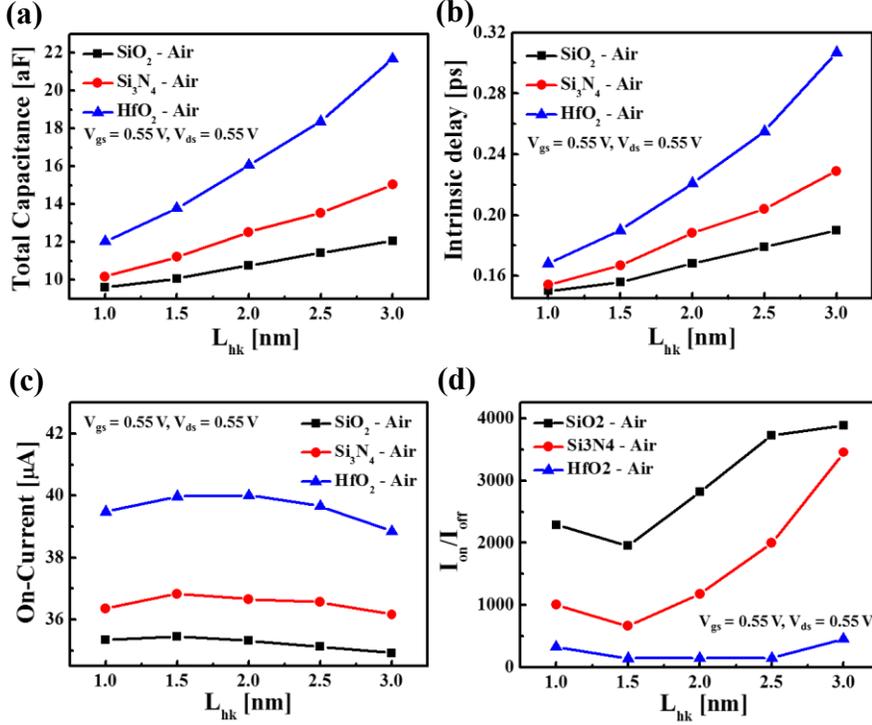


Figure 24. Variation of active performance according to inner spacer material and  $L_{hk}$  : (a) Total capacitance, (b) intrinsic delay (c) on-current (d)  $I_{on}/I_{off}$

reduced about 65 % compared to single-k spacer, shown in Fig.20, which enhance the dynamic performance. Fig. 24 (c) and 24 (d) shows the on-current and the on / off current ratio ( $I_{on}/I_{off}$ ) according to the spacer material and  $L_{hk}$ . For precise GIDL analysis, the threshold voltage was matched through the WF tuning process, which results in an overall variation of on-current within 5%. Therefore,  $I_{on}/I_{off}$  is mainly affected by GIDL current. Considering this property, the larger the permittivity of the inner spacer material, the higher the GIDL current then the largest  $I_{on}/I_{off}$  can be obtained for the spacer material  $\text{SiO}_2$ . As the  $L_{hk}$  increases more than 2 nm, the field dispersion effect becomes more dominant, and the GIDL current decreases, which causes the enhancement of  $I_{on}/I_{off}$ . Use of dual-k spacer degrades the GIDL currents over single-k spacer, which can be seen in fig. 5 and 11, in all cases, causing the

deterioration about  $I_{\text{on}}/I_{\text{off}}$  performance and static power consumption. Consequently, in the case of dual-k spacer, it is certain that this structure enhances the on-current performance and dynamic performance when compared to single-k spacer structure. However, due to the severely degraded GIDL current, the dispersion of the gate fringe field should be maximized by adjusting the  $L_{\text{hk}}$  in each inner spacer material.

# Chapter 6

## Conclusions

In this study, structural and material optimization of the gate sidewall spacer was performed from gate-induced drain leakage perspective. By adjusting the structural and material components, not only GIDL current but also active performances was enhanced in various structure.

First, the mutual variation of the structural components (gate-spacer or S/D-spacer) was analyzed. Considering the mutual length variation of the gate and the spacer, the GIDL current reduced by 51% for  $\Delta L_{\text{ext,G}}=0.5$  nm and 87% for  $\Delta L_{\text{ext,G}}=1$  nm. Due to the effectively reduced GIDL current,  $I_{\text{on}}/I_{\text{off}}$  was enhanced by up to 4.2 times with a proper DIBL characteristic. The improved  $I_{\text{on}}$  and appropriate intrinsic delay can be obtained with the  $\text{Si}_3\text{N}_4$  spacer material. For the S/D-spacer, the GIDL current reduction rate was 1.6 times larger than that of gate-spacer case because the different band shifting mechanism. The highest  $I_{\text{on}}$  and the enhanced  $I_{\text{on}}/I_{\text{off}}$  can be obtained in  $\Delta L_{\text{ext,SD}}=0.5$  and 1 nm. For the same reason as in the gate-spacer case, the  $\text{Si}_3\text{N}_4$  spacer material should be used. The GIDL current was reduced by ~52% in the S/D-spacer case compared to that in the gate-spacer case, enhancing  $I_{\text{on}}/I_{\text{off}}$  by 93% and giving better immunity to the DIBL degradation.

Second, various electrical characteristic especially GIDL current was enhanced in asymmetric spacer structure as one of the methods for improving device characteristics. The GIDL current was minimized by up to 99.6% with the use of ASR above 1.25. The GIDL current tendency according to the spacer material was analyzed in extreme cases (ASR=0.5 or 1.5). Considering active performance, the

on/off current ratio was enhanced 1.9 times for ASR of 1.25 and 4.7 times for ASR of 1.5, while the on-current degradation was minimized with the use of a high permittivity spacer material. However,  $\text{Si}_3\text{N}_4$  was found to be the most appropriate for spacer material. The reason is that its parasitic capacitance is increased about 2.4 times due to highest permittivity of  $\text{HfO}_2$ , which causes deterioration of intrinsic delay by up to 400%. Consequently, optimized electrical performances can be obtained in ASR above 1.25 with  $\text{Si}_3\text{N}_4$  spacer material.

Finally, GIDL current in dual-k space structure was analyzed according to physical length and material of the inner high-k spacer. Intrinsic delay was enhanced due to the 65% reduced parasitic capacitance and on-current boost effect can be observed when compared to single-k structure. However, due to the partially used high-k spacer, GIDL current was severely degraded. Consequently, to minimize the GIDL current, field dispersion effect should be maximized by adjusting the  $L_{\text{hk}}$  as long as possible in all cases.

Through this study, not only the GIDL characteristic but also the active performances was enhanced in various structure. Considering these properties, it is expected that the optimization method, presented in this study, can be utilized as guideline for gate sidewall spacer for the future devices.

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# 초 록

본 논문에서는 오프 상태 누설 전류의 관점에서 게이트 측벽 스페이서의 구조 및 물질 최적화를 3nm 노드 나노 플레이트 소자에서 수행했다.

첫째, 게이트 누설 전류의 주 요인 인 기들 (GIDL) 전류와 능동 성능 (온 전류, 온 / 오프 전류 비)가 게이트 측벽 스페이서와 게이트 및 소스/드레인과의 구조적 상관 관계에 따라 공동 최적화되었다. 또한, 게이트-스페이서와 소스/드레인-스페이서 사이의 구조적 관계를 비교함으로써 기들 측면에서 보다 나은 구조 최적화 방법이 제안되었다.

두 번째로, 기들 관점에서 비대칭 스페이서 구조의 최적화를 수행했다. 스페이서가 비대칭으로 설계되는 경우, 디바이스의 전기적 특성은 그에 따라 변한다. 비대칭 스페이서의 최적화를 통해 기들 전류가 72 % 감소하여 전반적인 오프 상태 누설 전류가 67 % 감소했다. 그 결과로 온 / 오프 전류 비는 4.7 배 증가했다.

마지막으로, dual-k 스페이서 구조는 high-k 스페이서 길이를 따라 다양한 재료를 사용하여 조사된다. High-k 스페이서의 유전율이 높은 재료가 온 전류를 증가시킬 뿐만 아니라 low-k 스페이서의 유전율이 낮은 재료가 오프 전류를 효과적으로 감소시키는 것으로 알려져있다. Dual-k 스페이서가 기들 전류에 미치는 영향을 검증하기 위해, 주로 dual-k 스페이서 구조에서 GIDL 특성에 영향을 주는 내부 스페이서 물질에 따라 다양한 dual-k 스페이서의 GIDL 특성을 비교했다.

본 논문에서 제안 한 게이트 측벽 스페이서의 최적화를 통해 기들 전류를 효과적으로 감소시키고 능동 성능을 향상시킬 수 있으며 이는 초 소형화 된 소자의 스페이서 설계 지침으로 활용 될 수 있다.

**주요어 :** 기들, 스페이서, 초소형 소자, 나노플레이트 소자, 스페이서 물질, 구조 최적화

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