Ph.D. DISSERTATION

Development of the HfO_2 based memristor and the TiO_2 based selector for various application

by

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Development of the HfO_2 based memristor and the TiO_2 based selector for various application

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Abstract

Neuromorphic applications of memristors are intriguing research topics in electronics. The advantage of memristor-enabled neuromorphic circuits is that the biological components in the nerve systems can be mimicked by the memristors so that the neuromorphic devices can be constructed in a much simpler manner compared to any conventional methods that mostly utilized CMOS-based circuits. Human nerve system is composed of three main parts: receptor, neuron/axon, and synapse. So, all these components must be constructed using memristors to complete the memristor-based neuromorphic circuit. While the exploration of solid-state memristors to the synapse and neuron/axon has been quite extensive, its exploration to receptor is still immature. To efficiently implement artificial intelligence (AI) and artificial receptors, development of high-density memory device should take fundamental precedence. In addition, memory products currently under development and production are expected to face limitations in improving density in the near future. For example, vertical NAND (V-NAND) flash memory, which currently occupies a large portion of non-volatile memory (NVM) product market, is expected to be developed with ~300 layers of stack in about ten years according to the NAND roadmap. Increasing the cell stack of V-NAND beyond 300 layers would not be possible for a variety of reasons. In other words, after about ten years, it would be hard to improve the memory density of current memory products, and commercialization of next-generation memory devices should be realized.

In crossbar array (CBA) format, the unit cell size of a memristor can be as small as $4F^2$, where F represents the minimum feature size. While, DRAM, NAND, and NOR flash memory have unit cell sizes of $6F^2$, $5F^2$, and $10F^2$, respectively. That is, the memristor is the most advantageous device for implementing a highly integrated memory device. Since the inception of memristor by Chua in 1971, and its experimental demonstrations in the 2000s, memristor research has been extremely active in the field of information technology. Most of the early researches focused on the memory application of the memristors and recent researches expand its horizon to other fields such as a neuromorphic computing, biocompatible memory, and wearable device.

In the first part of this study, characteristics of the nociceptor, which is the sensory neuron that responds to the threatening external stimuli, were emulated from the Pt/HfO_2/TiN memristor. The device showed four specific nociceptive behaviors; threshold, relaxation, allodynia, and hyperalgesia, according to the strength, duration, and repetition rate of the external stimuli. Such nociceptive behaviors are attributed to the electron trapping/detrapping to/from the traps in the HfO_2 layer, where the depth of trap energy level is ~0.7 eV. Also, the built-in potential by the work function mismatch between the Pt and TiN electrodes induces time-dependent relaxation of trapped electrons, providing the appropriate relaxation behavior. The relaxation time could take from several milliseconds to tens of seconds, which corresponds to the time span of the decay of biosignal. The material-wise evaluation of the electronic nociceptor in

comparison with other material, which did not show the desired functionality, Pt/Ti/HfO_2/TiN, reveals the importance of careful material design and fabrication.

In the second part of this study, Pt/TiO_2/TiN selector, where the atomic-layer-deposited TiO_2 film thickness varied from 2 to 8 nm, was fabricated using an appropriately engineered sputtered-TiN bottom electrode layer. An optimized selector with the 8nm-thick TiO_2 layer was connected serially by an external cable to the Pt/2nm-thick HfO_2/TiN bipolar resistive switching memory cell. It showed a highly feasible performance without involving the breakdown and significant switching voltage increase under no compliance current. The array writing margin (WM) was seriously limited by unwanted reset (switching from a low-resistance-state to a high-resistance-state) of the parallel connected cell to the selected cell at the moment of reset of the selected cell. This was also closely related with the presence of an interconnection wire resistance, which induced the switching voltage drop on the wire. It was confirmed by the HSPICE (simulation program with integrated circuit emphasis) simulation that ~0.5 Mb array size could be obtained by using the tungsten electrode, which is widely used in the industry, demonstrating the feasibility of commercializing the 1S1R devices.

In the third part of this study, vertical structured Pt/HfO_2/TiN memory device had been examined. In the case of the vertical structural device, the selector cannot be adopted, and the memory device should have self- rectifying or self-

nonlinear characteristics to suppress the sneak current in CBA format. When a positive voltage was applied to the Pt top electrode (TE) of Pt/HfO_2/TiN device, electrons were injected fluently from TiN to HfO_2 due to a quasi-ohmic contact formed between HfO_2 and TiN. On the other hand, when a negative voltage was applied to the Pt TE, the injection of electrons from Pt to HfO_2 was restricted, and self-rectifying characteristics were exhibited due to the Schottky contact formed between Pt and HfO_2. The two-layer vertical structured device was fabricated in a 2 x 2 array, and I-V characteristics were found to be quite similar in a total of 8 cells. In the worst scenario where only the selected cell was put into a high-resistance-state (HRS), and all the remaining cells were put into a low-resistance-state (LRS), it is confirmed that the HRS of the selected cell could be read without interrupting of the sneak current. Based on the experimentally obtained I-V graph, the allowable array size was calculated, and it was confirmed that ~0.5 Mb density could be obtained from the vertical device developed in this study when the 1/3 voltage scheme was adopted.

Keywords: neuromorphic memory, artificial receptor, resistive switching memory, memristor, nociceptor, selector, vertical structure, HfO_2, TiO_2

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device (a) and PTHT device (b). It was confirmed that the ratio of Hf:O was ~1:2.2 for the PHT device and ~1:1.8 for the PTHT device, indicating that Ti induced additional oxygen vacancies in the HfO_2. Unexpectedly, a considerable amount of oxygen was detected over the entire Ti electrode and formed TiO_x ($x < 1$) that must be due to the in-situ oxidation during the electron-beam evaporation process by the residual oxygen in the chamber. Then, the O contents at the Ti/HfO_2 interface was higher than the O in the Ti bulk, suggesting the Ti attracted the O from the HfO_2 and induced oxygen vacancies in the HfO_2. At the Pt/Ti interface, the higher O signal was detected due to the oxygen in the air. The cross-sectional transmission electron microscope image of the PHT device (c) and PTHT device (d). The crystallized HfO_2 and TiN layers were well observed in both devices. In the PTHT device, the region of the Ti TE adjacent to the Ti/HfO_2 interface appears to be amorphous, while some crystallized regions are observed at a distance from the Ti/HfO_2 interface as indicated by the blue dashed line in the Figure S5d. As mentioned above, the Ti was deposited in the form of TiO_x, so it may appear to be amorphous. Near the Ti/HfO_2 interface, the portion of O in TiO_x is relatively high due to the reaction of Ti with O in HfO_2, and most region appears to be amorphous. The portion of O in TiO_x is relatively low at locations away from the interface, and crystallized Ti was observed in several regions. These results are well consistent with the AES data of the

1. Introduction

1.1. Resistive switching Random Access Memory

Resistance switching random access memory (ReRAM), which has a two terminal device of MIM structure, is a highly appealing contender as one of the most promising next-generation non-volatile memory devices. ReRAM has some advantages compared to NAND flash memory. First, vertical NAND (V-NAND) flash memory, which is currently the mainstream of NAND flash memory market, uses polycrystalline-Si (poly-Si) channel which has a very low electron mobility of ~0.1 cm^2/Vs, while, ReRAM uses metal bit line (BL) and word line (WL) which has much faster electron mobility in operation. Second, the unit cell size of ReRAM can be as small as $4F^2$, where F represents the minimum feature size, while, NAND flash memory has a unit cell size of $5F^2$. Third, the cell stack of NAND flash memory is relatively complicated as 'metal gate (or control gate)/block oxide/trap nitride (or floating gate)/tunneling oxide/channel poly-Si', while, ReRAM cell has a simple structure of 'metal/insulator/metal'.[1,2] For the above reasons, ReRAM is attracting attention as a highly integrated memory to replace NAND flash memory. Since the resistance state of the device varies depending on the direction and amount of electric charge flow, the ReRAM is also referred to as a memristor.[3]

There are two types of ReRAM operation as unipolar and bipolar resistive switching (URS and BRS) as shown in Figure 1.1.[4] URS represents that set (switching from HRS to LRS) and reset (LRS to HRS) of the device occurs

irrespective of the polarity of the applied voltage. BRS represents that set and reset of the device occurs in the opposite polarity of the applied voltage.

Figure 1.2 shows many mechanisms for resistive switching (RS) which categorized to phase change mechanism (PCM), the thermo-chemical mechanism (TCM), valence change mechanism (VCM), electrochemical metallization(ECM), and electronic mechanism.[4] Among them, the electronic mechanism could be regarded as most feasible mechanism since it leads to the movement of electrons not ionic species while other ionic RS mechanisms generally cause the movement of ionic species during the device operation. The movement of ionic species during device operation could lead to the random generation of conducting filament (CF), which could be a major cause of poor reliability and uniformity of the electrical characteristics of the device. The electronic mechanism is usually attributed to the trapping/detrapping of electrons according to the bias polarities at trap sites in the switching layer.[4–6]

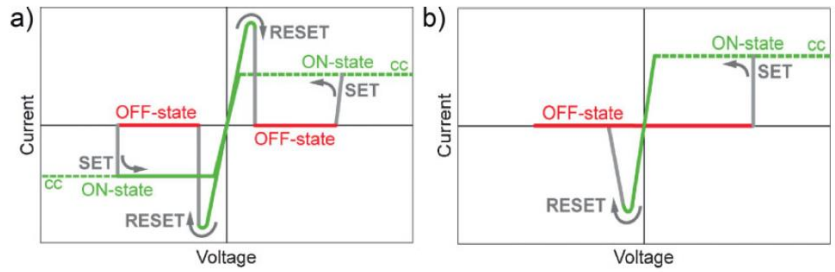

Figure 1.1 The operation schemes of ReRAM. (a) Unipolar resistive switching (URS). (b) Bipolar resistive switching (BRS). Adapted from [4].

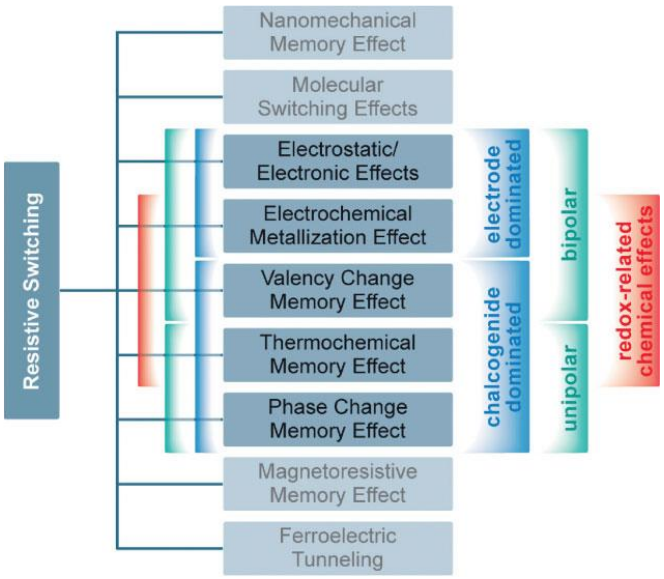

Figure 1.2 Classification of the resistive switching effects. Adapted from [4].

1.2. Technical issue in commercializing ReRAM

Although ReRAM has been actively studied for the past decade, there are some typical problems preventing its commercialization such as sneak current, overset, line resistance, etc. Sneak current is a problem caused by the passive array structure of the CBA. When attempting to read (write) a selected cell, unwanted currents flowing through the unselected cells interfere the reading (writing) operation as shown in Figure 1.3.[7] Overset is a problem in which the conducting path is excessively formed during the set operation of the device, causing a reset failure or increasing the reset voltage.[8] In addition, in a CBA structure, The source voltage (V_s) should be applied to the selected WL, and the selected BL was assumed to be grounded while reading the selected cell. The voltage drop (V_{drop}) along the WL and BL due to the finite wire resistance makes it necessary to increase the V_s to compensate for such a loss, and it is one of the limiting factors for allowable CBA density.[9] In order to solve the problems mentioned above, an appropriate selector such as a diode or nonlinear selector should be developed and adopted.[10–13] In addition, low wire resistance must be adopted, which can be achieved by using a low-resistivity metal, such as W or Cu, and increasing the wire thickness.[9,14] Especially, in the case of vertical ReRAM (V-ReRAM) that has a V-NAND like structure as shown in Figure 1.4, the line resistance problem can be exacerbated by filling the hole with metal BL. On the other hand, metal WL would be free from line resistance problem since they are formed in the form of a plane.[7]

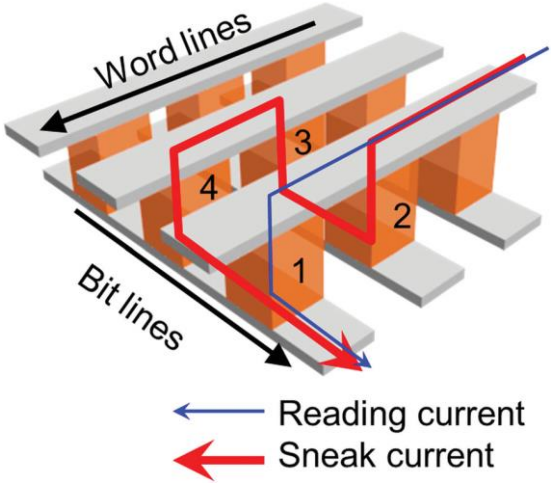

Figure 1.3 Schematic figure of sneak current problem in CBA structure. Adopted from [7].

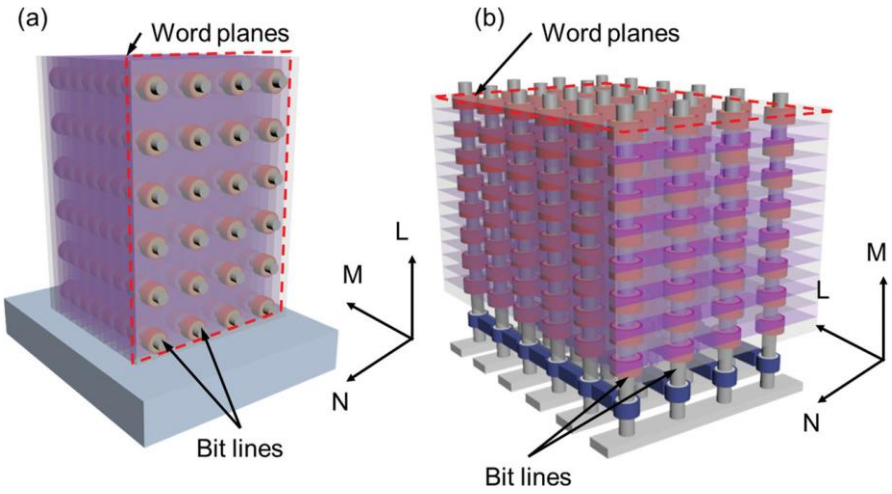

Figure 1.4 Schematic figure of the V-ReRAM. (a) vertical stacking and (b) horizontal stacking of word-planes. Adopted from [7].

1.3. Research scope and objective

One of the important research areas for the fourth industrial is humanoid, and for the development of humanoid, the development of artificial receptors needs to be carried out more actively because they are still immature. Artificial receptors and artificial intelligence also require a highly integrated memory device, and current memory products are expected to face limitations in improving integration in about ten years.

In Chapter 2, Pt/HfO_2/TiN memristor shows all the necessary behaviors as a solid-state nociceptor, which is the sensory neuron that responds to the threatening external stimuli, due to its specific trap-distribution in the band gap of the HfO_2 dielectric layer and built-in potential due to the work function mismatch between the two electrodes. The Pt/HfO_2/TiN device and Pt/Ti/HfO_2/TiN device also carefully compared the material and electrical properties to clarify the reason why the Pt/HfO_2/TiN device can show the nociceptive behavior whereas the other cannot.

In Chapter 3, based on the characteristics of HfO_2-based BRS devices, a non-linear selector based on TiO_2 was developed. Extensive optimization works of the non-linear selector were performed by changing the thickness of TiO_2 and the type of TiN electrode. After all, by increasing the asymmetry of the selector, it has been proved that the overset of the memory device can be prevented to reduce the reset (switching from LRS to HRS) voltage and improve the uniformity of the current-voltage (I-V)

curve. Based on the achieved device performance of the 1S-1R, writing and reading margin analysis were conducted using commercial simulation package, HSPICE.

In Chapter 4, The Pt/HfO_2/TiN self-rectifying memory device was implemented in a vertical structure. The two-layer vertical structured device was fabricated in a 2x2 array, and I-V characteristics were found to be quite similar in a total of 8 cells. In addition, the allowable CBA density was able to calculate based on the experimentally obtained I-V curves, in consideration of the writing margin (WM) and reading margin (RM) during device operation. From this, the possibility of commercialization of the V-ReRAM could be confirmed.

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2. Nociceptive memristor

2.1. Introduction

Since the missing memristor proposed by Chua in 1971[1] was found in 2008 by Strokuv et al.,[2] memristor research has been extremely active in the field of information technology. While most of the early researches focused on the memory application of the memristors,[3–5] recent researches expand its horizon to other fields, such as the power-saving computing, which may overcome the von Neumann bottleneck.[6] The neuromorphic computing based on hardware implementation is the critical application of the memristors in this regard. They have been utilized as synaptic devices in spike time dependent plasticity algorithm for spiking neural network,[7–10] or analogue-type weight update device for convolutional or feed forward neural network.[11] These synaptic performance has been accomplished from the analogue-like (or multi-valued) resistance switching (RS) functionality of memristors. On the other hand, they also possess the threshold switching (TS) functionality, which could provide the neuromorphic circuit with a neuristor,[12,13] which plays a role as an integrate-and-fire neuron. Such functionalities of the memristor (i.e., synaptic and neuronal), however, correspond to signal handling, transfer, and storage, but not to a generation of signals in response to external stimuli. Memristor has been adopted as a biocompatible memory element in skin-electronics[14] or wearable electronics.[15] One of the exciting future research areas of the combined activity of these neuromorphic and biomimetic (or biocompatible) studies is robotics, especially “humanoid” (a human-like robot).

One of the significant hurdles for fabricating a humanoid is installing an efficient sensory system.[16,17] The human sensory system has very characteristic features, which are quite complicated to be mimicked by the conventional sensor and data processing system based on complementary metal oxide semiconductor (CMOS) devices. The receptor is an outermost sensory nerve that responds to external stimuli and generates initial biochemical signals according to the strength, duration, and repetition of the stimuli. Among the various types of sensory receptors, a nociceptor is one of the most important and distinguishing receptors that generate pain signals to make the body avoid dangers.[18] For the nociceptor to play such role, it responds to the external stimuli in particular ways. That is, it has normal and abnormal behaviors. When the nerve cell is in the normal state, it shows “threshold” and “relaxation” behaviors, and in the abnormal state, it shows “allodynia” and “hyperalgesia” behaviors. For the threshold behavior, it does not respond to a weak stimulus lower than a threshold value, whereas it strongly responds to the stimuli exceeding the value. The nociceptor is turned off slowly for a time span, known as the relaxation period, once it is ignited by the over-the-threshold stimulus. Interestingly, during this relaxation period, the stimuli to re-ignite the nociceptor becomes lower than the threshold value because the nociceptor is partially activated, and then, it requires fewer stimuli to activate fully. Such threshold and relaxation behaviors make the body avoid from critical and continuous stimuli that called dangers.

When the nociceptor experiences much stronger stimuli as to damage it, the nociceptor falls into the abnormal state, and it responds to the stimuli as a common

receptor. The allodynia and hyperalgesia behaviors indicate the stimuli-vs-response relation in this abnormal state compared to those in the normal state; the allodynia is the behavior that generates the response signal even at the under-threshold stimuli, and the hyperalgesia is the behavior that does a stronger signal at the over-threshold stimuli than that in the normal state.[19] In other words, the nociceptor in the abnormal state has no threshold value against the external stimuli, and thus it appears to be the common receptor. Through such behaviors in the abnormal state, the body can immediately respond to and avoid from the external stimuli to protect the body from the further damage. A typical example can be found from the very sensitive response of burnt skin cell to very low heat. It can be easily anticipated that such complicated functionalities of a nociceptor can hardly be achieved from the conventional sensor and CMOS-based circuits, so it will be beneficial if these nociceptive behaviors can be achieved as a functional material system. In this way, the memristor can play the complete roles of critical information sensing/generation device as well as its more conventional information storage/processing units.

In this study, a Pt/HfO_2/TiN (PHT) memristor was fabricated to demonstrate that the aforementioned four critical functionalities of the nociceptor (i.e., threshold, relaxation, allodynia, and hyperalgesia) can be reproduced in a single electronic device. For comparison, a Pt/Ti/HfO_2/TiN (PTHT) device was also fabricated as the non-nociceptive device. The PHT device shows TS and RS behaviors depending on the electrical stimuli. A charge-trapping- and charge-detrapping-associated mechanism are proposed to explain the dual switching behaviors. Such dual switching capability in PHT device allows reproducing the four crucial nociceptive behaviors

(i.e., threshold, relaxation, allodynia, and hyperalgesia). Finally, an inverted threshold switch circuit is configured using the device that can mimic an autonomic reflex behavior in the nervous system.

2.2. Experimental

For the fabrication of the Pt/HfO_2/TiN memristor, 50-nm-thick TiN was deposited on a SiO_2/Si substrate using a sputtering system (Endura, Applied Materials). Then a 10-nm-thick HfO_2 film was deposited sequentially via atomic layer deposition (ALD), using $Hf[N(CH_3)(C_2H_5)]_4$ and O_3 as the Hf precursor and oxygen source, respectively, and using an 8-inch-diameter-scale traveling-wave-type ALD reactor (CN-1 Co. Plus 200) at a 280ºC substrate temperature. The film thickness was examined using an ellipsometer (J.A. Woollam Co., Inc., ESM-300). Then 50-nm-thick Pt top electrodes were electron-evaporated through a 120-μm-hole-diameter metal shadow mask. For the Pt/Ti/HfO_2/TiN memristor, 50-nm-thick Ti as the contact electrode followed by a 5-nm-thick Pt as the passivation layer were deposited by the electron beam evaporation without vacuum break instead of the single Pt top electrode. The depth profile of each element and cross-sectional transmission electron microscope images were analyzed using an Auger electron spectroscopy (Perkin-Elmer, PHI 660), and transmission electron microscope (JEOL, JEM-2100F), respectively. An HP4145B semiconductor parameter analyzer and an Agilent 81110A pulse generator were used for the DC and pulsed measurements, respectively. During the DC measurement, the Pt (Ti) top electrode was biased, and the TiN bottom electrode was grounded, while during the pulsed measurement the top electrode was biased, and the bottom electrode was connected to channel 2 of the oscilloscope.

2.3. Results and Discussions

First, the current-voltage (I-V) sweep responses of the PHT device with a ~11,300 μm^2 area were examined. Figure 2.1 (a) shows the I-V curves obtained from this device at 0.1 μA (left panel) and 10 μA (right panel) I_{CC} conditions, where the Pt top electrode (TE) was biased while the TiN bottom electrode (BE) was grounded. In both panels, the sweep voltage and sequence were identical, but only the I_{CC} value was different. In the first voltage sweep (curve 1, black line), the applied voltage was increased from 0 to 6 V, with the I_{CC} applied, and the device showed a drastic current increase at ~4 V. Then, a second voltage sweep was attempted (curve 2, red line), with the same conditions as the first sweep. When the I_{CC} was 0.1 μA (left panel), the second sweep overlapped with the first sweep, suggesting that the device showed the TS behavior. The subsequent sweeps in the negative bias down to -4 V showed a very low current (curves 3 and 4, green and blue lines). The subsequent curve by the positive sweep showed an identical TS behavior as curves 1 and 2 (curve 5, cyan line). When the I_{CC} was increased to 10 μA (right panel), however, the state of the device turned into the nonvolatile conductive state after the first voltage sweep, and as such, the second sweep followed curve 2 (red line), suggesting that the device showed the RS behavior. This conductive state can be reversed to the initial state through the opposite-bias application. A third and fourth (curves 3 and 4, green and blue lines) voltage sweeps were performed from 0 to -4 V, and they showed a rectifying behavior. Although the reset switching was not observed due to the rectifying characteristic, the negative sweep changed the high conductivity state to the initial resistive state.

The subsequent positive sweep confirmed it (curve 5, cyan line). Double-sweep I-V behavior of the device was shown in Figure 2.1 (b). The distinct hold voltage (~2.2 V) is observed with the 0.1 μA I_{CC} condition (left panel), indicating that it is typical TS behavior. A much lower hold voltage (~1 V) appears with the 10 μA I_{CC} condition (right panel), showing that this behavior is close to RS. Similar RS behaviors were reported by Yoon et al. from the Pt/Ta_2O_5/HfO_2/TiN (or Ti)[20,21], and by Kim et al. from the Pt/NbO_x/TiO_y/NbO_x/TiN devices,[22] whose switching mechanism was explained by the trapping-induced electronic bipolar resistance switching. Meanwhile, the PTHT device showed only the RS behavior (Figure 2.2). The dual switching behavior in PHT device compared to the RS-only PTHT device can be understood by the presence of shallow trap levels and the internal electric field by the work function difference between two electrodes. More detailed discussion is followed in the next section.

The dual switching (TS and RS) behaviors in the PHT device can be understood from the electron trapping/detrapping process with respect to the bias polarity. The trap level of this system was calculated by measuring the temperature-dependent current-decaying characteristics, which are related to the activation energy for the trapped electrons to escape from the traps (Figure 2.3). It was estimated to be ~0.7 eV below a conduction band edge that corresponds to the energy level of the charged oxygen vacancy in HfO_2.[23] The Schottky barrier height at the Pt/HfO_2 interface was obtained from the temperature dependent I-V characteristics under the negatively biased condition. The barrier height and the high-frequency dielectric constant of the

HfO_2 were estimated to ~0.9 eV and ~2.2, respectively, by the Schottky fitting in the voltage span between -6.1 V and -6.3 V (Figure 2.4). The detailed switching process can be understood by the following interpretation. The trap sites in HfO_2 are initially empty, which makes the pristine device remain in a high resistance state (HRS). When a sufficiently high positive voltage is applied to the Pt TE so that the trap level is pulled down to below the Fermi energy level of the TiN BE, the trap sites can be filled with the electrons by the electron injection from the TiN BE (Panel i in Figures 2.5 (a) and (b)). When the traps are filled the electrons, the electron transport suddenly increases due to the trap-assisted tunneling conduction between the trap sites, and as such, the device reaches a low resistance state (LRS). Here, depending on the maximum current allowed by the I_{CC}, the amount of trapping electrons are regulated. When the I_{CC} was 0.1 μA for the TS mode, the traps were only partially filled near the Pt TE, where the energy level was relatively low (Panel i in Figure 2.5 (b)). When the applied voltage was removed under this condition, the energy level of the trapped electrons near the Pt electrode moved up over the Fermi level of TiN. Meanwhile, the work function difference between the Pt and TiN electrodes induced an internal electric field even under the zero external bias condition. Then, the internal electric field induced instant detrapping of the trapped electrons from the trap sites and restored the initial HRS (Panel ii in Figure 2.5 (b)). Whereas, when the I_{CC} was 10 μA for the RS mode, all the traps in the HfO_2 layer could be filled with electrons by the sufficient supply of electrons from the BE TiN (Panel i in Figure 2.5 (c)). Then, the trapped electrons in the higher energy level compared to the Fermi level near the

Pt TE could still be emitted out from the trap sites instantly, which may result in the noisy characteristic in the I-V curve (curve 2 in the right panel in Figure 2.5 (a)). Meanwhile, the trapped electrons near the TiN BE required more time to be thermally emitted from the trap sites so that they could stay longer, which was shown as the RS (Panel ii in Figure 2.5 (c)). Although those traps could stay longer, they would decay slowly over time as shown in Figure 2.3. The electron detrapping can be accelerated by applying the negative polarity bias, which corresponds to the reset switching for recovering the HRS (Panel iii in Figure 2.5 (c)). In the case of the PTHT device, the Ti electrode takes oxygens from the HfO_2 layer, and consequently, it leads to the generation of the oxygen vacancies in the HfO_2.[24] Auger electron spectroscopy (AES) of the PHT and PTHT devices confirmed the decrease of the oxygen profile in the HfO_2 layer when the Ti was present (Figure 2.6 (a), (b)). Also, Ti electrode regions adjacent to the Ti/HfO_2 interface appears as an amorphous, which may TiO_x ($x = \sim 1$) as it takes O from the HfO_2, in the high-resolution transmission electron microscopy (HRTEM) images of the PTHT device. The portion of O in TiO_x at locations away from the Ti/HfO_2 interface was relatively low, and the crystallized Ti was observed at several regions (Figure 2.6 (d)). The trap energy level, which was obtained from the Poole-Frenkel (P-F) fitting with the temperature dependent I-V behaviors under the negative bias condition of the PTHT device, was estimated to 1.2 eV that corresponded to the deep traps (Figure 2.7). In this case, the electrons filled in the deep traps are hard to be detrapped by the thermal and electrical energies (due to similar work functions of Ti and TiN, the internal bias voltage is weak). Therefore, TS did not occur.

Such timing controllable electron trapping and detrapping process in the PHT device can replicate the nociceptor characteristics. Figure 2.8 (a) shows a schematic diagram of the typical biological nociceptor neuron.[25] Figure 2.8 (b) shows reference data from the biological nociceptor to be mimicked that was obtained experimentally from a rat's nociceptive neuron.[26] In Figure 2b, mechanical stimulation (pressure) was applied to the left knee joint (upper panel), and the response signals were recorded in the central nucleus of the amygdala of the right hemisphere (bottom panel). In this specific case, the response signal was detected only if the stimulus intensity exceeded ~70 g/mm^2, which becomes the threshold value of this nociceptor neuron. This threshold characteristic can be precisely mimicked by the PHT device. Figure 2.8 (c) shows the circuit configuration for the electrical testing of the device, where DUT stands for the device under test (PHT memristor). For this electrical test, a voltage pulse was applied using a pulse generator (PG), whose amplitude was increased from 4.5 to 8.5 V with a 1 V step, and the output current was monitored using an oscilloscope (OSC) with two channels (Ch1, Ch2). The pulse width was fixed to 6.5 ms, with a 3.5 ms pulse rising and falling time to reduce the noise signals, i.e. overshooting and charging/discharging signals. The interval between pulses was set to 6.5 ms to guarantee the full relaxation of the device after each pulse termination. Figure 2.8 (d) shows the input voltages (V_{IN}) that were monitored from Ch1 (upper panel) and the output currents (I_{OUT}) that were monitored from Ch2 (lower panel) obtained from this configuration. At the output signal, about 0.5 and -0.5 μA height humps at the onset and end of the pulse are related to the noise signals which must be disregarded. The results reproduced a similar stimulus-

response relation to that in the Figure 2.8 (b), where a ~5.5 V threshold voltage was estimated.

Other nociceptive characteristics of this device are signal relaxation and overlapping which are related to the dissipation of the response signal. Here, the signal relaxation means how the response signal decays over time after the stimulus is removed. In the nociceptor, as the response intensity is stronger, it takes the longer time until the response signal disappears completely. Such behavior can be easily understood from the common human experience; the stronger pain lasts longer. Meanwhile, signal overlapping means how the nociceptor accumulates the subsequent stimulus before the previous response signal disappears. As one can feel more pain even from a weak stimulus when it comes before the previous pain completely disappears, in the nociceptor, the signals can be overlapped, and it results in the decrease of the effective threshold value. Figure 2.9 (a) shows the signal relaxation characteristics of the device. The upper and lower panels show the input voltage stimuli and the output current responses, respectively. For these tests, two different amplitude voltage pulses (V_1 and V_2) were applied sequentially with various delay times (t_d) between the two pulses. The first pulse (V_1) was fixed to 8.5 V, which is higher than the threshold for turning on the device. The second pulse (V_2) was set to 4.5 V which is slightly below the threshold for detecting the residual response under the turned-off state. The pulse widths of V_1 and V_2 were 6.5 and 16.5 ms, respectively, with a 3.5 ms pulse rising and falling time. During the V_1 period, the output current as high as ~2.5-3.5 μA confirmed that the device was turned on. The subsequent output currents during the V_2 period showed the time-dependent

relaxation characteristic. When the t_d was 5 ms, no output current was detected as the V_2 amplitude was smaller than the threshold voltage (5.5 V). The inset of the lower panel in Figure 3a shows the magnified view of output currents during the V_2 period, showing the complete relaxation does occur at a 5 ms of t_d (magenta line). As the t_d became shorter, however, higher output currents were detected, which confirmed that the device was unrelaxed or partially relaxed during the t_d. Figure 2.9 (b) plots the output currents during the V_2 period averaged from ten measurements for each data point as a function of the delay time for the devices preprogrammed by V_1 = 6.5, 7.5, and 8.5 V. When the V_1 was 8.5 V, a higher output current was detected as the delay time became shorter, which indicates that the output signal decayed over time. Then, as the V_1 decreased, the decay time also decreased. In other words, as the stimulus is stronger, the residual response signal lasts longer. For the signal overlapping test, a fixed 8.5 V of V_1 pulse was applied, and V_2 pulses from 4.5 to 8.5 V were applied without a delay time. Note that, at these V_1 and t_d conditions, the device was turned on and was partially relaxed, as shown in Figure 2.9 (b). Figure 2.9 (c) shows the input voltages (upper panel) and output currents (lower panel), and Figure 2.9 (d) summarizes the results. In Figure 2.9 (d), the results from Figure 2.8 (d) are included to compare the effects of the residual response. The results show that an output current was detected at the V_2 amplitude as low as 4.5 V, which indicates that the threshold voltage was decreased to 4.5 V compared to 5.5 V in Figure 2.7 (d) due to the residue of the prior stimuli. The raw data for the Figure 2.9 (b) and (d) are included in Figure 2.10 and 2.11, respectively.

The next nociceptive characteristics to be confirmed were the so-called allodynia and hyperalgesia characteristics, which were explained in the introductory section. Figure 2.12 (a) schematically compares the response signals of the nociceptors in normal and damaged states, where the allodynia and hyperalgesia behaviors by under- and over-threshold stimuli in the damaged state are indicated compared to the normal state. In the PHT device, the switching transition from TS to RS can reproduce the same characteristics as allodynia and hyperalgesia. Figure 2.12 (b) compares the output current as a function of the identical voltages at the TS and RS states. The raw data are included in Figure 2.13. The RS state was excited by applying a DC positive bias to the Pt TE with a high I_{CC} condition (I_{CC} = 10 μA) before obtaining its response. It can be immediately understood that the device in RS mode corresponds to the allodynia and hyperalgesia states at the input voltages lower and higher than ~5.5 V, respectively. It is obvious that the RS mode can be recovered to the TS mode after the DUT stayed unbiased for sufficiently long time as if the allodynia and hyperalgesia are self-healed after a sufficient rest. Interestingly, the RS mode can be reversed to the TS mode by applying the reverse bias for resetting the device, which corresponds to an active treatment process of the nociceptor (Figure 2.14).

Lastly, a reflex action—one of the crucial function in the nerve system—is demonstrated through a simple circuit including the electrical nociceptor device. The reflex action is conducted as the following sequence: when a body is exposed to a noxious stimulus, the nociceptor response signal is generated and delivered to the spinal cord, and it passes the signals directly to the motor neurons for triggering effectors (muscle or gland), causing a proper reflex motion. To emulate these

functionalities, a circuit shown in Figure 2.15 (a) was composed, where the voltage signal from the PG corresponds to the external stimuli, and the DUT corresponds to the nociceptor, as before. The stimulus (i.e., the input signal) and the response (i.e., the output signal) were monitored by the Ch1 and Ch2 of OSC, respectively. If the DUT is in the turned-off state, its resistance is much higher than the internal resistance of OSC Ch2 (1 MΩ) so that almost no voltage could be seen at the Ch2 of OSC. However, if the DUT turns on, its resistance decreases to several MΩ, and then a perceptible level of current can be seen. Being different from those of the previous circuit shown in Figure 2.8 (c), a p-type enhancement-mode field effect transistor (p-FET, FQP27P06, Fairchild) was adopted, whose gate was connected to the output of DUT. At this configuration, the Ch2 of OSC shares the same node with the gate of p-FET, so the voltage monitored by the Ch2 (V_{Ch2}) corresponds to the gate voltage. This p-FET was considered to represent the spinal cord, which amplifies the output response of the nociceptor signal. It is worth noting that the p-FET stays on-state at zero gate voltage, and starts to be turned off as the gate voltage increases in the positive direction. The semiconductor parameter analyzer (SPA) provides a ~500 μA source current (at the 3 V source voltage and grounded drain), which represents a signal for making the motor neuron work at the drain node. When the stimulus was not present, as shown in Figure 2.15 (b) ($0 < t < 20$ s), the gate was open, which is a reference state representing the normal functioning of the motor neuron. When the pulse voltage with a height of 4.5 V and a duration of 20 s was applied to the DUT at $t = 20$ s, the slow and weak response signal was detected at Ch2 until $t = 40$ s because

the DUT was stimulated very weakly so stayed in the HRS, which induced a current drop to ~10 – 50 μA. When the pulse voltage application was terminated (40 s < t < 60 s), the response signal disappeared, and the p-FET went back to the reference state. When the external stimulus exceeding the threshold value (5.5 V) was applied at t = 60 s for 20 s, the DUT turned on instantly, and the stronger response signal was detected. As a result, the p-FET current decreased below ~2 μA, which corresponds to the immediate response of the nervous system to the noxious external stimulus. Afterward, the DUT went back to the normal state at 80 s as soon as the stimulus removed and the p-FET returned to the reference state. The reflex action circuit shows the feasibility of the artificial nerve device utilizing the PHT electronic nociceptive device. The wide operation time span from milliseconds to tens of seconds of the device shown in Figures 2.9 and 2.15, and well-matched relaxation time scale with the typical biological system,[27] are favorable for the biomimetic device. If the relaxation time is too fast, the body cannot respond to the short and repetitive stimuli which can also be harmful. If it is too slow, it is the receptor, no more the nociceptor. The PHT device will be suitable for the practical application in terms of the relaxation time scale.

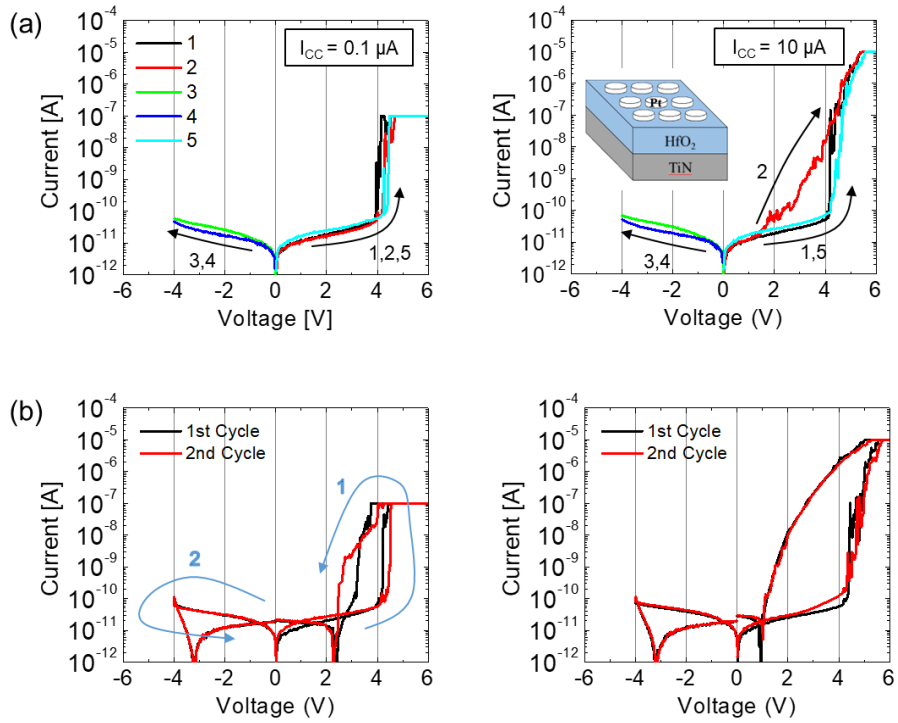

Figure 2.1 Threshold and resistance switching behaviors in the PHT device (a) Single-sweep I-V curves obtained at the 0.1 μA (left panel) and 10 μA (right panel) I_{CC} conditions. The right-panel inset schematically shows the device structure. (b) Double-sweep I-V behavior of the PHT device with the 0.1 μA I_{CC} condition (left panel) and 10 μA I_{CC} condition (right panel).

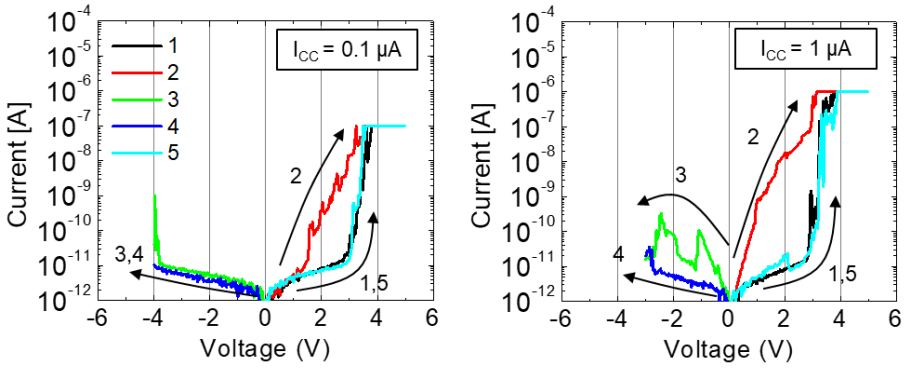

Figure 2.2 The I-V curves of the PTHT device. (a) I-V curves obtained at the 0.1 μA (left panel) and 1 μA (right panel) I_{CC} conditions. Unlike the PHT device (Figure 2.1 (a)), the RS-only behavior was shown with the low I_{CC} (I_{CC} = 0.1 μA) and high I_{CC} (I_{CC} = 1 μA).

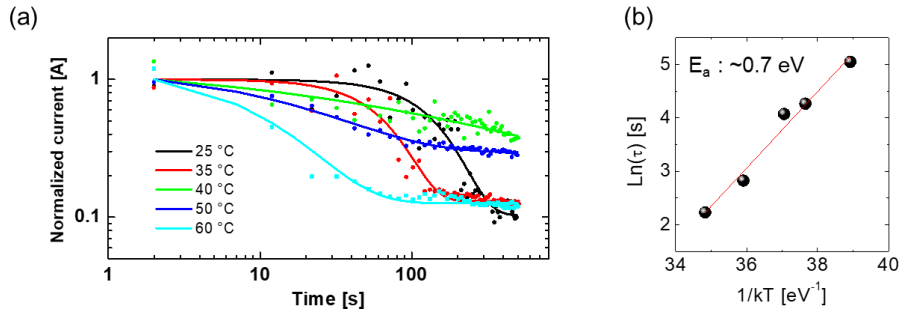

Figure 2.3 The trap level in PHT device was calculated from the time-dependent current-decaying characteristics of the trap-filled on-state at various temperatures. For this test, the current was measured at the 3 V read voltage, and the temperature was varied from 25 to 60 ℃. (a) The read currents as a function of time at various temperatures. Here, the read current was normalized to the initial current at t=0. The data shows that the read current decayed over time as the trapped electrons were being detrapped. These decaying curves were fitted with the stretched exponential function ($f_\beta(t) = Ae^{-\left(\frac{t}{\tau}\right)^\beta} + B$) to attain the time constant (τ) at each temperature. (b) The Arrhenius plot of ln(τ) vs. 1/kT showed a ~0.7 eV activation energy, which corresponds to the trap depth of the system.

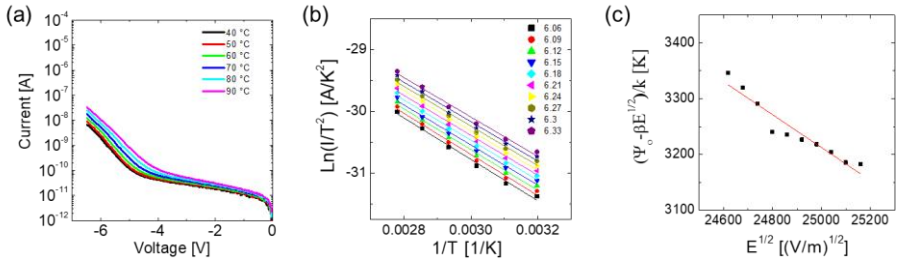

Figure 2.4 Temperature-dependant I-V curves and the fitting results to analyze conduction mechanism of the PHT device. (a) The temperature-dependant I-V curves by applying a negative bias to the Pt TE with different temperature ranging from 40 to 90 ℃. (b) The plot in the form of $Ln(I/T^2)$ vs. 1/T for Schottky fitting in the ~6.1-6.3 V range. (c) $((\Psi_0 - \beta E^{\frac{1}{2}})/k)$ value, obtained from (b), plotted as a function of $E^{1/2}$. The Schottky barrier height of the Pt/HfO_2 interface and the dielectric constant of the HfO_2 was found to be ~0.9 eV and ~2.2, respectively.

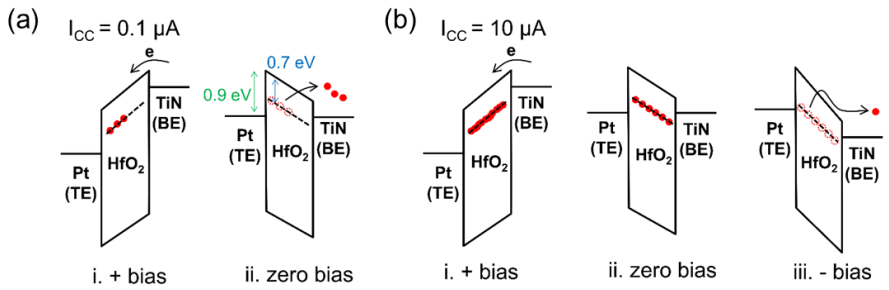

Figure 2.5 Schematic band diagram of the device (a) with a 0.1 μA I_{CC} condition and (b) with a 10 μA I_{CC} condition.

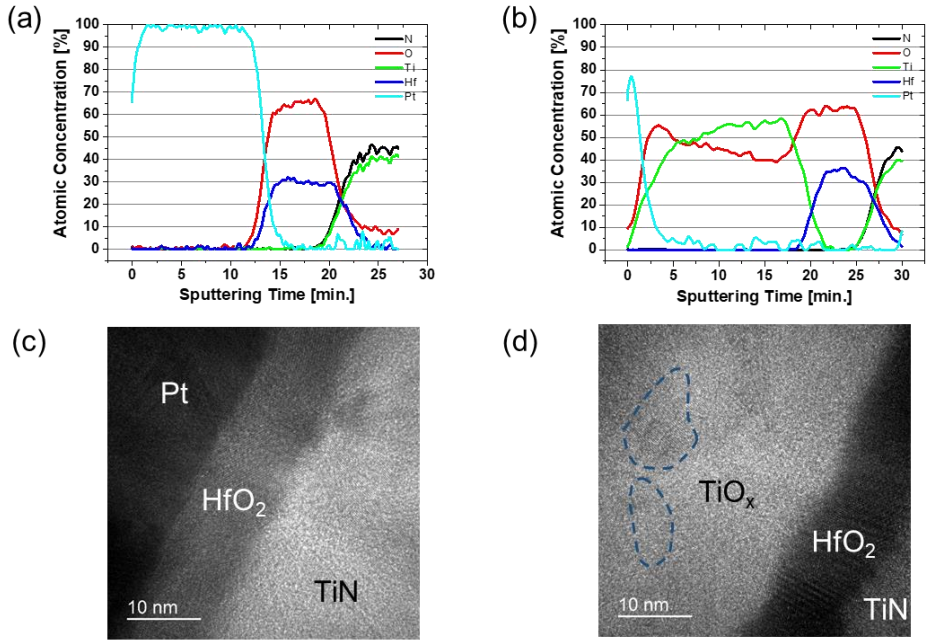

Figure 2.6 The depth profiling in Auger electron spectroscopy of the PHT device (a) and PTHT device (b). It was confirmed that the ratio of Hf:O was ~1:2.2 for the PHT device and ~1:1.8 for the PTHT device, indicating that Ti induced additional oxygen vacancies in the HfO_2. Unexpectedly, a considerable amount of oxygen was detected over the entire Ti electrode and formed TiO_x ($x < 1$) that must be due to the in-situ oxidation during the electron-beam evaporation process by the residual oxygen in the chamber. Then, the O contents at the Ti/HfO_2 interface was higher than the O in the Ti bulk, suggesting the Ti attracted the O from the HfO_2 and induced oxygen vacancies in the HfO_2. At the Pt/Ti interface, the higher O signal was detected due to the oxygen in the air. The cross-sectional transmission electron microscope image of the PHT device (c) and PTHT device (d). The crystallized HfO_2 and TiN layers were

well observed in both devices. In the PTHT device, the region of the Ti TE adjacent to the Ti/HfO_2 interface appears to be amorphous, while some crystallized regions are observed at a distance from the Ti/HfO_2 interface as indicated by the blue dashed line in the Figure S5d. As mentioned above, the Ti was deposited in the form of TiO_x, so it may appear to be amorphous. Near the Ti/HfO_2 interface, the portion of O in TiO_x is relatively high due to the reaction of Ti with O in HfO_2, and most region appears to be amorphous. The portion of O in TiO_x is relatively low at locations away from the interface, and crystallized Ti was observed in several regions. These results are well consistent with the AES data of the PTHT device.

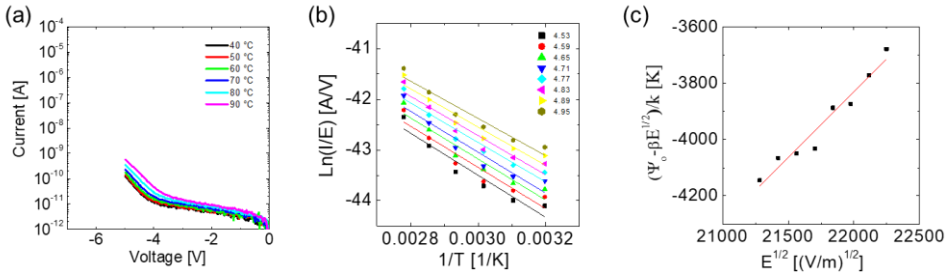

Figure 2.7 Temperature dependent I-V curve and the fitting results to analyze conduction mechanism of the PTHT device. (a) The temperature dependent I-V behavior by applying a negative bias to the Ti TE with different temperature ranging from 40 to 90 ℃. (b) The plot in the form of Ln(I/E) vs. 1/T for P-F fitting in the ~4.5-5.0 V range. (c) $((\Psi_0 - \beta E^{\frac{1}{2}})/k)$ value, obtained from (b), plotted as a function of $E^{1/2}$. The trap depth and the high-frequency dielectric constant of the HfO_2 were found to be ~1.2 eV and ~3.6, respectively. Meanwhile, Schottky fitting did not fit well (data not shown).

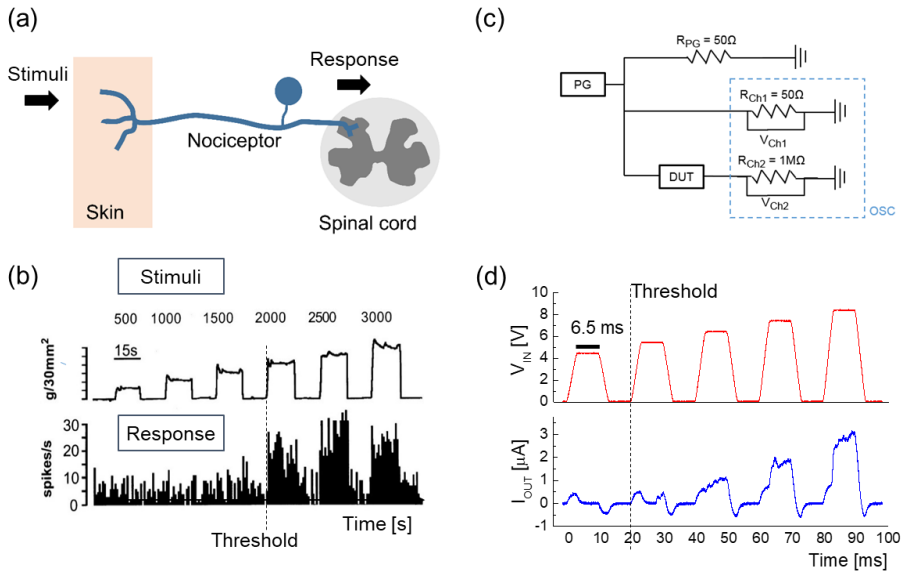

Figure 2.8 Threshold characteristic of the nervous system and the PHT device. (a) A schematic diagram of the typical nociceptor nervous system. The external stimuli are detected at the skin side end of the nociceptor, and the response signals are sent to the spinal cord (or the brain) through the opposite end of the nociceptor. (b) One of the representative stimuli vs. response results obtained experimentally from a rat's nociceptive neuron. The data was reproduced with permission from Ref. 26. (c) Circuit configuration for the electrical testing of the device. (d) Input voltages applied by the pulse generator that were monitored from Ch1 (upper panel), and output currents that were monitored from Ch2 (lower panel).

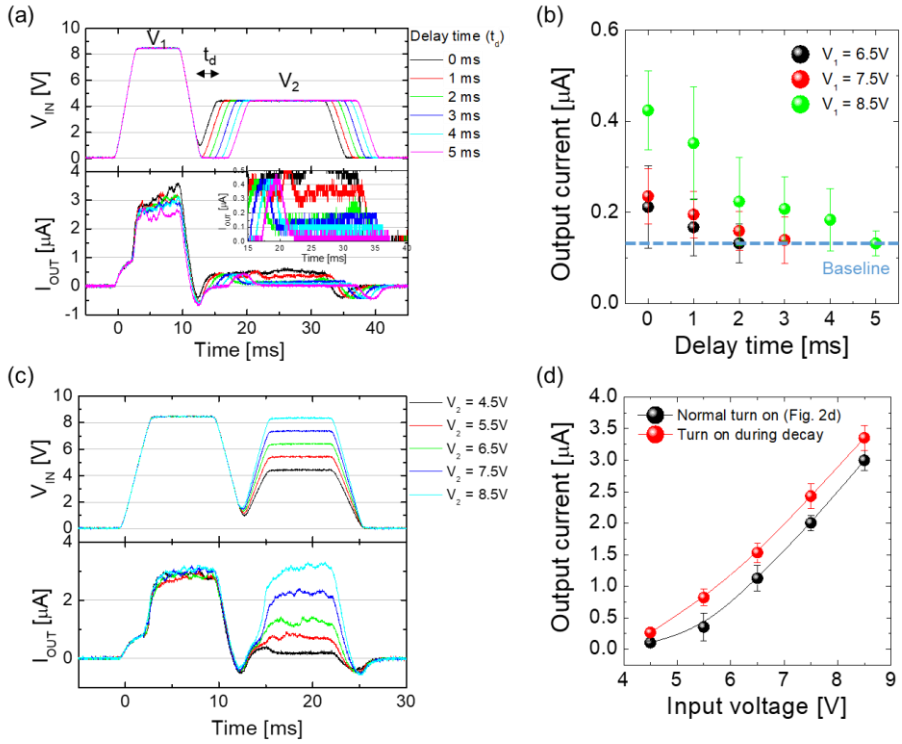

Figure 2.9 Threshold characteristic of the nervous system and the PHT device. (a) A schematic diagram of the typical nociceptor nervous system. The external stimuli are detected at the skin side end of the nociceptor, and the response signals are sent to the spinal cord (or the brain) through the opposite end of the nociceptor. (b) One of the representative stimuli vs. response results obtained experimentally from a rat's nociceptive neuron. The data was reproduced with permission from Ref. 26. (c) Circuit configuration for the electrical testing of the device. (d) Input voltages applied by the pulse generator that were monitored from Ch1 (upper panel), and output currents that were monitored from Ch2 (lower panel).

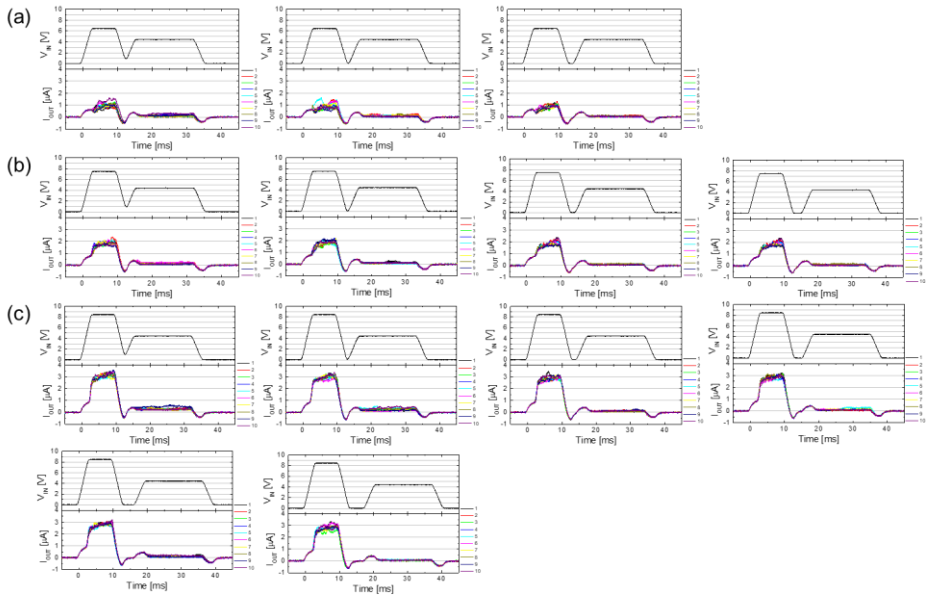

Figure 2.10 Raw data for drawing Figure 2.9 (b). (a) V_1=6.5 V; (b) V_1=7.5 V; and (c) V_1=8.5 V.

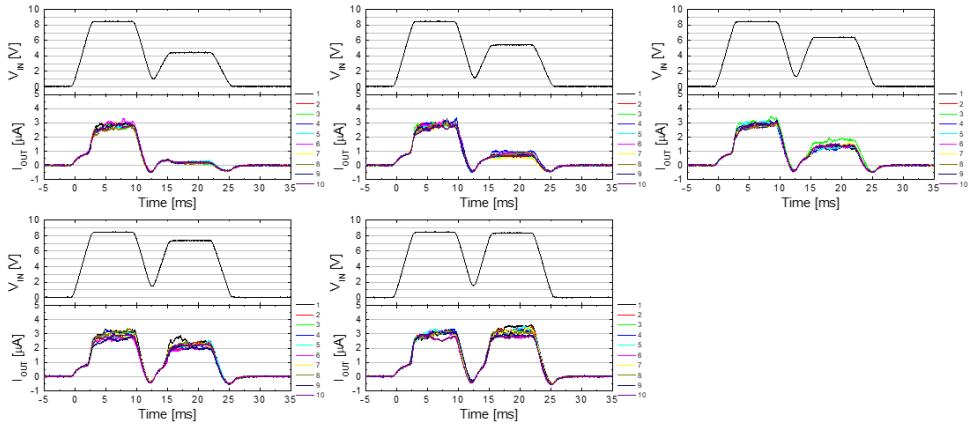

Figure 2.11 Raw data for drawing Figure 2.9 (d).

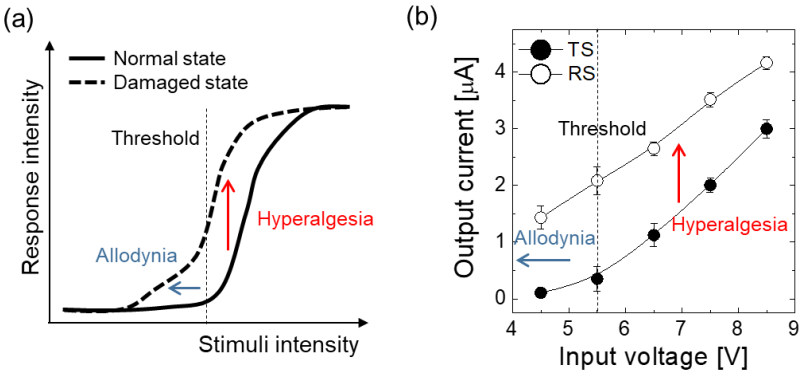

Figure 2.12 Allodynia, hyperalgesia characteristics and the reflex behavior. (a) Typical stimuli vs. response relation in the nociceptor in the normal and damaged states. (b) Output currents as a function of the identical voltages at the TS and RS modes.

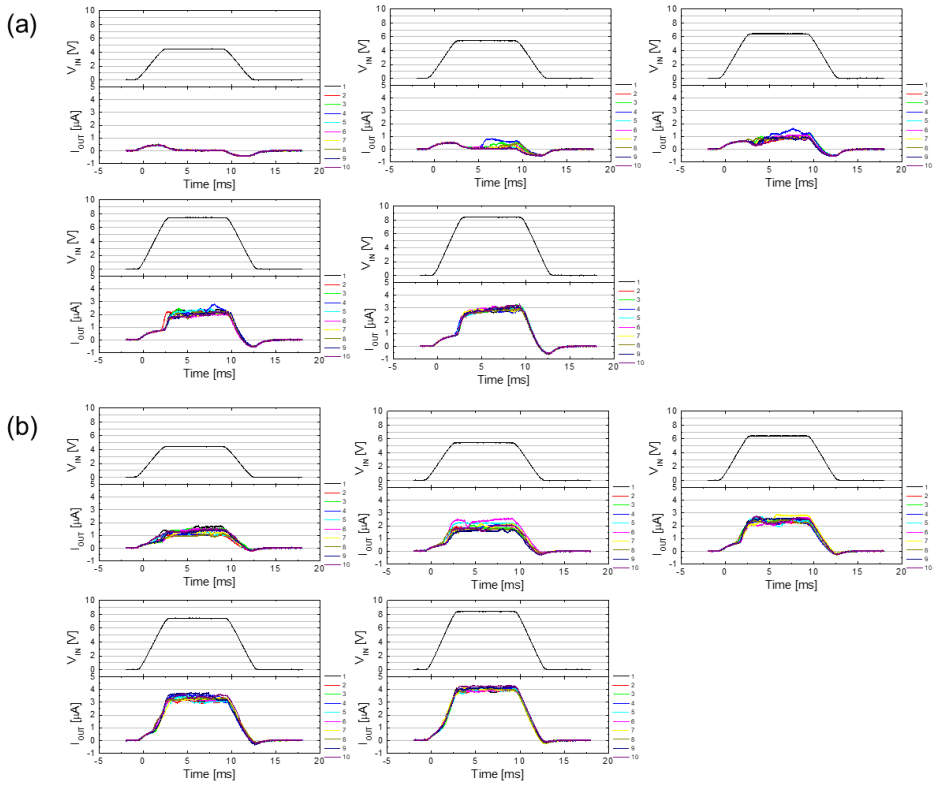

Figure 2.13 Raw data for drawing Figure 2.12 (b). Data recorded from the PHT device (a) in the TS mode and (b) in the RS mode.

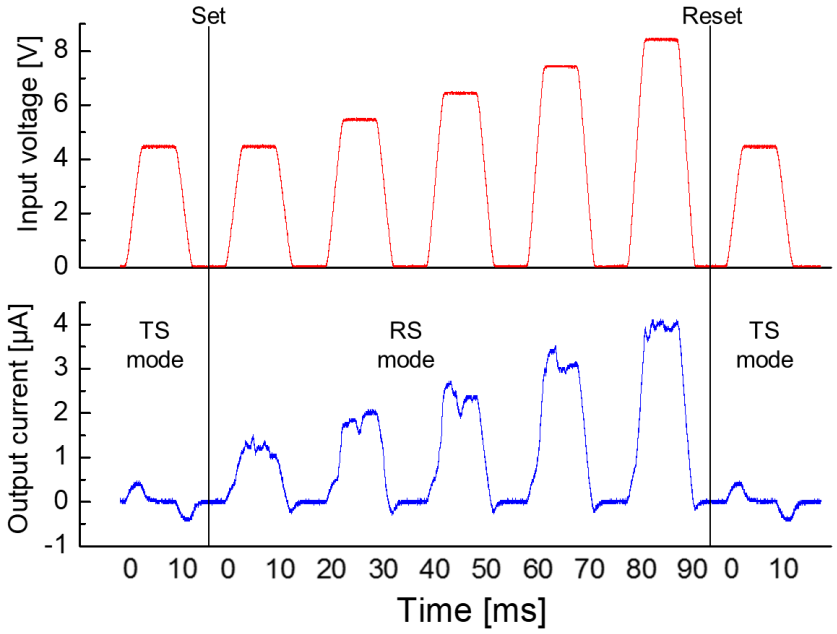

Figure 2.14 The TS and RS modes can be convertible into each other. The figure shows the input voltages (upper panel) and output currents (lower panel) while the mode changed from TS via RS to TS. From the initial TS mode, the device could be turned to the RS mode by applying a DC positive bias to the Pt TE with the 10 μA I_{CC} condition (set operation). While the device stayed in the RS mode, increased output currents were detected at the voltage range from 4.5 to 8.5 V. The increased currents are regarded as the allodynia and hyperalgesia characteristics in the damaged nociceptor in the main text. After that, the device could be returned to the TS mode by applying a -4 V of DC negative bias to the Pt TE (reset operation).

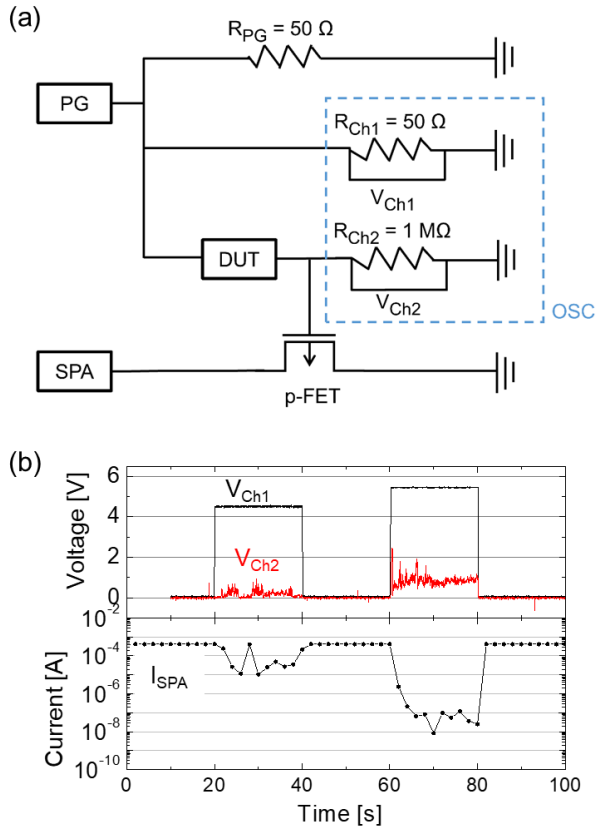

Figure 2.15 The reflex device using the nociceptive memristor. (a) Circuit configuration for demonstrating the reflex behavior. (b) Input voltages (V_{Ch1}) applied by the pulse generator, and output node voltages (V_{Ch2}) applied to the p-FET (upper panel) and currents (I_{SPA}) monitored by the semiconductor parameter analyzer (lower panel).

2.4. Summary

In summary, a solid-state nociceptor with a Pt/HfO_2/TiN memristor structure was demonstrated, which showed all the necessary functionalities of the threshold, relaxation, allodynia, and hyperalgesia of the biological nociceptor in an extremely wide time scale from several milliseconds to several tens of seconds. Such functionalities can be ascribed to the favorably distributed shallow electron trap levels within the HfO_2 switching layer, whose trap depth was estimated to be ~0.7 eV from the current relaxation time measurements at different temperatures. The appropriately formed built-in potential in Pt/HfO_2/TiN device, which forced the electrons to move out from the shallow trap levels of HfO_2 to the TiN BE at zero bias condition, induced relaxation behavior. The unrealized nociceptive behavior from Pt/Ti/HfO_2/TiN device that lacked both the appropriate traps and built-in potential confirmed the crucial key factors for the nociceptive memristor. The characteristics of the Pt/HfO_2/TiN devices shown above can be used to mimic the biological nociceptive functions of the human sensory system even in standalone or with a few transistors, which will require very complex CMOS circuits if only the standard Si technology is used.

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3. Novel selector induced current limiting effect by controlling asymmetry for high-density one selector-one resistor crossbar array

3.1. Introduction

Crossbar array (CBA) is the most feasible architecture for the resistance switching random access memory (ReRAM) in a high-density format.[1–5] Since the CBA is a passive array device, the selector is indispensable to suppress the sneak current flow.[6–10] When the ReRAM cell is of a unipolar or non-polar type, the diode is the most suitable selector as long as the forward/reverse rectification ratio and forward current density are sufficiently high.[11,12] However, if the bipolar-type ReRAM cell is adopted, the requirements for the selector become complicated because of the relative directionality (polarity-dependent characteristics) of the memory cell and selector must be considered, in addition to the necessary specifications for the selector itself. The voltage application schemes, such as floating, half-V_{cc}, etc., also have an influence on it.[4] When the bipolar resistive switching (BRS) cell turns on and off at the negative and positive bias polarities, respectively, as the Pt/HfO_2/TiN cell of this work, the serially connected selector must have following characteristics. In this study, the floating scheme, which is regarded as the most energy efficient scheme in such a passive array, was assumed.[13,14] First, the non-linearity in the reading bias polarity (positive (forward) bias) must be high enough. The forward bias current of the selector must be sufficiently high near the reset (switching from a low-resistance-state (LRS) to a high-resistance-state (HRS)) voltage compared with the reset current

of the BRS cell. Otherwise, the reset voltage increases significantly by the voltage partake effect of the selector at the moment of reset.[15,16] In the negative (reverse) bias region, the selector current must be higher than that of the HRS current of the BRS cell. Otherwise, the set (switching from HRS to LRS) voltage increases significantly by the voltage partake effect at the moment of the set, or the selector would be broken down at the excessively high set voltage. Nonetheless, the reverse current should be appropriately lower than the current compliance (I_{cc}) level of the BRS cell, which is applied to the single BRS cell to protect the memory cell from a complete breakdown when it is switched on. Under this condition, the memory cell can be feasibly operated even without the external I_{cc} circuit, which is usually a big burden to the circuit design. In the one-transistor – one-resistor (1T1R) configuration, a limited drain current by applying an appropriate gate voltage to the transistor played the role as the I_{cc}, but in such one-selector – one-resistor (1S1R) configuration, the selector itself must have all these properties, which require extensive engineering efforts.[13,14]

The authors' group have reported excellent performances for the Pt/TiO_2/Ti Schottky diode as the cell selector for the unipolar resistance switching Pt/TiO_2/Pt memory.[11] In the Pt/TiO_2/Ti Schottky diode structure, the Pt/TiO_2 and TiO_2/Ti junctions constitute the Schottky and (quasi) Ohmic junctions, respectively, showing the very high rectification ratio of as high as 10^8 and sufficiently high forward current density (~10^7 A/cm^2), when the TiO_2 film was grown by a sputtering with a thickness of ~100 nm.[11] It has been noted that the reverse current increases rapidly with the

decreasing film thickness. This implies that the similar selector might be used for the BRS memory when it is appropriately engineered. However, the sputtering technique might not be a feasible film growth method for the extremely thin films, i.e., << 10 nm, which will be an indispensable requirement for the ultra-high density integration, including the vertical ReRAM structure.[4,17,18] In this regard, atomic layer deposition (ALD) could be the most appropriate method to grow the very thin TiO_2 films. In this case, however, it was found that Ti was too reactive, so that too much oxygen was taken out from the thin TiO_2 layer.[19] Therefore, this work adopted a more stable electrode, TiN, as the quasi-Ohmic electrode, while the Schottky-type electrode, Pt, was preserved.[20] After the initial study, however, it was found that a change in the TiO_2 film thickness for the given electrode materials and growth conditions could not offer the necessary performances mentioned above. Therefore, the growth conditions for the TiN electrode were varied by using two different types of reactive sputtering systems. In this work, 50-nm-thick TiN was deposited on a SiO_2/Si substrate by using two different sputtering systems; one is a mass-production compatible tool and the other is a research scale one. The TiN film grown by the former and latter method was named A-TiN and S-TiN.

When the S-TiN electrode had a certain controlled level of surface roughness and residual oxygen concentration, the Pt/TiO_2/S-TiN selector with a TiO_2 thickness of 8 nm demonstrated a highly feasible functionality when it was connected to the Pt/2nm-HfO_2/TiN BRS memory cell through an external cable. Although this work does not

provide the data from the integrated 1S1R devices, the cable connected 1S1R revealed critical ingredients for the successful implementation of 1S1R CBA.

Furthermore, this set of data can provide fundamental information for the quantitative simulation on the achievable array size taking the reading margin (RM) and writing margin (WM) into consideration. It has been noted that the necessary selector performances for the reading and writing processes are different, making the worst aspect of the performance by the imperfection of the 1S governs overall achievable array size.[21] In this work, it was demonstrated that the optimized asymmetric selector could extend the array size to over 10^5 cells in regards to the RM. However, it was only ~3 x 10^3 cells when the WM was considered. This was mainly attributed to the involvement of the abnormally high interconnection wire resistance of the Pt and TiN, which were deposited by the research scale systems. The tungsten (W) electrodes are widely used in the semiconductor industry and 3D cross-point (3D X-point) products developed by Intel and Micron. It was demonstrated by HSPICE (simulation program with integrated circuit emphasis) simulation that ~0.5 Mb of the CBA density could be obtained if the W electrodes were used for the 1S1R devices developed in this study.

3.2. Experimental

For the fabrication of the Pt/TiO_2/TiN selector, 50 nm thick TiN was deposited on a SiO_2/Si substrate by using two different sputtering systems; one is a mass-production compatible tool (Endura, Applied Materials) and the other is a research

scale one (SRN120, SORONA). The TiN films were patterned by photolithography followed by a photoresist lift-off process as the BE. For the TiN film deposited using an Applied Materials sputtering system (A-TiN), Ti target, with a diameter of 12 inches, was used with 15 standard cubic centimeter per minutes (sccm) of Ar gas and 85 sccm of N_2 gas. The DC power and the substrate temperature were set to 5000 W and 200 ℃. The base and operating pressure were ~10^{-8} torr and 4 mtorr, respectively. For the TiN deposited using a SORONA sputtering system (S-TiN), Ti target with a diameter of 4 inches was used with 20 sccm of Ar gas and 3 sccm of N_2 gas. The RF power and substrate temperature were set to 500 W and room temperature. The base and operating pressure were ~10^{-7} torr and 1 mtorr, respectively. The A-TiN film was also used as the BE of the BRS memory cell adopting the HfO_2 film. For the BRS memory cell fabrication, 2-nm-thick HfO_2 films were deposited through an ALD using $Hf[N(CH_3)(C_2H_5)]_4$ and O_3 as the Hf-precursor and oxygen source, respectively, at a substrate temperature of 230 ℃. The 2-, 4- and 6-nm-thick TiO_2 films were deposited on the A-TiN BE through another ALD using $Ti(OC_3H_7)_4$ and O_3 as the Ti-precursor and oxygen source, respectively, at a substrate temperature of 250 ℃. 6- and 8-nm-thick TiO_2 films were deposited on the S-TiN BE using an identical ALD process. The thinner TiO_2 films on the S-TiN were too leaky to be tested. Then, 50 nm thick Pt top electrode (TE) was deposited by the e-beam evaporator (Maestech, ZZS550-2/D) and patterned by photolithography followed by photoresist lift-off process for the crossbar structure. The width of BE and TE was 6 μm, so that the areas of the selector and BRS memory cell were 36 μm^2. SEM (Hitachi, S-4800) and

AFM (JEOL, JSPM 5200) were used to observe the morphology of the A-TiN and S-TiN BE surfaces. The cross-sectional transmission electron microscope images of the Pt/TiO_2/S-TiN sample were observed through the use of a HRTEM (JEOL, JEM-2100F). The depth profiles of the two types of TiN film were estimated by AES (ULVAC-PHI, PHI-700). The I-V characteristics were measured using an HP4145B semiconductor parameter analyzer. During the measurement, the Pt TE was biased and TiN BE grounded.

A CBA simulation was performed using the HSPICE tool based on the I-V characteristics of the optimized 1S1R device. The interconnection wire resistances used in the HSPICE simulation were split based on experimentally derived values, and the values of W wire typically used in the industry as electrodes. The experimental values were estimated from the test pattern with a constant length but variable width. Detailed information for the wire resistance estimation is available in Figure 3.9.

3.3. Results and Discussions

Figure 3.1 (a) and (b) show the Auger electron spectroscopy (AES) depth profile results of the A-TiN and S-TiN films. Both films had uniform Ti and N profiles along the depth direction with oxygen impurities near the surface due to exposure to air before the AES analysis. The oxygen concentration in the S-TiN was almost doubly higher than that in the A-TiN, which could be understood from the higher based pressure of the sputtering chamber (~10^{-7} vs. ~10^{-8} torr) and lower growth rate (~2 Å/s vs. ~12 Å/s).[19] (See experimental section for details.) The resistivity of the S-TiN was also higher than that of the A-TiN (~290 μΩcm vs. ~220 μΩcm). However, both are useful as the bottom electrode (BE) layer. The atomic force microscopy (AFM) topographic image shown in Figure 3.1 (c) and (d) revealed that the S-TiN has a rougher surface morphology than that of A-TiN (0.51 nm vs. 0.29 nm of root-mean-square roughness), which appeared to have a close relationship with the current-voltage (I-V) characteristics of the TiO_2 film selector, as will be shown later. The scanning electron microscopy (SEM) images shown in Figure 3.2 corroborate the AFM analysis results. Figure 3.3 shows the cross-section high-resolution transmission electron microscopy (HRTEM) image of the Pt/8nm-TiO_2/S-TiN sample. The interface between the TiO_2 and S-TiN appears rather rough, which could be induced by the initial roughness of the S-TiN film and possible chemical interaction to form the TiON during the ALD of TiO_2. The TiO_2 film was partly crystallized.

Figure 3.4 (a) shows the typical BRS I-V switching characteristics of the Pt/2nm-HfO_2/A-TiN memory cell. The BRS sweep showed typical set and reset voltages of ~-2.5 – -3.0 V and ~+2.0 V, respectively, when the I_{cc} of 50 μA was applied. Figure 3.4 (b) summarizes the representative I-V curves of the Pt/TiO_2/TiN selectors with different TiO_2 thickness and TiN BE types. The selectors did not show any breakdown up to a +4 V and very abrupt current variation with voltage in the positive bias region up to ~1 V for the A-TiN BE (~10^7 A/V) and S-TiN BE (~10^5 A/V) suggesting a high potential as a non-linear selector. The TiO_2 film on the S-TiN showed a higher leakage current at the lower positive V region (< 0.8 V) compared with the A-TiN case, which could be due to the higher roughness of the former than the latter.

Interestingly, the current in the positive bias region showed minimal change with TiO_2 thickness variation and types of TiN BE. This finding suggests that the TiO_2/TiN interface forms a quasi-Ohmic junction, and the electron injection from the TiN BE to TiO_2 layer was quite fluent. This is supported by the conduction mechanism analysis shown below. In contrast, the current in the negative bias region showed a significant dependency on the TiO_2 film thickness and types of TiN BE. Generally, the films on A-TiN showed a much lower current, as can be directly identified by the comparison of data from the common 6 nm-thickness TiO_2 cases (green line and dash), which could also be understood from the roughness comparison of the two TiN BE types. The 2, 4 and 6 nm-thick films on the A-TiN showed the hard breakdown at approximately -2, -3 and -4 V, respectively. The 6 and 8 nm-thick films on the S-TiN did not show such a hard breakdown down to -5 V. Interestingly, the leakage current

of the 6 nm-thick TiO_2 film on the A-TiN was almost identical to that of the 8 nm-thick film on the S-TiN. However, the non-involvement of the hard breakdown in the latter case makes it more useful for the selector application as shown below. The asymmetry of the I-V curve with respect to the bias polarity further enhanced their usefulness as the selector, whereas the thinner films showed more symmetric I-V curves. From the data in Figure 3.4, it can be anticipated that the Pt/8nm-TiO_2/S-TiN would be the best selector for the given HfO_2 memory cell.

Figure 3.5 (a) on the left panel shows the I-V curve of the Pt/8nm-TiO_2/S-TiN selector measured at temperatures ranging from 30 to 80 ^oC to understand the current conduction mechanism. In the positive bias region, the I-V curve showed a significant temperature dependency, suggesting a thermally-activated current conduction mechanism. Therefore, the temperature-dependent I-V curves were fitted with the Schottky emission and Poole-Frenkel (P-F) emission mechanisms[22,23]. It was found that P-F mechanism displayed the best matching result with the experiment as shown in the middle panel of Figure 3.5 (a). The extracted trap depth was ~1.2 eV and the optical dielectric constant (ε_r) was ~4.6. This was a reasonable value considering the optical refractive index ($\varepsilon_r \sim n^2$, where n is the refractive index ~2.0 – 2.2 of the ALD TiO_2 film).[24,25] The P-F fitting was also successful in other selectors, whose summary (trap depth and ε_r) were included in table I, and raw data in Figure 3.6. In contrast, the current in the negative bias region, especially V = ~-1 V showed almost no temperature dependency, suggesting that a tunneling mechanism works. Replotting the data according to the Fowler-Nordheim (F-N) tunneling

formalism showed a qualitative coincidence (right panel of Figure 3.5 (a)) with the model.[23,26] A schematic diagram showing the current conduction mechanism under the positive and negative bias conditions can be drawn as shown in Figure 3.5 (b), where the F-N tunneling had a higher TiO_2 film thickness-dependent current conduction property than the P-F conduction.

Figure 3.7 (a) showed the switching I-V curve of the Pt/HfO_2/A-TiN memory cell without applying an I_{cc} during the set at ~-3 V (black line). Although the first subsequent reset could be achieved at approximately +5 V, the second set – reset cycles (red line) revealed that reset could not be achieved even after only two switching cycles, due to the too strongly formed current path(s). Figure 3.7 (b) showed the switching I-V of the cable connected 1S1R where the 1S was Pt/4nm-TiO_2/A-TiN, whose I-V is given in Figure 3.4 (b) (red line), and the 1R was the same Pt/HfO_2/A-TiN with no I_{cc} application. Due to the presence of the 1S, the current increased to approximately 2 x 10^{-4} A after the first set at ~-4.2V (black line), whereas it would be 10^{-3} A if there was no 1S adopted (Figure 3.6 (a)). The LRS also showed quite a high non-linearity in the negative bias region during the subsequent sweep (red line). However, the device showed a sudden current increase at approximately -4.5 V (indicated by a circle), which indicated that the 1S was broken down at this voltage. This is consistent with the behavior of the specific selector in Figure 3.4 (b). The break down could be identified from the very abrupt increase in the current from the beginning during the third sweep into the positive bias direction (green line). The fourth sweep into the positive bias region (blue line) indicated that the Pt/HfO_2/A-TiN could be still reset during the previous reset sweep (green line) although the

selector was broken down. Therefore, this selector could not be adopted. Figure 3.6 (c) showed the 1S1R results with the Pt/6nm-TiO_2/S-TiN selector without applying any I_{cc}. The connected structure could be switched repeatedly as shown by the 15 times overlapped switching I-V curves. However, the performance was not optimal. While the selector limited the current at the moment of the set at ~-2.5 V, which is similar to that of the single Pt/HfO_2/A-TiN memory, the current limiting effect was not sufficient, and the formed conduction channel was too strong. Therefore, the subsequent reset voltage was increased to > ~5 V. Moreover, the limited nonlinearity in the positive voltage region resulted in a relatively low selectivity at half of the read voltage (V_r). Figure 3.6 (d) showed the variation in the nonlinearity ((I_{LRS} at V_r)/(I_{LRS} at V_r/2)) and Forward/Reverse (F/R) ratio ((I_{LRS} at V_r)/(I_{LRS} at -V_r)) of the LRS as a function of V_r in the positive bias region, where I_{LRS} means the current at LRS. The maximum value for the nonlinearity and F/R ratio were only ~80 at a V_r of ~0.7 V and ~14 at a V_r of ~0.6 V, respectively. When the selector was changed to Pt/8nm-TiO_2/S-TiN, which showed a rather high asymmetry in its I-V curve (Figure 3.4 (b), blue dashed line), the connected 1S1R structure showed the most promising results as clearly shown in Figure 3.6 (e). Due to the limited maximum current in the negative bias region of the selector, the formed conducting channel was not too strong, and the subsequent reset voltage was almost identical to that of the 1R device (~2.5 V). In addition, the high nonlinearity and F/R ratio could be confirmed as shown in Figure 3.6 (f). The maximum value of the nonlinearity and F/R ratio were ~270 and ~10810, respectively, at a V_r of ~0.9 V. This could be ascribed to the asymmetric I-V behavior and smaller leakage current at low positive voltage region, as compared to the case

of Figure 3.6 (c). The switching uniformity was also improved as shown by the almost precisely overlapped 15 cycles of the I-V curves in Figure 3.6 (e). Similar improvement in the switching uniformity and reliability by adopting a series resistor has been reported elsewhere.[15,16] The only slight problem was the decreased (absolutely increased) set voltage to ~-3.5 V due to the voltage partake effect of the selector. However, the improvements in other aspects can overcompensate the weakness of the selector device.

Next, the estimation of the available CBA size was attempted using the data given in Figure 3.6 (c) and (e), and the estimated interconnection wire resistance whose width and length were identical to the cell dimension (6 μm). For the given resistivity (ρ) of the interconnection wire (~220 and ~11 μΩcm for the A-TiN and Pt), it should be noted that this cell-to-cell wire resistance (R_{cc}) is independent of the device design rule of the feature size (F), which corresponds to the memory cell size for the given technology node because $R_{cc} = \rho(2F/tF)$, where *t* is the film thickness.[21] As it can be seen below, the R_{cc} is one of the most critical factors that ultimately limit the available array size. Therefore, the lower R_{cc} must be adopted, which can be achieved by using a low-resistivity metal, such as W or Cu, and increasing the wire thickness.

Figure 3.8 (a) shows the schematic figure of the CBA (left panel) and calculated RM as a function of the total number of bits in a given CBA block (right panel) of the 1S1R CBA, where the 1S and 1R are assumed to be stacked. Here, RM was defined as $\frac{I_{REF}-I_{HRS}}{I_{REF}-I_{HRS,0}}$, where I_{REF} is defined as $\sqrt{I_{LRS,0}I_{HRS,0}}$ and $I_{HRS,0}(I_{LRS,0})$

indicates the HRS (LRS) read current of a single device.[21,27] Since the square shape of the CBA was assumed in this simulation, the number of word-lines (WL) and bit-lines (BL) were identical and given as the square-root of the allowed number of bits. When the RM was decreased to 10 % at a certain increased number of bits, which the bit number corresponded to the allowed array size for the read without disturbance due to the involvement of sneak current. In the simulation, the floating scheme was used, which has the least power consuming and easy to use in the practical operation of the ReRAM CBA. In the left panel of Figure 3.8 (a), the orange bar at the most right lower corner of the array indicates the selected cell. The source voltage (V_s) should be applied to the selected WL and the selected BL was assumed to be grounded during reading the selected cell. All the unselected word and bit lines are floated. The purple bars, blue bars and black arrow indicate the half-selected cells, unselected cells, and possible sneak current paths, respectively. Here, hollow and filled bars indicate the cells with HRS and LRS, respectively. The selected cell was assumed to be in the HRS (hollow orange bar), while all other cells were assumed to be in the LRS (filled blue and purple bars) to investigate the worst case in the RM simulation. The R_{cc} values of the Pt used as the WL and TiN used as the BL were set to 20 and 200 Ω, respectively, which were estimated from the test pattern shown in the Figure 3.9 (a for the Pt, b for the TiN). Details for the estimation of the unit line resistance were reported elsewhere.[21] The right panel of Figure 6a shows the simulation results of the RM when the selector was assumed to be Pt/6nm-TiO_2/S-TiN or Pt/8nm-TiO_2/S-TiN, which are denoted as the symmetric or asymmetric selectors, respectively. As it can be seen from Figure 3.7 (d) and (f), the V_r with

maximum nonlinearity of the symmetric and asymmetric selectors were ~0.7 V and ~0.9 V, respectively. However, considering the resistance state of the cells arranged so as the RM is at the worst case, the V_r was taken as 1 V and 1.2 V for the symmetric and asymmetric selectors, respectively, which could maximize the RM in each case in the simulation. The CBA size allowing for a 10 % RM was ~10^3 with the symmetric selector and it was increased to over 10^5 with the asymmetric selector. This is due to the forward sneak current paths (the purple bars in the left panel of Figure 3.8 (a) that were suppressed as the nonlinearity ((I_{LRS} at V_r)/(I_{LRS} at $V_r/2$)) was increased from ~45 for the symmetric selector to ~161 for the asymmetric selector. The reverse sneak current paths (the blue bars in the left panel of Figure 3.8 (a)) were also suppressed as the F/R ratio was increased from ~4 for the symmetric selector to ~5527 for the asymmetric selector. For the asymmetric selector, it took a long time to run the simulation due to the large array size. Therefore, the simulation was stopped at ~60 % of the RM as shown in Figure 6a, but the trend was obviously seen. The calculation of WM requires much further complicated considerations for different circumstances.[21] First, because the set and reset polarity and voltage values were different, the WM for the set and reset should be separately calculated. Second, for each case, there were half selected (or even unselected) cells of which the bias polarity was identical and opposite to the bias polarity of the selected cells when the selected cell was biased to be set or reset. The unselected cells could be connected to the selected WL or BL through the LRS cells. Moreover, the voltage drop (V_{drop}) along the WL and BL due to the finite wire resistance makes it necessary to increase the V_s to compensate for such a loss. This makes the unwanted voltage applied to the half

selected cell further increased. Under such circumstances, the WM could be defined as $\frac{|V_{set\ (or\ reset)}|-|V_{unwant}|}{|V_{set\ (or\ reset)}|}$, where the $V_{set(or\ reset)}$ is set or reset voltages determined from the single 1S1R device, where the V_{unwant} is the applied voltage at the unwanted cell of interest, as will be indicated by red arrows in the following figures. The V_s becomes higher than the $V_{set(or\ reset)}$ as the CBA size increases because of the increasing V_{drop} along the interconnection wire, which makes the V_{unwant} become higher and the WM smaller.[21] For example, Figure 3.8 (b) showed the case where the filled orange bar at the most right lower corner was supposed to be reset (it is now in LRS) by applying a positive V_s to the corresponding WL. In this case, the V_s must be appropriately increased to compensate for the V_{drop} along the WL to the selected cell position, where the V_{drop} was I_{LRS} x R_{cc} x (CBA density)$^{1/2}$. Therefore, the V_s should be higher than the V_{reset} by this V_{drop}, which also increases other spurious effects discussed below. Since the reset process is not simply governed by the voltage effect but also aided by the current flow, which could induce the Joule-heating effect. All the half selected cells sharing the same BL could be influenced by the reset V_s application through the influence by the sneak paths. Among these half selected cells, the most left lower corner cell, indicated by the red arrow in left panel of Figure 6b, is under the worst circumstance for unwanted reset. This is because it is under the same reset bias polarity and all the sneak current is concentrated at this cell for the given states of other cells. In such a situation, all the cells sharing the selected WL (filled purple cells) and the WL that is connected to the arrowed cell (filled blue cells) are at LRS, and all other cells are in HRS. If some of the unselected cells are in LRS,

some of the sneak current would be flown into the cells connected to the half selected BL. Therefore, the disturbance current could be distributed and the stress to the worst case cell became mitigated. The WL connecting the filled blue cells was supposed to be floated. However, the LRS of the red arrowed cell connects that WL to ground, and the V_s could be applied as shown by the black dashed lines and arrows. It should be noted that the voltage polarity across the purple and blue cells was opposite. Given the circumstance that the selectors of the purple cells are under the forward polarity (of course, the selected cell is also under the forward bias polarity) the blue cells are under the reverse bias polarity. Therefore, an asymmetry of the selector greatly improved the achievable CBA density as can be seen from the right panel of the same figure considering this constraint. Nonetheless, the limited asymmetry of the Pt/8nm-TiO_2/S-TiN selector (F/R ratio ~19.8 at a 2.5 V of V_{reset}) allowed an integration density of only ~ 3 x 10^3 cells, whereas the symmetric selector allowed only ~200 cells. The X mark at the last point of the simulation means that further simulation was not possible because the V_s became too high (> 10 V) to make the selected cell voltage reach the V_{reset}.

In contrast, there was a concern about the simultaneous unwanted set at the most left upper corner cell (indicated by the red arrow in left panel of Figure 3.8 (c)). This is because this cell is under the opposite bias polarity to that of the selected cell, and the corresponding WL is at the ground potential due to the LRS of the most left lower cell (filled purple cell). In this case, the sneak current flow effect has less significance because the set is mostly field-driven-effect. Moreover, the current through the HRS cell was lower than that in the LRS cell. For this consideration, the symmetric selector

allowed almost no CBA integration density, but the asymmetric selector allowed almost an identical CBA density (~3 x 10^3 cells) as can be understood from the right panel. The discussions up to this point dealt with the possible complications involved with the reset of the selected cells. Similar situations for the set must also be considered. Figure 3.8 (d) showed the case where the selected cell at the most right lower corner is in the HRS, and a negative value of V_s was applied to the selected WL. Here, as for the case of Figure 3.8 (b), the filled purple and blue cells are in LRS but the most left lower corner cell, indicated by the red arrow, is in the HRS. Since the bias polarity of the selected cell and this red arrow indicated cell is identical, this cell is under the risk of the unwanted set. Being compared with the Figure 6b, two factors are different; first, the directionality of the selectors in purple and blue cells are reversed, but since they are serially connected as indicated by the dashed black lines, this reversal does not induce any difference in the overall conductivity along the indicated paths. Second, since the red arrowed cell is in the HRS, the ground potential does not go directly into the connected WL making the sneak problem less serious. If the resistance ratio of the memory cell is large enough, the concerned WL would be completely floated. As a result, this consideration would be unnecessary. However, the memory cell had a significant off-current, so this must be considered. Anyway, because of this inefficiency in delivering the ground potential to the concerned WL, the WM could be enhanced greatly as can be identified for both the symmetric and asymmetric cases shown in the right panel of the same figure. Therefore, this is not a critical concern compared with the unwanted reset cases (Figure 3.8 (b)). Similar consideration must be taken for the unwanted reset of the red

arrow indicated cell in Figure 3.8 (e) under the given negative V_s to the selected WL. Interestingly, the symmetric selector showed no degradation at all up to the possible simulation range of the array density, because the V_{reset} was very large in this case. This means that no matter how low the V_s (absolutely high V_s), the voltage at the red indicated cell does not reach the V_{reset}. For the asymmetric selector case, there was a certain degradation in the WM up to the possible simulation region due to the lower value of the V_{reset} in this case. However, the WM is far higher than the other cases, making this concern of degradation the least significant. Overall, the side effects that could be accompanied by the set of the selected cell are much less significant than the cases with the reset of the selected cells. The WM simulation demonstrated that the achievable CBA size was only 3 x 10^3 cells, even with the optimized Pt/8nm-TiO_2/S-TiN, which is impractical to be adopted for a high-density memory as well as analog synapse array in neuromorphic circuits.[28–30] This is mainly due to the abnormally high line resistance of Pt and TiN electrodes deposited with the research scale apparatus. The allowable CBA density could be improved by adopting the W electrode, which is widely used in the semiconductor industry and has a much lower ρ (~5.6 $\mu\Omega$cm) than the Pt (~11 $\mu\Omega$cm) and TiN (~220 $\mu\Omega$cm) used in the experiment. In this study, considering the commercialization of the 1S1R device, the W electrode was assumed to have the same dimensions as those used in the 3D X-point products, with a width of 20 nm and a thickness of 100 nm.

Figure 3.10 shows the variation in the achievable array density for the different values of R_{cc} under the assumption that the asymmetric selector was adopted. R_{cc} was

split as 1.1, 5, 20, 100 and 200 Ω based on the value of W (1.1 Ω), Pt (20 Ω) and TiN (200 Ω). It was assumed that top and bottom electrodes have the same R_{cc}. The settings for the LRS and HRS of the cells shown in the left panels of Figure 7a-e were arranged to investigate the worst scenario for each RM and WM simulation, as for Figure 6. As shown in the right panels of Figure 3.10, the allowed array size confirming the RM slightly increased as the R_{cc} decreased (Figure 3.10 (a)), where the achievable array size was ~5 x 10^5 cells. In contrast, the allowed array size confirming the WM increased dramatically (Figure 3.10 (b)-(e)) with the decreasing R_{cc}. This could be understood as follows. First, since the V_r (1.2 V) is much smaller than the absolute values of V_{reset} (2.5 V) and V_{set} (-3.5 V), the resistance of the cells is much larger when the read operation is performed than when the writing (set or reset) operation is performed. That is, the read operation is less affected by the line resistance due to the relatively larger resistance of the cells. Second, the parallel circuits for each simulation should be considered. There are $(N-1)^2$ and (N-1) parallel sneak paths for the RM simulations in Figure 3.9 (a) and the WM simulations in Figure 3.10 (b) and (d), respectively. Moreover, there is only one sneak path for the WM simulations in Figure 3.10 (c) and (e). In all cases, the number of the unit wire for each sneak path is equal to 2N. This indicates the total resistance of the circuit considering only the wire (without consideration of the cell) is $\frac{2N \times R_{cc}}{(N-1)^2}$ for the RM simulation, $\frac{2N \times R_{cc}}{(N-1)}$ for the WM simulation in Figure 3.10 (b), (d), and 2N x R_{cc} for the WM simulation in Figure 3.10 (c), (e). Of course, $\frac{2N \times R_{cc}}{(N-1)^2}$ is the smallest value. Because of the two factors above, the increase of the allowable array size due to the

decrease of R_{cc} during the reading operation was smaller than in the writing operation. As shown in the right panel of Figure 3.9 (a), the allowed array size was ~10^5 at R_{cc} value of 200 Ω, and increased to only ~5 x 10^5 as R_{cc} value decreased to 1.1 Ω. Figure 3.10 (b) shows the WM simulation in the case for the unwanted reset occurs in the red arrowed cell during the reset process of the selected cell, which was worst WM case in Figure 3.8 (b). When the R_{cc} was 100 and 200 Ω, the allowable array size was only ~10^3 due to the influence of V_{drop} on the wire. As the R_{cc} decreased to 1.1 Ω, which is the value of the W electrode, the allowable array size increased to over 1Mb. Because of the large density, the simulation took a long time to perform and it was stopped at the point where 1 Mb of the allowable array size was obtained. Similar results were obtained for the case of the unwanted set occurring at the red arrowed cell during the reset process of the selected cell (Figure 3.10 (c)). Next, the WM simulation, for the case of the unwanted set occurs during the set process of the selected cell, was performed (Figure 3.10 (d)). As described above, in this case, the grounded WL is isolated by the HRS cell marked in red arrow, making the sneak problem less serious. As a result, the WM could be improved more than the previous cases, and > 1 Mb of allowable CBA density could be achieved even at 5 Ω of the R_{cc}. Lastly, during the writing of the select cell, a case where an undesired reset occurs in the red arrowed cell was examined (Figure 3.10 (e)). In this case, > 1 Mb of the allowable array size could also be achieved even at 5 Ω of the R_{cc}. That is, this case is not a limiting factor for the allowable array size. It should be noted that the critical margin governing the allowable array size was changed from the WM to RM as the

R_{cc} decreased, for the reasons described above. When the R_{cc} decreased to 1.1 Ω, all the WM calculations showed that > 1 Mb intergration was possible, but the RM calculation indicated that the maximum size was ~5 x 10^5 (black in Figure 3.10 (a)). Overall, when a W electrode was adopted for the commercialization of the 1S1R device, the achievable CBA density was ~5 x 10^5, which is a reasonably useful value for the high-density memory and analog synapse array in neuromorphic circuits.

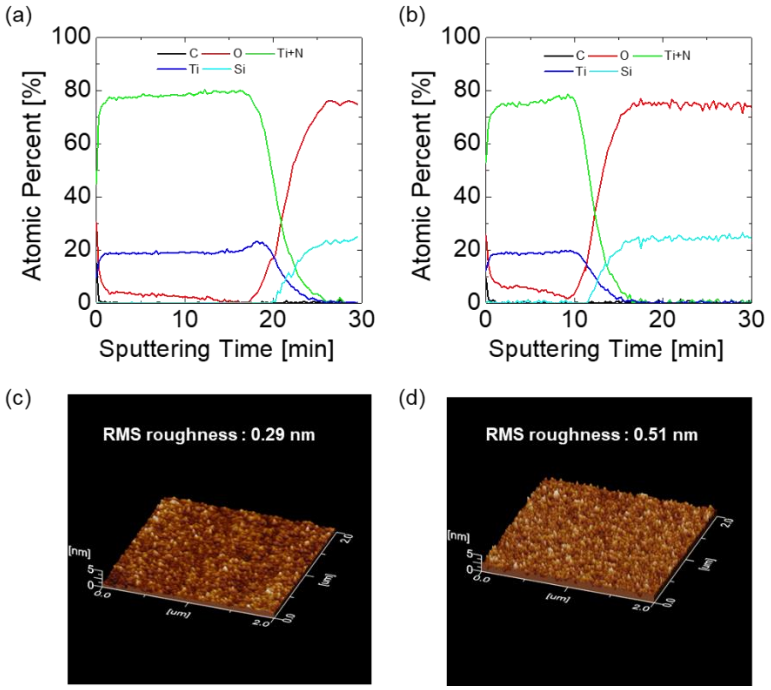

Figure 3.1 The AES depth profile results and AFM topographic images of the A-TiN films (a), (c) and S-TiN films (b), (d) on a SiO_2 substrate.

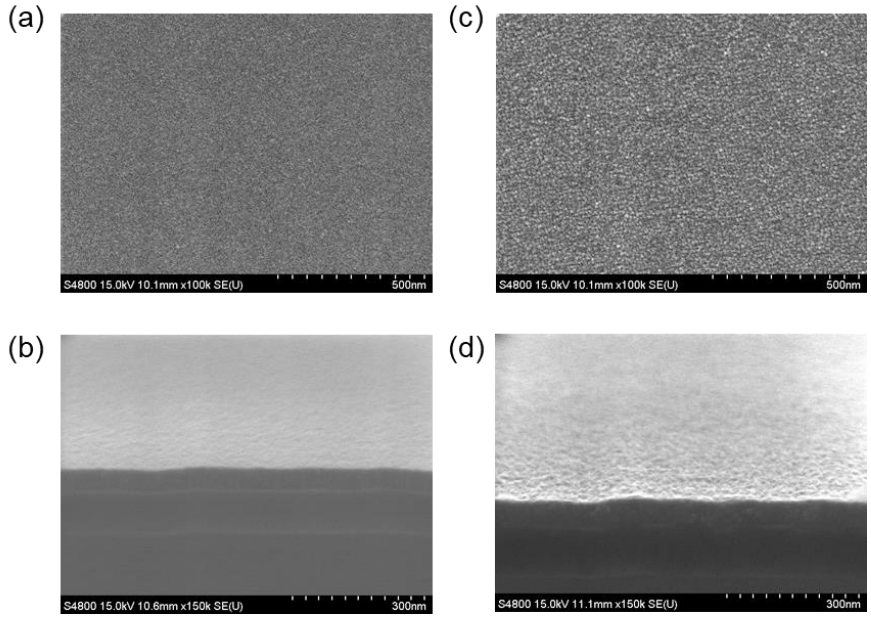

Figure 3.2 Plan-view and cross-sectional SEM images of the A-TiN ((a), (b)) and S-TiN ((c), (d)). S-TiN has a relatively rough surface than A-TiN.

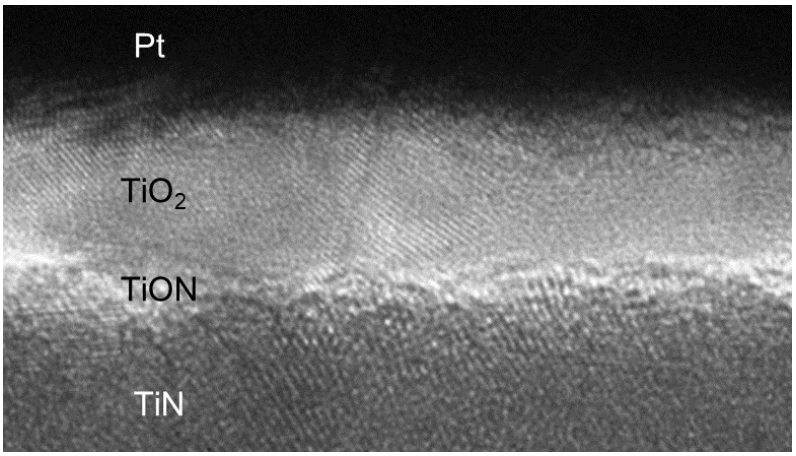

Figure 3.3 The cross-sectional HRTEM image of the Pt/8nm-TiO_2/S-TiN sample.

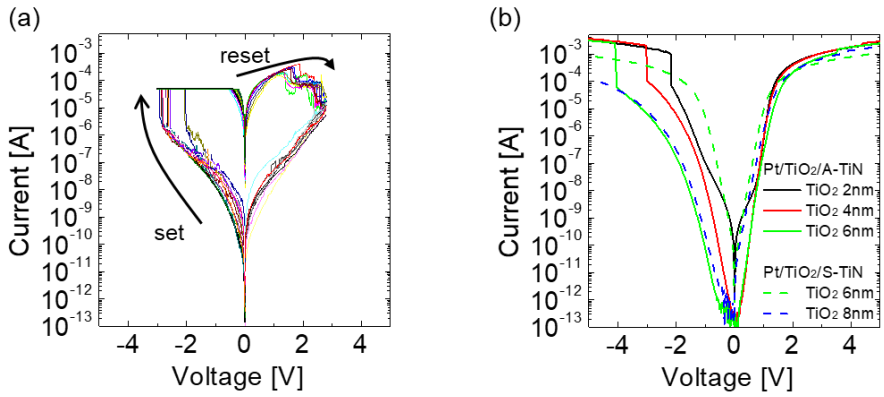

Figure 3.4 (a) The 15 cycles of the I-V curves obtained from the Pt/2nm-HfO_2/A-TiN BRS device with the 50 μA of I_{CC} condition. (b) The I-V curves of the Pt/TiO_2/TiN selectors with different TiO_2 thickness and TiN BE types. The solid and dashed lines are for the A-TiN and S-TiN BE, respectively. Black, red, green and blue lines are for the 2 nm, 4 nm, 6 nm and 8 nm thickness of the TiO_2 layers, respectively.

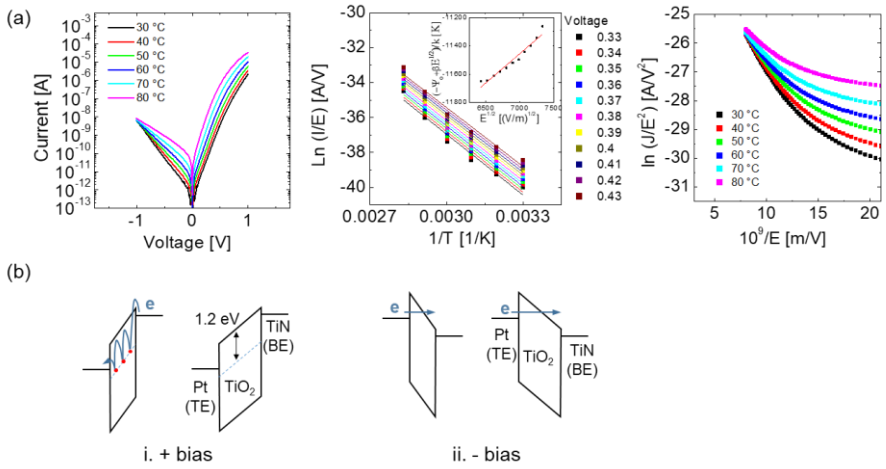

Figure 3.5 (a) Temperature dependent I-V curves and the fitting results to analyze the conduction mechanism of the Pt/8nm-TiO_2/S-TiN selector. The temperature dependent I-V behavior with different temperature ranging from 30 to 80 ℃ (left panel), the plot in the form of Ln(I/E) vs. 1/T for P-F fitting in the ~0.3-0.4 V range (middle panel), $((-\Psi_0 + \beta E^{\frac{1}{2}})/k)$ value plotted as a function of $E^{1/2}$ (upper right inset of the middle panel), and the plot in the form of Ln(J/E^2) vs. 1/E for FN tunneling fitting in the negative voltage range (right panel). (b) A schematic diagram showing the P-F conduction under the positive bias condition (left panel) and FN tunneling under negative bias condition (right panel).

Table 3.1. Conduction mechanism fitting results of the Pt/TiO_2/TiN selectors.

Device	Conduction mechanism + bias region / - bias region	Trap depth	Optical dielectric constant
Pt/TiO_2 6 nm/S-TiN	P-F conduction / FN tunneling	1.0 eV	3.5
Pt/TiO_2 8 nm/S-TiN		1.2 eV	4.6
Pt/TiO_2 4 nm/A-TiN		1.5 eV	7.1
Pt/TiO_2 6 nm/A-TiN		1.3 eV	6.9

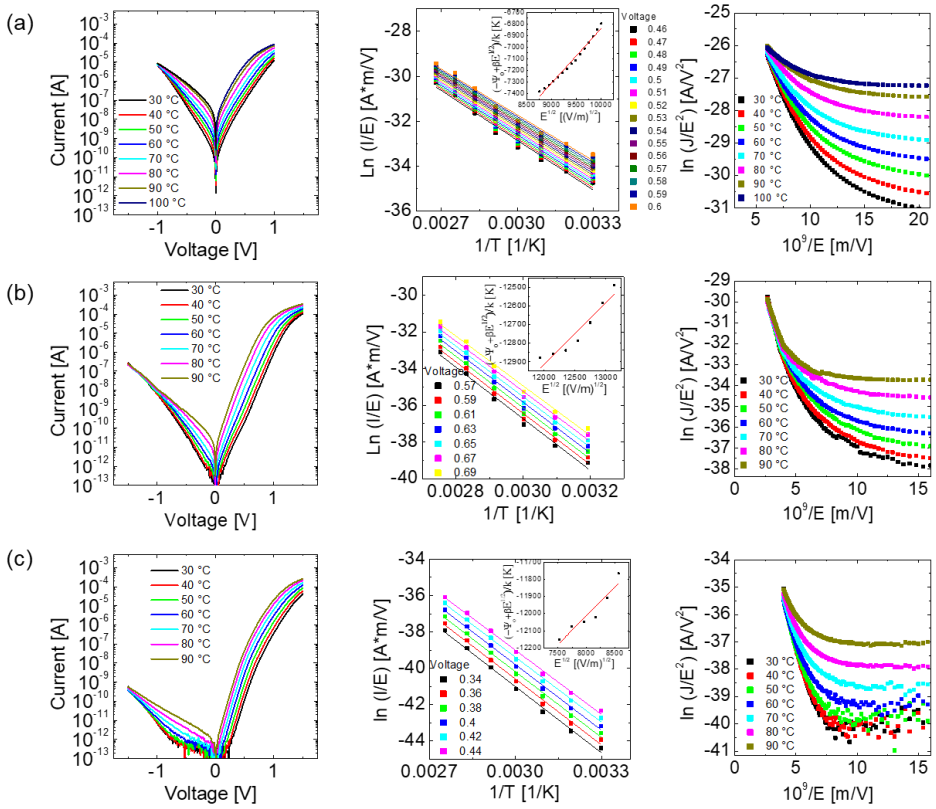

Figure 3.6 Temperature dependent I-V curves and the fitting results to analyze the conduction mechanism of the (a)Pt/6nm-TiO_2/S-TiN selector, (b)Pt/4nm-TiO_2/S-TiN selector and (c)Pt/6nm-TiO_2/A-TiN selector. The configuration of the panels is the same as in Figure 3.5.

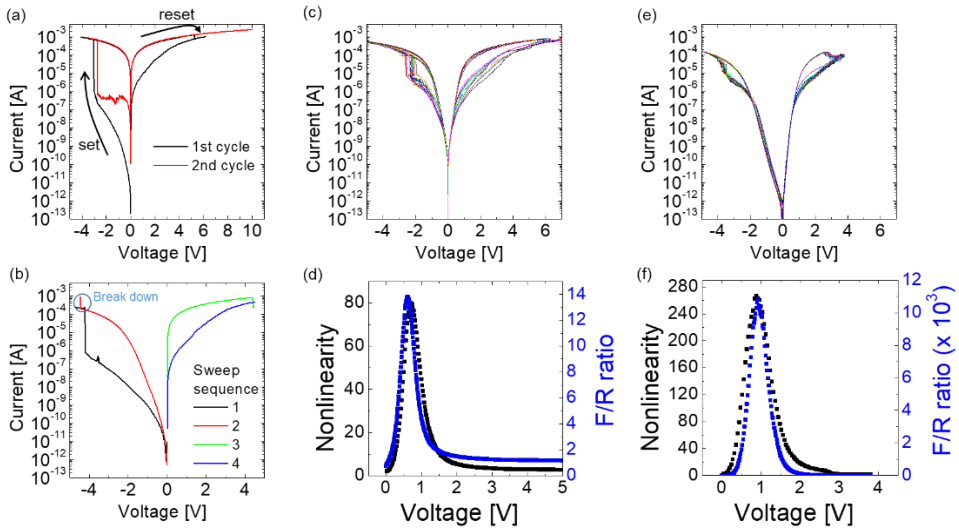

Figure 3.7 (a) The I-V curves of the Pt/HfO_2/A-TiN memory cell without applying the I_{cc}. Black and red lines indicate the first and second cycles, respectively. (b) The I-V curves of the 1S1R where the 1S was Pt/4nm-TiO_2/A-TiN and the 1R was the Pt/HfO_2/A-TiN with no I_{cc} application. The black, red, green and blue lines indicate the first, second, third and fourth sweep, respectively. A circle indicates that the 1S was broken down. (c) The I-V curves of the 1S1R where the 1S was Pt/6nm-TiO_2/S-TiN and the 1R was the Pt/HfO_2/A-TiN with no I_{cc} application. (d) The variation in the nonlinearity (black) and F/R ratio (blue) of the LRS of the I-V curves in (c) as a function of V_r in the positive bias region. (e) The I-V curves of the 1S1R where the 1S was Pt/8nm-TiO_2/S-TiN and the 1R was the Pt/HfO_2/A-TiN without applying any I_{cc}. (f) The variation in the nonlinearity (black) and F/R ratio (blue) of the LRS of the I-V curves in (e) as a function of V_r in the positive bias region.

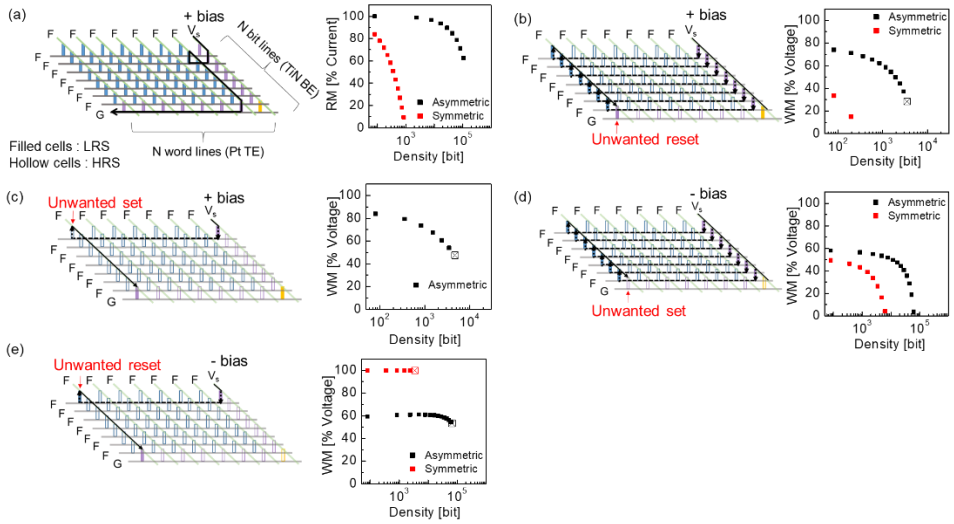

Figure 3.8 The schematic figure of the CBA for the worst scenario (left panels in (a)-(e)) and the HSPICE simulation results to obtain the allowable CBA size considering reading and writing margins (right panels in (a)-(e)). The orange, purple and blue bars indicate the selected, half-selected and unselected cells, respectively. Here, hollow and filled bars indicate the HRS and LRS, respectively. The black and red arrows indicate the sneak current paths and the most stressed cells by the sneak current, respectively. (a) Percent reading margin according to the array size. (b-e) Percent writing margin according to the array size. (b) In the case for the unwanted reset of the red arrowed cell occurs during the reset process of the selected cell. (c) In the case for the unwanted set of the red arrowed cell occurs during the reset process of the selected cell. (d) In the case for the unwanted set of the red arrowed cell occurs during the set process of the selected cell. (e) In the case for the unwanted reset of the red arrowed cell occurs during the set process of the selected cell.

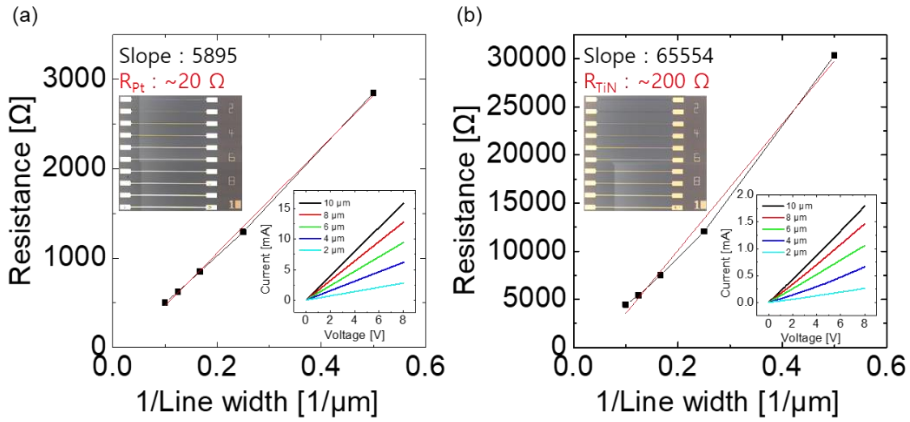

Figure 3.9 Pad-to-Pad resistance vs. 1/line width curves for estimating the R_{cc} (a) for the Pt WL, (b) for the TiN BL.The R_{cc} can be calculated from the equation; $R_{cc} = \frac{2}{l}\frac{d(R_{pad-pad})}{d(\frac{1}{line\ width})}$, where *l* is the pad to pad distance. Here *l* is 680 μm, and the R_{cc} of the Pt and TiN was found to be ~20 and ~200 Ω, respectively. The insets show the raw I-V curves. The details for the estimation of the R_{cc} were reported elesewhere.[21]

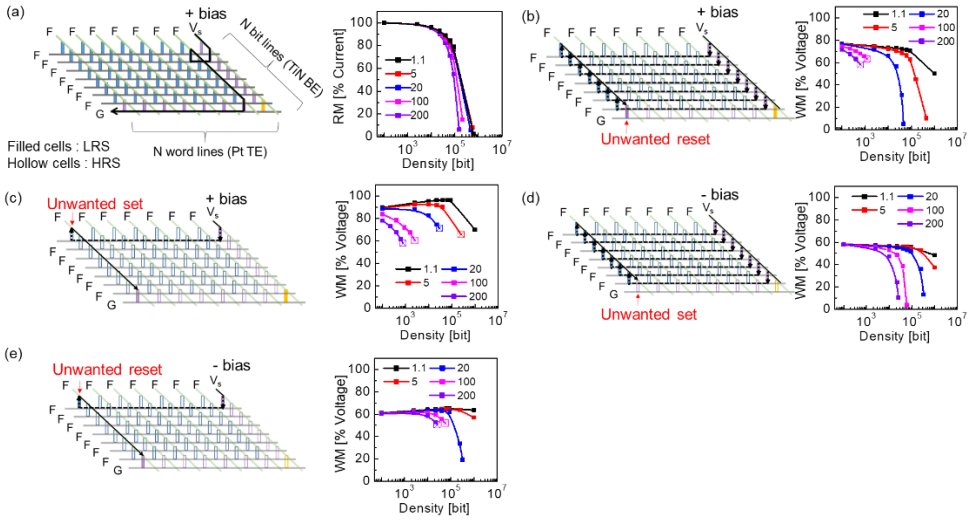

Figure 3.10 The schematic figures for the worst scenario in each simulation, with the same configurations and symbols shown in Figure 3.8 (left panels in (a)-(e)). The variation in the achievable array density for the different values of R_{cc} under the assumption that the asymmetric selector was adopted (right panels in (a)-(e)).

3.4. Summary

In conclusion, a prototypical 1S1R device was fabricated using the Pt/2nm-HfO_2/TiN and Pt/8nm-TiO_2/TiN as the bipolar resistive switching memory cell and nonlinear cell selector, respectively. For the given BRS performance of the memory cell, the optimization of the selector required the search for the TiO_2 film thickness and modification of the TiN BE to make it slightly rougher than the industry standard smooth TiN. The optimized selector showed a maximum nonlinearity of ~270 and rectification ratio of ~10810. The forward (positive) current of the selector near the reset voltage of the memory cell was sufficiently higher than that of the memory cell making the reset voltage of the 1S1R device almost invariant compared with the memory itself. The involved asymmetry or rectification ratio of the selector, resulting from the lower current at the reverse (negative) bias, provided the 1S1R with the self-limiting functionality of the current increase at the moment of the set, which eliminated the application of compliance function. However, this slightly increased the absolute value of the set voltage in the negative bias region, but the degree of increment was minimal because the reset state of the memory was much more resistive than that of the selector in the reverse bias direction.

Based on the achieved functionality of the 1S1R devices, the maximum achievable array size (bit density) was simulated taking into consideration the unit interconnection wire resistance of the TiN (200 Ω) and Pt (20 Ω). The most significant limiting factor was unwanted reset during the the reset operation of the selected cell, whereas the read margin due to the sneak current issue was much less severe under

the given condition. The limited writing margin induced by such unwanted switching operation severely limited the allowable CBA array size to only several kbit. Interestingly, decreasing the interconnection wire resistance by adopting a W electrode, which has a 1.1 Ω of unit wire resistance has changed the limiting factor for the CBA density from the writing margin to the reading margin. This is because the allowable CBA density, when considering the reading margin, was less affected by the line resistance due to the relatively large cell resistance and many parallel paths in the circuit. The 1S1R device developed in this study was able to prevent the overset by limiting the set current without using external circuits or transistors. Moreover, ~0.5 Mb CBA density could be achieved by adopting the W electrode.

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4. HfO_2 based 3D memory device with vertical structure for high density ReRAM

4.1. Introduction

Resistance switching random access memory (ReRAM) is a next-generation memory device and has been studied with great interest for past decades.[1–5] Although vertical NAND (V-NAND) flash memory is now the mainstream of the memory device market, it is expected that this will also face the limit of improvement of memory density in the near future.[6–8] ReRAM has been verified through various studies on the possibility of applying it to not only memory device but also neuromorphic computing, artificial receptors and wearable devices.[9–11] All of these various fields also require basically high-density ReRAM devices. Therefore, it is time to commercialize highly integrated ReRAM. Despite much interest in ReRAM research, there are still problems to be solved for commercialization. Some of the typical problems are limited reliability (rewriting endurance and data retention), sneak current problem, non-uniform switching of the device. The problem of limited reliability can be greatly mitigated when a capacity of memory devices became huge enough since the need for a large number of endurance would not be required. Retention problem in non-volatile memories (NVM) is becoming less significant due to the shortened life span of electronic products does not require 10-year retention data. It was also proposed to overcome the retention problem through materials engineering.[12] Non-uniform switching problems are also thought to be overcome by the incremental step pulse programming (ISPP) method used in NAND flash

memory.[13] The most suitable structure for high-intensity memory devices is the crossbar array (CBA) architecture. The most suitable structure for highly integrated memory devices is the CBA structure. There are two main ways to implement a highly integrated CBA. One is a 3D-Xpoint structure developed by Intel and Micron, which is a stack of planar CBAs stacked up. The other is a V-ReRAM structure based on a V-NAND structure, in which a WL and an isolation layer are sequentially stacked, hole etching is performed, and a switching layer and a BL are deposited in the hole to implement resistance switching on the side wall. A selector is required to suppress the sneak current, which is necessarily associated with the CBA structure.[8] However, since the resistance switching (RS) is occurs at the side wall of the V-ReRAM cell, the adoption of the intermediate electrode is difficult and the selector could not be applied to the device. Thus, devices with self-rectifying or self-nonlinearity characteristics are required in V-ReRAM. Also the cell-to-cell wire resistance (R_{cc}) should be considered. It should be noted that this R_{cc} is independent of the device design rule of the feature size (F), which corresponds to the memory cell size for the given technology node since the wire width and length decrease simultaneously.[14] As the R_{cc} increases, the voltage drop (V_{drop}) along the word line (WL) and bit line (BL) increases. The source voltage (V_s) applied to the selected WL to deliver the writing (or reading) voltage to the selected cell of the CBA necessarily increases as the V_{drop} increases during operation of the device. This reduces the writing/reading margin of the CBA and reduces the achievable density.[14] In other words, materials such as Cu and W having low resistivity should be used for WL and BL basically, and the structure of the ReRAM device, which can reduce the unit line

resistance, should also be devised. In the 3D-Xpoint structure, both WL and BL resistance should be considered, while, the V-ReRAM structure could be free from line resistance problems of WL since WL is formed in a planar shape. In addition, the 3D-Xpoint structure requires three photolithography processes to form a double-layered cells, and the photolithography process increases linearly as the number of layer increases. The V-ReRAM structure is capable of forming ~100 layers of memory cells with only two photolithography processes, considering the technology of V-NAND products. In this chapter, a study on vertical structure device using $Pt/HfO_2/TiN$ memristor in which RS occurs at the side wall of the device as in V-ReRAM is shown. The device showed self-rectifying and self-nonlinearity characteristics suitable for vertical structure devices, enabling the implementation of high-density ReRAM.[15]

4.2. Experimental

For the fabrication of the planar type Pt/HfO_2/TiN device, 50 nm thick TiN was deposited on a SiO_2/Si substrate by using sputtering systems (Endura, Applied Materials). The TiN films were patterned by photolithography followed by a photoresist lift-off process as the BE. For the TiN film, Ti target, with a diameter of 12 inches, was used with 15 standard cubic centimeter per minutes (sccm) of Ar gas and 85 sccm of N_2 gas. The DC power and the substrate temperature were set to 5000 W and 200 ℃. The base and operating pressure were ~10^{-8} torr and 4 mtorr, respectively. Then, 10-nm-thick HfO_2 films were deposited through an ALD using $Hf[N(CH_3)(C_2H_5)]_4$ and O_3 as the Hf-precursor and oxygen source, respectively, at a substrate temperature of 230 ℃. After that, Plasma treatment was performed in shower-head-type ALD chamber using 1000 sccm of Ar gas and 100 sccm of O_2 gas. Then, 50 nm thick Pt top electrode (TE) was deposited by the e-beam evaporator (Maestech, ZZS550-2/D) and patterned by photolithography followed by photoresist lift-off process for the crossbar structure.

For the fabrication of the vertical type Pt/HfO_2/TiN device, multi-layer stacked SiO_2 (130 nm)/TiN (50 nm)/SiN (50 nm)/TiN (50 nm) was deposited on a SiO_2/Si substrate. For the TiN film, sputtering systems (Endura, Applied Materials) was used as in the case of the planar type device. For the SiO_2 and SiN films, plasma-enhanced chemical vapor deposition system (Oxford instruments, PlasmaPro System100) was used. Then, the multi-layer was patterned and etched into a line shape. For the SiO_2 layer etching, reactive-ion etching system (Oxford Instruments, RIE 80 plus) with 40

sccm of CF_4 gas and 4 sccm of H_2 gas was used. In this etching condition, SiO_2 layer was well etched, while etching of nitride films was suppresed. For the TiN/SiN/TiN layer etching, another inductively coupled plasma (ICP) type etching system (Oxford Instruments, PlasmaPro System100 Cobra) with 33 sccm of BCl_3 gas and 50 sccm of Cl_2 gas was used. In this etching condition, nitride films were well etched, while etching of SiO_2 layer was suppresed. After the etching process, a 10nm thick HfO_2 film was deposited and the plasma treatment was performed by the same equipment and process as those of the planar type device. Then, 80 nm thick Pt TE was deposited by the e-beam evaporator (Maestech, ZZS550-2/D) and patterned by photolithography followed by photoresist lift-off process for the crossbar structure.

The width of BE and TE was 10 μm, so that the areas memory cell were 36 μm^2 and 5 μm^2 for the planar and vertical type device, respectively. SEM (Hitachi, S-4800) was used to observe the etching profile of the vertical type device. The cross-sectional transmission electron microscope images of the vertical type device were also observed through the use of a FE-TEM (JEOL, F200). The I-V characteristics were measured using an HP4145B semiconductor parameter analyzer. During the measurement, the Pt TE was biased and TiN BE grounded.

CBA simulation was performed using the HSPICE tool based on the I-V c haracteristics of the devices. The interconnection wire resistances used in the HSPICE simulation were estimated from the test pattern with a constant leng th but variable width. Detailed information for the wire resistance estimation is available in Figure 3.9 of chapter 3.

4.3. Results and Discussion

As shown in chapter 1, Pt/HfO_2/TiN devices show the threshold switching (TS) characteristics since the trapping/detrapping occurs at the shallow trap sites, which exists within the HfO_2.[11] In the case of Pt/Ta_2O_5/HfO_2/TiN devices, the HfO_2 film underwent plasma damage while the Ta_2O_5 was deposited on the HfO_2 using the plasma enhanced atomic layer deposition (PEALD) system, and the deep trap was formed in the HfO_2 film. This has resulted in a stable resistance switching (RS) characteristic in the device.[16] In this study, to obtain memory characteristics in Pt/HfO_2/TiN device, after the HfO_2 layer deposition, plasma treatment was performed before Pt top electrode (TE) deposition to induce deep trap formation in the HfO_2 layer (See experimental section for details). Figure 4.1 (a) shows the Hf 4f (left panel) and O 1s (right panel) core levels in the XPS analytical results of the HfO_2 (10nm) / Si samples with (red lines) and without (black lines) plasma treatment. In the plasma treated samples Hf 4f and O 1s peaks were shifted toward the low binding energy, indicating that an oxygen deficient HfO_2 film was formed.[17] Figure 4.1 (b) shows the current-voltage (I-V) characteristics obtained from the Pt/HfO_2/TiN device at 1 nA compliance current (I_{CC}) conditions without plasma treatment (left panel) and with plasma treatment (right panel), where the Pt TE was biased while the bottom electrode (BE) was grounded. The insets schematically show the device structure. The I-V graphs of the device without plasma treatment (left panel of Figure 4.1 (b)) shows the behavior of the first sweep (black line) and the second sweep (red line) exactly coinciding. On the other hand, in the case of a plasma-treated device (right panel of

Figure 4.1 (b)), the device was turned into the nonvolatile conductive state after the first voltage sweep (black line), and as such, the second sweep followed curve 2 (red line), suggesting that the device showed the RS behavior. In other words, it can be deduced from Figure 4.1 that a deep trap caused by oxygen vacancy is formed in the HfO_2 film during the plasma treatment. As shown in chapter 1, even in the presence of only shallow traps in the HFO_2 film in the Pt/HfO_2/TiN device, transient RS phenomenon is observed when the I-V characteristic is measured with relatively high I_{CC}. However, when the voltage is removed, the trapped electrons in the HfO_2 film escape to the TiN BE over time due to the internal bias which is caused by the difference in work function between Pt TE and TiN BE. Figure 4.2 shows the I-V curves and the retention characteristics of the device at room temperature with and without plasma treatment. Left panels of Figure 4.2 (a) - (c) show the I-V curves obtained from the Pt/HfO_2/TiN device at 100 nA I_{CC} conditions and right panels of Figure 4.2 (a) - (c) show retention characteristics. The I-V graph shows similar behaviors between the device without plasma treatment (a), the device with 90 cycles of plasma treatment (b), and the device with 130 cycles of plasma treatment. In the case of devices without plasma treatment, the LRS current drops to the HRS current level after several thousand seconds at room temperature (right panel of (a)). This is because the electrons trapped in the shallow trap sites in the HfO_2 film escape to the TiN BE over time, as mentioned above. That is, stable memory behavior is not obtained in the device. In the device with 90 cycles of plasma treatment, the retention characteristic was improved compared to the device without plasma treatment, but the LRS current drops to the HRS current level at ~10000 seconds (right panel of (b)).

In other words, it seems that the formation of deep trap sites in HfO_2 film was insufficient. In the case of the device with 130 cycles of plasma treatment, the LRS current is maintained stably for up to 10,000 seconds, and the deep trap sites in the HfO_2 film were thought to be sufficiently formed. All of the electrical characteristics shown below are obtained from the devices with 130 cycles of plasma treatment. The left panels of Figure 4.3 (a) and (b) are optic images with devices formed of 2 × 2 and 4 × 4 arrays, respectively. The middle panel in Figure 4.3 (a) and (b) shows the I-V curves shown in all cells in each array, showing the equivalent I-V behavior between cells in each array. The middle panel in Figure 4.3 (a) and (b) are the I-V curves obtained from all the cells in each array, showing the equivalent I-V behavior in all cells in each array. The right panels of Figure 4.3 (a) and (b) shows that reading operation of the selected cell, which is in the HRS, is performed without disturbance of sneak current in the worst scenario. In the case of a 2 x 2 array, only the '1' cell (selected cell) in the optic image is set as HRS, and the remaining 2-4 cells are set as LRS by the set operation. Then, the DC voltage was applied to 6 V, which is below the set voltage (7.2 V), to read the state of the all cells. The selected '1' cell was clearly distinguished as shown in the right panel of Figure 4.3 (a). This is because the self-rectifying characteristic of the device effectively suppressed the sneak current that could flow in the reverse direction through the '4' cell. The same method of DC reading was also performed on a 4 x 4 array (Figure 4.3 (b)). Only selected '6' cell was set as HRS. The rest of the cells were put into LRS for worst scenario. By DC read operation, the reading of the selected '6' cell set to HRS could be performed without interference of sneak current. In Figure 4.3, a floating scheme was used in

which the voltage is applied to the selected WL, the selected BL is set to ground, and all the remaining lines are floating. According to our previous work, the writing margin (WM) is defined as $\mathrm{WM} = |V_{reset}| - V_s$ for a device that exhibits self-rectifying characteristics.[Ref] For a device with an absolute reset voltage less than the set voltage, due to lack of WM, the device cannot operated in array form. Therefore, 1/2 V or 1/3 V scheme should be adopted for the array operation of this device as shown in Figure 4.4 (a). Through HSPICE simulation, the allowable array size could be obtained considering WM and reading margin (RM). However, HSPICE simulation would sometimes be inefficient because it takes too much time to perform simulation for a CBA having a density of 1 Mb or more. In this chapter, the equations that can calculate WM and RM and obtain acceptable CBA size without going through HSPICE simulation were formulated. When reading the selected cell on the CBA, the following formula is established.

$$V_s - \triangle V_{drop} = V_r \qquad (4.1)$$

Where V_s is the source voltage, $\triangle V_{drop}$ is the dropped voltage at the selected WL and BL, and V_r represents the read voltage of the selected cell. That is, at V_s applied to the selected WL for reading the selected cell, the value obtained by subtracting $\triangle V_{drop}$ is transmitted to the selected cell. $\triangle V_{drop}$ is defined by the following equation.

$$\triangle V_{drop} = R_{Pt}(i_{w1} + i_{w2} + \cdots + i_{wN}) + R_{TiN}(i_{b1} + i_{b2} + \cdots + i_{bN}) \qquad (4.2)$$

Where R_{Pt} and R_{TiN} are the unit line resistances of WL and BL, respectively. As

found in Chapter 3, R_{Pt} and R_{TiN} are 20 and 200 ohms, respectively. i_{wN} and i_{bN} are denoting the currents flowing along the Nth unit wire of the selected word and bit lines from the selected cells. i_{wN} and i_{bN} can be defined by the following equations

$$i_{wN(LRS,HRS)} = i_{bN(LRS,HRS)} = \frac{V_r}{R_{cell(LRS,HRS)}} + i_{h(V)}(N-1) \quad (4.3)$$

$i_{wN(LRS,HRS)}(i_{bN(LRS,HRS)})$ represents the $i_{wN}(i_{bN})$ when the selected cell is in the LRS and HRS states, respectively, and $R_{cell(LRS,HRS)}$ represents the cell resistances at the read voltage when the selected cell is LRS and HRS, respectively. $i_{h(V)}$ represents the LRS current depending on the voltage of the stand-alone device and can be obtained from Figure 4.4 (b). The gray dots in Figure 4.4 (b) replotting the LRS current in the I-V curve of the middle panel in Figure 4.3 (b). The blue line was obtained by polynomial fitting of gray dots. N represents the number of WL and BL. $i_{wN}(i_{bN})$ increase as the distance from the selected cell increases (N increases) by Kirchhoff's law. A detailed analysis of the relevant details is given in our previous study.[14] The above equation shows that the sum of the current flowing in the selected cell and the current flowing in the half-selected cell connected to the selected WL (or BL) is $i_{wN(LRS,HRS)}(i_{bN(LRS,HRS)})$. When using the 1/2 V (1/3 V) scheme in the CBA, the voltage applied to the half-selected cell is a maximum of 1/2 Vs (1/3 Vs). The above equation can be summarized as follows using the formula for the sum of an arithmetical progression.

$$i_{w1} + i_{w2} + \cdots + i_{wN} = i_{b1} + i_{b2} + \cdots + i_{bN} = \frac{NV_w}{R_{cell(LRS,HRS)}} + \frac{N(N-1)i_{h(V)}}{2} \quad (4.4)$$

By substituting equation (4.4) into (4.2), and substituting equation (4.2) into (4.1), a quadratic equation for N is obtained as follows.

$$\frac{i_{h(V)}}{2}N^2 + \left[\frac{V_w}{R_{cell(LRS)}} - \frac{i_{h(V)}}{2}\right]N + \frac{V_w - V_s}{R_{Pt}+R_{TiN}} = 0 \qquad (4.5)$$

From equation (4.5), N according to V_s could be obtained. Also, RM is defined as follows.

$$RM = \frac{I_{REF}-I_{HRS}}{I_{REF}-I_{HRS,0}} \quad where, I_{REF} = \sqrt{I_{LRS,0}I_{HRS,0}} \qquad (4.6)$$

Where, I_{REF} is defined as $\sqrt{I_{LRS,0}I_{HRS,0}}$ and $I_{HRS,0}(I_{LRS,0})$ indicates the HRS (LRS) read current of a single device.[18,19] I_{HRS} is the output current of the CBA, that is, $i_{bN(LRS,HRS)}$, when the selected cell is HRS. Overall, since N and i_{bN} can be obtained according to V_s, the RM according to the density can be calculated, and Figure 4.4 (c) shows the result. Closed black and red circles are calculated values by using the above equations for the RM according to the density when using the 1/2 V scheme and the 1/3 V scheme, respectively (hereafter, the value calculated by the above equations will be referred to as 'theory value'). When the RM (WM) was decreased to 10 % at a certain increased number of bits, which the bit number corresponded to the allowed array size for the read (write) without disturbance due to the involvement of sneak current. The allowed array size was ~5 x 10^3 bits and ~5 x 10^4 bits for using the 1/2 V scheme and 1/3 V scheme, respectively. Opened black and red circles are graphs of HSPICE simulation of RMs according to density when using the 1/2 V scheme and 1/3 V scheme, respectively (hereafter, calculated by HSPICE simulation value will be referred to as the 'HSPICE value'). It was

confirmed that the theory value and the HSPICE value are in fairly good agreement. That is, RM could be quickly predicted by the theory value, without the time-consuming HSPICE simulation. The left panel of Figure 4.5 (a) shows CBA schematic figure when using the 1/2 V scheme. The right panel of Figure 4.5 (a) shows the theory value and HSPICE value for WM verification when using the 1/2 V scheme (right panel of (a)). WM could be defined as follows when using 1/2 V scheme.

$$WM = \frac{V_w - \frac{1}{2}V_s}{V_w} \qquad (4.7)$$

When V_s is applied to selected WL for transfering V_w to the selected cell in writing operation, maximum of 1/2 V_s could be applied to half-selected cells. If 1/2 V_s approaches the value of V_w, an unwanted reset could occur in the half-selected cell. Equation (4.7) can also be applied to WM calculation using V_w (7.2 V) instead of V_r (5 V). However, in consideration of the RM, it should be considered that the selected cell is LRS or HRS, in consideration of the WM, the R_{cell} value can be fixed. Using the equation (4.5), N corresponding to the change in V_s can be obtained, and WM according to the change in V_s can be obtained using the equation (4.7). After all, WM according to density can be calculated as the right panel in Figure 4.5 (a). Closed black circles indicating the theory value show the density already exceeded 10^7 when WM is 46 %. Since the allowable array size is determined by the worse value among WM and RM considerations, the allowable array size in the 1/2 V scheme should be determined by RM and its value is ~5 x 10^3 as shown in Figure 4.4 (c). The open circles represent the HSPICE values and the simulation is performed up to 1 Mb

because it took a long time to run the simulation due to the large array size. As shown in the right panel of Figure 4.5 (a), the theory and HSPICE values were well-matched.

WM could be defined as follows when using 1/3 V scheme.

$$WM = \frac{|V_{reset}| - \frac{1}{3}V_s}{|V_{reset}|} \qquad (4.8)$$

maximum of 1/3 V_s could be applied to unselected cells as indicated by red arrow. If 1/3 V_s approaches the value of $|V_{reset}|$, an unwanted reset could occur in the unselected cells. As shown in right panel of Figure 4.5 (b), the allowable density considering the WM compared to RM is also much larger when using the 1/3 V scheme. In addition, the theory and HSPICE values well-matched. Figure 4.6 shows the result of calculating the power consumed when writing selected cell of CBA using 1/2 V and 1/3 V scheme. The power consumption when using a 1/2 V scheme can be defined by the following equation.

$$\begin{aligned} Power\ consumption = {} & V_w i_{w1} + \frac{1}{2}V_s i_{h(V)}(N-1) \times 2 \\ & + R_{Pt}\left({i_{w1}}^2 + {i_{w2}}^2 + \cdots + {i_{wN}}^2\right) \\ & + R_{TiN}\left({i_{b1}}^2 + {i_{b2}}^2 + \cdots + {i_{bN}}^2\right) \end{aligned} \qquad (4.9)$$

$V_w i_{w1}$ is power consumed in selected cell, $\frac{1}{2}V_s i_{h(V)}(N-1)$ is power consumed in half-selected cell, $R_{Pt}\left({i_{w1}}^2 + {i_{w2}}^2 + \cdots + {i_{wN}}^2\right)$ and $R_{TiN}\left({i_{b1}}^2 + {i_{b2}}^2 + \cdots + {i_{bN}}^2\right)$ are power consumed in selected WL and BL. Equation (4.3) is substituted into equation (4.9) and can be expressed as follows.

$$\begin{aligned} Power\ consumption = {} & V_w i_{w1} + V_s i_{h(V)}(N-1) \\ & + \left[\frac{N{V_w}^2}{{R_{cell}}^2} + \frac{N(N-1)(2N-1){i_{h(v)}}^2}{6}\right](R_{Pt} + R_{TiN}) \end{aligned} \qquad (4.10)$$

The theory values of the power consumption are shown as a closed black circles in Figure 4.6. The power consumption (open black) confirmed by HSPICE simulation also well-matched with the theory value.

Power consumption when using 1/3 V scheme can be defined by the following equation.

$$Power\ consumption = V_w i_{w1} + \frac{2V_s}{3} i_{h(V)}(N-1) + \frac{V_s}{3} i_{reverse}(N-1)^2 + \left[\frac{NV_w{}^2}{R_{cell}{}^2} + \frac{N(N-1)(2N-1)i_{h(v)}{}^2}{6}\right](R_{Pt} + R_{TiN}) \quad (4.11)$$

$V_w i_{w1}$ is power consumed in selected cell, $\frac{2}{3} V_s i_{h(V)}(N-1)$ is power consumed in half-selected cell, $\left[\frac{NV_w{}^2}{R_{cell}{}^2} + \frac{N(N-1)(2N-1)i_{h(v)}{}^2}{6}\right](R_{Pt} + R_{TiN})$ is power consumed in selected WL and BL. Unlike the power consumption equation in the 1/2 V scheme (equation (4.10)), the $\frac{V_s}{3} i_{reverse}(N-1)^2$ term added to the power consumption equation in the 1/3 V scheme (equation (4.11)) represents power consumption in unselected cell. $I_{reverse}$ represents the current flowing through unselected cells in the reverse direction. As can be seen in Figure 4.6, the theory values of the power consumption in 1/3 V scheme (closed red circles) were well-matched to the HSPICE value (open red circles) of the power consumption in 1/3 V scheme. 1/3 V scheme compared to 1/2 V scheme uses power in the reverse direction, so as the density increases, the power consumption in the 1/3 V scheme is larger than the power consumption in the 1/2 V scheme. In order to commercialize the memory device, the capacity should be about 1 Mb/block, but the capacity of the device is not enough to

be commercialized to the maximum ~5 x 10^3. Vertical structured device was designed and fabricated to increase the capacity. Figure 4.7 (a) shows the fabrication process of two-layered vertical device. The vertical etching profile on the side of the cell is very important for the fabrication of the vertical device, since the number of layer of the device will be limited when the etching profile is oblique.[20,21] First, a SiO_2/TiN/SiN/TiN stack is deposited and patterned. In order to obtain a vertical etching profile of the device, SiO_2 is etched in a vertical shape by over-etching of the SiO_2 under the condition that TiN is not etched but only SiO_2 is etched. After that, over-etching the TiN/SiN/TiN layer is performed to obtain a vertical shape of multi-nitrites layer under the condition that the SiO_2 layer is not etched well. (see the experimental part for detailed procedure and conditions). Figure 4.7 (b) is a schematic diagram of the vertical device. The pad area of each cell was opened as shown in the figure through the selective etch to contact the TiN BE of the top cell and the bot cell with the probe tip. Figure 4.8 is a SEM images of various regions of the vertical device. Figure 4.8 (a) shows that the side wall of the cell which is etched in a vertical shape. Figure 4.8 (b) shows that the Pt TE was well deposited on the side wall of the cell. Figure 4.8 (c) shows that the pad areas of the top cell and the bottom cell were well open, respectively. Figure 4.9 (a) and (b) show the cross-section field emission transmission electron microscopy (FE-TEM) image and energy-dispersive X-ray spectra (EDS) mapping result of the vertical device. From Figure 4.8 and 4.9, it can be seen that the vertical device has been successfully fabricated. The vertical device were fabricated in a 2 × 2 array as shown in Figure 4.10 (a). Figure 4.10 (b) shows I-V curves for a total of 8 cells, all of which show equivalent I-V behavior, with I_{cc} set

to $5x10^{-8}$ A. In Figure 4.10 (c), only the selected cell indicated by the red circle in Figure 4.10 (a) is set as HRS, and all the remaining cells are in the LRS. Then, DC voltage is applied up to 7.5 V to read all cells. The HRS of the selected cell ccould be read well without interrupting the sneak current as shown in Figure 4.10 (c). Figure 4.11 shows an analysis of the RM in the vertical device in a similar way to the analysis of the planar element above. 4.11 (a) is a schematic diagram of a cell array for calculating RM when using a 1/2 V scheme and a 1/3 V scheme in a vertical device. Assuming that the vertical device is commercialized and the unit cell height is 20 nm, the unit cell height of the vertical device could be defined as 1F since the current memory product uses ~20 nm technology node. As in the case of the planar element, the relationship between V_s, V_{drop} and V_r can be defined by the equation (4.1). However, V_{drop} is defined for the vertical device as follows, unlike the planar device.

$$\triangle V_{drop} = (L+1)R_{Pt}(i_{w1} + i_{w2} + \cdots + i_{wN}) + R_{TiN}(i_{b1} + i_{b2} + \cdots + i_{bN}) \quad (4.12)$$

Here, L means the number of layers in the vertical device. As mentioned above, by defining one layer of the vertical element as 1F, (L + 1) term is added to account for the increase in the length of the Pt TE as the number of layer increases. Also, as the L increases, the number of half-selected cells connected to the selected WL also increases. Therefore, the current flowing to the selected WL can be defined by the following equation.

$$i_{wN} = \frac{V_r}{R_{cell(LRS,HRS)}} + i_{h(V)}(LN-1) \quad (4.13)$$

The other terms in equation (4.13) are all the same as in the case of planar device (equation (4.3)), and only the term representing the number of half-selected cells has

been changed from (N-1) to (LN-1). $i_{h(V)}$ can be obtained by replopting the LRS current in Figure 4.10 (b) (gray dots) and fitting it to the polynomial (blue line) as shown in Figure 4.11 (b). The number of half-selected cells connected to the BL is the same as that of the planar device regardless of the number of layer in the vertical device, so i_{bN} is the same as in equation (4.3). To calculate the RM according to the density, the equation is summarized by a quadratic equation for N as follows.

$$\left[\frac{i_{h(V)}}{2}[L(L+1)R_{Pt}+R_{TiN}]\right]N^2$$
$$+\left[\frac{V_r}{R_{cell(LRS)}}[(L+1)R_{Pt}+R_{TiN}]-\frac{i_{h(V)}}{2}[(-L^2+L+1)R_{Pt}+R_{TiN}]\right]N$$
$$+V_r-V_s=0 \qquad (4.14)$$

From equation (4.14), N according to V_s could be obtained. Also, RM according to V_s could be obtained from equation (4.6) as in the case of the planar device. In Figure 4.11 (c) closed black and red circles are theory values of the RM according to the density when using the 1/2 V scheme and the 1/3 V scheme, respectively. The allowed array size was ~3 x 10^5 bits and ~8 x 10^5 bits for using the 1/2 V scheme and 1/3 V scheme, respectively. Opened black and red circles are HSPICE values of RMs according to density when using the 1/2 V scheme and 1/3 V scheme, respectively. It was confirmed that the theory value and the HSPICE value are in fairly good agreement.

Equation (4.14) can be applied directly to the WM calculation if V_r (7 V) is changed to V_w (10 V) and the R_{cell} is changed to the cell resistance of the set voltage of 10 V. The WM of the vertical device can be defined as equation (4.7) and (4.8) when it

using 1/2 V scheme and 1/3 V scheme, respectively. The left panels of Figure 4.12 (a) and (b) show CBA schematic figure when using the 1/2 V and 1/3 V scheme, respectively. The right panel of Figure 4.12 (a) and (b) show the theory value and HSPICE value for WM verification when using the 1/2 V scheme and 1/3 V scheme, respectively. Closed black circles indicating the theory value show the density exceeded 10^7 and 10^9 when the 1/2 V and 1/3 V scheme was used, respectively. Since the allowable array size is determined by the worse value among WM and RM considerations, the allowable array size in the 1/2 V and 1/3 V scheme should be determined by RM and its value is ~3 x 10^5 bits and ~8 x 10^5 bits, respectively, as shown in Figure 4.11 (c). In the right panels of Figure 4.12 (a) and (b), the open circles represent the HSPICE values and the simulation is performed up to 1 Mb because it took a long time to run the simulation due to the large array size. As shown in the rights of Figure 4.12 (a) and (b), the theory and HSPICE values were well-matched.

The power consumption in the 1/2 V scheme of the vertical device CBA could be calculated by the following equation.

$$\begin{aligned} Power\ consumption = {} & \mathrm{V_w i_{b1}} + \frac{\mathrm{V_s}}{2}\mathrm{i_{h(v)}(NL-1)} + \frac{\mathrm{V_s}}{2}\mathrm{i_{h(v)}(N-1)} \\ & + R_{Pt}\left({i_{w1}}^2 + {i_{w2}}^2 + \cdots + {i_{wN}}^2\right) \\ & + R_{TiN}\left({i_{b1}}^2 + {i_{b2}}^2 + \cdots + {i_{bN}}^2\right) \end{aligned} \qquad (4.15)$$

$V_w i_{b1}$ is power consumed in selected cell, $\frac{1}{2}V_s i_{h(V)}(N-1)$ is power consumed in half-selected cells which were connected to selected BL, $\frac{1}{2}V_s i_{h(V)}(NL-1)$ is power consumed in half-selected cells which were connected to selected WL, $R_{Pt}\left({i_{w1}}^2 +\right.$

$i_{w2}{}^2 + \cdots + i_{wN}{}^2\big)$ and $R_{TiN}\big(i_{b1}{}^2 + i_{b2}{}^2 + \cdots + i_{bN}{}^2\big)$ are power consumed in selected WL and BL. Equation (4.13) is substituted into equation (4.15) and can be expressed as follows.

$$Power\ consumption$$

$$= \mathrm{V_w i_{b1}} + \frac{\mathrm{V_s}}{2}\mathrm{i_{h(v)}(NL-1)} + \frac{\mathrm{V_s}}{2}\mathrm{i_{h(v)}(N-1)}$$

$$+(\mathrm{L}+1)\mathrm{R_{Pt}}\left[\frac{\mathrm{NV_w}^2}{\mathrm{R_{cell}}^2} + \mathrm{i_{h(v)}}^2\left(\frac{\mathrm{L}^2}{6}\mathrm{N(N+1)(2N+1)} - \mathrm{LN(N+1)} + \mathrm{N}\right)\right]$$

$$+\mathrm{R_{TiN}}\left[\frac{\mathrm{NV_w}^2}{\mathrm{R_{cell}}^2} + \frac{\mathrm{i_{h(v)}}^2\mathrm{N(N-1)(2N-1)}}{6}\right] \qquad (4.16)$$

In the same way, the power consumption when using the 1/3 V scheme is defined as follows.

Power consumption

$$= \mathrm{V_w i_{b1}} + \frac{\mathrm{V_s}}{3}\mathrm{i_{h(v)}(NL-1)} + \frac{\mathrm{V_s}}{3}\mathrm{i_{h(v)}(N-1)} + \frac{\mathrm{V_s}}{3}\mathrm{i_{reverse}}[(\mathrm{N}-1)^2\mathrm{L} + (\mathrm{N}-1)]$$

$$+(\mathrm{L}+1)\mathrm{R_{Pt}}\left[\frac{\mathrm{NV_w}^2}{\mathrm{R_{cell}}^2} + \mathrm{i_{h(v)}}^2\left(\frac{\mathrm{L}^2}{6}\mathrm{N(N+1)(2N+1)} - \mathrm{LN(N+1)} + \mathrm{N}\right)\right]$$

$$+\mathrm{R_{TiN}}\left[\frac{\mathrm{NV_w}^2}{\mathrm{R_{cell}}^2} + \frac{\mathrm{i_{h(v)}}^2\mathrm{N(N-1)(2N-1)}}{6}\right]$$

The theory values of the power consumption are shown as a closed black and red circles when the 1/2 V and 1/3 V scheme was used, respectively, in Figure 4.13. The power consumption confirmed by HSPICE simulation (open black and red circles when the 1/2 V and 1/3 V scheme was used, respectively,) also well-matched with the theory value.

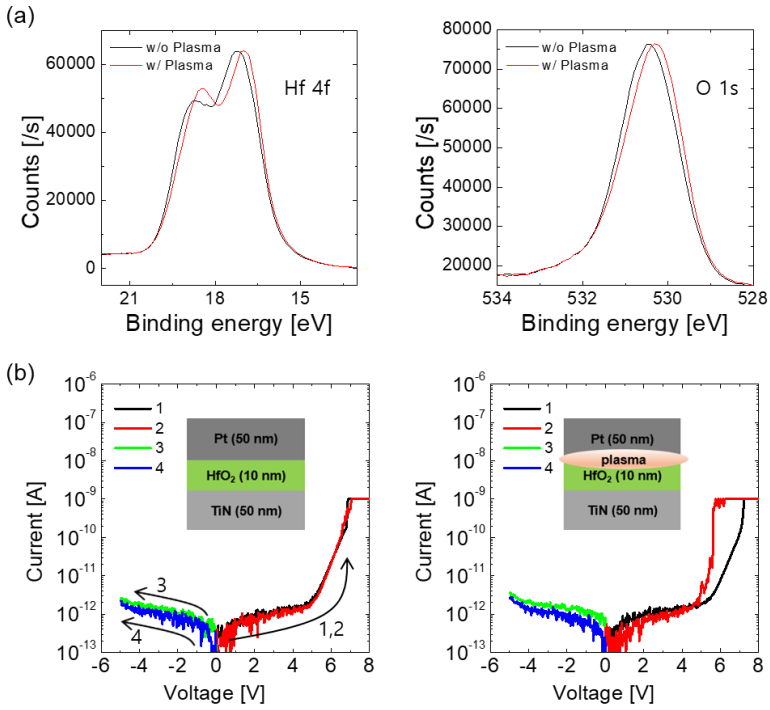

Figure 4.1 (a) Hf 4f (left panel) and O 1s (right panel) core levels in the XPS analytical results of the HfO_2 (10nm)/Si samples with (red lines) and without (black lines) plasma treatment. (b) I-V characteristics obtained from the Pt/HfO_2/TiN device at 1 nA I_{CC} conditions without plasma treatment (left panel) and with plasma treatment (right panel).

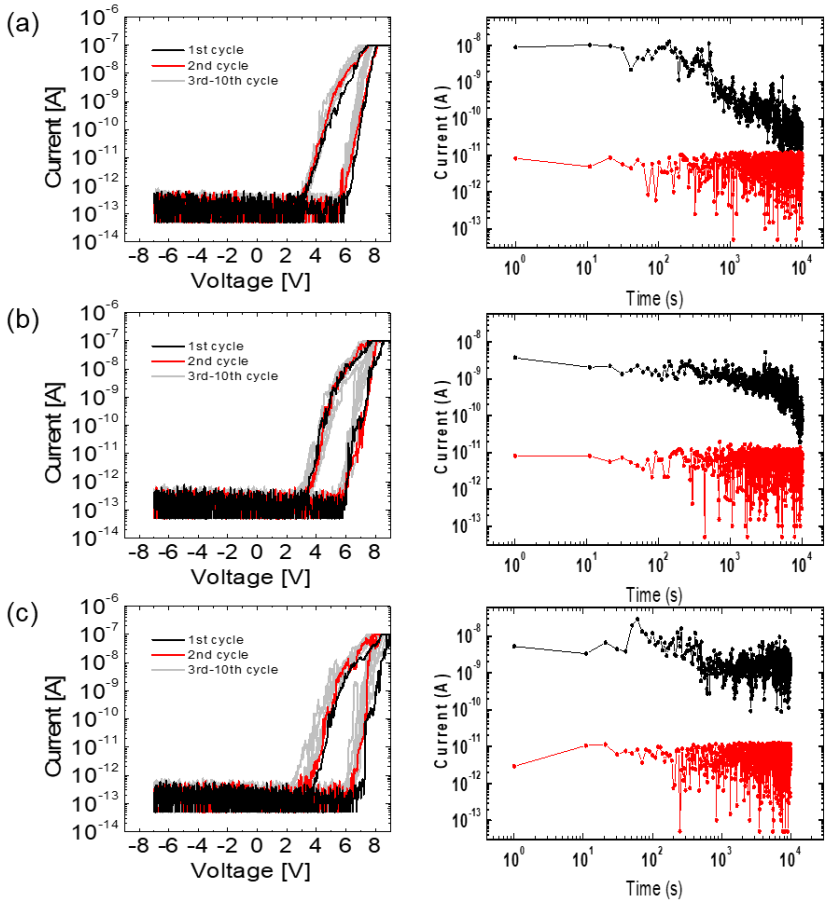

Figure 4.2 I-V curves (left panels) and the retention characteristics (right panels) of the device at room temperature. (a) without plasma treatment (b) with 90 cycles of plasma treatment (c) with 130 cycles of plasma treatment.

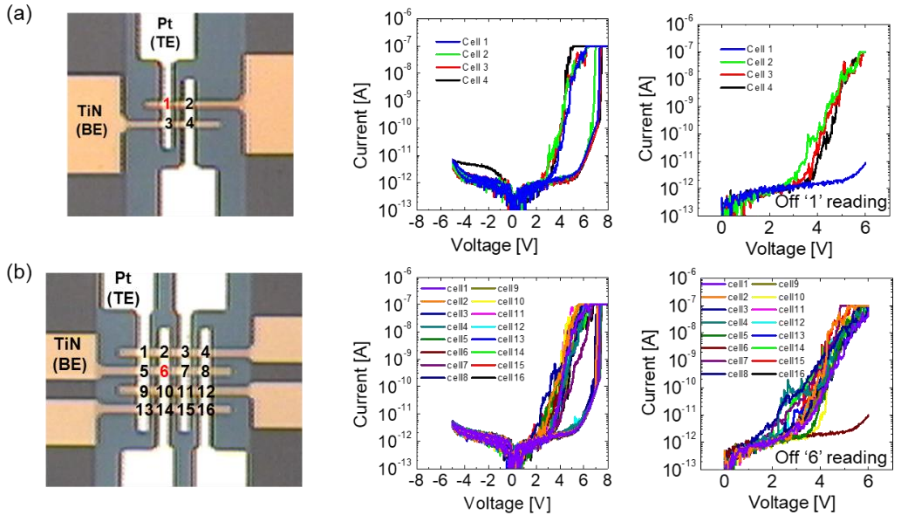

Figure 4.3 Optic images (left panels), the I-V curves of all cells (middle panels), and, the I-V curves during DC reading operation of the selected-cell (right panels), for the 2 x 2 array (a) and 4 x 4 array (b).

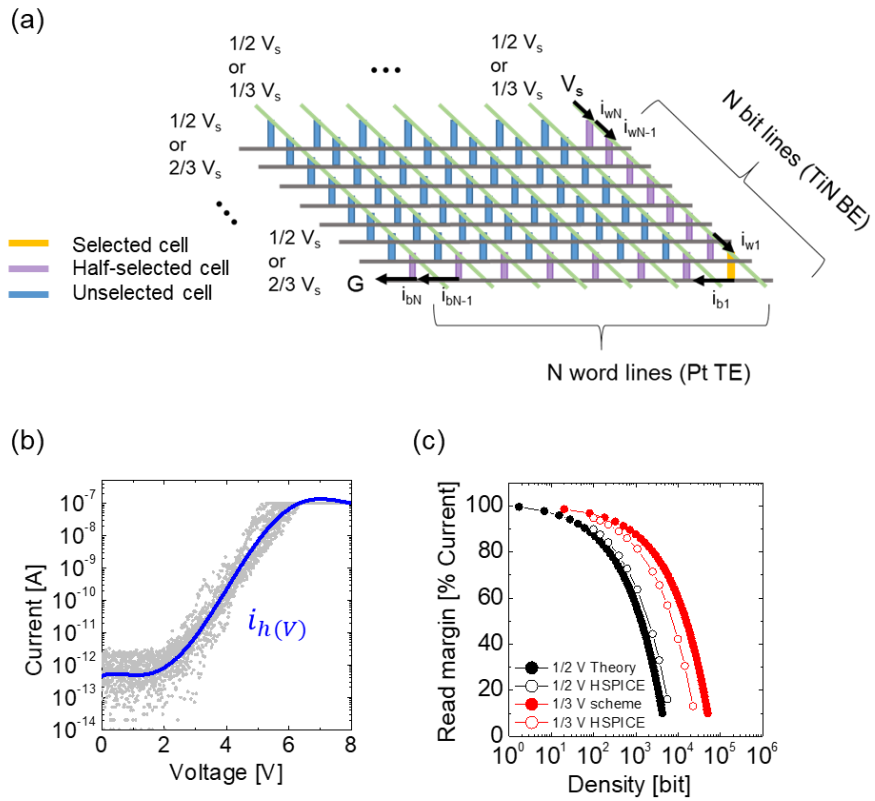

Figure 4.4 (a) Schematic figures of the CBA. (b) Reploted graphs of the LRS current in the I-V curve of the middle panel in 'Figure 4.3 (b)' (grey dots), and polynomial fitting graph of gray dots (blue line). (c) The calculated RM according to the density.

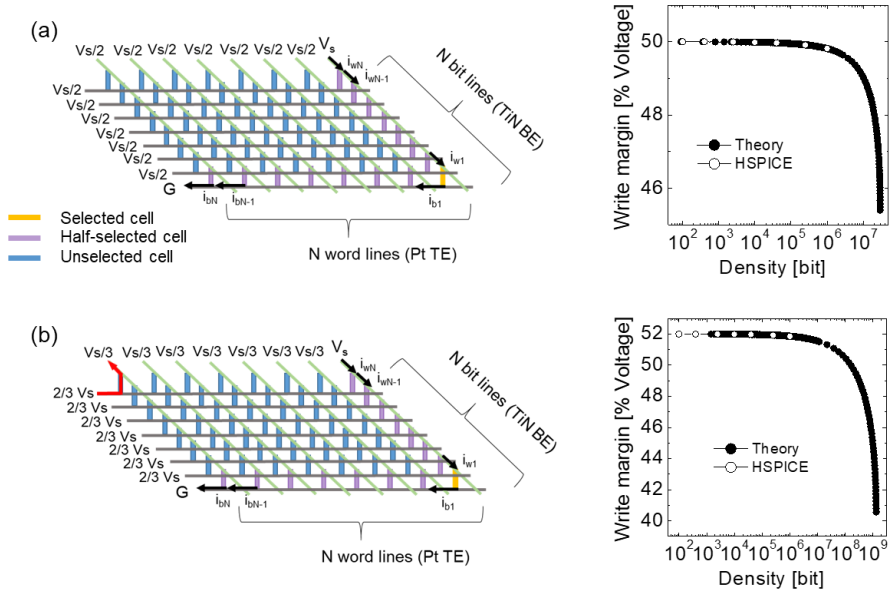

Figure 4.5 (a) Schematic figure of the CBA (left panel), and the theory value and HSPICE value for WM verification (right panel) when the 1/2 V scheme is adopted for operation of the CBA. (b) Schematic figure of the CBA (left panel), and the theory value and HSPICE value for WM verification (right panel) when the 1/3 V scheme is adopted for operation of the CBA.

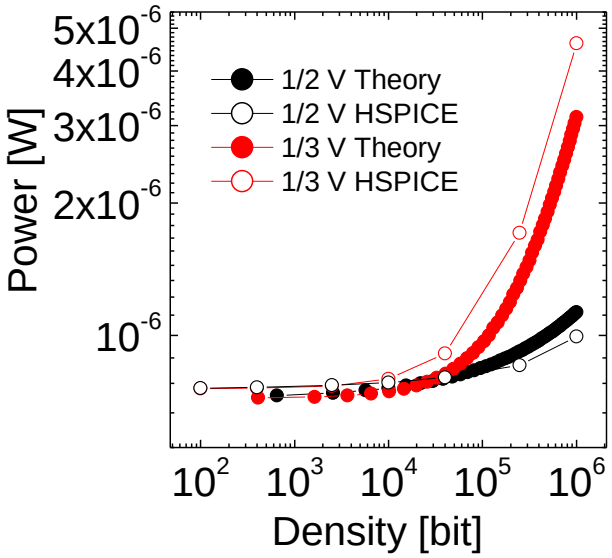

Figure 4.6 Results of calculating the power consumed when writing selected cell of CBA using 1/2 V and 1/3 V scheme. Closed and open circles represent the theory and HSPICE values, respectively.

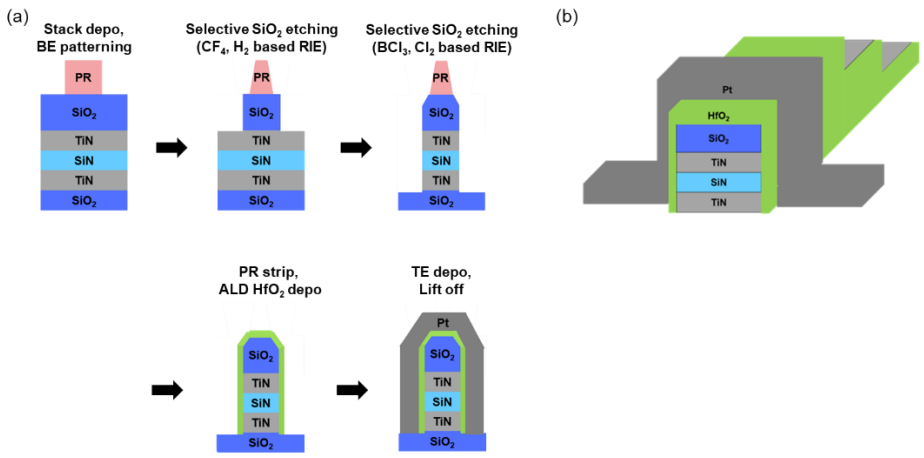

Figure 4.7 (a) The fabrication process of two-layered vertical device. (b) Schematic diagram of the vertical device

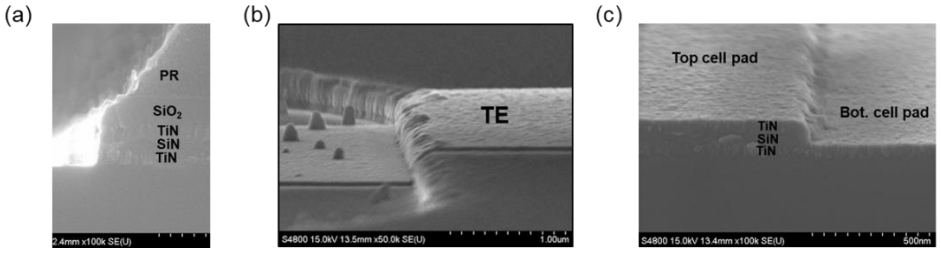

Figure 4.8 SEM images of various regions of the vertical device. (a) SEM Image of the side wall of the cell which is etched in a vertical shape. (b) SEM Image of the Pt TE. (c) SEM Image of the pad areas of the top and the bottom cell.

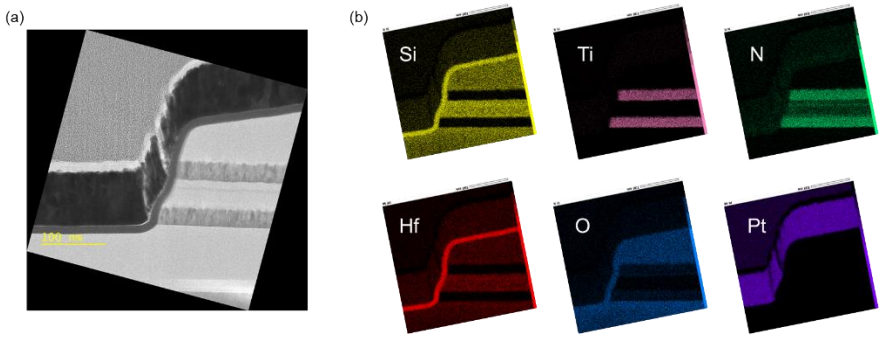

Figure 4.9 (a) The cross-section FE-TEM image and (b) EDS mapping result of the vertical device.

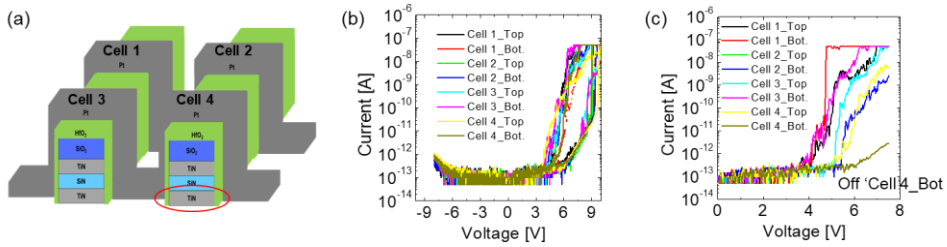

Figure 4.10 (a) Schematic figure of the vertical device in 2 x 2 array format. Red circle represents the selected cell. (b) I-V curves of all cells in the array. (c) I-V curves during DC reading operation of the selected-cell.

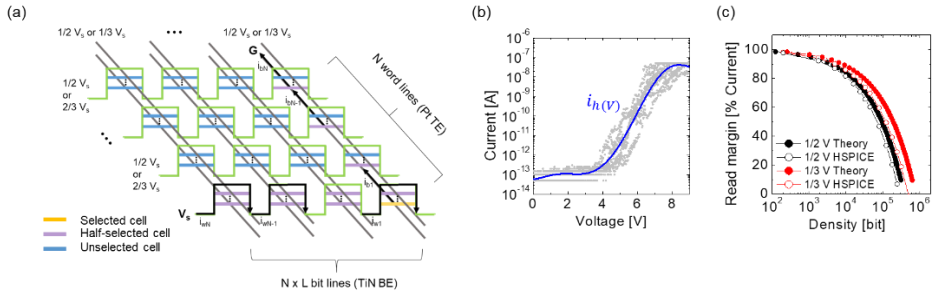

Figure 4.11 (a) Schematic figure of the CBA. (b) Reploted graphs of the LRS current in the I-V curve of the middle panel in 'Figure 4.10 (b)' (grey dots), and polynomial fitting graph of gray dots (blue line). (c) The calculated RM according to the density.

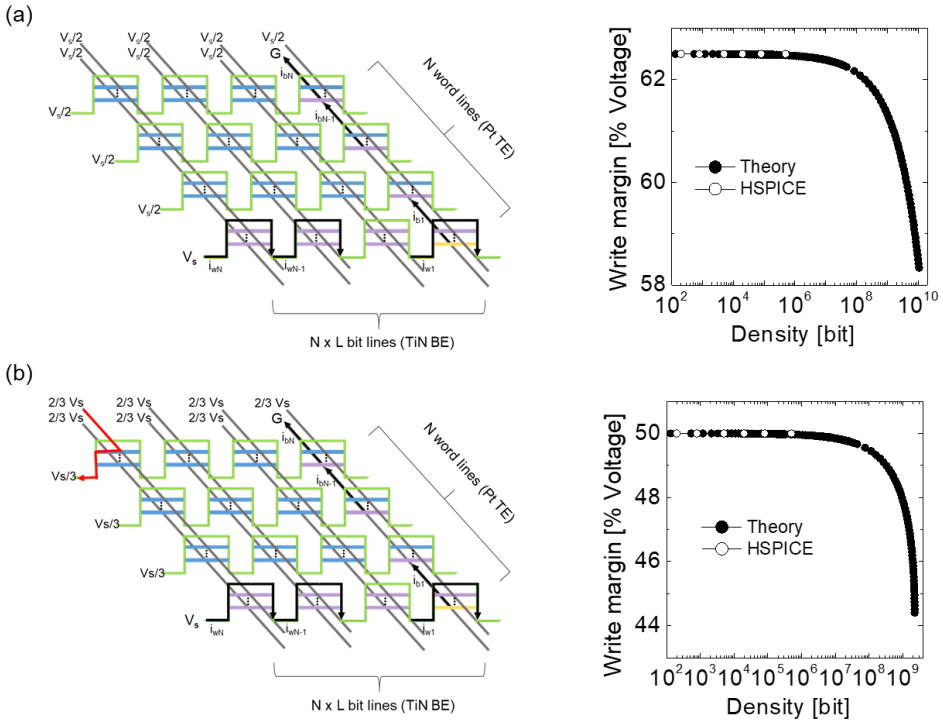

Figure 4.12 (a) Schematic figure of the CBA (left panel), and the theory value and HSPICE value for WM verification (right panel) when the 1/2 V scheme is adopted for operation of the CBA. (b) Schematic figure of the CBA (left panel), and the theory value and HSPICE value for WM verification (right panel) when the 1/3 V scheme is adopted for operation of the CBA.

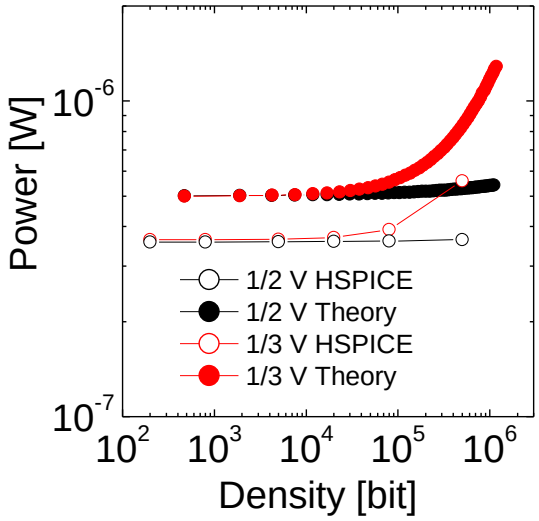

Figure 4.13 Results of calculating the power consumed when writing selected cell of CBA using 1/2 V and 1/3 V scheme. Closed and open circles represent the theory and HSPICE values, respectively.

4.4. Summary

As V-NAND, which is the mainstream of the memory product market, is expected to meet the limitation of integration in the near future, it should accelerate the commercialization of next-generation memory devices. In the CBA structure, the unit cell size of the resistance-change memory device is $4F^2$, which is the smallest among the other non-volatile memory (NVM) and is the most advantageous product in the improvement of the memory cell density. In terms of cost and efficiency, it seems to be the V-ReRAM structure that simulates the structure V-NAND structure that is most advantageous for improving density of ReRAM. In this study, vertical structured Pt/HfO_2/TiN device, which has a resistance switching in the side wall of device like V-ReRAM structure, is developed. In the case of the vertical structure device, it is difficult to adopt the selector device. Therefore, the self-rectifying and self-nonlinearity characteristics of the Pt/HfO_2/TiN device itself was required. To achieve these characteristics, plasma treatment on the HfO_2 film was performed and it induces deep trap in the HfO_2 layer. This enables the device has stable NVM memory behavior with self-rectifying and self-nonlinearity characteristics. Planar device and vertical device were fabricated as array, and it was verified that equivalent characteristics were obtained from all cells in each array. In addition, the equations for predicting acceptable CBA densities was devised, and the CBA density could be quickly calculated without going through time-consuming simulations. It was confirmed that the calculation of the reading/writing margin and power consumption from the equations is well matched with the results of the HSPICE simulation. Through

theoretical calculation and simulation, it was confirmed that the density of ~1 Mb could be achieved from the vertical device which was developed in this study.

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5. Conclusion

Chapter 2 shows the results of research on artificial receptors, which are necessary for humanoid generation but which are still immature. The nociceptor is a nerve system that enables a person to feel the pain, and its characteristics were emulated by Pt/HfO_2/TiN memristor. When a person receives any stimulus from the outside, if the degree of this stimulus does not reach a certain threshold, the person's brain does not recognize it as pain. On the other hand, when the stimulus is above the threshold, it is recognized as pain. That is, the nociceptor exhibits threshold switching characteristics. As a result of attempting to find a memristor capable of implementing the threshold switching characteristics of a nociceptor, Pt/HfO_2/TiN memristor was found. In addition, it shows all the necessary behaviors as a solid-state nociceptor, such as relaxation, overlapping, allodynia and hyperalgesia, thanks to its specific trap-distribution in the band gap of the HfO_2 dielectric layer and built-in potential due to the work function mismatch between the two electrodes. we also carefully compared the material and electrical properties of the Pt/HfO_2/TiN device and Pt/Ti/HfO_2/TiN device to clarify the reason why the Pt/HfO_2/TiN device can show the nociceptive behavior whereas the other cannot.

To implement artificial receptors or artificial intelligence in hardware, a high-density memory device is basically required. In addition, vertical NAND flash memory (V-NAND), which is the mainstream of the memory product market, is expected to meet the limit of improvement in integration in the near future. In Chaper 3-4, a method to realize highly integrated CBA as two structures using the memristor

which is most advantageous compare to other non-volatile memory (NVM) devices, in terms of improvement of integration degree is proposed.

The first one is a 1 selector-1 resistor (1S1R) structure in which a selector device and a resistance change device are connected in series. Here, Pt/TiO_2/TiN nonlinear selector device was used as 1S, and a Pt/HfO_2/TiN bipolar resistance switching (BRS) device was used as 1R. In order to apply a nonlinear selector to a 1S1R device, the performance of the selector itself, such as high nonlinearity and high current level, is important, and compatibility of the selector electrical characteristics to the 1R are also important to be considered. For example, the selector current must be higher than that of the HRS current of the bipolar resistance switching (BRS) cell. Otherwise, the set voltage increases significantly by the voltage partake effect at the moment of the set, or the selector would be broken down at the excessively high set voltage. We performed extensive optimization works of the non-linear selector by changing the thickness of TiO2 and the type of TiN electrode. After all, by increasing the asymmetry of the selector, it has been proved that the overset of the memory device can be prevented to reduce the reset (switching from LRS to HRS) voltage and improve the uniformity of the current-voltage (I-V) curve. Based on the achieved device performance of the 1S-1R, writing and reading margin analysis were conducted using commercial simulation package, HSPICE. As the Forward/Reverse (F/R) ratio increased by increasing the asymmetry of the selector, the reverse sneak current could be suppressed in the CBA structure, and the achievable CBA density could be significantly improved considering reading and writing margins. The

principle of controlling the asymmetry of the selector through the investigation of the conduction mechanism has also been systematically analyzed. It has been confirmed that the CBA density of ~0.5 Mb could be obtained when applying the tungsten electrode, which is widely used in the semiconductor industry, to the 1S1R device developed in this study.

The second one is a V-ReRAM structure based on a V-NAND structure, in which a WL and an isolation layer are sequentially stacked, hole etching is performed, and a switching layer and a BL are deposited in the hole to implement resistance switching on the side wall. In this study, to obtain memory characteristics in Pt/HfO_2/TiN device, after the HfO_2 layer deposition, plasma treatment was performed before Pt top electrode (TE) deposition to induce deep trap formation in the HfO_2 layer. As a result, stable RS characteristic could be obtained from the device. The vertical device was fabricated as array, and it was verified that equivalent characteristics were obtained from all cells in each array. In addition, the equations for predicting acceptable CBA densities was devised, and the CBA density could be quickly calculated without going through time-consuming simulations. It was confirmed that the calculation of the reading/writing margin and power consumption from the equations is well matched with the results of the HSPICE simulation. Through theoretical calculation and simulation, it was confirmed that the density of ~1 Mb could be achieved from the vertical device which was developed in this study.

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1. **Yumin Kim**, Woojin Lee, Dae-Ryong Jung, Jongmin Kim, Seunghoon Nam, Hoechang Kim and Byungwoo Park, Optical and electronic properties of post-annealed ZnO:Al thin films, Applied physics letters, 96, 171902 (2010)

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Abstract (in Korean)

생체 모방 소자 및 비휘발성 메모리 소자로서 응용 가능한 HfO_2 기반 멤리스터와 TiO_2 기반 선택 소자 개발

4차 산업혁명을 위한 중요한 연구 분야 중 하나로 로봇 공학을 꼽을 수 있고, 그 중 특히 인간형 로봇(humanoid)는 4차 산업혁명의 핵심 키워드라고 할 수 있다. humanoid 연구의 발전을 위해서는 인공지능(artificial intelligence (AI)) 연구도 중요하지만, 그에 못지 않게 humanoid가 사람과 같이 외부 자극을 받아들일 수 있게 해줄, 인공수용기(artificial receptor)에 대한 연구도 이에 못지 않게 중요하다. 하지만, 최근 몇 년간 AI에 대한 연구는 급속도로 증가하고 있는 반면, 인공수용기에 대한 연구는 아직 미진한 실정으로, 인공수용기에 대한 연구가 더욱 활발히 수행될 필요가 있다. AI와 인공수용기가 효율적으로 구현되기 위해서는 기본적으로 고집적도 메모리 소자의 개발이 우선되어야 한다. 더군다나 현재의 메모리 제품은 약 10년 내에 그것의 집적도 향상의 한계에 직면할 것이라고 예상된다. 예를 들어, 현재 비휘발성 메모리 제품 시장의 상당 부분을 차지하고 있는 vertical NAND(V-NAND) 플래시 메모리는 약 100단의 제품이 개발 중에 있으며 메모리 셀 영역의 높이는 약 5μm이다. 휴대전화와 같은 전

자 제품에 메모리 칩을 장착하기 위해서는 칩 높이가 약 30μm를 넘지 않아야 한다. 이 30 μm 중 메모리 칩을 외부 환경으로부터 보호하는 패키징 공정에 약 15 μm 가 할애된다. 즉, 메모리 면적의 높이는 ~15 μm를 초과할 수 없다. ~100단 V-NAND 제품의 셀 영역 높이가 5μm인 점을 감안하면 V-NAND 제품의 층수 제한은 300층 정도라고 쉽게 예상할 수 있다. NAND 플래쉬 메모리의 개발 로드맵에 따르면 300단 V-NAND 제품은 약 10년 안에 개발될 것으로 예상된다. 즉, 약 10년 후에는 기존 메모리 제품의 메모리 집적도를 향상시키기가 어려울 확률이 높다. 그러므로, 차세대 메모리 장치의 상용화가 필요한 시점이다.

멤리스터는 크로스바 어레이(CBA)형태로 제작되었을 때, 단위 셀 크기는 4F2 이다. 여기서 F는 구현 가능한 최소 선폭을 나타낸다. 반면 DRAM, NAND, NOR 플래시메모리는 각각 $6F^2$, $5F^2$, $10F^2$ 의 단위 셀 크기를 갖고 있다. 즉, 멤리스터는 고집적 메모리 소자의 구현에 가장 적합한 소자라고 할 수 있다. 멤리스터는 1971년 추아 교수에 의해 그 개념이 소개된 후 2008년 휴렛팩커드(HP) 사에서 멤리스터 연구 내용을 발표한 것을 기점으로, 현재까지 큰 관심을 받으며 많은 연구가 진행되고 있다. 초기 연구들은 대부분 멤리스터의 메모리 소자로서의 연구에 초점이 맞춰졌던 반면, 근래에는 뉴로모픽 컴퓨팅, 생체 호환성 메모리 소자, 웨어러블 기기 등과 같은 다른 분야의 응용으로 연구 영역이 확장되고 있다.

본 논문의 첫 번째 파트에서, 위협적인 외부 자극에 반응하는 신경 세포인 통각수용기(nociceptor)의 특성이 Pt/HfO_2/TiN 멤리스터로 세계 최초로 구현 되었다. 통각수용기는 어떤 임계값 이상의 자극만 통증으로 느끼는 문턱 스위칭 특성을 보인다. Pt/HfO_2/TiN 멤리스터 또한 HfO2 막내에 존재하는 shallow trap sites에 전자가 trapping/detrapping 되는 현상으로부터 기인하는 문턱스위칭특성을 보인다. 이 소자로 통각수용기가 가지는 통각과민증, 이질통, 자연 치료, 통증 누적의 특성들이 모사될 수 있었다. HFO2 막내의 trap sites는 전도대로부터 약 0.7 eV 아래에 존재함을 본 연구에서 분석하였다. Pt와 TiN 전극 간의 일함수 차이에 의해 소자에 존재하게 되는 internal bias는, 깊이가 0.7 eV인 얕은 trap sites에 포획 되어 있던 전자들이 시간이 지남에 따라, 하부 TiN 전극 쪽으로 빠져나가게 한다. 이로 인해 통각수용기의 자연 치료 특성이 모사될 수 있다. 또한 본소자를 동작 시킬 시, 컴플라이언스 전류(compliance current) 값을 조절함으로서 trap sites에 포획되는 전자의 양을 조절할 수 있다. 이로 인해 통각과민증, 이질통, 통증 누적의 특성들이 구현될 수 있었다. 소자의 shallow trap sites와 internal bias가 통각수용기의 특성을 모사 가능하게 해주는 주요 요소임을 분석하였고, 이 두 요소가 결핍된 Ti/HfO_2/TiN 소자의 경우 통각수용기의 특성이 모사가 되지 않음 또한 확인되었다.

본 논문의 두 번째 파트에서는, 비휘발성 메모리 및 뉴로모픽 메모리 소자로서 응용 가능한 1 selector-1 resistor (1S1R) 소자를 개발하였다. 스퍼터

링 증착 조건을 변경 시켜 roughness와 비저항 등을 최적으로 엔지니어링 한 TiN 하부 전극층 위에 단원자증착법으로 TiO_2 막을 증착 후, Pt 상부 전극을 증착하여 Pt/TiO_2/TiN 선택 소자(selector)를 크로스바(cross bar) 형태로 제작하였다. 8nm 두께의 TiO_2 층을 갖는 최적화 된 선택소자는 외부 케이블에 의해 Pt/HfO_2 (2nm)/TiN bipolar resistance switching(BRS) 메모리 소자에 직렬로 연결되었다. 이렇게 연결된 1S1R 소자는 회부 회로나 트랜지스터에 의한 전류 제한이 없이도, 소자의 breakdown 이나 과도한 쓰기 동작 없이 안정적인 저항변화 메모리 거동을 보였다. 이는 선택소자와 메모리 소자와의 전류 레벨을 조절하여, 선택 소자에 의한 자가 전류 제한 효과를 유도 하였기 때문이다. 크로스바 어레이 (crossbar array (CBA))에서의 쓰기 마진(writing margin)은 선택된 셀을 쓰는 순간에 병렬적으로 연결된 선택되지 않은 셀의 원치 않는 지우기 동작이 일어나는 것을 고려하는 것으로서, 허용 가능한 크로스바 어레이의 크기를 제한하게 된다. 이것은 또한 셀간 연결되어 있는 라인의 저항과도 밀접한 연관이 있으며 라인 저항이 클 경우 라인에서 일어나는 전압 강하 때문에 허용가능한 어레이 크기는 더욱 제한되게 된다. 반도체 메모리 업계에서 널리 사용되는, 비저항이 낮은 텅스텐 전극을 본 소자의 전극으로 채택하였을 때 ~0.5 Mb의 용량 확보가 가능함을 HSPICE 시뮬레이션을 통해 입증하였다. 이는 1S1R 구조의 저항변화 소자의 상용화 가능성 및 뉴로모픽 메모리로의 응용이 가능함을 제시한 연구 결과이다.

본 논문의 세 번째 파트에서, 고집적화에 보다 유리한 수직 구조의 $Pt/HfO_2/TiN$ 메모리 소자를 디자인하고 제작하였다. 수직 구조 소자의 경우 메모리 셀의 측벽에서 저항변화 스위칭이 발생하며, 구조상 선택소자를 채택할 수 없다. 따라서 크로스바 어레이 형태에서 sneak 전류를 억제하기 위해서는, 메모리 소자가 자가 정류 또는 자가 비선형 특성을 가져야 한다. 이를 위해 TiN 하부 전극의 측벽에 HfO2 증착 후, 상부 전극 증착 전 plasma 처리를 하여 HfO2 막내에 deep trap sites의 생성을 유발하였다. 본 논문의 처음 파트에서 분석 되었듯이, HfO_2 막내에 존재하는 shallow trap sites에 의해 $Pt/HfO_2/TiN$ 소자는 문턱스위칭 거동을 보였다. 반면 plasma 처리에 의해 deep trap sites 형성이 유발된 $Pt/HfO_2/TiN$ 소자의 경우 안정적인 메모리 거동이 보임을 확인하였다. Pt 상부 전극에 양의 전압을 가했을 때 HfO_2와 TiN 사이에 형성된 quasi-ohmic contact으로 인해 TiN에서 HfO_2로 전자가 원활하게 주입되었다. 반면, Pt 상부전극에 음의 전압을 가할 시 Pt에서 HfO_2로의 전자 주입은 제한되었고, 이는 Pt와 HfO2 계면에 형성된 Schottky contact으로 인한 것으로서, 자가 정류 특성을 확보할 수 있었다. 2층의 수직 소자는 2 x 2 어레이로 제작되었으며, 총 8개 셀에서 동등 수준의 I-V 특성을 확인할 수 있었다. 선택한 셀만 고저항 상태(HRS)로 두고 나머지 셀은 모두 저저항 상태(LRS)로 설정한 소위 최악의 시나리오(worst scenario) 상태에서 sneak 전류의 방해 없이 선택된 셀의 HRS를 읽을 수 있었다. 즉, 소자의 자가정류 특성으로 인해 sneak

전류가 효과적으로 억제됨이 입증되었다. 실험적으로 획득한 I-V 그래프를 기반으로 허용 가능한 어레이 크기를 계산했을 때, 본 연구에서 개발한 2층 수직 소자에서 최대 약 0.5 Mb의 용량을 얻을 수 있는 것으로 확인되었다.

핵심어: 저항변화메모리, 멤리스터, 통각수용기, 선택소자, 수직소자, TiO_2, HfO_2

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